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ABSTRACT

ULTRATHIN SILICON WAFER BONDING: PHYSICS & APPLICATIONS

by
Michael H. Beggans

Ultrathin silicon wafer bonding is an emerging process that simplifies device fabrication, reduces manufacturing costs, increases yield, and allows the realization of novel devices. Ultrathin silicon wafers are between 3 and 200 microns thick with all the same properties of the thicker silicon wafers (greater than 300 microns) normally used by the semiconductor electronics industry. Wafer bonding is one technique by which multiple layers are formed.

In this thesis, the history and practice of wafer bonding is described and applied to the manufacture of microelectomechanical systems (MEMS) devices with layer thickness on the scale of microns. Handling and processing problems specific to ultrathin silicon wafers and their bonding are addressed and solved. A model that predicts the conformal nature of these flexible silicon wafers and its impact on bonding is developed in terms of a relatively new description of surface quality, the Power Spectral Density (PSD). A process for reducing surface roughness of silicon is elucidated and a model of this process is described. A method of detecting particle contamination in chemical baths and other processes using wafer bonding is detailed. A final section highlights some recent work that has used ultrathin silicon wafer bonding to fabricate MEMS devices that have reduced existing design complexity and made possible novel, and otherwise difficult to produce, sensors. A new fabrication process that can reduce the required time for "proof-of-principle" devices using ultrathin silicon wafers is also described.

ULTRATHIN SILICON WAFER BONDING: PHYSICS AND APPLICATIONS

by
Michael H. Beggans

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May 2001

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APPROVAL PAGE

ULTRATHIN SILICON WAFER BONDING: PHYSICS AND APPLICATIONS

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Michael H. Beggans, Dentcho I. Ivanov, Steven G. Fu, T. G. Digges, Jr., K. R. Farmer, "Optical pressure sensor head fabrication using ultra-thin silicon wafer anodic bonding,"
Proceedings of the 199 SPIE International Symposium on Design, Test and Microfabrication of MEMS/MOEMS, Paris France, March 1999.

M. Beggans, T. G. Digges, Jr. and K. R. Farmer,
"Oxidation effect on microcontamination and bondability of ultrathin silicon wafers,"
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In memory of my father, James P. Beggans, Jr.

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LIST OF DEFINITIONS

Bonding: General term denoting the joining of two, not necessarily different, materials which were initially separate. Similar terms include gluing, welding, soldering, splicing, etc. Usually not applied to situations where the materials are temporally attached and/or can be separated without special processing, tools, conditions, etc.

Wafer Bonding: General term for the bonding of two, not necessarily different, materials that are in the form of thin, circular disks.

Direct Bonding: General term denoting the joining of two, not necessarily different, materials without the use of an additional material, e.g. a glue. This term includes situations where processing-induced derivatives of either of the materials are included at the interface, such as oxide or nitride compounds. In practice, most material surfaces that have no foreign materials, such as adsorbed water, can only be formed under ultrahigh vacuum conditions.

Fusion Bonding: General term for the joining of two, not necessarily different, materials that implies that the connection is permanent. Various authors interchange **Fusion** and **Direct** bonding.

Indirect Bonding: General term denoting a joining of two, not necessarily different, materials by use of an additional material. In the literature, bonding of deposited thin films is sometimes referred to as direct or fusion bonding of the bulk materials. In these cases, the author denotes bonding between the deposited films as direct and that of the bulk materials as indirect.

Anodic Bonding: General term denoting the joining of two, not necessarily different, materials with the use of externally applied electric fields.

Thermal/Compression Bonding: General term denoting a joining of two, not necessarily different, materials requiring heat treatment and/or externally applied pressure.

Low-Temperature Bonding: General term for the joining of two, not necessarily different, materials requiring little or no heat treatment after contact to achieve a high mechanical strength connection (see **Anneal** below). Bonding is usually performed under ultrahigh vacuum (UHV) conditions and may be referred to as **UHV Bonding**.

III-IV Bonding: General term denoting the joining of two materials from the III and V columns of the periodic table.

LIST OF DEFINITIONS
(Continued)

Eutectic **Bonding**: General term denoting the joining of two, not necessarily different, materials whereby one or both materials diffuse into the (each) other.

Spontaneous **Bonding**: A joining of two, not necessarily different, materials characterized by a propensity for the two, initially separated, surfaces to come into intimate contact across the entire interface once intimate contact is achieved at a single location.

Hydrophilic **Bonding**: General term used to denote the joining of two, not necessarily different, materials whose surfaces display an affinity for water.

Hydrophobic **Bonding**: General term used to denote the joining of two, not necessarily different, materials whose surfaces display an aversion to water.

Glass-Frit **Bonding**: The joining of two, not necessarily different, materials using an intermediate material called glass-frit, which when cured, becomes a glass-like substance. Glass-frit is generally available in a liquid form that is solidified by the curing process.

Contact **Wave**: Term used to describe the propagation of intimate contact across the interface in **Spontaneous** **Bonding**. The term arose from the observation of the contrast difference between separated and contacted surfaces when bonding of silicon is observed with Infrared (IR) imaging and how that intensity edge moved across the wafer under spontaneous bonding conditions.

Anneal: Heat treatment of joined materials intended to increase the, usually mechanical, strength of the formed bond. In contrast, **Thermal/Compression** **Bonding** requires heat treatment to create the initial connection between two materials.

Cure/**Curing**: any of a number of specific processes in which the material properties of an intermediate layer, see **Indirect** **Bonding** above, are altered, e.g. to increase mechanical strength. Although heat treatment can be a curing process, as in **Anneal**, this term is usually reserved for when only the material properties of the intermediate layer are intended to change.

Ultrathin **Silicon** **Wafers**: Silicon wafers with thickness between 3 and 200 microns. Due to their thinness, these wafers exhibit more flexibility than normal thickness, 300 – 500 microns, silicon wafers, but otherwise retain all other properties such as mechanical strength, electrical resistance, absorption wavelengths, etc.

CHAPTER 1

INTRODUCTION

Ultrathin silicon wafer bonding can reduce fabrication complexity, increase yield and allow the manufacture of novel devices that are either not practical or possible with existing technologies. Paralleling the size-reduction trend in the electronics industry, researchers and industry have turned to miniaturizing mechanical devices. Present-day tools for manipulating structures and materials on the scale of microns or less are chiefly those that have been developed in response to the needs of the semiconductor electronics industry. Using planar technology, the fabrication of electronic devices through the selective deposition and removal of thin (typically ten to several thousand angstroms thick) material layers on a substrate, hundreds of devices can be produced at one time resulting in significant savings compared to the cost of producing each device separately.

However, planar technology suffers from increasing cost and difficulty as the number and thickness of layers increase. Devices designed to respond to or act upon our macroscopic world require much thicker layers than electronic devices, on the order of one to several hundred microns (one micron equals 10,000 angstroms). Producing such thick layers with semiconductor equipment is prohibitively expensive and difficult. Alternative methods suffer from repeatability, material quality and even cost issues. In this thesis, the author will demonstrate the production of miniature mechanical devices quickly, cheaply and reliably using ultrathin silicon wafers and the proven tools of the modern semiconductor industry. The incorporation of ultrathin silicon wafers into the planar manufacturing process is accomplished by wafer bonding, a technology that offers the promise of combining materials in ways not previously possible.

1.1 Scope of Research

This research has concentrated on the incorporation of ultrathin silicon wafers into the standard processing technologies of the modern semiconductor industry and the demonstration of the usefulness of ultrathin wafers in reducing fabrication complexity and cost and allowing novel device designs. Ultrathin silicon wafers, especially below 100 microns thick, are more fragile than standard (300 – 500 microns thick) wafers and direct processing, without modifications, can result in loss. They can be the building blocks out of which devices can be made, but the thinner the wafer, the more there is a need for structural support. Wafer bonding is a method for combining a structural support with the ultrathin wafer and adding subsequent layers. This thesis focuses on (1) indirect bonding using SU-8 photoresist, (2) direct bonding of ultrathin silicon to normal thickness, 300 – 500 microns, silicon wafers and (3) anodic bonding of ultrathin silicon wafers to Pyrex® substrates. The basic science of bonding is investigated to optimize the conditions for ultrathin silicon and to define its limitations. Modifications and solutions to handling for general processes and for manual and automated bonding were derived in the course of demonstrating successful ultrathin wafer bonding and its application to device fabrication.

It has been suggested that any material that can form an oxide can be bonded by direct bonding methods [1]. Silicon is one material that spontaneously forms an oxide in air. This thesis has concentrated on making the use of ultrathin silicon wafers a viable processing alternative that utilizes existing equipment and techniques with minimal modification. Rather than limiting the scope of application, this work has elucidated the dominating factors involved in bonding ultrathin silicon wafers to any other material. Their increased flexibility allows them to adhere to surfaces that are rougher than what

normal thickness wafers can bond. The thinner wafers, which can even be bent into cylindrical shapes in some cases, allow the possibility of bonding to curved surfaces. Ultrathin silicon wafer bonding not only improves aspects of device manufacture (see Chapter 6), but also allows combinations of materials in forms other than flat, planar surfaces. By concentrating on integrating ultrathin wafers into existing processes, this research provides both immediate benefits and insight into manufacturing techniques, such as bonding to curved surfaces, not imaginable with less flexible, normal thickness wafers.

1.2 Statement of Purpose

The purpose of the research presented here has been to (1) investigate the physical process of bonding ultrathin silicon wafers, (2) model the bonding mechanisms and limitations, (3) improve the bonding performance, (4) develop processing techniques scalable to production and (5) demonstrate the use of ultrathin silicon wafers in the fabrication of devices.

1.3 Dissertation Outline

The presentation is divided into seven chapters and one appendix. Chapter 1 is the introduction to this work and presents the problems and questions to be covered in later chapters. Chapter 2 is a review of wafer bonding, its history and current physical models, and bonded layer thinning techniques. Chapter 3 describes the initial difficulties in bonding ultrathin wafers, the investigation into the physical causes of poor bonding and the development of a physical model to explain why ultrathin silicon wafers are bondable under conditions that would prohibit bonding of standard thickness wafers. Chapter 4 details the methods developed to improve the quality of ultrathin silicon wafer bonding

and presents a model of the physical processes involved. Chapter 5 covers the processing procedures required by ultrathin silicon wafers for manual bonding and the use of automated equipment. Chapter 6 describes the new devices produced with ultrathin silicon wafer bonding, their production steps and their simulated and actual performance. Chapter 7 presents the conclusions drawn from this research and finishes with suggested future work. Appendix A contains the detailed processing parameters for bonding and annealing and the recipes used with the automated bonding equipment.

CHAPTER 2

REVIEW OF WAFER BONDING

2.1 Overview

This chapter outlines the history of direct and anodic bonding of silicon, the pioneering work and initial applications. The requirements, limitations, current theories and models of bonding are reviewed in some detail. Various methods of thinning bonded wafers are then described and contrasted as motivation for the use of ultrathin silicon wafers. The final section highlights the bonding requirements and theories that most apply to ultrathin wafers.

2.2 History of Bonding

The history of direct or fusion bonding can be dated back to at least 1792 when Desagulier showed that pressing two spheres of lead together resulted in strong adhesion. The lead spheres conformed enough for intimate contact only after plastic deformation of their rough surfaces due to large external pressure [2].

Bonding without using external pressure, spontaneous bonding, was reported in the early 1900's in Sweden in experiments with polished metal pieces used in a distance-measuring tool [3]. The spontaneous bonding of polished metal pieces may also have been known in Germany around the same time [2]. In 1936, Lord Rayleigh observed the adhesion of polished silica spheres and plates and calculated the interaction energy between them [4]. By whom and when the first deliberate bonding was performed is debatable, but the modern era of bonding has a slightly more definitive start, at least in the literature.

Although several companies may have already performed bonding in house prior to this publication, the modern age of direct or fusion bonding began in 1985 when Lasky *et al.* reported on the bonding of oxidized silicon wafers [3]. The wafer pairs were annealed at high temperature to increase their bond strength and one side thinned to form a Silicon-On-Insulator structure (SOI) [5]. At almost the same time, Shimbo *et al.* reported a similar process using wafers with no oxide layer, for replacement of thick epitaxial growth of silicon on silicon, used in applications for power devices [6]. Soon after, bonded silicon was used to fabricate a micromachined pressure sensor [7]. The demonstrated application for these three different types of devices was probably the spark for the enormous effort to date investigating bonding of many different materials. The reader interested in the detailed history of fusion bonding is referred to various review articles, conference proceedings, theses and books [1,3,8-14].

Anodic bonding was reported in 1969 by Wallis and Pommerantz for bonding metals and other materials to glass [15], but it was not until 1985, as indicated by the lack of publications prior, when Anthony [16] and Frye *et al.* [17] investigated anodic bonding for SOI applications, that widespread interest in the method developed. This may have been due to the fact that constituents of the glass can contaminate the material to which it is bonded [8] or that the method was patented [18]. The applicability of anodic bonding is restricted by the need for at least one material to be insulating. However, the comparative ease of anodic bonding combined with long-established processes for machining glass can be an advantage when the stringent roughness requirements of direct bonding cannot be satisfied [19]. The following sections highlight the limitations of direct and anodic bonding and indicate where one method is preferable to the other.

2.3 Bonding Requirements, Restrictions and Limitations

The major requirement for direct bonding is that the two interacting surfaces be smooth and conformal enough for attractive van der Waals forces to form a bond. The strength and quality of the final bond also depends upon conditions such as the preparation and chemistry of the two surfaces, their flatness and overall smoothness, and if there is any contamination at the interface. Other factors that may influence bond quality are material flexibility, lattice mismatches, thermal expansion mismatches and annealing conditions, and the application of voltage (for anodic bonding) or external pressure, and the environment in which the bond takes place. Three conditions, contact area (flatness and smoothness), surface preparation and contamination, dominate for all types of bonding and materials and will be discussed first. The other important factors, lattice mismatch, thermal expansion coefficients, etc., mentioned above, that have significant influence in specific contexts, but may not otherwise be applicable, will be described in the later sections. As an example, differences in thermal expansion coefficients are important when bonding two different materials, but are generally not a concern when bonding identical materials.

2.3.1 Contact Area (Flatness and Smoothness)

The flatness and smoothness of the two materials determines the total amount of contact between them. To illustrate this consider that the total contact between two rigid convex pieces is limited to a small area about the point(s) of contact, either at the center or on the edges as shown in Figure 2.1. The extent of the contact area will be determined by the flexibility of the materials, the strength of the surface forces pulling them together, and the amount of pressure exerted on the pair. As the radii of curvatures increase for the two

wafers, their surfaces become flatter and the contact area between them increases. The more they are in contact, the stronger they will bind together, if they are attracted to each other. One expects that if the two wafer surfaces perfectly match and are in the closest possible contact, then the bond strength between them will be greatest.

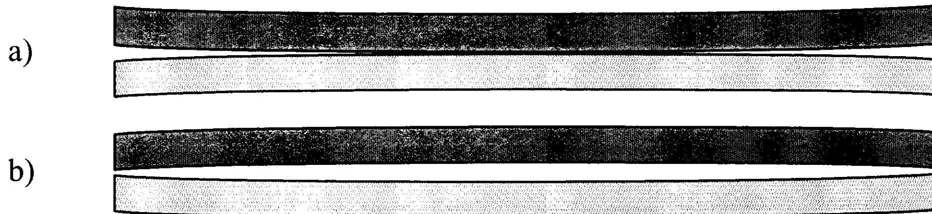


Figure 2.1. Bonding contact areas of two a) convex wafers and b) concave wafers (exaggerated curvatures).

In this thesis, roughness, defined as deviations from flatness, is divided into three regimes for typical silicon wafers with diameters of 5 to 20 centimeters. First is large-scale such as wafer bow (Figure 2.1) and waviness (akin to waves on the surface of water) and is on the order of centimeters (10^{-2} meters). The second regime consists of macroscopic features such as scratches, tooling marks, and other surface deformations on the scale of millimeters (10^{-3} meters). The third regime is often referred to as microroughness because the considered features are on the scale of microns (10^{-6} meters) and smaller. The relative importance of the three regimes to bonding is from large-scale (very important) to microroughness (important only after larger-scale roughness has been reduced). Only when the wafers are flat or their individual curvatures offset will small imperfections on the surface begin to determine the bond quality. The need for flat and smooth surfaces arises from the fact that van der Waals forces, the theorized sources of attraction, are short-range on a macroscopic scale.

Van der Waals forces arise from dipole interactions between molecules [2]. There are three types of van der Waals forces: a dipole-dipole force between two polarized molecules, a dipole-induced force between a polar and a nonpolar molecule and a "dispersion" force between two nonpolar molecules that arises due to a time variation in the distribution of charge. This dispersion force can be thought of in terms of the varying position of the orbiting electron in a hydrogen atom. The electron's motion exposes the positive charge of the nucleus to other atoms or molecules in a time-varying way. Van der Waals forces diminish rapidly as the distance between two molecules increases:

$$F \propto d^{-7}, \tag{1}$$

where F is the van der Waals force and d is the distance.

The overall bonding force between two surfaces will be the result of many-body interactions between surface molecules. Pair-wise summation of all the interatomic forces acting between all the atoms can be considered as a first order approximation. The resultant surface force depends upon the geometry of the bodies and decreases as the inverse third or second power. For flat plates the surface force is:

$$F \propto A/d^{3}, \tag{2}$$

where F is the surface force, A is the Hamaker constant and d is the distance. For spheres, the distance is raised to the second power [1]. The important point is that the strength of attraction falls off rapidly away from the surface. Therefore, to have strong bonding, the surfaces must be flat (or conformal) and smooth at all length scales.

The smaller the dominant roughness features are, the closer the wafer surfaces will be to each other and the greater the attractive force. Normal thickness (300 – 500 microns), standard silicon wafers used by the semiconductor electronics industry satisfy the flatness and smoothness requirements for van der Waals bonding [20]. Lack of bonding or poor bond quality usually arises from contamination of the surfaces by unwanted chemical species. However, chemical bonds can be longer range than van der Waals forces and modification of the termination chemistry of the wafer surface may compensate for some small-scale roughness. The next section details the importance of the chemical nature of the bonding surface, the processing factors that influence the surface chemistry and how these can be both a deterrent (contaminants) and a benefit (long range bonds).

2.3.2 Surface Chemistry

"Pure" surfaces, where no materials are present other than the bulk material, are usually achieved only under ultrahigh vacuum conditions (UHV). In the atmosphere are gases, dust, water vapor and other things such as airborne bacteria, viruses, etc. that can collect on an exposed surface. Once on the surface, some of these things, such as water, may react with the material to form a strong bond or a different chemical species. For example, water on steel produces an oxide called rust. These spontaneous reactions, and the presence of foreign matter, are generally a deterrent to performing repeatable processing and steps are taken to control the type and amount of contamination. The need for a controlled environment is why advanced semiconductor manufacturing is performed in cleanrooms, which filter the air for dust and other particulates, monitor and adjust the humidity and temperature, and generally limit the amount of foreign matter.

Even "factory-fresh" wafers, produced and packaged in cleanrooms, have some chemical species on the surfaces. For example, bare silicon in air spontaneously reacts with ambient water vapor (humidity) to form a silicon dioxide layer a few nanometers thick. Other contaminants can come from the shipping containers themselves [8]. The possibility of contamination during packaging and shipping is why all wafers are usually cleaned when first brought into a cleanroom. This is the first modification of the wafer's surface chemistry, but not the last, as all processing has some effect.

Some processing factors that impact wafer bonding are the methods of cleaning, the rinses (for wet, chemical baths, usually deionized (DI) water), the drying methods (spin dry, oven, Isopropal Alcohol (IPA), etc.) and the bonding environment (in air, vacuum, water, in a specific gas, etc.). A simple bond process consists of cleaning the wafers (when brought into the cleanroom), surface activation (which can be just the initial clean, see Section 2.3.2.3), contacting the materials and anneal at elevated temperatures. The flow chart in Figure 2.2 shows some of the general steps.

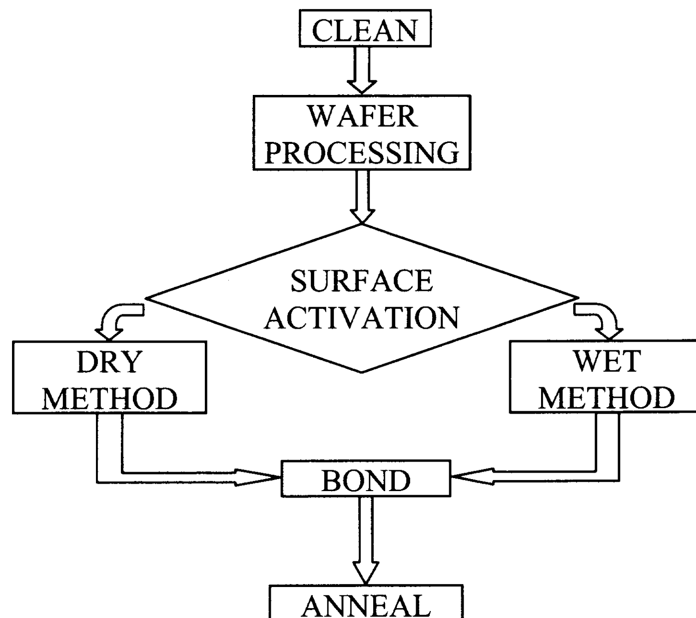


Figure 2.2. Flowchart of a bonding process.

The next few sections describe some of the more common cleaning, drying and surface activation methods. They are not meant to be exhaustive as there are continuous improvements and new methods being researched. Bond and anneal conditions are mentioned briefly as more details on these processes are given in Section 2.4.

2.3.2.1 Wafer Cleaning The bonding process begins with a cleaning of the wafers to remove dust particles and residual contamination from the shipping containers. Examples of typical wet cleans are RCA1 (Ammonia, Water, Peroxide, NH_4OH: H_2O: H_2O_2), SPM (Sulphuric acid Peroxide Mixture, H_2SO_4: H_2O_2) otherwise known as Piranha or P-clean, and hot nitric acid (HNO_3). The result of these cleans is a hydroxyl (OH) terminated, hydrophilic surface oxide (SiO_x) of varying quality and thickness (10 – 40 Å). Hydrophilic surfaces have an affinity to water as opposed to hydrophobic surfaces that repel water. Successful bonding can be performed with wafers immediately after drying or in the rinse water and is termed hydrophilic bonding. An observed increase in bondability arises through hydrogen bonding between Si-OH groups and between adsorbed water molecules on both wafer surfaces [9]. Storage in air gradually reduces the number of OH groups on the wafer surfaces and their positive effect on bonding. Hydrofluoric acid (HF) is also used in combination with these solutions to remove the native oxide and leaves a surface with H (hydrogen) and some F (fluorine) termination and with an aversion to water (hydrophobic). More detail is given in following section.

There are many variations of chemical concentrations and mixtures, temperatures, rinse and drying methods involved in the initial cleaning of wafers. New processes, such as ozone-rich water cleaning, are continually being developed [21]. For this thesis, SPM with deionized water (DI) rinse, and spin (thick wafers), or oven and filtered-gas blow

(ultrathin wafers) drying were used to clean all wafers. Details are given in Appendix A on the concentrations, temperatures, duration, etc. of all processes used in this thesis to bond ultrathin wafers. As the first step in the bonding process, the only requirement of the initial cleaning is to remove contaminants contracted from the packaging and shipping of the wafers. Table 1.1 shows some common cleaning solutions and their impact of the surface chemistry.

Table 1.1 Some chemical processes and the resulting surface termination [9].

Chemical Solution	Main chemical termination	Hydrophilic/phobic
RCA, SPM, HNO_3	OH	PHILIC
HF	H	PHOBIC
HF + RINSE	H	PHOBIC
HNO_3:HF	F	PHOBIC
HNO_3:HF + RINSE	OH	PHILIC

2.3.2.2 Native Oxide Removal In many cases, the native oxide on silicon wafers is either not of sufficient quality and thickness or is not desired at the bond interface. It can be removed and a new, high quality oxide grown, or other materials deposited. Removal of the native oxide and any oxide formed by cleaning is most easily done in Hydrofluoric Acid (HF) of varying concentrations. The resulting surface is primarily hydrogen (H) terminated with some fluorine (F) termination at steps and surface irregularities. The removal of oxide can increase the roughness of the wafer surface in solutions where there are oxidizing species such as peroxide and water. This increased roughness is more pronounced in lower concentrations of HF due to the larger number of oxidizing species [22]. Spontaneous bonding of hydrophobic silicon wafers has been observed when the usual water rinse is omitted [9]. If the wafer is rinsed in water, the fluorine is exchanged with OH and bonding is reportedly more difficult.

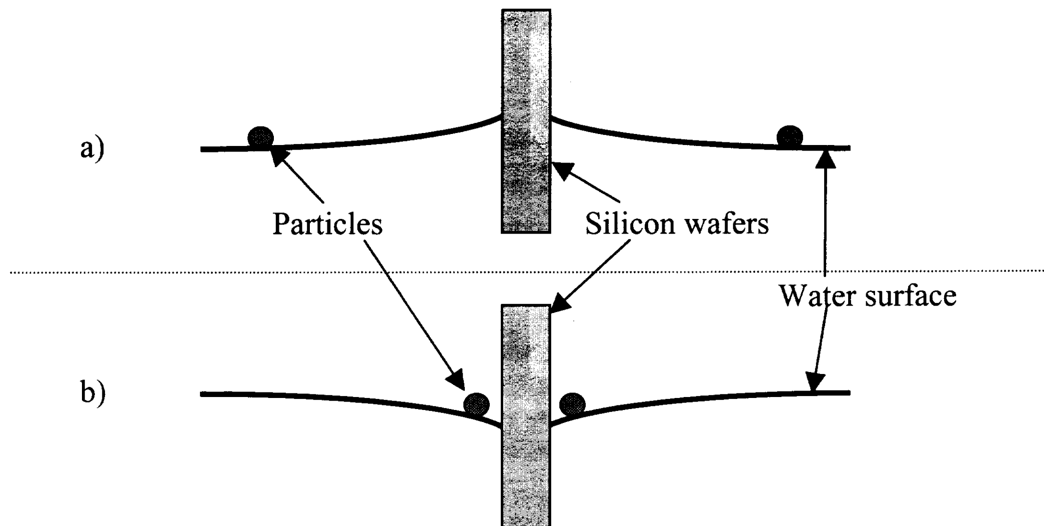


Figure 2.3. Effect on water surface and particles from insertion into the bath of a) hydrophilic and b) hydrophobic wafer.

The increased difficulty in bonding rinsed wafers may be due in part to the reaction of the rinse water surface to a hydrophobic wafer. Figure 2.3 shows how the rinse water surface might react to hydrophobic and hydrophilic wafers and what possible movement particles on the water surface may have. The differing effects are due to the attraction (repulsion) of the water to (from) the hydrophilic (hydrophobic) wafer surface. The electrical charge of the wafers and the particles are assumed to be neutral and motion of the particles is considered due to gravity and surface tension alone.

The above factors, nearly pure van der Waals bonding, possible increased roughness and greater risk of particle contamination, make achieving high quality hydrophobic bonds more difficult than hydrophilic.

The effect of hydrophilicity on the bonding of wafers has been studied extensively and various chemical solutions have been examined [23-26]. Hydrophilic surfaces have been shown to increase bondability and hydrophobic surfaces can make bonding more difficult. The effect on bonding is due to the differences in the chemical makeup of the

wafer surface. Hydrophilic surfaces can form bridging networks of adsorbed water that can overcome small roughness features. Deliberate alteration of the chemical termination species of wafers is called surface activation and some alternate methods are described below.

2.3.2.3 Surface Activation Activation methods are employed to improve bond quality or decrease the required anneal temperatures for achieving high bond strengths. Plasma treatments have been shown to yield high strength bonds at low temperatures, ≥ 400 °C for SF_6 and CHF_3 or ≤ 400 °C for O_2 plasmas [27]. Plasma treatments are often used in what is generally called low temperature wafer bonding (due to decreased anneal temperatures) and can be applied to many materials other than silicon [28]. Silicon wafers bonded are typically annealed at more than 800 °C and up to 1200 °C for the highest bond strengths. Diffusion of implanted species and degradation of metal interconnects in microelectronic circuits effectively limit their thermal processing to about 400 °C. The high bond strengths achieved at low annealing temperatures allows processed wafers with electronic circuitry to be bonded. The study of plasmas for surface activation is relatively new and much work is continuing in this area [29-33]. In this thesis, activation was achieved by recleaning the wafers in SPM after any processing such as oxide growth or wafer etching. This left the wafer surfaces hydrophilic and with a thin layer of oxide between otherwise bare wafers.

2.3.2.4 Other Chemical Processing Methods Other investigations have concentrated on preventing bubbles from forming during anneal and reducing the roughening effect of various cleaning and surface activating solutions [34, 35].

2.3.2.5 Bond and Anneal Conditions The environment under which the wafers are contacted can also be manipulated to improve bond quality and alter the surface chemistry. Often silicon wafer bonding is performed at room temperature in air. As noted previously, the surfaces will most likely contain adsorbed water and, in bonding, gases may be trapped at the interface. The presence of water vapor or air can be detrimental to or have a large impact on the performance of devices [36]. In cases where trapped gases are undesirable, the contacting of the wafers is best done in vacuum. In vacuum, the amount of adsorbed water is reduced along with the positive effect of hydrophilic surfaces on bondability, which may make the initial bonding slightly more difficult. If the wafers are also cleaned in the vacuum chamber, the possibility of contamination by particles is greatly reduced. Bombarding the surface with ions, such as Ar^{+2}, can etch away the top layer, cleaning the wafer and leaving a "pure" surface. The bonding of "pure" surfaces can reduce the required anneal temperature for high strength [37]. High temperature anneals are required when the silicon surface has other molecules upon it that must diffuse away from the interface before silicon-to-silicon bonds can form (see Section 2.4). Ultrahigh vacuum bonding, with "pure" surfaces, has shown promise in bonding dissimilar materials with large differences in thermal expansion coefficients, which prevents high anneal temperatures [28, 38-41].

The anneal is the final step of the bonding process. The elevated temperatures involved bring about a series of chemical reactions that strengthen the bonds between the wafer surfaces. It is usually performed at high temperature in a furnace with a controlled atmosphere of nitrogen or other pure gases. The details will be left until Section 2.4.

2.3.3 Contamination

The most difficult part of bonding any two materials together is preventing dust and other airborne particulates from collecting on the surfaces to be mated. Cleans, plasma treatments and bonding in vacuum all help reduce the presence of unwanted material. Under infrared (IR) imaging, particles as small as 0.25 microns show gaps as interference fringes produced by the separation of the wafers of over ¼ wavelength (when viewing at 1 micron). A cleanroom with standard HEPA® filters removes particles down to ~ 0.3 microns. The cleanroom at NJIT is rated class 10 for 0.3 microns particles.

Micro-cleanroom environments designed specifically for wafer bonding use an enclosed chamber with a cleaning solution injected between closely spaced, rotating wafers. The solution removes particles from the surfaces and the wafers are bonded in place. Figure 2.4 shows a diagram of the micro-cleanroom setup. One of the largest sources of particle contamination is the operator, and the methods employed to reduce particle contamination are detailed in the discussion of ultrathin silicon wafer bonding (Chapter 3) and handling (Chapter 5).

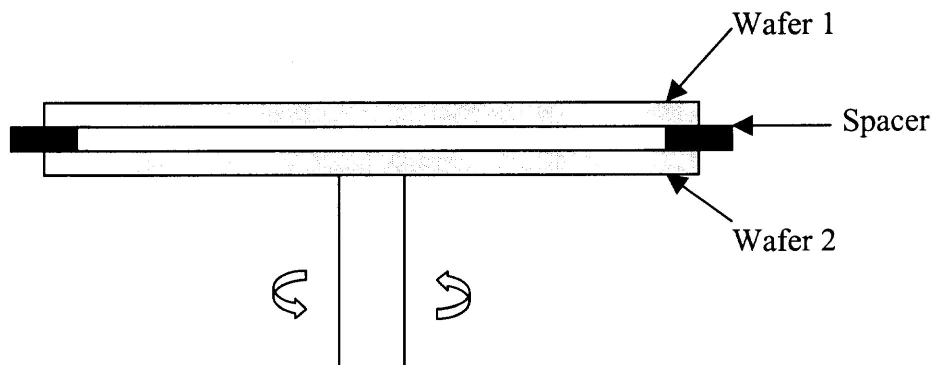


Figure 2.4. Diagram of the micro-cleanroom setup [2].

2.3.4 Other Bonding Requirements

The next most important consideration for bonding is the flexibility of the materials. If the surfaces are not perfectly flat and smooth, the wafers must be able to conform to each other to allow for intimate contact. Stiffness varies from material to material, but, in general, flexibility decreases as the thickness increases. For bonding, this would require that the wafers must be flatter and less rough as their thickness increases [42, 43].

For bonding of dissimilar materials, the effects of crystalline lattice mismatch and thermal expansion coefficients play a dominating role. If the mismatch of lattices is greater than ~ 1 %, interface stress can prevent adhesion of the material surfaces [2]. Any mismatch will introduce strain at the interface and can lead to dislocations and defects. Lattice mismatch can also be found in bonds between wafers of identical material but different crystallographic orientations.

Thermal expansion differences can cause separation under annealing conditions or afterwards when the pair is cooled. Even if the materials do not separate, there will be residual strain at the interface after heat treatments. The low temperature bonding approach is pursued partly to overcome this problem in bonding materials with large thermal expansion mismatches. Anodic bonding, generally performed at elevated temperatures, is often done with Corning Pyrex® code 7740 because it has a thermal expansion coefficient very close to that of silicon.

Most remaining restrictions depend upon the type of bonding to be performed. Anodic bonding requires one material to be at least semi-insulating. The insulating layer causes a buildup of space charge at the interface that drives the surfaces together through electrostatic attraction. At an applied voltage of 1 kV, the electric field strength can reach 10^6 V/cm, corresponding to a pressure of ~ 100 psi (pounds per square inch) [15,

17]. This large pressure can overcome mechanical mismatch, cause plastic deformation of the surface and therefore, allow bonding to far rougher surfaces than otherwise possible. External pressure may help surfaces temporarily conform to large-scale roughness such as wafer bow and waviness, but without plastic deformation of surface features, there will be residual stress at the interface. This stress can result in wafers separating after the external pressure is removed. The extent to which external pressure will influence bonding will depend upon the material (plastic deformation) and the nature of the roughness, the width and height of the asperities (see Sections 2.4 and 3.3).

Eutectic bonding requires that at least one material be able to diffuse into the other. Thermal compression bonding may utilize a third material that imposes other constraints, such as nonuniformity of the added material, temperature and environmental conditions that can have adverse effects on this "glue," and the process of "curing" this intermediate bonding material. The limitations and conditions of these specific processes are broader than can be incorporated in this thesis and so attention is reserved for those theories that may explain the general properties of direct and anodic bonding.

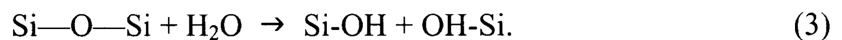
2.4 Bond Theories

The following sections illustrate the current theories on the physical, chemical, mechanical and, for anodic bonding, electrochemical reactions that take place in the bond process. The first two sections, bonding chemistry and mechanical models, apply mainly to direct bonding while the third is concerned with anodic bonding. A final section will recap the major theoretical themes, some details that are unique for ultrathin silicon, and how these properties are expected to affect wafer bonding.

2.4.1 Bonding Chemistry

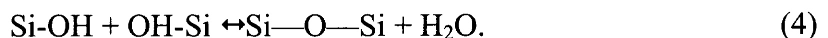
Hydrophilic and hydrophobic surfaces have been shown to bond differently. The different chemical species for hydrophilic and hydrophobic surfaces require that different mechanisms are responsible for achieving high bond strengths. As mentioned in section 2.3.2.1, hydrophilic surfaces are primarily OH terminated while hydrophobic surfaces are primarily H terminated. Additionally, there is usually adsorbed water on the surfaces of hydrophilic wafers, but not on hydrophobic wafers.

2.4.1.1 Hydrophilic Bonding [44] Bonding and annealing of hydrophilic silicon wafers appears to be a four step process based upon measurement of the surface energy before and after heat treatment. The first region extends from room temperature to 110 °C. The bond strength is a result of hydrogen bonding between adsorbed water triplets. The water triplets on each wafer surface can act over a distance of ~ 10 Å, allowing bonding of wafers with ~ 5 Å roughness. The presence of water is theorized to crack the Si—O—Si bonds on both wafer surfaces resulting in more Si-OH extending into the interface region. The increased number of Si-OH bonds allows the adsorption of more water molecules. The proposed reaction is:



$$\text{Si—O—Si} + H_2O \rightarrow \text{Si-OH} + \text{OH-Si.} \quad (3)$$

Between 110 °C and 150 °C, the silanol groups (Si-OH) can polymerize according to the reaction:



$$\text{Si-OH} + \text{OH-Si} \leftrightarrow \text{Si—O—Si} + H_2O. \quad (4)$$

If the water is removed, then strong Si—O—Si bonds can form between the wafer surfaces. Above 110 °C, water is presumed to diffuse from the interface to the wafer edge, but some may diffuse through the oxide and react with at the silicon surface to form additional silicon dioxide and hydrogen. This needed diffusion is one reason for the high temperatures involved in annealing silicon wafers. Bonding done in vacuum has much less adsorbed water and other materials and requires lower anneal temperatures.

From 150 °C to 800 °C the bond energy is almost constant; implying that almost all silanol groups have converted to siloxane bonds at ~ 150 °C according to equation (4). The surface energy is then a function of the real contact area between wafers. Since no wafer has a perfectly smooth surface, the bond strength of the interface cannot reach that of bulk silicon.

From 800 °C up, the flow of silicon dioxide is the most likely candidate for explaining increased bond strength. This flow can fill in any micro voids between the wafer surfaces. In hydrophobic bonding, which has no oxide, the bonded pair reaches near bulk strength across the interface at ~ 800 °C. Bond strength is usually measured by inserting a razor blade into the bonded interface and measuring the length of the resulting wafer separation [10]. Above 800 °C, the bond strength is such that 3-dimensional fracture across the interface results from attempting to insert the razor blade.

2.4.1.2 Hydrophobic Bonding [9] Without the adsorbed water of hydrophilic bonding, hydrophobic bonding is less forgiving of surface roughness and is initially more difficult. The hydrophobic surface is terminated mainly by H, with some F or OH (if water rinsed) termination at surface defects. Particle contamination from the water rinse may be the

cause of conflicting results on bonding of HF treated wafers (See Figure 2.3 in Section 2.3.2.2). Studies of differing concentrations of F and OH termination have revealed no significant change in bond strength at room temperature. The proposed bonding mechanism is therefore nearly pure van der Waals bonding with some possible hydrogen bonding between Si-H, Si-F or Si-OH [9]. Because no water or hydroxol groups exist between the wafers, there is no need for these molecules to dissociate and diffuse from the interface.

Hydrophobic bonded wafers anneal in apparently only two steps. The interface bond of a hydrophobic wafer pair shows a sharp increase in strength between 300 and 400 °C. This bond energy is greater at 400 °C than bonded hydrophilic wafers. The bond energy continues to increase up to about 800 °C where it saturates at near-bulk strength. The proposed reaction is a formation of ≡Si—Si≡ bridges across the gap between wafers and a diffusion of hydrogen gas out of the interface.

2.4.2 Bonding Mechanics

Successful bonding requires the conforming of surfaces to achieve intimate contact. Hydrophilic bonding can overcome ~ 5 Å roughness according to the theory of adsorbed water layers (see Section 2.4.1.1) without deformation of surface asperities or the wafer itself. Most wafers, however, are not perfectly flat. The successful mating of two non-flat wafers or wafers with trapped particles or surface features will require physical accommodation by elastic distortion, plastic deformation or mass transport.

Mass transport is the suspected reason for increased bond strength of hydrophilic wafers annealed at > 800 °C, but this effect is not significant at room temperature. For brittle materials, like silicon, plastic deformation is not possible. Any deformation of a

surface feature will result in either fracture or, upon removal of the external pressure, complete restoration. Therefore, elastic distortion is assumed to be the mechanism by which silicon wafers conform to surface imperfections. The following derivation is taken from Yu and Suo in Reference [43].

The surfaces to be bonded are characterized by surface tensions (energies) that can be attractive or repulsive. The interface can also have tension (energy), acquired during the bonding process. Bonding is achieved when the two surface energies exceed that of the interface energy and reduce the overall free energy. This reduction is known as the Dupré work of adhesion and can be formulated as:

$$\Gamma = \gamma_1 + \gamma_2 - \gamma_{12}, \tag{5}$$

where γ_1, γ_2 denote the surface tensions and γ_{12} is the interface tension. The necessary condition for bonding is that $\Gamma > 0$. For perfectly flat or conformal surfaces, the interface energy is close to zero, but for rough surfaces, γ_{12} acquires the energy from the elastic deformation needed to achieve contact across gaps. If the gap (misfit) is large, the interface energy will be greater than is possible for bonding.

Figure 2.5 illustrates the bonding of two rough surfaces and the possible outcomes.Successful bonding is illustrated in Figure 2.5 (c). In this case, the surface energy of the two wafers was greater than the energy needed to close the gaps. In Figure 2.5 (d), the available surface energy is less than required to close the gaps. Whether or not a gap completely closes will depend upon the dimensions of the gap and material properties.

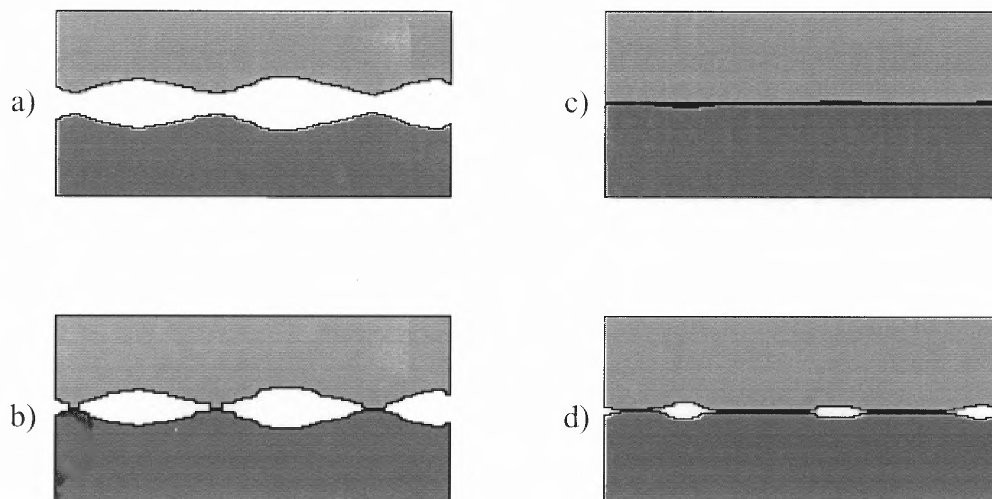


Figure 2.5. a) Two wafers with sinusoidal surface imperfections brought into contact, b), with resulting interface either c) completely closed or d) with some remaining gaps.

The salient features of the problem are depicted in Figure 2.6. The gap is assumed sinusoidal in the x and y directions (parallel to the wafer surface) with a width of length, L and a total gap height of 2H. The wafer thicknesses are denoted t_1 and t_2.

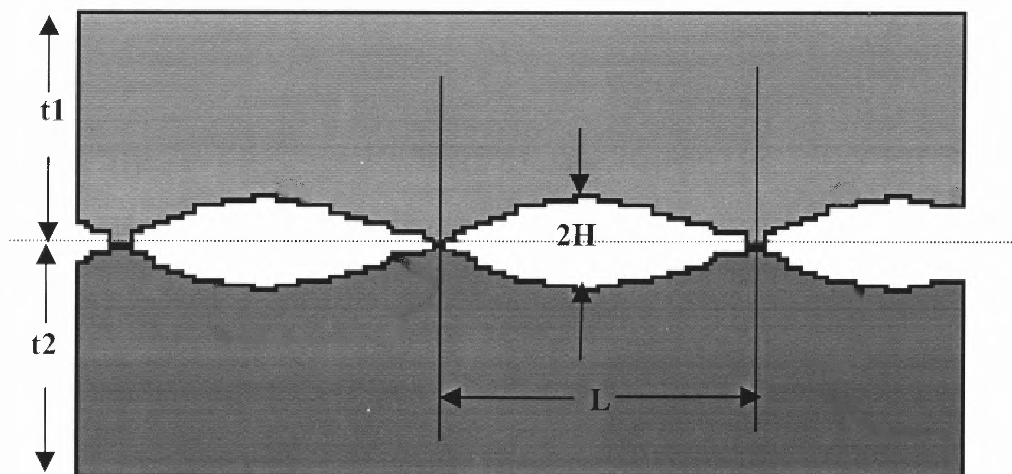


Figure 2.6. Sinusoidal gap of length L and width 2H between two wafers of thickness, t_1 and t_2.

If the ratio H/L is taken to be so small that linear elastic theory applies then the displacement field will obey Navier's equation, with $(u_1,u_2,u_3) = (u,v,w)$:

$$(1-2\nu)u_{i,jj} + u_{j,ji} = 0, \tag{6}$$

and the stresses, σ_{ij}, will relate to the displacements as:

$$\sigma_{i,j} = \frac{E}{1+\nu}\cdot\left[\frac{1}{2}\cdot\left(u_{i,j} + u_{j,i}\right) + \frac{\nu}{1-2\cdot\nu}\cdot u_{k,k}\cdot\delta_{i,j}\right], \tag{7}$$

where E is Young's modulus, ν is Poisson's ratio, $\delta_{i,j} = 1$ when $i = j$, and $\delta_{i,j} = 0$ if $i \neq j$. The elastic constants, E and ν, can be different values for bonding of dissimilar wafers.

Assuming the gap is sinusoidal, the displacement field is posited to take the form:

$$\begin{aligned} u &= \sin(kx)\cos(ky)\,f(kz), \\ v &= \cos(kx)\sin(ky)\,f(kz), \\ w &= w_0 + \cos(kx)\cos(ky)g(kz), \end{aligned} \tag{8}$$

where $k = 2\pi/L$ and w_0 represents a rigid body translation. Substitution of equation (8) into equation (6) yields the functions, f and g. These equations turn out to be ordinary differential equations of constant coefficients. The coefficients of these equations are determined by the boundary conditions.

Assuming the following boundary conditions: (i) on the free surface ($z = t_1$) the normal stress vanishes, (ii) on the free surface ($z = t_1$) the shear stress vanishes, (iii) on the interface ($z = 0$) the shear stress vanishes, and (iv) on the interface ($z = 0$) the vertical displacement is:

$$w_1 = -\frac{H_1}{2}\cdot(1 + \cos(kx)\cdot\cos(ky)) \quad , \tag{9}$$

where H_1 is the gap height on wafer 1.

From these conditions, the coefficients of the functions, f and g, and the normal stress at the interface are derived:

$$\sigma_{zz} = \frac{k\cdot H}{\sqrt{2}}\cdot\cos(kx)\cdot\cos(ky)\cdot\left(\frac{1}{\overline{E_1}\cdot I(kt_1)} + \frac{1}{\overline{E_2}\cdot I(kt_2)}\right)^{-1} \quad , \tag{10}$$

where

$$\overline{E} = \frac{E}{1 - v^2} \quad , \tag{11}$$

and

$$I(\alpha) = \frac{e^{2\cdot\sqrt{2}\cdot\alpha} + e^{-2\cdot\sqrt{2}\cdot\alpha} - 2 - 8\cdot\alpha^2}{e^{2\cdot\sqrt{2}\cdot\alpha} - e^{-2\cdot\sqrt{2}\cdot\alpha} + 4\cdot\sqrt{2}\cdot\alpha} \quad . \tag{12}$$

The elastic energy per period of the bonded interface is:

$$U=\frac{1}{2}\cdot\int_0^L\int_0^L (w_2-w_1)\cdot\sigma_{zz}\,dx\,dy \qquad (13)$$

where

$$w_2-w_1=H\cdot(1+\cos(kx)\cdot\cos(ky)) \qquad (14)$$

and σ_{zz} is given in equation (10).

Complete bonding occurs when the free energy change per period of the bonded interface is negative:

$$U-\Gamma\cdot L^2<0 \qquad (15)$$

where Γ is given in equation (5). Integrating equation (13) using equations (10) and (14) and substituting the results into equation (15) results in an expression determining the critical condition for bonding.

This condition is found to be:

$$\frac{(H_c)^2}{\Gamma\cdot L}=\frac{4\cdot\sqrt{2}}{\pi}\cdot\left(\frac{1}{\overline{E_1}\cdot I(k\cdot t_1)}+\frac{1}{\overline{E_2}\cdot I(k\cdot t_2)}\right). \qquad (16)$$

In equation (16) above, the critical misfit amplitude, H_c, is the maximum height of a surface feature with a characteristic length of L, for which the available surface energy, ΓL^2, is greater than the energy required for elastic deformation, U (equation (15)).

Three cases deserve consideration. The first two cases concern the limit where the thickness of the two wafers is much greater than the misfit wavelength, $L << t_1, t_2$. For dissimilar materials, the elastic constants are different and:

$$H_c = 1.34 \cdot \left[\Gamma \cdot L \cdot \left(\frac{1}{E_1} + \frac{1}{E_2} \right) \right]^{\frac{1}{2}}, \tag{17}$$

due to the limit $I(\alpha) \rightarrow 1$ as $\alpha \rightarrow \infty$. The misfit gap is accommodated mainly by the more compliant wafer and the stiffer wafer has little influence. If the two wafers have identical elastic constants, this expression simplifies to

$$H_c = 1.90 \cdot \sqrt{\frac{\Gamma \cdot L}{E}}, \tag{18}$$

which has the same form as given by Tong and Gösele but with a different constant [42].

A final consideration is when the thickness of identical wafers is much less than the misfit wavelength, $t_1 = t_2 = t << L$. This is true when considering roughness features such as wafer bow and waviness that are on the order of centimeters. Typical silicon wafers are 0.5 mm thick.

The critical bonding condition in this case is then,

$$H_c = 0.176 \cdot \sqrt{\frac{\Gamma \cdot L^4}{\bar{E} \cdot t^3}}, \tag{19}$$

which is the same result, derived from thin plate theory, found by Tong and Gösele [42].

The authors, Yu and Suo, Reference [43], note that the preceding theory assumes that there is no residual shear stress at the interface and that the misfit of the wafers has only one wavelength. For crystalline materials of different lattice constants, the shear stress may not vanish and should be considered in the determination of the coefficients of the functions f and g in equation (8).

The authors also note that the surface of a wafer rarely has only one misfit wavelength. One could obtain the misfit magnitude as a function of roughness frequency, or k as in equation (8), by performing a Fourier Transform of a surface profile, calculate the stress field for each frequency using the above procedure and find the total stress by linear superposition. They note that the roughness feature with the largest H^2/L ratio will require the most energy to overcome and that the critical condition for this one frequency might be used as an approximate limit for overall bonding.

The use of Power Spectral Density (PSD) or Fourier transform of surface roughness measurements has grown in recent years due to the fact that it retains the two dimensional information and is independent of the bandwidth of the device used. RMS (root-mean-square) roughness figures are often reported to indicate the smoothness of wafer surfaces but this statistical calculation depends strongly on the size of the area

scanned and the bandwidth limitations of the instrument. The nature of the roughness is also lost as two different scale features can result in the same rms roughness value, depending upon their relative magnitudes. Increasingly, surface finishes are reported as a power spectral density function to avoid the problems associated with comparing rms values. In Section 4.1.3, the details of the derivation of a PSD plot from surface height data are elucidated. Its limitations are also discussed. For now, the important feature of the PSD is that the plot is of the surface height squared per unit wavelength (power) versus frequency (inverse length of a periodic roughness feature).

Roberds and Farrens have developed an empirical limit for bondable surfaces, based on PSD calculations from atomic force microscopy (AFM) scans [45]:

$$P = 100\, f^{-2.5}, \tag{20}$$

where P is the roughness power in units of micron-$Å^2$ and f, the frequency in microns^{-1}. Silicon wafers with PSD measurements generally below this line bonded while those with greater roughness did not. It is not known at this time whether or not this empirical limit extends beyond the bandwidth range of AFM. The AFM instrumentation and operating procedures are discussed in detail in Chapter 3.

2.4.3 Anodic Bonding [46]

If at least one material is insulating, an applied voltage across the wafer stack may help in bonding. The mechanics are not fully known, even for silicon to glass, but the process generally involves elevated temperatures (300–500°C) and high voltages (400–1000 V).

Because of the elevated temperatures, materials with similar thermal coefficients of expansion (TCE) should be used to avoid high interface stress, which could lead to cracking or debonding, upon cooling down.

With its closely matching TCE, Pyrex® code 7740 is commonly bonded to silicon. Pyrex® consists of about 80% SiO_2, 13% B_2O_3, 3.5% Na_2O, and 2.35% Fe_2O_3, Al_2O_3. The large voltage applied creates an electrostatic field in the gap between wafers. At the elevated temperatures commonly used, sodium ions are mobile and tend to be drawn away from the interface if the silicon is biased positive with respect to the glass. This results in a space charge region at the interface that promotes attraction to the silicon surface.

The bonding chemistry is understood less well. The high electrical field is assumed to cause oxygen ions to leave the glass and react with silicon to form an observed oxide at the interface. This assumption is strengthened by the fact that anodic bonding of silicon and Pyrex® is not completely reversible. If the bias is made such that the glass is now positive with respect to the silicon, the oxide layer does not completely dissociate and the wafers remain bonded.

Because of the high electric field and resulting space charge region that promotes bonding, surface roughness and flatness is less critical than for direct wafer bonding. Similarly, particle contamination can be more easily accommodated.

2.4.4 Recap

Wafer bonding depends upon flatness and smoothness of the surfaces to achieve intimate contact and adhesion due to van der Waals forces and chemical bonds. Contamination by foreign matter generally deters bonding, but deliberate manipulation of the termination

species can help by forming bridging networks of molecules. Thermal and lattice constant mismatch should be minimized to avoid stress at the interface that can deter bonding. Increased material flexibility reduces the requirements on flatness and roughness. This is expected to be the main difference between bonding of ultrathin and normal thickness silicon wafers.

Below about 100 microns in thickness, ultrathin silicon wafers are flexible enough to accommodate wafer bow on the order of millimeters. Ten microns thick wafers can conform to curved surfaces and can even be rolled into a tube. This increasing flexibility will limit the longer roughness wavelengths that affect bonding. In other words, wafer bow, with wavelengths on the order of centimeters, is less important when bonding flexible ultrathin silicon wafers below 100 microns thickness and may not be relevant at all for wafers approaching 10 microns thickness. As the wafer gets thinner, the roughness scale that has an effect on bonding might be expected to decrease from wafer bow down to large scratches, depending upon how much the wafer can conform. In Chapter 3, the relationship between roughness and wafer thickness for bonding will be shown.

2.5 Wafer Thinning

In this section, the various methods for producing thin silicon layers will be reviewed. The limitations of each method will be highlighted as motivation for studying and improving the bonding of ultrathin silicon wafers. There are three main techniques for producing thin silicon layers: mechanical thinning, chemical etching and layer transfer. Since many universities and companies are actively pursuing research in this area, some recent refinements of these methods and new processes will be highlighted.

A leading interest in wafer thinning comes from the semiconductor electronics industry and is for Silicon-On-Insulator (SOI) wafers or structures. A buried insulator layer under an active silicon layer greatly reduces stray capacitance and allows for higher device densities [47]. A typical SOI schematic is shown in Figure 2.7. An oxide layer is sandwiched between the active and substrate layers. This oxide layer can also be used as a sacrificial layer for MEMS device manufacturing. For MEMS, the active silicon layer is typically several microns thick for mechanical robustness. For the microelectronics industry, this layer is typically 0.1- 0.05 microns.

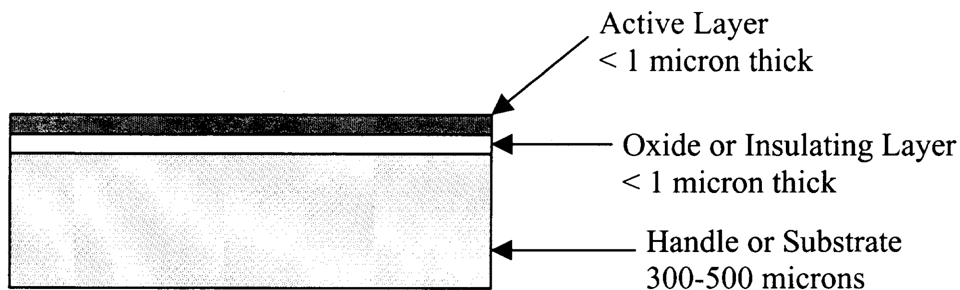


Figure 2.7. Schematic of a typical SOI wafer.

A simpler configuration for a SOI wafer involves only two layers made by either bonding directly to, or by growing a layer on, an insulating substrate. Silicon-On-Sapphire (SOS) is one example of an epitaxial layer grown directly on an insulator. A silicon wafer bonded to glass is another example of a two-layer SOI. SOS is the earliest SOI material design and, despite the difficulty in obtaining defect-free epitaxial silicon and its expense, is still used for applications where radiation hardness is essential [48].

2.5.1 Mechanical Thinning

Perhaps the most direct method of producing thin silicon layers is to bond oxidized wafers and lap, grind and polish one wafer to a desired thickness. This necessitates that the bond strength of the wafers is great enough to withstand the forces involved in such rough processes. Lapping, grinding and mechanical polishing introduces subsurface damage as deep as 25 microns. Chemical-mechanical polishing (CMP) removes this damaged layer, but reduces the overall flatness of the wafer. Presently, this technique can produce silicon layers of generally greater than one micron thickness with a uniformity of ± 0.5 microns. This level of uniformity is achieved by use of single-wafer polishers [8].

The main drawbacks to this technique are process repeatability, large thickness, need for very strong bonds, single wafer polishing and cost. Patterned wafers, or wafers with structures susceptible to damage, may not have the bond strength or robustness to withstand mechanical thinning. Variations in layer thickness and thickness uniformity between wafers are other drawbacks. Finally, although CMP has become an accepted process in fabrication of multi-layer devices, the methods of lapping, grinding and mechanical polishing are not "clean" and may have to be done outside a cleanroom where other processing is performed.

Methods of producing very thin, ~ 1 micron or less, silicon layers by polishing require a stop layer with a low rate of removal compared to silicon. This layer is either implanted or formed by depositing material over etched pits in the silicon surface with subsequent removal of material from around those pits. After bonding, the wafer is polished to the stop layer. Implantation methods can result in a whole, thin silicon layer

about as thick as the implantation level was deep. The filled-pit method leaves silicon islands, separated by the polish-stop material, about as thick as the depth of the initial etched pits. The process flow for filled-pit polish stops is shown in Figure 2.8. Because the polishing pad is not perfectly rigid, the thickness of the silicon islands depends greatly on their size or the distance between polish-stop materials. The limitations of implantation techniques are discussed in more detail in Section 2.5.3, but these include damage to the silicon device layer and the need for a final polish.

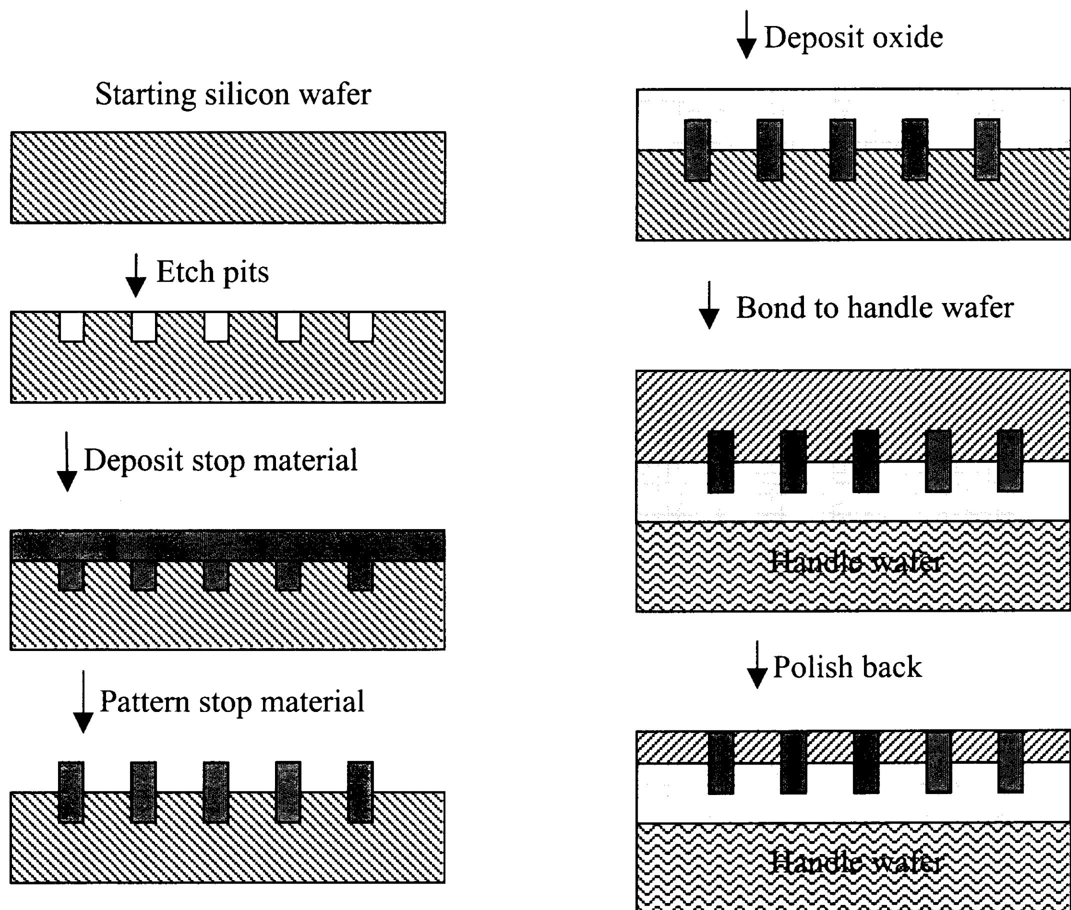


Figure 2.8. Process flow for polish-stop wafer thinning.

Plasma Assisted Chemical Etching (PACE) is another method for thinning wafers that appears to have achieved high thickness uniformity of the active layer. A thickness map of the silicon layer left after grinding and polishing is made to determine the dwell time of the etching electrode. The wafer surface is exposed to a plasma generated by the electrode in a chamber at relatively high pressure. The size of the electrode determines the removal rate and uniformity. By using progressively smaller electrodes, thickness variations are reduced [49,50]. The main drawback seems to be the time required to complete a single wafer.

2.5.2 Chemical Thinning

Bond-and-Etch-back SOI (BESOI) is a chemical method of thinning the active silicon wafer and is a generic term for a number of similar processes [9]. The etch rate of the silicon wafer in a solution can be much higher than the removal rate of polishing and does not introduce subsurface damage. The simplest implementation is a timed etch of a bonded wafer pair in a chemical solution. The repeatability and thickness uniformity will depend upon many factors such as pH, temperature, dissolved silicon concentration, agitation or flow of the etchant, and the degree to which the active silicon wafer is a perfect crystal. Because many of these conditions are not precisely controllable or known, the timed-etch method of thinning wafers results in large variations in thickness and thickness uniformity.

For more controlled chemical thinning, an etch-stop layer is implanted in the silicon wafer. After bonding, the wafer pair is etched in a chemical solution while protecting the handle wafer. This method depends upon a greatly reduced etch rate of the etch-stop layer compared to that of silicon. The etch-stop layer is then selectively

removed by either another chemical solution or by polishing. The final silicon layer thickness is dependent upon the depth of implantation and its thickness uniformity and that of any needed final polish.

Various chemical etchants are used to thin wafers such as KOH, NaOH, CsOH, NH_4OH, EDP (ethylenediamine-pyrocatechol-water), TMAH (tetramethyl ammonium hydroxide) and hydrazine. Implanted layers can be oxygen, boron, carbon, germanium and nitrogen. Etch removal rates and selectivity depends upon the concentration, pH, temperature, etc. The interested reader is referred to the literature [2, 51-62]. The generic process is depicted below in Figure 2.9.

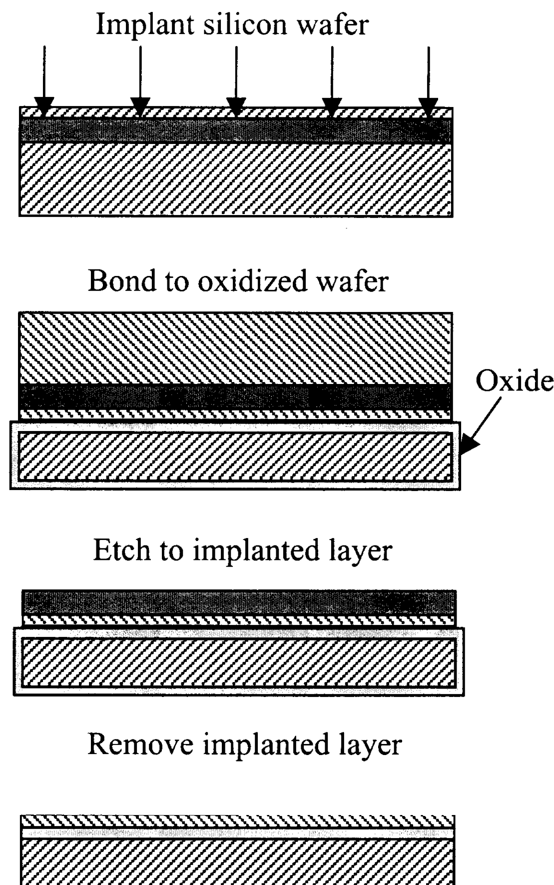


Figure 2.9. Generic process steps for etch-polish method of thinning wafers.

2.5.3 Layer transfer

Although the above methods transfer a thin silicon layer to a handle substrate, the term layer transfer generally refers to wafer splitting by implantation and heat treatment or epitaxial growth of a material on a sacrificial layer that is removed after bonding. Methods such as Smart-Cut® use an implanted layer and controlled heating cycles to split a bonded wafer [63]. Thermal treatment causes the implanted species to form defects that grow and connect in a layer parallel to the surface at a depth dependent upon the dosage energy. Eventually the defect layer causes a split between the remaining wafer and the thin region still bonded to the substrate. The thin layer that remains is then polished. Final thickness depends on the depth of implantation and the amount of silicon removed by polishing. In reference to Figure 2.9, after bonding, the "etch-stop" layer splits upon heat treatment. The remaining implanted layer is then removed, and the thin silicon layer polished smooth. This method is attractive in that the wafer from which the thin silicon layer was removed can be reused.

Other methods of layer transfer utilize an intermediate, sacrificial layer upon which the desired thin film is epitaxially grown. The intermediate layer compensates for lattice mismatches with the substrate or handle wafer and can be removed by side etching. Examples are of silicon on porous silicon and $Al_xGa_{1-x}As$ on AlAs on GaAs. The grown layer can then be bonded to another wafer or attached to a handle with wax or other temporary material [2]. A recent variation on the use of porous silicon achieves separation by water jet cutting of the porous layer [64]. The remaining porous silicon still needs to be removed chemically or mechanically.

2.6 Summary

Wafer bonding relies upon research and advances into many different areas of physics, chemistry, materials, mechanics and metrology, to name a few. While the starting materials are sometimes immediately bondable, most instances require modification of the surface properties, control of bonding conditions, and even new handling techniques, especially for thin layers. The drive of research in all areas that affect wafer bonding is the desire for cheaper, easier or completely new methods of combining materials to produce better or novel devices.

Ultrathin silicon wafer bonding is simple compared to the complexity of existing methods for producing thin, uniform silicon device layers. However, until recently, high quality ultrathin silicon wafer bonding has not been achievable. The investigation into the causes for poor bonding has involved physics, the mechanical properties of thin wafers, chemistry, the surface chemical species and surface activation methods, metrology, the morphology of the surfaces to be bonded, and the development of new handling and bonding techniques.

The proceeding sections of this chapter have detailed the current understanding and limitations of wafer bonding. Of these, ultrathin silicon wafer bonding most relies upon surface morphology, chemistry and surface activation, contamination and bonding mechanics. Because this thesis has concentrated on silicon-to-silicon or -silicon dioxide bonding, the effects of thermal expansion and lattice mismatches are minimized. Likewise, there is no need to thin the bonded wafer because ultrathin silicon wafers are already the desired thickness. There are no processing changes for anodic bonding of ultrathin wafers, apart from handling issues, and indirect bonding, with its dependence upon an intermediate material has restrictions that are outside the scope of this research.

The following chapters detail the research that has been undertaken to improve ultrathin silicon wafer bonding, the investigation into underlying causes for poor bonding, the determination of limiting parameters, and new methods and techniques for handling, preparing, and successfully bonding ultrathin silicon wafers. Ultrathin silicon wafer bonding is now high quality and repeatable. Several devices fabricated by the author and other members of our research group show how using ultrathin silicon can improve the performance and reduce the design complexity of existing devices. These are detailed in Chapter 6.

CHAPTER 3

ULTRATHIN SILICON WAFER BOND TRIALS

This chapter outlines the initial bonding experiments performed with Virginia Semiconductor Inc. ultrathin silicon wafers, the difficulties encountered in producing high-quality and successful bonding, various attempts to correct the problems and the eventual discovery of sources of nonbonding behavior. While many of these attempts did not improve bond quality, they each addressed a possibility that had to be eliminated.

The first section sets forth the conditions under which wafers were initially bonded and details the procedures used. Handling solutions developed when bonding very thin, < 100 micron thick, wafers, will be more thoroughly covered in Chapter 5. This chapter is more a record of the initial difficulties encountered and the first attempted solutions.

3.1 First Bonding Trial

3.1.1 Experimental Details

The first bond trials were with <100>, 4 inch diameter, ~ 250 microns thick silicon wafers and <100>, 4 inch diameter, ~ 500 microns thick, oxidized, silicon substrates. Although 250 microns thick wafers are not considered ultrathin, they were handled delicately in anticipation of bonding thinner wafers. The work was performed in a Class 10 cleanroom facility that maintains a standard Complimentary Metal Oxide Silicon (CMOS) processes. Wafers were cleaned in a “dirty” sulfuric acid bath, a “clean” sulfuric acid bath (SPM solution, see Section 2.3.2.1) and 100:1 HF in order to remove contaminants and the native oxide. “Thin” wafers were blown dry with nitrogen while the substrate wafers were spin-dried.

The substrate wafers were then steam oxidized to grow a ~ 1 micron thick silicon dioxide film. Then the substrates and "thin" wafers were recleaned in SPM to achieve hydrophilic surfaces and manually bonded. Manual bonding initially consisted of placing a substrate on a clean surface and a "thin" wafer directly on top. After aligning their flats, the wafers were pressed together in the center to remove the thin air layer separating them. The pair was then tapped lightly on the side to see if bonding had been achieved. Bonded pairs were annealed in nitrogen at 1100 °C for one hour, removed from the cleanroom and inspected under an IR camera. Some results are shown in Figure 3.1.

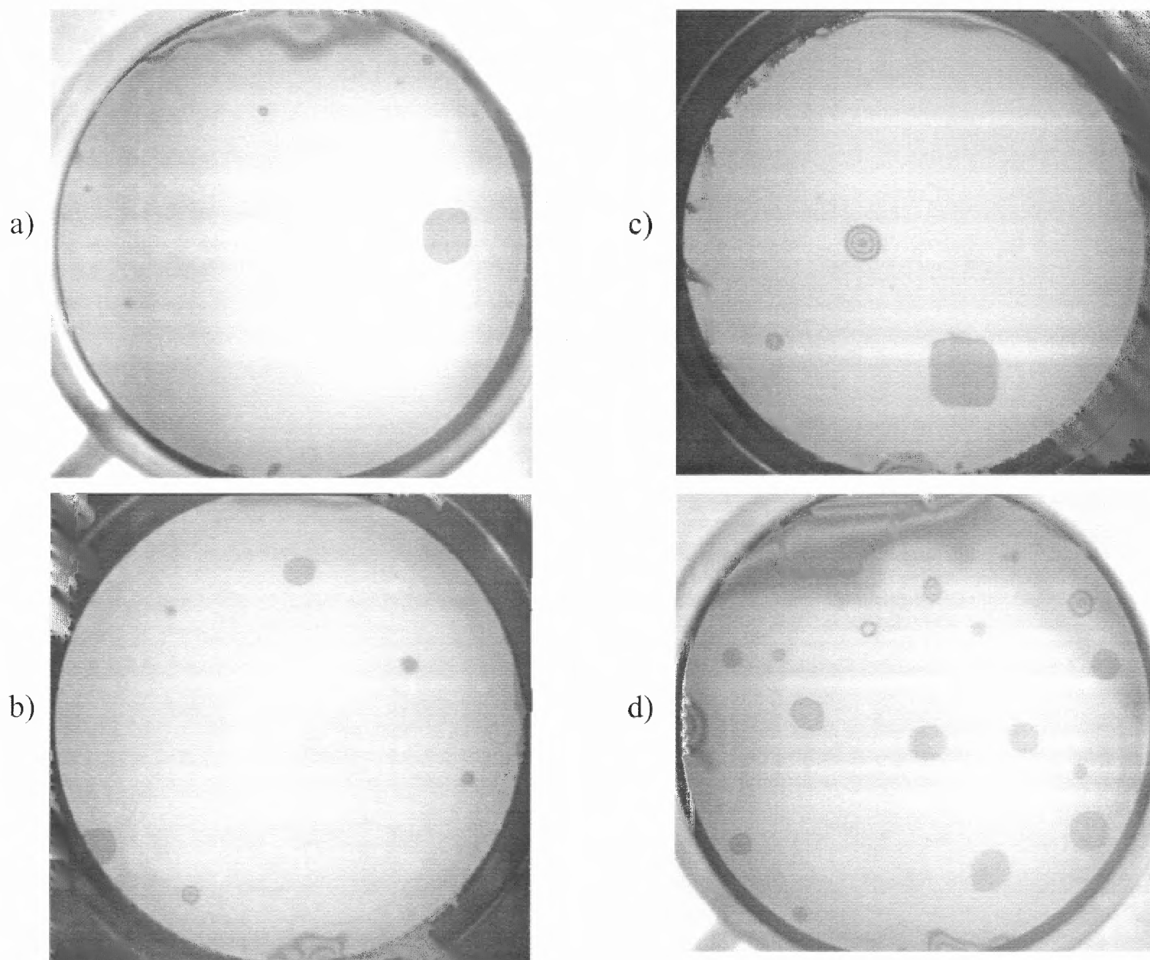


Figure 3.1. Four bonded wafer pairs showing air pockets, particle contamination and edge delamination. Wafer labels are (a) K8, (b) K4, (c) K3, (d) K14.

The changes in contrast seen in some areas of the wafers in Figure 3.1 are caused by separations between the wafers. Because the camera, with a visible filter, detects light of about 1 micron wavelength, each ring is caused by a separation of ~ 0.25 microns (a quarter-wavelength spacing results in reflections that cause destructive interference). These defects are not acceptable for bonding. The defect sources were probably particulates (smaller circular areas), air pockets (large circular areas) or, perhaps due to handling, scratches/roughening (edge delamination).

The surface upon which bonding was performed was a possible source of particle contamination. Starting with the second run, all manual bonding was performed in the wafer carriers used for cleaning. The two wafers to be bonded were placed in adjacent slots, pulled slightly out of the carrier, contacted at their flats and then completely removed. This kept the wafer surfaces parallel to the vertical airflow of the cleanroom as well as eliminating possible contamination from a surface. Bonding was also tried under the general sink hood to remove the wafers from the downward airflow completely, and on elevated surfaces above the sidewall air intakes, to avoid any dust stirred up by motion of the operator's feet. One bond trial was even performed, after a fifteen minute wait, in an otherwise empty cleanroom to limit the possibility of dust from other people. No discernable effect was seen on the amount of particle contamination of bonded wafer pairs. It was therefore concluded that the location of bonding, and that the presence of other people, had no real impact on particle contamination.

The operator himself though, was a possible source of contamination. In particular, the apparel that he wears could generate particles, especially the gloves that are in intimate contact with the wafers when bonding. To determine if the operator's

gloves were the source of particle defects, several possibilities were explored. A second pair of gloves was donned just prior to bonding, and, in some cases, rinsed and dried in high purity deionized water (DI). Gloves were also blown off with filtered nitrogen to help remove any particles. Different types of gloves were also used, including the acid-resistant type worn while processing wafers in the chemical baths. These attempts to control particle contamination did not result in any positive effect on the bond quality.

At the same time, attempts were made to eliminate the large area defects, assumed to be air pockets due to their size. When manual bonding is performed in the way described above, wafers could come together abruptly, slightly after the midpoint, as they were pulled from the carrier slots. The air pocket defects were thought to arise from this uncontrolled contact and several different methods of maintaining the wafers' separation were examined. Attempts were made to keep the wafer pair along the carrier slot as it was drawn from the carrier. Several Teflon® spacers, of different shapes and sizes, were placed in a slot between the wafers. Unfortunately, if they were too thick, the wafers would come together as abruptly as before, and if too thin, they could be pinched between the wafers. There was also the increased risk of particles as cleaning these spacers was difficult. Overall, these methods either had no effect on air pockets or reduced their number, but increased the particle contamination.

Filtered gas was blown between the wafers as they were held by the carrier slot. A separately cleaned, empty wafer carrier, to which the wafers were transferred prior to bonding, was also tried. Better filters, down to 0.2 microns particle size, were installed on the gas lines. These had no positive effect. The source of particles remained unknown and the air pockets were not affected by variations of the bonding method.

Not to be deterred, a second trial with six, 50 microns thick wafers was performed. As with the 250 microns wafers, these were cleaned in two sulfuric acid baths and their native oxides removed in 100:1 HF. Additional 500 microns thick wafers were oxidized for use as substrates. Standard processing of these wafers, although they were more difficult to blow dry, did not result in any loss until manual bonding was performed.

The substrate and the 50 microns thick wafers were recleaned in SPM and dried prior to bonding. The various methods described above, such as new gloves, various bonding sites, etc., to control particle contamination were continued. The first two thin wafers did not bond and the third broke in the attempt. Wafers that did not bond the first time were recleaned and additional attempts made to bond them. Out of the six wafers used, five bonded partially, one well. Figure 3.2 shows some annealed wafer pairs.

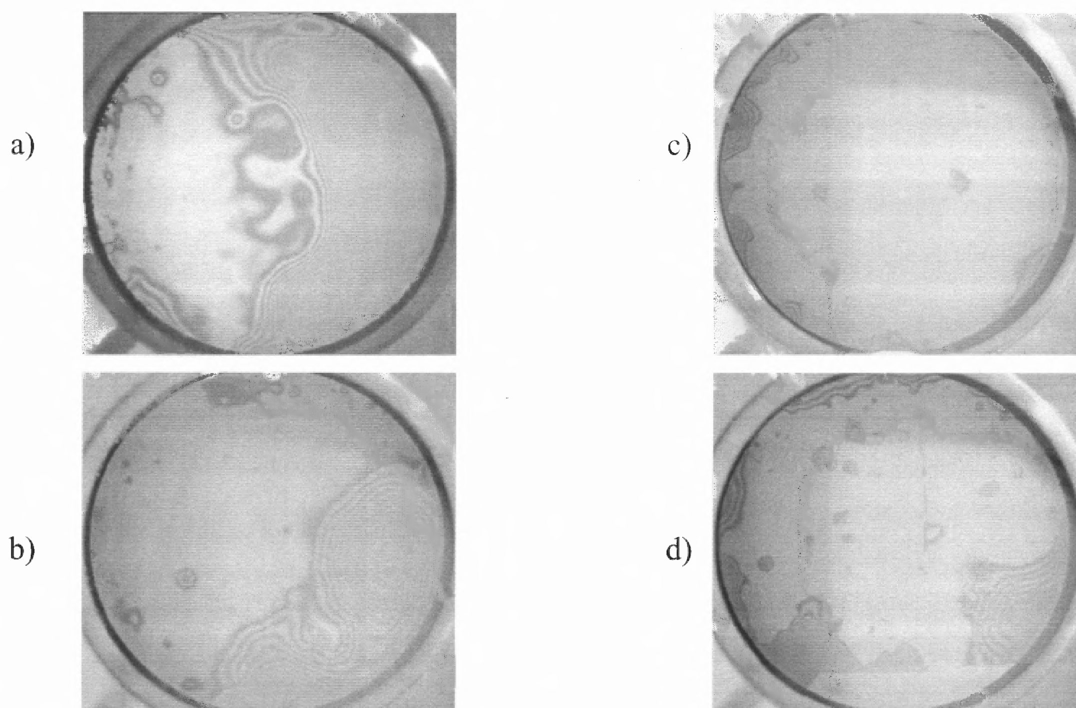


Figure 3.2. Results from bonding trial of 50 micron thick wafers. Wafers (a), (b) and (d) bonded about 50% while wafer (c) bonded almost

The results of the 50 microns thick wafer bonding were actually encouraging since one wafer bonded extremely well. The particle contamination pattern was nearly the same as for the 250 microns thick wafers, at least over the areas of the wafers that did bond. Air pockets also seemed to be absent in the bonded areas. The increase flexibility of the 50 microns thick wafer allowed for a smoother contact when pulled from the carrier compared to the 250 microns thick. What still needed to be determined was the source of the particle contamination and the reason why the one 50 micron thick wafer bonded so much better than the others did.

A third bonding trial was performed with 20 microns thick wafers. The same procedure was used as in the 250 and 50 microns wafers. In this trial, only two thin wafer bonds were attempted. Any bond was very difficult to achieve, but one wafer did bond partially. The result is shown below in Figure 3.3.

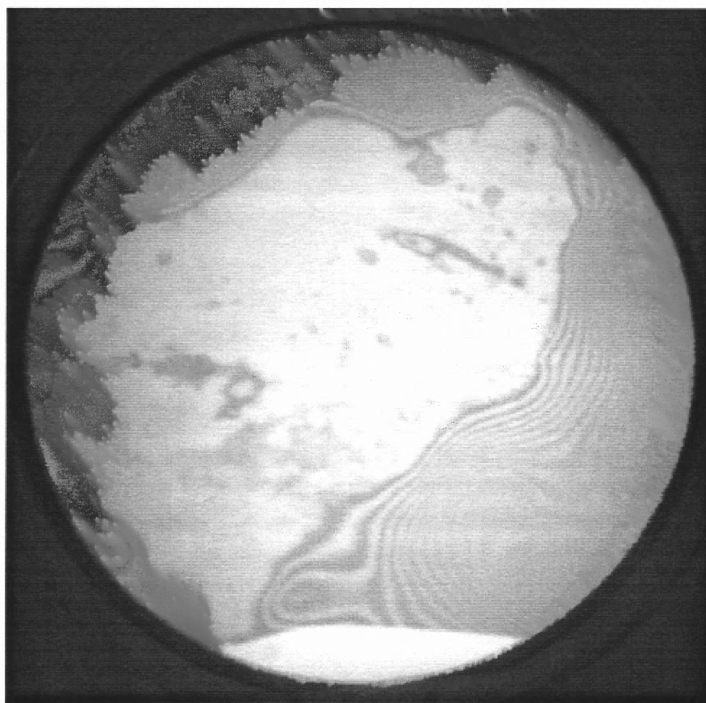


Figure 3.3. IR picture of 20 micron thick wafer "bonded" to a 500 micron thick, oxidized substrate. Sample labeled K20-1.

An additional trial was attempted for direct bonding of 12 micron thick silicon wafers to glass substrates, but these wafers broke when they were first blown dry. The wafer edges adhered to the carrier slots due to residual moisture. When blow drying was attempted, the wafers cracked along the carrier slot edges. The flexibility of these wafers is such that upon removal from their shipping carriers, they immediately bent to follow the cleanroom airflow (The class 10 cleanroom at NJIT utilizes sidewall intakes meaning that filtered air comes into the room through the ceiling and out waist-high vents along the walls). The barely perceptible wind caused these wafers to flap about like flags.

Although not a resounding success, the results of these trials showed that ultrathin silicon wafers were bondable. The question to be answered was why they did not bond well. A number of observations of the bond process were made and representative results for the three wafer thicknesses are tabulated in Table 3.1.

Table 3.1 Representative bonding properties for three wafer thicknesses, 20, 50, and 250 microns.

Sample File name	Thickness microns	Contact Wave Pressure/ Continuity	Relative Bond Energy before Annealing	Bonded Area %
K14	250	No Pressure Continuous	Strong	95
K8	250	No Pressure Continuous	Strong	95
K3	250	No Pressure Continuous	Strong	99
K50-1	50	Pressure Non-Continuous	Weak	35
K50-4	50	Pressure Continuous	Medium	90
K50-5	50	Pressure Non-Continuous	Weak	75
K20-1	20	Large Pressure Non-Continuous	Weak	40

The one column in Table 3.1 that is probably not immediately recognizable is the center, Contact Wave – Pressure/Continuity. When two wafers are initially placed together, they are usually kept apart by a very thin air gap. A slight pressure is needed to force away this air pocket and achieve intimate contact. From this initial point, a "contact wave" spreads across the surfaces of the wafers, driving out the thin layer of air separating them. The speed of this wave, and its continuity, is an indication of the quality of a bond. If it is relatively slow or discontinuous, then something is inhibiting the surfaces from forming intimate contact. The relative bond energy was found by tapping the wafer's edge and inserting tweezers to see by how much the wafers would separate.

In Table 3.1, from the increasing need for pressure to initiate bonding and the decreasing continuity of the contact wave, it is clear that as the wafers become thinner, they become harder to bond, with the exception of the one anomalous 50 micron thick wafer, K50-4 (See Figure 3.2, wafer (c)). The results are perplexing and contrary to intuition and wafer bonding theory. A thinner wafer, with its increased flexibility, should be able to conform to defects or particle contamination much easier than thicker, more rigid wafers. Wafer bonding models predict this result when varying the thickness, but assume that the surface does not change.

Ultrathin and normal thickness wafers both have mirror finishes and appear flat and smooth. The cleans and other processing are standard and have been used in numerous other bonding experiments in the literature for standard thickness silicon wafers. In order to understand the bonding behavior of ultrathin silicon wafers, the quality of their surfaces beyond what could be seen, had to be determined.

3.1.2 Ultrathin Wafer Surface Investigation

While the investigation into possible sources of particle contamination continued with the cooperation and help of cleanroom personnel, the literature on direct silicon bonding suggests (See Chapter 2) two critical parameters for successful bonding, surface roughness and chemical composition of the bonding layer. The scale of roughness that interferes with bonding was shown to extend to near atomic lengths.

A check for chemical contamination was performed using Fourier Transformed Infrared and micro-Raman spectroscopy and showed no unusual chemical species within the detection limits of the methods [65]. Besides silicon, only oxygen and carbon, known contaminants of the manufacturing process of silicon wafers, were detected. Later tests using X-ray Photospectroscopy (XPS) showed no evidence of the metals iron, chromium and nickel, which might have been incorporated in the manufacture of ultrathin wafers. While the level of detection, parts per million or less, of these methods does not rule out the possibility of ultrathin wafers having these contaminants, they do set an upper limit on their amounts. This upper limit is much less than would be expected if they were to have a noticeable impact on wafer bonding. By itself, chemical contamination in the manufacturing process could not account for the lack of bonding of ultrathin wafers.

The investigation now focused on the morphology of ultrathin silicon surfaces below the visible threshold. To characterize the surface roughness in the microscopic regime, optical profilometry using a Zygo® interferometer was performed by Rodel, Inc. Interferometric methods of profiling surface morphology can show sub-nanometer amplitude roughness on the horizontal scale of 10's of microns and up. Additionally, with the cooperation of Dr. Stephen Garofalini at Rutgers University, use of an Atomic Force Microscope (AFM), a Nanoscope II model, allowed characterization of what is

commonly called micro-roughness. AFM allows profiling to near-atomic levels, both vertically and horizontally, in areas up to 10 square microns for this model. Figure 3.4 shows the Root Mean Square (RMS) roughness for five ultrathin wafers, 12, 20, 37.5, 50, and 250 microns thick, compared to the handle or substrate wafer, 500 microns thick.

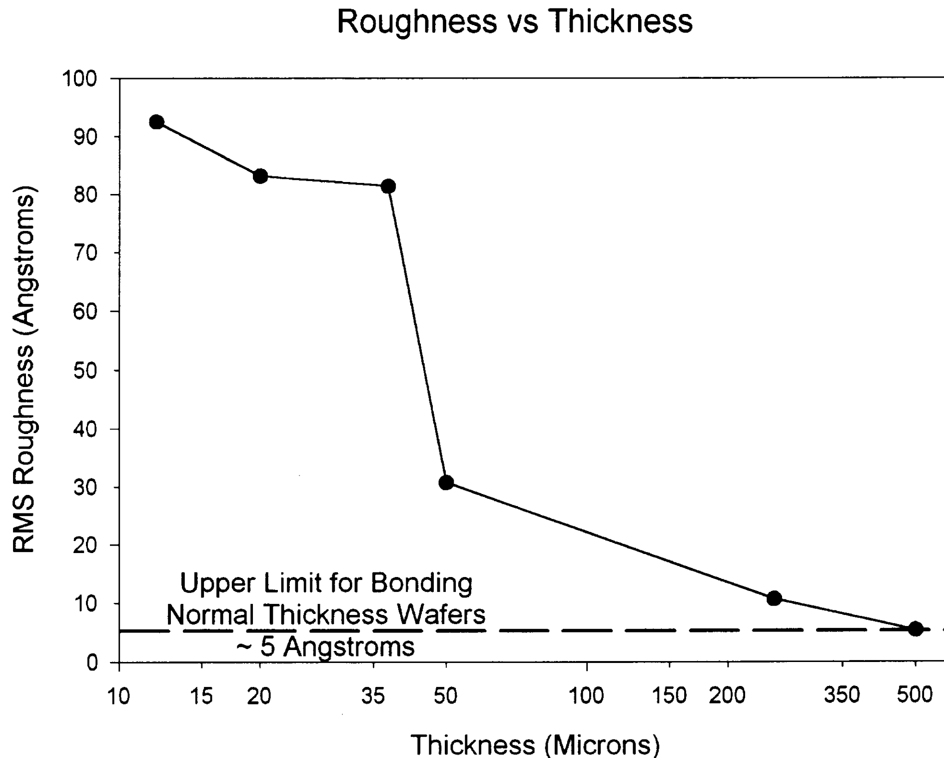


Figure 3.4. RMS roughness versus thickness for ultrathin and substrate wafers. Dashed line represents normal thickness, wafer bonding limit [42].

From Figure 3.4 it is not apparent why the 250 μm wafers bonded well but thinner wafers did not. The upper limit on rms roughness for bonding of normal thickness wafers, derived from the theory of water layers on the wafer surfaces, is ~ 10 angstroms (Å) (Section 2.4.1.1). This does not take into account other possible effects such as elastic deformation or other chemical bonds, but it has been used as a rule-of-thumb.

Using this 5 Å benchmark, wafers with rms roughness below this level should bond easily while those with greater roughness should be harder or impossible to bond. However, the rms roughness of the 250 microns thick wafer is about equal to this presumed upper limit and yet it was readily bonded. It is possible that this upper limit is not correct (see Section 2.4.2) or that there is something unique about ultrathin wafers.

The flexibility of ultrathin wafers, which is greater than for normal thickness wafers, might account for their ability to overcome the 5 Å rms roughness limit. The ability of ultrathin wafers to bond with even larger rms roughness is apparent for wafers less than 250 microns thick. For the 50 microns thick wafers, the roughness figure, 30 Å, is such that one would expect poor bonding if not complete failure. These also bonded, albeit with much more difficultly and less completely. For ultrathin wafers 20 microns thick, the rms roughness, ~ 80 Å, is so high that even the achieved partial bonding, shown in Figure 3.3, is completely unexpected using the 5 Å benchmark. However, the chemical and physical forces involved in the initial marriage of two surfaces are on a smaller scale than can be resolved with the Zygo® interferometer so the investigation turned to the AFM measurements.

The operation of an Atomic Force Microscope might be compared to the old phonograph record player. A sharp needle is moved over the surface and the vertical displacement of the needle is measured. The displacement of the needle can be measured by capacitive or piezoresistive methods or optically. The actual displacement that is measured is that of the needle support structure. This structure can have piezoresistors embedded in it, which have a relatively large change in resistance when their physical dimensions are altered, or be one contact of a capacitive structure, whose capacitance

changes as the distance between two contacts is altered. Piezoresistors are usually formed by the implantation of a material into the silicon to provide a path for electrical current, whose magnitude changes for a set voltage, as the resistance changes. A capacitive structure needs two surfaces, usually formed by depositing metal, separated by a small distance. One surface is on the needle support structure and the other is fixed nearby and parallel. As the moveable "plate" changes position relative to the fixed, the capacitance of the electrical circuit, to which the two plates are connected, is altered.

The optical method relies on the reflection from the top of the needle structure of a focused laser beam that is then steered onto a detector array. A long path length ensures a large movement across the array for a small displacement of the needle. The Nanoscope II®, the instrument model used in this thesis, employs optical detection of the needle motion.

A centimeter square chip of the sample material is mounted on a small metallic disk using double-sided tape. The disk is place on a magnetic platform that moves in the x and y directions. This movement is produced by a piezoelectric stack under the magnetic platform. Piezoelectricity is a current formed by deformation of certain types of material. Supplying a current to this material causes it to expand. A cigarette lighter that uses an electric spark for ignition is an example of a piezoelectric application.

The first three AFM images in Figure 3.5 are 10 microns by 10 microns area scans of wafers 250, 50, and 20 microns thick. The final image is a close up scan (note the horizontal scale of Figure 3.5 (d)) of the "spikes" that can be seen most clearly in the 50 microns thick AFM image (Figure 3.5 (b)). These spikes were ubiquitous on most ultrathin wafers and are believed to be a cause of poor bonding.

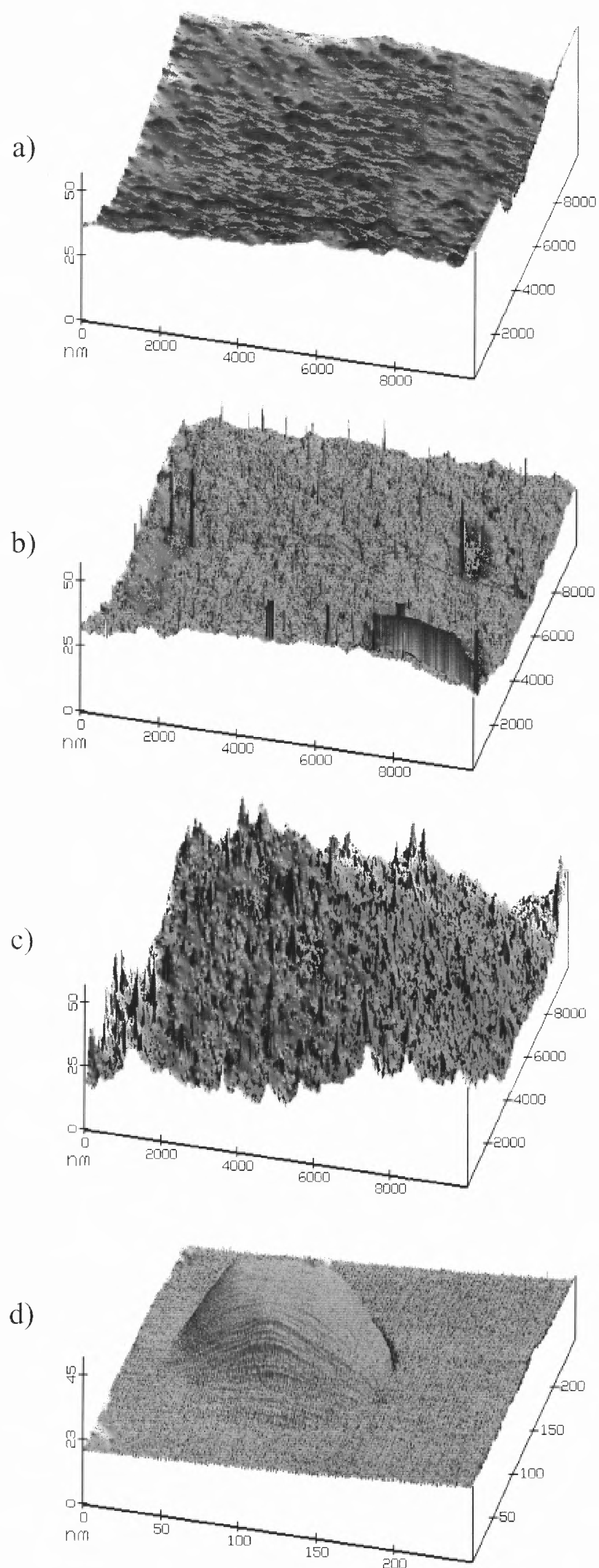


Figure 3.5. AFM scans of 250, 50 and 20 micron thick ultrathin silicon wafers, (a), (b), (c), respectively. Scan (d) is of a roughness "spike" shown in (b).

The first thing that is noticed in Figure 3.5 is that the overall roughness increases as the wafers get thinner. The second apparent feature is the appearances of "spikes" in the 50 microns thick wafer scan. These spikes turn out to resemble hillocks when examined more closely, Figure 3.5 (d). Their dimensions are roughly 100 by 50 by 45 nanometers and some, like Figure 3.5 (d), seem to have a faceted nature. This facet is roughly at angle of 56 degrees from the surface, which is close to the 54.7 degree angle of the <111> to <100> silicon planes. Although standard cleaning methods do not remove these features, they can be moved across the surface with the AFM tip.

It is known that polishing of silicon wafers is often done with silica particles of roughly 100 angstroms size, but this is an order of magnitude smaller than these particles [2]. Another possible source may be the wafer thinning process. Mechanical means such as lapping, grinding and polishing cannot reliably thin wafers below about 200 microns. Therefore, some method of chemical etching is probably used to achieve ultrathin wafer dimensions. The particles seen in the AFM scans could be aggregates of etched silicon that have attached to the surface upon removal from the chemical solution [66]. The conclusion drawn is that these are silicon or silicate particles, due to the null results of XPS and micro-Raman spectroscopy, that have adhered to the surface of the wafers at some point in the manufacturing process.

It was also found that the number of particles was not the same for the two sides of double-polished wafers. One side was found to have predominately more particles than the other. This may explain why the one 50 microns thick wafer bonded easily and readily, K50-4 (See Figure 3.2 (c) and Table 3.1). Figure 3.6 shows a small area AFM scan of the background roughness of a 50 microns thick wafer (See Figure 3.5 (b)).

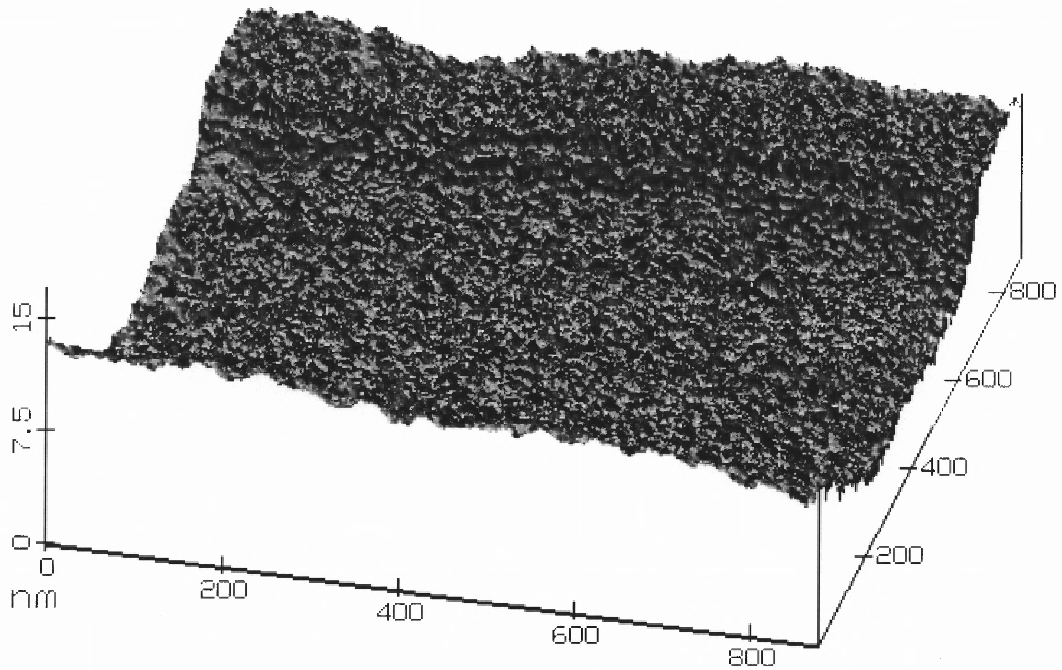


Figure 3.6. Small area AFM scan of a 50 micron thick silicon wafer. Note the vertical scale in comparison to Figure 12 (b).

Although the roughness seen in Figure 3.6, is large for normal thickness (300 – 500 microns) wafer bonding (5 Å rule-of-thumb), it may not be enough to deter bonding of the much more flexible 50 microns thick ultrathin wafer. However, that possibility cannot be tested unless a way is found to remove the particles without increasing the surface roughness.

In response to this work, Virginia Semiconductor Inc. (VSI) instituted a study of different polishing methods for their ultrathin silicon wafers. Surface roughness tests using the Zygo® interferometer at Rodel and AFM were repeated. RMS roughness results are shown on the following page in Figure 3.7 for the AFM scans. The improved polishing methods had the most impact on the 10 microns thick wafers. As one can see, the rms roughness has been reduced by almost an order of magnitude.

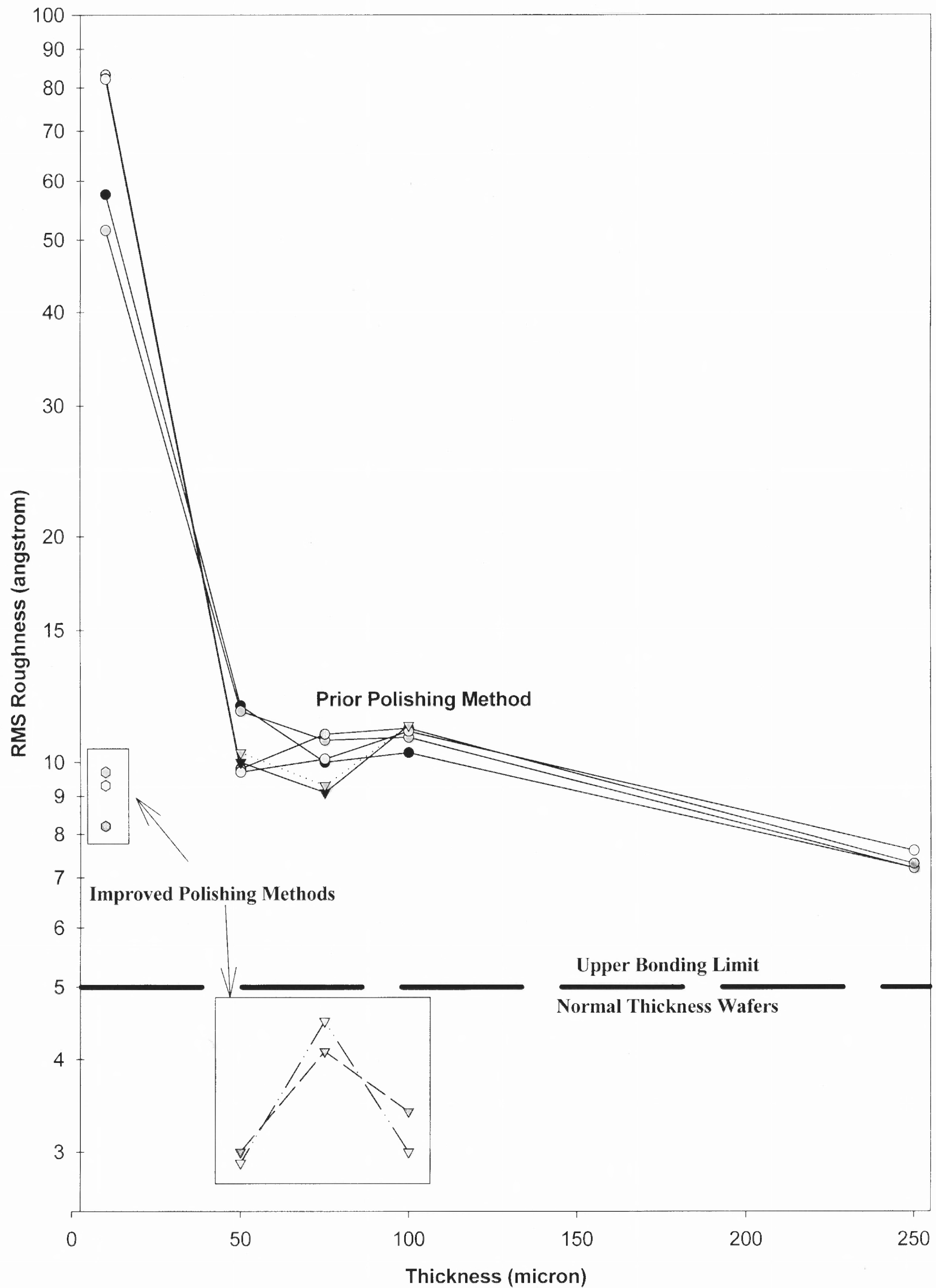


Figure 3.7. RMS roughness versus thickness for original (lines) and improved (boxes) polishing methods of VSI. Dashed line indicates rule-of-thumb bonding limit on roughness, ~ 5 Å.

The roughness values in Figure 3.7 are an indication that the surface quality has been improved, by proprietary methods, and that bonding of these wafers should be more successful. RMS roughness, however, does not indicate the nature of the roughness. The distribution of the magnitudes of individual roughness features may have a greater impact on bondability than the overall magnitude. Chapter 2.4.2 highlights some of the drawbacks of using rms roughness to determine the success of bonding. Figure 3.8 shows the roughness change for a 50 microns thick wafer, with the new polish method.

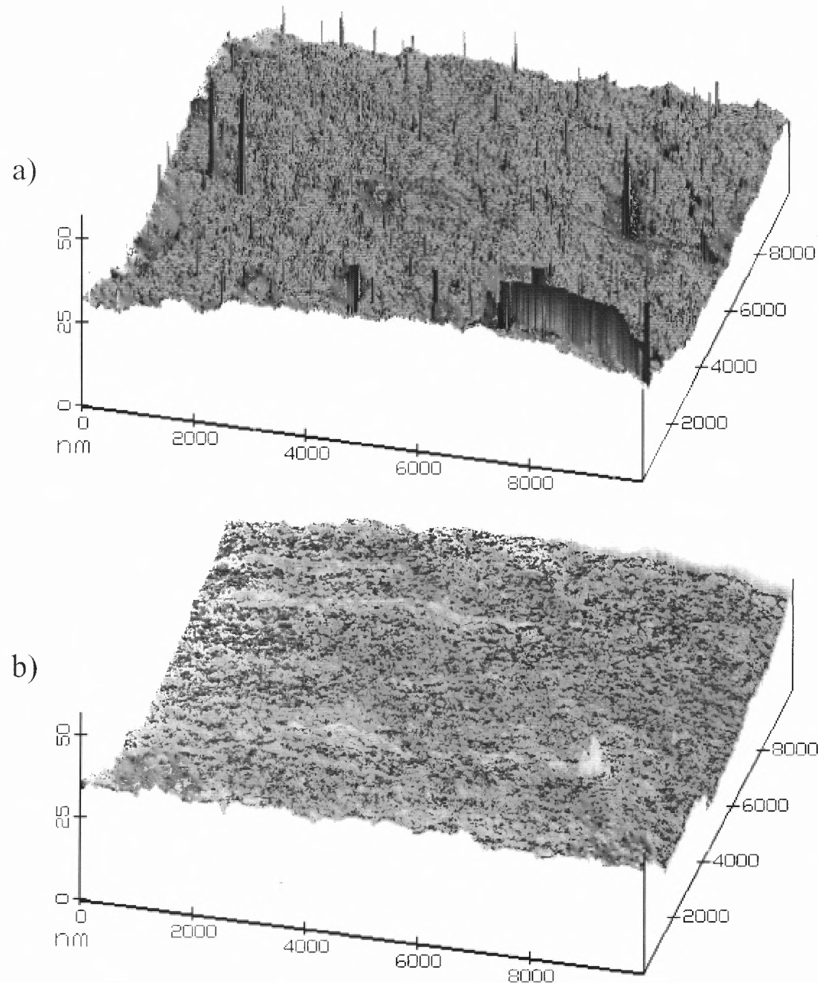


Figure 3.8. 50 microns thick wafer surface after a) old polishing and b) best new polishing methods.

Figure 3.8 (b) shows an absence of the roughness "spikes" found in Figure 3.8(a), but the background roughness does not appear to be significantly improved. The absence of "spikes" should help the bondability of these wafers, but it is uncertain how the change in background roughness will affect bonding. Returning to Figure 3.7, one sees that the change in rms roughness, significant for 50 microns thick wafers, is not a reliable indication of the surface quality. It may be that the surface roughness of the original polishing process, without the spikes, is less than that of the new polish. Virginia Semiconductor, Inc. did modify or otherwise improved its post-polish cleaning methods, perhaps using a megasonic cleaning process, but the new polishing methods were already in use at the time, so no comparison could be done.

3.1.3 Summary

Wafer bonding became harder as the wafers became thinner. No chemical contamination was found in enough abundance to be thought to inhibit bonding. Roughness studies by Zygo® Interferometer and AFM showed increasing roughness with decreasing thickness. Particles of unknown nature were also found and thought to be a remnant of the manufacturing process. These particles were predominantly on one side of double-polished wafers. The good bond quality of the one 50 micron thick wafer is thought to be due to bonding to the less particle-contaminated side of the wafer. Poor bonding of ultrathin wafers is most likely due to increased roughness. The increased flexibility of ultrathin silicon wafers is believed to be the primary reason the thinnest wafers bonded at all despite the relatively large roughness of their surfaces.

3.2 Second Bond Trial

Virginia Semiconductor, Inc. had reduced the rms surface roughness of their thinner wafers to near or below that of the easily bonded 250 microns thick wafers. What effect this reduced roughness had on bonding, still needed to be examined. The other process steps, cleans, oxidation, etc., remained the same as the first trial. Unfortunately, these wafers were 3" diameter and the only available substrates at the time were 4" diameter from the previous bond trial. This made manual bonding more difficult.

The wafer carriers, previously used, could not accommodate both wafer sizes. If a 4" carrier were used, the slots were too far apart to keep separate the 3" wafers. If a 3" carrier were used, the 4" substrate wafers would not fit in the slots. The separation flags of the automated bonding system (See Chapter 5) were also too short to keep apart the 3" wafers. In the end, the 3" wafers were essentially laid down on the 4" substrates and pressed together. Without any control of the separation, it was expected that the interface would contain an increased number air pockets and particulates compared to the first trial. As long as no significantly large changes in the size and type of defects was observed, it was assumed that lack of bonding control would account for differences in the number of defects between the two trials.

The important question that was to be answered was how well the new-polish-method wafers would adhere. As in Table 3.1, the factors that would indicate an improvement in bonding were the amount of pressure needed to initiate the contact wave and its continuity, the relative strength of any achieved bond, and the percent of area that was ultimately bonded after the anneal. Some IR images of the results are shown below in Figure 3.9. The third wafer, Figure (c), was broken prior to bonding.

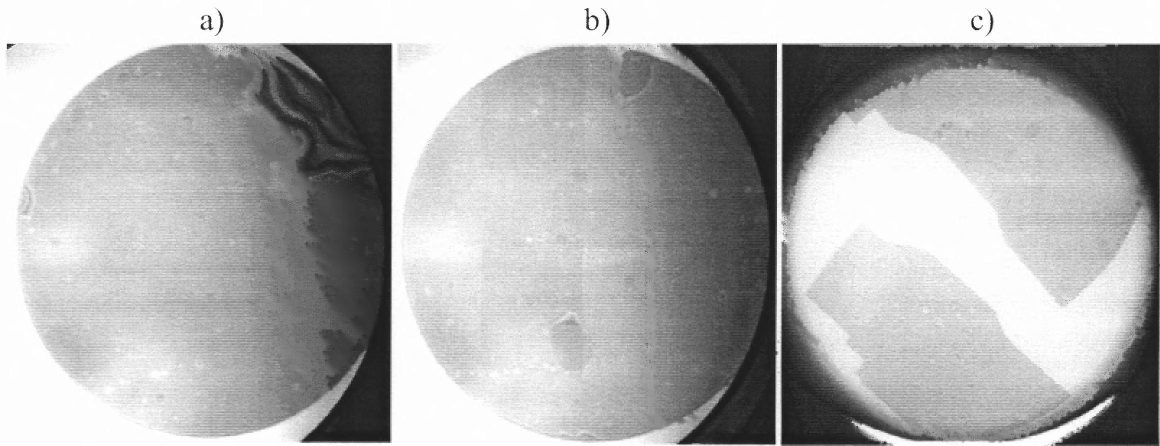


Figure 3.9. Three IR images of bonded 3" ultrathin to 4" substrate wafers. From left, a) 100 microns thick, b) 75 microns thick and c) 10 microns thick.

While the images in Figure 3.9 show large amounts of contamination and defects, probably due to the method of bonding, the differences between them are slight. The defects are most likely particles and small air bubbles trapped by uncontrolled contact waves originating at several points. A better bonding method would probably reduce these problems. This is indicated by the fact that all thickness wafers, 100, 75, and 10 microns, displayed characteristics of high quality bonding. All wafers needed little or no pressure to start the contact wave, adhered strongly to the substrate and showed approximately the same percentage of bonded area after anneal. The 10 microns thick wafer (Figure 3.9 (c)) achieved these results even after it had been broken.

With these results, it was believed that if a bonding method could be developed that reduced or eliminated the particle contamination and trapped air pockets, ultrathin wafer bonding could be successfully performed with any thickness wafers down to 10 microns. In addition, due to the results of the first trial, ultrathin wafers could bond to rough surfaces to which normal thickness wafers could not possibly bond.

3.3 Ultrathin Roughness Limits

The preceding sections showed qualitative results of improved bonding by the new polishing methods. The focus of this section is to attempt to quantify the roughness limitations for ultrathin silicon wafer bonding. For these wafers, large-scale roughness features, such as wafer bow and waviness, should have little or no effect on bonding. Smaller scale roughness is expected to play a larger role in determining whether a bond will be successful. The question to be answered is how much roughness and on what scale can be accommodated by different thickness ultrathin wafers?

3.3.1 Bond Mechanics and Power Spectral Density

Section 2.4.2 of this thesis detailed the theory of elastic accommodation by Yu and Suo [43] and how a height limit, for successful wafer bonding, for a single, sinusoidal roughness feature was derived in that model. In their conclusion, Yu and Suo proposed a way of providing a fuller description of bonding limits, for more realistic surfaces that have more than one roughness wavelength. They proposed taking the Fourier Transform of surface height data in order to relate the magnitude of individual roughness features to their spatial wavelengths and then, using the methods described in the elastic accommodation model, find the total interface stress by superposition of the solutions for each wavelength.

The Power Spectral Density (PSD) is a Fourier Transformation of the surface height data and is equal to the surface height squared per frequency. The critical condition for bonding, derived by Yu and Suo (Section 2.4.2) is unchanged by the consideration of multiple roughness wavelengths. Each wavelength's critical height, or critical bonding condition, is derived in terms of its unit length. By rearranging terms of

the critical condition, the bonding limit may be expressed as a surface height squared per frequency and related to the Power Spectral Density. This model should hold, as long as linear elastic theory applies, over the entire frequency range of roughness possible for wafers of 100 mm diameter, specifically, 0.01 mm^{-1} to ~ 0.1 $angstrom^{-1}$. Because surface roughness is routinely stated in terms of the PSD for profilometers with different bandwidths, a model describing the bonding limits across all roughness scales is needed to help determine the critical frequency intervals, and therefore, the instrumentation required for surface characterization, for a given application.

The following is a continuation of the derivation shown in Section 2.4.2. Appendix A shows that the assumption of multiple roughness wavelengths does not alter the form of the critical bonding height formula.

The critical condition is

$$\frac{H^2}{\Gamma \cdot L} = \frac{4 \cdot \sqrt{2}}{\pi} \cdot \left(\frac{1}{\overline{E_1} \cdot I(k \cdot t_1)} + \frac{1}{\overline{E_2} \cdot I(k \cdot t_2)} \right), \tag{21}$$

where H is the roughness height, L is the roughness wavelength, Γ is the surface energy,

$$\overline{E} = \frac{E}{1 - \nu^2}, \tag{22}$$

where E is Young's modulus and ν is Poisson's ratio, and,

$$I(\alpha) = \frac{e^{2\cdot\sqrt{2}\cdot\alpha} + e^{-2\cdot\sqrt{2}\cdot\alpha} - 2 - 8\cdot\alpha^2}{e^{2\cdot\sqrt{2}\cdot\alpha} - e^{-2\cdot\sqrt{2}\cdot\alpha} + 4\cdot\sqrt{2}\cdot\alpha} \tag{23}$$

For silicon to silicon bonding, the Young's modulus and Poisson's ratio will be equal, $E_1 = E_2$. The roughness frequency is $k = 2\pi/L$. So equation (21) above simplifies to:

$$H^2\cdot k = 8\cdot\sqrt{2}\cdot\frac{\Gamma}{\bar{E}}\cdot\left(\frac{1}{I(k\cdot t_1)} + \frac{1}{I(k\cdot t_2)}\right), \tag{24}$$

which, divided by k^2 gives the limit in terms of H^2/k, the form of the PSD,

$$PSD = \frac{H^2}{k} = \frac{8\cdot\sqrt{2}\cdot\Gamma}{\bar{E}}\cdot k^{-2}\cdot\left(\frac{1}{I(k\cdot t_1)} + \frac{1}{I(k\cdot t_2)}\right). \tag{25}$$

Equation (25) can be simplified by setting C equal to constant factors before k^{-2},

$$PSD = C\cdot k^{-2}\cdot\left(\frac{1}{I(k\cdot t_1)} + \frac{1}{I(k\cdot t_2)}\right). \tag{26}$$

The PSD depends only then, on the material properties, which are incorporated in the constant C, the inverse square of the frequency and function $I(\alpha)$.

Now the function $I(\alpha) \to 1$ as $\alpha \to \infty$, and $I(\alpha) \to (2/3)\alpha^3$ as $\alpha \to 0$, so the PSD varies roughly between,

$$PSD = C \cdot k^{-2}, \tag{27}$$

as $k \to \infty$ and,

$$PSD = C \cdot k^{-5}, \tag{28}$$

as $k \to 0$.

At some interval a crossover between k^{-2} and k^{-5} occurs. This is dependent upon the function $I(\alpha)$ which, in turn, depends upon the product of the wafer thickness and frequency. For bonding of ultrathin wafers, equation (26) cannot be simplified by setting $t_1 = t_2$, i.e. taking the wafer thickness to be equal.

It is found that $I(0.1) \approx 4.7 \times 10^{-4}$ and $I(5) \approx 0.9998$. For a 500 μm thick wafer, the frequency has to be $< 0.002\ \mu m^{-1}$ for the $1/I(\alpha)$ factor to be greater than 1. For a 10 μm thick wafer, the frequency has to be $< 0.5\ \mu m^{-1}$. AFM scans of 10 μm x 10 μm have a minimum frequency of $0.1\ \mu m^{-1}$ and a maximum of $20\ \mu m^{-1}$. Smaller area scans shift the range to higher frequencies. In the range of AFM, the bond limit goes as,

$$P = C\,k^{-2}, \tag{29}$$

where P is the power spectral density, C is a constant and k is the frequency.

For ultrathin wafers, the crossover to a k^{-5} form should start at around 0.1 μm^{-1} with the transition occurring at smaller frequencies for thicker wafers. Figure 3.10 below shows a plot of the bond limit as a function of frequency for a theoretical scan covering wavelengths from 100 mm to 1 nm. This range covers the entire diameter of a 4" silicon wafer down to near-atomic spacing for wafers ranging in thickness from 10 to 500 μm bonded to 500 μm thick silicon substrates.

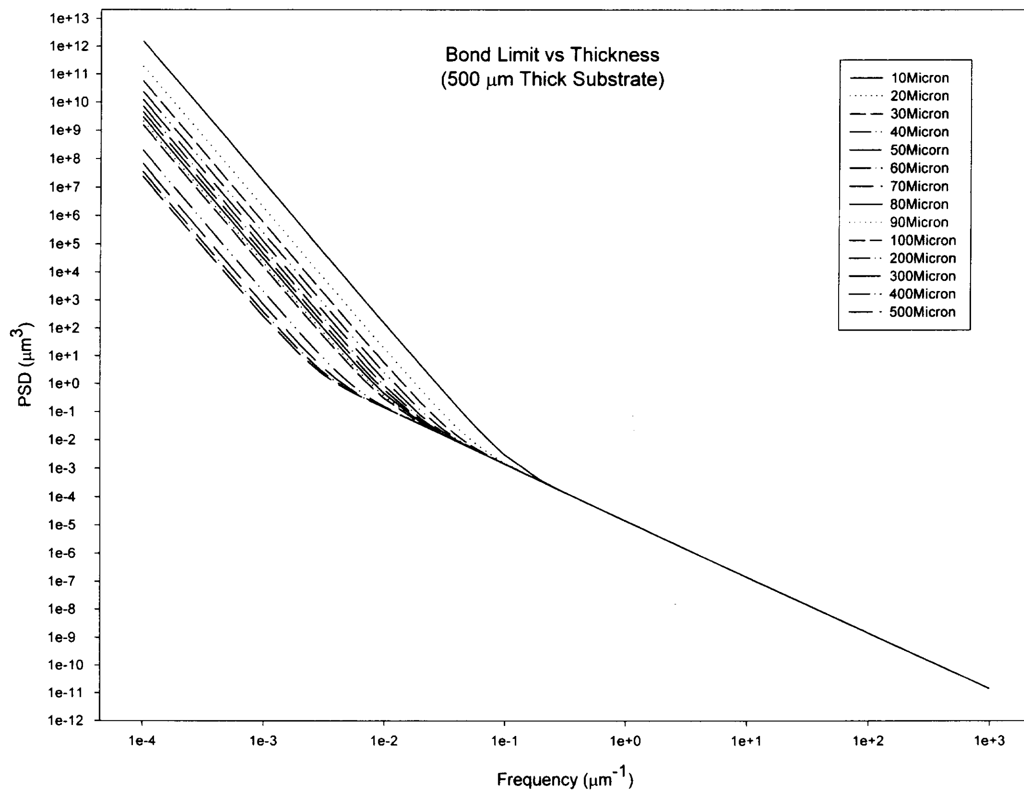


Figure 3.10 Graph of the bonding limit model for ultrathin and thick silicon wafers ranging from 10 to 500 μm bonded to 500 μm silicon substrate wafers.

The crossover from k^{-2} to k^{-5} occurs around 0.1 μm^{-1} for 10 μm thick wafers and not until ~ 0.005 μm^{-1} for 500 μm thick bonded wafers. This model indicates that successful bonding is not dependent upon wafer thickness in the high frequency roughness regime, the scale of common AFM measurements. In contrast, bonding to large-wavelength-scale roughness, on the scale of surface features of processed wafers, depends strongly on the bonding wafer thickness.

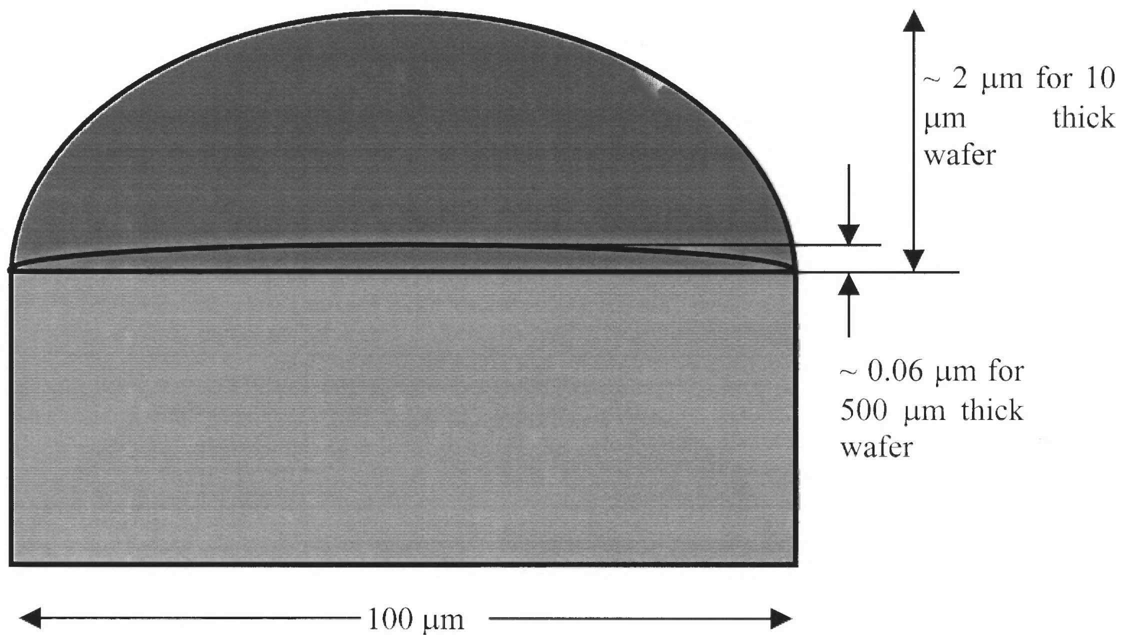


Figure 3.11. Example of the difference in feature height accommodation by a 10 microns thick wafer versus a 500 microns thick wafer. Not-to-scale

Figure 3.11 shows the effect of wafer thinness on wafer accommodation to surface features, according to the theory. Although ultrathin wafers can conform to such large features, the surfaces must be smooth on a microroughness scale also, in order for bonding to occur. In other words, unless the roughness at high frequencies is low, using a thinner wafer to conform to larger features will still not allow bonding.

The following graph, Figure 3.12, shows a plot of the bonding limit versus high frequency roughness, across the AFM frequency range, for ultrathin wafers 50 μm thick, that had roughness features altered by oxidation smoothing (Chapter 4).

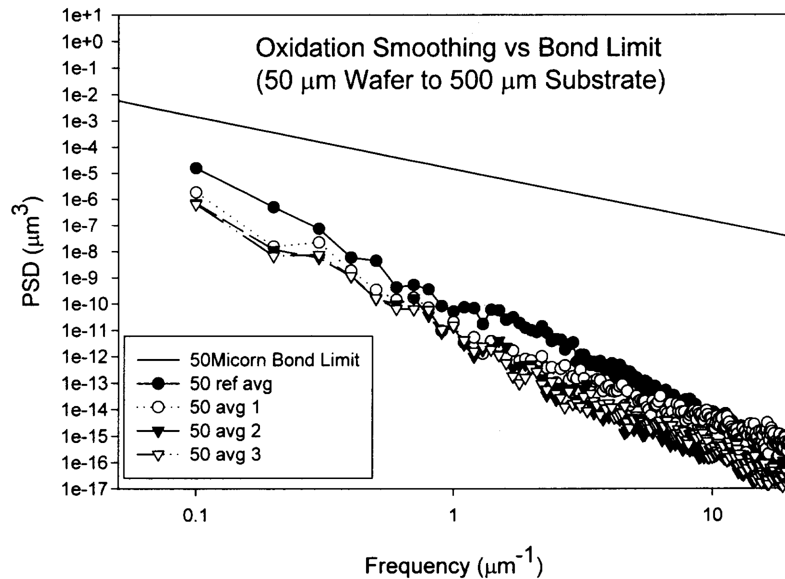


Figure 3.12 Plot of the model bond limit and AFM data for ultrathin wafers 50 μm thick with varying roughness.

Figure 3.12 indicates that because their PSD values are below the bond limit, 50 μm thick wafers should bond well. This assumes that there are no large roughness features, which are outside the limits of AFM, that are above the bond limit.

Section 3.1 described the bonding of original finish, 50 thick wafers. Although there was one 50 μm thick wafer that bonded very well, most did not. Figures 3.5 and 3.6, together with the bond limit theory, may explain this bonding behavior of the 50 μm thick wafers. The PSD bond limit theory indicates that the features seen in Figure 3.5 (b) are the reason for poor bonding in 50 μm thick wafers. These features, the "spikes," were probably averaged out in the PSD calculations, which were done over many wafers, due

to large variations in their density between wafers. The background roughness (Figure 3.6) of the 50 μm wafer surface was small and probably would not prevent successful bonding. Once the "spikes" were removed, bonding was repeatedly successful (Table 4.1 in Section 4.2.3).

In Figure 3.13, the roughness of the 20 μm thick wafers has components that are greater than the bonding limit, but the bonding results for smoothed wafers (lower plots) was much improved (Table 4.1 in Section 4.2.3). Complete bonding was not achieved with the 20 μm thick wafers and the components of the roughness above the bond limit may be the reason for this result. The AFM frequency extent does not cover the crossover between k^{-2} and k^{-5} dependence of the bond limit for 20 μm thick wafers, after which it is expected that the roughness of the 20 μm thick wafer will again be below the bonding limit as it is at the higher frequencies in this graph.

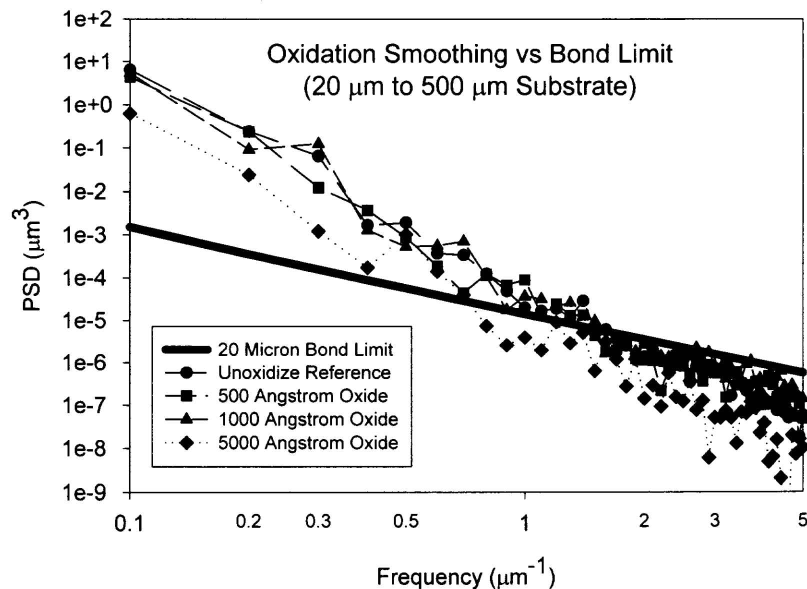


Figure 3.13. Plot of the model bond limit and AFM data for ultrathin wafers 20 μm thick with varying roughness.

That partly successful bonding was achieved may be due to the hydrophilicity of the surface which may overcome ~ 10 Å roughness (see Section 2.4.1.1) through water bridging. The partial success may also be due to the known flow of oxide during high temperature anneal. Bonding without an oxide may not be successful with 20 μm thick wafers with the roughness shown in Figure 3.13. Another point that must be made is that the constant factor of the PSD bond limit model, which determines the height of the limit plot, depends upon the surface energy, which, in turn, depends upon the surface activation and hydrophilicity, and which may not be accurately known.

The PSD bond limit does predict that ultrathin wafers will conform to large surface feature and that 20 μm thick wafers should be hard to bond. The computation method used to calculate the PSD probably averaged out the surface features of 50 μm thick wafers seen if Figure 3.5 (b). These wafers, which did not bond well initially, a result that is not in agreement with the PSD bond limit model, bonded successfully after the features were removed. Partially successful bonding of 20 μm thick wafers, contrary to the roughness above the limit in Figure 3.13, may be explained by the fact that the modeling did not take oxides into account or that the surface energy term in the model is dependent upon chemistry such as hydrophilicity.

3.3.2 Other Models and Summary

In Section 2.4 of this thesis, reference was made to an empirical bonding model proposed by Roberds and Farrens that showed a bonding limit with a $k^{-2.5}$ dependence that matched the slope of their PSD data very well [45]. In their paper, they went on to relate this model to a fractal description of the wafer surface. The distinction that has to be made is that their model is a description of the surface roughness and not that of the bonding

behavior. Any bond limit model should only depend upon the properties of the materials and not on the form of the roughness, and therefore, has no reason to mimic the roughness profile. For this reason, their model may not be considered to be a bond limit model, but rather a description of the nature of the roughness features.

The bond limit model given above seems to agree with the results of the work involved in this thesis. It correctly predicts the ability of ultrathin wafers to bond to rougher surfaces than thicker wafers, and the observed difficulty in bonding the 20 μm wafers. Since it covers the entire frequency range, from atomic displacement to wafer bow, this model may help predict bonding limits when using processed wafers with elevated surface features and the role of oxide flow in overcoming roughness features during high temperature anneals.

3.4 Particle Contamination

Contamination and defects plagued the early bonding trials detailed in the previous sections. With the use of the Electronic Vision's EV501S bonding system, the number of voids found when bonding standard thickness (300 – 500 μm) dropped to almost zero. More important was avoiding scratches or damage to the wafers' edge that would prevent bonding. The use of handle wafers (Chapter 5) also decreased the number of voids when bonding ultrathin wafers. Particle contamination, however, was a problem in search of a solution. The source(s) of contamination had not been found by the time the EV501S bonder was installed and the qualification bonding trials contained many particles. They had to be found before wafer bonding could be performed successfully.

The initial attempts to control particle contamination were described previously in Section 3.1. While some of the early defects might be attributed to the quality of the

ultrathin surface polish, VSI's institution of new polishing methods and the resultant reduction in roughness, made it clear that particles were being introduced in the processing steps. A test of the processing steps involved in bonding was initiated to try to determine the source(s) of contamination. It would also serve as a check on the surface quality of VSI wafers. If little or no contamination were found using another manufacturer's wafers, then the surface quality of the VSI wafers would be the source of defects in bonding.

Standard thickness (~ 500 μm), monitor-grade (used to check process parameters, not for device production), non-VSI, wafers were subjected to the same processes as ultrathin wafers prior to bonding. After each process, one pair of wafers was spin-dried and one oven dried, then bonded together and examined by IR. The processing steps were (see Appendix A.7 for specifics) M-Pyrol (clean), P-Clean, 100:1 HF (native oxide removal), oxidation and RCA2. Results are shown below in Figure 3.14.

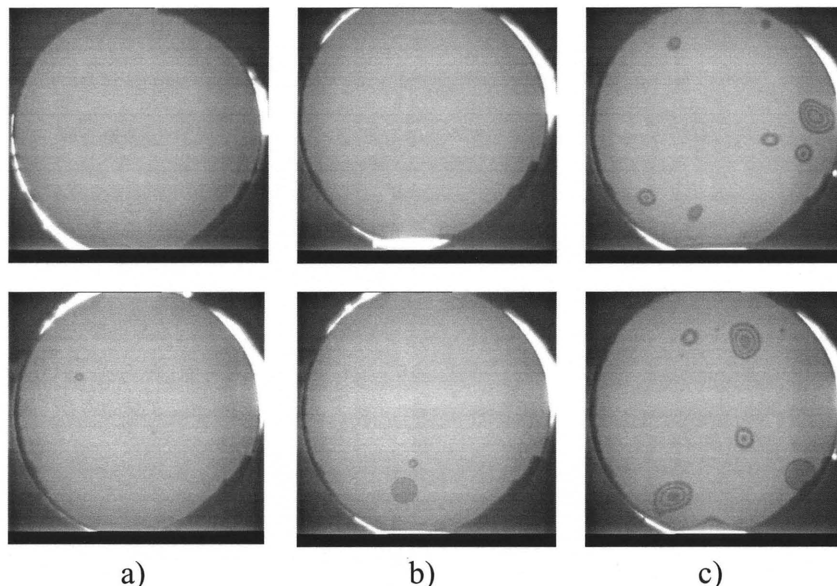


Figure 3.14. Bonded wafer pairs spin dried (top row), or oven dried (bottom row) after a) M-Pryol, b) P-Clean, and c) HF.

In Figure 3.14, the top row wafer pairs were spin-dried and the bottom row pairs were oven-dried for the three chemical baths, M-Pyrol, P-Clean, and 100:1 HF. Looking at columns a) and b) of the images, one can see that there are a few particles on each wafer on the bottom row (oven-dried) pairs, but no particles on the top row (spin-dried) pairs. This indicated either that the oven-dry method was introducing a small amount of contamination or that the baths were slightly contaminated and spin-drying was removing the particles. Due to the purity of the chemicals used and the fact that the baths are not exposed to the cleanroom airflow, it is more likely that the convection oven, which was also used occasionally to bake photoresist, was contaminated. Column c) shows particle contamination for both wafers. Section 2.3.2.2 discusses the possibility that particles on the rinse water surface were drawn to the wafer by the repulsion of the water from the hydrophobic surface. By allowing some time for overflow of the rinse water to remove any surface particles, the number of defects from this process was significantly reduced.

The other processing steps, RCA2 (surface activation) and steam oxidation indicated other problems. The RCA2 results were uniformly poor, with large defects and number of particles, and this process was discontinued as a surface activation method. The bonding results for oxidation showed large voids, which may have been due to lack of surface activation or oxide non-uniformity, but no particles. The oxidation furnace underwent routine maintenance soon after this test and some problems, such as varying oxide thickness with the same process parameters, were corrected by recalibration of the steam bubbler and gas flow monitors. Bonding results after the maintenance for steam oxidation and P-Clean surface activation were void and particle free.

The EV501S bonder was installed about the same time as these tests were conducted and bonding trials still showed particle contamination. Knowing that the source could not be the processing, the cleanroom personnel reinstalled a particle counter near the bonding station. It was found that an object (besides a cleaned wafer), when moved over the first-loaded wafer's exposed surface, could lose particles which would fall onto the surface. Chapter 5 has more details on the procedure for loading wafers in the bond chamber. The operator's gloves were especially prone to particle generation. By avoiding motion over the face-up, first-loaded wafer, the number of particles detectable by IR imaging could be reduced to zero.

3.5 Summary

The first bonding trials using ultrathin silicon wafers showed that direct bonding was certainly possible, but that it was increasingly difficult as the wafers became thinner. Micro-Raman spectroscopy and XPS failed to show, within their detection limits, contamination by metals or foreign chemicals. Zygo® interferometer and AFM examinations of the surface quality revealed significant roughness, which increased with decreasing wafer thickness. These measurements also revealed minute particles that were unaffected by standard cleaning.

In response, Virginia Semiconductor, Inc. initiated a series of new polishing methods and introduced new cleaning methods into their fabrication process. The surfaces of ultrathin silicon wafers polished by the new methods were examined by AFM and Zygo®, and two processes were identified which had significantly improved the surface roughness. Bonding with the smoother wafers gave much improved results and indicated that bond quality was not dependent upon wafer thickness.

Ultrathin wafers had bonded in the first trials with such large surface roughness that even partial bonding was unexpected, by the standards of the literature. As increased flexibility was the one significant difference between ultrathin and standard thickness wafers, a model relating wafer thickness and surface roughness was constructed. It attempts to elucidate the limitations on surface features that can be accommodated by varying thickness of silicon wafers. The focus of the model was to provide a framework for the experimental results and to gain insight into the possibility of bonding ultrathin wafers to processed wafers with surface features, and curved or significantly non-flat materials.

Bonding methods, roughness reduction processes, ultrathin wafer handling solutions and particle and contamination controls have been continually developed throughout the course of this research. The following chapters relate some of the more significant solutions and developments that have led to the now routine use of ultrathin silicon wafers in fabrication of improved and novel devices.

CHAPTER 4

SURFACE MODIFICATION

In the previous chapter, it was seen that surface roughness and particles that were not removed by standard cleans deterred the bonding of ultrathin silicon wafers. While VSI set about improving the surface finish by alternative polishes, work was being done on other methods of improving surface roughness. In this chapter, alternate methods for reducing ultrathin surface roughness and removing contaminants such as the particles seen in Chapter 3, Figure 3.5, were researched. One process, referred to as oxidation smoothing, was developed that both removed the known contaminants and greatly reduced the overall surface roughness.

4.1 Introduction

Processes that were already available in our cleanroom were examined to see if these standard CMOS methods could remove particles and reduce roughness of ultrathin wafers. Physical methods of contamination removal, such as the use of a photomask scrubber, in which a strong jet of water scours across the wafer surface, led to breakage of the thinnest wafers due to the large force of the spray. The effect of other standard chemical solutions, such as concentrated hydrofluoric acid and RCA1 and RCA2, was investigated, but these either had no significant effect or removed some particles but greatly roughened the surface. Ultrasonic cleaning had no effect on particle removal.

The thinning process used by Virginia Semiconductor, Inc. (VSI) to fabricate ultrathin wafers most likely uses an etching solution to obtain the smallest thickness wafers. As only VSI knows the details of the process, any improvements in that method

would have to come from them. Standard chemical solutions had failed and physical methods such as scrubbing had proven too stressful for ultrathin wafers. Since the thinner wafers had the largest number of particles and roughness, a method for removing particles and reducing roughness was sought that subjected the wafers to the least amount of stress. Furnace processing is one method that subjects wafers to small, external physical stress. Moreover, furnace processing alters the wafer's surface in many cases. Alteration of the surface was exactly what was sought.

4.2 Oxidation Smoothing

At the suggestion of cleanroom personnel, a known method of recovering processed wafers for reuse was tried. The method, as they referred to it, is called a "denuding" oxidation. The oxidation of silicon whether in a "wet" or "dry process depends upon the consumption of silicon to form the oxide. A "wet" or "steam" process uses water vapor to induce the reaction of oxygen with silicon. A "dry" process uses only oxygen gas. In both cases, the silicon surface atoms of the wafer react with oxygen to form SiO_2 at the silicon/oxide interface. The depth to which silicon is consumed is approximately 46 percent of the final oxide thickness.

Because oxidation proceeds in all directions, albeit not always equally, a contaminant on the surface of a wafer will eventually be underetched. Oxidation will begin by consuming the surrounding surface silicon first. As it continues, silicon under the contaminant will be consumed, forming an oxide underneath the contaminant. If the oxide is then removed, so is the contamination. While this would probably remove the roughness "spikes" seen in Chapter 3, Figure 3.5, it was also thought that the consumption of silicon might have a positive effect on the surface roughness.

After ultrathin wafers were oxidized and stripped (of the oxide in HF), it was found that the process not only removed the unwanted particles, but also greatly reduced the overall roughness of the wafer's surface. As will be shown later in this section, the amount of roughness reduction depends upon the starting roughness and the oxide thickness. Some details of the oxidation process will be presented first. The details of the experiment and the results will follow. The section will finish with a simple model for the reduction of surface roughness and other discussion of the results.

4.2.1 The Oxidation Process

While the initial oxidation process, thickness less than ~ 200 Å is not completely understood, a fairly simple model, the Deal-Grove model, successfully explains the oxidation rates of thicker oxides [67]. As the width of the unwanted particles on ultrathin wafers is at least 1000 Å, an oxide thickness of about 1100 Å is required for complete underetching and is modeled well by Deal-Grove. The following derivation is taken from Reference [67].

First assume that one has a silicon surface covered by an oxide layer of thickness, x_0, as shown below in Figure 4.1. It is assumed that oxidation proceeds by the inward movement of a species of oxidant rather than by the outward movement of silicon. The transported species must therefore go through three stages:

(1) from the bulk of the oxidizing gas to the outer surface,

(2) across the oxide film to the silicon surface,

(3) where it reacts to form a new layer of SiO_2.

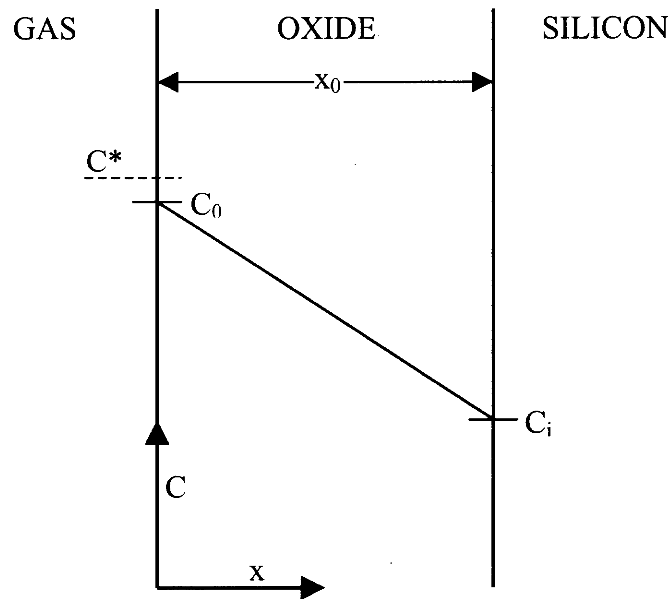


Figure 4.1. The oxidation process model showing the two interfaces and the relative concentrations of oxidant.

It is further assumed that the fluxes of oxidant in the three stages are equal (steady state). The flux from the gas to the outer surface of the oxide is taken to be:

$$F_1 = h\,(C^* - C_0), \tag{30}$$

where h is the gas-phase transport coefficient, C_0 is the concentration of oxidant at the outer surface, and C* is the equilibrium concentration of oxidant in the oxide.

The equilibrium concentration, C*, is assumed related to the partial pressure of the oxidant in the gas by Henry's Law,

$$C^* = K\,p. \tag{31}$$

The flux of the oxidant across the oxide layer is assumed given by Fick's law,

$$F_2 = -D_{eff}(dC/dx), \qquad (1)$$

where D_{eff} is the effective diffusion coefficient and dC/dx is the concentration gradient of the oxidizing species. From the assumption of steady-state, the concentration of oxidant in the oxide must be linear as indicated in Figure 4.1. Therefore the flux, F_2, is given by,

$$F_2 = D_{eff}(C_0 - C_i) / x_0, \qquad (2)$$

where C_i is the concentration of the oxidant near the oxide-silicon interface. And the final flux is that of the reaction between the silicon surface and the oxidizing species,

$$F_3 = k\, C_i, \qquad (3)$$

where k is the reaction rate constant.

In the steady-state, $F_1 = F_2$ and $F_2 = F_3$, and one can solve for C_i and C_0 in terms of C*. With C_i and C_0 eliminated, the flux is given by,

$$F = F_1 = F_2 = F_3 = kC^* / [1 + k/h + kx_0/D_{eff}] \qquad (4)$$

If N_1 is the number of oxidant molecules incorporated into a unit volume of the oxide layer, then the rate of growth of the oxide layer, dx_0/dt, is equal to F/N_1.

With the initial condition that $x_0 = x_i$ at $t = 0$, the solution to the differential equation, dx_0/dt, is,

$$x_0^2 + A\, x_0 = B\, t + x_i^2 + A\, x_i, \tag{5}$$

which can be written in the form,

$$x_0^2 + A\, x_0 = B\, (t + \tau),$$

where

$$\begin{gathered} A = 2\, D_{eff}\, (1/k + 1/h) \\ B = 2\, D_{eff}\, C^{*} / N_1 \\ \tau = (x_i^2 + A\, x_i) / B. \end{gathered} \tag{6}$$

The quantity τ represents a shift in time of the solution to account for any initial oxide on the surface of the silicon wafer. As for the other constants, B is referred to as the parabolic rate constant and A as the linear rate constant. These constants are different for the different crystalline planes of silicon, i.e. a <111> oriented wafer will oxidize at a different rate than a <100> wafer [68], process temperatures and conditions (wet or dry), and doping level of the wafer [69]. The oxidation rates for thin oxides are also higher than this model suggests and are of great interest to the semiconductor electronics industry. Gate oxides are now typically less than 100 Å. For additional information on the oxidation process, especially in the initial (< 200 Å) regime, the reader is referred to the literature [70-74].

4.2.2 Experimental Details

Ultrathin silicon wafers of thickness 20, 50 and 100 μm, <100> orientation, n-type doping, and resistivity ≥100 ohm-cm, underwent wet oxidation at 1050 °C to produce oxide thicknesses of 500, 1000 and 5000 Å. Average measured thicknesses were 485, 955, and 5010 Å, respectively. The oxides were then stripped away in a buffered oxide etch (BOE) of 6:1 ammonium fluoride: hydrofluoric acid solution (49%), just until the wafer surfaces were hydrophobic. Along with unoxidized reference wafers, all oxidized/stripped wafers were then examined by AFM. The power spectral density (PSD) and root-mean-square (RMS) roughness of each scan was then computed. In most measurements, the scan area was 10 μm by 10 μm, with 400 data points per line, corresponding to a PSD frequency range of 0.1 to 20 μm^{-1}.

The bondability of each surface was determined in a standard experiment in which the different wafers prepared above were subsequently oxidized along with normal thickness substrate wafers to an oxide thickness of 5000 Å, cleaned in sulfuric peroxide to activate the oxide, and then bonded in ultrathin/thick wafer pairs. The pressure required to initiate the bond, the relative contact wave speed and the relative bond energy before annealing were noted, and the fraction of bonded area after annealing in O_2 for one hour at 1100 °C was measured from IR photographs of the voids at the bonded interface.

4.2.3 Experimental Results

As expected from the starting roughness differences, the 100 μm thick wafers required the least oxidation, ~ 500 Å, to achieve the best surface quality. The 50 μm thick wafers required about twice as much oxidation, ~ 1000 Å, and the 20 μm thick wafers required an oxide thickness of at least ~ 5000 Å. The 50 and 100 μm thick wafers exhibit higher

frequency (smaller spatial extent) roughness after oxidation and strip, which can be seen by examining the edges of their AFM scans in Figure 4.2. The 20 μm thick wafer shows the largest reduction in roughness but the surface may not be the best possible. Longer oxidation times, greater oxide thickness, or a repeat of the process might reduce the surface roughness even further.

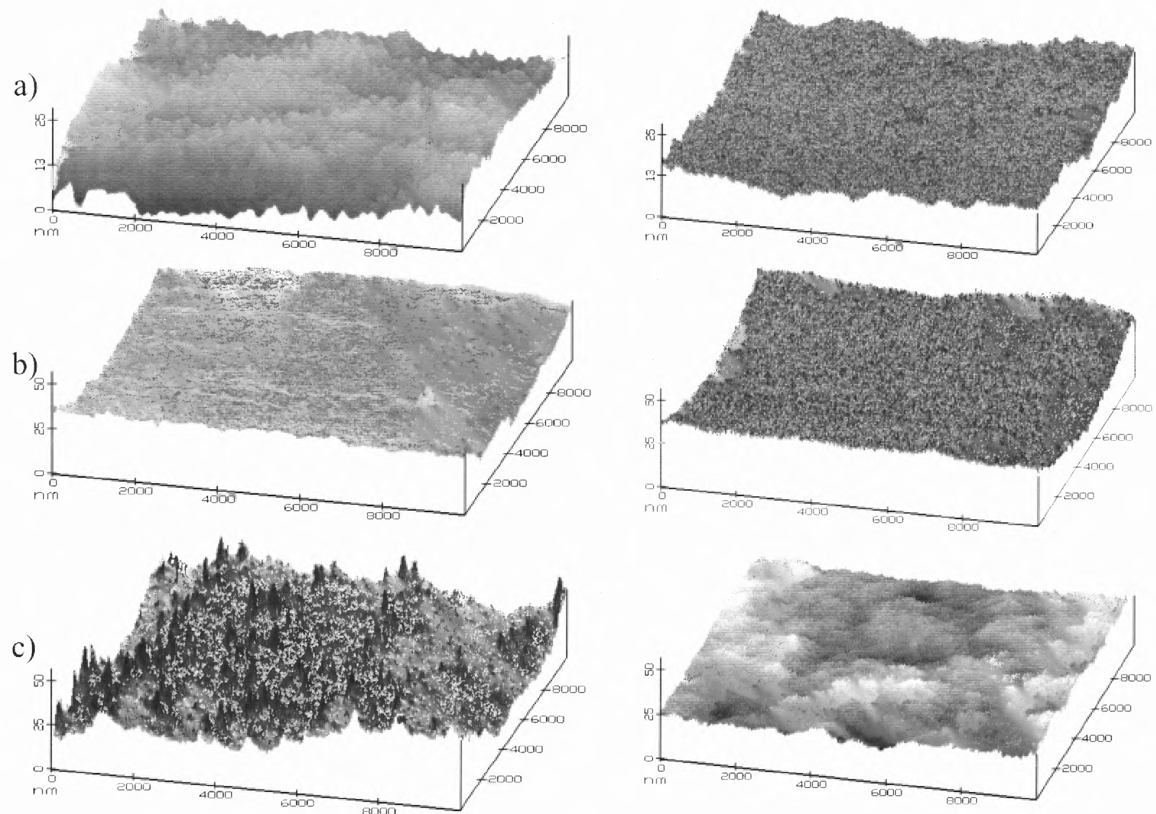


Figure 4.2. AFM scans of unoxidized (left side) and oxidized and stripped (right side) of wafers 100, 50 and 20 microns thick, denoted by (a), (b), and (c) respectively. Note the 100 micron thick wafer is shown with a vertical scale half that of the other wafers due to its relatively small roughness.

In Chapter 3, the roughness of wafer surfaces was characterized by a single number, the rms roughness, a statistical average of the deviation from a plane for all points in the scanned area. Surfaces with differing roughness and roughness scales can

therefore have the same rms roughness value, so this quantity can only be used as a "rule of thumb" for determining bonding behavior. A more informative measure of a surface is the power spectral density (PSD).

The Fourier transform of the discrete, vertical points scanned on a surface shows the varying scales of roughness and their respective amplitudes. Furthermore, this measure is independent of the bandwidth of the instrument doing the scan. The bandwidth limitations of an instrument are known directly from the extent of the frequencies that can be calculated. Since, the computation of the Fourier transform of a discrete set of data involves issues such as data windowing, correct scaling factors, the meaning of zero frequency, etc., the details are left to the interested reader. All calculations of the power spectral densities (PSDs) in this thesis follow the work of S. J. Fang, *et al.*, in Reference [75]. The evolution of PSD with increased oxidation can be seen in Figure 4.3 for 50 μm thick wafers.

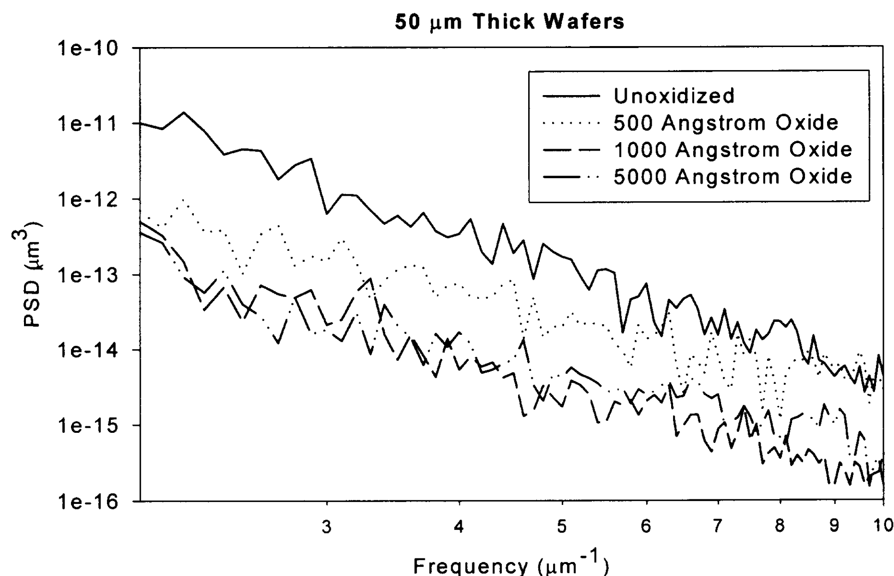


Figure 4.3. Change in PSD for a 50 μm wafer. The 500 μm oxide reduced the roughness by about an order of magnitude in this range. 1000 and 5000 Å thick oxides resulted in more than an order of magnitude reduction.

Notice that for the intermediate starting roughness of the 50 μm thick wafers, the PSD amplitude decreases in this frequency range by nearly an order of magnitude after the 500 Å oxidation, and by over an order of magnitude after the 1000 Å oxidation. The amplitude of the PSD at lower frequencies, 0.1 to 2 μm^{-1}, was reduced by about an order of magnitude for all oxidations.

No further significant improvement was observed for the 5000 Å oxidation over the entire frequency range. In fact, one unexpected consequence of longer oxidation is an increase in the higher frequency roughness components. This over-oxidation effect is shown clearly in Figure 4.4, which shows PSDs in the frequency range from 5 to 20 μm^{-1} for 100 μm thick wafers before and after a 5000 Å oxidation.

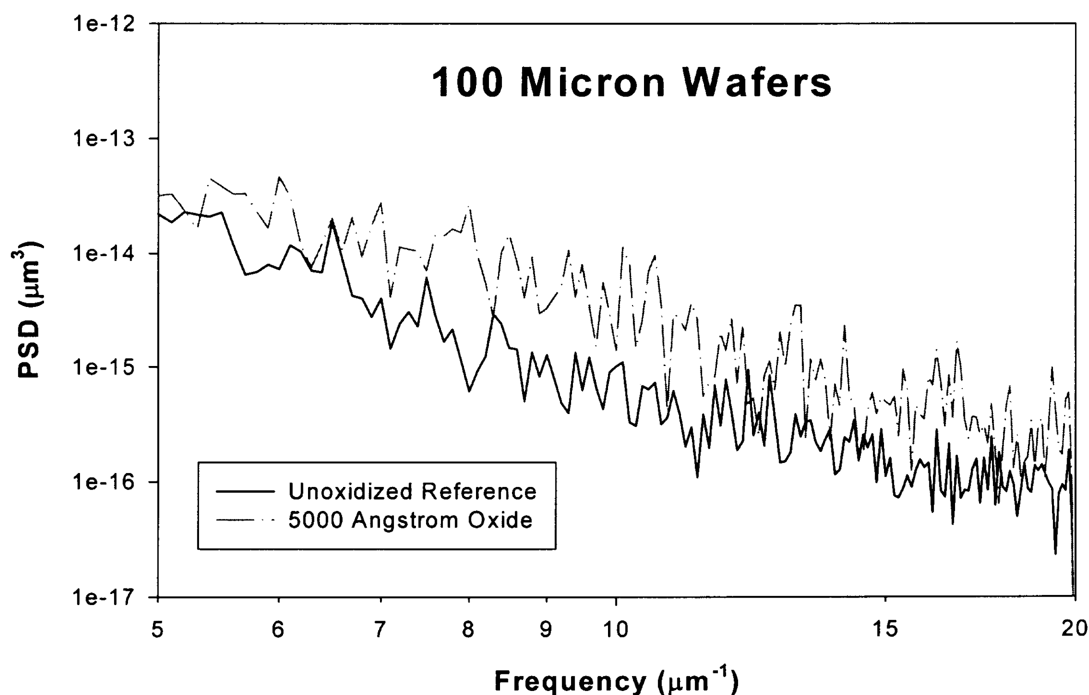


Figure 4.4. An increase in the higher frequency roughness was observed for 100 μm wafers oxidized to 5000 Å, longer than necessary to reduce the starting roughness to a minimum.

In this case, the roughness after oxidation exceeds that of the reference wafer surface by as much as an order of magnitude at some frequencies. It is important to note that in the low frequency region, from 0.1 to 5 μm^{-1}, the over-oxidation effect is not observed. Rather, the roughness after oxidation remains less than that of the reference sample. The increased high frequency roughness after over-oxidation may be expected to affect the bondability of these wafers, but this was not observed (see Table 4.1).

Table 4.1. Bondability results for ultrathin silicon wafers without (first three rows) and with (second three rows) optimum oxidation smoothing. The final row presents the results for over-oxidation.

Oxidation and Strip (Angstrom)	Thickness (microns)	RMS Roughness (Angstrom)	Pressure	Contact Wave Relative Speed	Relative Bond Energy before Annealing	Approximate % Bonded Area
No	100	12	Slight	Fast	Strong	95
No	50	15	Medium	Medium	Medium	<50
No	20	26	Large	Slow	Weak	<33
500	100	10	None	Fast	Strong	>95
1000	50	8	Slight	Fast	Medium	90
5000	20	8	Slight	Fast	Medium	<60
5000	100	15	None	Fast	Strong	>95

Table 4.1 correlates the oxidation smoothing effect with the bondability of ultrathin silicon wafers. We find that when no oxidation/strip is performed, the wafers with the smoothest starting surfaces are easiest to bond, but the bond results are not ideal. As shown in the table, when the oxidation/strip process is performed to produce the

highest quality surface prior to bonding, the best results are obtained, including little or no pressure required to initiate bonding, high relative contact wave speed, relatively strong bond energy before annealing and an increased fraction of usable bonded interface after annealing. Similar good results are obtained for the over-oxidized samples, indicating that the induced high-frequency roughness apparently has a smaller effect on the bondability of ultra-thin wafers than the low-frequency roughness below 5 μm^{-1}. This finding suggests that the low frequency range may be a critical region for predicting the successful bonding of the ultrathin wafers.

4.2.4 Discussion and Roughness Reduction Model

The oxidation of rough silicon surfaces results in a decrease in feature heights up to a point where high frequency roughness begins to increase. An increase in surface defects may explain this over-oxidation effect. It is well-known that an atomically smooth <100> surface is not thermodynamically stable [76], so after the initial roughness has been removed, defects would be expected to be created at the high oxidation temperatures. Furthermore, interstitial oxygen is known to be present in Czochralski silicon at a concentration of about 10^{18} cm^{-3} and may diffuse to the surface under the long growth time for thick oxides [77]. For evenly distributed oxygen, the surface concentration would have an average spacing of ~ 0.3 μm. This spacing corresponds to a frequency of ~ 3.3 μm^{-1} which is near the region of increased roughness.

Whatever the cause of this increased, high frequency roughness, there was no observed effect on the bonding of ultrathin wafers. Wafers with large roughness had those features reduced and bonding was substantially improved. An additional oxidation and strip might further increase the percentage of bonded area for 20 μm thick wafers.

The reduction of silicon roughness peaks by oxidation can be described using a straightforward geometrical model. A simplified geometry of a roughness feature is depicted in Figure 4.5 and serves as the basis for our model.

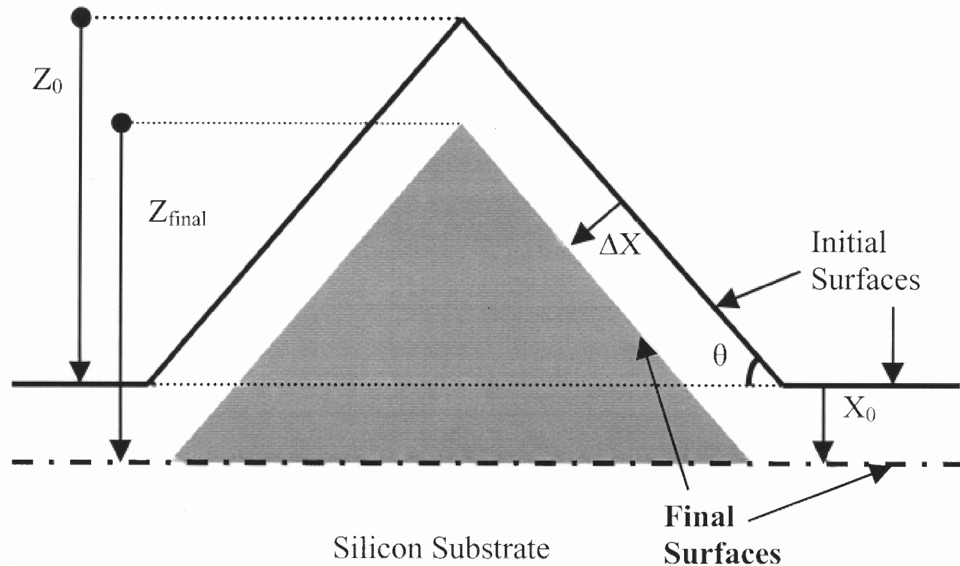


Figure 4.5. Model of the effect of oxidation on an idealized surface roughness feature. The roughness peak recedes to Z_{final} while the wafer surface moves down a distance X_0. Equivalently, the reduction in peak height is $X_0 - \Delta X/\cos(\theta)$.

Surface contamination and particles will leave a similar silicon shape after underetching. This model will therefore apply to surface roughness and to contaminant-induced roughness. Figure 4.5 shows the original surface of the wafer and roughness feature, and their expected shapes after oxidation for an arbitrarily short period of time.

Oxidation proceeds by the transport of an oxidizing species (H_2O or O_2) to the silicon-oxide interface where it reacts with a silicon atom to eventually form SiO_2. The oxidation process consumes a volume of silicon about 46% of the final oxide thickness. The oxidizing species can travel only a certain distance to form an oxide in any given time period. The maximum volume of silicon consumed at the peak of the roughness

feature is therefore limited by this distance and will, in general, be less than at the flat wafer surface. The point at which oxidizing species will just meet from either side of the roughness is the new peak of the silicon roughness feature. Assuming the oxidation consumes silicon perpendicular to the roughness surface a distance ΔX, the intersection will occur at the original feature height Z_0 minus ΔX/cos θ. The wafer surface will also recede during this time and will be a distance X_0 below its starting level. Therefore, the final height of the surface, Z_{final}, will be the initial height minus the difference between the reduction in the peak height and the reduction of the wafer surface height. That is,

$$Z_{final} = Z_0 + (X_0 - \frac{\Delta X}{\cos(\theta)}) \cdot \qquad (29)$$

If the silicon consumption distances, X_0 and ΔX, are proportional to each other such that,

$$\Delta X = C * X_0 \ , \qquad (30)$$

then the change in height is given by,

$$\Delta Z = X_0 * (1 - \frac{C}{\cos(\theta)}) \ . \qquad (31)$$

Reduction by oxidation of the height of the roughness peak requires that,

$$C > \cos(\theta) \ . \qquad (32)$$

By approximating the surface of the roughness feature to be a silicon crystalline plane, the angle between the flat surface of the wafer and the surface of the roughness feature can be represented as the dot product of the two planes. Thus,

$$C > \frac{\langle h,j,k \rangle \bullet \langle l,m,n \rangle}{|h,j,k| * |l,m,n|} \quad , \tag{33}$$

which allows comparison of the observed reduction process to known data on the oxidation rates of the various planes in silicon.

For example, a <100> roughness feature on a <111> wafer surface requires C to be greater than 0.577. The smallest ratio of <100> to <111> oxidation rates is 0.571, using the linear rate constants in the Deal-Grove model of oxidation at 1000 °C for wet thermal oxidation [78]. The parabolic rate constants, which dominate for oxides thicker than a few hundred angstroms, are nearly identical, i.e. the ratio is ~ 1. Thus, in this interpretation, individual <100> roughness peaks on <111> surfaces will not change their heights after brief oxidations where the linear rate constants dominate, but for thicker oxidations where the parabolic rate constants dominate, significant reduction in peak heights would be expected. The PSD reductions for different oxide thicknesses in Figure 4 are consistent with this expectation.

The model also suggests that because cos(θ) will always be less than one, in lieu of thermal oxidation, any etchant that anisotropically oxidizes silicon, i.e. oxidation ratios are ~ 1, and removes silicon dioxide may be sufficient to reduce the roughness. For either method, thermal oxidation and strip or the use of an oxidizing etchant, the desired surface features must accommodate some amount of silicon consumption.

4.3 Hydrogen Annealing

Another method that has been shown to reduce silicon surface roughness is hydrogen anneal. In this process, wafers are baked at elevated temperatures in a furnace in which hydrogen gas flows. This method can produce atomically flat silicon surfaces and is used in epitaxial deposition on silicon.

The primary cause of surface defect rearrangement appears to be due to the high temperature of the anneal. The activation energy required to move surface defects, kinks steps and other features may be reduced by the presence of hydrogen or the use of hydrogen plasma pretreatment. The vertical scale presented in the literature is on the order of several atomic layers. The scale of roughness of ultrathin silicon is tens of nanometers, an order or two of magnitude greater. Experiments with ultrathin silicon wafers for anneal times up to 5 hours showed no significant effect on the surface roughness. While use of this process may reduce the high frequency, i.e. small wavelength, roughness, the lack of appreciable effect on bonding by this scale roughness (such as that induced by over-oxidation) did not warrant further study of this method. The reader is referred to the literature for further information on this phenomenon and the significant impact it has had on surface and solid state physics [79-82].

CHAPTER 5

HANDLING AND PROCESSING OF ULTRATHIN SILICON WAFERS

This chapter concerns the handling and processing of ultrathin silicon wafers. Due to their extreme thinness, ultrathin wafers cannot withstand forces as strong as normal thickness wafers can, but they are much more flexible. This flexibility allows forces to bend wafers far beyond that which would break a normal silicon wafer. Figure 5.1 is picture of a 10 microns thick silicon wafer from VSI being flexed in a person's hand. At this thickness, a wafer can be rolled into a tube. Of course, as the thickness increases, the flexibility decreases and wafers will bend less before fracturing.

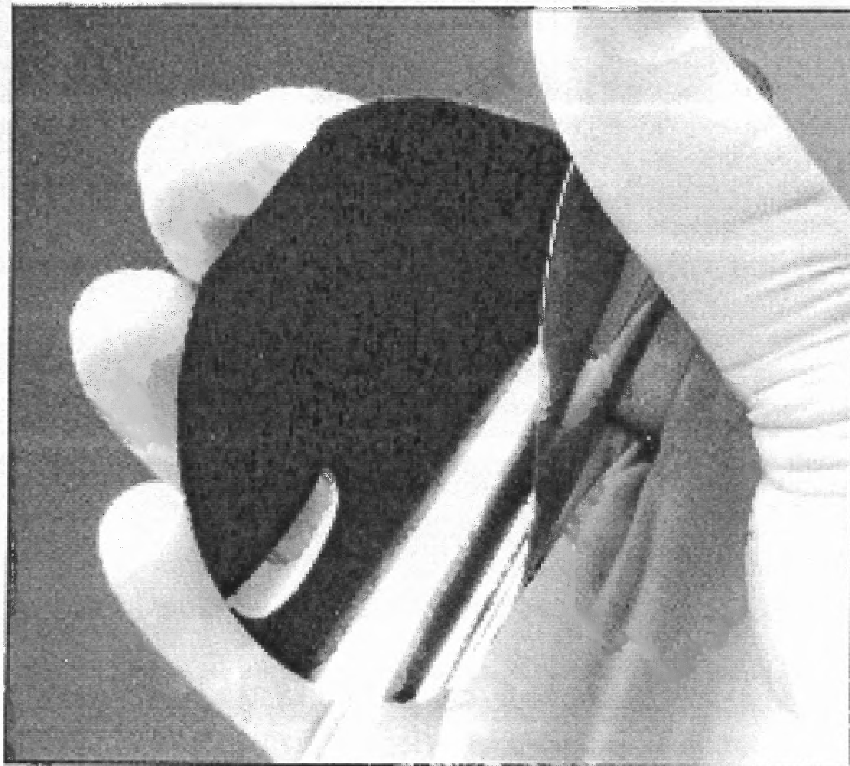


Figure 5.1. Reproduction of VSI advertisement showing the extreme flexibility of a 10 mm thick silicon wafer.

The crystalline structure of silicon determines how it fractures or breaks. This characteristic is employed in cleaving to separate devices fabricated on silicon wafers. A small scratch, or scribe, is made in the direction of a crystalline plane while the wafer is seated on a raised edge. When the hanging portion of the wafer is pressed, a crack will propagate from the scribe along the crystalline plane. If the raised edge is oriented with the crystalline plane, the hanging portion of the wafer is split or cleaved off cleanly from the remaining wafer. The scribe mark, having thinned and weakened that area of the wafer, initiates the split that continues along the crystalline plane. The edges of the two pieces (the hanging and remaining wafer) will be straight and relatively smooth. In amorphous material, the crack initiated by a scribe may propagate randomly, leaving jagged and rough edges.

The direction of the applied force is therefore important when handling ultrathin wafers. A sharp blow to the edge of a secured wafer may only chip a normal thickness wafer, but may shatter or crack an ultrathin wafer. Conversely, the same force applied perpendicular to the surface may crack or shatter a normal thickness wafer, but only bend an ultrathin one. This dichotomy can be beneficial or detrimental depending upon the direction and magnitude of the forces. As an example, relatively small capillary forces can cause ultrathin wafers to adhere strongly to surfaces, but not affect thick wafers, while high-stress depositions may cause normal thickness wafers to crack, but may be accommodated by ultrathin wafers.

Bonding trials (Chapter 3) with ultrathin wafers have shown that, above ~100 microns in thickness, these wafers can be processed as normal thickness wafers. Some care should be exercised as these wafers will not withstand rough handling quite as well

as normal thickness wafers, but otherwise no special procedures are necessary. Even spin-drying was possible with 100 microns thick wafers, but this is not recommended due to the difficulty of cleaning these machines if a wafer should break, and the resultant ire of the cleanroom staff. At or below 100 microns, ultrathin wafers require some additional restraints on handling and the use of alternate processing methods that are nonstandard, but generally available in a CMOS foundry.

The following section details the manual handling requirements and adjusted processing steps that most general fabrication methods might entail when ultrathin wafers as used. Specific solutions will be presented for particular challenges encountered in this research along with a broader discussion of the physical causes and effects. This should allow the reader both to follow the same steps used in this research and to extend the use of ultrathin silicon wafers to new or different processes. As an example, the use of handle wafers should allow ultrathin silicon wafers to undergo all CMOS processes, even automated handling, as long as the bond between handle and ultrathin is not compromised. The handling requirements of our automated bonder system, EV501S, will then be detailed. The methods employed should be applicable to other automated systems with similar configurations. A final section will recap the most important and general ideas.

5.1 Manual Handling

5.1.1 General Considerations

Tweezers with individual tines are not recommended since the wafer can fit in between those tines and be broken when the tweezers are compressed. Those with raised edges, used to limit their contact to the wafer edge, have been the most significant cause of loss

due to forceful contact with the thin silicon wafer's edge. Vacuum wands may be used if the vacuum is kept low and widely distributed, but the maximum amount of vacuum that can be used decreases as the wafer thickness decreases. Plastic tweezers are recommended since they are unlikely to damage the ultrathin wafer surface and generally do not have raised edges or tines.

5.1.2 Wet Processing

Wet processing of ultrathin silicon wafers presents a few challenges that may not be easily remedied. The first and most obvious inconvenience, to anyone who has tried processing these wafers, is that thin wafers float. The decreased mass of the wafer means that it will not immediately sink into a solution. Fortunately, wafer retainers, which fit over the carrier tops, are available and prevent this from becoming a problem in most cases. If the carrier is dropped rapidly into the solution, however, an ultrathin wafer may bend, twist, and ultimately slide out between the retainer bars. Similarly, agitation of the solution should also be kept to a minimum to prevent the same occurrence.

The second challenge arises from the attribute that makes thin wafer bonding possible, attraction to other surfaces. The origin of the attractive force can be the surface energy of silicon, adsorbed water or other molecules, or an electrical charge might be imparted by the reactions of chemical solutions. In any case, ultrathin wafers with an attractive potential and their inherent flexibility can move large distances in order to adhere to another attractive surface. Normal thickness (300 – 500 microns) wafers are generally restrained by their weight or by partitions such as carrier slots from moving in response to an attractive surface. Ultrathin wafer, on the other hand, have greatly reduced weight and can bend and twist to get past small partitions.

For these reasons, when processing in chemical baths, ultrathin wafers cannot be placed in slots directly adjacent to any other wafer. Attractive forces can be strong enough to cause these wafers to flex further than the distance between slots and spontaneously bond. They can even cause ultrathin wafers to jump slots in an effort to bond. This effect can best be seen as a wafer carrier is removed from the rinse water of a surface activating chemical bath. The water adhering to the wafers' surfaces and the increased surface energy due to the activation can have ultrathin wafers skipping across multiple slots. If this does occur, the easiest solution is to return the carrier to the rinse water (stopping any overflow), twist it from side-to-side until the wafers separate, and then carefully move the wafers far apart while they are still submerged. If using a retainer, be sure to remove it before returning the carrier to the rinse water. In addition, if an ultrathin wafer has bonded to another surface in this manner, its surface may have been roughened and subsequent bonding may be impaired. Experience with different thickness wafers will teach the operator how far apart ultrathin wafers must be kept to prevent slot hopping.

An alternate solution to having many empty slots between ultrathin wafers is to use buffer wafers. Since normally only one side of a wafer is to be bonded at a time, single-side polished wafers can be placed in proximity to ultrathin wafers with the rough side between them. The backside roughness of these wafers is less attractive to the ultrathin wafer and if contact is made, it is unlikely that the bond will be strong. The desired bonding is then done with the side of the ultrathin wafer that did not contact the buffer wafer. The attractive forces can be offset by careful positioning of single-side polished buffer wafers between ultrathin wafers.

While in the bath, some agitation of the carrier may be necessary in order to separate ultrathin wafers and buffer wafers, and allow the solution to act upon all surfaces. This generally means that there will still be need for empty slots, but the use of buffer wafers minimizes the number. Caution and experience will show how much agitation of the carrier is needed, and how far apart the buffers and ultrathin wafers should be placed.

Another challenge in wet processing comes from surface tension and other liquid forces upon removal of the wafers from the bath. These attractive forces can cause an ultrathin wafer to adhere to surfaces not normally attractive to silicon, such as the Teflon® carrier slots and even tweezers. These forces do not generally affect a normal thickness wafer, but for ultrathin wafers, with their reduced rigidity and mass, unexpected adhesion from liquid forces can lead to wafer loss. For example, liquid adhesion to a carrier slot effectively clamps the edge of the thinnest wafers, below about 20 μm thick, and attempting to move these wafers can result in fracture along the slot edge, just as in cleaving wafers mentioned above. Because of this, ultrathin wafers should be dried completely, in the carrier if possible, before handling with tweezers. Figure 3.9 (c) shows the result of attempting to remove a 10 microns thick wafer before it was completely dried. Bear in mind that some water may be trapped between a wafer and the carrier slot long after the visible water has evaporated or otherwise been removed.

5.1.3 Drying

Spin drying is not a feasible method of drying ultrathin wafers since, below 100 microns thickness, they cannot withstand the forces to which wafers are subjected. Blow-drying ultrathin wafers with filtered gas, a process used in the preliminary bonding trials, was

eventually replaced by heating, above 100 °C, the entire carrier full of wafers in a standard convection oven. The force of blow-drying occasionally caused the thinnest wafers to cleave along slot edges (as described above) or forced flexible wafers to jump slots and adhere to other wafers, or otherwise suffer some chipping or cracking. The filters used on the gas line also had to be replaced frequently or blow-drying would become another source of contamination.

By using a convection oven, wafer loss and damage was reduced. Unfortunately, this oven was also used for photoresist baking and it did contribute to wafer contamination. A dedicated oven would probably eliminate or greatly reduce the number of particles introduced by this drying method.

Other non-contact, forceless methods of drying, such as isopropyl alcohol (IPA) or Infrared (IR) lamps, may reduce wafer loss and particle contamination during the drying step, but they have not been explored in this thesis.

5.1.4 Furnace Processing

Wet oxidations have been performed with ultrathin wafers as thin as 15 microns, without breakage and with good uniformity of the grown oxide. The main difficulty in processing arises from the way the wafers are held in the quartz "boats" used in furnace processing. In these boats, the wafers are held vertically in slots of quartz bars arranged symmetrically around only the bottom of the wafer. There is a constant flow of gas through the furnace tube and this effective wind can cause the top portion of the ultrathin wafers to bend. This flexure causes variations in oxide thickness. When stripped, these variations, which imply differences in amount of consumed silicon (see Section 4.2.4), manifest themselves as roughness that deters bonding in those areas.

Baffle wafers of normal thickness can minimize the flexure of the ultrathin wafers and reduce the oxide variation near the boat slot. When placed on either end of the boat and between ultrathin wafers, the baffle wafers reduce the force of the gas flow. While this does not eliminate the variation in oxide thickness around the support slots, the manifest roughness is reduced enough for ultrathin wafers to bond in those areas. An enclosing boat, with quartz slots all around the wafer might reduce the observed variations, but may just as well increase the number of problem areas. A simpler solution might be to reduce the gas flow in the furnace tube and increase the process time. Baffle wafers on the boats end slots is recommended for all thickness wafers due to the observation that wafers in these positions experience that largest variations in oxide thickness.

5.1.5 Other Processes

The processes used in this thesis prior to bonding of ultrathin wafers were wet chemical cleaning and oxide removal, convection oven and blow drying, oxidation and annealing in forming gas (hydrogen annealing, Chapter 4, Section 4.2). Annealing is performed in the same type of furnace as oxidation but in different gaseous atmospheres and/or temperatures. Other processes such as Reactive Ion Etching (RIE), Chemical Vapor Deposition, sputtering and lithography were not tested with ultrathin wafers. A handle or support wafer would probably be needed to keep ultrathin wafers from breaking, bending, or otherwise moving. Handle wafers are described in more detail in the next section. Lithography, for example, has strict demands on the flatness of the wafer surface due to a small depth of focus. If the surface is outside this range, features imaged on it will be blurred at best. A photoresist coating also needs to be spun on at high rotation speeds.

5.2 Automated Bonding

During the course of this thesis work, an automated bonding system from Electronic Visions Inc. was purchased. The EV501S is capable of performing direct, anodic and thermal compression bonding, under vacuum or in a supplied gas, of wafers 4, 5 and 6 inches in diameter in a repeatable fashion. As much as 2000 volts can be applied for anodic bonding, 2500 Newtons pressure for thermal/compression bonding, vacuum as low as 10^{-6} Torr and the wafers can be individually heated up to 550 °C.

Wafers to be bonded are loaded into a chuck that has three removable flags that separate the wafers. Loading can be done into a manual chuck, for flat-to-flat alignment, or an alignment chuck, that has openings for visual and IR alignment using the separate alignment tool. Flat-to-flat alignment can be accurate to ± 10 microns, while visual and IR alignment can be as high as ± 1 micron. Since this thesis has dealt with blank ultrathin silicon wafers, only flat-to-flat alignment was used. Without alignment marks, visual or IR alignment could not be performed. For the manual alignment, the chuck can be loaded directly in the bonding chamber. For visual and IR alignment, the chuck needs to be transported to the bond chamber from the alignment tool.

The bond chamber consists of supports for the wafer chuck, inlet ports for gases, three actuator arms to remove the separation flags when required, a chuck temperature sensor, and ports to pressure sensors and vacuum pumps. The backside support for the chuck can be heated. The lid of the chamber consists of a circular, machined plate with a spring-loaded metal/ceramic pin in the center and an electrode for supplying voltage for anodic bonding. This electrode has been removed in Figure 5.1. It would be located along the groove almost directly below the center pin. The circular, machined plate is mounted on the end of an adjustable piston that is surrounded by IR lamps.

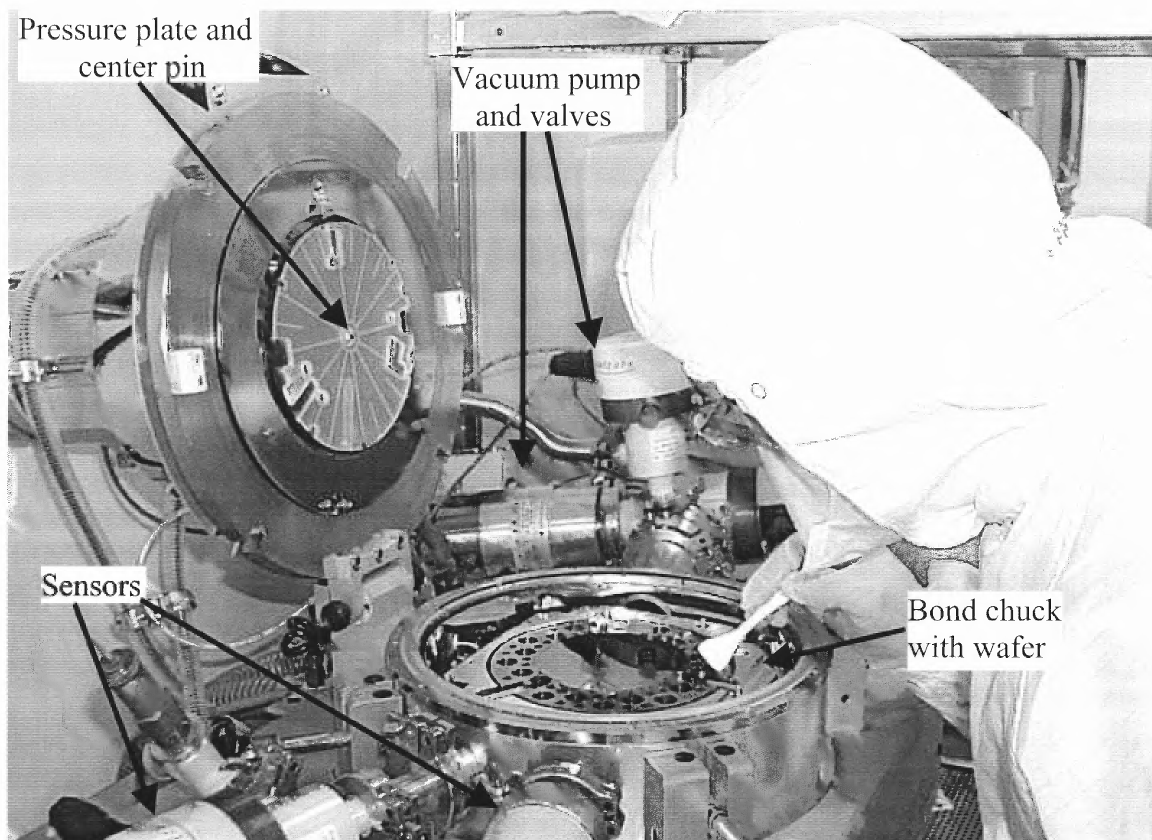


Figure 5.1. Photograph of the bond chamber of the EV501. Operator is has already loaded one wafer on the bond chuck. Several features are noted.

5.2.1 Basic Automated Bonding Process

The first wafer is placed on the chuck with its bonding surface up. The separation flags are pushed in and the second wafer placed on them. The piston height is adjusted for the thickness of the wafers and for any distributing electrode placed over them (for anodic bonding). The chamber is closed and sealed. Vacuum or a specific gas can then be introduced into the chamber and the wafers heated from one side or the other or both. The piston then lowers the plate until just the center pin pushes the two wafers together (if the piston height is correctly set). The pressure of the pin, which can be adjusted between ~ 0 and ~ 20 Newtons (N), should initiate bonding at the center of the wafers.

The contact wave spreads (ideally) continuously to the edges where the flags still separate the wafers. The flags are then removed and the bonding (ideally) completes. The piston can then apply force to the wafers, the electrode voltage, and the IR lamps and backside support, heat. The most difficult steps are before the chamber lid is closed and sealed. In order for complete and successful bonding, the wafers must be particle free, properly aligned (within alignment limits), sufficiently separated to prevent uncontrolled bonding, and with one wafer flat against the bond chuck and the other supported parallel to it by the separation flags.

5.2.2 General Handling Considerations

The first source of possible problems is the loading of wafers onto the bond chuck. The first wafer has its bonding surface up and fully exposed to the environment before the other wafer is placed above it in close proximity. Since all things are a possible source of particles, nothing, including the operators hands, should be above this first wafer surface. Extreme care has to be exercised when loading the second wafer not to scratch the surface of the bottom wafer or introduce particles.

During the search for sources of particle contamination in wafer bonding (Chapter 3), it was found that the operator's gloves are the single largest generator of particles in the cleanroom. The stretch of the gloves' material when flexing one's fingers releases a shower of particles. Therefore, the operator's hands, especially, should never be above the first wafer surface while it is exposed.

When placing the second wafer, a bent vacuum wand was the best tool if the wafer was thick enough to withstand the pressure difference. The chuck sits below the rim of the bonding chamber and there is not enough room to comfortably accommodate

hands and tweezers when placing the second wafer. This wafer needs to be held parallel to the first and set down lightly on the flexible separation flags. Angled tweezers do help but are generally metal and these can roughen the surface and cause poor bonding. In addition, the thickness of the tweezers is usually greater than the separation flag thickness. Even with angled tweezers, it is difficult to avoid touching the first wafer surface with either the bottom of the tweezers or the second wafer's edge. Either contact could scratch the first wafer's surface.

One of the only ways to avoid this contact is to hold the second wafer on an edge opposite to the location of a separation flag, place the wafer edge onto this first flag, and then ease the tweezers out between the wafers while settling the second wafers on the two remaining flags. Doing this correctly takes practice and a steady hand.

Since the vacuum wand holds the second wafer by suctioning to the back surface, this wafer can be held parallel to the first, if the wand is bent enough, and laid down on the three separation flags at once. Contact between the wafers or between tweezers and bonding surfaces can be avoided. While a steady hand is favorable, this loading method requires little dexterity and vacuum wand use may already be well known to the operator.

The thickness of the separation flags must also be considered if bonding is to be successful. If they are too large and the wafers do not flex sufficiently, contact will not be achieved with the relatively small pressure exerted by the center pin. If the flags are too small, the wafers may contact spontaneously and randomly. Random and multiple contact points may generate several contact waves which may trap air (if bonding at atmospheric pressure) or form voids (if bonding in vacuum). The thickness of the separation flags is accounted for in the piston height setting, which determines how much

pressure, if any, is exerted by the center pin. Ultrathin wafers, with their ability to flex and to even jump carrier slots, were not controlled by even relatively (at most 500 microns) thick separation flags.

5.2.3 Ultrathin Wafer Bonding

In Section 5.1.2, it was noted that ultrathin wafers are extremely attractive to other surfaces. While high surface energy promotes bonding and is generally beneficial, the flexibility of these wafers means that any other attracting surface within several centimeters can be spontaneously contacted. This randomness and spontaneity means that bonding can initiate anywhere across the surface and even at several places at once when ultrathin wafers are loaded on the bonding chuck. This leads to trapped gas pockets or voids and generally poor bond quality.

5.2.3.1 Separation Flags The separation flags are the only means by which the two wafers are kept apart in the automated bonder. For normal thickness wafers that are rigid, flags of 50-100 microns thick are sufficient. For wafers down to ~ 80 microns, 100 micron thick flags may be sufficient, but as the wafers get thinner, the separation, or flag thickness, must be greater. It was found that for 50 microns thick wafers, separation flag thickness of even 500 microns did not always prevent spontaneous bonding. Constructing even larger flags would be expensive and would soon interfere with the operation of the pressure plate. The center pin only extends a few millimeters. Larger separations would prevent the center pin from initiating contact.

With 500 microns thick flags as a practical limit, another solution needed to be found for preventing spontaneously and random bonding of ultrathin wafers. Since the difficulty arises from the flexibility of the wafers, a method was sought to make the

wafers more rigid. If an ultrathin wafer were already attached to a thick, relatively inflexible substrate, it would not be able to flex very much. The questions that needed answers were how to attach the wafer in a temporary manner to a substrate in a way that would not overly interfere with the bonding process and what material to use.

5.2.3.2 Handle Wafers The strong adherence of ultrathin wafers to other surfaces when wet, a difficulty in chemical processing, was used to an advantage. A small drop of water was placed on the rough backside of a single-side polished silicon wafer. This material was chosen because the wafer surface, although rough, is very flat and the rough surface prevents any strong silicon-to-silicon bonding. When the ultrathin silicon wafer is brought into contact with the wet surface, a strong bond is formed by the thin layer of water. The wafer pair exhibits the flexibility of the thick wafer, which allows automated bonding to be performed in a controllable manner. The main difficulties of this method are aligning the flats of the two wafers, so that alignment on the bond chuck is acceptable, and contacting the two wafers in a way that allows the water layer to spread evenly between the surfaces.

One way this can be performed involves two plastic tweezers. One holds the wafers together at their flats and the other holds the ultrathin wafer far apart from the rough, wet wafer. Once acceptable alignment is achieved, the one tweezers clamps the wafers together at their flats, and the other slowly lowers the ultrathin wafer while controlling the contact. As the wafer is lowered, contact will spread from the flats, across the wafer surface until only the tweezers keeps a small area separated. Since the water is not usually distributed evenly across the rough wafer surface, the first time the wafers are water bonded, they will probably not be flat. The tweezers holding the wafers apart at the

edge can be slowly inserted into the interface. If done carefully, the two wafers can be completely separated. As long as water remains, the wafers can be separated and bonded repeatedly until the alignment and flatness is satisfactory.

After the ultrathin wafer has been bonded to the desired wafer or material, the handle wafer is heated until the water bond is broken and then removed. If the handle wafer does not immediately drop off after the water is gone, inserting tweezers between the handle and ultrathin is usually sufficient for the wafer to separate completely. Another way to separate off the handle wafer once the desired bonding has been achieved is to place the three-wafer stack in vacuum where the water will rapidly sublimate. This is a limitation though, if the desired bonding between the ultrathin wafer and other material must be performed in vacuum to prevent trapped gases.

5.2.3.3 Vacuum Bonding Ultrathin wafers can be bonded under vacuum in the automated bonder, assuming they can be kept separate by the flags, but using vacuum is not straightforward. The large suction created by the vacuum pump can pull an ultrathin wafer into the exhaust port or otherwise move the wafer out of alignment. The center pin can be used to hold the wafers together when vacuum is applied, but gas can still be trapped at the interface, especially if the wafers bond out to the flags. The water-bonded handle wafer will rapidly separate in vacuum.

A second handle-wafer method, developed by Dr. Suresh Sampath of the Microelectronics Research Center, uses photoresist instead of water to form the bond between handle and ultrathin wafers. A thin layer of photoresist, usually Shipley 3813, is spun on a standard thickness, polished silicon wafer surface at ~ 2000 rpm for 30 seconds to achieve a uniform coating about one micron in thickness. The wafer is then heated to

110 °C for 60 seconds (pre-bake). The ultrathin wafer is contacted in a like manner as the water-bonding method above, but the wafers are not as readily separated and rebonded if the alignment or flatness is poor. The pair is then heated to 115 °C for 60 seconds (post-bake) to obtain a strong bond. The photoresist will not be adversely affected by the application of vacuum when bonding the ultrathin wafer to another surface. Removal of the photoresist can be accomplished with acetone, if not hardened at 115 °C, or standard photoresist cleaning solutions. This debonding can be considerably time-consuming since the photoresist removal proceeds from the wafer's edges to the center. The temperatures, times and rotation speed are from the standard cleanroom process for photolithography, with bonding exchanged for the exposure step.

5.3 Recap

To a thickness of ~ 100 microns, ultrathin wafers can be processed like normal thickness wafer, but with some extra care to avoid rough handling. Below 100 microns, wafers cannot withstand spin drying or similar processes that subject the wafer to high stress. Only tweezers without raised edges or tines should be used when handling ultrathin wafers. Wet chemical processing requires the use of wafer retainers on the carriers and careful insertion and removal from the baths. Agitation of the baths should also be kept to a minimum. Handle wafers may be necessary in using the automated bonder and for any process where the flexibility of ultrathin wafers is a detriment. The overall conclusion is that experience decreases loss when handling ultrathin wafers.

Additional details, such as bath temperatures, oxidation temperatures and time, etc., on all processes can be found in the cleanroom travelers in Appendix A.

CHAPTER 6

APPLICATIONS FOR ULTRATHIN SILICON WAFER BONDING

Ultrathin silicon wafer bonding has been developed to the point where it can be used for prototyping and production. The surface quality has been improved by Virginia Semiconductor, Inc. to the point that roughness is no longer the dominant concern. In addition, a method of removing excess roughness has been discovered and elucidated, and handling issues have been resolved. Ultrathin silicon wafer bonding is now readily accomplished in NJIT's cleanroom. Now that the major issues have been resolved in bringing ultrathin silicon wafer bonding to the at least prototype production level, the final part of this thesis is to provide a few demonstrations of the usefulness of this new fabrication method.

Measures of the value of any new process include a reduction of cost and complexity, improved performance of existing devices, or the manufacture of novel designs not readily accomplished by existing processes. The following sections will describe devices produced by the author and other members of the Microelectronics Research Center that reduce cost and complexity, improve performance of existing devices, and enable new devices through the use of ultrathin silicon wafer bonding. A final section will spotlight a new Rapid-MEMS-Prototyping process developed at NJIT, which combines Deep Reactive Ion Etching (DRIE), SU-8 and ultrathin wafer bonding. While the examples highlight the work done mainly by other researchers, they illustrate how the research contained in this thesis, especially the handling and bonding methods used with ultrathin silicon, has spawned a variety of applications.

6.1 Introduction

The thickness of ultrathin silicon wafers lends itself to production of devices that can react to or upon the macroscopic world. As mentioned in Chapter 1 in the introduction and motivation of this research, semiconductor electronics typically use layers of materials measured on the scale of angstroms (or 1/10,000 of a micron). Some power electronic devices can require silicon layers of several microns thickness, but using ultrathin wafers to produce these would probably require bonding wafers thicker than needed, thus requiring a subsequent thinning process, the avoidance of which is a prime motivation for using ultrathin wafers in the first place.

Stacking circuits on multiple thick layers of silicon and protecting fabricated circuits by wafer bonding are two other possible uses for ultrathin silicon wafers in the field of semiconductor electronics. However, there is another field in which silicon layers of more than several microns are readily employed, miniaturization of optical and mechanical devices that can sense, probe, manipulate or otherwise interact with physical things other than electrons. This field is generally called MicroSystems Technology (MST) or MicroElectroMechanical Systems (MEMS).

The devices that will be discussed in the following sections can all be classified as MEMS. MEMS is a general term for devices that are not purely electrical in nature (e. g. microprocessors, computer memory), but react to or upon the environment and are miniature in scale. They can be the equivalent of large-scale devices such as switches, gears, and motors. One way to describe MEMS is as an extension of CMOS-type processing, an essentially planar technology that typically utilizes layers of materials less than one micron thick, into the third dimension where devices have vertical scales comparable to or larger than their planar extent.

A distinction between MEMS and other technologies may be made from the processing tools used. Miniature systems can be assembled (albeit with difficulty) by hand or formed by precision tooling. Nanotechnology makes use of the highest resolution lithography techniques such as electron beam lithography and methods such as self-assembly to make things on a near-atomic scale. MEMS devices generally fall somewhere in between what is possible with precision tooling and the cutting edge of atomic-level manipulation of materials.

Because of the scale, somewhere between angstrom (CMOS and nanotechnology) and fractions of a millimeter (precision tooling), MEMS can most benefit from the availability of single-crystal silicon layers of a few microns thickness. As a further incentive for using ultrathin silicon wafers, MEMS device fabrication often requires a sacrificial layer to release structures from a substrate. A buried sacrificial layer of precise thickness is readily obtained by bonding oxidized silicon wafers. Freestanding structures can then be fabricated directly by Deep Reactive Ion Etching (DRIE) to reach the oxide layer and released by selective chemical etching. Ultrathin silicon wafers have the additional benefit of being able to bond to surfaces with large roughness features, as would be found on processed wafers. This creates the possibility of creating true, three-dimensional devices that have multiple active layers.

The first device described is a pressure sensor head that was fabricated using ultrathin silicon anodic bonding to a micromachined glass substrate. The glass substrate was machined ultrasonically by Bullen Ultrasonic. Stephen Fu of Iota, Inc., 105 Lock St., Newark, NJ 07103, did assembly and testing of the device. The author's contribution was preparing the ultrathin silicon and glass substrate and performing the actual bonding.

6.2 Optically Interrogated Pressure Sensor

A schematic of the device is shown in Fig. 6.1. A thin silicon wafer is anodically bonded to a micromachined glass substrate, forming the pressure sensing diaphragm or membrane. The pressure sensor head is epoxied to a glass ferrule into which dual optical fibers have been inserted and secured. The assembly is then packaged for commercial use.

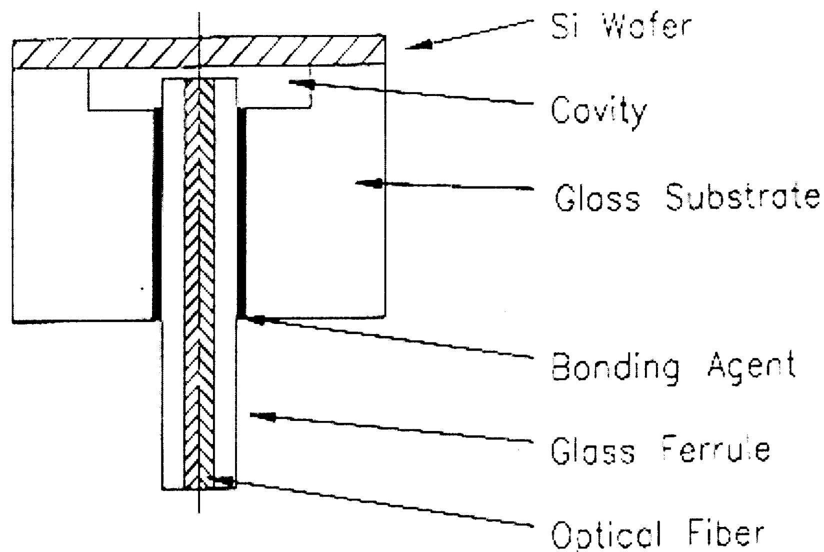


Figure 6.1. Schematic of pressure sensor head assembly showing optical fiber and glass ferrule.

Figure 6.2 shows an IR view of an anodically bonded 20 μm thick silicon wafer to micro-machined glass, forming the pressure sensor heads (of two sizes). The wafer is then diced and the individual sensors separated for packaging. The sensor itself is complete at this point. Note that the fabrication consists of only two steps, machining the glass and anodically bonding the silicon wafer. The remaining work involves the interrogation method assembly and the packaging.

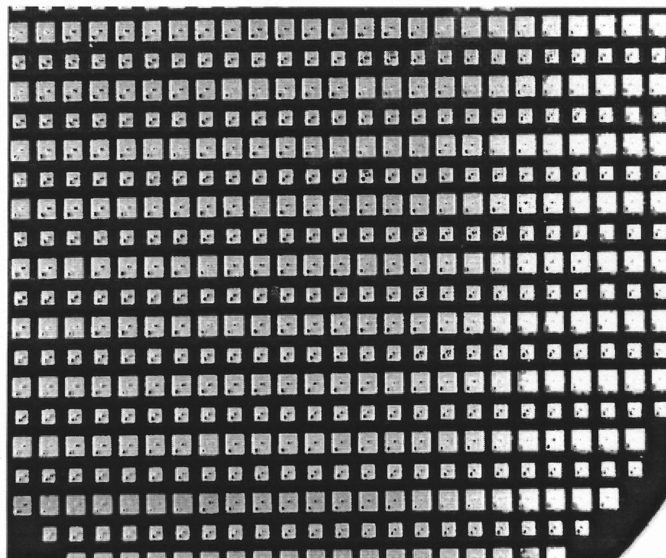


Figure 6.2. IR picture of bonded 20 micron wafer to machined Pyrex glass to form the pressure sensor head. The smaller squares are 1.2 mm on a side.

In optical interrogation, a fraction of the light sent through the optical fiber reflects back from the membrane surface and enters the second fiber. This reflected light is directed to a detector. The reflected intensity is linearly related, over a fixed region, to the distance between the fiber end and the membrane. Figure 6.3 is a plot of the relative intensity of the reflected light versus fiber position.

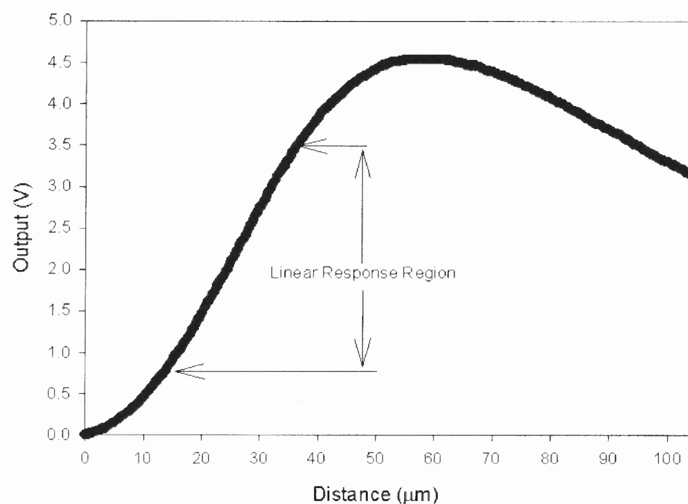


Figure 6.3. Relation between fiber to membrane distance and intensity of reflected signal.

A difference in pressure between the exposed and internal surfaces of the membrane causes a deflection. The magnitude of the deflection is dependent upon diaphragm thickness and can be approximated from standard models [83,88]. The working pressure range can then be estimated from the expected deflection magnitudes and the linear response region. Figure 6.4 shows the typical response of this pressure sensor within the linear range noted in the previous graph.

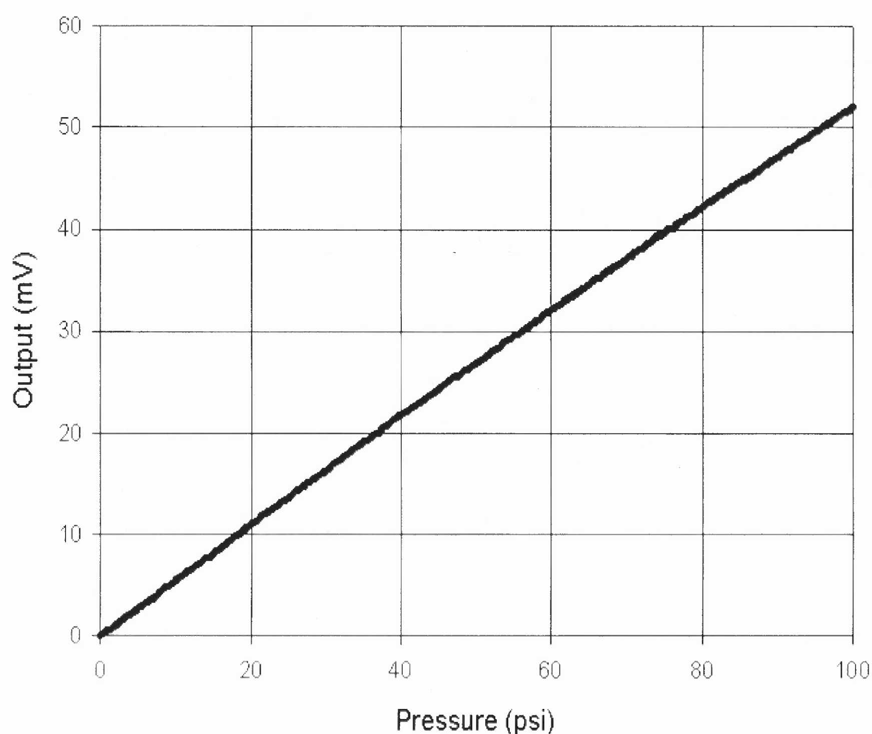


Figure 6.4. Graph of the response of the sensor to both increasing and decreasing pressure.

If the fiber is hermetically sealed then the pressure in the cavity is fixed for fixed temperature, and absolute measurements of pressure can be performed. An alternate design has an additional hole drilled through the glass wafer into the cavity. Pressure measurements are then relative to the surrounding air pressure.

The next few subsections outline some of the methods presently used to fabricate pressure sensors. This is to show the contrast between the complexity and, by extension, cost and repeatability (yield), of traditional processes and the use of ultrathin silicon wafer bonding. Following the fabrication sections, several interrogation methods will also be discussed. Optical interrogation was used in the present design, but the use of ultrathin silicon does not prevent the implementation of these other methods.

6.2.1 Fabrication by Deep Etching

Etching a hole almost completely through a starting material can form the membrane of pressure sensors. In silicon, potassium hydroxide (KOH) is widely used because its anisotropic etch forms a smaller diaphragm than isotropic etching. Timed etching is the simplest method of deep etching, but uniform membranes of exact thickness are difficult to achieve and membranes thinner than ~ 10 microns cannot be fabricated by timed etch alone [84]. In chemical etches, the composition of the solution can change over time, altering the silicon removal rate and reducing reproducibility. Implanted etch stop layers have been used to improve uniformity and thickness control for wet etching, but these methods can decrease the sensitivity of the device and alter the mechanical response of silicon [85]. The use of implanted layers restricts the type of etchant to those with sufficient selectivity between silicon and the implanted layer. The relatively new Deep Reactive Ion Etch process can remove large amounts of silicon with aspect ratios greater than 20:1, but this method suffers from depth control, similar to wet etching, and non-uniformity across the wafer. It is also increasingly expensive in proportion to the etch depth. DRIE would reduce device footprint compared to KOH etching, but the increased number of devices per wafer would probably not offset the cost.

6.2.2 Fabrication by Sacrificial Layers

Depositing polysilicon or other materials over a sacrificial layer has also been used to form diaphragms. This method requires etching completely through the backside of the wafer and then using a suitable etchant to remove the sacrificial layer. Thickness control is dependent upon the deposition and sacrificial layer removal process. Some drawbacks are that the mechanical properties of single crystal silicon are much better than polysilicon and that it is hard to grow high quality films greater than a few microns.

Zone melt recrystallization methods have been used to make the polysilicon film a single crystal, but the methods are complex and expensive [86]. Epitaxial growth of a material does allow precise control over the membrane thickness, but producing thick layers is difficult and time-consuming (expensive).

6.2.3 Fabrication by Bonding

Another fabrication method is to create holes and cavities in a substrate of glass, silicon or other material, and then bond a second layer over the cavities. This second layer is then thinned to the desired membrane thickness. As an example, the deep etching by KOH described above can be continued until a suitable size hole is opened in the silicon wafer. Over this, a second silicon wafer is then bonded and thinned [87]. A schematic of this type of pressure sensor is shown below in Figure 6.5.

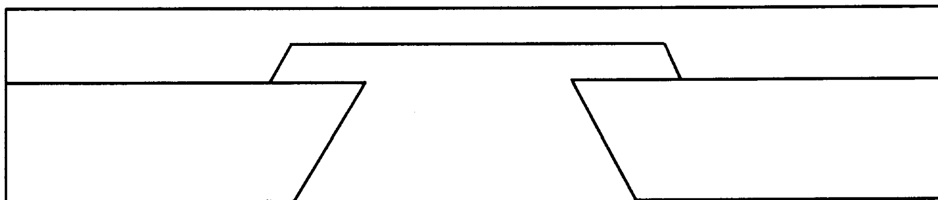


Figure 6.5. Schematic of a pressure sensor fabricated by through-wafer etching and wafer bonding and thinning.

The main drawback of this method historically has been the difficulty in obtaining consistent thickness and uniformity of the pressure diaphragm. The second wafer used to form the sensing membrane must be thinned to a few tens of microns. Implanted polish or etch stops can be used to help obtain a desired thickness, but doping control and uniformity can vary greatly across the wafer and between lots. The physical forces involved in polishing can also destroy the membrane or change its mechanical response.

As described in Reference [87], the implantation itself can alter the behavior of the membrane. If the bonded wafer is already the required thickness, all of the above issues are moot. By using ultrathin silicon wafers, the behavior of the sensor can be modeled accurately using only the known cavity size, membrane thickness and material properties, without processing-dependent effects.

6.2.4 Diaphragm Deflection Measurement Methods

Measurement of the deflection of the membrane or diaphragm can be made by such methods as piezoresitive, capacitance, and optical reflection changes. Piezoresitivity is the change in resistance of a material under mechanical stress. In silicon, the piezo effect is dependent upon the doping concentration and crystal orientation. Piezoresistive sensors typically use four small strain gauges coupled to form a Wheatstone Bridge on a diaphragm measuring about 1 mm in diameter. Diffusing p-type regions of high electrical conductivity into an n-type diaphragm can form the strain gauges. Sensors using this type of deflection measurement can operate from 100 kPa up to 10 Mpa [88].

If the diaphragm is one plate of a parallel plate capacitor, a change in the distance to the opposite plate will change the capacitance measured in a connected resonant LC circuit. The capacitor structure usually requires either some metal deposition or

implantation on the membrane. These devices are typically rectangular and measure ~ 2 mm on the longer side. Although the pressure ranges of capacitive devices are limited to 0 to 40 kPa, their sensitivity can be as high as 0.33 percent.

Optical methods utilize reflection of light off the membrane surface(s) to measure the position of the diaphragm. These methods can be interferometric or intensity based and, since their implementation does not require semiconductor processing, are typically integrated apart from the fabrication of the sensing membrane. Piezoresistive and capacitance measurements both require additional semiconductor processing. The strain gauges, plates of the capacitor, and other circuitry and connections to these components must be fabricated on the wafer, in addition to the membrane. The doping and/or deposited layers of other materials must also be taken into account when modeling the sensor response. In contrast, the optical fiber does not need to contact the membrane or be so close as to restrict its motion. Fiber optic operation is also immune to interference from electromagnetic sources.

6.2.5 General Fabrication Process

Pyrex glass wafers, 500 μm thick, were machined ultrasonically by Bullen Ultrasonic, Inc. to form the pressure sensor cavity and optical fiber feedthrough and vent holes. Two cavity sizes were fabricated on the same wafer (Figure 6.2 above). The feedthrough holes were 250 μm in diameter. The 20 μm thick, 100 mm diameter silicon wafers were produced by Virginia Semiconductor, Inc.

The silicon and glass wafers were cleaned in standard chemical baths prior to bonding. The Pyrex substrate wafer was first placed on the bond chuck. Then the ultrathin silicon wafer was placed on top, the bond chamber evacuated to 10^{-5} Torr and a

voltage of 1200V applied across the wafer stack for 3 minutes. The silicon wafer was positively charged with respect to the glass wafer. The bonded wafer stack was then diced. The final pressure sensor head dimensions were 1.5 mm x 1.5 mm square by 520 μm thick. Prior to dicing, the measured device yield was over 95%. Figure 6.6 shows a photograph of an optically interrogated pressure sensor head mounted on a glass ferrule. The thin dark layer at top is the 20 μm thick silicon wafer.

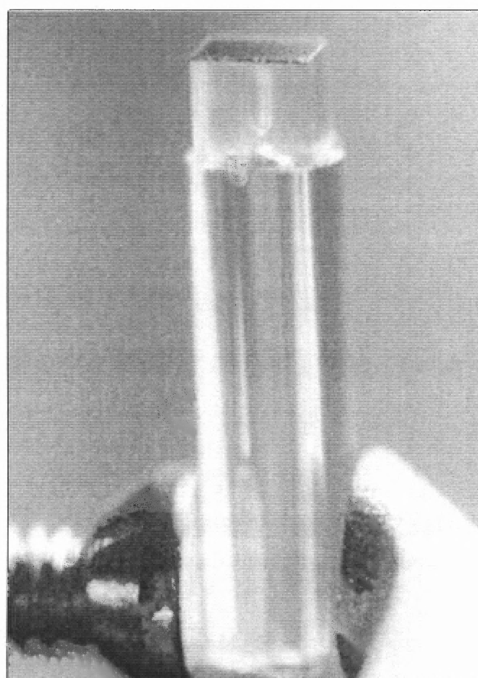


Figure 6.6. Photograph of a pressure sensor head chip mounted on a glass ferrule, which will eventually hold the optical fibers.

6.2.6 Advantages of the Alternative Technology

Ultrathin wafer bonding removes the thinning step from pressure sensor fabrication by bonding. No etching or polishing steps are required in fabricating the pressure membrane since the bonded wafer is already the desired thickness. The thickness variation, doping, and uniformity of the membrane are all known and controllable before fabrication.

In contrast, membrane thickness control is about 0.5 microns for etch-stop techniques of thinning silicon wafers and the membrane doping profile and concentration is dependent upon the specific etch or polish method [87]. The variability in membrane thickness of other technologies is eliminated, doping profile and concentration of the membrane is unrestricted, and the surface quality is comparable to that of unprocessed, normal thickness, prime grade silicon wafers. Optical interrogation is immune to electromagnetic interference and can be integrated into the device outside the cleanroom, which simplifies the semiconductor processing.

The fabrication of the pressure sensor head by use of ultrathin silicon wafer bonding is simple, reliable, and should be much cheaper than the other methods described. By using fiber optics integrated outside the cleanroom, the expense of implementing the interrogation methods is minimal. Ultrathin silicon wafer uniformity constrains the response of all sensors, across and between wafers, to a much more narrow range, which translates into higher yields.

6.3 Optical Modulators [89]

Optical fiber communications has a need for modulators to perform switching and add/drop functions. For twisted pair, copper wire telecommunications, these functions are electronically controlled. An optical equivalent can be as simple as a movable mirror. The light from a fiber reflects off the mirror surface. By changing the angle of the mirror, the light is steered in different directions. It could be directed into another fiber (switching or adding function) or off into space (drop function).The simplest variable mirror has two positions, flat or angled. To obtain repeated performance (or angle), the mirror is nominally flat and when switched, rapidly changes angle until hitting a stop.

The following work was done by Drs. Richard Brown and K. R. Farmer of the NJIT Microelectronics Research Center and V. A. Aksyuk of Bell Laboratories, Lucent Technologies, 700 Mountain Ave, Murray Hill NJ 07974.

They identified a need for large-area (~ 500 x 500 μm^2), variable mirrors for fiber optic communications. However, large, flat mirrors cannot be easily fabricated using conventional silicon deposition and micromachining technology. This is because the mirror surface (e.g., gold on polycrystalline silicon) constitutes a bimorph structure, which is generally, highly non-planar. Using 20 μm thick, ultrathin silicon wafer bonding, they fabricated various mirror sizes using several spring designs. The relatively large thickness compared to polycrystalline silicon deposited layers, that are typically less than a few microns, allowed these structures to remain planar after metal deposition. The single-crystal nature of the material probably also helped maintain mirror flatness when switched.

The devices were fabricated by first etching cavities in 4-inch diameter, standard (500 μm) thickness, silicon substrate wafers, which were then oxidized to a thickness approximately 1 μm, for electrical isolation. Ultrathin silicon wafers, 20 μm thick, were then fusion bonded to these substrate wafers. The ultrathin wafer was subsequently patterned by photolithography. The mirror and spring structures were then formed by DRIE etching, through the ultrathin wafer, to the oxide layer. Finally, chromium/gold was deposited on the mirrors by physical vapor deposition. The mirror dimensions varied from 400 to 700 μm. Figure 6.7 below shows a Scanning Electron Microscopy (SEM) image of one mirror. The mirror area is ~ 700 x 700 μm.

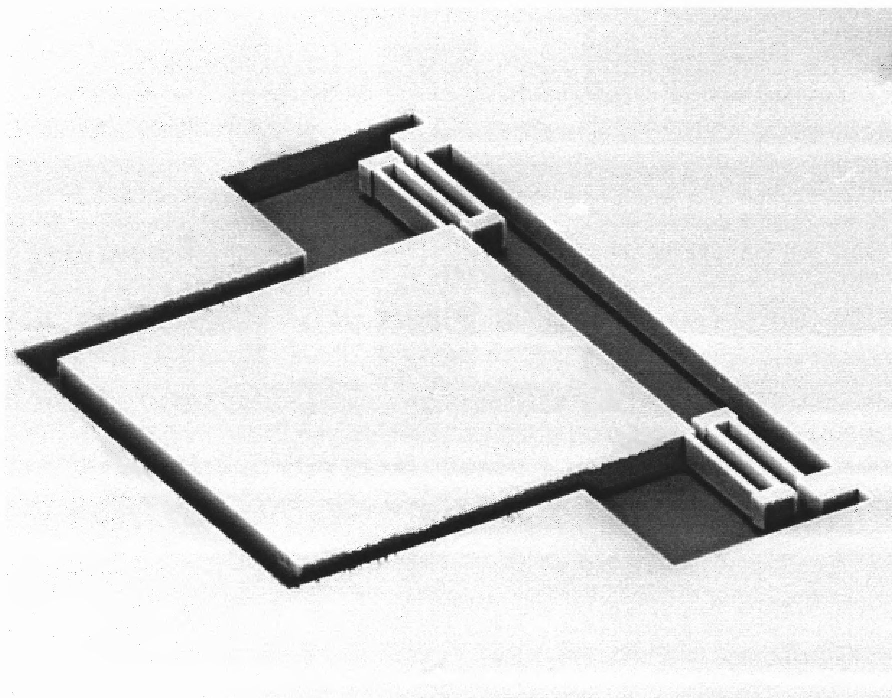


Figure 6.7. SEM image of 700 x 700 mm area mirror and supporting springs.

The DC actuation of the devices was characterized with a Wyko optical profilometer. Without applied voltage, even the largest plates were essentially flat, having a very slight upward deflection of 0.014° to the wafer surface. By applying voltage, the mirror plates deflected downwards into the cavity. The mirror forms one plate of a parallel plate capacitor. Applied voltage creates an attractive force which goes as F = E/d, where F is the force, E is the electric field and d is the separation distance between plates.

Figure 6.8 shows a typical depth profile along the deflection plane, showing a downward deflection of 6 μm at the end of the mirror plate, corresponding to an angle of 0.5° to the wafer surface. Although this angle seems small, over a long optical path length, this small deflection leads to large displacements of the incoming beam. Note the mirror remains extremely flat across its entire surface.

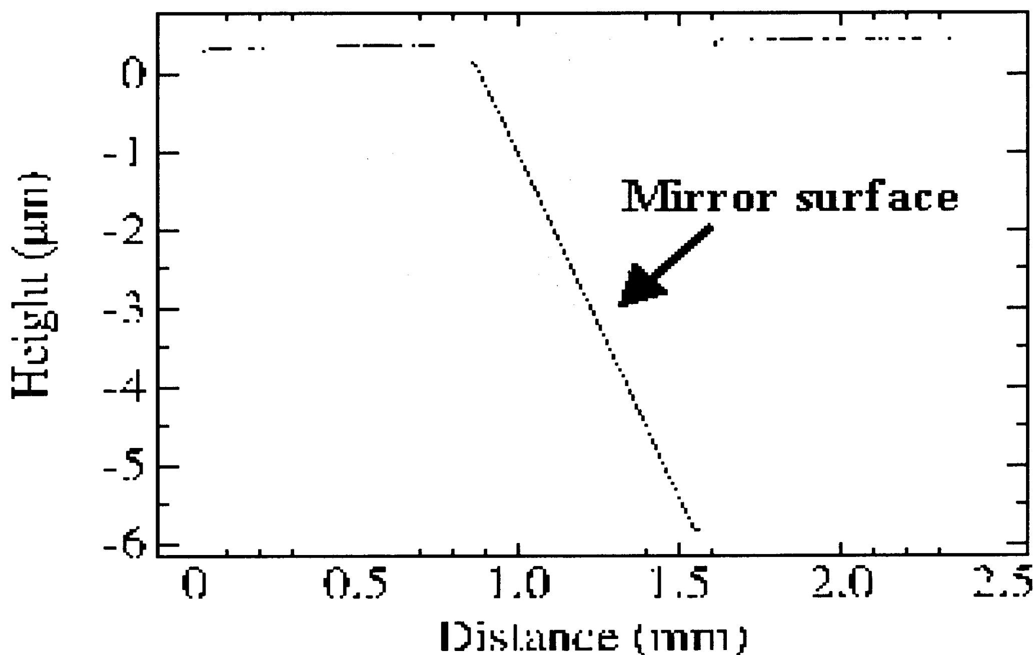


Figure 6.8. Wyko profile of the mirror surface under applied voltage.

Profiling data indicates a smooth increase of deflection angle with increasing voltage up to the snap-down voltage of 46 volts. At snap-down, the mirror quickly moves until it contacts the bottom of the cavity. The mirror remains down until the voltage is decreased below 42.7 volts, corresponding to a deflection angle of 0.24°. The other device designs showed similar behavior, with snap down voltages ranging from 31 to 85 volts. Work continues on these devices to lower the snap-down voltages and improve the spring designs [90].

6.4 Shear Stress Sensor [91]

A shear stress sensor has been devised to measure the horizontal or shear velocity of a liquid or gas flow impacting upon a surface. The velocity of the shear component is related to the deflection of a small mass held on the end of a thin, long cantilever. The deflection of the cantilever is measured by a capacitance change between electrodes

placed symmetrically on either side. The amount of deflection depends upon the area of interaction of the suspended mass, and the velocity of the flow. A diagram of the proposed device is shown in Figure 6.9. This work was done by Jiang Zhe and Dr. Vijay Modi of Columbia University using the resources of the Microelectronics Research Center here at NJIT, enabled by the ultra-thin bonding developed in this thesis. The author's contribution was in the wafer bonding process.

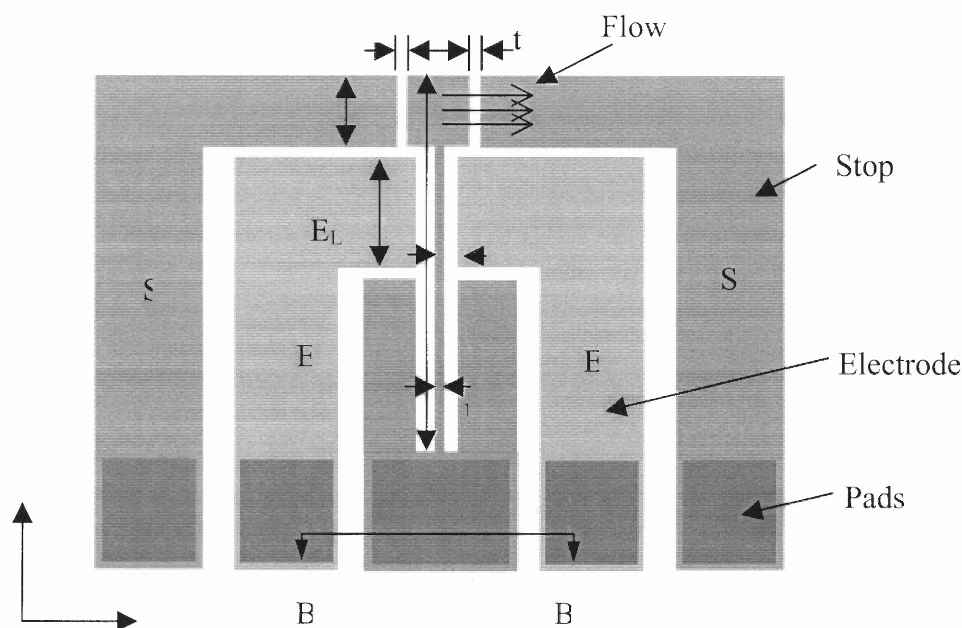


Figure 6.9. Schematic of the shear sensor. The large mass supported by the thin cantilever (center) moves between two stops (S), and two electrodes (E). Readout is either from the stops or the electrodes.

The floating mass on the cantilever end is formed from a 50 μm thick silicon wafer bonded over a cavity that allows motion of the suspended mass. SEM photographs of a fabricated device are shown in Figure 6.10. The second photo is a close-up of the floating element that is about 200 μm x 500 μm. The expected sensitivity of this device is from 5 ~ 50 nN with a horizontal deflection of 0 - 0.5 μm.

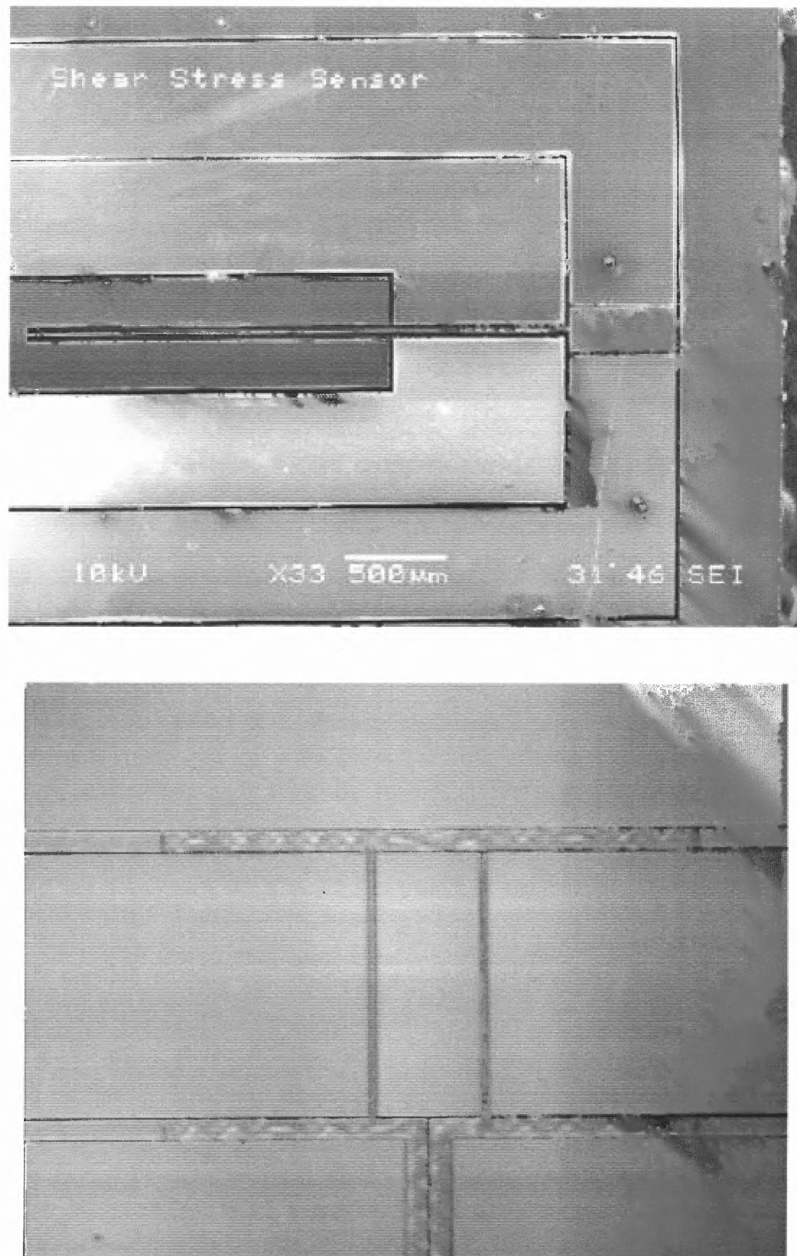


Figure 6.10. SEM photographs of a fabricated shear stress sensor for measuring fluid flow. a) The entire sensor and b) a close-up of the floating element.

This device is designed to examine an important element of flow that is involved in everything from plumbing to aircraft wing design. The shear components of a flow help determine the types of and behavior of turbulence. This design is still under test.

6.5 Rapid-MEMS-Prototyping [92]

Rapid prototyping is way of making devices quickly and cheaply for test purposes without devoting large amounts of time, labor and materials. Several alternatives exist for making large-scale forms. Extruded plastic can be cured in place by computer-controlled, focused radiation and the desired form built by layering many extrusions. Metal or plastic powders can be sintered by CO_2 laser into any desired form. Computer-controlled tooling can cut almost any shape desired out of many different types of materials [93]. All these methods work well for large objects.

For MEMS devices that are on the scale of microns, making a single working device can take enormous effort. Advances in modeling have helped give a rough idea of the operation of a proposed device, but actual performance depends largely upon processing parameters and fabrication methods. It is not always possible to fabricate a modeled device using existing technology. A way to rapidly test a design for general operating and fabrication principles can save enormous time and resources.

One particular requirement that is common to many MEMS devices is the need for a uniform, patterned, insulating spacer layer to separate movable structures from a substrate. This layer must also be able to withstand the chemical, thermal and mechanical stresses of device processing. SU-8 photoresist is a material that can be patterned by UV lithography, applied up to ~1000 μm thick, adheres to silicon wafers well, is electrically insulating, and once cured above 100 °C, chemically resistant and stable to over 200 °C. SU-8 is also compatible with the Bosch Deep Reactive Ion Etching (DRIE) process. Combining patterned SU-8, ultrathin wafer bonding and DRIE allows the rapid fabrication of "proof-of-principle" devices.

The following work was done by Dr. S. K. Sampath, L. St.Clair, X. Wu, D.V. Ivanov, Q. Wang, C. Ghosh and K.R. Farmer. The author of this thesis contributed ultrathin wafer handling instructions and suggestions on improving bond quality, made possible by the work in this thesis.

Electrostatically actuated, mm-sized, ~50 μm thick, spring suspended plates

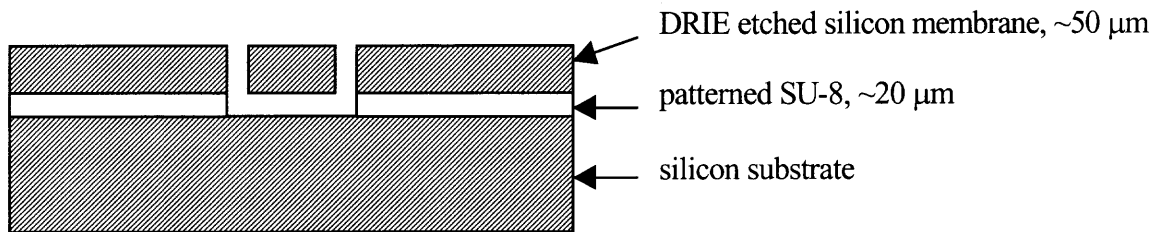


Figure 6.11. Cross-sectional illustration of a rapidly prototyped, electrostatically actuated, mm-sized, 50 μm thick, spring suspended plate bonded via a ~23 μm patterned SU-8 resist layer above a silicon substrate.

suspended over a ~23 μm SU-8 cavity were designed and modeled using MEMCAD 4.8. A range of designs were simulated to process several microns vertical motion with the application of ten's of volts bias. Figure 6.11 shows a schematic of the device.

The basic process steps were: deposition on the silicon substrate wafer ~ 20 μm of SU-8 photoresist which was then patterned by a standard UV aligner, bonding an ultrathin silicon wafer to the SU-8 layer, patterning the ultrathin silicon layer using standard photoresist, and DRIE etch to form the suspended structure.

Ultrathin silicon wafers were used in this design to avoid having to thin the active device layer after bonding. The bond strength of the SU-8/ultrathin silicon wafer interface was sufficient to withstand the further processing steps and, once the device was fabricated, diamond saw dicing.

Figure 6.12 shows the high quality of the SU-8/ultrathin silicon bond. Figure 6.13 is a VEECO® interferometric profile of the fabricated device showing excellent planarity between the suspended layer, the support hinges and the remaining silicon surface. A difference in color indicates a change in height, which is only apparent in the openings around the structure.

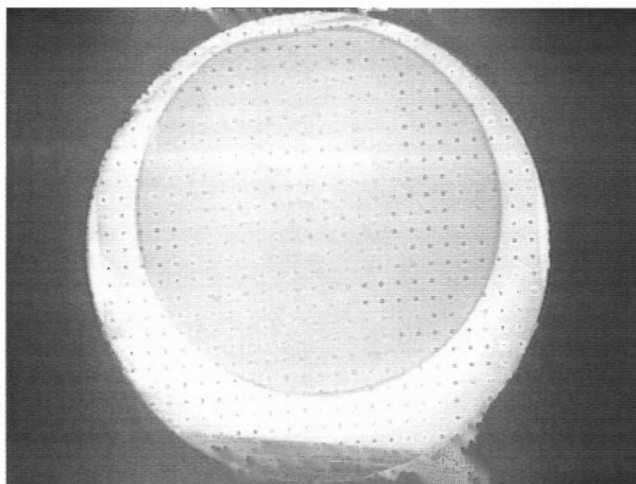


Figure 6.12. IR image of a 75 mm diameter, ~50 μm thick silicon wafer bonded to a ~23 μm thick patterned SU-8 layer on a standard thickness, 100 mm diameter silicon substrate.

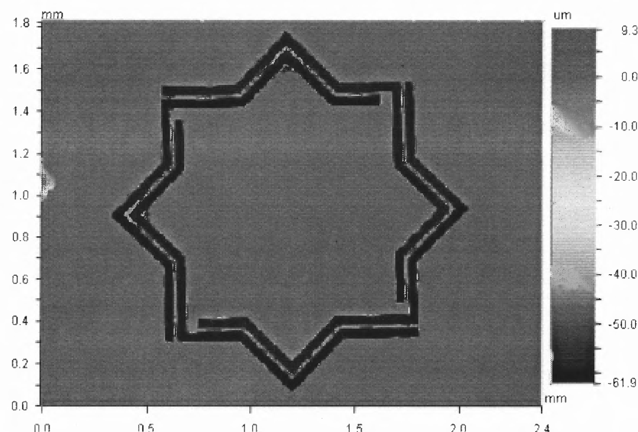


Figure 6.13. VEECO optical profilometer image of a completed, functioning chip. The plate shape is a square on top of a 45° rotated square. The square side length is 1 mm. The spring width is 10 μm.

The Rapid-MEMS-Prototyping process has demonstrated quick and easy fabrication of suspended structures with controlled thickness and gap spacing and a high degree of planarity. Although SU-8 photoresist is more difficult to use than other standard UV lithography resists, the ability to quickly form patterns up to 1000 microns in height makes it desirable for MEMS device production.

The devices performed as expected from simulations using MEMCAD 4.8. Figure 6.14 shows the vertical displacement of the suspended structure with applied voltage.

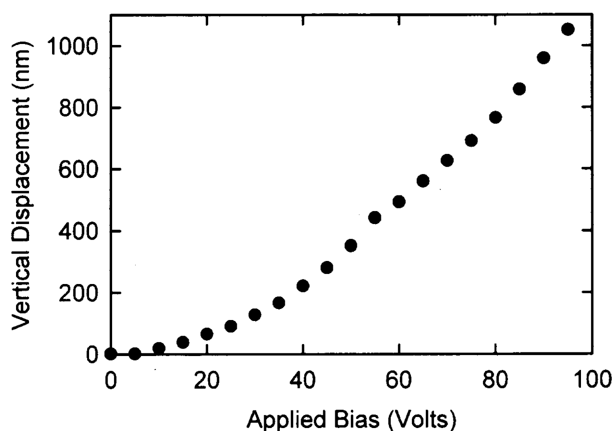


Figure 6.14. Measured vertical displacement of the movable plate as a function of applied bias.

The researchers believe that this process method was so successful, both in its simplicity and versatility, that it may be sufficient for device production in some situations where a thermal coefficient of expansion mismatch between the spacer and electrodes may not be an issue. It is also suspected that this approach may not be limited to silicon-based systems. SU-8 may bond well to many materials other than ultrathin silicon wafers. These possibilities are sure to be examined in future work.

6.6 Recap

The three devices described in the preceding sections are a representation of the potential of ultrathin silicon wafer bonding to fabricate MEMS devices more cheaply, quickly and reliably than other technologies. They were all enabled by the handling and bonding work of this thesis. The pressure sensor head highlighted the ease of anodic bonding, the superior uniformity and response of ultrathin silicon compared to fabricated thin membranes, and the reduction in processing complexity, cost and device variation. The shear sensor and optical modulator, while still in early development, show how ultrathin silicon wafer bonding can produce novel designs not readily fabricated by other methods. The Rapid-MEMS-Prototyping would not be so quick or easy if the bonded wafer needed to be thinned. Using ultrathin wafers, this production method has reduced the time, complexity and cost of fabricating suspended structures, common among MEMS devices, and "proof-of-principle" designs.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Ultrathin silicon wafer bonding can improve the production of MEMS devices by simplifying designs, reducing costs by eliminating process steps, decreasing device variations and making possible novel devices. The handling and cleanroom processing of this material has been developed to the proto-type production level with only minor modifications to standard equipment and procedures. Wafer loss is now more a question of operator error. The initial contamination and surface quality issues have been resolved. A new method for reducing wafer surface roughness has been developed and may help extend the use of bonding ultrathin wafers to multiple layer devices. Bonding limitations for all thickness wafers across the entire possible frequency range for 4" wafers has been developed. It correctly predicts the ability of ultrathin wafers to bond to increasing roughness with decreasing thickness and indicates when surface roughness may inhibit successful bonding.

Several devices have been produced by the author and others in the MRC center using ultrathin silicon wafer bonding. The pressure sensor and optical modulator devices improve upon existing designs and reduce their fabrication steps and complexity. The shear stress sensor enables investigation into physical processes not readily accessible to existing technology, and Rapid-MEMS-Prototyping forms a basis for an entirely new fabrication methodology. Ultrathin silicon wafer bonding now stands ready to impact the design, fabrication and conventional limitations of MEMS manufacturing.

7.2 Future Work

There exists a need for high strength bonding without high temperature processing. Investigations in this area have concentrated on UHV conditions for achieving ultraclean surfaces that do not require dissolution of the interface contaminating species found in room temperature, atmospheric pressure, bonding of silicon. The bond strength of silicon without annealing and under varying anneal conditions should be investigated. Due to the large conformity to gross surface features, these wafers may be used for packaging of electronic devices, but only if the unannealed bond strength is high. Other work could include:

- Fully automated processing of ultrathin silicon wafers would be an interesting challenge for any mechanical engineering student.
- Investigation of the applicability of the wafer bond limit model to larger surface features should allow ultrathin wafers to be used in multiple layer device fabrication without the current need for CMP planarization.
- Additional studies on the oxidation smoothing should be performed to determine the roughness scales such processes as hydrogen annealing and multiple oxidation and strips most impact, and the optimal process parameters.
- Of course, there is the unlimited area of MEMS device development that can be explored through ultrathin, single-crystal, silicon wafer bonding.

APPENDIX A

ULTRATHIN SILICON WAFER PROCESSING TRAVELERS

This Appendix contains the documentation travelers that accompany any project that uses the Microelectronics Research Center cleanroom facilities at NJIT. They are broken down into sections that denote the generic processes, such as cleaning, native oxide removal, oxidation growth, manual bonding, anneal, etc. These are taken from full process flow sheets and specify the parameters used and the desired results; for example the temperature and time used to achieve an oxide thickness of ~ 1 micron on silicon by wet oxidation. Due to variations in processing equipment and facilities, in using these travelers to duplicate the work in this thesis, one should consult with cleanroom personnel on their facility's standards and equipment to adjust such parameters as time and temperature to achieve the desired result.

Following the generic processes is the documentation for specific materials, equipment or projects, such as oxidation and strip for oxidation smoothing (Chapter 4), the use of SU-8 photoresist for Rapid-MEMS-Prototyping (Chapter 6), automated bonding, etc. Again, cleanroom personnel should be consulted for possible variations in processing parameters. General notes are given, where needed, to address specific issues such as ultrathin wafer handling, glass cleaning for anodic bonding, etc.

A.1 Wafer Cleaning

The following process sheet details the now standard procedure for cleaning wafers not packaged in cleanroom facilities or those materials that otherwise have excessive contamination. Prior procedure had two separate P-clean baths.

M-Pyrol Cleaning

Process Description	Date	Wafer #	Operator	Comments
1. Primary bath 95 °C, 10 min				
2. Secondary bath 95 °C, 10 min				
3. Rinse cold DI water 10 min				
4. Oven dry 15 min @ 100 °C				
5. Inspect				

P-Clean

Process Description	Date	Wafer #	Operator	Comments
1. P-clean (H_2SO_4/H_2O_2) 110°C, 10 min.				
2. Hot DI water rinse 10 min.				
3. Cold DI water rinse 5 min.				
4. Oven Dry 15 min. @ 100 °C				
5. Inspect				

General notes:

1. For ultrathin wafers, carrier retainers must be used. Carriers must be slowly submerged and removed from baths.

2. Chapter 3 describes the prior use of filtered nitrogen gas for blow-drying ultrathin wafers. Convection oven drying was implemented due to damage caused by the force of the compressed gas. If wafers are blown off prior to bonding, filters with maximum particle size of 0.20 μm must be used. Larger particles are detectable by IR imaging.

3. Standard thickness wafers (300 – 500 μm) are spun-dry.

A.2 Native Oxide Removal

In many cases, the native oxide on silicon wafers, which forms in air spontaneously, is unwanted either because no oxide is desired or a well-characterized oxide is to be formed by wet or dry oxidation. The oxidation process requires the removal of the native oxide and is included as the first step in the traveler documents (see Section B.3).

OXIDE REMOVAL

Process Description	Date	Wafer #	Operator	Comments
1. 100:1 H_2O:HF 1 minute (until hydrophobic)				
2. Rinse 10 minutes				
3. Oven dry 15 min @ 100 °C				

General notes:

1. In our cleanroom facilities, the 100:1 HF bath is continually cycled and this agitation may cause damage to ultrathin wafers. Carriers should be held just below the liquid surface to prevent wafers from being forced out of the carrier.

2. Wafer retainers must be used with ultrathin silicon wafers.

3. The deionized (DI) water rinse in our cleanroom is of the overflow type. This should be turned on 1 minute prior to rinse to remove any possible particles from the water surface (see Sections 2.3.2.2 and 3.4).

4. Insertion of hydrophobic, ultrathin silicon wafers into the rinse bath should be done slowly and carefully as the repulsive force between the wafer surface and the water can cause ultrathin wafers to twist, crack or escape from the carrier.

5. Standard thickness wafers are spin-dried.

A.3 Steam Oxidation

Dry oxidation, which uses only oxygen gas as the oxidizing species, was not performed in this thesis. The furnace tubes, quartz "boats" and general operation is the same as for wet or steam oxidation so the following traveler will apply. No ultrathin wafers were lost or damaged in this process during any of the work of the thesis. There were initial difficulties with non-uniformity near the quartz boat slots and from motion of the ultrathin wafers from the gas flow that have been addressed (see Section 5.1.4).

STEAM OXIDATION

Process Description	Date	Wafer #	Operator	Comments
1. Furnace pre-clean 100:1 H_2O:HF >1 minute (until hydrophobic)				
2. Rinse 10 minutes				
3. Oven dry 15 min @ 100 °C				
4. Steam oxidation O_2 bubbler: 530 sccm O_2 main: 7.5 l/min Temp: 1050^0C Time: ~05:00:00				
5. Measure: target= 10 kÅ Mean: ________Å Std. Dev.: ______Å # pts./wafer: ______				

General notes:

1. See notes for native oxide removal.

2. The flow rates are for the water vapor (O_2 bubbler) and oxygen gas (O_2 main). The temperature and time (~ 5 hours) were for a target of ~ 1 μm oxide thickness.

3. Step 5 above was performed by on a Leitz® thin film inspection station.

A.4 Surface Activation

Surface activation of ultrathin silicon wafers was attempted using M-Pyrol, P-Clean (see B.1 Wafer Cleaning), and RCA2 solution. The P-Clean surface activation method resulted in the least number of particles trapped in the bonded interface and is now the standard activation method for ultrathin wafers in our cleanroom (see Section 3.4). The RCA2 solution had the largest particle contamination, but this may have been because this process had just been introduced into our cleanroom facilities. Only the RCA2 process is documented here. The use of P-Clean as an activation is the same as for the clean (B.1).

RCA2 SURFACE ACTIVATION

Process Description	Date	Wafer #	Operator	Comments
1. RCA-2 95 °C 10 min.				
2. Hot DI water rinse 60-70°C, 5 min				
3. Cold DI water rinse 5 min				
4. Oven dry 15 min @ 100 °C				
5. Inspect				

General notes:

1. Wafer retainers must be used with ultrathin wafers.
2. This process no longer used for surface activation.

A.5 Manual Bond

The following traveler is a general description of wafer bonding done by hand by contacting wafers at their flats and removing them from the carrier. The slot edges of the carrier helped maintain wafer separation until about midpoint, where the lower half of the

wafers were no longer in contact. While still performed for odd shaped or mismatched materials, the use of the EV501S automated bonding station is preferred. More details on the difficulties of this bonding method can be found in Section 3.1.1. Mismatched materials are now generally bonded with matched handle wafers (see Sections 5.2.3.2 and 5.2.3.3).

Manual Bond

Process Description	Date	Wafer #	Operator	Comments
1. Manual bond Align flats of wafers to be bonded in adjacent slots of cassette. Lift both wafers from cassette. Initiate contact at top of wafers. Pull slowly from cassette to bond wafers.				

General notes:

1. Thick wafers (> 100 μm silicon) will snap together after wafers are pulled ~ ½ out of the carrier because the slot edges will no longer separate them.

2. The risk of particle contamination is high due to the use of operator's.

3. Carrier (cassette) must be thoroughly dried if used in wet baths prior to bond.

A.6 Anneal

The anneal of bonded ultrathin silicon wafers must proceed under near-isothermal conditions to prevent the thin wafer from heating much more rapidly than the thicker substrate. The thermal coefficients of silicon are the same for both thick and ultrathin wafers, but a temperature gradient would mean that one wafer would either expand or

contract faster than the other and put stress on the interface. Note the temperature ramp up and down times. The anneal furnace is maintained at 300 °C and insertion and removal of bonded wafers should be as slow as possible.

Anneal

Process Description	Date	Wafer #	Operator	Comments
1. Anneal 1100°C Tube #4 Time: 60 min. O_2 2.5 l/min. N_2 7.5 l/min.				
2. Push-in time: ~30 min.				
3. Ramp up from 300 to 1100 °C: ~160 min.				
4. Temperature Stabilization: ~10 min.				
5. Anneal: 60 min.				
6. Ramp down from 1100 to 300 °C: ~160 min.				
7. Push-out time: ~30 min.				

General notes:

1. Push-in/out times are approximate due to the variable start position of the quartz boat.

2. Long temperature ramp up and down times are critical to avoid thermal stress at bonded interfaces when using ultrathin silicon wafers.

3. <u>Quart boat slots must be thick enough to accommodate bonded pairs</u>.

4. Anneal temperature dependent upon bonding conditions and desired bond strength. See Section 2.4.

A.7 Photoresist-bonded Handle Wafer

In Section 5.2.3.3 a general description was given on the use of photoresist bonding to substrate wafers provide mechanical support and prevent uncontrolled ultrathin wafer contact during automated bonding. This procedure is necessary when bonding under vacuum with ultrathin wafers, both because ultrathin wafers need rigid support for controlled bonding and because water-bonded handle wafers would separate. Water-bonded wafers also cannot be wet chemical processed. The substrate and ultrathin wafers should be cleaned before this procedure.

PHOTOLITHOGRAPHY - Frontside

	Date	Wafers	Operator	Comments
1. Apply Photoresist HEADWAY Apply Prime @ 800RPM Dry 30sec @ 2000RPM APPLY Shipley 3813 Spin @ 2000RPM				
2. Bake 110 °C Hot plate 60sec.				
3. Manual bond ultrathin wafer to photoresist				
4. Bake 115 °C Hot plate 60 sec.				
5. Inspect				

General notes:

1. Handle wafer can be removed in M-Pyrol or with acetone.
2. Manual bonding done by carefully laying ultrathin wafer onto flat substrate.
3. For photolithography, step three is mask alignment and exposure followed by developer and then 115 °C bake.
4. If bonding unsuccessful, bake temperature can be reduced or not done.

A.8 Automated Bonding

The following two sections are the recipes used for anodic and direct bonding of ultrathin silicon using the EV501S bonder. Details on the loading and general use of this system are given in Chapter 5. These process steps can be done manually or entered into a file that can be run automatically. For direct bonding of ultrathin silicon, water-bonded handle wafers were used. No handle wafer was used for anodic bonding due to lack of spontaneous adherence.

A.8.1 Anodic Bonding

This process flow was used for the fabrication of the pressure sensor head described in Section 6.2. The micromachined glass wafer was cleaned with acetone and methanol before being loaded first into the bond chamber. The 20 μm thick ultrathin wafer was cleaned in the standard manner, (see section B.1) laid on top of the glass wafer, and their flats aligned. A voltage distributing, graphite wafer was placed on the stack and the bond cover closed and sealed. The piston height was adjusted to account for the glass thickness, ~ 500 μm, the ultrathin thickness, ~ 20 μm, and the graphite wafer, ~ 2 mm. The following instructions were then performed by the bonder control system.

Automated Anodic Bonding

	Comments
1. Wafer bow	Center pin pushes wafers together.
2. Heat chuck to 350 °C	Increases mobility of sodium ions.
3. Temperature stabilize: 10 min.	
4. Pressure plate down at 30 N force	Ensures contact between graphite wafer and electrode.
5. Apply 1200 Volts for 1 min.	
6. Cool down for 45 min.	Longer cool down minimizes thermal stress.
7. Release pressure plate	Wafer pair can now be unloaded.

A.8.2 Direct Bonding

Ultrathin silicon wafers were cleaned, sometimes oxidized, stripped and reoxidized (see Chapter 4 on oxidation smoothing), and after cleaning, water bonded to the rough side of a single-side polished silicon wafer. Substrate wafers were cleaned and usually oxidized. The separation flags were 500 μm thick and alignment flat-to-flat on the manual bond chuck. Water-bonded ultrathin wafers were loaded first, the separation flags moved into place, and the cover closed and sealed. Heating and vacuum were not usually applied. The piston height was adjusted for the substrate thickness, ~ 500 μm, the ultrathin wafer thickness, 20 – 100 mm, and the separation flag thickness, ~ 500 μm. The following steps can be performed manually or entered into a file to be run automatically.

Automated Direct Bonding

	Comments
1. Wafer bow for 1 min.	Allows contact wave to travel to wafers' edge. Vacuum can be applied here by closing vent and starting pump.
2. Remove flags	
3. Wait 1 min.	Spontaneous bonding should be complete.
4. Pressure plate down at 1200 N force for 2 min.	Not strictly necessary but may help remove any non-flatness of the water-bond.
5. Release pressure plate	Vacuum can also be applied here to release handle wafer.
6. Heat to 110 °C for 5 min.	Releases water-bonded handle wafer.
7. Cool down 10 min.	Wafer pair can be removed.

If full bond strength is not required, a low temperature anneal (< 550 °C, bonder limit) can be performed in step 6. Indications are that good results can be obtained with low-temperature, anneals performed in vacuum over a long time (> 12 hours) [2]. If vacuum is required prior to bond initiation, the handle wafer must be photoresist-bonded to prevent premature separation.

A.9 Rapid-MEMS-Prototyping

The general description of this new production process is given in Section 6.5. It consists of applying SU-8 photoresist in a thick layer upon a silicon substrate wafers, patterning the resist to form cavities, bonding an ultrathin silicon wafer to the patterned SU-8, patterning the ultrathin silicon and DRIE etching through to the SU-8. The next two sections are the details of the overall process and the specific details of the application and preparation of the SU-8 photoresist layer.

A.9.1 Rapid Prototyping Process

Step
1. P-clean substrate and ultrathin wafers
2. Oxidize substrate and ultrathin wafers, ~250 nm, pyrogenic steam, 1050 °C
3. Spin SU-8 onto substrate, ~23 μm; expose and develop to form cavities
4. Bond ultrathin wafer to patterned SU-8 • Attach ultrathin wafer to a handle wafer • Bond in EV-501 system: 1×10^{-3} mbar, 1500 N force, 100 °C, 10 min
5. Photolithography on ultrathin wafer surface for DRIE etching, Shipley 3813 photoresist
6. Dry etch oxide from exposed areas of ultrathin wafer surface
7. DRIE ultrathin wafer, Bosch process; stops on oxide at bond surface of ultrathin wafer
8. Dry etch oxide from back surface of substrate wafer to enable electrical contact to substrate as a ground plane
9. Dry etch oxide from DRIE cavities to release suspended device structures
10. Metallize top surface by evaporation (Cr/Au); does not short active layer to substrate
11. Protect active devices with photoresist, dice wafer, clean individual chips and test.

The Reactive Ion Etching (RIE) processes (dry etch and DRIE) are device specific and must be obtained from either the manufacturer or lab personnel. Metallization parameters likewise depend upon the equipment used, such as e-beam evaporator, sputterer, etc. Dicing is usually done with a diamond saw but is not performed at NJIT.

A.9.2 SU-8 Patterning Process

1. Spin coat (specially programmed ramps to and from final spin speed): • 2000 rpm for a 32 μm spacer layer thickness • 2500 rpm for a 25 μm spacer layer thickness • 3000 rpm for a 23 μm spacer layer thickness • 3500 rpm for a 21 μm spacer layer thickness
2. Soft pre-exposure bake at 60 °C for 3 min, 2 min ramp to 95 °C, 5 min bake at 95 °C, >5 min ramp to room temperature
3. Expose, ~260 mJ/cm^2 (30 sec at ~8.5 mW/cm^2)
4. >5 min ramp to 95 °C, 5 min post-exposure bake at 95 °C, >5 min ramp to room temperature
5. 1st develop for 1 min in fresh PGMEA poured onto wafer surface, spin off developer, 2nd develop for 4 min in fresh PGMEA poured onto wafer surface, spin dry

SU-8 is a relatively new photoresist and processing parameters can vary greatly depending upon the application. The suppliers can provide more details for variations on the above process or offer suggestions on solving known problems, such as the difficulty in removing cured SU-8. Various MEMS websites have additional information on working with this material. SU-8 is a product of MicroChem Corporation, Newton, MA.

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