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Three-dimensional magnetic field sensor in IBM 0.18μm CMOS technology

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ABSTRACT

THREE-DIMENSIONAL MAGNETIC FIELD SENSOR IN IBM 0.18μm CMOS TECHNOLOGY

by
Gang Wang

This work presents a compact three-dimensional Magnetic Field Sensor (MFS) designed in standard Complementary Metal–Oxide–Semiconductor (CMOS) technology. A circular Vertical Hall Device (VHD) for horizontal magnetic field detection and a split-drain Horizontal Hall Device (HHD) for the vertical magnetic field detection are integrated to implement the three-dimensional MFS. This merged design has the advantage of smaller area and lower power consumption. The sensitivity of the vertical hall device (ring-shaped magneto-resistor) and the horizontal hall device (Split-Drain Magnetic Field-Effect Transistor (SD-MAGFET)) is estimated as 0.11V/T and 2.88V/T respectively. The vertical direction of the magnetic field detection demonstrates a higher sensitivity. A high gain cascode differential amplifier is integrated with the sensor to further amplify the magnetic signal.

THREE-DIMENSIONAL MAGNETIC FIELD SENSOR IN IBM 0.18μm CMOS TECHNOLOGY

by
Gang Wang

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APPROVAL PAGE

THREE-DIMENSIONAL MAGNETIC FIELD SENSOR IN IBM 0.18µm CMOS TECHNOLOGY

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This thesis is dedicated to
My Family

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A_V	Gain of the amplifier
A_β	Proportionality constant
B	External magnetic field
C_{OX}	Capacitance per unit area of the gate oxide
E_e	External electrical field
E_H	Hall electric field
G	Geometrical correction factor
g_m	Trans-conductance
q	Electrical charge of a carrier
I	Current
I_p	Bias current
J	Current density
L	Length of the gate
N	Number of values in the sample
n	Density of free electrons
R_H	Hall coefficient
r_H	Hall scattering factor
r_o	Channel modulation resistance
S	Sensitivity of magnetic field sensors
SNR	Signal to noise ratio
t	Thickness of the strip

LIST OF SYMBOLS
(**Continued**)

$V_{H\infty}$	Hall voltage of hypothetical point-contacts
V_n	Velocity of charge carriers
V_T	Threshold voltage
W	Width of the gate
w	Width of the strip
$\bar{x}$	Mean value of the sample
x_i	Random value obtained from the sample
β	Conductance of the transistor
μ_n	Drift mobility of electrons
μ_{Hn}	Hall mobility of electrons
σ	Standard deviation

CHAPTER 1

DESIGN CONSIDERATIONS IN THIS THESIS

Complementary Metal–Oxide–Semiconductor (CMOS) technology has been widely used for three-dimensional Magnetic Field Sensors (MFSs) due to low power consumption (compared with Bipolar Junction Transistors (BJTs)), very high density without any requirements of cooling systems and strong noise immunity. The sensor can be used in tough environments with low power supply [1]. MFSs based on the Hall Effect can be utilized in various ways. For example, they can be used in cars as position sensors or used in hard disc drives for personal computers. Advanced fabrication technology provides the advantage of low power consumption such that the MFS can be set up in low power devices such as cell phones and network sensor systems.

A three-dimensional MFS is designed in IBM 0.18μm technology to achieve high performance in this work. The literature of MFSs in CMOS planar technology illustrates that the structure of three-dimensional MFSs usually focuses on a square pattern, and sensors are always designed to utilize the properties of the Hall Effect in both horizontal and vertical directions. In successful designs, the tradeoff is the detection of sensitivity in the vertical direction with minimum interference from the field components in horizontal directions. Typically, the sensitivity in the vertical direction is much lower than it is in the horizontal direction. Thus, the achievements of higher performance in the vertical direction and a competitive performance in the horizontal direction need to be addressed.

For the horizontal magnetic field detection, a circular Vertical Hall Device (VHD) structure is utilized to design the sensor with low noise and high precision [2]. For

the vertical magnetic field detection, a Split-Drain Magneto Field Effect Transistor (SD-MAGFET) is utilized. The design of the CMOS three-dimensional magnetic field sensor in this work has two advantages:

1. To detect the vertical component of the magnetic field, four SD-MAGFETs are designed in the center of the circular VHD. To improve the precision of the sensor, a compact layout is designed including both different sensor components. The placements of detecting horizontal components and the vertical component are carefully separated to reduce interference. To detect the horizontal components of the magnetic field, a circular VHD is used to detect the intensity. This structure is much more effective due to the increased number of power contacts and hall probe contacts in specific phases.

2. By designing in a more advanced technology, the power consumption of the sensor is decreased, and the device area is reduced, which aids in achieving a higher precision and selectivity for three-dimensional magnetic field detection.

Chapter 2 introduces the basic theory and concept about hall devices. Popovic first introduced the circular design of MFSs to detect both vertical and horizontal components of the magnetic field [2]. A circular shape is used to reduce the offset voltage and to improve the performance of two-dimensional MFSs.

Chapter 2 also provides a general review about the operational principle of the Hall Effect in semiconductors from a one-dimension to a three-dimension. The theory about how to define the properties of a magnetic sensor is described. Then, basic operational principles of the SD-MAGFET and the circular VHD are introduced.

Chapter 3 presents an implementation of the three-dimensional MFS with enhanced performance. A specific structure of the SD-MAGFET and the circular VHD is

combined together. Extensive simulation results for each structure are achieved in Hspice. The entire layout of the three-dimensional MFS is presented in this chapter.

Chapter 4 displays equivalent circuits of the entire sensor integrated along with an amplifier, which amplifies considerable signal of the magnetic field. A structure of the high gain amplifier is designed as a cascode structure to enhance the sensitivity. The results of each part with amplifiers are plotted from the simulation.

CHAPTER 2

BACKGROUND AND BASIC PROPERTIES OF MAGNETIC FIELD SENSORS IN SEVERAL DESIGNS

Integrated MFSs are designed and fabricated for various applications in standard CMOS technology. For low power applications, the MFS needs to be designed in scaled CMOS technology. To understand the original devices of MFSs in this chapter, the basic operational principle of MFSs and the literature survey are introduced. Several previous designs of MFSs are also described.

2.1 Hall Effect Theories

A basic mechanism of the Hall Effect is shown in Figure 2.1 where current flows in the X-direction and the Lorentz force is exerted in the Y-direction when the external magnetic field is applied. When a long current-carrying strip is exposed to a DC magnetic field, charged carriers are impacted by the Lorentz force as denoted in Equation 2.1. [5]

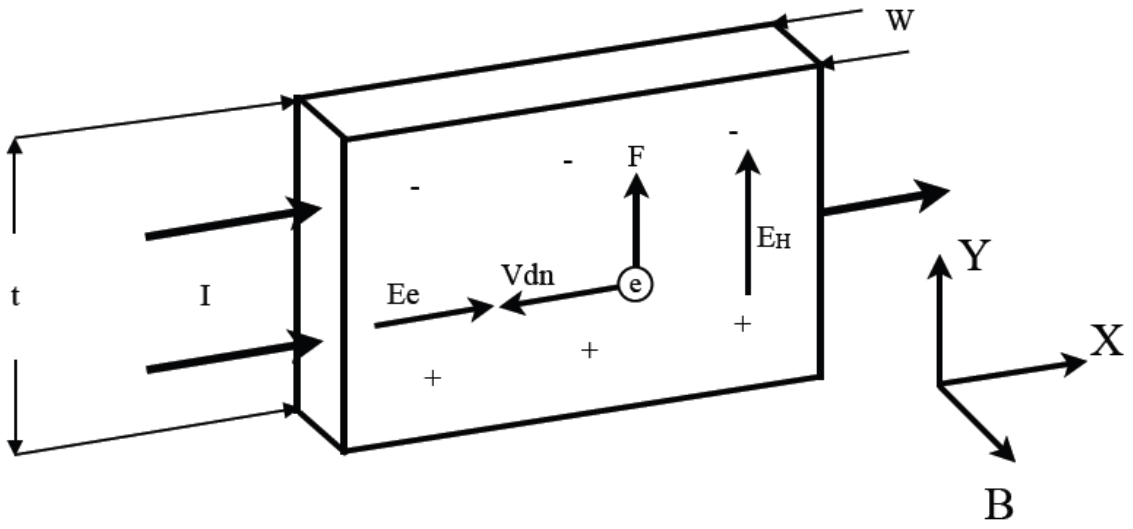

Figure 2.1 A Hall Plate which suggests the Hall Effect.

$$\overline{F} = q \cdot \overline{E} + q \cdot (\overline{v} \times \overline{B}) \tag{2.1}$$

Here q denotes the electrical charge of a carrier. E is the external electrical field, v is the velocity of a charge carrier, and B is the magnetic flux density. The direction of B is perpendicular to the strip plane.

After assuming the strip is an n-type semiconductor and an external electrical field E_e is applied along the long strip, the velocity of charge carriers (V_n), n-type, could be calculated as follows:

$$\overline{V}_{dn} = \mu_n \cdot \overline{E}_e \tag{2.2}$$

where μ_n is the drift mobility of electrons. The associated current density is given by

$$\overline{J}_n = q \cdot n \cdot \mu_n \cdot \overline{E}_e \tag{2.3}$$

where n is the density of free electrons.

The Lorentz force can be given by

$$\overline{F}_{mn} = q \cdot \mu_n [\overline{E}_e \times \overline{B}] \tag{2.4}$$

By applying the external magnetic field (B) on the strip, an electric field (E_H) can be generated between top and bottom sides of the strip. It can be related with the Lorentz force:

$$\overline{F}_{en} = -q \times \overline{E}_H \tag{2.5}$$

where E_H denotes the electric field generated by the Lorentz force, which is called the Hall electric field. E_H could be expressed as

$$\overline{E}_H = -\mu_{Hn}[\overline{E}_e \times \overline{B}] \tag{2.6}$$

μ_{Hn} denotes the Hall mobility of electrons, which is given by

$$\mu_{Hn} = r_H \cdot \mu_n \tag{2.7}$$

where r_H is the Hall scattering factor. In the most circumstances, r_H modifies the mobility of the carriers by less than 20%.

Another useful expression for the Hall electrical field is obtained when the external Hall electrical field in Equation 2.6 is expressed by the current density J in Equation 2.3.

$$\overline{E}_H = -R_H[\overline{J} \times \overline{B}] \tag{2.8}$$

Here R_H denotes the Hall coefficient and in this case R_H is given by

$$R_H = \frac{1}{q \cdot n} \tag{2.9}$$

By neglecting thermal agitation Equation 2.9 can be rewritten as

$$R_H = \frac{r_H}{q \cdot n} \tag{2.10}$$

This is another function for Hall magnetic sensors, which is utilized in relatively low-doped semiconductor material.

In addition, the most tangible property associated with the Hall Effect is the voltage (V_H) between edges of the strip called Hall voltage, which is generated by the movement of charge carriers due to the magnetic field (2.11).

$$\overline{V}_H = \int_{S_1}^{S_2} \overline{E}_H ds \tag{2.11}$$

From Figure 2.1, it is also obtained that

$$\overline{V}_H = \mu_n \cdot w \cdot [\overline{E}_e \times \overline{B}] \tag{2.12}$$

where *w* denotes the width of the strip. Assume that *B*, the magnetic flux density vector, is perpendicular to the strip plane. Otherwise, *B* should be replaced by the perpendicular component.

By combining two equations, (2.3) and (2.11), a new equation for current density can be obtained as the following:

$$\bar{J} = \frac{\bar{I}}{t \cdot w} \tag{2.13}$$

Here, *I* denotes the current in the strip and *t* is the thickness of the strip. Thus, the Hall voltage is also given by

$$\overline{V}_H = \frac{R_H}{t} \cdot [\bar{I} \times \overline{B}] \tag{2.14}$$

2.2 Sensitivity of MFSs

Sensitivity, the important property of MFS, reflects the basic property about how well the sensor responds to the external magnetic field. It is influenced by the geometry of the Hall plane, including the geometry of contacts. The geometrical correction factor, *G*, describes the decrease of the Hall voltage in the Hall device depending on the placement of Hall probe contacts.

$$G = \frac{V_H}{V_{H\infty}} \tag{2.15}$$

where V_H denotes the Hall voltage across the finite electric field, and $V_{H\infty}$ denotes Hall voltage of hypothetical point-contacts.

Theoretically, $0<G<1$.

Then, the equation of the Hall voltage can be given by

$$\overline{V}_H = G \cdot \frac{R_H}{t} \cdot [\overline{I} \times \overline{B}] \tag{2.16}$$

The sensitivity of Hall devices is given as

$$S = \frac{V_H}{B} \tag{2.17}$$

By combining two equations, (2.16) and (2.17), *S* can be denoted as

$$S = \frac{G \cdot r_H}{n \cdot q \cdot t} \cdot I_p = S_I \times I_p \tag{2.18}$$

where

$$S_{Imax} = \frac{G \cdot r_H}{n \cdot q \cdot t} \tag{2.19}$$

In Equation 2.18, I_p denotes the bias current. Thus, S_I was fixed in general situations and its value can only be varied in fabrication processes.

2.3 One-Dimensional Magnetic Field Sensor

A one-dimensional integrated semiconductor MFS is called a Hall Plate. In this section, the operational principle of the Hall Plate will be introduced. Carriers flow through the

semiconductor device will be discussed. The next generation of the Hall Plate in standard CMOS technology is designed by using a split-drain MOSFET called the SD-MAGFET. Different variations of SD-MAGFETs and operational theories of MFSs are also described. The implementations of one-dimensional MFS in both vertical and horizontal directions are outlined.

2.3.1 Hall Plate

Figure 2.2 shows the basic principle of a conventional Hall Plate. Current flows from the left side to the right side through the conducting plate in the Y-direction. By applying an orthogonal magnetic field (*B*) on the plate, carriers are deflected to side contacts in the X-direction depending on the direction of the magnetic field. Then, a bias voltage due to the magnetic field can be detected between contacts, *C1* and *C2*, by Hall Probes. For example, it can be assumed that if the external magnetic field is applied towards the plate, its perpendicular component will only be effective. As a consequent, current will be deflected towards Hall probe contacts on the plate. Meanwhile, an electric field between two contacts is constructed and the Hall voltage between two contacts varies as a function of the intensity of the magnetic field.

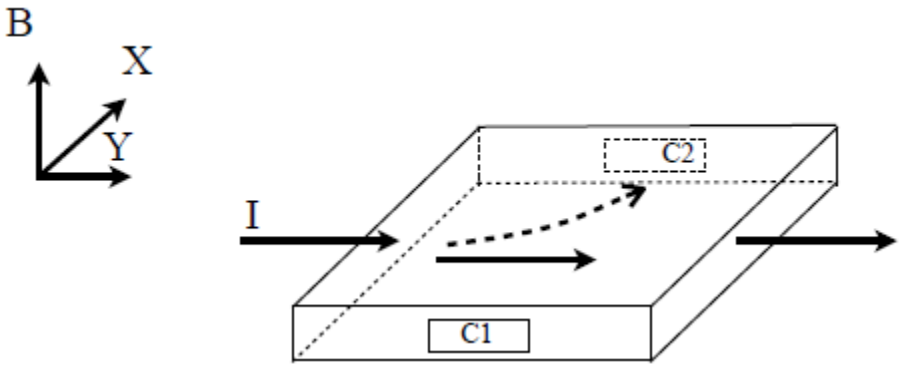

Figure 2.2 A conventional Hall Plate which shows the current flow direction (solid line) and deflected current (dash line) by external magnetic field.

2.3.2 Horizontal Hall Sensor (HHD)

Figure 2.3 shows another structure of the one-dimensional MFS in standard CMOS technology. A single nMOS is utilized in the same way as that of the Hall Plate (Figure 2.2). Current flows from drain to source and two Hall probe contacts located at the side of the nMOS structure detect deflected current when the external magnetic field is applied. Because the influence of the external magnetic field, carriers are deflected to side contacts where the Hall Voltage is detected.

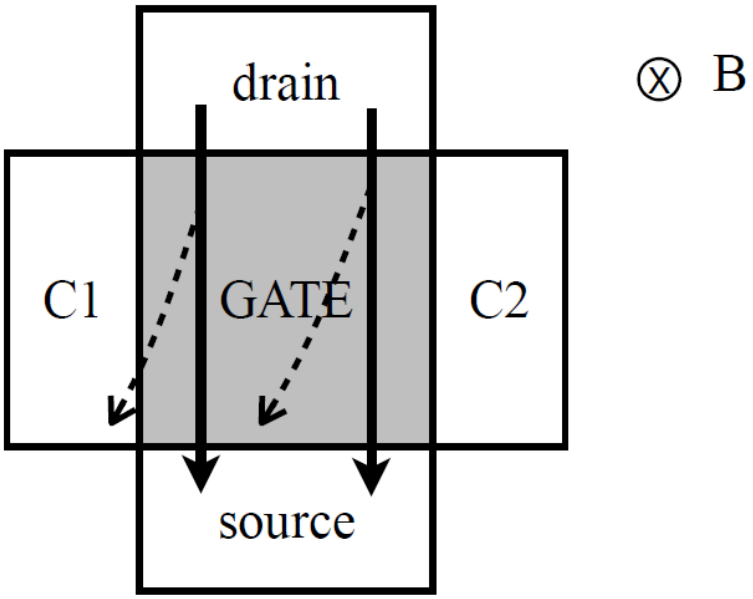

Figure 2.3 The top view of the horizontal MFS in the MOS structure adapted from [4].

2.3.3 Split-Drain (SD) MAGFET

A SD-MAGFET [5] is based on a specific structure where two drains are designed within a single MOSFET to detect the influence of the external magnetic field applied perpendicularly to the device as shown in Figure 2.4. The contacts of the Hall device are transferred from each side of the horizontal Hall device (Figure 2.3) to the SD structure (Figure 2.4). The Hall Effect is demonstrated by the variation of current flowing through

two drains. With the orthogonal magnetic field, current through the channel is deflected from one drain to another. Thus, the magnitude of current at one of the drains increases, while at the other drain decreases. Then, with a resistive load or an active load, the current variation is converted to a voltage signal. By using the SD-MAGFET, small area is consumed and it is easy to be implemented in standard CMOS technology.

Without the external magnetic field applied perpendicularly on the SD-MAGFET, the two drains of the SD-MAGFET maintain a same current value. Carriers are deflected according to the intensity of the magnetic field, which will cause the imbalance of current flowing in two drains. The sensitivity of the device is denoted as follows:

$$S_A = \left|\frac{\partial V_H}{\partial B}\right| \tag{2.20}$$

$$S_{RI} = \left|\frac{1}{t} \cdot \frac{\partial V_H}{\partial B}\right| = \frac{r_n \cdot G}{q \cdot n \cdot t} \tag{2.21}$$

$$S_{RV} = \left|\frac{1}{V} \cdot \frac{\partial V_H}{\partial B}\right| = \mu_n \cdot (\frac{W}{l}) \cdot G \tag{2.22}$$

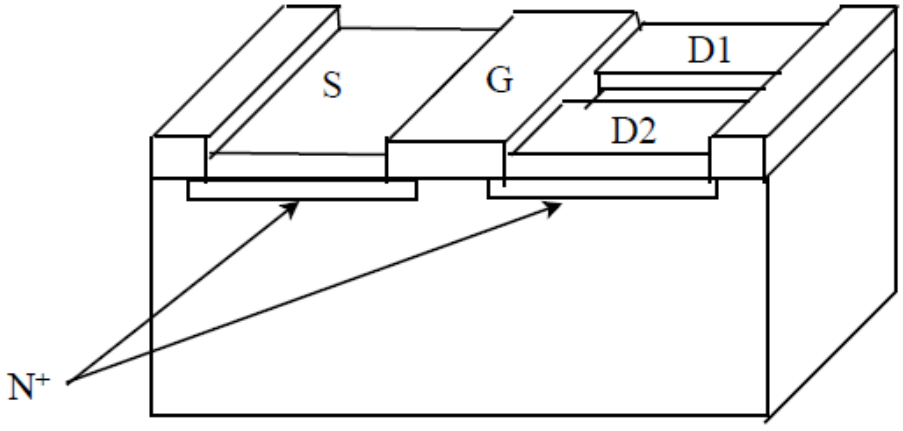

Figure 2.4 The three-dimensional view of the SD-MAGFET adapted from [5].

2.4 Two-Dimensional Magnetic Field Sensor

For the improvement of one-dimensional MFSs, two-dimensional MFSs which involve the function to detect two orthogonal directions of magnetic field are implemented in standard CMOS technology. In this section, several types of two-dimensional MFS for the detection of the horizontal components of the magnetic field are introduced. The advantages and disadvantages are also presented.

2.4.1 Theory of the Vertical Hall Device

In the conventional Hall device (Figure 2.2), Hall probe contacts are connected to each side of the Hall Plate and the current provided by the power supply. However, the conventional Hall Plate cannot be fabricated in standard CMOS technology, due to the limitations of planar manufacturing processes. Thus, a new design which is appropriate to be fabricated in standard CMOS technology is developed (Figure 2.5). In this structure, Hall probe contacts (*H1* and *H2*) are located between the ground contact (*C0*) and power contacts (*C1* and *C2*), and the current is generated between them. By applying the external magnetic field (*B*), the current is deflected as the dash line as shown in Figure 2.5, and a bias voltage between two Hall probe contacts is generated by the influence of the horizontal magnetic field. The sensitivity of the VHD is given in Equation 2.23 as follows:

$$S = \frac{V_B}{B} = \frac{G \cdot r_H}{n \cdot q \cdot t} \times I_p = S_I \times I_p \tag{2.23}$$

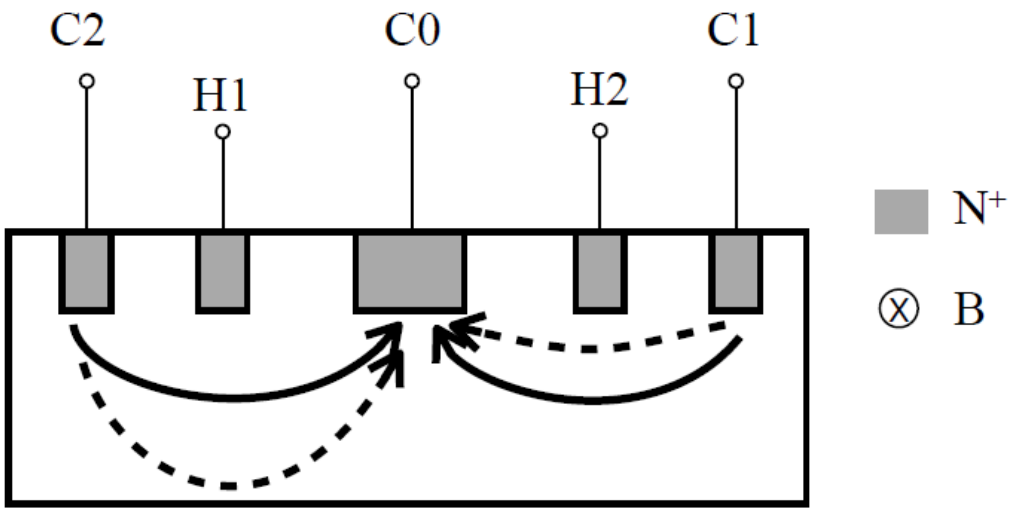

Figure 2.5 The vertical Hall Plate has three Power contacts and two Hall probe contacts. C1 and C2 are connected with VDD, and C0 is connected with GND. Current will flow from C1 and C2 to C0. H1 and H2 are used to detect the variation of current caused by the magnetic field.

2.4.2 Square-Shaped Sensor

An implementation of a two-dimensional MFS in square-shape is introduced in planar CMOS technology as shown in Figure 2.6 [6]. With the potential between power contacts (*C1*, *C2*, *C3* and *C4*) and the central grounded contact (C0), the current flow is set up in N type substrate. Four Hall probe contacts (*H1*, *H2*, *H3* and *H4*) are integrated symmetrically between power contacts and the ground contact. By using a protective ring (P^+), carriers are shaped to flow in the substrate other than the surface of the sensor at the beginning. This implementation increases the ratio of utilization of carriers for the external magnetic field detection. The sensitivity of the device is also increased compared with the conventional Hall Plate. By applying the external magnetic field, the current will be deflected either towards or backwards to the surface of the sensor to generate voltage signals, which can be detected by each Hall probe contact.

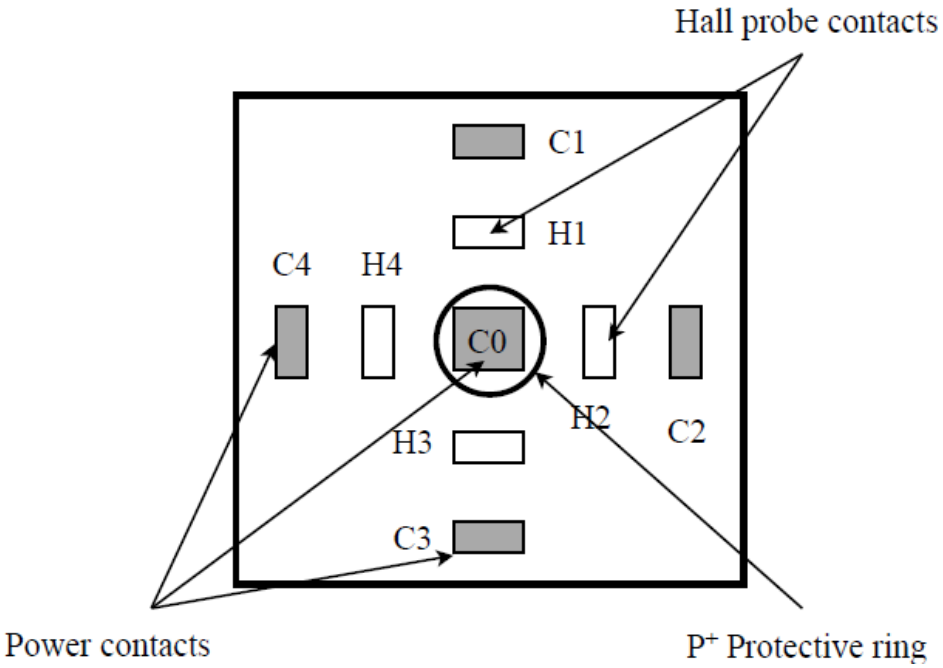

Figure 2.6 The square-shaped two-dimensional MFS adapted from [6].

2.4.3 Bar-Shaped VHD

A Bar-shaped sensor to compensate the drawbacks of conventional VHDs in two-dimensional magnetic field detections is implemented in 0.35μm standard CMOS technology as shown in Figure 2.7 [7]. With a ground contact (*C1*) and two power contacts (*C2* and *C3*), identical current flows prior to the application of any magnetic field between the ground contact and power contacts of the MFS. Hall probe contacts (*CS1* and *CS2*) are placed outside of the power contacts and ground contact to increase the resolution. This design decreases the influence of the flicker noise generated by a shallow N well substrate in 0.35μm CMOS technology. Due to limited current flowing towards Hall probe contacts, the sensor has the same sensitivity compared with the conventional VHD but enhanced resolution in magnetic field detection. With the applied orthogonal magnetic field, current is deflected to Hall probe connections (*CS1* and *CS2*)

as shown in Figure 2.7. By connecting a signal conditional circuit, the signal can be further amplified.

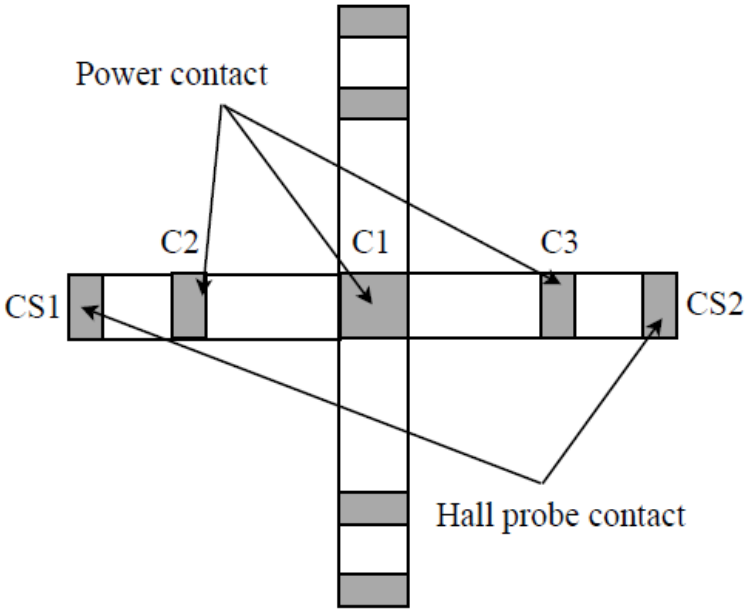

Figure 2.7 The bar-shaped two-dimensional MFS adapted from [7].

2.4.4 Circular Sensor

By utilizing the same operational theory from conventional VHDs, a circular two-dimensional VHD is designed by introducing numerous contacts along the annulus as shown in Figure 2.8 [8]. Each contact is used as the Hall Probe contact and the Power Supply contact alternatively. The signal extracted from each contact is sampled by a programmed embedded system located around the sensor. A sinusoidal signal is generated at the output of the embedded system to detect the intensity of horizontal components of the magnetic field from various angles. In this implementation, the initial offset and nonlinearities caused by the internal interference is reduced. Therefore, more precise signals for the magnetic field detection are obtained.

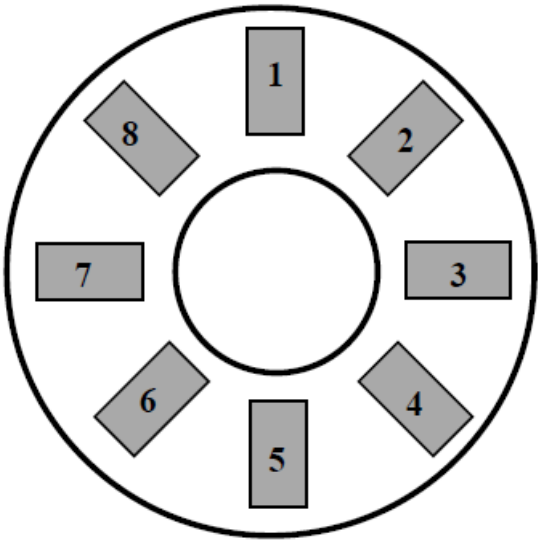

Figure 2.8 The circular-shaped two-dimensional MFS with a Phase Sampling system adapted from [8].

2.5 Three-Dimensional Magnetic Field Sensor

By utilizing the property of the HHD, the structure for the vertical magnetic field detection is integrated with the two-dimensional MFS in standard CMOS technology. Three different implementations are addressed in this section.

2.5.1 Square-Shaped Sensor with the Grounded Central Connection

For the three-dimensional magnetic field detection, the sensor is modified from a two-dimensional MFS introduced in Section 2.2.1. A square-shaped sensor with the central power connection is presented (Figure 2.9) [9]. The function of the three-dimensional magnetic field detection is achieved by splitting each vertical Hall probe contact into two parts to create a contact pair. Under the influence of the horizontal magnetic field, the Hall voltage obtained from each contact pair is identical. With the additional orthogonal magnetic field applied on the sensor surface, the bias voltage in each contact pair is generated according to the signal of the vertical magnetic field. But interferences caused

by the detection of the three-dimensional magnetic field reduce the sensitivity of this MFS. In other words, if the magnetic field has a specific angle against the surface of the sensor, the precision of the MFS is reduced.

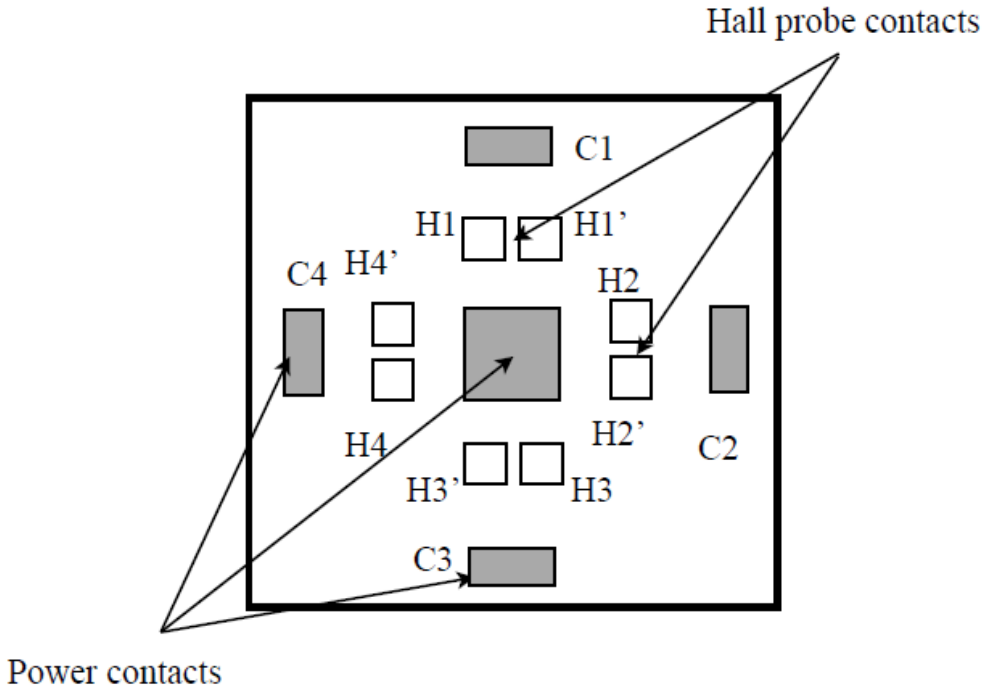

Figure 2.9 The three-dimensional MFS with split Hall probe contacts adapted from [9].

2.5.2 Square-Shaped Sensor with Corner Power Supply Connections

By modifying power and ground contacts to the corner, a square-shaped MFS is designed as shown in Figure 2.10 [10]. Four contacts located at the corner of the square are designed as power or ground contacts. Other contacts are introduced as Hall probe contacts. For the detection of the horizontal magnetic field, the operational principles are identical as that of the VHD. Two opposite Hall probe contacts are implemented as a pair to detect the intensity of the horizontal magnetic field. For the vertical magnetic field detection, adjacent contacts are connected with Hall probes to obtain the signal. But the

detection of the magnetic field with a specific angle remains as a limitation for this device.

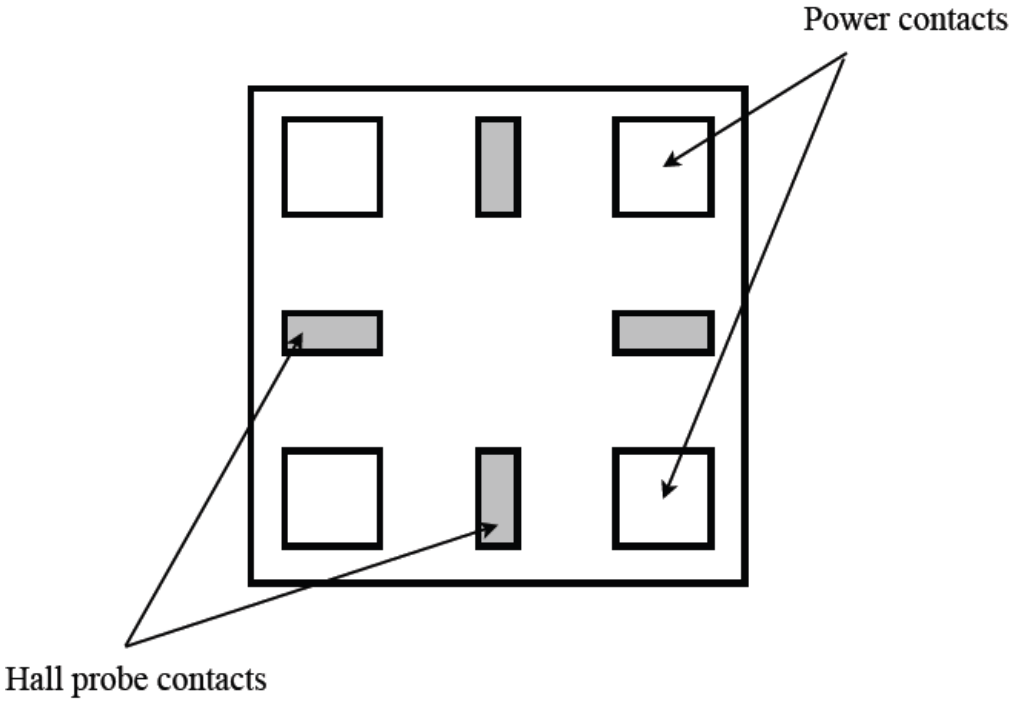

Figure 2.10 The Square-shaped three-dimensional MFS with power supply contacts located at the corner adapted from [10].

2.5.3 BiCMOS Magnetic Field Sensor

To increase the precision of three-dimensional MFSs, a BiCMOS three-dimensional magnetic field sensor is presented as shown in Figure 2.11 where bipolar junction transistors (BJTs) are utilized for the horizontal magnetic field detection, and a split-drain MOSFET is used to detected the vertical magnetic field [11]. The component of the horizontal magnetic field detection (BJT) and the vertical magnetic field detection (SD-MAGFET) is independent. Because they are well integrated, the interference is reduced while detecting the three-dimensional magnetic field. But the power consumption of the BiCMOS three-dimensional MFS is high because of the application of bipolar transistors.

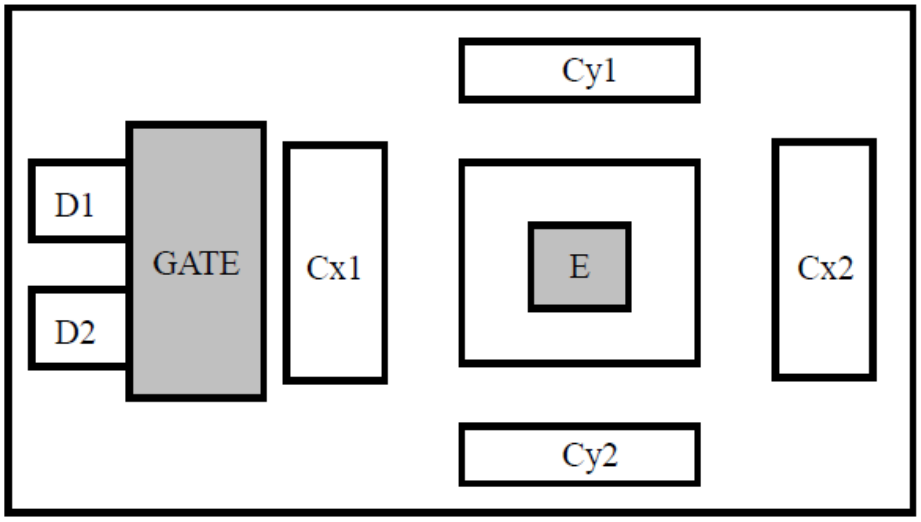

Figure 2.11 The three-dimensional MFS in BiCMOS technology adapted from [11].

CHAPTER 3

THREE-DIMENSIONAL MAGNETIC FIELD SENSOR

In this chapter, a new compact three-dimensional MFS which combines a SD-MAGFET for vertical magnetic field detection and a circular VHD for horizontal magnetic field detection is presented. A brief theory is addressed to clarify the principle of how the sensor works under the external magnetic field. The schematic graph about the position of each unit is introduced. Then the layout design is completed in IC Station and presented in the last section of this chapter.

3.1 SD-MAGFET Structure for the Vertical Magnetic Field Detection

In this design, the SD-MAGFET to detect the orthogonal component of magnetic field is utilized to conduct a competitive result in IBM 0.18μm CMOS technology. The basic operational function is introduced in this section. To design a practicable sensor, four SD-MAGFETs are combined together to reduce the interference due to the geometry mismatch. The layout design is also addressed in this section.

3.1.1 The Operational Principle of the SD-MAGFET

The top view of the SD-MAGFET is shown in Figure 3.1 (a). Without the orthogonal component of magnetic field, Current directly flows from each drain to source. Figure 3.1(b) shows the current flow with the applied vertical component of the magnetic field. The value of Hall electric field is generated corresponding to the intensity of the magnetic field. As a result, part of current flowing through the channel is deflected to the adjacent

drain (e.g., From *D2* to *D1*). For the reverse direction of the vertical magnetic field, part of current is deflected from *D1* to *D2*.

To achieve a high sensitivity [12], the gate ratio (*W/L*) of SD-MAGFET is proved as 1/2, namely, the gate ratio (*W/L*) for each drain is approximated as 1/4.

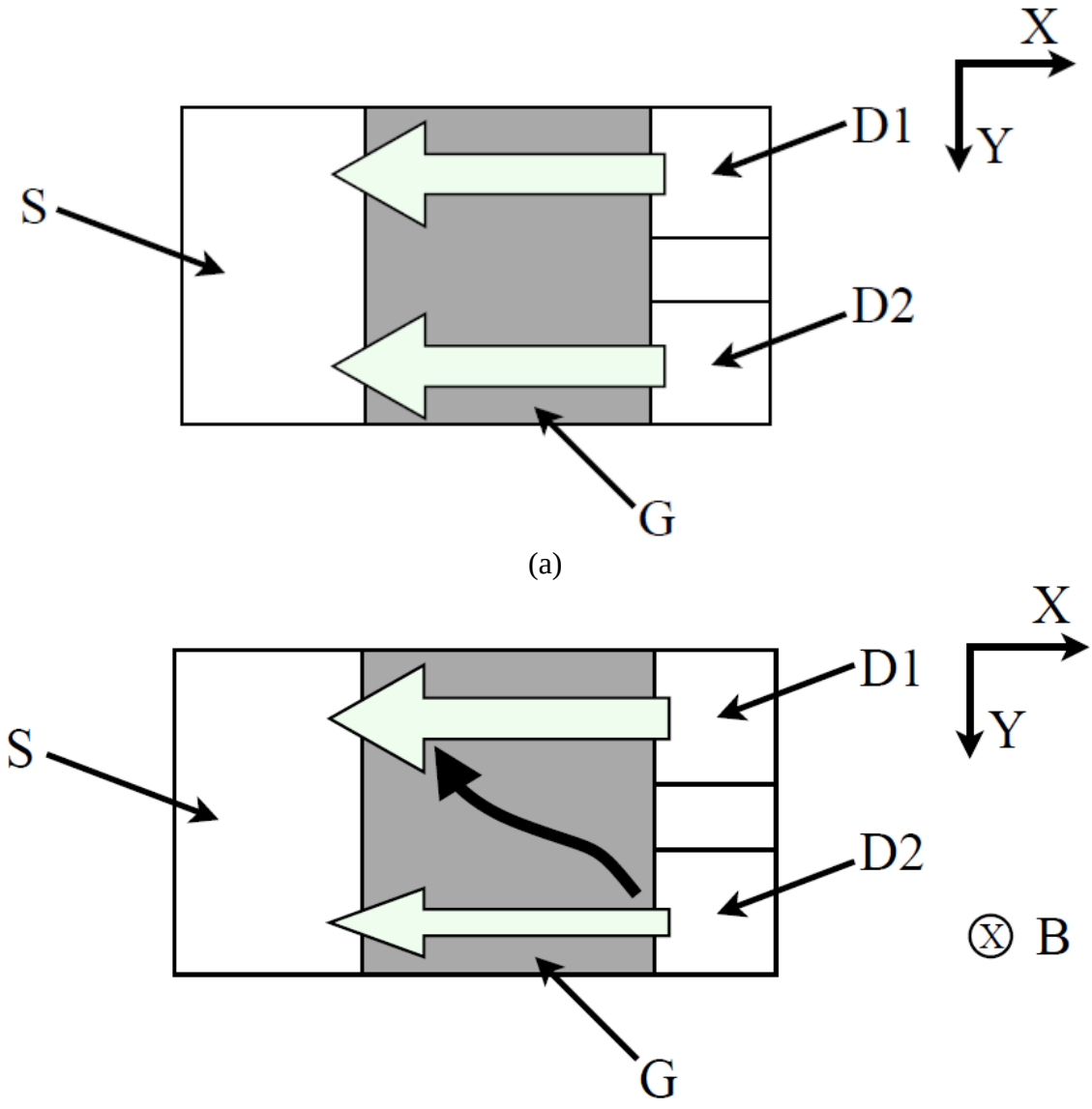

Figure 3.1 Current flows in SD-MAGFET with or without the magnetic field. Figure (a) demonstrates the current-flow without the external magnetic field, and Figure (b) reflects the variation of current inside the SD-MAGFET with the vertical magnetic field.

3.1.2 The Complete Design for the Vertical Magnetic Field Detection

To obtain high precision in the horizontal magnetic field detection, a common source structure is used to connect four SD-MAGFETs as shown in Figure 3.2. The source contact (*S*) connected with ground is designed in the center of the sensor for each SD-MAGFET. Four pairs of the split-drain structure from *D1* to *D8* are utilized to provide a precise signal after computing the average values of all SD-MAGFETs. This is done to enhance the sensitivity and compress the offset.

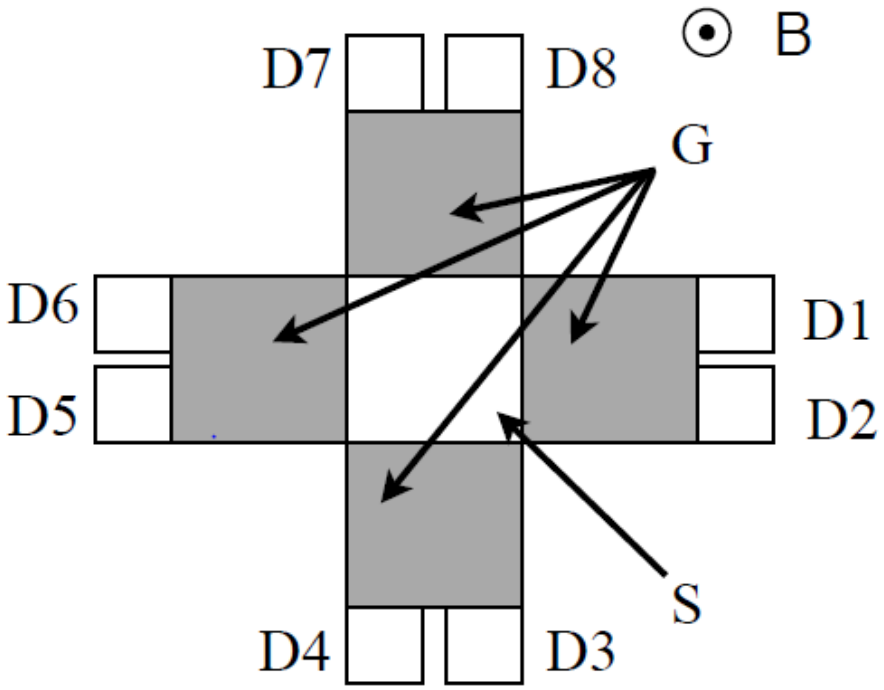

Figure 3.2 Four SD-MAGFETs with a common source connection.

3.1.3 Layout Design for the Vertical Magnetic Field Detection

By considering a high response of sensor in a small area, the layout design for the vertical magnetic field detection is completed in Mentor Graphic IC Station in IMB 0.18μm standard CMOS technology as shown in Figure 3.3. The gate ratio (*W/L*) of each SD-

MAGFET is designed as 8λ/16λ (λ=0.1μm). Thus, the effective width of the common source contact is 8λ and the width for each drain is 3λ.

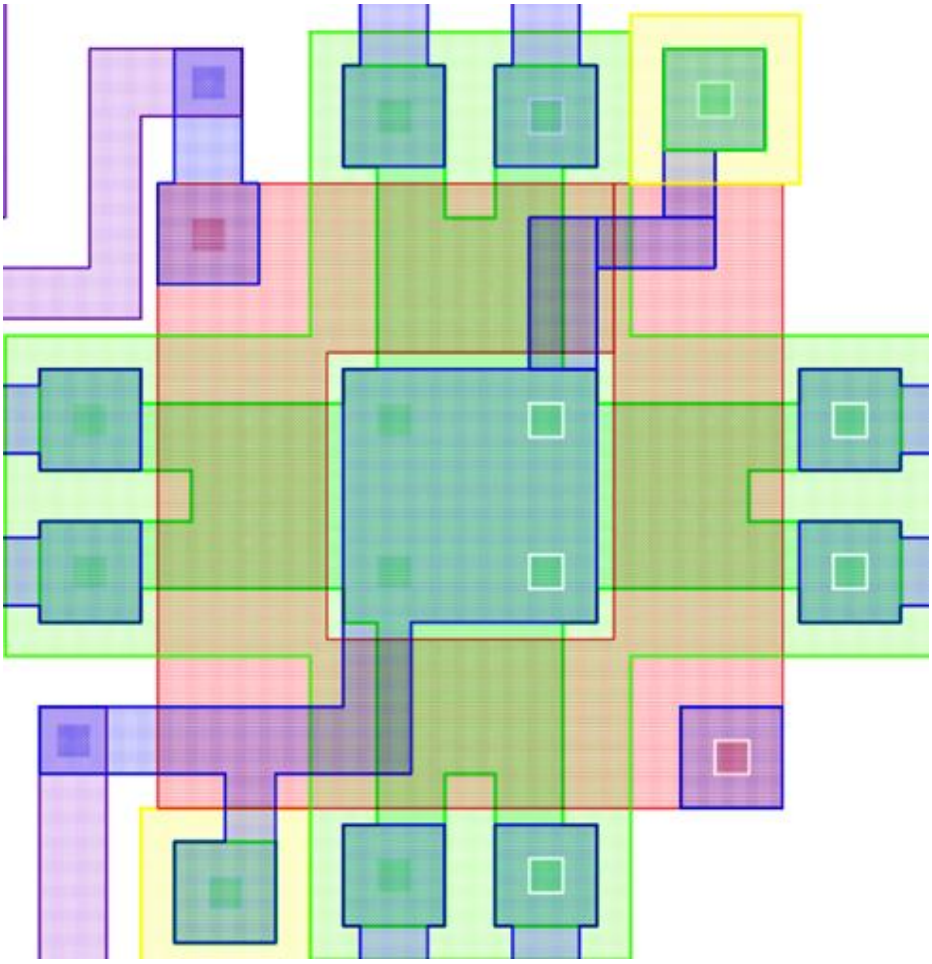

Figure 3.3 The entire layout design for the vertical magnetic field detection

3.2 A Circular VHD Structure for Horizontal Magnetic Field Detections

By utilizing the property of compressing the thermal interference and the basic principle of the square-shaped VHD, a circular VHD is designed for horizontal magnetic field detections. One fourth of the circular VHD is introduced to describe the operational principle. The layout for this part is presented Section 3.2.3.

3.2.1 The Operational Principle of the Circular VHD

To introduce the operational principle of the VHD, the cross section of the circular VHD and the current flow without the external magnetic field is given as shown in Figure 3.4(a). Current flows through the substrate of the device from V_{DD} to V_{SS} along the ring-shaped structure. With Hall probe contacts between power connections (V_{DD} and V_{SS}), a bias voltage is set up for the prior state. By applying the horizontal magnetic field, current is deflected to either bottom or top of the VHD as shown in figure 3.4(b) and 3.4(c) according to the directions of magnetic field. In other words, the voltage between two Hall probe contacts decreases or increases.

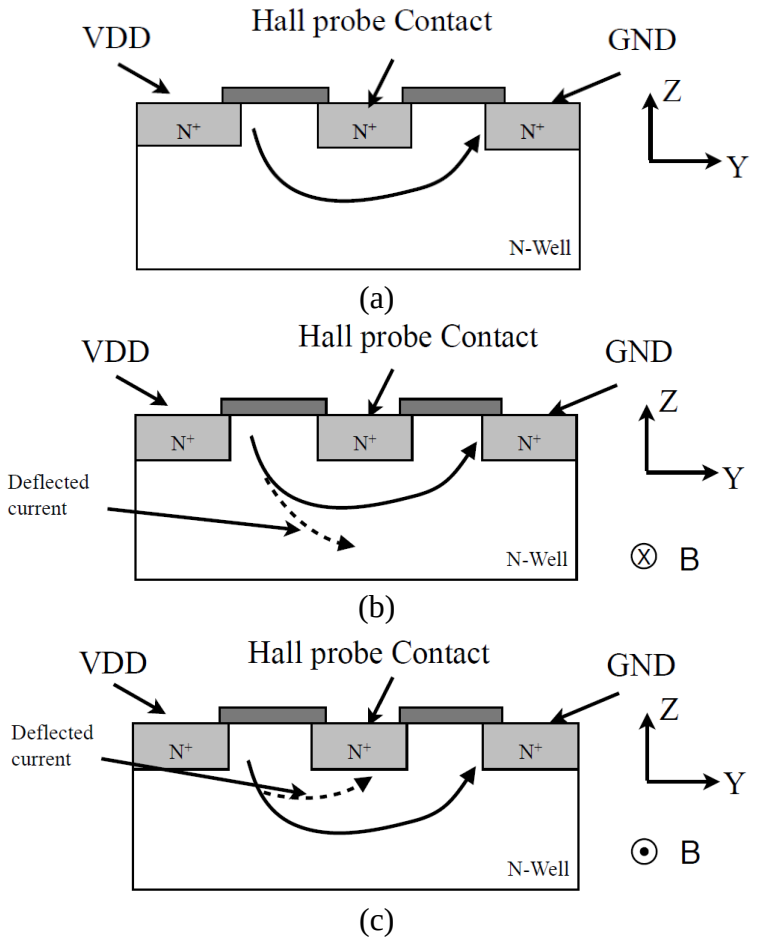

Figure 3.4 Current flowing in the circular VHD with or without the magnetic field. Figure 3.4(a) shows the current-flow in the circular VHD. Figure 3.4(b) and (c) reflect deflected current with the external magnetic field.

3.2.2 The Complete Design for Horizontal Magnetic Field Detections

The circular VHD is designed in this work to detect the components of the magnetic field in horizontal directions as shown in Figure 3.5, where only one fourth of the circular VHD with the current-flow along the dash line is presented in top view. To minimize the size of the MFS and improve the sensitivity, the width of the circular VHD is designed as 40λ. By utilizing the data in the model file of IBM 0.18μm CMOS technology, the resistance of N-well between each contact is calculated from the sheet resistance corresponding to the layout design. The region between the power contact and the Hall probe contact is estimated to a square where the value of width (*W*) and length (*L*) is extracted from the layout. The value of resistance between the power contact and the Hall probe contact is calculated as 1161Ω.

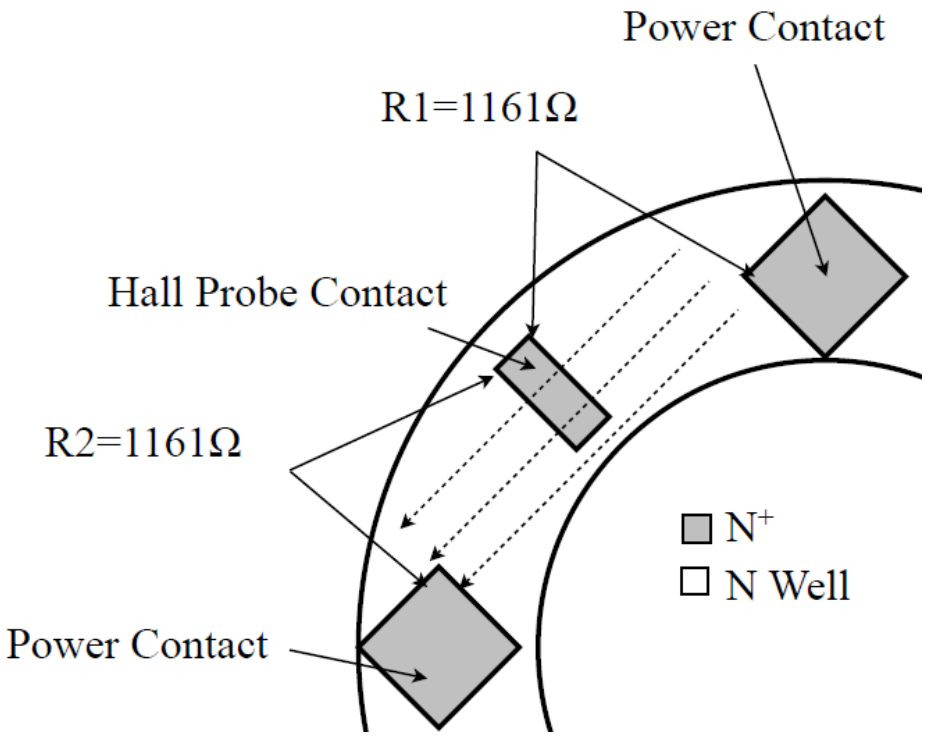

Figure 3.5 One fourth of the circular Hall device. From the extraction, resistance between each power contact and Hall probe contact is designed as 1161 ohms.

The operational principle of the circular VHD [8] aims to improve the sensitivity of the MFS. In this work, a simplest pattern of the ring-shape VHD is designed for rudimentary experiments. By increasing the number of the Hall probe contact on the plate, higher precision will be achieved. Instead of using the sampling method introduced in Propovic's literature [8] to extract the value from the circular VHD, four Hall probe contacts (*Hall Probe Contact 1* to *Hall Probe Contact 4*) are placed to detect the influence of the magnetic field. These contacts are placed between four power terminals (Figure 3.6).

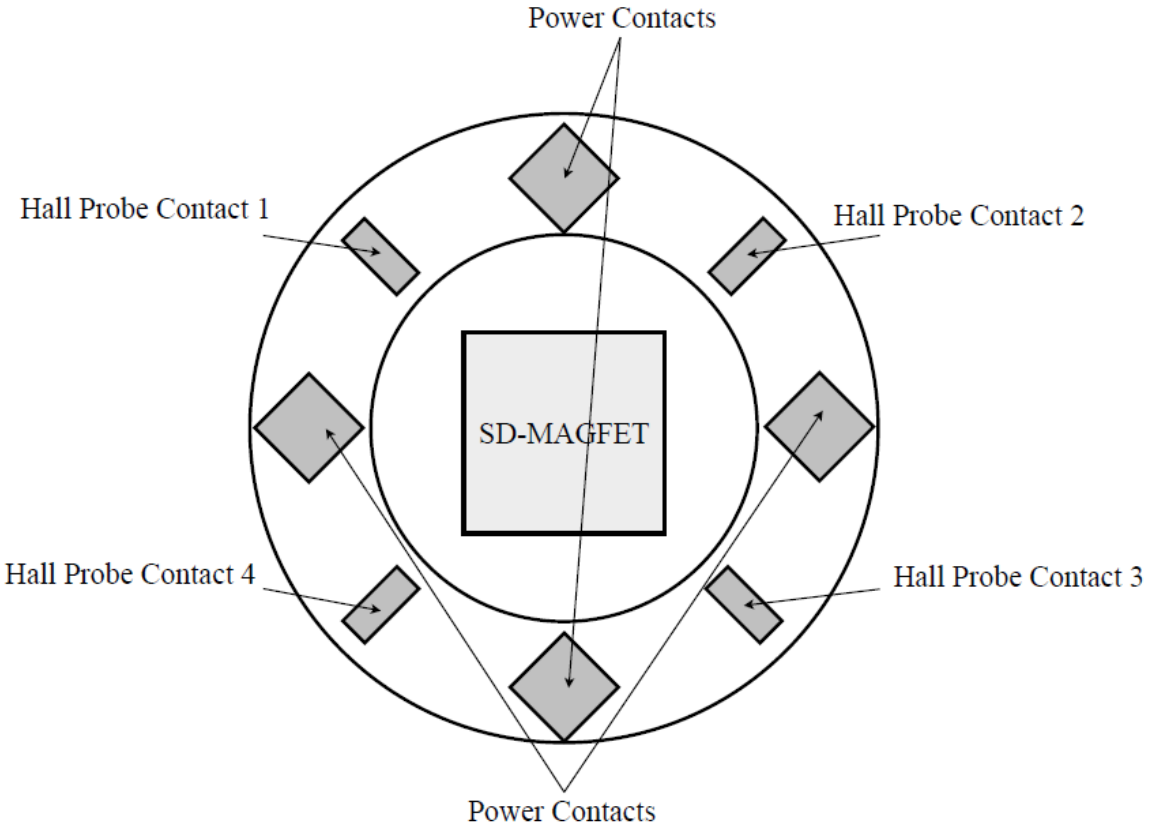

Figure 3.6 The entire pattern of the three-dimensional MFS is shown in this figure. The SD-MEGFET which has the independent power supply is located at the center of the device. The detail of the circular VHD located around the SD-MAGFET is also shown in this figure.

3.2.3 The Layout Design for Horizontal Magnetic Field Detections

According to the schematic diagram shown in Figure 3.6, the layout design is completed in Mentor Graphic IC Station in IMB 0.18μm CMOS technology as shown in Figure 3.7. The minimal space around the SD-MAGFET, located in the center, provides enough space for metal interconnects.

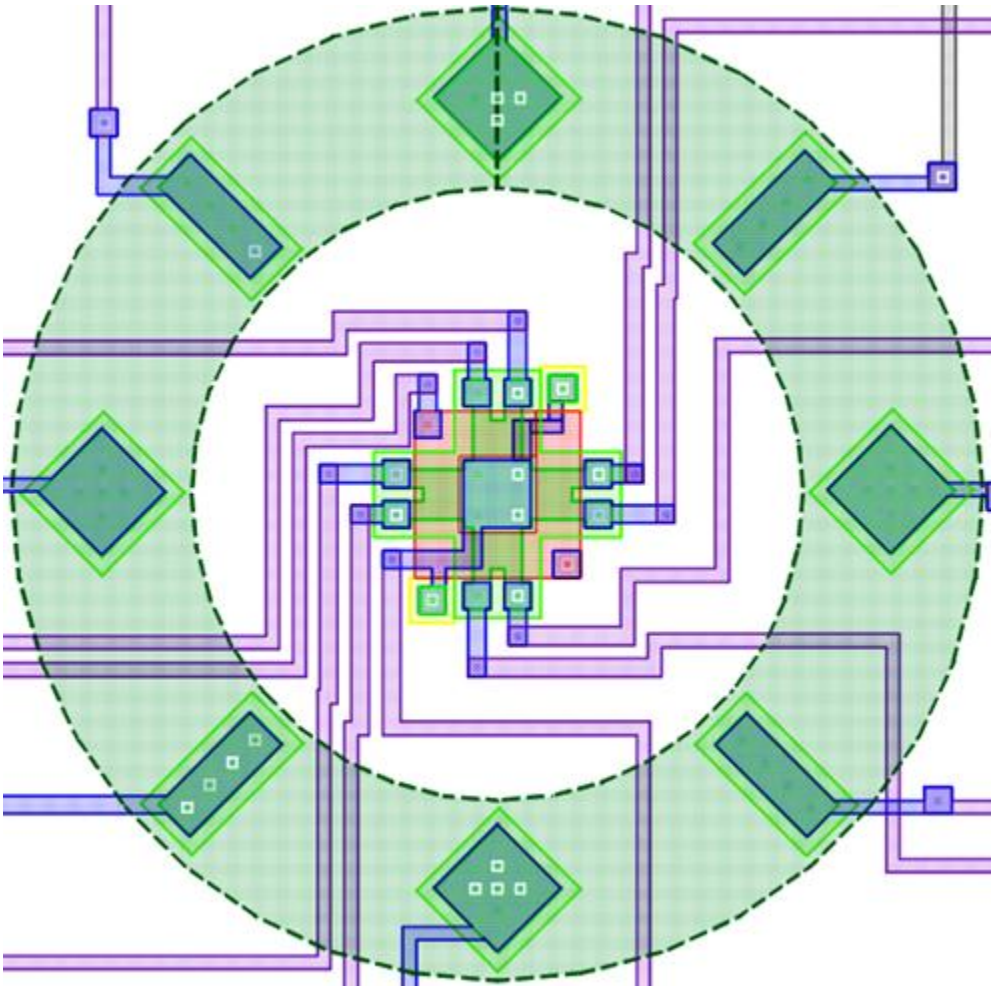

Figure 3.7 The layout of the circular VHD for the horizontal magnetic field detection.

3.3 The Entire Layout Design of the Three-Dimensional MFS

The layout of the entire sensor designed after the schematic is successfully simulated with an optimized device structure. Figure 3.8 shows the entire layout of the three-dimensional MFS along with signal conditioning circuits. The size of the three-dimensional MFS without amplifiers is 31.6μm by 31.6μm and the size of the entire layout for SD-MAGFET is 5.8μm by 5.8μm. Figure 3.9 shows the three-dimensional MFS with bounding pads and its connections with signal amplification circuits. In the center of the layout, only the signal conditional circuit is connected to bounding pads for further experiments. The layer of the over-glass is drawn for each bounding pad. The entire size of the chip is 2.2mm by 2.2mm in 40 pins package.

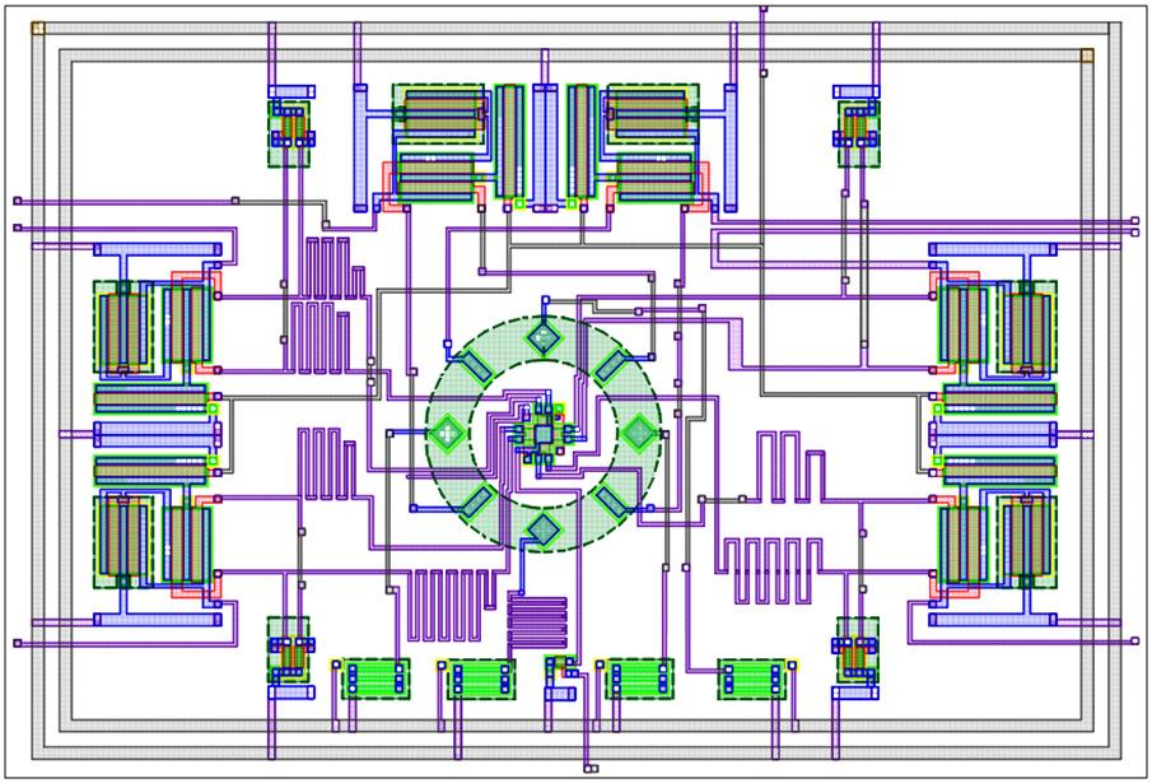

Figure 3.8 The entire layout of the three-dimensional MFS.

In addition, each part of the sensor is connected with separate pads as shown in Figure 3.9. The individual function of sensors and amplifiers can be tested separately to obtain detailed results. The first part is the connection with the entire sensor, the second part is the connection with the circular VHD for the horizontal magnetic field detection, the third part is the connection with the SD-MAGFET for the vertical magnetic field detection and the fourth part is the connections of every node for both SD-MAGFET and circular VHD.

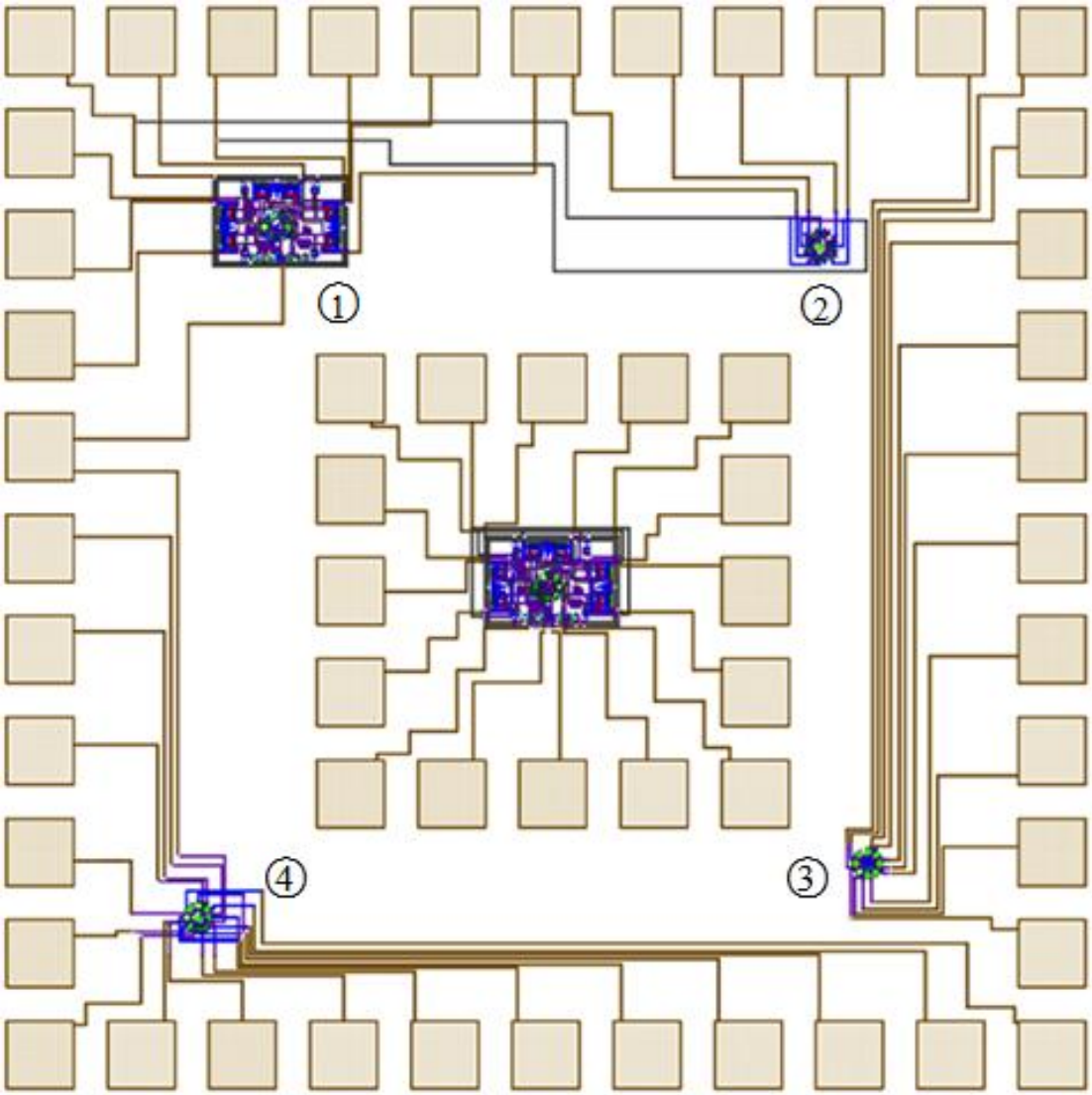

Figure 3.9 The chip layout of the three-dimensional MFS for further experiments.

3.4 Summary

In this chapter, the basic operational function of the sensor to detect external magnetic field is introduced. A complete design of the three-dimensional MFS is presented. The sensor is connected to the signal amplification circuit to further amplify the signal obtained from the external magnetic field. The Layout design is completed and verified in Mentor Graphic IC Station.

CHAPTER 4

THE AMPLIFICATION IMPLEMENTATION AND EQUIVALENT CIRCUIT

The main advantage of this sensor designed in CMOS technology is the integration of signal amplification circuits along with the sensor in a same substrate. The signal amplification circuit needs to be optimized by the circuit simulator software, Hspice. Since the MFS consists of the unique design as described in Chapter 3, the equivalent circuit of the MFS needs to be extracted such that both MFS and the signal amplification circuit can be simulated together. This enhances the system performance. In this chapter, the equivalent circuits of the MFS and the amplifier are presented to conduct the simulation in Hspice. The results of simulations are obtained to verify the sensitivity of each component of MFS, and the property of the signal conditioning circuit. The resolution of the MFS is analyzed also.

4.1 Equivalent Circuit of MFS

To optimize the layout design, the equivalent circuit of the three-dimensional MFS needs to be simulated in Hspice. To maximize the signal amplification, the characteristics of the output voltage swing are outlined.

4.1.1 SD-MAGFET for the Vertical Magnetic Field Detection

From Chapter 3, the gate ratio (*W/L*) of the SD-MAGFET is assigned as 8/16 in order to obtain high sensitivity with a minimal area. For the implementation of the SD-MAGFET in Hspice, the SD-MAGFET devices are split into two identical transistors. The

schematic of the circuit is shown in Figure 4.1. The aspect ratio (*W/L*) of each MOSFET is considered as the half of the original SD-MAFGET concluded as 4/16.

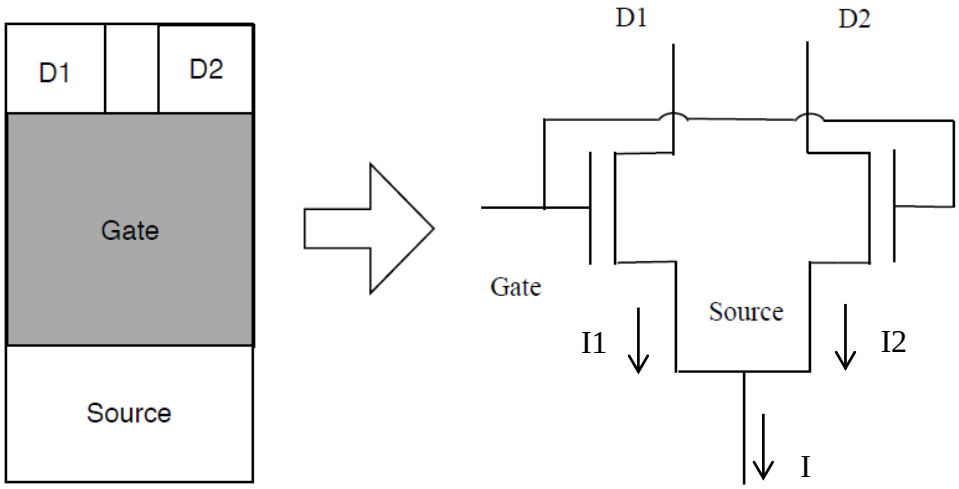

Figure 4.1 The equivalent circuit of the SD-MAGFET.

In standard CMOS technology, a pMOS active load is considered to maintain the n-channel MFS working in the saturation mode. The basic amplification circuit along with the SD-MAGFET is shown in Figure 4.2. To fabricate in 0.18 µm CMOS technology, the bias current (*I*) is set to 20 µA with the positive power supply (V_{DD}=*1.8V*) and the negative power supply (V_{SS}=*-1.8V*). Thus, the current at each drain (*D1* and *D2*) of the SD-MAGFET is 10 µA. After extensive simulations, the geometry of the bias transistor (pMOS active load, *MP3* and *MP4*) is determined in the ratio as 4/18. The gate of the SD-MAGFET (*BIAS1*) is connected to the ground to provide a prior voltage at output nodes (*Vout1* and *Vout2*). To emulate the carrier deflected by the external magnetic field in the MFS, the current for each drain is altered manually. With the integration of the pMOS active load, the current imbalance generated by the magnet field is converted to a voltage signal at the output nodes of the SD-MAGFET as shown in Figure 4.2. To calculate the sensitivity of SD-MAGFET, Equation 4.1 is used as follows:

$$S = \frac{|I_1 - I_2|}{(I_1 + I_2)|B|} \tag{4.1}$$

I_1 and I_2 are the current at *D1* and *D2* as shown in Figure 4.1. To calculate the mobility of carriers under the external magnetic field, Equation 4.2 is introduced

$$\mu_H = \mu_n \cdot r_H \tag{4.2}$$

where μ_H suggests the Hall mobility generated by the external magnetic field at the channel of each equivalent MOSFET, μ_n is the effective mobility of electrons, the main carrier of the nMOS, and r_H denotes the Hall scattering factor.

Let $\Delta I_{DS}=|I_1-I_2|$ and ΔI_{DS} can be calculated in Equation 4.3 [5],

$$\Delta I_{DS} = \frac{1}{2}\mu_H \left(\frac{L}{W}\right) I_{DS}|B|G \tag{4.3}$$

where *G* denotes the geometrical correction factor and $I_{DS}=I_1+I_2$. By assuming a condition that $G=1$ and $r_H=1$, with $I_{DS}=20\mu A$ the sensitivity of the SD-MAGFET can be calculated as 16.2%T^{-1}, which means that for each 1T change of magnetic field, the current value in each drain is altered by 1.62 μA.

For the simulation of the SD-MAGFET in Hspice, the equivalent circuit given in Figure 4.1 is used. Because the SD-MAGFET is biased in the saturation mode to maintain the linearity for the MFS, the expression for saturation current in MOSFETs is utilized as shown in Equation 4.4.

$$I_{DS} = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2 \tag{4.4}$$

I_{DS} is the saturation current, μ_n suggests the mobility of electron, V_T is the threshold voltage, and C_{OX} denotes the capacitance per unit area of the gate oxide. Furthermore, μ_n, C_{OX} and V_T are given in the model file of IBM 0.18μm CMOS technology. V_{GS} is fixed by connecting the gates of *MN1* and *MN2* (Figure 4.2) to the ground. Then, the current variation can be emulated by modifying the widths (ΔW) of *MN1* and *MN2*. In other words, the width of *MN1* is increased by 0.015λ/T whereas the width of *MN2* is decreased by 0.015λ/T to emulate 1.62μA changes in current at each drain. Figure 4.3 shows the output voltage property of the SD-MAGFET after applying the vertically external magnetic field (*B*).

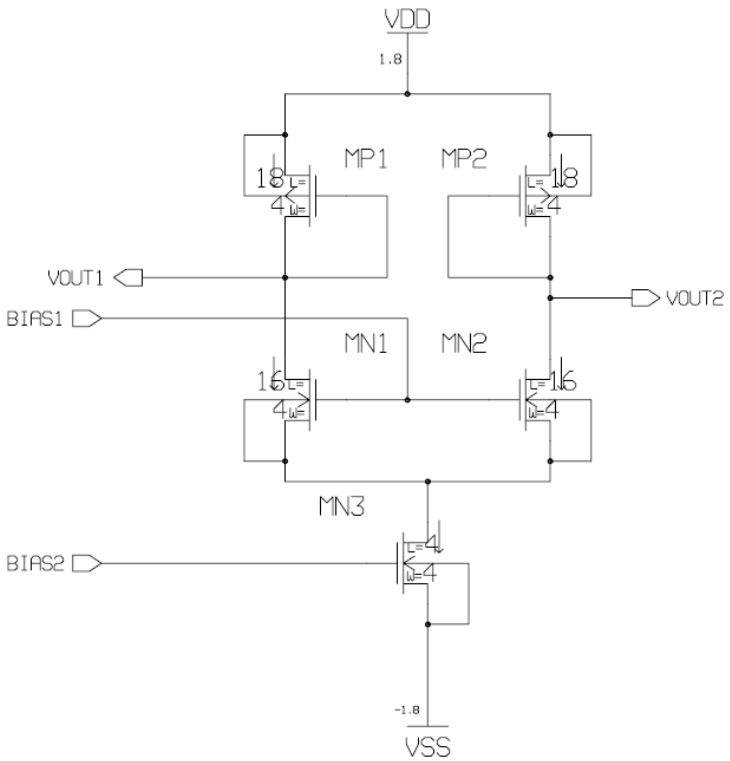

Figure 4.2 The equivalent circuit of the SD-MAGFET. Circuit of the pMOS active load and the current sink is shown in this figure as well. The SD-MAGET is split into two nMOSs.

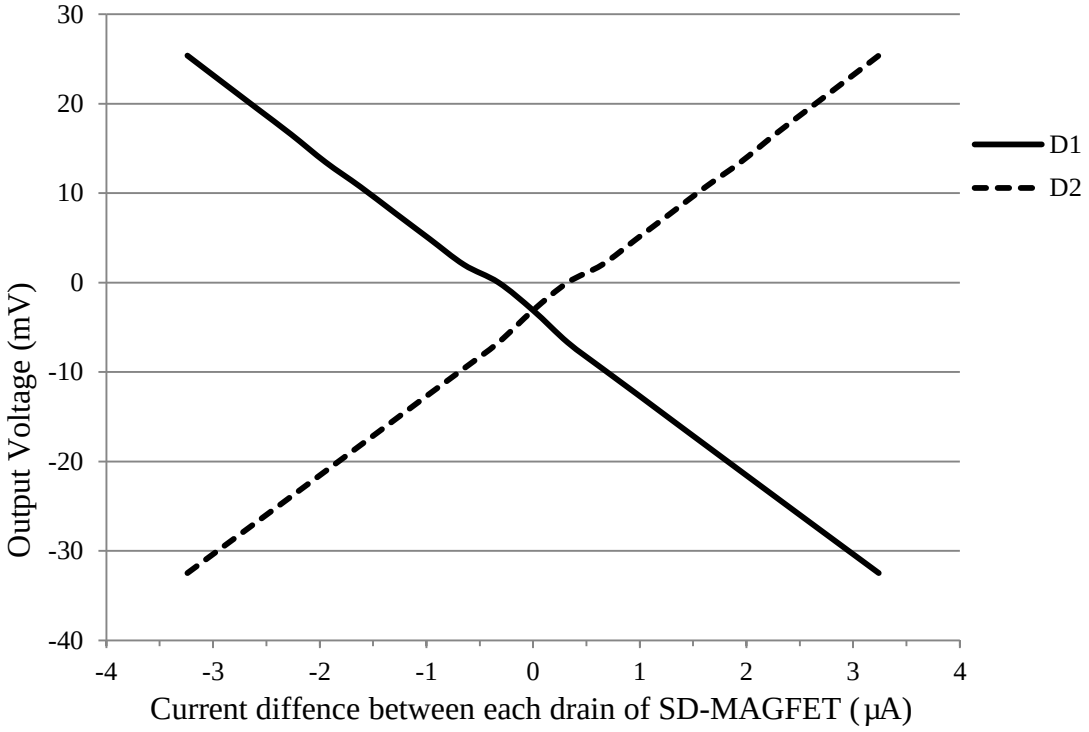

Figure 4.3 The output voltage swing of the SD-MAGFET.

4.1.2 Circular VHD for Horizontal Magnetic Field Detection

To implement the circular VHD to the schematic circuit that can be further simulated in Hspice, the space (n-Well) between each power contact and Hall probe contact is converted into resisters (from *R1* to *R8*) as 1116Ω. The value of each resistor is extracted from the layout as shown in Figure 4.4.

To simulate the circular VHD, the equivalent circuit is obtained by using two resisters (*R1*, *R2*) between power contacts and Hall probe contacts according to the geometric size in layout as shown in Figure 4.5. To provide bias current at the prior state, two resistive loads (*R9* and *R10*) are connected to either *VDD* or *VSS*, respectively.

The bias current in circular VHD is assigned as 50μA to achieve comparable sensitivity with the SD-MAGFET. According to the exact size measured from the layout,

the value of the load resistors is calculated as 17.4KΩ. The prior value of the Hall contacts is set to zero to utilize the maximum voltage swing of the amplifier. The sensitivity of the circular VHD integrated in N-well structure can be calculated by Equation 2.18 with a given value of n (density of free electrons), t (thickness of the N-well) from the model file. I_p (bias current) is given as 50 µA. Consequently, the proximate value of sensitivity of the VHD is calculated as 1100V/(AT) [8] which is 23.7 µA/T after considering the supply voltage. The characteristic of the voltage at each Hall probe contacts is shown in Figure 4.6 where exhibits voltage variations due to the influence of the external magnetic field.

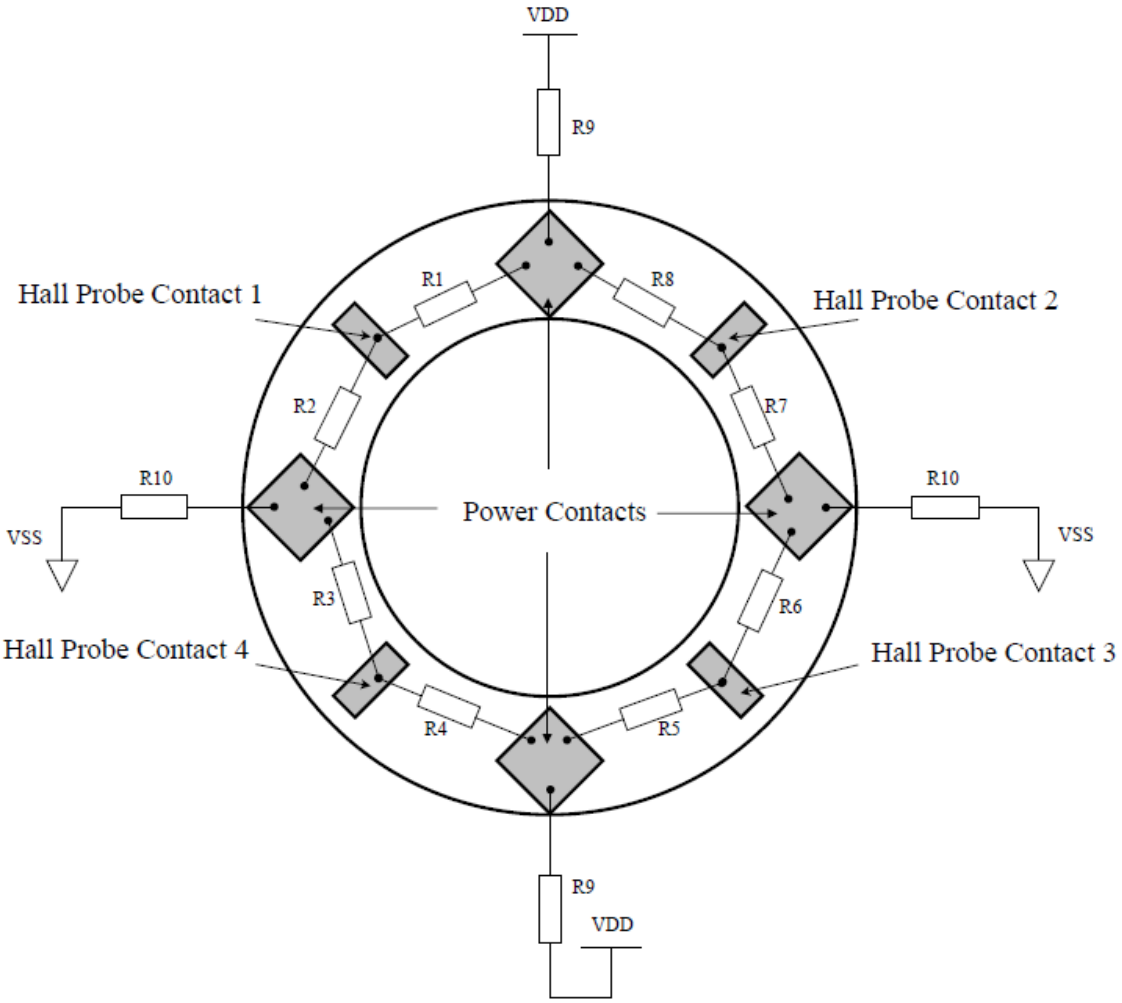

Figure 4.4 The conversion of the VHD in the form of resistor.

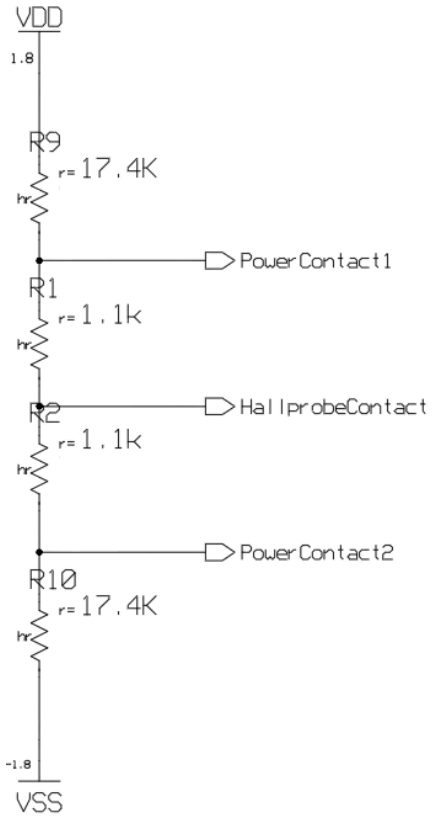

Figure 4.5 The equivalent circuit of the circular VHD.

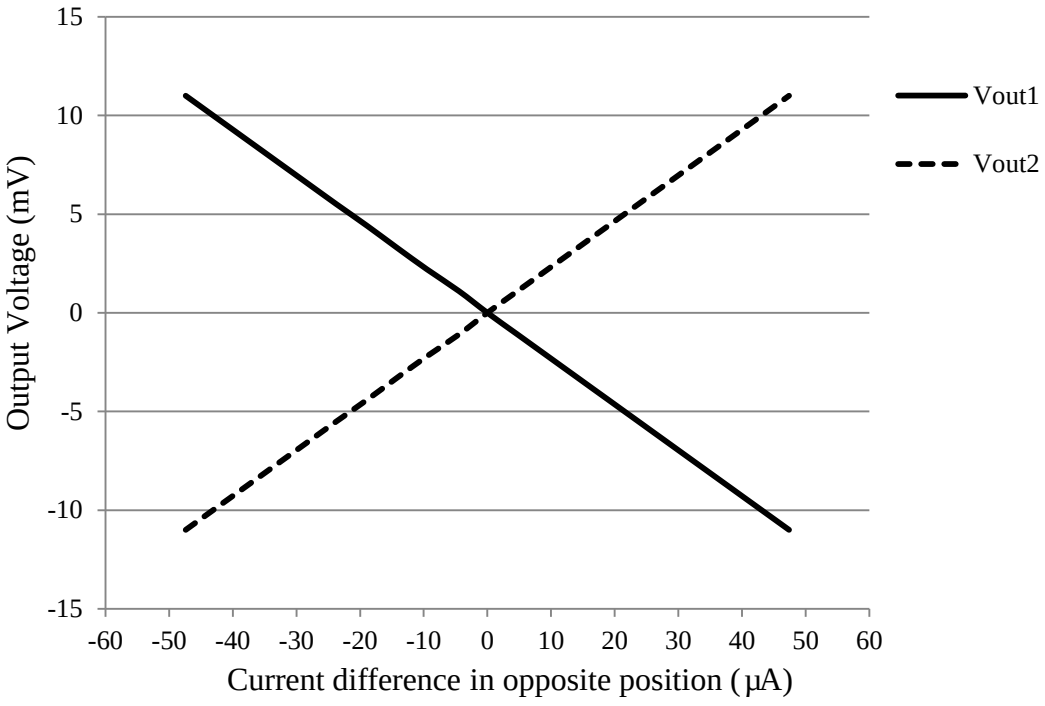

Figure 4.6 The output voltage swing after applying the horizontal magnetic field.

4.1.3 The Resolution Analysis of Three-dimensional MFS

The intrinsic noise (Thermal noise or Flicker noise) is beyond the scope of the DC signal analysis for the simulation with the external magnetic field. Thus, to analyze the resolution of the MFS, the mismatch of the devices is considered. From the data published by TSMC in 0.18μm CMOS technology [13], the single chip device mismatch is minimal for the adjacent device. The equation describing the mismatch technology is given below [13]:

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W \cdot L} \tag{4.5}$$

where A_β is the proportionality constant which is technology-dependent. β is the conductance of the transistor and it can be calculated by the equation as follows:

$$\beta = 0.5\mu_n C_{OX}\frac{W}{L} \tag{4.6}$$

$\Delta\beta$ in Equation 4.5 is the mismatch value that depends on manufacturing technology of the device. $\sigma(\Delta\beta)$, the standard deviation of $\Delta\beta$, is calculated by equation given below:

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})^2} \tag{4.7}$$

where σ is the standard deviation, N is the number of values in the sample, x_i is the random value obtained from the sample and $\bar{x}$ is the mean value of the sample.

A_β is the constant extracted from real chip measurements. The value of A_β is obtained under 1.8V supply voltage in 0.18µm CMOS technology. From the literature [13], A_β is given as 0.33% in micron meter.

To analyze the mismatch in the SD-MAGFET, the width (W) and length (L) are considered as 0.8µm and 1.6µm, respectively. Thus, the values of W and L for the simulation are 0.4µm and 1.6µm for each nMOS transistor that is used to emulate the dual-drain SD-MAGFET. Consequently, the product of W and L can be calculated from Equation 4.5. Then, $\Delta\beta$ can be estimated as 1.0041β by using Equation 4.6 and 4.7.

Therefore, the current variation due to the mismatch in each drain can be obtained from Equation 4.4 prior to application of any magnetic field. Then, the Signal-to-noise ratio (SNR) can be calculated from the equation given below.

$$SNR = \frac{I_{signal}}{I_{noise}} \tag{4.8}$$

Thus, the SNR is concluded as 243.9. In addition, the resolution of the SD-MAGFET can be determined and the minimum value that can be detected by the SD-MAGFET is 0.43mT in DC signal analysis.

For the analysis of the circular VHD, the same method is used to obtain the resolution of the sensor. Because $\Delta\beta$ can be calculated in Equation 4.6, the mismatch of β can be setup as the mismatch of W/L. By using this method, the mismatch of the resistance between each contact can be estimated in the circular VHD. The SNR and the

resolution of the circular VHD are determined to be in the same order of magnitude as that of the SD-MAGFET.

4.2 Signal Conditioning Circuit

By integrating the amplification circuit, the variation of the sensor signal can be further amplified to provide a significantly large signal for detecting low intensity magnetic field. The equivalent circuit and characteristics of the amplifier circuit are discussed in this section. To utilize the maximum voltage swing at the output of the amplifier, extensive simulations were carried out and device sizes were optimized. Then, to estimate the intensity of the magnetic field that can be amplified linearly, the circuit diagrams of amplifiers along with the sensor circuit was simulated. The results of this simulation are discussed towards the end of this chapter.

4.2.1 Design of Amplifier

A dual-input amplifier is considered where each output terminal of the sensor is connected to the input nodes of the amplifier. Figure 4.7 shows the one of six identical differential amplifiers in telescopic cascode topology that is designed and connected to the output nodes of the SD-MOSFET (Four) and the circular VHD (Two). The transistors of this circuit are designed as *AMN1* to *AMN3* and *AMP1* to *AMP4*.

The bias current that influences the gain of the amplifier needs to be determined. After being simulated in Hspice, four pMOSs (*AMP1, AMP2, AMP3* and *AMP4*) (*W/L = 100/10*) are integrated as cascode current mirrors. This integration determines voltage levels at each node and control the maximum value of voltage swing at the output. The

gates of the nMOSs (*AMN1* and *AMN2* with *W/L=50/100* each) are designed as the inputs of the amplifier. The trans-conductance can be calculated in Equation 4.9.

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} \tag{4.9}$$

The current bias transistor (*AMN3*) that is set as the current source, has an aspect ratio *W/L=100/30*. This derives a 50 µA current for the amplifier. Thus, the current in *AMN1* and *AMN2* equals to 25 µA. With a given value of $\mu_n \cdot Cox$ in the model file of 0.18 µm CMOS technology and the ratio of *AMN1* and *AMN2*, g_m is calculated as 1.7651×10^{-4} (1/Ω). In addition, the output impedance is concluded in Equation 4.10 as follows.

$$R_{out} = r_{O(MN2)} || (r_{OMP2} + r_{OMP4}) \tag{4.10}$$

where r_O suggests the channel modulation resistance. Then, R_{out} can be calculated as $7.93 \times 10^5 \Omega$.

For DC signal processing in this work, the maximum voltage swing at the output node is important. Thus, the power supply for the amplifier is assigned from -1.8V to 1.8V and the common mode input range is assigned from -0.5V to 1.5V. The gain (A_V) of the amplifier estimated by using the Equation 4.11 is calculated as 182 [14].

$$\mathrm{A_V} = \mathrm{g_M} \cdot \mathrm{R_{out}} \tag{4.11}$$

To verify the operational function of the amplifier, the voltage at the prior state of each node is extracted after the simulation in Hspice, The voltage at the drain of current sink (*MN3*) is -0.97V, the voltage at each output node is 0.4V and the voltage at the drain of pMOS active loads (*MP3* and *MP4*) are both 1.1V.

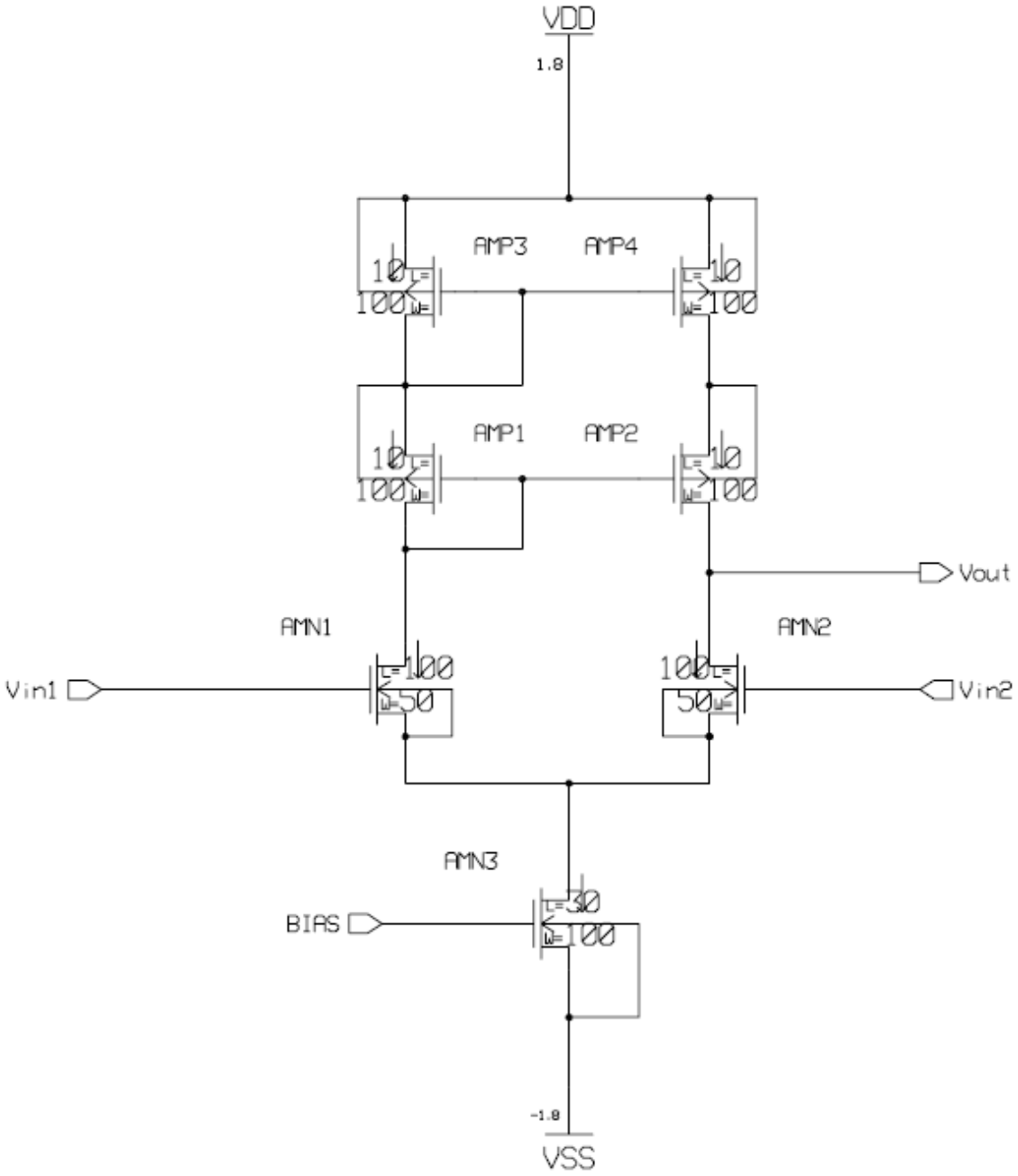

Figure 4.7 The equivalent circuit of the cascode amplifier.

4.2.2 SD-MAGFET with amplifier

To simulate the characteristics of the SD-MAGFET for the vertical component of the magnetic field detection, the equivalent circuit of the SD-MAGFET is connected to the input node of the cascode amplifier as shown in Figure 4.8. Current flowing through the two nodes (*A* and *B*) (Figure 4.8) is altered due to the deflection of carriers in the SD-MAGFET. The output voltage at these nodes of the SD-MAGFET is either increased or decreased according to the direction of the magnetic field.

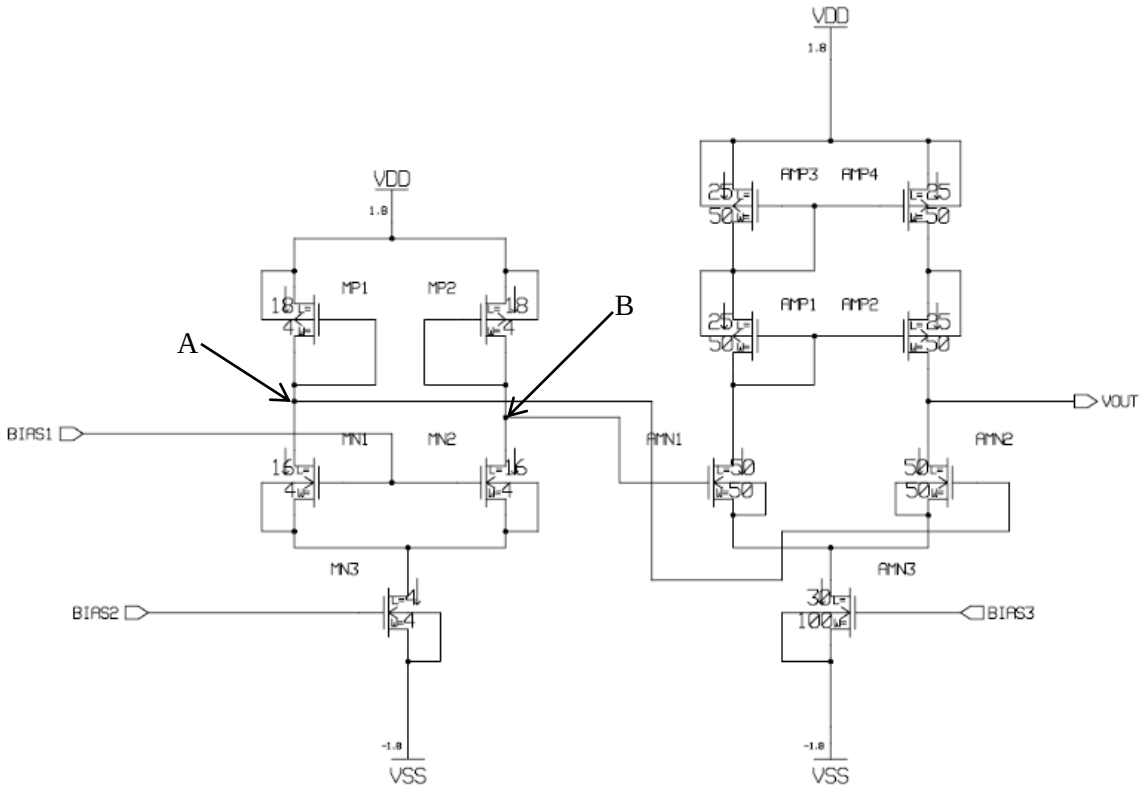

Figure 4.8 The equivalent circuit of the SD-MAGFET with the amplifier.

Because G and r_H can be tested only from the experiment, the exact value of current that is altered by the external magnetic field cannot be obtained before that. However, by assuming $G=1$ and $r_H=1$, the trend of the variation caused by the magnetic field can be emulated by the alternation of current in the SD-MAGFET. Thus, a

simulation result (current vs. voltage) is obtained to imitate the output voltage swing under the vertical magnetic field (Figure 4.9). Assuming that the sensitivity of the SD-MOSFET is calculated as $16.2\%T^{-1}$, for every 100mT changes in magnetic field, the total current will change 0.324μA as the input signal for the amplifier. In Figure 4.8, *BIAS1* is connected to the ground to provide the bias voltage for the SD-MAGFET, *BIAS2* is connected to the current sink to maintain a stable bias current for SD-MAGFET, and *BIAS3* is connected to the current sink of the amplifier.

In addition, the linear region, the effective working interval of the amplifier, is assigned from -500mT to 500mT for the external magnetic field detection. Each 100mT change is simulated as 182mV voltage variations at the output nodes of the amplifier.

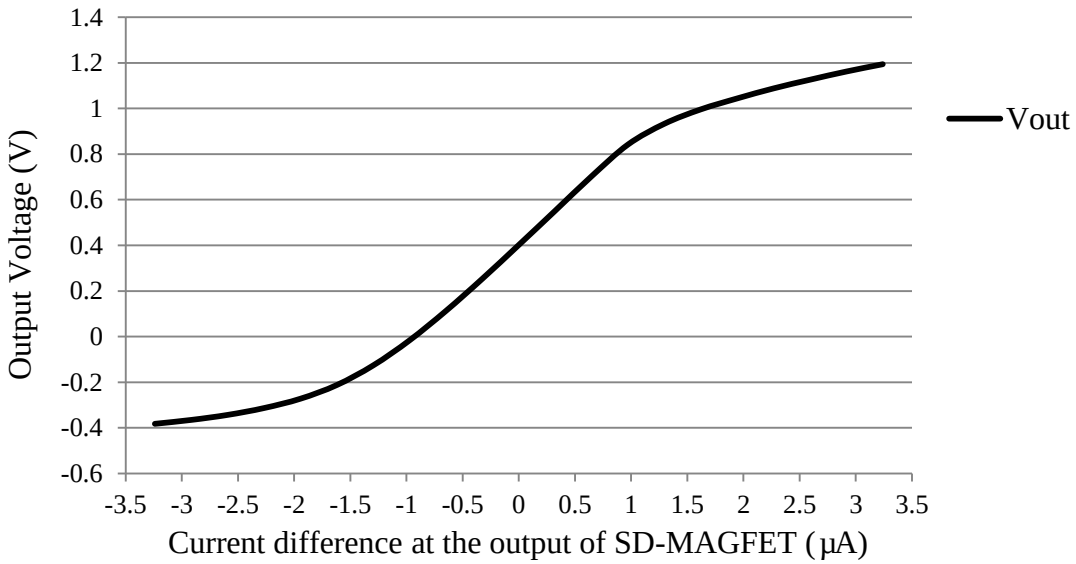

Figure 4.9 The voltage characteristic of the amplifier at the output node.

4.2.3 Circular VHD with amplifier

To examine the characteristics of the circular VHD, two Hall probe contacts located at the opposite side on the device are simulated. The equivalent circuit of the circular VHD connected with the signal conditional circuit is shown in Figure 4.10. Two resistor pairs (*R1*, *R2* and *R5*, *R6*) are extracted from the circular VHD as shown in Figure 4.4. Two output nodes (*Hall Probe Contact 1* and *Hall Probe Contact 4* in Figure 4.4) are connected to two input nodes of the differential amplifier.

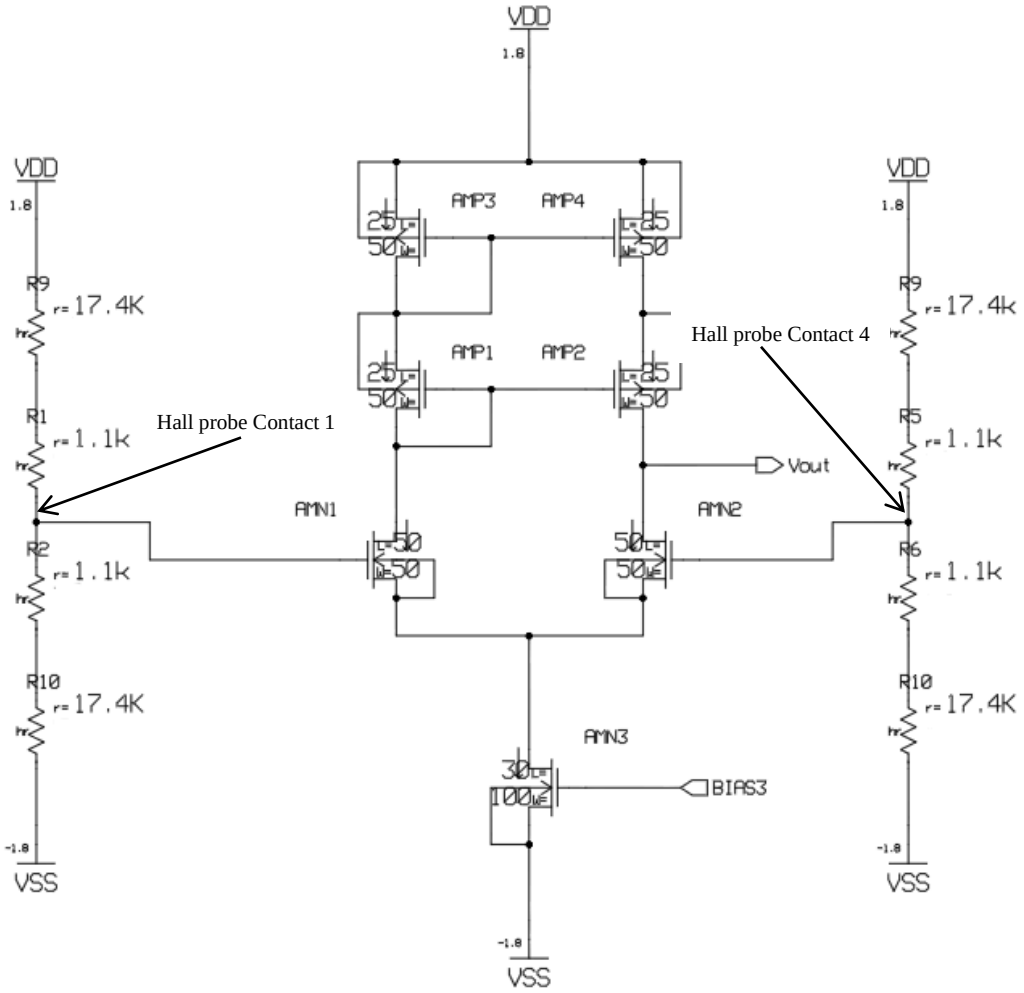

Figure 4.10 The equivalent circuit of the circular VHD connected with the amplifier.

From the analysis [8], the sensitivity of the circular VHD is obtained as 23.7 μA/T. The other resistor pair (*R9* and *R10*) is the resistive load providing a prior current value

for the circular VHD. With the influence of the external magnetic field, the voltage at one Hall contact of the sensor is increased while the other is decreased. Thus, for each 100mT variations of the horizontal magnetic field, the current of the device will be changed as approximate 2.37μA. In other words, the output voltage at one Hall probe contact will be altered by 0.55mV. With the simulation of the equivalent circuit, the diagram (voltage vs. current) is given to obtain the variation of magnetic field which is proportional to the current modification at each Hall probe contact. The property for this device is shown in Figure 4.11. The range of the magnetic field intensity from -600mT to 600mT is amplified linearly.

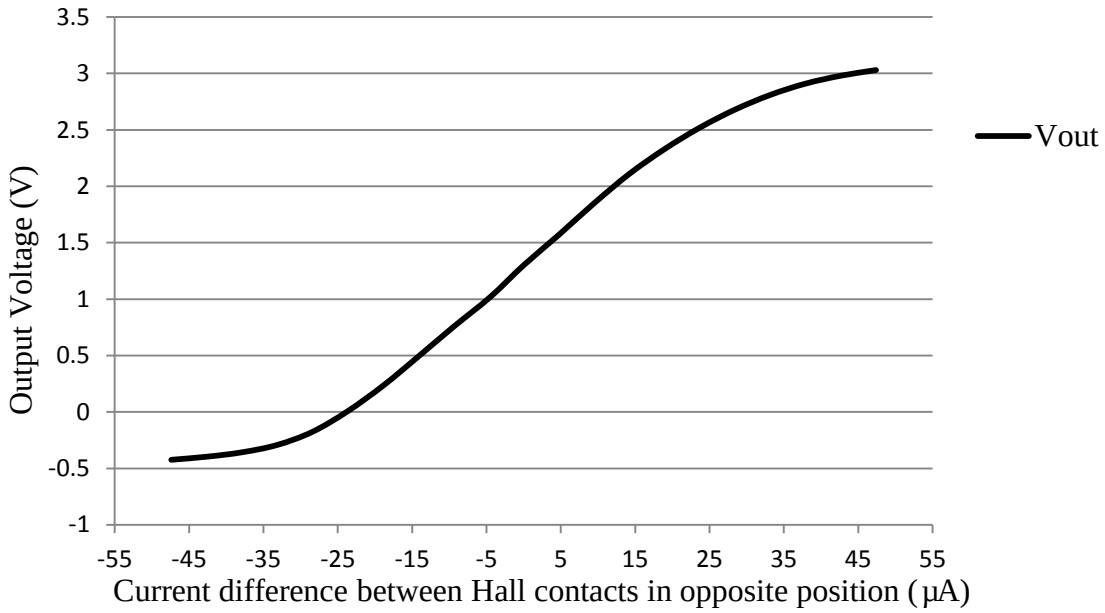

Figure 4.11 The simulation result of the circular VHD connected with the amplifier.

4.3 Summary

In this chapter, two equivalent circuits of the three-dimensional MFS are simulated. The characteristics of each component of the magnetic sensor shown in diagrams are obtained from the simulation in Hspice. The amplifier in telescopic topology is designed in 0.18μm CMOS technology as a gain of 182. Because the voltage or current variation is directly proportional to the variation of the external magnetic field, the output signal was plotted as a function of current change instead of magnetic field variations. The resolution of the three-dimensional MFS (0.43mT) is analyzed according to the mismatch of the MFS due to the fabrication process in 0.18μm CMOS technology. The simulation of the MFS connected with the amplifier is carried out, and the schematic of the circuit is shown in this chapter.

CHAPTER 5

SUMMARY AND CONCLUSIONS

In this thesis, a three-dimensional magnetic field sensor is designed in IBM 0.18μm CMOS Technology by implementing structures of a SD-MAGFET and a circular VHD. The SD-MAGFET is utilized to detect the vertical components of the magnetic field. The gate ratio of the SD-MAGFET is optimized as 8/16 for a high sensitivity. To compress the offset in the magnetic field detection, four SD-MAGFETs are used and connected as a common source structure. Thus, the total area of this structure is 5.8μm by 5.8μm. Then, the circular VHD for horizontal magnetic field detections is designed with eight contacts for both applications of power and Hall probe connections. After deploying the circular VHD along with the SD-MAGFET, the entire area of the three-dimensional MFS is 31.6μm by 31.6μm. The signal conditioning circuit is designed to further amplify the signal generated from the MFS. The layout design of this three-dimensional MFS with signal conditioning circuit was completed in Mentor Graphic IC station.

The simulation of the sensor along with the signal conditioning circuit is conducted to enhance the signal sensitivity of the device. The gain of the amplification circuit is designed as 182 and precise simulation results under external magnetic fields in different values are presented. The sensitivity of the three-dimensional MFS is estimated by using Hspice with the assigned values of Hall factor ($r_H=1$) and geometric coefficient ($G=1$). The sensitivity of the SD-MAGFET was found to be 1.62μA/T^{-1} and the sensitivity of the circular VHD was found to be 23.7μA/T^{-1}. It is demonstrated that this structure of the magnetic field sensor has the advantage of smaller area, less power

consumption, less parasitic capacitance, and higher precision in IBM 0.18μm CMOS technology. The device is further optimized in Hspice simulation to reduce the offset caused by connections of the metal line between the sensor and the amplifiers. The resolution of the three-dimensional MFS is estimated as 0.43mT in detecting the magnetic field. The design is in ready to be sent for fabrication with MOSIS in IBM 0.18μm CMOS technology.

5.1 Future Work

The design of the strong SD-MAGFET was achieved for the magnetic field detection. However, the interconnection can be reconfigured to further enhance the performance of the SD-MAGFET. The right side-drains of all four SD-MAGFETs can be connected together as are left side-drains as shown in Figure 5.1. The signal conditioning circuit also needs to be further optimized for this reconfiguration. This will increase the sensitivity for the vertical magnetic field detection. In addition, the temperature dependence of the device needs to be simulated. Once the fabricated chip arrives, experiments are required to validate the simulation results.

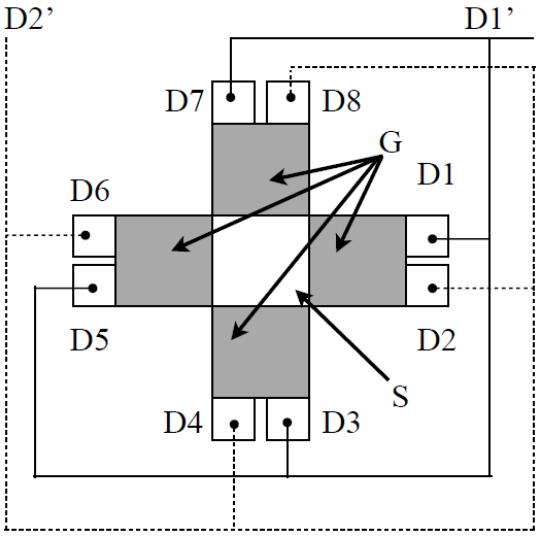

Figure 5.1 Four right side drains and four left side drains are connected separately to increase the performance of the SD-MAGFET.

APPENDIX

THE CODE OF SIMULATION AND THE MODEL FILE

In this chapter, the program used in Hspice for the simulation of SD-MAGET and amplifier is given. The model file of IBM 0.18μm technology is also provided in the appendix.

A.1 Hspice simulation for the SD-MAGAFET

```
VDD2 vdd 0 DC 1.8

VSS2 vss 0 DC -1.8

*----------------------------------------

mp1 1 1 vdd vdd p L=18 W=4

mp2 2 2 vdd vdd p L=18 W=4

*----------------------------------------

mn1 1 gnd n$5 n$5 n L=16 W=4

mn2 2 gnd n$5 n$5 n L=16 W=4

*----------------------------------------

mn3 n$5 n$6 vss vss n L=4 W=4

mn4 n$6 n$6 vss vss n L=4 W=4

*----------------------------------------

IB2 vdd n$6 20UA

.tran 10p 20N

.probe I(m1) I(m2) I(m5)

.end
```

A.2 Hspice simulation for the Amplifier

```
.include model018.m

.option scale=90n

.option post

*----------------------------------------

VDD1 3 0 DC 4.2VOLT

VSS1 4 0 DC -1.8VOLT

*----------------------------------------

M31 31 31 3 3 P L=25 W=50

M41 32 31 3 3 P L=25 W=50

M3 5 5 31 31 P L=25 W=50

M4 6 5 32 32 P L=25 W=50

M1 5 1 8 8 N L=50 W=50

M2 6 2 8 8 N L=50 W=50

M5 8 9 4 4 N L=30 W=100

M6 9 9 4 4 N L=30 w=100

IB1 3 9 100UA

*----------------------------------------

.tran 10p 20N

.probe I(m1) I(m2) I(m5)

.end
```

A.3 The Model File of 0.18μm IBM CMOS Technology

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.24/0.18			
Vth		0.43	-0.40	volts
SHORT	20.0/0.18			
Idss		579	-275	uA/um
Vth		0.48	-0.45	volts
Vpt		5.4	-5.4	volts
WIDE	20.0/0.18			
Ids0		60.8	-75.8	pA/um
LARGE	20.0/20.0			
Vth		0.35	-0.42	volts
Vjbkd		3.4	-4.5	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		155.9	-33.3	uA/V^2
Low-field Mobility		406.34	86.79	cm^2/V*s

PROCESS PARAMETERS	N+BLK	P+BLK	P+PLY	N+	P+	POLY RR	TaN	N_W	UNITS
Sheet Resistance	73.7	110.0	259.3	6.2	5.9	6.1	1458	62	323 ohms/sq
Contact Resistance		6.7	7.3	7.3	6.8				ohms
Gate Oxide Thickness			45						angstrom

PROCESS PARAMETERS	M1	M2	M3	MT	AM	UNITS
Sheet Resistance	0.062	0.088	0.088	0.089	0.0072	ohms/sq
Contact Resistance	2.5	2.2	2.7	0.29		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	D_N_W	N+	P+	POLY	M1	M2	M3	MT	AM	R_W	TaN	N_W	UNITS
Area (substrate)	205	902	1136	125	68	45	32	26	19	54	272		aF/um^2
Area (N+active)			7692										aF/um^2
Area (P+active)			7480										aF/um^2
Area (poly)				183									aF/um^2
Area (metal1)					127								aF/um^2
Area (metal2)						105							aF/um^2
Area (metal3)							31						aF/um^2
Area (MT)								32					aF/um^2

Area (r_well)	1111 878		aF/um^2
Area (NMOS varactor@1V)		7918	aF/um^2
Area (SINGLE-MIM)	2108		aF/um^2

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.78	volts
Vinv	1.5	0.83	volts
Vol	2.0	0.01	volts
Voh	2.0	1.78	volts
Vinv	2.0	0.88	volts
Gain	2.0	-17.69	
Ring Oscillator Freq.			
DIV512 (31-stg,1.8V)		448.34	MHz
D1024_THK (31-stg,2.5V)		252.38	MHz
Ring Oscillator Power			
DIV512 (31-stg,1.8V)		15.70	nW/MHz/gate
D1024_THK (31-stg,2.5V)		33.56	nW/MHz/gate
Operational Amplifier			
Gain	17		

COMMENTS: DEEP_SUBMICRON
V14A SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Jul  7/11
* LOT: V14A                WAF: 1001
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                       LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.5E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3001446
+K1      = 0.5507947    K2      = -0.0344117  K3      = 1E-3
+K3B     = 5.0112244    W0      = 1E-7        NLX     = 1.825596E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.4871475    DVT1    = 0.2479869   DVT2    = -0.1827522
+U0      = 266.0354346  UA      = -1.759866E-9  UB    = 3.148954E-18
+UC      = 6.664844E-11  VSAT   = 1.304081E5   A0     = 1.3488077
+AGS     = 0.3830331    B0      = -2.597671E-8  B1    = 0
+KETA    = -0.015554    A1      = 2.98715E-4  A2      = 0.5265292
+RDSW    = 150          PRWG    = 0.0405456   PRWB    = -0.1818997
+WR      = 1            WINT    = 1.153159E-8  LINT   = 1.703511E-8
+DWG     = 9.161063E-9  DWB     = 1.26734E-8  VOFF    = -0.0933944
+NFACTOR = 1.8355546    CIT     = 0           CDSC    = 2.4E-4
+CDSCD   = 0            CDSCB   = 0           ETA0    = 4.964141E-3
```

```
+ETAB    = -2.552708E-4   DSUB    = 0.0131917      PCLM    = 1.6877156
+PDIBLC1 = 0.2577534      PDIBLC2 = 5.761308E-3    PDIBLCB = -0.1
+DROUT   = 0.7978663      PSCBE1  = 2.506223E9     PSCBE2  = 1.014036E-9
+PVAG    = 0              DELTA   = 0.01           RSH     = 6.2
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 5E-10          CGSO    = 5E-10
+CGBO    = 1E-12          CJ      = 8.133682E-4    PB      = 0.9765652
+MJ      = 0.6000085      CJSW    = 1.653605E-10   PBSW    = 0.8
+MJSW    = 0.1699455      CJSWG   = 3.3E-10        PBSWG   = 0.8
+MJSWG   = 0.1699455      CF      = 0              PVTH0   = -2.395056E-3
+PRDSW   = 10.3498556     PK2     = 3.578424E-3    WKETA   = -6.078751E-5
+LKETA   = -5.361768E-4   PU0     = -4.6536932     PUA     = -5E-11
+PUB     = 1.236981E-24   PVSAT   = 1.087513E3     PETA0   = -2.841206E-5
+PKETA   = -2.594654E-3   )
*
.MODEL CMOSP PMOS (                              LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.5E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.4108634
+K1      = 0.5963806      K2      = -2.489931E-7   K3      = 0.077543
+K3B     = 19.6581293     W0      = 1E-6           NLX     = 3.12928E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.8563605      DVT1    = 0.674473       DVT2    = -0.3
+U0      = 116.5366039    UA      = 1.500119E-9    UB      = 1.078426E-21
+UC      = -1E-10         VSAT    = 1.76479E5      A0      = 1.0736456
+AGS     = 0.2043189      B0      = 1.236798E-6    B1      = 5E-6
+KETA    = 0.0230788      A1      = 7.45017E-4     A2      = 0.5500838
+RDSW    = 840.1647863    PRWG    = -0.2036656     PRWB    = -0.3692108
+WR      = 1              WINT    = 0              LINT    = 2.875806E-8
+DWG     = -2.295436E-8   DWB     = -1.029527E-8   VOFF    = -0.15
+NFACTOR = 0.8049188      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0    = 1.383466E-3
+ETAB    = -1.706135E-3   DSUB    = 4.29054E-3     PCLM    = 0.9980121
+PDIBLC1 = 0.0661906      PDIBLC2 = 1.019358E-3    PDIBLCB = -1E-3
+DROUT   = 0.9525903      PSCBE1  = 9.098741E9     PSCBE2  = 7.928343E-10
+PVAG    = 0.0541244      DELTA   = 0.01           RSH     = 5.9
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
```

```
+LL      = 0            LLN     = 1            LW      = 0
+LWN     = 1            LWL     = 0            CAPMOD  = 2
+XPART   = 0.5          CGDO    = 5E-10        CGSO    = 5E-10
+CGBO    = 1E-12        CJ      = 1.165977E-3  PB      = 0.8214639
+MJ      = 0.4256548    CJSW    = 1.220056E-10 PBSW    = 0.8008
+MJSW    = 0.1001       CJSWG   = 4.22E-10     PBSWG   = 0.8008
+MJSWG   = 0.1001       CF      = 0            PVTH0   = 4.9818E-4
+PRDSW   = -5           PK2     = 2.789944E-4  WKETA   = 0.0336784
+LKETA   = -7.448263E-3 PU0     = 5.8837793    PUA     = 3.022234E-10
+PUB     = 7.126168E-25 PVSAT   = 50           PETA0   = 5.4464E-5
+PKETA   = -5.567331E-3 )
*
```

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