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Investigation of a New Analog-to-digital Conversion Technique

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INVESTIGATION OF A NEW

ANALOG-TO-DIGITAL CONVERSION TECHNIQUE

BY

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INVESTIGATION OF A NEW

ANALOG-TO-DIGITAL CONVERSION TECHNIQUE

This thesis is approved as a creditable and independent investigation by a candidate for the degree, Master of Science, and is acceptable as meeting the thesis requirements for this degree, but without implying that the conclusions reached by the candidate are necessarily the conclusions of the major department.

Thesis Advisor / Date

Head, Electrical Engineering Department / Date

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CHAPTER I

INTRODUCTION

In the past decade, significant progress has been made in the technology of digital electronic systems. These are systems in which information is represented by numbers, usually in the form of groups of binary digits. These systems were developed for the purpose of processing information. Devices, which fit into this category, are digital computers and digital control systems. In order to utilize these devices, information must be taken from nature and presented to the digital device in a form it can understand. Previously, man had to act as an encoder to link the information into the digital machine. Physical sensors changed a quantity (such as temperature or pressure) into a decimal number which was understandable to man. Man coded this information into digital form so that the machine could operate on this information. This was a very slow and expensive process, where the machine received the information long after the actual physical occurrence. To alleviate this problem, physical sensors have been made which convert the physical information into an analog signal, such as a voltage variation. The magnitude of this analog signal gives the value of the physical quantity as a function of time. An encoder is needed which converts the analog signal into a digital representation. A device which preforms this function is called an analog-to-digital (A/D) converter.

A. Definition of Terms

The nature of a digital signal dictates that the conversion of an analog signal to a corresponding digital number can only be an approximation, for the analog signal can take on an infinite number of values, whereas the digital number is limited to a finite number of digits. The approximating process is called quantization and the number of discrete digits used in a digital representation are called quantization levels. Figure 1-1 shows an ideal A/D conversion characteristic as a dotted line and the quantization uncertainty which is the result of practical conversion devices. Quantization uncertainty is defined as the fraction of the analog input quantity (A_u/A_q) which may result in the same output level. This and other factors lead to a total converter error which is the maximum difference between the true input value for a given output level and the actual maximum or minimum input value that may produce the same output level.[1]

Some of the more important terms that express the speed of the A/D conversion process are maximum allowable input signal slewing rate, conversion time, conversion rate, and aperture. Maximum allowable slewing rate is the maximum change in input signal magnitude per unit time before the conversion process will commit an error.[1] Generally, conversion time is the interval between the time an A/D converter input reaches a final value and the time the output settles to a within-tolerance representation of that value. Conversion rate is a measure of the frequency at which conversions can be made. Aperture or aperture time is the uncertainty of the exact time the A/D

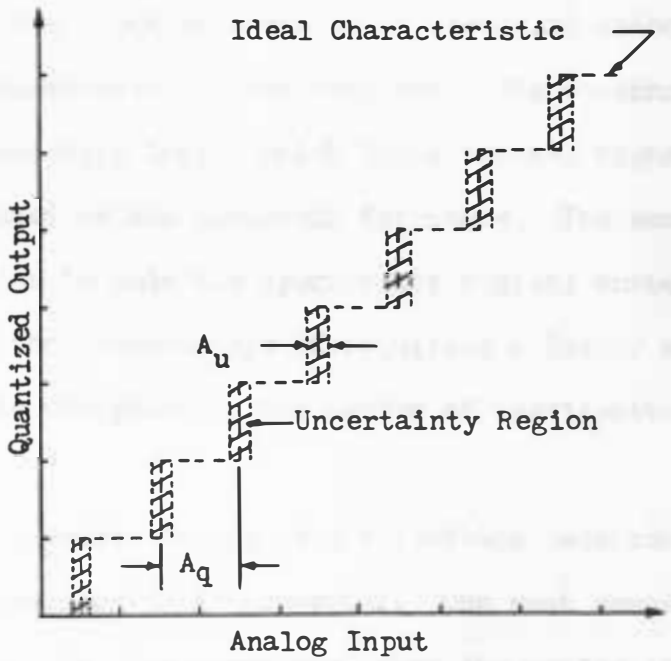


Figure 1-1. Quantization Characteristic of an A/D Converter

converter input was at the value represented by a given output code.[2]

B. Types of A/D Converters

Many types of A/D converters have been made which operate on several different principles. The following is intended as a brief introduction to some of the more popular techniques in A/D conversion.

Parallel A/D converters, also called simultaneous converters, are some of the faster types of A/D converters. The analog input voltage appears at the input to a number of threshold detectors equal to the number of quantization levels required. The threshold detector outputs drive the encoding logic, which looks for the highest reference exceeded, as indicated by the threshold detectors. The encoding logic uses this information to code the appropriate digital number. This technique has the disadvantage of requiring a larger and larger amount of electronic equipment as the number of quantization levels is increased.[3]

Several A/D converters incorporate a feedback path containing a parallel digital-to-analog (D/A) converter. One such converter is the servo A/D converter. In this converter, when the analog input voltage changes there is a difference between the feedback voltage and the input voltage. This difference voltage is called an error voltage and it is used to increment the digital representation in a direction to drive the error voltage to zero. The four basic circuit functions required in this type of a converter are summation, threshold function, up-down counting, and D/A conversion.[4]

Another type, which uses the parallel feedback technique, is the

successive-approximation A/D converter. This type of converter is one of the most popular types. In a successive-approximation A/D converter, a feedback voltage is made to approximate the input voltage in a sequence of successive steps. In each step, the feedback voltage is changed in accordance with the result of the previous comparison between the input and feedback voltages. This type of operation repeatedly divides the voltage range in half. Thus, the system first tries half scale. Next, it tries either quarter scale or three-fourths scale depending on whether the first approximation was too large or too small, respectively. Three such approximations would result in a 3-bit digital number. The circuits necessary to implement this type of converter are summing and threshold circuits, a timing generator, sequence control and storage circuits, a D/A converter, and output logic gates.[4]

Certain types of A/D converters have a counter as their main component. In the counter ramp A/D converter, the conversion process is started by a reset command resetting the counter. Following this command, clock pulses are counted by the counter and a D/A converter is used to create an equivalent analog voltage. As the count increases, the analog voltage from the D/A converter increases with time in a staircase manner until the staircase ramp voltage is equal to, or slightly greater than, the analog input signal. At this point, the comparator sends a signal stopping the counter. The digital number in the counter is then proportional to the analog input signal.[3]

An open loop counting type A/D converter is the analog-to-frequency converter. The analog-to-frequency converter converts the analog signal

into a variable frequency pulse signal. This variable frequency pulse signal is counted for a fixed time to give a digital representation of the analog input.[2]

Table 1-1 gives a comparison of the basic A/D conversion techniques that have just been discussed. The mode of operation of the A/D converters will be either multiplexed or continuous. In the multiplex mode, the converter is programmed to accept a source input and give its digital representation. It then resets and is ready to receive an input from another source. In the continuous mode, the converter continually follows changes in the analog input allowing digital readout at an extremely rapid rate. Some converters are suitable for operation in either of the above modes.

In Table 1-1, the cost column uses low, medium, and high as relative cost figures. Low would correspond to approximately $1,000, medium to $2,000, and high to $3,000 or greater. Cost will increase as more quantization levels are added and as speed and accuracy are increased.

C. Purpose of Thesis

It is the purpose of this investigation to theoretically and experimentally study yet another method of analog-to-digital conversion. The goals of low cost and flexibility of operation will be investigated. Because A/D converters are integral parts of digital control, telemetering, and simulation or measuring systems, system designers would benefit greatly if a low cost and versatile A/D converter was available.

Method	Most Suitable Operating Mode Multiplexed (M) Continuous (C)	Conversion Time 5 Bits (μsec)	Aperture Time 5 Bits (μsec)	Constant Time of Aperture?	Relative Cost
Simultaneous	M or C	Not Applicable		Yes	Medium to High
Servo	C	1.5	1.5	Yes	Low to Medium
Successive Approximation	M	7.5	7.5	Yes	Medium
Counter Ramp	M	16 Average	1	No	Low to Medium
Analog-to-Frequency	M	16 Average	1	Yes	Low to Medium

Table 1-1. Comparison of A/D Conversion Techniques.[5]

Digital techniques could be introduced in new areas, where they are not used at present, if low cost analog-to-digital converters were available. Two of these areas may be, receipt of information from remote land weather stations and physiological data acquisition.

To complete the above purpose, Chapter II is devoted to developing the principles used by the proposed technique, Chapter III describes possible circuits for implementing the proposed technique and a theoretical evaluation of the expected performance, and Chapter IV contains a discussion of the actual circuits used and the results of converting two typical analog signals. Chapter V contains the conclusions obtained from this study.

CHAPTER II

DEVELOPMENT OF THE TECHNIQUE

The main purpose of the analog-to-digital converters discussed in Chapter I is to quantize a given analog signal into the nearest digital quantization level. Some of the methods convert directly into a digital representation by comparison of the input with a feedback signal while others convert the analog signal into an intermediate form, such as pulse width or frequency. These intermediate forms are operated upon to yield a digital representation of the analog signal.

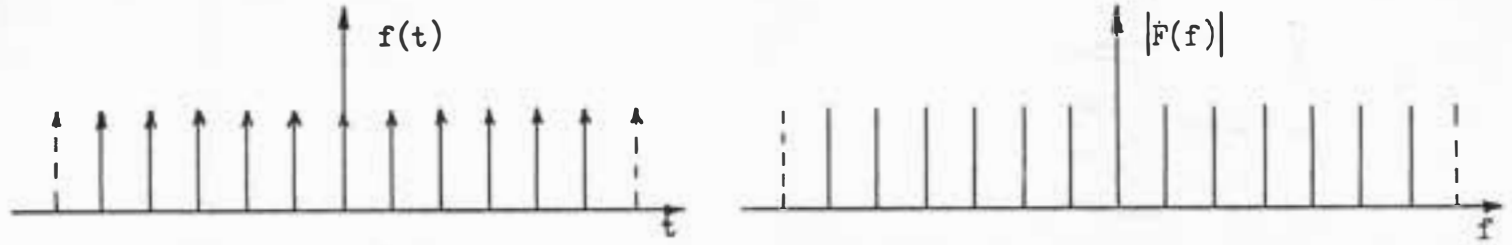
It appears that none of the current methods use frequency domain techniques to arrive at analog-to-digital conversion. Frequency techniques are becoming very popular because of the widespread knowledge of Fourier analysis and use of the spectrum analyzer. In the proposed technique, the analog signal is converted into a varying frequency sinusoid and then an appropriate time domain operation causes this signal to be quantized in the frequency domain. This differs from the analog-to-frequency technique discussed in Chapter I where the analog signal is converted into a variable frequency pulse signal. Since different operations in the time domain have varying effects in the frequency domain, an optimal time domain operation is required to produce a signal with a useable frequency spectrum. Several time waveforms and their corresponding frequency spectrums are considered in the paragraphs that follow.

A. Representative Frequency Spectra

A train of impulses in the time domain produces an optimum frequency spectrum but is physically impossible to implement. Figure 2-1 shows the time waveform and its corresponding harmonic content.[6, 7] A continuous recurrence of a triangular shaped pulse produces a series of harmonics in a $(\sin^2 x)/x^2$ amplitude configuration as shown in Figure 2-2.[7] This has the disadvantage of difficult detection of the sideband harmonics due to the rapid decrease in amplitude. The time domain operation is possible but not as readily implemented as a series of rectangular pulses which produce a $(\sin x)/x$ distribution of harmonics as seen from the development that follows. Similar developments have been made by others, but this development is included here to introduce necessary terminology and because it leads directly into a relationship involving the number of quantization levels.[6, 7, 8]

B. Frequency Spectrum of Pulsed-RF Train

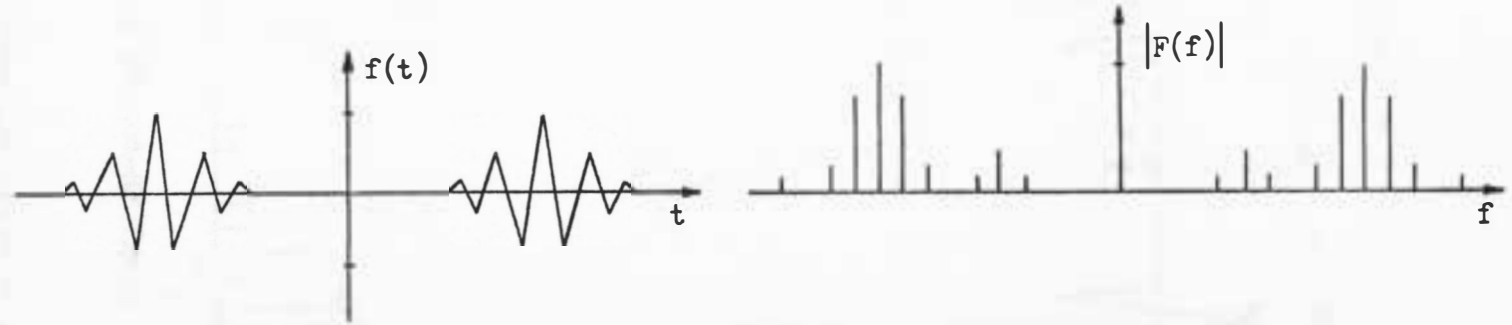
Figure 2-3a shows a continuous train of pulses of a cosine wave of constant angular frequency, W_c. In the remainder of this thesis, this will be referred to as a pulsed-RF train. Later, the effects of varying the angular frequency (W_c) will be evaluated, but for the present derivation W_c will be assumed constant. In Chapter III, the effects of this assumption will be evaluated. The pulse repetition frequency (f_o) is related to the period (T) and the angular repetition frequency (W_o) by equation 2-1.



(a) Impulse Train

(b) Frequency Spectrum of Impulse Train

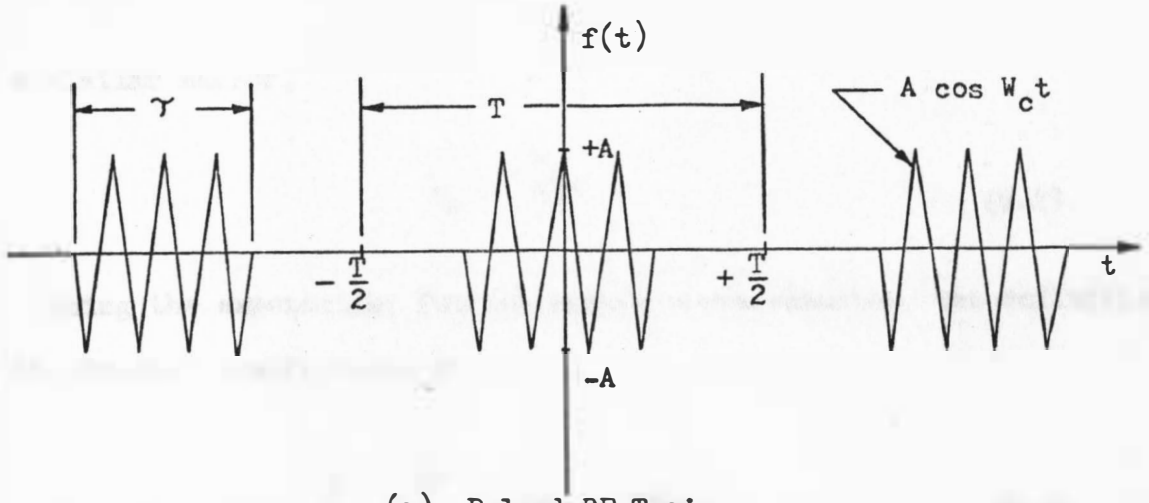
Figure 2-1. Time and Frequency Domain Representation of an Impulse Train



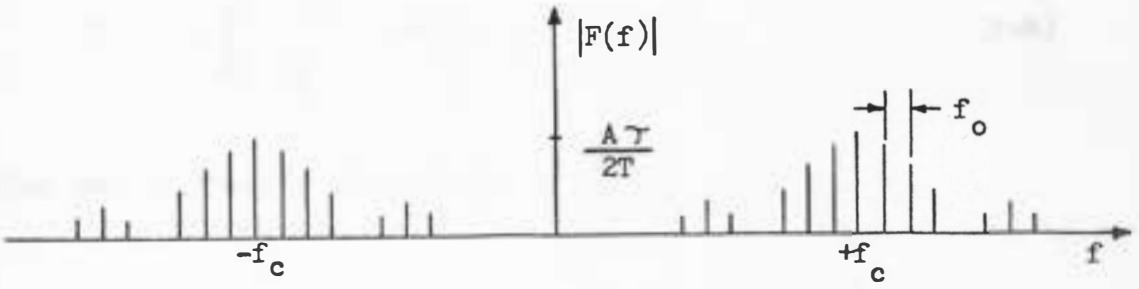
(a) Triangular Pulse Train

(b) Frequency Spectrum of a Triangular Pulse Train

Figure 2-2. Time and Frequency Domain Representation of a Triangular Pulse Train



(a) Pulsed-RF Train



(b) Frequency Spectrum of Pulsed-RF Train

Figure 2-3. Time and Frequency Domain Representation of a Pulsed-RF Train

$$f_o = \frac{1}{T} = \frac{W_o}{2\pi} \quad . \tag{2-1}$$

In a similar manner,

$$f_c = \frac{W_c}{2\pi} \quad . \tag{2-2}$$

Using the exponential Fourier series representation, the definition of the Fourier coefficients gives:

$$F_n = \frac{1}{T} \int_{-\frac{T}{2}}^{+\frac{T}{2}} f(t)\, e^{-jnW_o t}\, dt \quad . \tag{2-3}$$

Substituting for f(t) as shown in Figure 2-3a, with f(t) = 0, between $-\frac{T}{2} \leq t < -\frac{\tau}{2}$ and $+\frac{\tau}{2} < t \leq \frac{+T}{2}$ and with T and τ as defined in the figure, equation 2-3 becomes:

$$F_n = \frac{A}{T} \int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} \cos W_c t\, e^{-jnW_o t}\, dt \quad . \tag{2-4}$$

Making use of Euler's identity for $e^{-jnW_o t}$,

$$F_n = \frac{A}{T} \int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} \cos W_c t \left[\cos nW_o t - j \sin nW_o t\right] dt \quad . \tag{2-5}$$

By expanding,

$$F_n = \frac{A}{T}\int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} \cos W_c t \cos nW_o t \, dt - j\frac{A}{T}\int_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} \cos W_c t \sin nW_o t \, dt \, . \qquad (2\text{-}6)$$

Using standard integral tables, the second term becomes zero and the first term can be expressed as

$$F_n = \frac{A}{T}\left[\frac{\sin(W_c-nW_o)t}{2(W_c-nW_o)} + \frac{\sin(W_c+nW_o)t}{2(W_c+nW_o)}\right]_{-\frac{\tau}{2}}^{+\frac{\tau}{2}} \, . \qquad (2\text{-}7)$$

Substituting the limits of integration,

$$F_n = \frac{A}{T}\left[\frac{\sin(W_c-nW_o)\frac{\tau}{2}}{(W_c-nW_o)} + \frac{\sin(W_c+nW_o)\frac{\tau}{2}}{(W_c+nW_o)}\right] \, . \qquad (2\text{-}8)$$

Multiplying and dividing by $\frac{\tau}{2}$ gives the result in the (sin x)/x configuration.

$$F_n = \frac{A\tau}{2T}\left[\frac{\sin(W_c-nW_o)\frac{\tau}{2}}{(W_c-nW_o)\frac{\tau}{2}} + \frac{\sin(W_c+nW_o)\frac{\tau}{2}}{(W_c+nW_o)\frac{\tau}{2}}\right] \, . \qquad (2\text{-}9)$$

Equation 2-9 can be modified by substitution from Equations 2-1 and 2-2 to yield:

$$F_n = \frac{A\tau}{2T}\left[\frac{\sin\pi\tau(f_c-nf_o)}{(f_c-nf_o)} + \frac{\sin\pi\tau(f_c+nf_o)}{(f_c+nf_o)}\right] \, . \qquad (2\text{-}10)$$

Equation 2-10 gives the distribution and amplitude of the harmonics which compose the original waveform shown on Figure 2-3a. Figure 2-3b shows a representative harmonic distribution where $\frac{\tau}{T} = \frac{1}{4}$. Since T is related to f_o by Equation 2-1, changing T varies the spacing between adjacent harmonics. Changing τ varies the intercept points of the envelope, while changing the ratio, $\frac{\tau}{T}$, varies the number of harmonics in the major and all other lobes. This information is useful in evaluating the qualifications of a frequency spectrum which can be used in this technique. To have value in quantizing a signal, the harmonics in the harmonic distribution should be equally spaced. The condition of equal spacing is satisfied by the harmonics in the major lobe. These harmonics must be as numerous as the number of quantization levels required and for ease of detection their amplitudes must be above a certain minimum value.

C. Quantization Level Prediction

By referring to Equation 2-10 and Figure 2-3b, the number of harmonics in the major lobe can be ascertained. If the segment of the harmonic distribution from $+f_c$ extending to the left to the first cross over point is considered, only the first term in Equation 2-10 need be considered. Equation 2-10 reduces to

$$F_n = \frac{A\tau}{2T} \left[\frac{\sin \pi\tau(f_c - nf_o)}{\pi\tau(f_c - nf_o)} \right] \qquad (2\text{-}11)$$

For $\pi\tau(f_c-nf_o) = 0$, $\frac{A\tau}{2T}\left[\frac{\sin 0}{0}\right] = \frac{A\tau}{2T}$ and the center of the distribution occurs when $(f_c-nf_o) = 0$; thus, $n = \frac{f_c}{f_o}$. The first cross over point will occur when $F_n = 0$. This occurs when $\tau(f_c-n_1f_o) = 1$. This expression can be solved for n_1 to yield:

$$n_1 = \frac{\tau f_c - 1}{\tau f_o} \quad . \tag{2-12}$$

The number of harmonics between the center and the crossover point (h) will be

$$h = n - n_1 \quad . \tag{2-13}$$

Upon substitution for n and n_1,

$$h = \frac{1}{f_o} \quad . \tag{2-14}$$

Substitution for f_o from Equation 2-1 yields:

$$h = \frac{T}{\tau} \quad . \tag{2-15}$$

Because of symmetry, the total number of harmonics in the major lobe will be 2h-1. The one is subtracted because the center harmonic was counted twice in the 2h factor. If the number of quantization levels (q) is defined as the number of harmonics in the major lobe, then upon substitution from Equation 2-15 for h,

$$q = 2\frac{T}{\tau} - 1 \quad . \tag{2-16}$$

D. Explanation of the Technique

In the above derivation, it was assumed that f_c was constant. This would be the case only for a non-time varying signal. In general the analog input will be time varying and if a linear analog-to-frequency conversion is made, f_c will be time varying. Therefore, the complete harmonic distribution will be moving up or down the frequency scale depending on the value of f_c. It now becomes apparent that if a narrow bandpass filter were placed at a certain frequency, f_b, then as f_c varied, the discrete harmonic frequencies in the distribution would move through the filter bandwidth centered at f_b, and the filter would have an output as each harmonic passes through its passband. This output could then be detected and used as quantization information in the analog-to-digital process.

The quantization technique just described gives only quantizing information and does not give information as to whether f_c is increasing or decreasing. This information can be obtained directly from the slope of the analog signal. A slope detector would give the additional information needed in the analog-to-digital process.

The slope and quantization information must be coupled in such a way that they provide the necessary digital readout information for later reconstruction of the analog signal. A device, which would provide the necessary coupling, would have to digitally increment up on the positive slope of the analog signal and digitally increment down on the negative slope of the analog signal. This assumes that the analog-to-frequency conversion is linear with a positive slope.

A digital up-down counter would provide the coupling described above. Binary readout information would be available from the counter. Figure 2-4 shows a complete block diagram of the proposed analog-to-digital conversion technique.

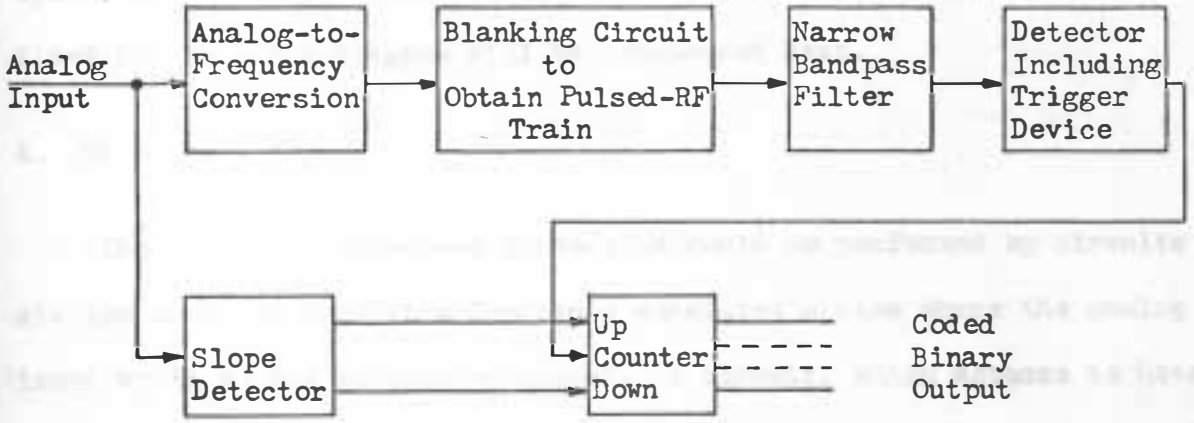


Figure 2-4. Block Diagram of Proposed A/D Conversion Technique

CHAPTER III

DEFINING THE SYSTEM

In Chapter II the proposed technique of analog-to-digital conversion was explained. Figure 2-4 shows a block diagram of the system as proposed. Possible circuits to perform the functions outlined on the block diagram will be considered next.

A. Circuits

The analog-to-frequency conversion could be performed by circuits similar to those used in a frequency modulated system where the analog input would be the modulating signal. A circuit, which appears to have certain characteristics useful for this system, is a voltage controlled oscillator, hereafter referred to as a VCO. VCO's have been built, which operate in the frequency range from a few hertz to hundreds of megahertz, with a control ratio of maximum frequency to minimum frequency as high as 20 to 1 for some units. Input control voltages may be as high as 30 volts.[10, 11, 12, 13, 14] Certain types of VCO's may even be producible in an integrated circuit form.[14] This flexibility of operation and the possibility of integrated circuit production are reasons why a VCO was chosen for the analog-to-frequency conversion in this technique.

After the analog input has been converted to a variable frequency sinusoid, this signal must be operated upon to form a pulsed-RF train. Circuits which will perform this function are amplitude modulators,

sampling gates, or chopper type configurations. Certain of the above types have the disadvantages of D-C offsets in the blanked portion of the waveform, switching transients, or transformer coupling at the input and output. A circuit which does not have these disadvantages is a chopper made from two diode transistor logic (DTL) NAND gates and some external components.[15] This circuit, when driven by a square wave with the proper value of repetition rate (f_o) and pulse width (τ), will produce a waveform similar to that shown in Figure 2-3a.

The filter used to detect the harmonics must be narrow in bandwidth compared to f_o, because f_o determines the spacing between adjacent harmonics. The quantization process, to be exact, requires a narrow bandpass filter such as a monolithic crystal filter, a crystal filter, or a mechanical filter. An LC filter would be too bulky and its bandwidth would not be sufficiently narrow. Figure 3-1 shows the availability of the above types for different center frequencies (f_b) and possible bandwidths defined as percent of f_b. Other parameters of the system must be investigated before the final filter selection can be made.

In the block diagram (Figure 2-4), the filter is followed by a detector and trigger circuit. The detector must detect the presence of a filter output, then the trigger must send a command to the up-down counter's count terminal. An envelope detector followed by a Schmitt trigger appears to satisfy the above requirements.

To this point, circuits have been suggested which fill the requirements of the quantizing portion of the proposed analog-to-digital

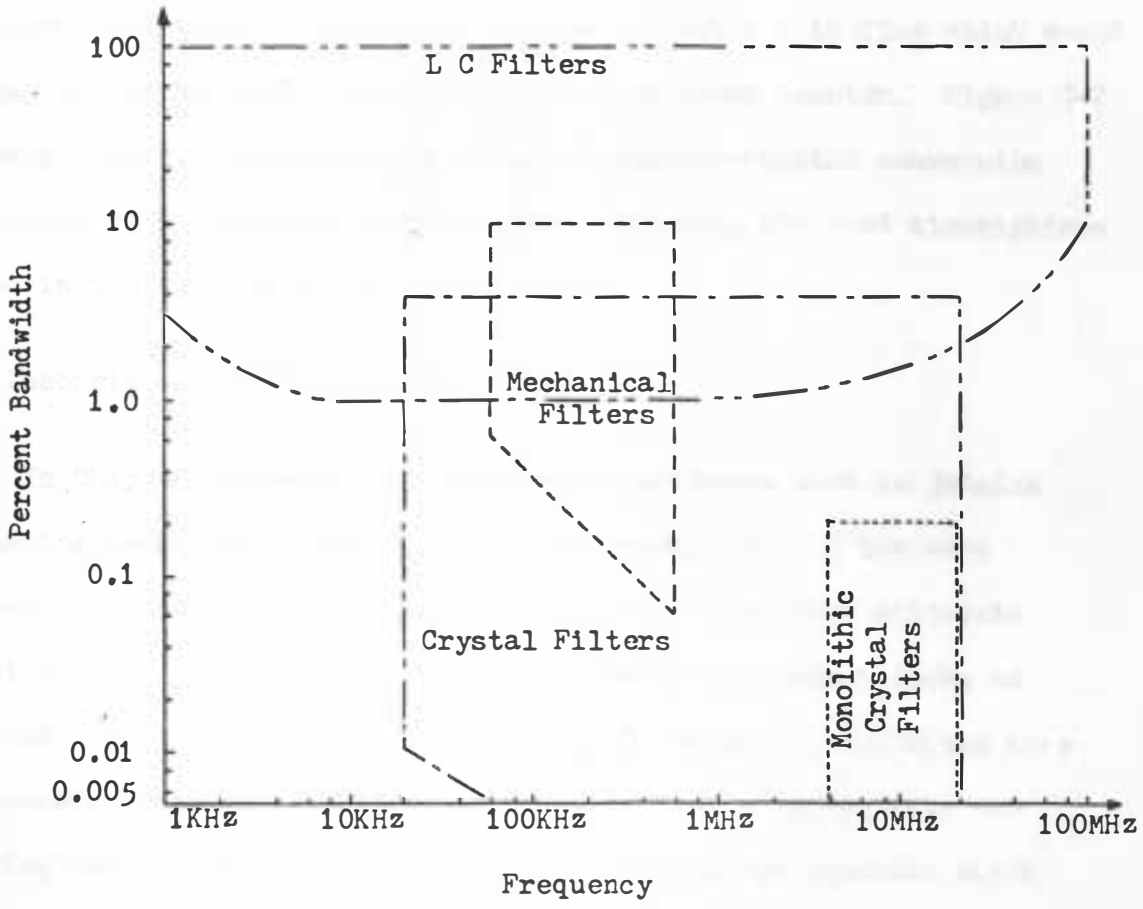


Figure 3-1. Availability of Filters by Type.[16]

technique. The slope information, as suggested previously, may be obtained directly from the analog input by a slope detection circuit. A direct method of obtaining this information would be to differentiate the analog input and follow this by a voltage level detector. The voltage level detector would be required to set a flip-flop which would supply the up and down information to the up-down counter. Figure 3-2 shows a complete block diagram of the analog-to-digital conversion technique with suggested circuit types replacing the word discriptions shown in the block diagram of Figure 2-4.

B. Theoretical Performance Evaluation

In Chapter I some of the performance criteria used in judging an analog-to-digital converter were discussed. One of the more important dynamic factors discussed was that of maximum allowable input slewing rate. Previously in this chapter, circuit forms to perform the basic functions of this analog-to-digital technique were suggested. From this information, it is possible to evaluate the slewing rate of this new technique. In deriving an equation which relates the input voltage to other parameters of the system, certain assumptions as to the speed of operation of various component functions must be made. The slowest functional component will constrain the slewing rate to a maximum value. From analysis of the circuits outlined in Figure 3-2, it appears that four functional blocks may impose an upper limit on slewing rate. The first is the VCO. If the rate at which the VCO can change frequency is the limiting factor, then the

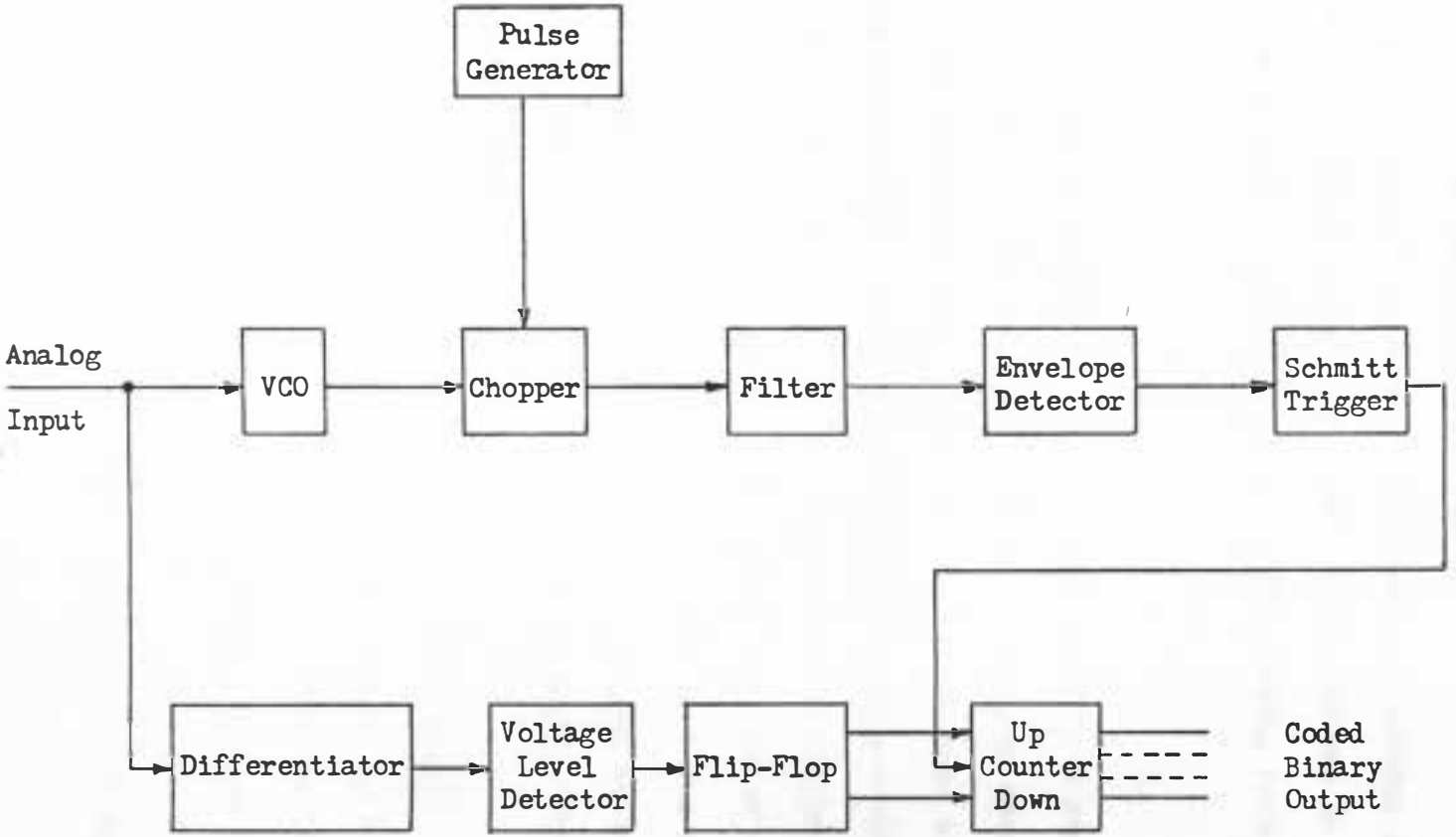


Figure 3-2. Circuit Block Diagram

slewing rate of the system will correspond to the modulation rate of the VCO. If this turns out to be incorrect, the second area of speed reduction could be the response of the filter.

If the filtering process is assumed to be the limiting component, then the relation between output and input of the VCO can be stated as given in Equation 3-1 for all possible input slewing rates.

$$f_c = KV_i \qquad (3\text{-}1)$$

V_i is the amplitude of the analog input signal and K is a conversion factor which depends on the specific VCO used. As f_c is caused to vary due to the analog input, the harmonics of the chopped waveform pass through the passband of the filter and are detected. Since a physically realizable filter cannot be made which can filter one single frequency, a bandwidth of B hertz will be associated with any filter chosen. If the filter is assumed to be the limiting component, a relationship between the maximum slewing rate and the filter parameters of bandwidth (B) and center frequency (f_b) should exist. This relationship is developed in the next section.

In order for the filter to produce a detectable output, the harmonic that is passing through the filter must remain in the filter bandwidth for a minimum time (t_B). If a criterion that at least m cycles of signal in the bandwidth of the filter be required for positive filtering and detection, then t_B will be the time related to m cycles of f_b, since f_b is the average frequency of the signal as it sweeps by the filter. Thus,

$$t_B = \frac{m}{f_b} \cdot \qquad (3\text{-}2)$$

The maximum change in frequency per unit time, $(\frac{\Delta f_c}{\Delta t})_{max}$, for a signal in the filter bandwidth can be related to B and t_B as shown in Equation 3-3.

$$(\frac{\Delta f_c}{\Delta t})_{max} = \frac{B}{t_B} \qquad (3\text{-}3)$$

If the rate of change of frequency with time were higher than this, the harmonic would pass through the filter bandwidth in less time than t_B, the minimum time required. In order that proper quantization occur, this condition cannot exist. In passing from one level to the next, f_c must change by an amount equal to f_o, because f_o is the difference in frequency between adjacent harmonics. The minimum time between levels (t_L) is then

$$t_L = \frac{f_o}{\left(\frac{\Delta f_c}{\Delta t}\right)_{max}} \qquad (3\text{-}4)$$

which upon substitution from Equations 3-3 and 3-2 becomes:

$$t_L = \frac{f_o m}{B f_b} \qquad (3\text{-}5)$$

The maximum number of levels per second (L_s) will be

$$L_s = \frac{1}{t_L} \qquad (3\text{-}6)$$

and upon substitution from Equation 3-5

$$L_s = \frac{Bf_b}{f_o m} \tag{3-7}$$

Equation 3-1 may be modified by expression V_i and f_c in rate of change forms as

$$\frac{\Delta f_c}{\Delta t} = K\left(\frac{\Delta V_i}{\Delta t}\right) \tag{3-8}$$

where $\frac{\Delta V_i}{\Delta t}$ is the analog input slewing rate. The maximum slewing rate can be expressed as

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{1}{K}\left(\frac{\Delta f_c}{\Delta t}\right)_{max} \tag{3-9}$$

which upon substitution from Equations 3-3 and 3-2 becomes:

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{Bf_b}{Km} \tag{3-10}$$

If q quantization levels are required and the analog input has a maximum range of V volts, then the VCO will be required to have a maximum frequency deviation (Δf_c) of qf_o. K can be expressed as

$$K = \frac{qf_o}{V} = \frac{\Delta f_c}{V} \tag{3-11}$$

Equation 3-10 can then be written as

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{VBf_b}{qf_o m} \tag{3-12}$$

The same result can be obtained by multiplying the maximum number of

levels per second (L_s), as obtained in Equation 3-7, by the number of volts per level. The number of volts per level will be the maximum change in voltage (V) divided by the number of quantization levels (q).

To insure that signals with different rates of change be quantized properly, B must be smaller than f_o. This may be stated quantitatively as

$$B = pf_o \tag{3-13}$$

where p is a fraction. Equation 3-12 may be altered by substitution for B from Equation 3-13 to yield:

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{Vpf_b}{mq} \tag{3-14}$$

Equation 3-14 is valid under the assumption that a filter with center frequency f_b can be made with bandwidth, $B = pf_o$, and that the filter is the speed limiting component in the system.

A third possible speed limiting component, which requires analysis, is the up-down counter. Depending on the construction of the counter, it will have a minimum time (t_1) required between successive count commands. This leads to a maximum counting rate of $1/t_1$. Since a count occurs for each quantization level, the maximum number of levels per unit time will also be equal to $1/t_1$. An expression for the maximum slewing rate is

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{V}{t_1 q} \tag{3-15}$$

where V/q is the number of volts per level. Equation 3-15 is valid under the assumption that all other components will function properly up to and including the maximum slewing rate computed from Equation 3-15.

A fourth possible speed limiting factor is associated with an assumption made in Chapter II. At the beginning of the development for finding the frequency spectrum of the pulsed-RF train, it was assumed that the frequency of the VCO was constant. The results of that development showed that the frequency spectrum was a line spectrum with a (sin x)/x magnitude envelope with the harmonics separated by a difference in frequency of f_o. The next question to be determined is: at what input signal slew rate, which results in a frequency slewing rate at the VCO output, does the frequency spectrum of the pulsed-RF train become altered significantly and therefore cause improper operation of the analog-to-digital converter? In order to answer this question, a different approach from that of Chapter II must be considered. Consider the pulsed-RF train as a product of two time functions. This product in the time domain suggests a composite frequency spectrum which is the convolution of two separate spectra.[7] The shape of the spectrum of the rectangular signal will not change as f_c changes, but the spectrum of the RF wave will change. As f_c varies, the spectrum of the RF wave will change to that of a frequency modulated carrier. It has been shown for a modulating signal, $\frac{V}{2} \cos W_m t$, and a carrier, $A \cos W_c t$, that the representation of the composite frequency modulated signal can be expressed as given in

Equation 3-16.

$$f_{FM}(t) = A\Big[J_o(m_f)\cos W_c t + J_1(m_f)\left\{\cos (W_c+W_m t)-\cos (W_c-W_m)t\right\} + J_2(m_f)\left\{\cos (W_c + 2W_m)t + \cos (W_c-2W_m)t\right\} + J_3(m_f)\left\{\cos (W_c + 3W_m)t-\cos (W_c-3W_m)t\right\} + \ldots + \ldots\Big] \quad .^7 \tag{3-16}$$

The $J_n(m_f)$ are Bessel functions of the first kind and m_f is called the modulation index. m_f is defined as,

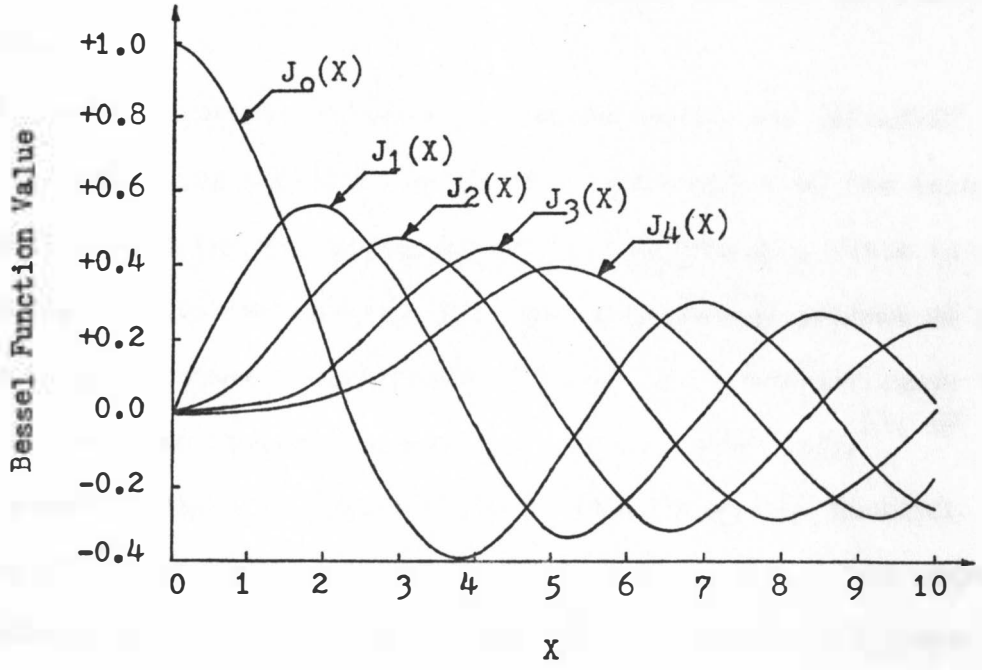
$$m_f = \frac{\Delta W}{W_m} \tag{3-17}$$

where ΔW is the change in angular frequency of the VCO. ΔW may be related to V and K or q and f_o by referring to Equation 3-11. Thus, Equation 3-17 becomes:

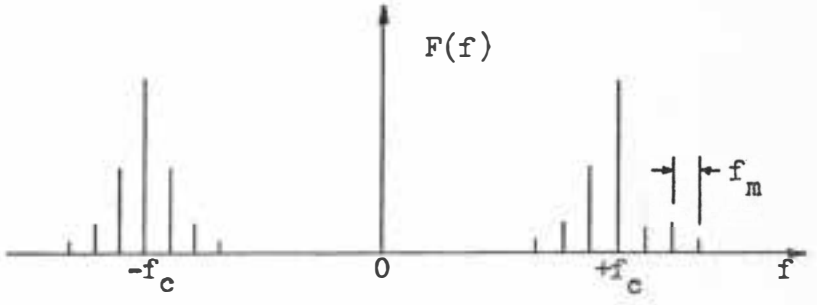
$$m_f = \frac{\pi 2 \Delta f}{W_m} = \frac{2\pi VK}{W_m} = \frac{VK}{f_m} = \frac{qf_o}{f_m} \tag{3-18}$$

where $W_m = 2\pi f_m$ and $VK = qf_o = \Delta f$. Figure 3-3 shows a plot of the Bessel functions and the frequency spectrum of a frequency modulated wave with $f_m = 5$ KHz and $m_f = 1.0$.[7]

In general, the analog signal will be a varying frequency signal and f_m and m_f will not be constant over any extended time period. The undesirable sidebands associated with the frequency modulated carrier cannot be easily predicted for a random analog input. Since these sidebands will interfere with the analog-to-digital process, an area of operation must be chosen where their amplitude is such that they do



(a) Bessel Function of the First Kind



(b) FM Carrier Spectrum

Figure 3-3. Bessel Function Plot and FM Carrier Spectrum

not affect the process. From Figure 3-3a, it appears that for $m_f < 0.8$ the largest sideband amplitude will be at least half of the fundamental's amplitude.

If the FM signal is pulse modulated to obtain the pulsed-RF train, the resulting spectrum should be a convolution of the (sin x)/x distribution with the FM carrier spectrum. In practice, this is not the result. Due to the carrier shifting in frequency because of the pulse modulation process (incidental FM) and the non-ideal shape of the FM pulses, the frequency spectrum is not as predicted.[17, 18]

A recent article by Engleson and Breaker discusses spectrum analysis of frequency modulation within the RF pulses. They suggest a new modulation index (I) which can be used to predict the shape of the pulsed-RF train spectrum. If ΔF is defined as the peak to peak frequency modulation deviation during one cycle of the pulse train (T), then the peak to peak frequency modulation deviation (D), during the pulse "on" time (τ), may be stated in terms of ΔF, T, and τ as

$$D = \frac{\Delta F \tau}{T} \tag{3-19}$$

If R is defined as the frequency modulating repetition rate, then I is given by Equation 3-20.

$$I = \frac{D}{R} = \frac{\Delta F \tau}{RT} \tag{3-20}$$

R is related to f_m as

$$R = \frac{1}{f_m} \tag{3-21}$$

The magnitude of I appears to give information on the amount of sideband harmonic amplitude increase in the (sin x)/x distribution. For $I \leq 10$ the spectrum is similar to the one shown in Figure 2-3b; but, for $I > 10$ the sidebands become larger in amplitude and the amplitude of the fundamental is reduced; also, due to the FM sidebands, the harmonics seem to come together.[18]

In order that the proposed technique function properly, a value of $I \leq 10$ appears to be desirable. To relate maximum input slewing rate to the maximum frequency of the input, the derivative of the expression for the modulating signal must be taken.

$$\frac{d}{dt}\left(\frac{V}{2}\cos W_m t\right) = -\frac{VW_m}{2}\sin W_m t \tag{3-22}$$

This has a maximum at t = 0; therefore, the maximum slewing rate magnitude can be expressed as

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{VW_m}{2} = V\pi f_m \tag{3-23}$$

Using Equations 3-20 and 3-21, Equation 3-23 can be rewritten as

$$\left(\frac{\Delta V_i}{\Delta t}\right)_{max} = \frac{V\pi TI}{F\tau} \tag{3-24}$$

Equation 3-24 is valid under the assumption that all other components will operate up to and including this maximum rate and that the converter will function properly for $I \leq 10$.

A conclusion as to which of the four possible speed limiting factors; the filter response (Equation 3-14), the counting speed of the up-down counter (Equation 3-15), the frequency modulation effect on the frequency spectrum (Equation 3-24), or the modulation rate of the VCO cause an upper limit on input slewing rate will be deferred until the prototype has been discussed.

CHAPTER IV

EXPERIMENTAL RESULTS

In this chapter, the actual circuits used in constructing the prototype for implementing the proposed analog-to-digital technique will be discussed.

A. Prototype

1. VCO

The first circuit type to be discussed is the VCO. Certain considerations must be made before the actual VCO can be chosen. The form and magnitude of the input signal and the number of quantization levels required must be specified. This, together with information on available filter types, can be used to specify the total frequency deviation required, including the end point frequencies. It was decided that a bipolar signal of magnitude ± 1 volt would be used as the analog input. This was to be divided into 5 quantization levels. A filter with a nominal center frequency of 455 KHz and a maximum 6db bandwidth of 0.9 KHz was used. A total frequency deviation of at least 5 times the maximum value of f_o was required by the VCO. Using Equation 3-13, with $p \leq 1/40$, a minimum value of f_o would be, $f_o = 36$ KHz. The total frequency deviation required is then, $\Delta f_c = 180$ KHz. Then, using Equation 3-1, K will equal 90 KHz/volt. A Beckman 9010 Function Generator was available which had a manual or voltage controlled output frequency. Figure 4-1 shows a plot of input voltage versus

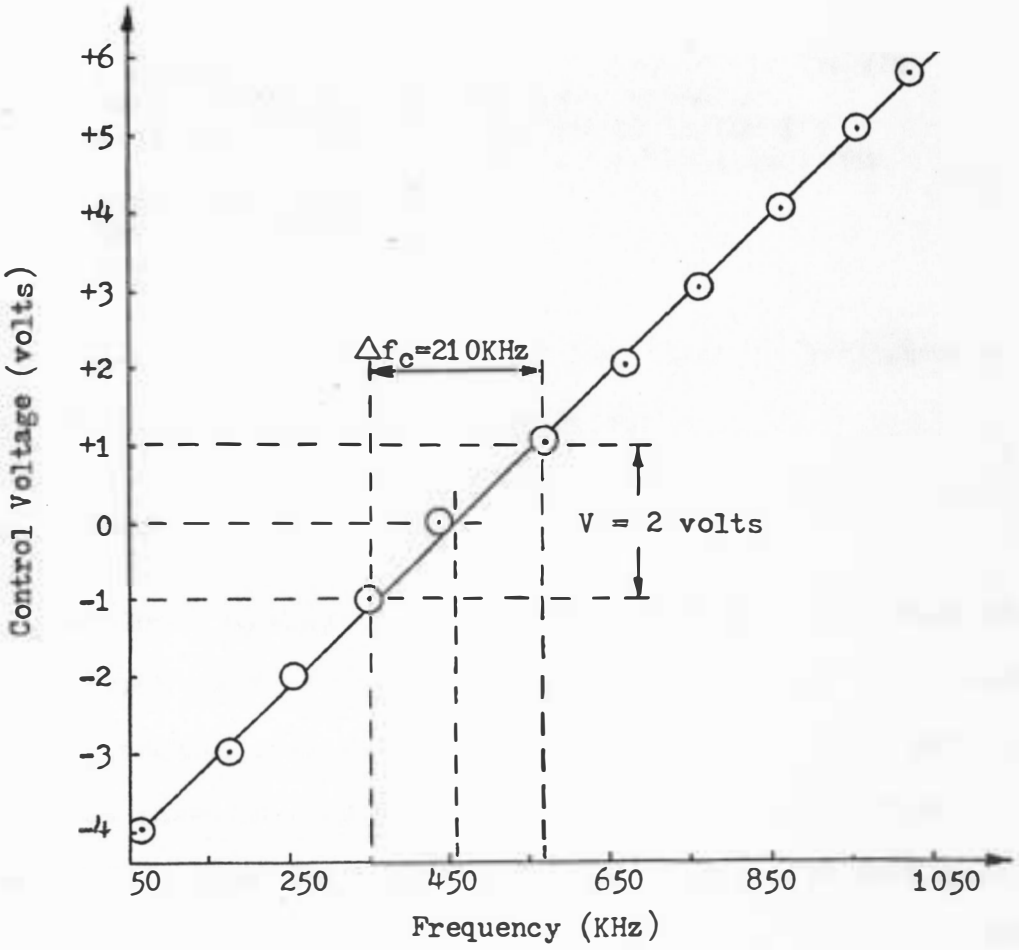


Figure 4-1. VCO Transfer Characteristic

output frequency with the center frequency (f_c) set at 455 KHz. A Δf_c of 210 KHz with V = 2 volts gives a K factor (Equation 3-11) of 105 KHz/volt. The instruction manual for the VCO gives the following relevant data:

Linearity: 0.1% for f_c vs. V_i from 50 to 100 KHz
Output Voltage: 0 to 30 volts, variable
Sine wave distortion: 1% from 50 to 100 KHz
2% from 100 KHz to 1 MHz
Input Impedance: 715 K Ω
Output Impedance: 50 Ω
Modulation Rate: 100 KHz

Given the above modulation rate of 100 KHz, Equation 3-23 gives a maximum VCO slewing rate of 628,318 volts/sec.

2. Chopper

As mentioned in Chapter III, the chopper chosen to produce the pulsed-RF train was to be made from two DTL NAND gates. Two Westinghouse, type WM231G, NAND gates, three resistors, and two diodes were connected as shown in Figure 4-2, along with the VCO and pulse generator, to produce the pulsed-RF train. Part of one NAND gate is used as a driver for the next gate which actually performs the chopping operation.[15] A Hewlett Packard, model 214A, pulse generator was used as the square wave source to set up the required values of T and τ. The square wave amplitude was three volts. When the output of the pulse generator is at zero volts, Q1 is off and Q2 and Q3 are on. Q2 and Q3 are manufactured in an identical manner so that they have matching characteristics. They are driven from the same source, so the

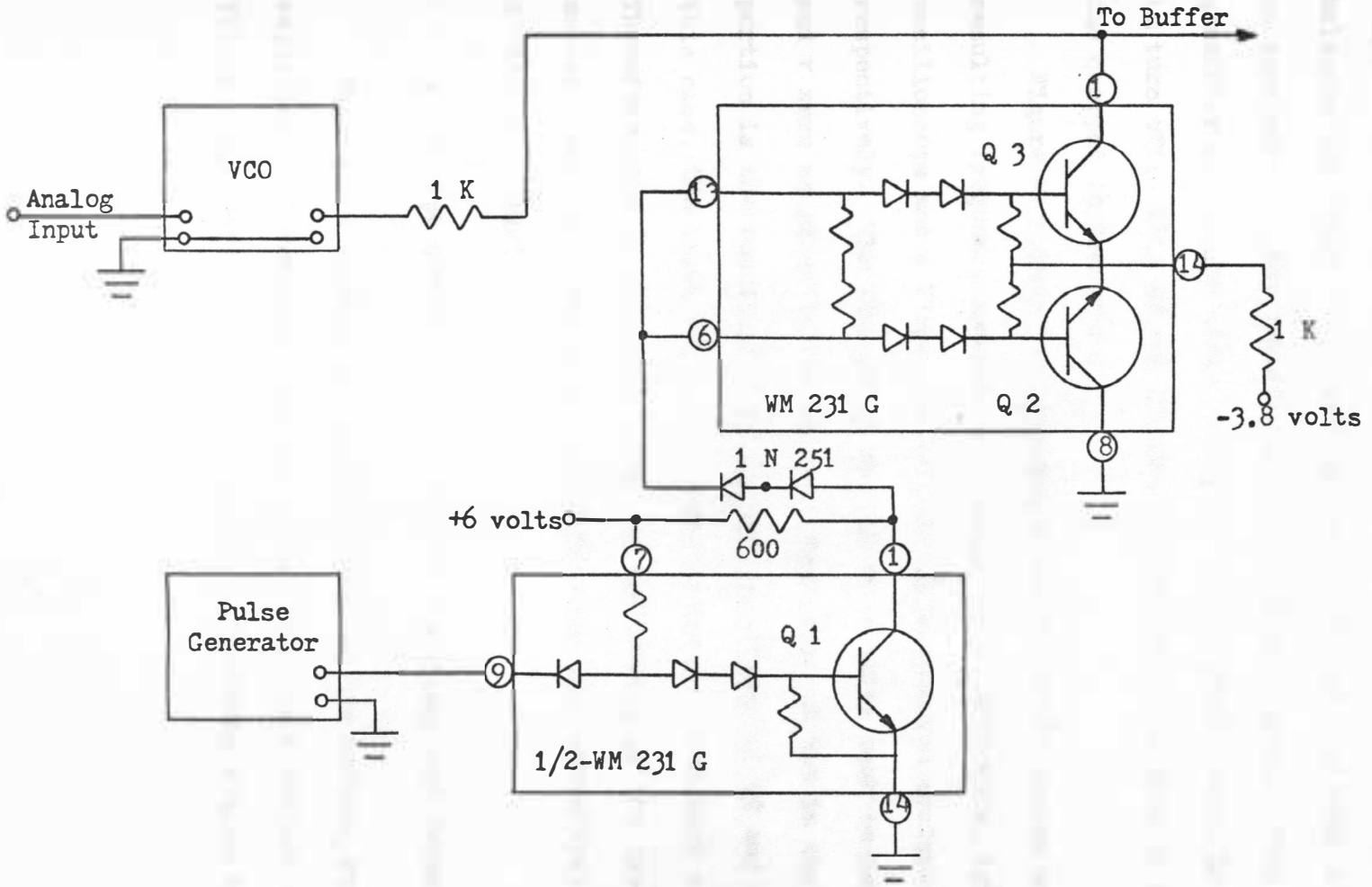


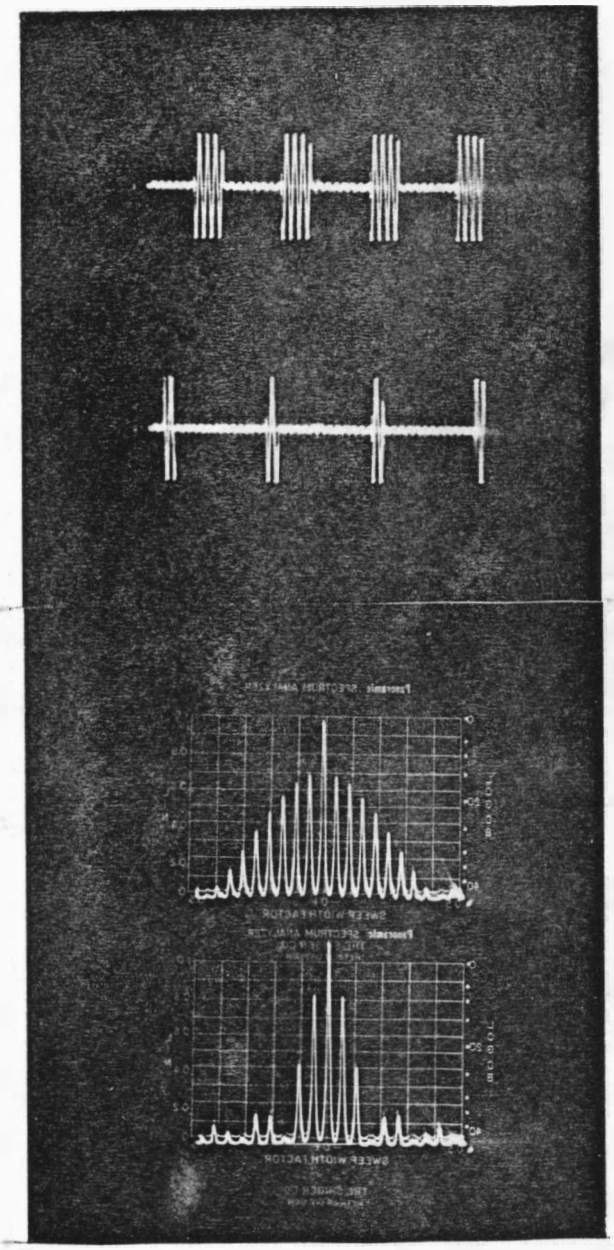
Figure 4-2. VCO, Pulse Generator, and Chopper Interconnection Diagram

base current to each is identical. Theoretically, the offset of Q2 balances the offset of Q3 causing pin 1, at the collector of Q3, to be at zero volts. This results in a zero output signal. When the pulse generator is at plus three volts, Q1 is on, which causes Q2 and Q3 to turn off. With Q2 and Q3 off, the VCO output passes on through the chopper to the buffer.

Figure 4-3 shows two representative pulsed-RF trains and the resulting frequency spectra as observed on a Tektronics, type 545A oscilloscope and a Singer, model SPA-3/25a spectrum analyzer, respectively. The VCO output was set at 4 volts peak-to-peak and T and τ were as given in the figure. The small offset in the blanked portion is the result of a difference in offsets of Q2 and Q3. For this case, the input voltage to the VCO was at a constant zero volts. Therefore, the frequency spectrum was not moving on the frequency scale. Each frequency spectrum agrees with the theoretical spectrum predicted by Equation 2-10.

3. Filter Buffer, Filter, Filter Amplifier, and Detector

Figure 4-4 shows the circuit diagram of the buffer, filter, filter amplifier, and envelope detector. The filter is a Collins mechanical filter, type F455FA-08. The filter specifications are as follows:



(a) Pulsed-RF Train
T = 28μsec, τ = 9μsec

Scale:
(a) and (b) 1 v
10 μsec

(b) Pulsed-RF Train
T = 28μsec, τ = 3.5μsec

(c) Frequency Spectrum of (b)
Linear Amplitude Scale
455 KHz Center Frequency
70 KHz/Div. Sweep Rate
Approximately 23db
Input Attenuation

(d) Frequency Spectrum of (a)
Same as (c)
Except Approximately
32db Input Attenuation

Figure 4-3. Pulsed-RF Train and Frequency Spectra for Different Pulse Widths

NOTE:

Resistor values in ohms.
Capacitor values in microfarads unless stated otherwise.
1pf = 10^{-12} farads.

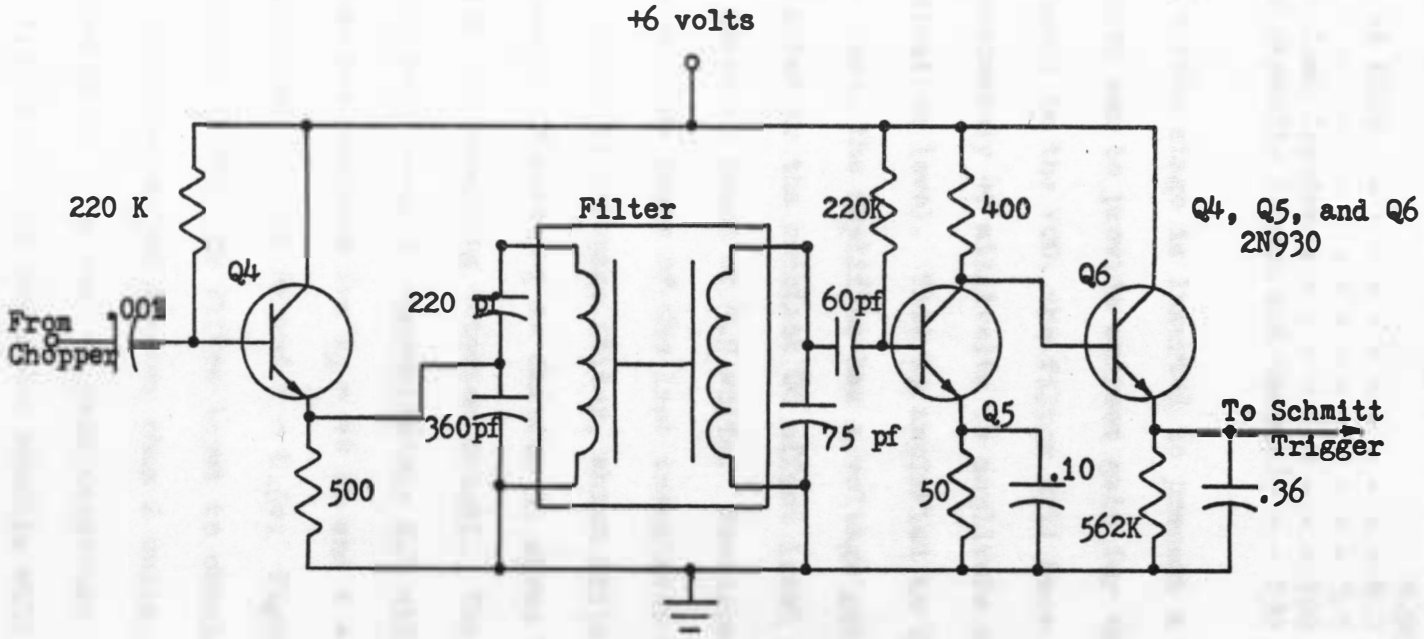


Figure 4-4. Buffer, Filter, Filter Amplifier, and Detector Circuit Diagram

Center Frequency- - - - - - - - - - - - - - - -	455	KHz nominal
Bandwidth at 3db- - - - - - - - - - - - - - - -	0.50	KHz minimum
Bandwidth at 6db- - - - - - - - - - - - - - - -	0.60	KHz minimum
	0.90	KHz maximum
Bandwidth at 60db - - - - - - - - - - - - - - -	4.0	KHz maximum
Ripple- -	3.0	db maximum
Source and Load Impedance - - - - - - - - - - -	100	KΩ
Resonating Capacity (Input and Output)- - -	130	pf±5pf

[19]

The emitter follower buffer stage is inserted to present a high impedance to the chopper and to provide current gain for the signal. With a 20 Hz input signal to the VCO, the filter will have a typical output signal of approximately 40 millivolts in amplitude whenever the input crosses a quantization level. This is amplified to 2.2 volts by the filter amplifier; thus, the amplifier has a voltage gain of 55. This 2.2 volts, when added to the constant DC offset level of 1.8 volts, gives a total detector input of 4.0 volts. Envelope detection results when the base-emitter diode of the last transistor transfers the amplifier output to the RC low-pass filter, which filters out the 455 KHz carrier frequency. Figure 5-1 in Chapter 5, shows 1/2 cycle of the analog input and the resulting detector output. The length of the filter response for each level is approximately 2.2 milliseconds. A similar response time was obtained for f_m = 40 Hz and V = 2v, f_m = 40 Hz and V = 0.5v, and f_m = 20 Hz and V = 0.5v. Figure 4-5 shows the number of cycles of 455 KHz filter input to obtain a given detector output. To obtain an output greater than 2 volts, at least 16 cycles of signal are required. The peak to peak magnitude of the filter input was 4.0 volts. Figure 5-1 and the above results will be used in Chapter V to make conclusions as to system speed, quantization

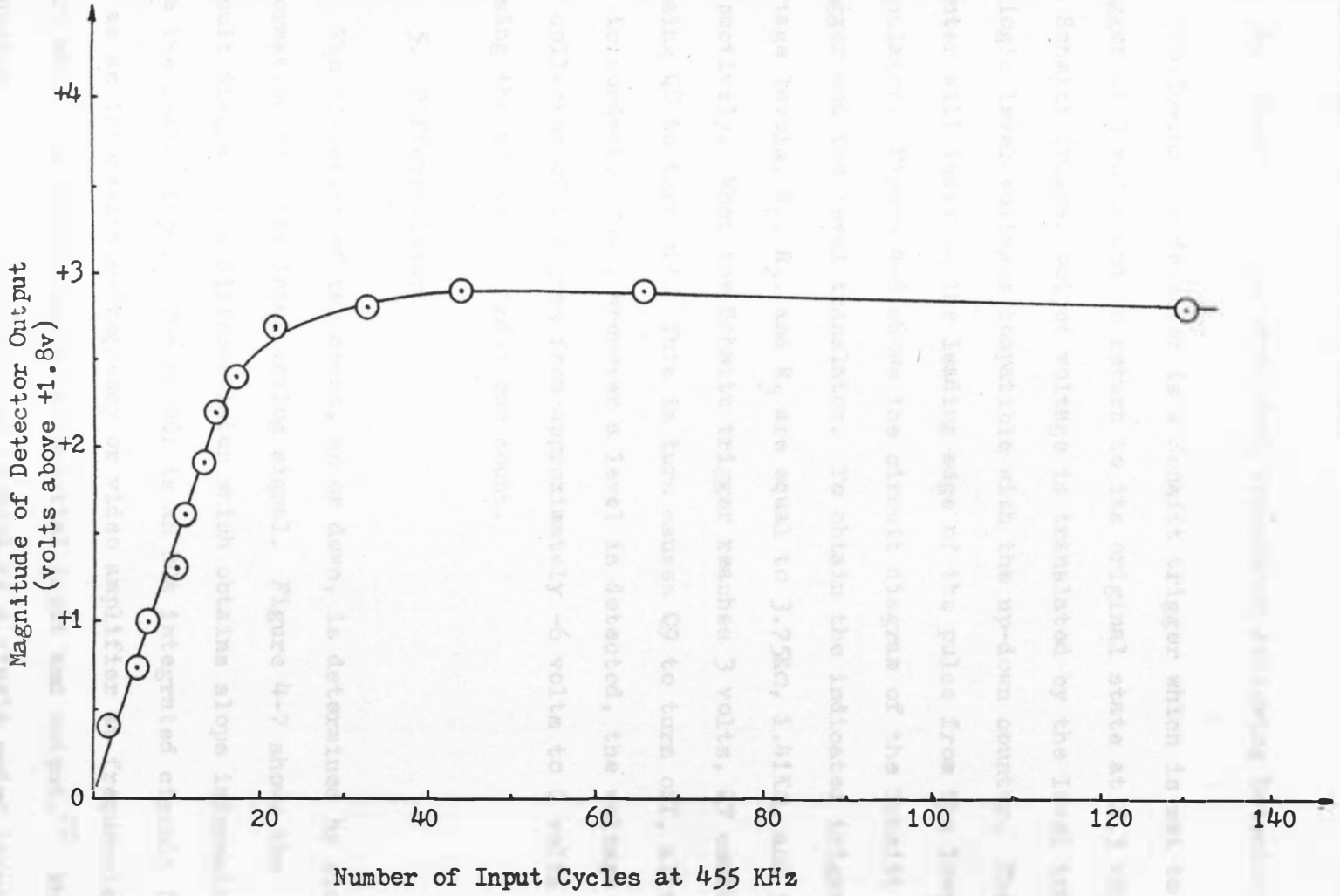


Figure 4-5. Number of Cycles of 455 KHz Filter Input Signal Versus Detector Output Voltage

uncertainty, and system lag time.

4. Schmitt Trigger and Level Translator Following Detector

Following the detector is a Schmitt trigger which is set to trigger at 3 volts and to return to its original state at 2.3 volts. The Schmitt trigger output voltage is translated by the level translator to logic level voltages compatible with the up-down counter. The counter will index on the leading edge of the pulse from the level translator. Figure 4-6 shows the circuit diagram of the Schmitt trigger and the level translator. To obtain the indicated trigger voltage levels, R_1, R_2, and R_3 are equal to 3.75KΩ, 1.41KΩ, and 5.8KΩ, respectively. When the Schmitt trigger reaches 3 volts, Q7 conducts causing Q8 to turn off. This in turn causes Q9 to turn off, allowing Q10 to conduct. Thus, whenever a level is detected, the voltage at the collector of Q10 goes from approximately -6 volts to 0 volts causing the counter to index one count.

5. Differentiator

The direction of the count, up or down, is determined by slope information from the input analog signal. Figure 4-7 shows the circuit diagram of a differentiator which obtains slope information from the analog input. The CA3001 is an RCA integrated circuit for use as an intermediate-frequency or video amplifier at frequencies up to 20 MHz. The CA3001 has a differential input and output.[20] When connected as shown, the amplifier is used as a single ended input

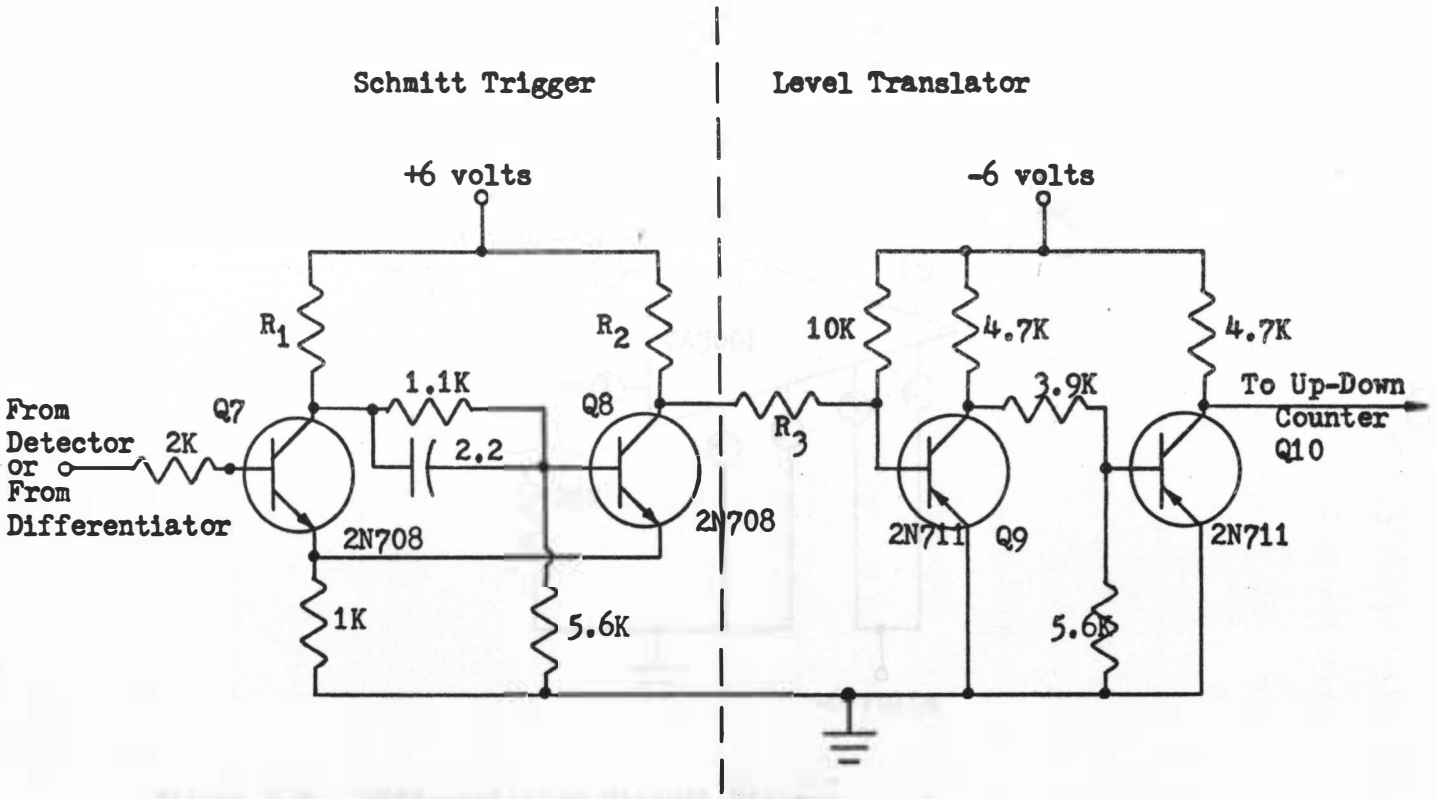


Figure 4-6. Schmitt Trigger and Level Translator Circuit Diagram

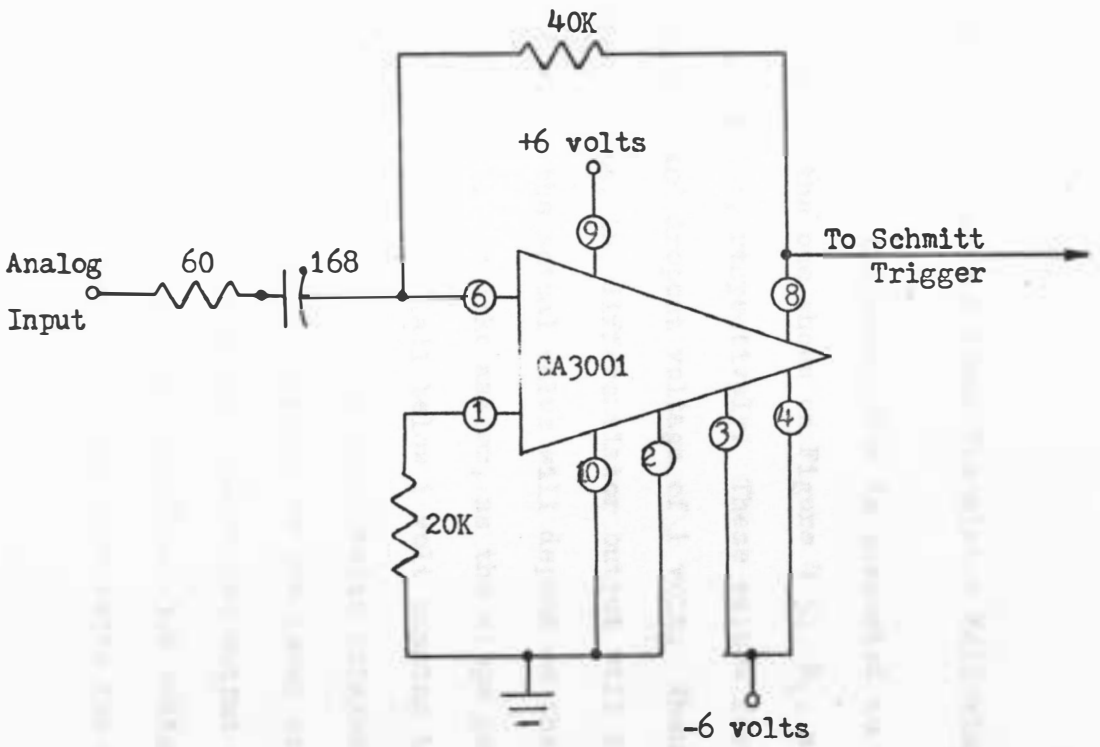


Figure 4-7. Differentiator Circuit Diagram

and output device, with the output having a DC offset of 1 volt.

The 40KΩ feedback resistor and the 0.168 μf capacitor are used in conjunction with the amplifier to produce a differentiating circuit. The 60Ω resistor is used to limit the gain of the amplifier at high frequencies; thereby, reducing the susceptibility to high frequency noise.

6. Schmitt Trigger and Level Translator Following Differentiator

The output of the differentiator is connected to a Schmitt trigger circuit similar to the one shown on Figure 4-5. R_1, and R_2, and R_3 are 5KΩ, 2KΩ, and 10KΩ, respectively. These values result in a nearly identical trigger and dropout voltage of 1 volt. When the analog signal has a positive slope, the differentiator output will increase to a value over 1 volt, the actual value will depend on the rate of increase of the analog signal. In like manner, as the slope goes negative the differentiator output will fall below 1 volt causing the Schmitt trigger to dropout. The output of the Schmitt trigger is connected to a level translator which is similar to the level translator discussed previously. Because of the load on the output of the level translator, the output voltage changes from -3.6 volts for a signal with a negative slope to approximately zero volts for a signal with a positive slope.

7. Up-Down Counter

The load on the output of the level translator is a bistable

multivibrator; hereafter, referred to as a flip-flop. Figure 4-7 shows a block diagram of how this flip-flop (F/F D) couples the slope information into an up-down counter. All the logic components used for the circuit shown on Figure 4-8 are part of a Digiac 3010 computer logic educational kit. The type of up-down counter used is similar to one shown in Computer Logic by Flores.[21] The voltage levels for the logic system are 0 to -0.3 volts for a logical 0 and -3 volts to -6 volts for a logical 1. The outputs of the flip-flops change state when their inputs change from a logic 1 to a logic 0. The monostable multivibrators (MMV) produce a 200 microsecond, 0 volt pulse, at the NP terminal, when their input changes from a logic 0 to a logic 1. The counter shown has a capability of counting to any number from 0 to 7 with the output of the counter taken from the 1 terminal of the flip-flops, giving the count in coded binary form. The sample analog signals used in testing the prototype were divided into 5 quantization levels. The binary codes and their respective voltage levels are given in Table 4-1. The change in voltage magnitude between levels can be calculated from the values of T and K used in the experimental setup. The values used were T = 23.8 μsec and K = 105 KHz/volt. With a T of 23.8 μsec, f_o will be 42.0 KHz and the voltage magnitude between levels will be K/f_o or 0.40 volts. With τ equal to 7.9 μsec, Equation 2-16 gives a q of 5. This agrees with the measured values given in Table 4-1.

The counter output is connected directly to a digital-to-analog converter. The D/A converter is used to allow a continuous visual readout of the count in the form of voltage levels at its output.

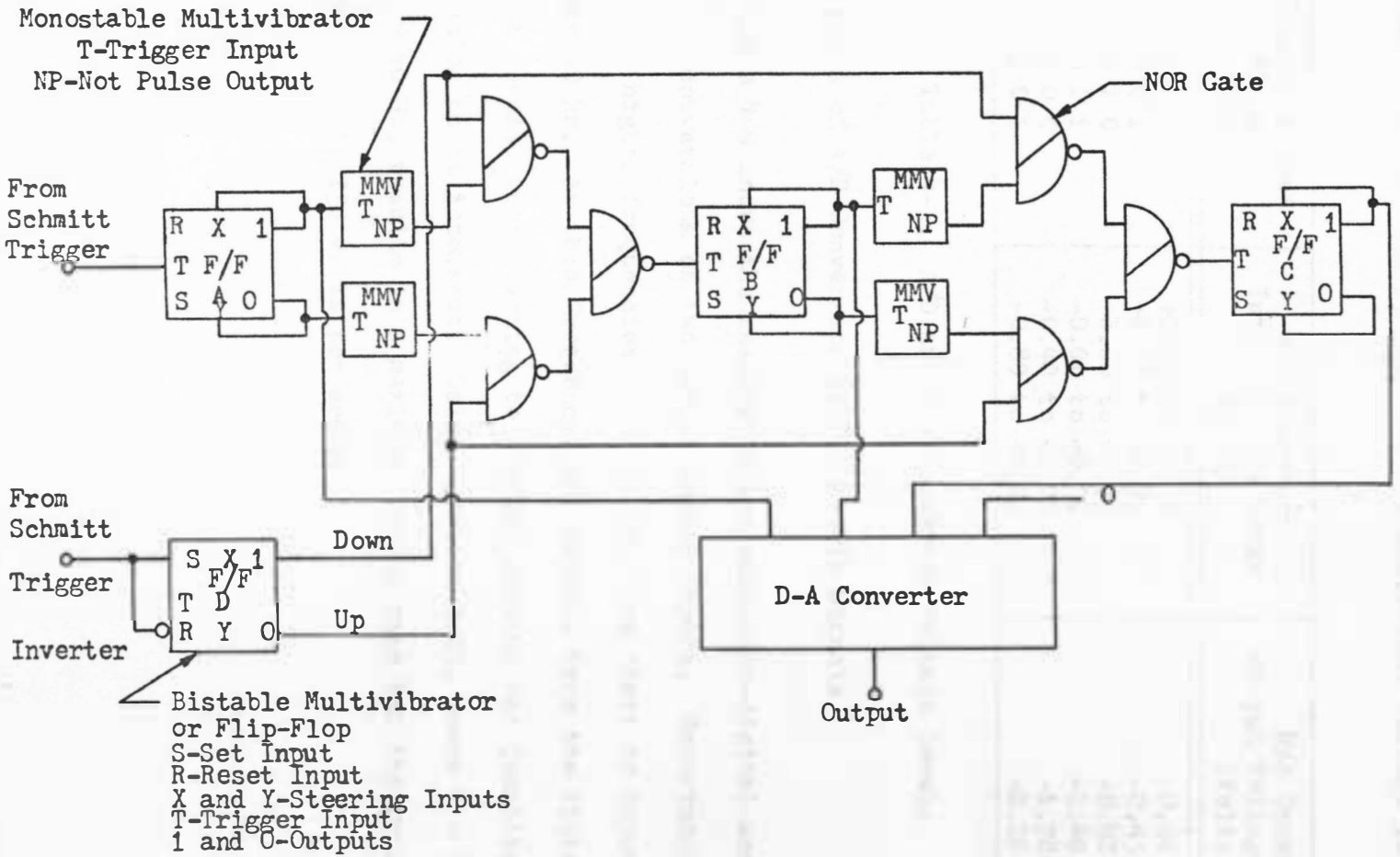


Figure 4-8. Logic Diagram of Up-Down Counter

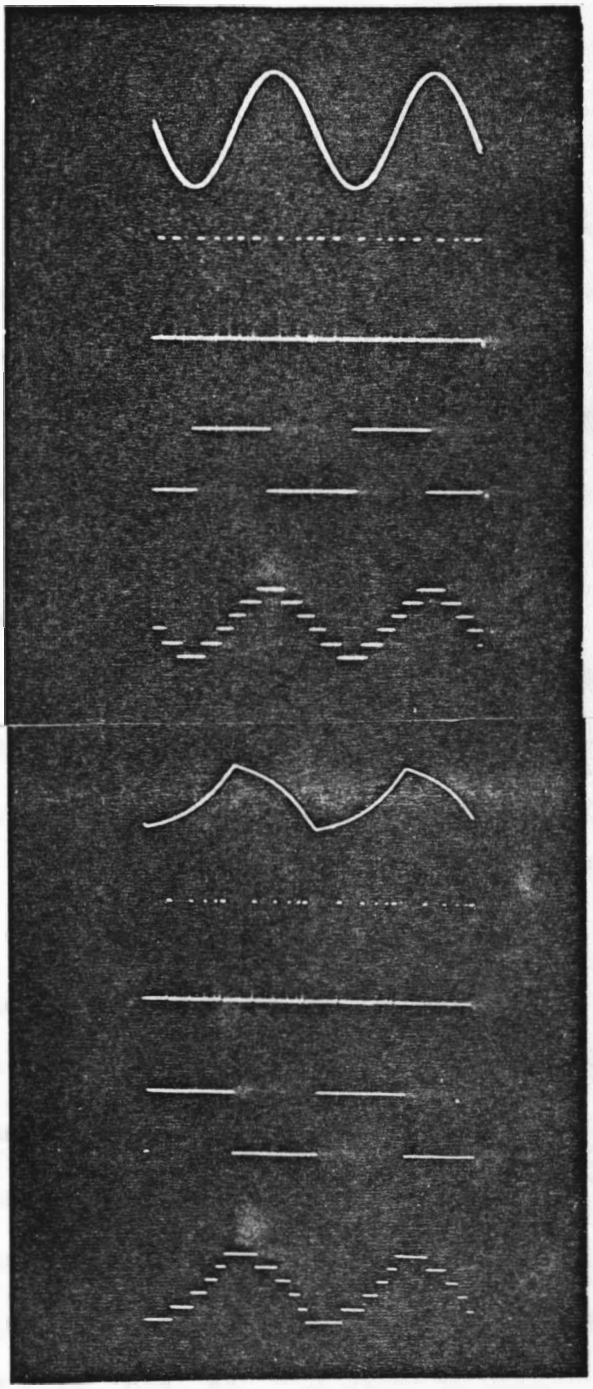
Table 4-1 gives the binary code and its equivalent voltage level.

Counter Output Binary Code	A/D Converter Input Voltage Range (Volts)	D/A Converter Output Voltage Level (Volts)
0 0 0	+0.80 to +1.00	0.00
0 0 1	+0.40 to +0.79	-0.45
0 1 0	0.00 to +0.39	-0.92
0 1 1	-0.01 to -0.39	-1.40
1 0 0	-0.40 to -0.79	-1.78
1 0 1	-0.80 to -1.00	-2.20

Table 4-1. A/D and D/A Converter Voltage Levels

B. Results of A/D Conversion of Two Sample Signals

Figure 4-9 shows the results of the analog-to-digital and digital-to-analog conversions of two sample analog inputs. Experimentation with signals at higher frequencies resulted in a top limit on input frequency of about 40 Hz. At this frequency, the outputs from the filter, for the adjacent levels, were starting to overlap causing the quantization information to be incorrect. Using Equation 3-23, where V = 2 volts and f_m = 40 Hz, results in a maximum slewing rate for the prototype of approximately 250 volts per second.



(a) 20 Hz Sine Wave Input 2 Volts Peak to Peak

(b) Quantization Pulses at Trigger Input of F/F A

(c) Slope Information at Set Input of F/F D

(d) Reconstruction of (a) at the Output of D-A Converter

(e) 20 Hz Exponential Wave Form, Input 2 Volts Peak to Peak

(f) Quantization Pulses at Trigger Input of F/F A

(g) Slope Information at Set Input of F/F D

(h) Reconstruction of (e) at the Output of D-A Converter

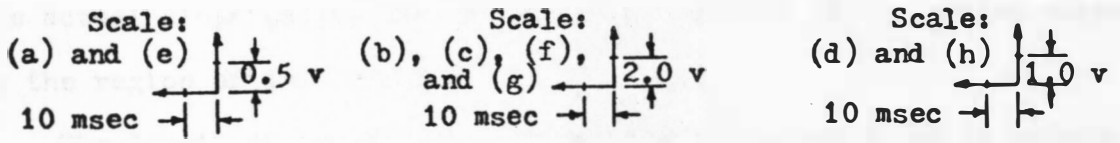


Figure 4-9. Results of Conversion of Two Sample Analog Inputs

CHAPTER V

CONCLUSIONS

Figure 5-1 shows 1/2 cycle of a sample analog signal and the resulting detector output. Each time axis represents the same time instants. Because of a time lag through the filter, the detector output, for any given level, is not centered over the specified quantization point. It can be seen from Figure 5-1, that the delay time through the filter varies from approximately 100 to 300 μsec depending upon the amplitude and shape of the detector output for any given level. The delays encountered in the remaining parts of the system are small compared to 100 μsec; therefore, the total system delay time varies between 100 and 300 μsec.

This variable delay time causes the actual point of quantization to vary around the ideal quantization point. The direction it varies depends on the slope of the analog input. Referring to Figures 1-1 and 5-1, it is apparent that as the analog signal increases, the actual quantization occurs in the shaded portion to the right of the ideal characteristic and as the analog signal decreases, the actual quantization occurs on the left side of the ideal characteristic. The actual point of quantization will depend on the specific delay time for that level and the shape of the detector output, which depends on the actual slope (magnitude as well as direction) of the analog signal in the region of quantization.

The length of the detector output for any given level is approximately 2.2 msec as given in Chapter IV. It was also stated that the

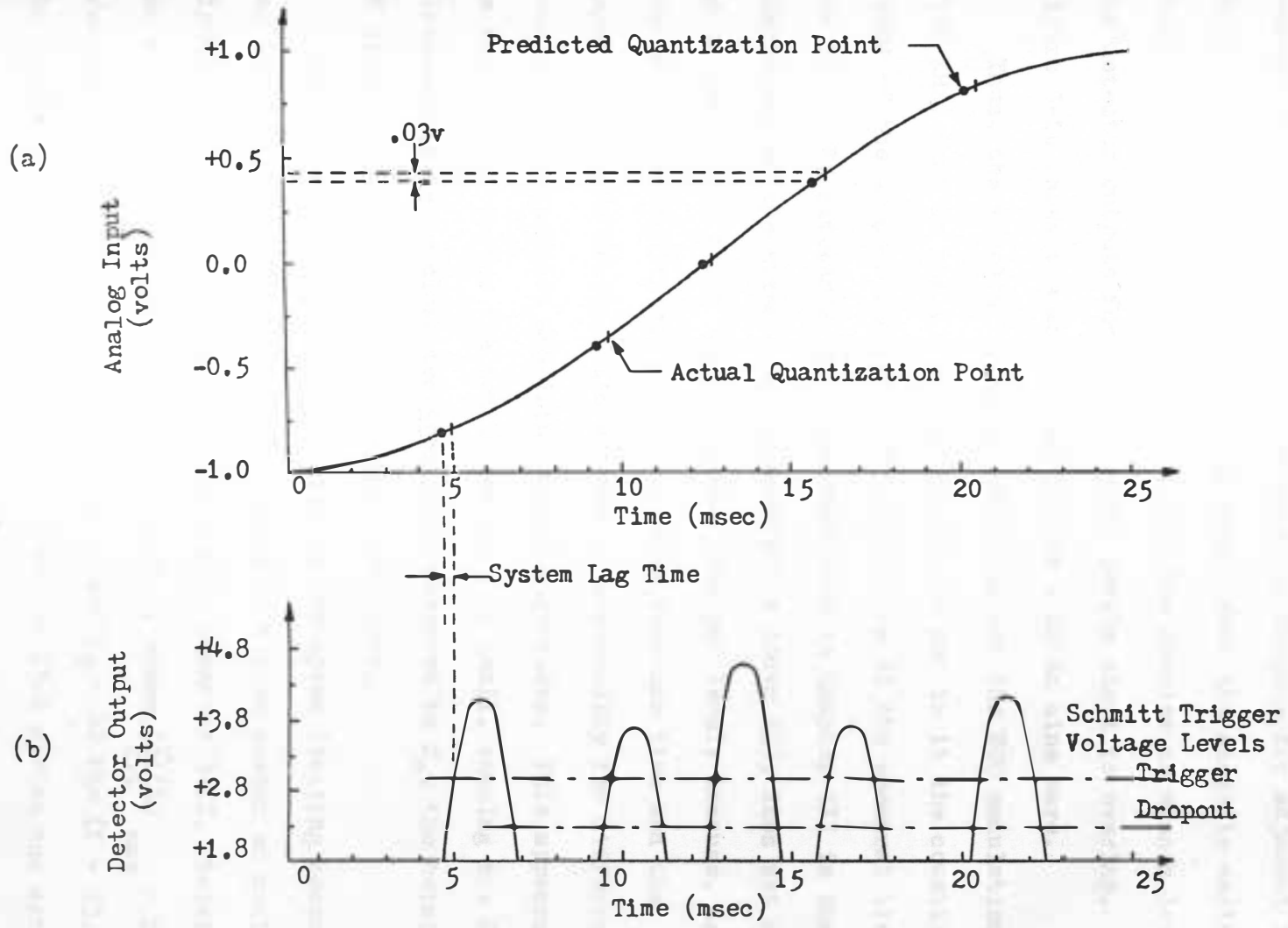


Figure 5-1. Quantization Results

prototype model had a maximum slewing rate of 250 v/sec, corresponding to a sine wave input to the VCO of 40 Hz. This slow slewing rate results because of the overlapping of the detector outputs for adjacent levels. For a sine wave input, overlapping occurs when the slope is maximum, which occurs near 0 volts. This causes the counter to miss a level as the detector outputs for the 3 central levels start to overlap. Figure 5-1b shows the actual spacing for a 20 Hz sine wave.

Thus, the results indicate that it is not the VCO modulation rate (100 KHz) that is the speed limiting factor nor is it the counting speed of the up-down counter. The broadening of the spectral lines due to the FM sidebands, that was mentioned in Chapter III in the discussion of the effects of the modulation index (I), does not appear to be the reason for a large response time per level; because, as stated in the results of Chapter IV, this response time and the magnitude of the response did not change appreciably for different modulation frequencies and input signal magnitudes. This appears to be reasonable because the modulation rate is small, causing the FM sidebands to be so close together that, compared to f_o, the total FM spectrum appears to be at a single frequency.

Further evidence that the filter is the speed limiting component can be obtained by calculating the value of m (the number of cycles of signal in the bandwidth of the filter) from Equation 3-12. Solving for m, Equation 3-12 gives, m = 15.6 cycles, where $(\frac{\Delta V_i}{\Delta t})_{max}$ = 250 v/sec, B = 0.9 KHz, f_b = 455 KHz, q = 5, and f_o = 42 KHz (T = 23.8 μsec). The results shown on Figure 4-5 show that for 15.6 cycles the detector

output should be 1.8 volts plus 1.7 volts or 3.5 volts. As seen from Figure 5-1, the actual responses varied from 3.6 to 4.5 volts showing good agreement. The difference in response magnitudes results from the non-equal amplitudes of the harmonics and the difference in the slope of the input signal for the various levels. As mentioned in relation to Equation 3-2, the fact that the frequency is continually changing causes the value of m, as calculated, to correspond to an equivalent number of cycles in the passband of the filter and not cycles of continuous 455 KHz signal.

One of the goals of this investigation was to provide a low cost A/D converter. If the total circuit was divided up and placed on five integrated circuit (IC) chips, so as to obtain versatility, the circuit could be divided as follows:

Circuit Function	Estimated Cost
VCO	$15.00
Pulse Generator & Chopper	$10.00
Filter Amplifier and Detector	$ 5.00
Differentiator, Detector, and Flip Flop	$10.00
Up-Down Counter	$10.00
Total IC Cost	$50.00

Added to the IC Cost would be the cost of the filter, which would be approximately $50.00, making the total estimated cost of parts, $100.00. A selling price at three to five times this amount would still put the price of this converter in the low cost category.

A second goal of this investigation was to provide a flexible A/D converter. As can be seen from Figure 4-3 and Equation 2-16, changing the number of quantization levels can be accomplished by changing the

ratio of T/τ. To increase the number of levels the up-down counter would have to be enlarged. The maximum number of levels that could be obtained would be limited by the fact that as more levels are added the amplitudes of the harmonics become smaller for a given magnitude of VCO output. The speed of operation of the prototype is low by comparison to other methods but further engineering work on the filter design should increase the speed of operation to a point where the effect of the frequency modulation process becomes the speed limiting factor.

As the prototype now exists, it operates best in a continuous mode. To extend this technique to operation in the multiplex mode, two additional functions must be added. One of the additions would be a low-pass filter at the input of the device and the other would be a resetting circuit which would reset the counter to a given code as it caused the input to go to zero. The input filter would function to exclude high frequency noise and it would also allow the input to have a slewing rate that the system could handle without making errors. It would also allow starting the A/D converter when the initial value of the analog signal is other than zero. With the input filter included, the VCO input rise time would never be greater than the rise time of the filter response. The addition of the reset function would allow the converter to be used in a continuous or multiplex mode. It and the filter are necessary to start the A/D conversion process without introducing errors. Once an error in count occurs, the system must be reset to correct for the error. In this respect it differs from other systems that correct

themselves after a certain number of counts following a slope overload.

A comparison of the working model, as studied, plus the above additions can be made with the methods of A/D conversion given in Table 1-1. This method would operate best in a continuous mode but could be operated in a multiplex mode. Conversion time and aperture would depend on the outcome of further engineering study on the maximum slewing rate obtainable with a filter that has a faster response time. The aperture time would not be constant because of the quantization uncertainty mentioned previously. The relative cost of this method would be low.

Therefore, the purpose of this investigation and the goals outlined in Chapter I have been met. This technique would be useful for slowly varying analog signals such as body or climatic temperature changes. This technique would adapt well to a remote sensing situation where the information was to be sent over a communication link. The quantization and slope information could be combined into two different frequency signals. One frequency would indicate an up count and the second frequency would indicate a down count. This information could be easily decoded at the receiver and fed into an up-down counter to obtain the digital representation. By transferring information in this manner, elaborate coding and decoding circuits would not be required. Also, a possible reduction in bandwidth could enable the communication link to carry many such channels of information.

In the course of this investigation, the following questions arose which require further study:

1. What is the best type of filter to use in detecting a varying frequency signal of the type used in this thesis?

2. Given a filter with the required response, what maximum slewing rate can be obtained before the frequency spectrum of the pulsed-RF signal becomes unusable for this technique?

3. What advantages over current methods does this technique have when used in conjunction with a communication link?

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