

1000-Fold Double-Flux-Quantum Voltage Multiplier Employing Directional Propagation of Flux Quanta Through Asymmetrically Damped Junction Branches

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journal or publication title	IEEE Transactions on Applied Superconductivity
volume	29
number	5
page range	1400105-1-1400105-5
year	2019-08
URL	http://id.nii.ac.jp/1438/00009291/

doi: 10.1109/TASC.2019.2895606

1000-Fold Double-Flux-Quantum Voltage Multiplier Employing Directional Propagation of Flux Quanta through Asymmetrically-Damped Junction Branches

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Abstract—Precise voltage generation is a unique feature of single-flux-quantum (SFQ) circuits, in addition to their high-speed digital signal processing with low power consumption. We investigated SFQ pulse-frequency modulation D/A converters for metrological applications. In our SFQ-based D/A converters, the maximum output voltage is determined by the maximum SFQ pulse-frequency at the pulse number multiplier, and by the voltage multiplication factor at the voltage multiplier. In this study, we present our new design for a double-flux-quantum amplifier (DFQA) that works as a quantum voltage multiplier. In the new parameter set, we tuned the damping parameters of the Josephson junctions to realize proper propagation of SFQ pulses. A 1000-fold DFQA designed with the new parameter set was fabricated using a $25\text{-}\mu\text{A}/\mu\text{m}^2$ Nb/AIO_x/Nb integration technology. A 1000-fold voltage multiplication was confirmed for the input voltage up to $43\text{ }\mu\text{V}$, with a corresponding SFQ repetition frequency of 21 GHz . That is, the output voltage reached 43 mV .

Index Terms—Superconducting integrated circuits, Josephson effect, Digital-analog conversion.

I. INTRODUCTION

THE AC Josephson effect is a phenomenon that occurs when the voltage, V across a Josephson junction is proportional to the temporal differentiation of the junction phase difference, ϕ . It is expressed as $V = (\Phi_0/2\pi)(\partial\phi/\partial t)$, where Φ_0 is a single-flux-quantum (SFQ). Its time average $\langle V \rangle$ is expressed as $\langle V \rangle = \Phi_0 f$, where f is the number of 2π phase leaps in a unit time.

In a superconducting SFQ circuit, one 2π -phase-leap of a Josephson junction corresponds to one SFQ pulse. This means that precise voltage generation is possible in an SFQ circuit with well-controlled SFQ pulse trains [1], [2]. Several prototypes of SFQ-based digital-to-analog converters (DACs) for metrological applications have been reported [3]–[5]. Our 9-bit, 2.5-mV DAC comprising 1544 Nb/AIO_x/Nb Josephson junctions has also been reported, where SFQ pulse-frequency modulation was employed for changing the analog output voltages [6], [7]. The maximum output voltage was determined by the maximum SFQ pulse-frequency at the pulse number multiplier (12.3 GHz), and by the voltage multiplication factor at the voltage multiplier (100-fold). (The product of 2.07×10^{-15} Wb, 12.3 GHz, and 100 is 2.5 mV.)

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Manuscript received October 22, 2018; revised December 23, 2018. This work was partially supported by JSPS KAKENHI Grant Numbers 15K13999 & 17K04979, and also by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

One disadvantage of SFQ-based DACs is their relatively small output voltages compared to other Josephson voltage standard technologies [8], [9]. For our SFQ-based DACs, improving the voltage multiplication factor could be the most effective way to address this shortcoming because a 10-fold improvement in the SFQ pulse-frequency would be difficult to achieve. Among several ideas on voltage multipliers [1]–[3], [10], [11], we employed the double-flux-quantum amplifier (DFQA) [12]. In fact, we implemented a 100-fold DFQA in the 9-bit DAC described above [6], [7], while evaluating a 1000-fold DFQA independently [13], [14]. The 1000-fold DFQA worked for input voltages up to $27\text{ }\mu\text{V}$, with a corresponding SFQ repetition frequency of 13 GHz . The maximum input voltage was approximately 40% of the value obtained by numerical simulation.

During our study on DFQAs, we discovered a new set of device parameters that enabled operation without flux biasing [15]. Its operation was experimentally demonstrated, although the range of its operation for the input voltage was less than $17\text{ }\mu\text{V}$ (40% of the numerical result). We also determined that the directional propagation of SFQ pulses was achieved in the new DFQA through asymmetrically-damped junction branches.

In this study, we refined the DFQA with a new parameter set [16]. A simple numerical simulation of directional SFQ propagation through asymmetrically-damped junction branches is presented prior to the detailed description of refinement. Furthermore, we present the design and operation of a 1000-fold DFQA realized through the new parameter set.

II. DIRECTIONAL PROPAGATION OF FLUX QUANTA THROUGH ASYMMETRICALLY-DAMPED JUNCTION BRANCHES

In SFQ circuitry, a buffer stage with an escape junction is commonly used to realize the directional propagation of flux quanta, where the difference in the critical currents of two serially-connected junctions is the most important consideration [17]. The original DFQA also employs the difference in critical currents [12]. Conversely, our parameter optimization using the SCOPE2 program [18] suggested that the difference in junction damping is a possible alternative design principle [15].

Fig. 1 shows a schematics of a part of a DFQA with a propagation sequence of flux quanta [12]. A three-junction loop (3JL) including a JJA, JJB, and JJC is a fundamental cell that is stacked in a DFQA. In the parameter set of

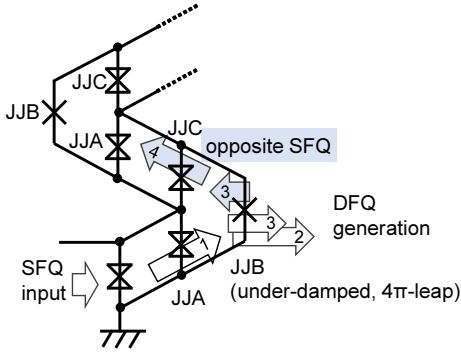
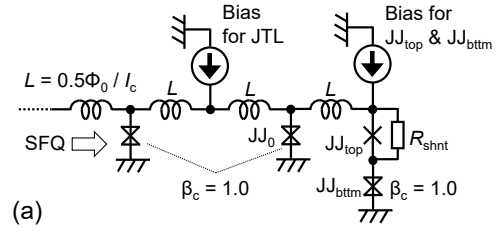


Fig. 1. Propagation of a SFQ in a three-junction loop (3JL) of a DFQA. Two magnetic bias lines are not shown.

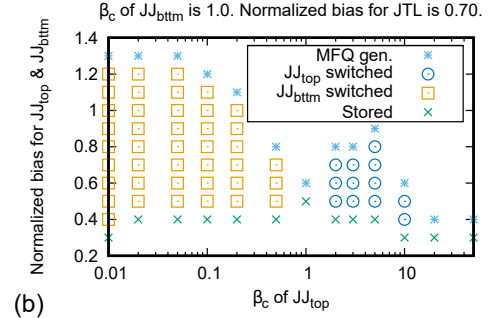
the original DFQA, the JJA and JJC are critically damped while the JJB is under-damped without a shunting resistor. Magnetic flux biases are also applied to 3JLs and two-junction loops in between, although they are not shown in Fig. 1. The sequence of operation is as follows: First, an input SFQ is transferred into the first 3JL through the JJA. Second, it passes through the JJB where the DFQ is generated (4π -transition). Concurrently, an opposite (reflected) SFQ is generated in the 3JL and transferred to the next cell through the JJC. Repeating this sequence f times in a unit time adds the average voltage of $\Phi_0 f$ to the output voltage.

There are two important steps towards realizing this DFQA operation: First, DFQ generation is performed at the under-damped junction, JJB. Second, the direction of propagation of the opposite (reflected) SFQ. The reflected SFQ needs to move towards next stage through the JJC and not return through the JJA. In the original parameter set [12], the critical current of the JJC is 40% less than that of the JJA. (Detailed values are shown in Table I and will be discussed later.) Thus, the reflected SFQs propagate to the next cell through the JJC. Conversely, there is no significant difference between the critical currents of the JJA and JJC in the new parameter set [15]. Instead, the JJA is heavily damped and the JJC lightly damped. Such difference in junction damping ensures that the direction of propagation of the reflected SFQs is through the JJC.

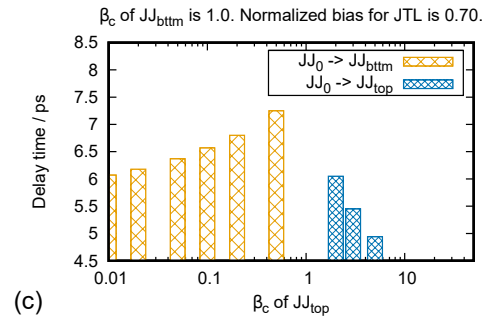
To demonstrate the directional propagation control using asymmetrical damping, we performed a simple circuit simulation. The circuit model is shown in Fig. 2(a). It is composed of a Josephson transmission line (JTL), in which the junctions are critically damped ($\beta_c \equiv 2\pi I_c C_J R_J^2 / \Phi_0 = 1.0$, where I_c , C_J , and R_J are the critical current, capacitance, and resistance of the junction, respectively), with two junctions in series at the right end. β_c is commonly referred to as the McCumber-Stewart parameter [19], [20]. One of the junctions, the JJ_{btm} is critically damped. The damping of the other, JJ_{top} , is varied by changing the value of the shunting resistance. Fig. 2(b) shows the dynamic properties of the SFQ propagation at the $JJ_{\text{top}}-JJ_{\text{btm}}$ branch. It was observed that SFQ propagates through the junction with larger β_c . This is an alternative principle for achieving directional SFQ propagation. That is, when β_c of JJ_{top} is greater than 1, an SFQ coming through JJ_0



(a)



(b)



(c)

Fig. 2. (a) Circuit model used in the simulation of asymmetrically-damped junction branches. SFQ pulses are transferred through a JTL comprising critically-damped Josephson junctions ($\beta_c = 1.0$). JJ_{btm} at the right end is also critically damped while the damping parameter (β_c) of the JJ_{top} is varied. The critical currents of all the Josephson junctions were assumed to be identical. (b) Propagation direction plotted on the β_c -normalized bias plane. (The bias currents are normalized by the critical current of a single Josephson junction.) The results are classified into four states: MFQ gen. (generation of multiple flux quanta), JJ_{top} switched (2π -phase leap only at JJ_{top}), JJ_{btm} switched (2π -phase leap only at JJ_{btm}), and stored (neither JJ_{top} nor JJ_{btm} switched by an SFQ). (c) Delay from the JJ_0 (the last junction of the JTL) to either the JJ_{top} or JJ_{btm} .

(the last junction of the JTL) passes through JJ_{top} . In contrast, when β_c of JJ_{top} is less than 1, an SFQ coming through JJ_0 goes through JJ_{btm} with a β_c of 1.0.

The delay from JJ_0 to JJ_{top} and from JJ_0 to JJ_{btm} are plotted in Fig. 2(c). When the β_c of JJ_{top} is greater than 1, the JJ_{top} switches, not the JJ_{btm} , and the delay becomes shorter as β_c of JJ_{top} increases because the damping of JJ_{top} is decreased.

Conversely, the bias margins for $\beta_c > 1$ shown in Fig. 2(b) are not as wide as those for $\beta_c < 1$. When the β_c of JJ_{top} is less than 1, the JJ_{btm} switches, not the JJ_{top} , and the delay becomes shorter as the β_c of JJ_{top} decreases. Although the β_c of JJ_{btm} is fixed at 1.0, the selection of a switching junction takes shorter time as the difference in the β_c values becomes larger.

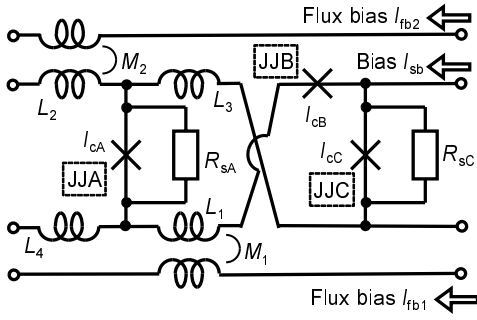


Fig. 3. Equivalent circuit of a 3JL used as a fundamental cell of a DFQA.

 TABLE I
 CIRCUIT PARAMETERS OF A 3JL CELL.

	This work	Original [12]
L_1 / pH	2.9	1.6
L_2 / pH	0.68	1.9
L_3 / pH	0.62	0.70
L_4 / pH	1.5	none
M_1 / pH	0.36	0.27
M_2 / pH	none	0.16
I_{cA} / mA	0.10	0.24
R_{sA} / Ω	0.58	1.6
β_{cA}	0.022	0.98
I_{cB} / mA	0.21	0.22
R_{sB} / Ω	384	366
β_{cB}	4.3×10^4	
I_{cC} / mA	0.13	0.14
R_{sC} / Ω	35	2.8
β_{cC}	138	1.0

*To calculate the McCumber parameters of β_{cA} , β_{cB} , and β_{cC} , we assumed that the Josephson current density, specific capacitance, and $I_{cB}R_{sB}$ product were $25 \mu\text{A}/\mu\text{m}^2$, $55 \text{ fF}/\mu\text{m}^2$, and 80 mV , respectively.

III. REDESIGN OF THE DFQA PARAMETERS

As described above, a DFQA comprises 3JL cells connected in series [12]. Figure 3 shows the equivalent circuit of a single 3JL.

The original 3JL has three bias lines: one for direct bias current and the other two for magnetic flux biases to the loops. From the viewpoint of large integration, less bias lines are desirable. Thus, in our previous study [15], we redesigned circuit parameters by gradually reducing the flux bias currents I_{fb1} and I_{fb2} . This was done using the optimization tool, SCOPE2 [18]. We finally reached the parameters that enabled us to operate a DFQA without flux biasing, although the operating margins were quite limited compared to the margins predicted by numerical simulation.

After the experimentation, we checked the layout and the equivalent circuit of the 3JL, and found that the equivalent circuit was not accurate enough [16]. We refined the equivalent circuit by adding L_4 in Fig. 3, then re-optimized the parameters using SCOPE2. The results of the re-optimization are listed in Table I with the original parameters [12].

In the original parameter set [12], the critical current of the JJC (I_{cC}) was set to 0.14 mA , which is 40% less than that of the JJA ($I_{cA} = 0.24 \text{ mA}$) as described in Table I. Conversely, in the new parameter set, the JJA is heavily damped ($\beta_{cA} = 0.022$) while the JJC is lightly damped

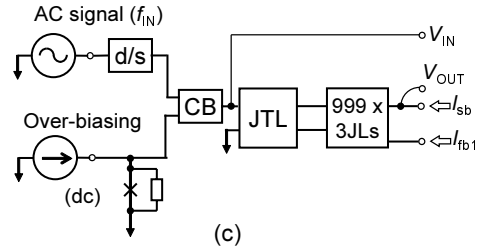
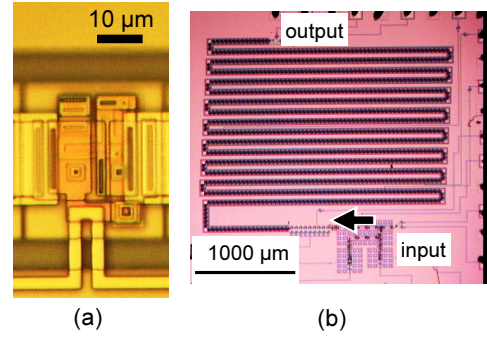


Fig. 4. (a) Photomicrograph of a 3JL. (b) Photomicrograph of a 1000-fold DFQA comprising 999 3JLs. (c) Measurement setup. An SFQ pulse train into the circuit can be introduced via either of the two possible methods: a dc/SFQ (d/s) converter driven by an ac current source, or a single junction overbiased by a dc current source. Two input paths are merged in a confluence buffer (CB). The average voltages of the input (V_{IN}) and output (V_{OUT}) were measured.

($\beta_{cC} = 138$). Such difference in damping makes the reflected SFQs to propagate through the JJC. It should be noted that the resistor of 35Ω would be long and have a certain amount of parasitic inductance. In this work, however, we did not include such parasitic inductance in numerical simulation for simplicity.

Besides the addition of L_4 , we decided to omit one flux bias line related to M_2 and I_{fb2} because the re-optimized M_2 value was one digit less than M_1 value. On the other hand, we needed to keep the other flux bias line to ensure that the operating margins were wide enough.

IV. EXPERIMENTS, RESULTS, AND DISCUSSION

We designed a 1000-fold DFQA using the new parameter set. Test chips were fabricated using the $25\text{-}\mu\text{A}/\mu\text{m}^2$ Nb/AIO_x/Nb Josephson integration process (STP2) of the National Institute of Advanced Industrial Science and Technology (AIST), Japan, which is based on Nb circuit fabrication process developed in the NEC Corporation [21]. Figs. 4(a) and 4(b) show photomicrographs of a single 3JL and the entire 1000-fold DFQA, respectively.

In the measurements, the test chip was cooled down in a liquid helium bath. The measurement setup is illustrated in Fig. 4(c). We adopted two methods for introducing an SFQ pulse train into the circuit. In the first method, we used a dc/SFQ (d/s) converter that was prepared as a fundamental cell in the CONNECT cell library [22], driven by an external ac current source. The input voltage was calculated as $\Phi_0 f_{IN}$, while the output voltage V_{OUT} was measured using a digital multi-meter. In the second method, we used a single Josephson

junction (input junction) overbiased by an external dc current source. (The critical current of the input junction was 0.10 mA, shunted by a 1.2 Ω resistor.) The average input voltage V_{IN} and V_{OUT} were acquired via digital oscilloscope through 40 dB differential voltage pre-amplifiers. The input SFQ pulse repetition frequency was calculated using V_{IN}/Φ_0 .

Fig. 5(a) shows f_{IN} - V_{OUT} characteristics obtained using a dc/SFQ converter for feeding the input SFQ pulse train. In this measurement, the maximum input frequency for the 1000-fold voltage multiplication was 1 GHz. Below 1 GHz, the V_{OUT} followed an ideal 1000-fold voltage multiplication line. The maximum relative error was 0.18%, calculated using $\{|V_{OUT} - 1000\Phi_0 f_{IN}|/1000\Phi_0 f_{IN}\} \times 100\%$ with the experimental values of $f_{IN} = 700$ MHz and $|V_{OUT} - 1000\Phi_0 f_{IN}| = 2.6$ μ V. These values are comparable with the results of our previous 1000-fold DFQA [14]. Although the origins of voltage errors are not clearly understood at the moment, external noise is probably dominant. Beyond 1 GHz, it was impossible to confirm stable operation because the multiplication factor was strongly dependent on the amplitude of the ac signal source. The bandwidth of our experimental setup seemed insufficient for input frequencies above 1 GHz.

Fig. 5(b) shows the experimental results for the V_{IN} - V_{OUT} characteristics measured using the overbiasing method. Voltage fluctuation was most likely due to external noise. The V_{OUT} followed the ideal line of $1000V_{IN}$ for V_{IN} below 43 μ V, with a corresponding SFQ repetition frequency of 21 GHz, which was 64% of the value obtained by numerical simulation. This maximum input voltage shows significant improvement over our previous result of 27 μ V (13 GHz) [13], [14]. Above 43 μ V, the V_{OUT} became less than the ideal values for the 1000-fold voltage multiplication.

As described in the introduction, the new parameter set realizes wider bias margins than the original parameter set [15]. For example, the margins for I_{sb} and I_{fb1} are improved from $\pm 17\%$ to $\pm 23\%$ and from $\pm 33\%$ to $\pm 157\%$, respectively. The wider bias margins realized by the new parameter set are likely to contribute to a wider operating range for V_{IN} . Numerical simulation also suggested that the transit time of an SFQ through one 3JL was improved from 12.5 to 10.5 ps. Faster SFQ propagation in the DFQA is also desirable for wider operating ranges.

V. CONCLUSIONS

We presented a new design for 3JLs in DFQAs, where the damping parameters of the Josephson junctions were tuned to realize proper propagation of SFQ pulses. Their directional propagation in asymmetrically-damped junction branches was numerically demonstrated using a simple circuit model. We then described our refinement of the equivalent circuit and re-optimization of the circuit parameters. A 1000-fold DFQA was fabricated through niobium integration technology using the new parameter set. A 1000-fold voltage multiplication was confirmed using two measurement methods. The multiplication accuracy was evaluated using a d/s converter with input frequencies below 1 GHz, with relative errors less than 0.18%. The maximum input voltage checked using the overbiasing

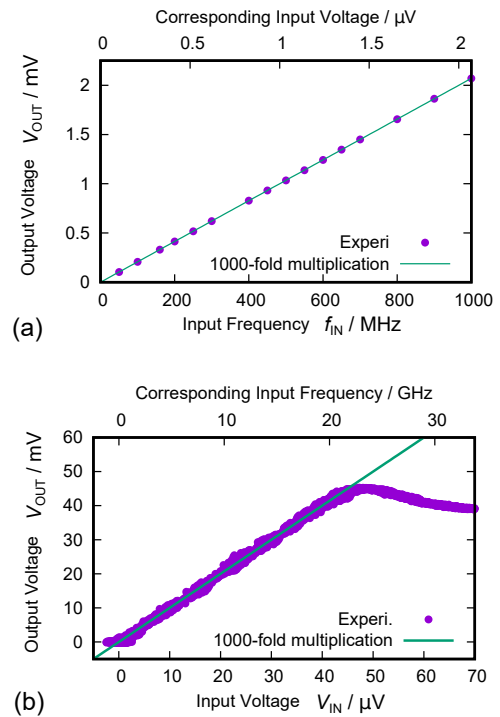


Fig. 5. (a) f_{IN} - V_{OUT} characteristics measured using a d/s converter. The maximum f_{IN} for correct operation was 1 GHz. The relative multiplication errors were less than 0.2%. (b) V_{IN} - V_{OUT} characteristics measured using the overbiasing method. The maximum V_{IN} for 1000-fold voltage multiplication was 43 μ V, with a corresponding SFQ repetition frequency of 21 GHz.

method was 43 μ V, with a corresponding SFQ repetition frequency of 21 GHz. The output voltage reached 43 mV. This was a 60% improvement over our previous 1000-fold DFQA design using the original parameter set [12]–[14].

ACKNOWLEDGMENT

The authors are grateful to M. Maezawa for initiation of the present work. The authors thank M. Tanaka, M. Moriya, Y. Takahashi, Y. Urai, K. Sawada, K. Higuchi, and K. Yamazaki for fruitful discussion and technical supports. Test circuits used in this study were fabricated using the AIST-STP 2 process in the Superconducting Clean Room (CRAVITY) at the National Institute of AIST. The stable supply of liquid helium from the Coordinated Center for UEC Research Facilities is also acknowledged.

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