Doctoral Thesis

Research on High Switching Frequency Resonant Converters: Output Voltage Regulation, Power Stage Design, and EMI Noise Reduction

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Abstract

A resonant converter has been widely used in various industrial applications, since it has high power conversion efficiency. The increase of the power density is necessary to obtain high cost-effectiveness and design freedom on the electric products. A high switching frequency operation can be an effective method to obtain the high power density of power converters. In this dissertation, three topic will be discussed to obtain the high power conversion efficiency and the high power density for the resonant converter, as follows:

First, the power stage and feedback loop are designed for the high switching frequency operation. The power stage is designed to obtain the high power conversion efficiency at the high switching frequency operation. In addition, the feedback loop is designed to guarantee the stability.

Second, the control algorithm is proposed to obtain the tight output voltage regulation at the high switching frequency operation. The operational principle and design of control algorithm are analyzed to obtain the tight output voltage regulation.

Third, the spread spectrum technique (SST) will be applied to the resonant converter to reduce the electromagnetic interference (EMI), which can improve the power density with small EMI filter size. In this research, the design constraint to implement the SST on the resonant converter is analyzed to obtain the dual functionality properly. In addition, the control algorithms are proposed to achieve tight output voltage regulation and EMI reduction, simultaneously. All the proposed design considerations and control algorithms are verified with the simulation and experimental results.

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I. Introduction

Recently, the high switching frequency operation is widely applied to the switching mode power supplies (SMPS) to improve the power density. In addition, a wide-band gap (WBG) switching devices enables high switching frequency operation up to several MHz compared to conventional silicon based switching devices. However, there are several issues to implement the high power density with high power conversion efficiency and high power quality. First, the parasitic component on the resonant tank induces large power loss on the power converter. Second, the loop gain should be properly designed to obtain the stability and fast dynamic performance. Third, the power converters has to satisfy an electro-magnetic interference (EMI) standard using the EMI filter. The EM noise reduction of the power converter is necessary to obtain the small sized EMI filter which can improve the power density in terms of the total power conversion system. Therefore, this dissertation introduces the solution to overcome the conventional limitation and constraints. First, the high switching frequency operation is applied to the resonant converter to achieve the soft switching capability. The power stage is analyzed and designed for the high power conversion efficiency at the high switching frequency operation. Second, the loop gain and feedback loop are analyzed and designed to obtain the stability of the converter and fast dynamic performance. The field-programmable gate array (FPGA) can be designed to improve the control bandwidth with small time-delay. Third, the control algorithm is proposed to obtain the tight output voltage regulation. Forth, the spread spectrum technique (SST) is applied to the resonant converters to mitigate the EM noise reduction.

The LLC resonant converter is widely applied to several industrial applications, because it has soft-switching capability, easy control implementation, and simple structure. In the conventional low switching frequency, the model of the LLC resonant converter ignores parasitic components in the resonant tank. However, when the switching frequency increases up to MHz, the secondary leakage inductance should be considered in the design of the power stage because the resonant tank component values become smaller and the parasitic components become more significant. Without considering the secondary leakage inductance, there is a significant design error, which can induce high switching loss, high circulating current, and high conduction loss. In this dissertation, the proper power stage design is proposed to obtain the high power conversion efficiency which considers the parasitic components.

In terms of control, the DSPs and microprocessors are widely used to generate high precision PWM signals under high switching frequency operation. They generally have high noise immunity and can implement complex control technique. However, the limited computation speed of the digital controller cannot cover the required control bandwidth for high switching frequency operation, which results in low dynamic performance and stability of the power converter. Therefore, a time delay effect caused by the limited performance of the digital controller should be considered to obtain a proper small signal model that includes feedback and control delay. In this dissertation, the loop gain for high switching

frequency is designed to achieve the stability and fast dynamic performance. In addition, FPGA is applied to reduce the time-delay effect.

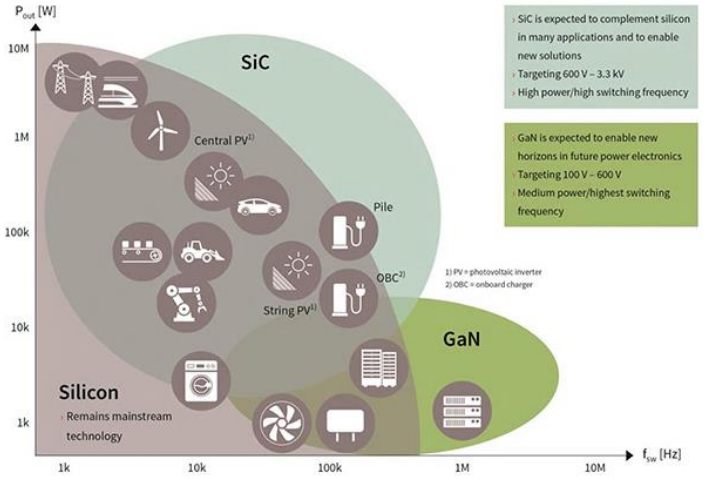
In terms of the output voltage regulation, the digitally controlled LLC resonant converter has a limited frequency resolution, since the digital controller is implemented using a limited clock speed to generate the PWM signals. Moreover, the limited frequency resolution can lead to performance degradation at high switching frequencies by a single frequency step in the digital signal processor (DSP). For example, a general-purpose DSP (TI TMS320F28335) provides 150 million instructions per second (MIPS) performance. However, it does not have high enough frequency resolution for a pulse frequency modulation (PFM) operating at several mega-hertz switching frequency. This limited frequency resolution induces high variation in the input-output voltage gain at high switching frequencies, which causes high output voltage ripple in the LLC resonant converter. Moreover, it results in high fluctuation of the primary- and secondary-side currents, which induces abnormal oscillations and high current stress on the passive components. In this dissertation, the PFM-PWM hybrid control algorithm is proposed to improve the output voltage regulation performance.

In terms of the EMI reduction, the EMI filter has been widely used to suppress the EM noise of the power converters. However, the EMI filter induces bulky and poor cost-effectiveness on the electric products. The SST can be a solution to suppress the EM noise with only control algorithms. In addition, it has been widely applied to the power converters, such as buck, boost, flyback converters. However, the available topologies are limited to implement the SST, because the SST requires large switching frequency variation. In this research, the SST is applied to the resonant converters. The resonant converter has sensitive voltage gain according to the switching frequency variation. Therefore, the power stage and the control algorithm are required to obtain the tight output voltage regulation and the EM noise reduction. From this section, the power density can be improved with the small EMI filter.

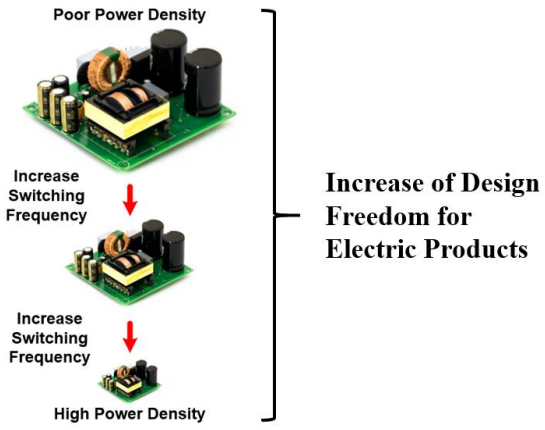
This dissertation considers the high power density of the resonant converter with the high switching frequency operation and small EM noise reduction. It covers the power stage design, control loop design, and control algorithms for the high power conversion efficiency and tight output voltage regulation at the high switching frequency operation. In addition, the EM noise reduction method of the resonant converter is proposed to improve the power density in terms of the total power system. All the proposed design and algorithm are analyzed in theoretical method. The simulation and experimental results verify the proposed design and algorithm.

II. Power Stage and Feedback Loop Design

The high switching frequency operation is one of methods to increase the power density with small passive components. Recently, the high switching frequency operation of the switch mode power supplies (SMPS) is available with the advance of the wide band-gap (WBG) devices, such as gallium nitride (GaN) and silicon carbide (SiC) [1]. Fig 1 (a) shows the operating range of the WBG devices [2]. Fig. 1 (b) shows the size decrease of electronic products by the high power density converter, which increases the design freedom of electronic products. Fig 1 (a) shows the operating range of the WBG devices [2]. Fig. 1 (b) shows the size decrease of electronic products by the high power density converter, which increases the design freedom of electronic products. In this section, the power stage and loop gain are designed to obtain the high power conversion efficiency and stability at the high switching frequency operation.



(a)



(b)

Fig. 1 High power density: (a) high switching frequency with WBG devices, (b) increase of design freedom with high power density converter.

2.1 Limitation of Conventional Model of LLC Resonant Converter

In conventional low-frequency applications, the model of the LLC resonant converter ignores parasitic components in the resonant tank, such that the model includes only a primary leakage inductance, a magnetizing inductance, and a resonant capacitance. Using the conventional model, a power stage design method has been well derived using first harmonic approximation (FHA), which can obtain the input-output voltage gain, resonant tank impedance, proper magnetizing inductance, transformer turn ratio [3]-[16]. The conventional LLC resonant converter has additional inductor to obtain the desired resonant inductance value. However, when the switching frequency increases up to MHz, the resonant inductance is integrated into the transformer [1]. Therefore, the secondary leakage inductance should be considered in the design of the power stage. Without considering the secondary leakage inductance, there is a significant design error, which can induce high switching loss, high circulating current, and high conduction loss.

In previous research, the secondary leakage inductance was considered to design the power stage of the LLC resonant converter [17], [18]. They took into account the model error of the input-output voltage gain due to the secondary leakage inductance. However, one of them is focused on unbalanced secondary current by unbalanced leakage inductance [17], and another only shows the change of voltage gain characteristics between the modified model and the conventional model [18]. The derived voltage gain in the previous research has significant design error with the consideration of only primary leakage inductance. In addition, previous research uses a separated winding structure in the transformer, which physically induces high secondary leakage inductance caused by low coupling coefficient.

2.1.A Voltage Gain and Impedance

The input-output voltage gain and the resonant impedance is important as the design criteria to obtain high power conversion efficiency in the LLC resonant converter. The conventional input-output voltage gain and resonant tank impedance are well analyzed using the FHA model, as follows:

$$M_{gain}(f_n)=\left|\frac{\lambda^{-1}\cdot f_n^{\,2}}{(\lambda^{-1}+1)f_n^{\,2}-1+j(f_n^{\,2}-1)f_n\cdot Q\cdot\lambda^{-1}}\right| \tag{1}$$

$$Z(f_n)=\left|\frac{jf_n}{\lambda+jf_nQ}-\frac{f_n^{\,2}-1}{jF_n}\right| \tag{2}$$

$$\lambda=\frac{L_r}{L_m},\quad f_{r1}=\frac{1}{2\pi\sqrt{L_rC_r}},\quad f_{r2}=\frac{1}{2\pi\sqrt{(L_r+L_m)C_r}},\quad f_n=\frac{f_s}{f_{r1}},\quad Q=\frac{\sqrt{L_rC_r^{-1}}}{R_{eq}},\ R_{eq}=\frac{8n^2}{\pi^2}R_o \tag{3}$$

where R_o is the output load resistance, R_{eq} is the resistive load of the resonant network at the FHA model, L_m is the magnetizing inductance, L_r is the primary leakage inductance, C_r is the resonant capacitor, f_{r1} is the series resonant frequency, f_{r2} is the parallel resonant frequency, f_s is the switching frequency, Q is

the quality factor, n is transformer turn ratio. Equation (1) shows that the conventional model that has a unity gain at f_{r1} and the imaginary impedance is zero at f_{r2}. At the early several kilo-hertz switching frequency, the resonant inductance is designed with the sum of the resonant inductance and the leakage inductance of the transformer. Therefore, the secondary leakage inductance is negligible in the converter model. However, when switching frequency increases up to mega-hertz, the secondary leakage inductance is large enough to be considered as one of the resonant components.

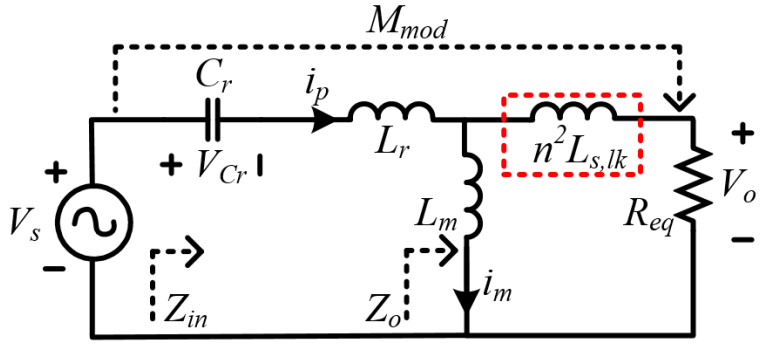
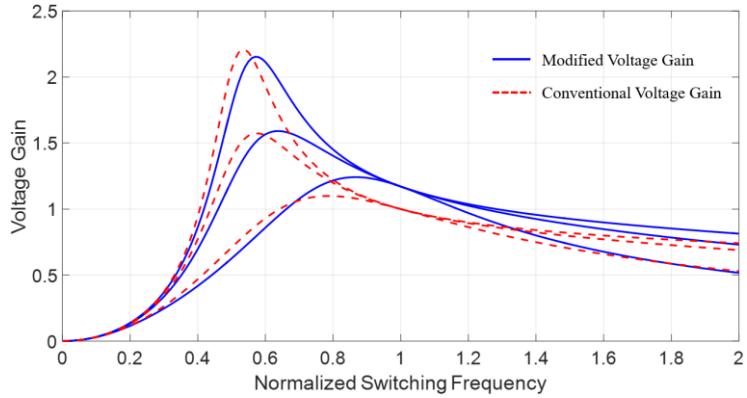
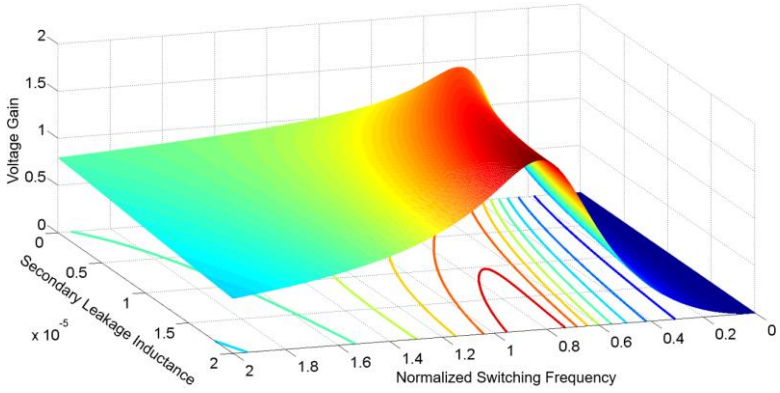


Fig. 2 Modified FHA model of LLC resonant converter with additional secondary leakage inductance.



(a)



(b)

Fig. 3 Input-output voltage gain curve of the LLC resonant converter: (a) Voltage gain difference between the modified and the conventional converter model, (b) Voltage gain surface according to the secondary leakage inductance at the switching frequency.

The modified FHA model with the secondary leakage inductance is shown in Fig. 2. From this model, the input-output voltage gain and the resonant tank impedance can be updated, as follows:

$$M_{\mathrm{mod}}(s)=\frac{V_{o,FHA}}{V_{in,FHA}}=\frac{Z_o(s)}{Z_{in}(s)}\cdot\frac{R_{eq}}{sn^2L_{s,lk}+R_{eq}} \tag{4}$$

$$Z_o(s)=\frac{sL_mR_{eq}+s^2L_mn^2L_{s,lk}}{sL_m+sn^2L_{s,lk}+R_{eq}} \tag{5}$$

$$Z_{in}(s)=sL_r+\frac{1}{sC_r}+Z_o \tag{6}$$

$$M_{\mathrm{mod}}(f_n)=\left|\frac{f_n{}^2C_rR_{eq}\omega_r}{jf_n{}^3(1+\beta)\omega_r{}^2+f_n{}^2C_rR_{eq}(1+\lambda)\omega_r-jf_n(1+\beta)\omega_r{}^2-R_{eq}\omega_r{}^3L_m{}^{-1}}\right| \tag{7}$$

$$Z_{\mathrm{mod}}(f_n)=\left|\frac{j(-f_n{}^2C_rL_r+\omega_r{}^2)}{f_n\omega_r{}^2}+\frac{-f_n{}^2C_rL_mn^2L_{s,lk}+jf_nC_rL_mR\omega_r}{C_rRZ_c\omega_r{}^2+jf_n(L_m+n^2L_{s,lk})\omega_r{}^2}\right| \tag{8}$$

$$f_{r1,\mathrm{mod}}=\frac{1}{2\pi\sqrt{(L_r+n^2L_{s,lk}\,\|\,L_m)C_r}},\ f_{r2,\mathrm{mod}}=\frac{1}{2\pi\sqrt{(L_r+L_m)C_r}},\ \omega_r=2\pi f_{r1,\mathrm{mod}},\ \omega_{r1}=2\pi f_{r2,\mathrm{mod}}$$
$$Q=\frac{Z_c}{R_o},\ Z_c=\sqrt{\frac{L_r+L_m\,\|\,n^2L_{s,lk}}{C_r}},\ \beta=\frac{n^2L_{s,lk}}{L_m} \tag{9}$$

where $L_{s,lk}$ is the secondary leakage inductance, $f_{r1,mod}$ and $f_{r2,mod}$ are the series and parallel resonant frequency modified by the proposed model, respectively. The coupling coefficient of the transformer is measured with the series-aiding series-opposing method [19]. The modified series resonant frequency $f_{r1,mod}$ affected by the secondary leakage inductance is different than the conventional resonant frequency f_{r1}, while the modified parallel resonant frequency $f_{r2,mod}$ equals the conventional resonant frequency f_{r2}. The updated voltage gain of the proposed converter model has a higher magnitude at $f_{r1,mod}$ than the unity one of the conventional model at f_{r1}, as shown in Fig. 3 (a). In addition, the updated voltage gain has the same magnitude at $f_{r1,mod}$ as the conventional voltage gain at f_{r1}. As the secondary leakage inductance increases, the magnitude of the updated voltage gain increases at $f_{r1,mod}$, as shown in Fig. 3 (b).

The resonant inductance at the conventional 100 kHz switching frequency is designed with the additional resonant inductance and leakage inductance of the transformer. However, the resonant inductance at the 1 MHz switching frequency is designed with the leakage inductance of the transformer to obtain high power density. Fig. 4 shows the effect of the secondary leakage inductance. At the conventional 100 kHz switching frequency condition condition, the additional resonant inductance and the primary leakage inductance are 50 μH and 25 μH, respectively. At 1 MHz switching frequency condition, the primary leakage inductance is 7.5 μH. Using the modified model, the input-output voltage gain is slightly higher than the unity gain (1.02) at $f_{r1,mod}$ with the conventional 100 kHz switching frequency. However, with 1 MHz switching frequency, the gain increases significantly (1.18) at $f_{r1,mod}$.

The gain increment induces significant design error which can introduce high circulating current and serious switching loss. Therefore, magnetics design, such as the transformer turn ratio and the magnetizing inductance should be achieved using the proposed converter model [20].

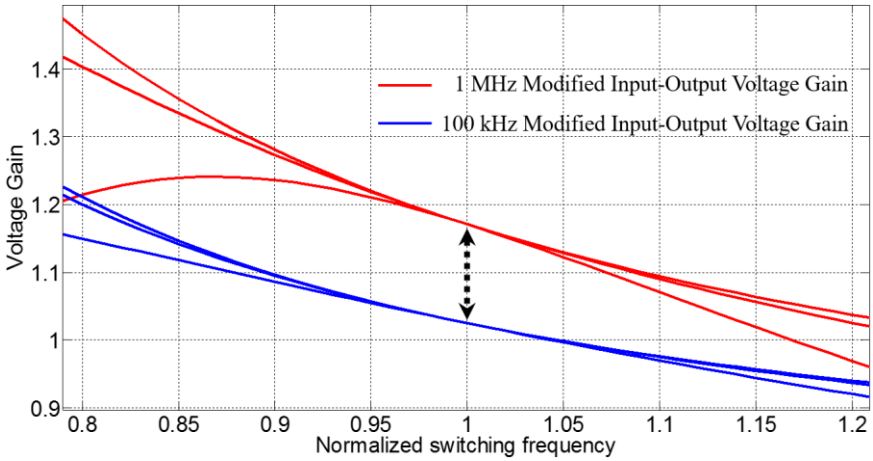


Fig. 4 Comparison of modified voltage gain according to the resonant frequency.

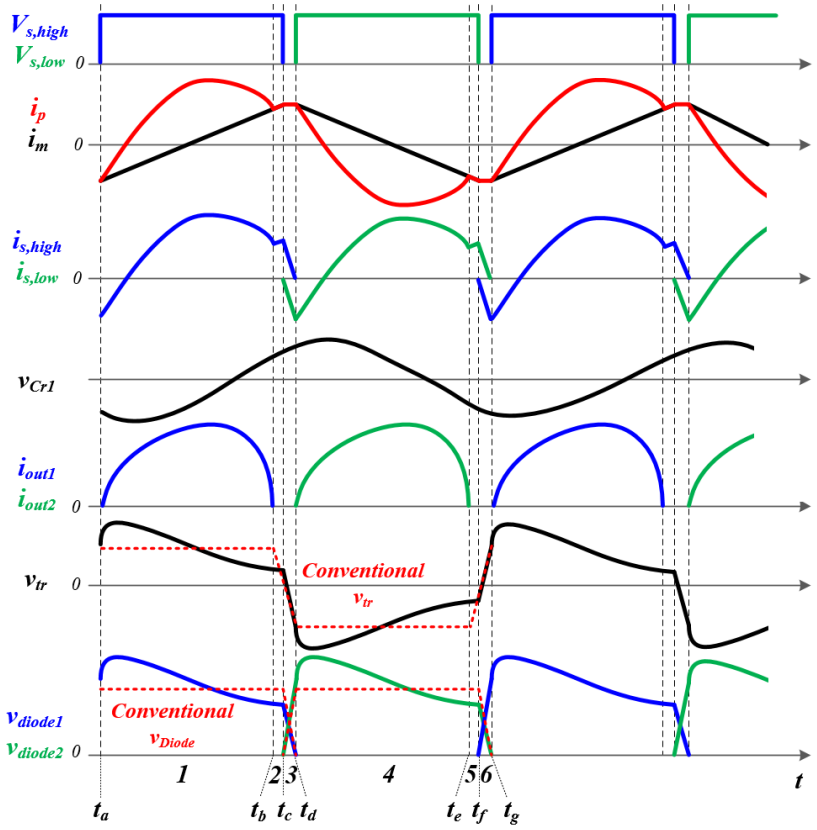


Fig. 5 Theoretical operating waveforms of the modified LLC resonant converter model.

2.1.B Operational Principles

Theoretical operating waveforms of the proposed converter model are different from the conventional waveforms, as shown in Fig. 5. The operating waveforms are derived into six modes. Mode 1, 2, and 3

are derived from the operation of the high-side switch, and Mode 4, 5, and 6 are related to the operation of the low-side switch. Mode 1 and 4 show resonance with L_r, L_m, $L_{s,lk}$ and C_r. Mode 2 and Mode 5 show resonance with L_m, L_r, and C_r. Mode 3 and Mode 6 represent dead time durations.

Mode 1 [$t_a - t_b$]: During this mode, electric power is transferred from the primary side to the secondary side through the transformer. In this mode, $L_{s,lk}$ and L_m participates in the resonance between L_r and C_r. Assuming negligible dead time duration, the primary current $i_r(t)$, the magnetizing current $i_m(t)$, the secondary current $i_{l2}(t)$, and the resonant capacitor's voltage $V_{cr}(t)$ can be derived as follows:

$$i_r(t) = C_r\omega_r\alpha\sin(\omega_r t) + C_r{\omega_r}^2\beta\cos(\omega_r t) \tag{10}$$

$$\alpha = V_{in} - V_{cr,ini} - nV_o + \frac{n^3 L_{s,lk} V_o}{n^2 L_{s,lk} + L_m},\quad \beta = n^2 L_{s,lk} I_{l2,ini} + L_r I_{r,ini} + \frac{n^2 L_{s,lk} L_m I_{m,ini}}{n^2 L_{s,lk} + L_m} - \frac{n^4 {L_{s,lk}}^2 I_{l2,ini}}{n^2 L_{s,lk} + L_m} \tag{11}$$

$$i_m(t) = \frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m} i_r(t) + \frac{nV_o}{L_m + n^2 L_{s,lk}} t + \frac{L_m}{L_m + n^2 L_{s,lk}} I_{m,ini} - \frac{n^2 L_{s,lk}}{L_m + n^2 L_{s,lk}} I_{l2,ini} \tag{12}$$

$$i_{l2}(t) = n\{i_r(t) - i_m(t)\} \tag{13}$$

$$V_{cr}(t) = V_{cr,ini} + \alpha - \alpha\cos(\omega_r t) + \omega_r\beta\sin(\omega_r t) \tag{14}$$

where $V_{cr,ini}$ is the initial voltage across C_r, $I_{r,ini}$ is the initial primary current, $I_{m,ini}$ is the initial magnetizing current, and $I_{l2,ini}$ is the initial secondary current. Assuming that the $i_r(t)$ and $i_m(t)$ are the same during the dead time, $I_{l2,ini}$ becomes zero. Therefore, $I_{r,ini}$ and $I_{m,ini}$ can be derived as follows:

$$I_{r,ini}(t_a) = I_{m,ini}(t_a) \cong C_r{\omega_r}^2\beta = \frac{n^2 L_{s,lk} C_r {\omega_r}^2 \beta}{n^2 L_{s,lk} + L_m} + \frac{M_{\mathrm{mod}} nV_o}{L_m + n^2 L_{s,lk}} \frac{T_s}{4} + \frac{n^2 L_{s,lk} L_m I_{m,ini}}{n^2 L_{s,lk} + L_m} \tag{15}$$

$$I_{r,ini}(t_a) = I_{m,ini}(t_a) \cong -\frac{M_{\mathrm{mod}} nV_o}{L_m} \cdot \frac{T_s}{4} \tag{16}$$

In addition, the secondary voltage equation can be derived using the flux balancing law in the transformer as follows:

$$V_{tr} = \frac{L_m}{L_m + n^2 L_{s,lk}} nV_o + \frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m}\left\{C_r\omega^2\alpha\cos(\omega_r t) - C_r\omega^3\beta\sin(\omega_r t)\right\} \tag{17}$$

$$V_{s,lk} = L_{s,lk}\frac{di_{l2}(t)}{dt} = nL_{s,lk}\left[\left(1 - \frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m}\right)\left\{C_r\omega^2\alpha\cos(\omega_r t) - C_r\omega^3\beta\sin(\omega_r t)\right\} - \frac{nV_o}{n^2 L_{s,lk} + L_m}\right] \tag{18}$$

where V_{tr} is the voltage across the magnetizing inductance and $V_{s,lk}$ is the voltage across the secondary leakage inductance. Equation (17) and (18) show that the large secondary leakage inductance and the high switching frequency can induce significant voltage fluctuations in the secondary side, which should be considered in designing the secondary side rectifier.

Mode 2 [t_b - t_c]: During this mode, the electric power is not transferred to the secondary side. In this section, $L_{s,lk}$ does not participate in the resonance. The primary current $i_r(t)$ and the resonant capacitor

voltage $v_{cr}(t)$ can be described as shown in (19) and (20), respectively.

$$i_r(t) = i_m(t) = I_{r,ini}\cos(\omega_{r1}t) + C_r\omega_1(V_{in} - V_{cr,ini})\sin(\omega_{r1}t) \tag{19}$$

$$V_{cr}(t) = (L_r + L_m)\omega_{r1}I_{r,ini}\sin(\omega_{r1}t) + (V_{cr,ini} - V_{in})\cos(\omega_{r1}t) + V_{in} \tag{20}$$

The soft commutation on the output rectifier can be achieved at the end of Mode 2, which reduces the rectifier's switching loss during the high switching frequency operation.

Mode 3 [t_c - t_d]: This mode is a dead time duration. In Mode 3, electric power is not transferred from the primary side to the secondary side. The primary current charges and discharges the output capacitance of the primary MOSFETs, which makes the MOSFETs operate in ZVS. After this process, the primary current will pass through the antiparallel diode before the MOSFET's turn-on.

Mode 4 to Mode 6 [t_d - t_g]: Mode 1 to Mode 3 repeats Mode 4 to Mode 6, respectively, every half switching cycle with the low-side MOSFET. During Mode 4, $i_p(t)$, $i_m(t)$, and $V_{cr}(t)$ can be derived as follows:

$$i_r(t) = C_r\omega_r(A')\sin(\omega_r t) + C_r\omega_r{}^2 B\cos(\omega_r t) \tag{21}$$

$$\alpha' = -V_{cr,ini} + nV_o - \frac{n^3 L_{s,lk}V_o}{n^2 L_{s,lk} + L_m} \tag{22}$$

$$i_m(t) = -\frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m}i_r(t) - \frac{nV_o}{L_m + n^2 L_{s,lk}}t - \frac{L_m}{L_m + n^2 L_{s,lk}}I_{m,ini} + \frac{n^2 L_{s,lk}}{L_m + n^2 L_{s,lk}}I_{l2,ini} \tag{23}$$

$$i_{l2}(t) = n\{i_r(t) - i_m(t)\} \tag{24}$$

$$V_{cr}(t) = V_{cr,ini} + \alpha' - \alpha'\cos(\omega_r t) + \omega\beta\sin(\omega_r t) \tag{25}$$

$$V_{tr}(t) = \frac{L_m}{L_m + n^2 L_{s,lk}}nV_o + \frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m}\{C_r\omega^2\alpha'\cos(\omega_r t) - C_r\omega^3\beta\sin(\omega_r t)\} \tag{26}$$

$$V_{s,lk}(t) = L_{s,lk}\frac{di_{l2}(t)}{dt} = nL_{s,lk}\left[\left(1 - \frac{n^2 L_{s,lk}}{n^2 L_{s,lk} + L_m}\right)\{C_r\omega^2\alpha'\cos(\omega_r t) - C_r\omega^3\beta\sin(\omega_r t)\} - \frac{nV_o}{n^2 L_{s,lk} + L_m}\right] \tag{27}$$

During Mode 5, $i_p(t)$ and $V_{cr}(t)$ can be described as shown in (28) and (29), respectively.

$$i_r(t) = i_m(t) = I_{r,ini}\cos(\omega_{r1}t) - C_r\omega_1 V_{cr,ini}\sin(\omega_{r1}t) \tag{28}$$

$$V_{cr}(t) = -(L_r + L_m)\omega_{r1}I_{r,ini}\sin(\omega_{r1}t) + V_{cr,ini}\cos(\omega_{r1}t) \tag{29}$$

Mode 6 is also a dead time duration. Using the model analysis with the secondary leakage inductance, the design accuracy of the converter's power stage can be improved for the high power conversion efficiency.

2.2 Power Stage Design for High Switching Frequency

In this section, power stage design such as the primary-secondary turn ratio, the magnetizing inductance, and the secondary diode selection will be discussed using the model analysis results presented in the previous section. All the design parameters will be addressed using the modified LLC resonant converter model.

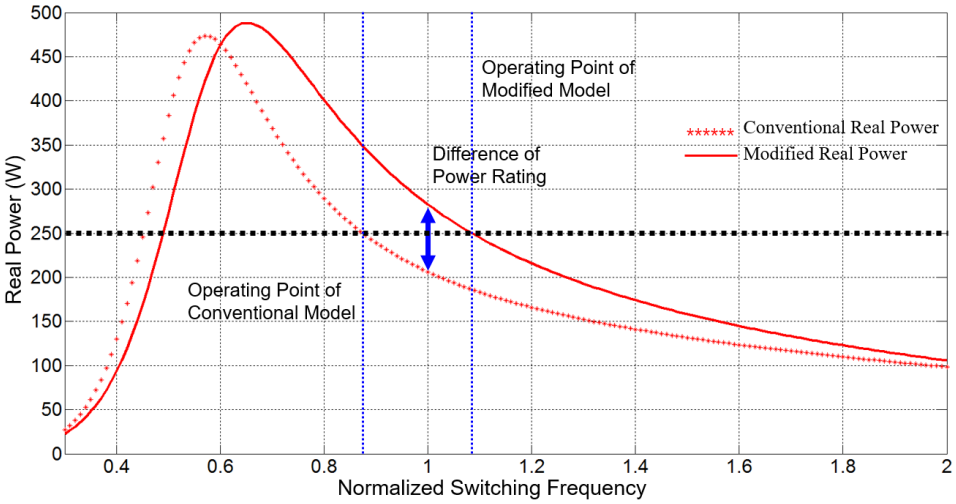


Fig. 6 Difference of the operating point between the conventional and modified converter model at the same power rating.

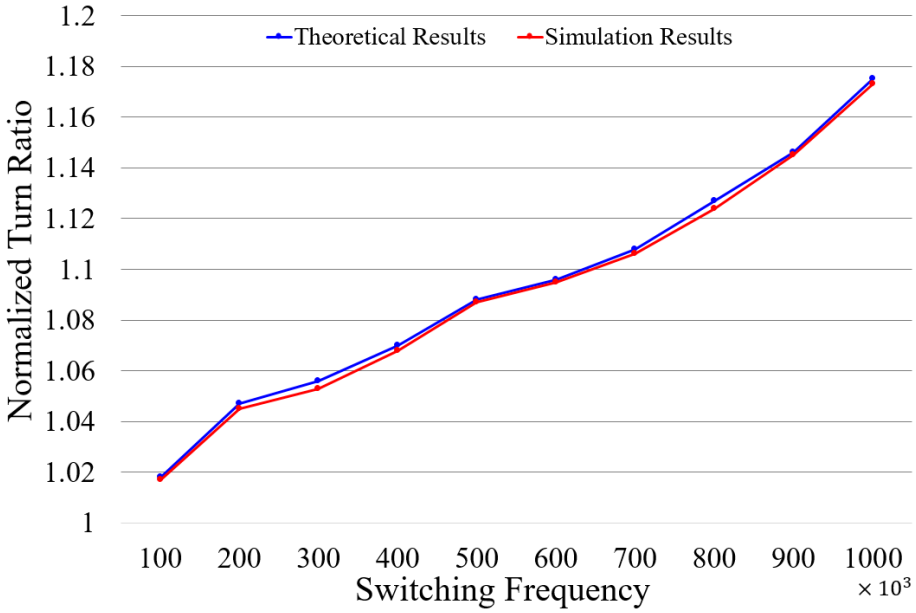


Fig. 7 Proposed transformer turn ratio according to the switching frequency.

2.2.A Transformer Turn Ratio for High Switching Frequency

The soft commutation of the output rectifier is required to reduce its reverse conduction loss which is proportional to the switching frequency. The LLC resonant converter generally operates between the maximum input-output voltage gain and the series resonant frequency to obtain soft switching capabilities in the primary MOSFETs and the secondary rectifiers. The conventional 100 kHz switching

frequency converter requires additional one or two primary turn number to compensate slightly higher voltage gain than the unity gain at the series resonant frequency, which implements the soft commutation on the output rectifier. However, the high switching frequency LLC resonant converter cannot implement the soft commutation in the output rectifier with the additional one or two primary turn number, because high switching frequency operation has more significant voltage gain boost at the series resonant frequency, as shown in Fig. 4. Fig. 6 shows the difference of operating power between the conventional model and the proposed modified model. This shows that the modified model cannot achieve soft commutation in the output rectifier by the conventional method of adding one or two primary turns in the transformer.

There are two solutions to obtain soft commutation in the output rectifier. One is adjusting the primary side turn number. The other is adjusting the secondary side turn number. The primary side turn number increment has more design freedom and more reduction of the maximum flux density to protect transformer saturation. However, this large turn number induces high winding resistance [21], [22]. The secondary turn number reduction has less design freedom to obtain proper turn ratio than the case of the primary turn number increment. Therefore, the modification of the primary turn number can be better to compensate the voltage gain boost under the high frequency operation.

The proposed transformer turn ratio can be calculated as follows:

$$n_{\mathrm{mod}} \geq \frac{N_p}{N_s} = \frac{V_{in,\max}}{2(V_o + V_F)} \cdot M_{\mathrm{mod}}(f_{r1,\mathrm{mod}}) \tag{30}$$

where n is the primary-secondary turn ratio, N_p is the primary side turn number, N_s is the secondary side turn number, V_F is the forward voltage drop of output rectifier, $V_{in,max}$ is the maximum input voltage, and $M_{mod}(f_{r1,mod})$ is the modified input-output voltage gain at $f_{r1,\mathrm{mod}}$. In (30), the term $V_{in,max}/2(V_o+V_F)$ is the conventional transformer turn ratio criterion for the LLC resonant converter. This voltage gain is updated in (30) using the modified voltage gain in (7), which makes the modified turn ratio a function of the switching frequency. If the secondary leakage inductance and the quality factor are equal to the modified converter model according to the switching frequency, the minimum transformer turn ratio for the soft commutation of the output rectifier can be calculated as shown in Fig. 7. This shows that the higher resonant frequency requires a higher transformer turn ratio. From (30), the modified primary turn number can be derived as follows:

$$N_{p,\mathrm{mod}} = \frac{M_{\mathrm{mod}}(f_{r1,\mathrm{mod}})V_{in}}{2 f_{r1,\mathrm{mod}} A_{\min} \Delta B_{\max}} \tag{31}$$

where A_{min} is the cross sectional area of the transformer and ΔB_{max} is the maximum flux density.

2.2.B Magnetizing Inductance for Soft-Switching Capability

The ZVS capability on the primary MOSFETs is one of the significant advantages of the LLC

resonant converter for high power conversion efficiency. ZVS can be achieved using proper dead time and the magnetizing inductance by inducing the amount of the primary current that charges and discharges the output capacitance of the MOSFETs. The proper magnetizing inductance induces a smaller magnetizing current which leads to smaller circulating current and conduction loss in the primary side. Also, proper dead time duration is required to obtain ZVS, operational stability, and lower conduction loss [10].

To achieve ZVS, the magnetizing current should be higher than the minimum primary current required to charge and discharge the output capacitance of the MOSFETs, as follows:

$$I_{m,ini}(t_a) \geq I_{ZVS,\min} = \frac{2C_{eq}V_{in}}{t_{dt}} \tag{32}$$

where C_{eq} is the output capacitance of the primary MOSFETs, t_{dt} is the dead time duration, $I_{m,ini}(t_a)$ is the magnetizing current at t_a, and $I_{zvs,\min}$ is the minimum primary current for ZVS capability. The magnetizing current after the dead time duration can be obtained as follows:

$$I_{m,ini}(t_a) = \frac{V_{in}}{8L_m f_{s,\max}} \tag{33}$$

where $f_{s,max}$ is the maximum switching frequency. Equation (34) shows that $I_{m,ini}(t_a)$ is a function of L_m, $f_{s,max}$, and V_{in}. From (33), the minimum dead time duration can be derived in (34).

$$t_{dt} \geq \frac{2V_{in} \cdot \max\{C_{S1}, C_{S2}\}}{\max\{|i_p(t_{dt})|\}} = 16C_S f_{s,\max} L_m \tag{34}$$

Using (34), the magnetizing inductance can be designed as follows:

$$L_m \leq \frac{t_{dt}}{16C_S f_{s,\max}} = \frac{t_{dt}}{16C_s f_r} \tag{35}$$

where (35) is satisfied only when $f_s \leq f_r$. However, it does not consider the modified input-output voltage gain effect of the secondary leakage inductance. The modified gain curve is bigger than the conventional gain curve, especially, at high operating frequencies. Therefore, the ZVS criterion of (35) has a significant error at high operating frequencies.

Using (7) and (34), the minimum dead time duration can be updated with the modified voltage gain as shown in (36).

$$t_{dt,n} \geq \frac{2V_{in} \cdot \max\{C_{S1}, C_{S2}\}}{\max\{|i_p(t_{dt})|\}} = \frac{16C_S f_{r1,\mathrm{mod}} L_m}{M_{\mathrm{mod}}(f_{r1,\mathrm{mod}})} \tag{36}$$

From (36), the updated dead time duration which guarantees ZVS of the primary MOSFETs is shorter than that of the conventional one. In addition, the magnetizing inductance criterion for satisfying the ZVS condition can be updated as shown in (37).

$$L_{m,n} = \frac{M_{\mathrm{mod}}(f_{r1,\mathrm{mod}})t_{dt,n}}{16 f_{r1,\mathrm{mod}} C_{eq}} \tag{37}$$

The updated magnetizing inductance is proportional to $M_{mod}(f_{r1,\mathrm{mod}})$, which shows that higher magnetizing inductance can be used at a high switching frequency than the conventional model. Using (36) and (37), the updated magnetizing inductance is around ten percent higher than the conventional one to guarantee ZVS, which shows that the conventional gain model induces large circulating currents and high conduction losses in a practical manner, as shown in Fig. 8.

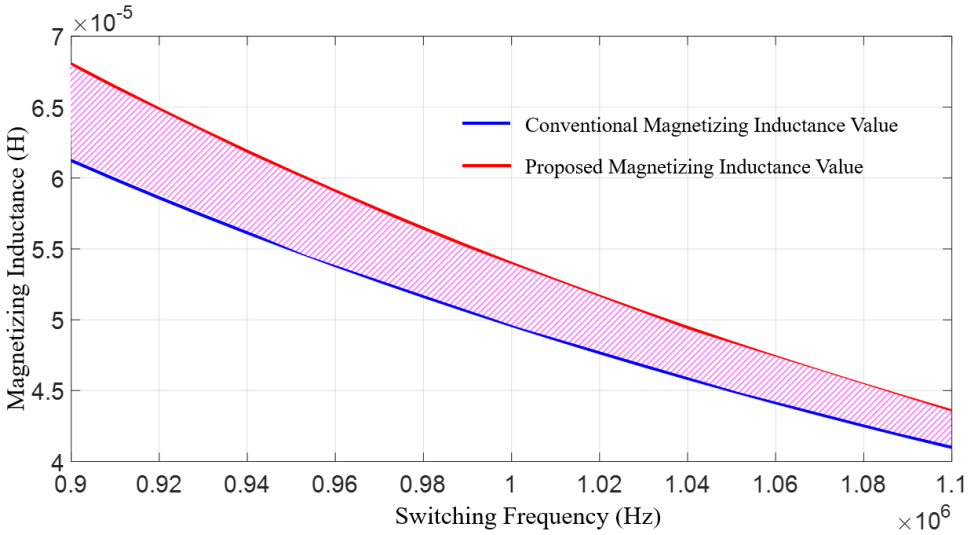


Fig. 8 Comparison of magnetizing inductance for ZVS capability between proposed model and conventional model.

2.2.C Secondary Diode Rectification for High Frequency Operation

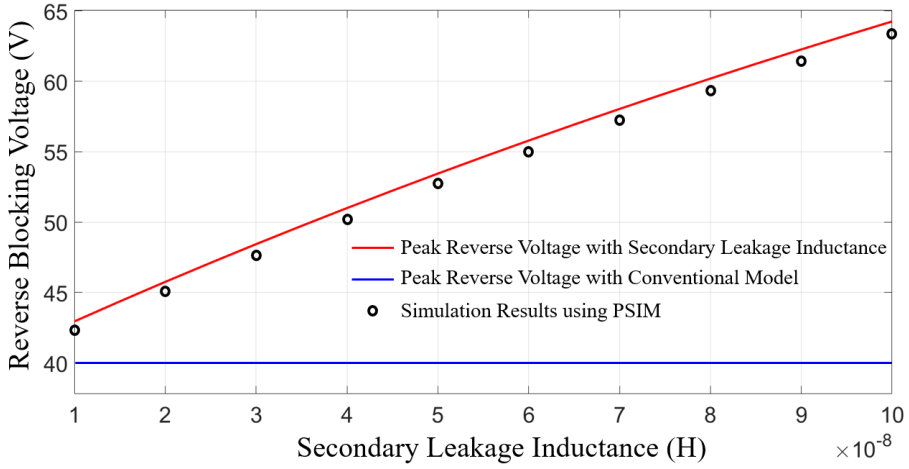
The selection of the secondary diode rectifier is important to implement high switching frequency operation with small conduction loss. In addition, the selected diode has to guarantee enough reverse blocking voltage to protect the diode breakdown. A Schottky diode is widely used for high switching frequency applications, since it has low forward voltage drop and no reverse recovery issues, which makes small conduction and turn-off losses. However, the reverse blocking voltage of the Schottky diode is relatively small. Therefore, proper secondary diode selection that considers the practical reverse blocking voltage is important to improve the operational stability and power conversion efficiency of the power converter.

The reverse blocking voltage of the LLC resonant converter's output rectifier can be described as follows:

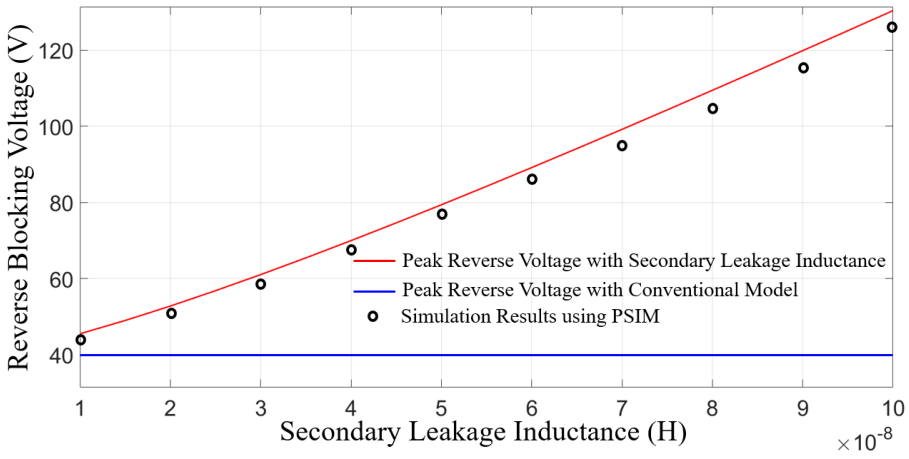
$$V_D \cong V_{s,tr} + V_o = 2V_o \tag{38}$$

where $V_{s,tr}$ is the voltage across the transformer's secondary winding which is almost the same as the output voltage at the series resonant frequency. However, (38) does not consider the secondary leakage

inductance which can increase the reverse voltage of the output rectifier. At the high switching frequency, the LLC resonant converter has to include the secondary leakage inductance which can induce large reverse voltage variations, as shown in (18) and Fig. 5. By differentiating (18), the peak magnitude of the voltage variation across the secondary leakage inductance can be derived as follows:



(a)



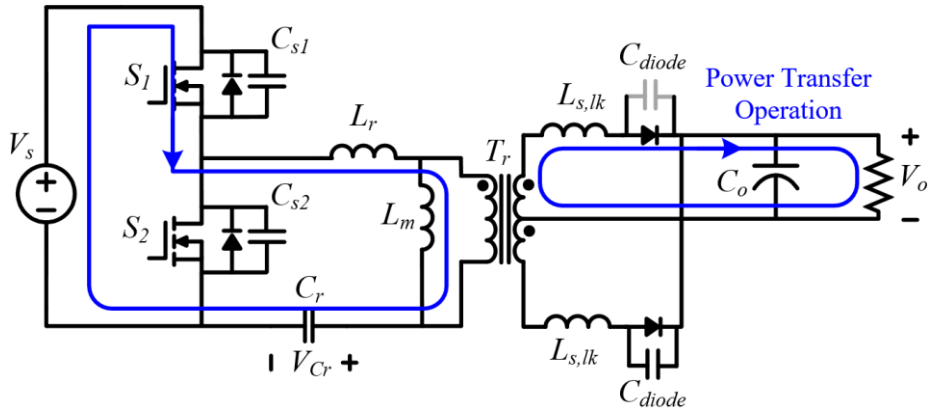
(b)

Fig. 9 Practical blocking voltage of the rectifying diode according to the secondary leakage inductance: (a) considering only secondary leakage inductance, (b) considering secondary leakage inductance and diode capacitor.

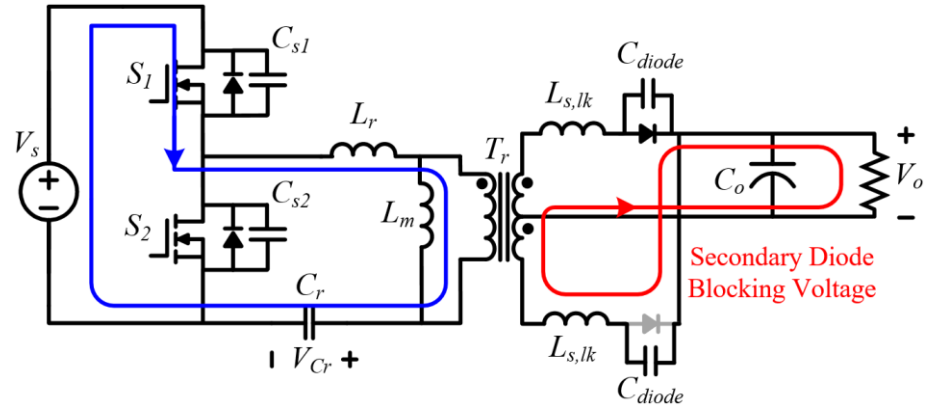
$$V_{s,lk,\max} \cong nL_{s,lk}\left[\left(1-\frac{n^2L_{s,lk}}{n^2L_{s,lk}+L_m}\right)\cdot C_r\alpha\omega^2-\frac{nV_o}{n^2L_{s,lk}+L_m}\right] \tag{39}$$

The magnitude of the voltage across the secondary leakage inductance can be reduced by using a small secondary leakage inductance value and low switching frequency, as shown in Fig. 9 (a). If the high side switch is turned on to transfer electric power from the primary to the secondary, one of the

output rectifier diodes is conducting and another is blocked, as shown in Fig. 10. In this condition, the parasitic capacitance of the blocking diode and the secondary leakage inductance participate in the secondary resonance, which makes high peak reverse voltage in the secondary diode. The magnitude of the resonant current can be calculated by using the voltage variation in the secondary leakage inductance as follows:



(a)



(b)

Fig. 10 Current paths of the secondary rectifying diode: (a) forward powering path, (b) reverse blocking path.

$$I_{res,\max} = \frac{V_{s,lk,\max}}{R_{out} + R_s} \tag{40}$$

where R_s is the parasitic resistance on the secondary power stage. The resonant current's magnitude is determined by total resistance of the secondary power stages, which is composed of transformer primary and secondary resistance, and output load impedance. From the resonant current, the resonant voltage's magnitude can be derived as follows:

$$V_{res,\max} = I_{res,\max} \cdot \frac{1}{2\pi f_{res} C_{diode}} = I_{res,\max} X_c \tag{41}$$

$$f_{res} = \frac{1}{2\pi\sqrt{L_{s,lk}C_{diode}}} \tag{42}$$

where f_{res} is the resonant frequency according at the blocking path, C_{diode} is the parasitic capacitance of the secondary diode, and X_c is the impedance of the parasitic capacitance. From (38), (39) and (41), the total reverse blocking voltage of secondary diode can be derived as shown in (43).

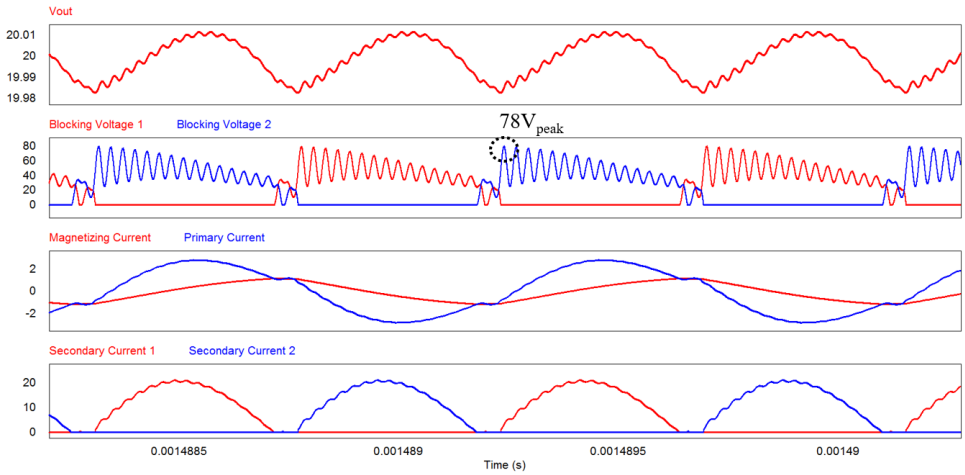


Fig. 11 Simulation waveforms of the secondary diode's blocking voltage.

$$V_{D,\mathrm{mod}} = V_D + V_{s,lk,\max} + V_{res,\max} = 2V_o + V_{s,lk,\max} + I_{res,\max}X_c \tag{43}$$

From (43), total blocking voltage is a function of V_o, $V_{s,lk}$, and $V_{res,max}$. Using (43), the reverse blocking voltage during mode 1 can be derived as follows:

$$V_{D,\mathrm{mod}} = 2V_o + nL_{s,lk}\left[\left(1-\frac{n^2L_{s,lk}}{n^2L_{s,lk}+L_m}\right)\cdot C_r\alpha\omega^2 - \frac{nV_o}{n^2L_{s,lk}+L_m}\right] + I_{res,\max}X_c \tag{44}$$

The high switching frequency and the large secondary leakage inductance induce a high reverse blocking voltage in the secondary rectifier, as shown in Fig 9 (b). Therefore, the practical reverse blocking voltage should be precisely calculated to select a proper secondary rectifying diode using (44). The practical blocking voltage of the secondary rectifier has very high frequency and very large voltage variation, as shown in Fig. 11.

2.3 Loop Gain Design for Fast Dynamics and Stability

In power converter control, digital signal processors (DSPs) and microprocessors are widely used to generate high precision PWM signals under high switching frequency operation. They generally have high noise immunity and can implement complex control techniques [23], [24]. However, the limited computation speed of the digital controller cannot cover the required control bandwidth for high

switching frequency operation, which results in low dynamic performance and stability of the power converter. Therefore, a time delay effect caused by the limited performance of the digital controller should be considered to obtain a proper small signal model that includes feedback and control delays.

An ideal converter control calculation should be completed within a single PWM cycle and be updated in the next PWM cycle. Thus, the closed loop gain at high switching frequency operation must obtain fast dynamic performance with enough phase margin. However, a practical digital controller has a limited computation speed which induces a time delay effect in the feedback control. As the increment of the switching frequency, the time delay becomes significant to the dynamic performance of the power converter. Therefore, for the closed-loop feedback control, the small signal model of the LLC resonant converter has to include the time delay effect caused by the digital controller to describe accurate small signal response and to design a proper digital feedback compensator, as shown in Fig. 12.

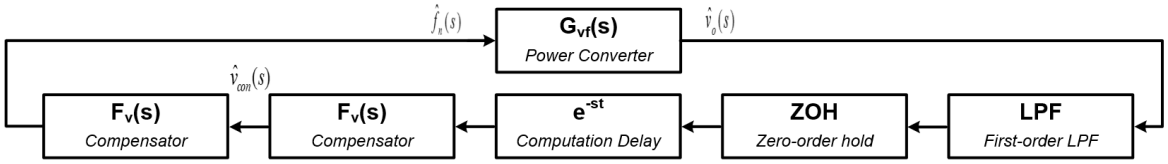
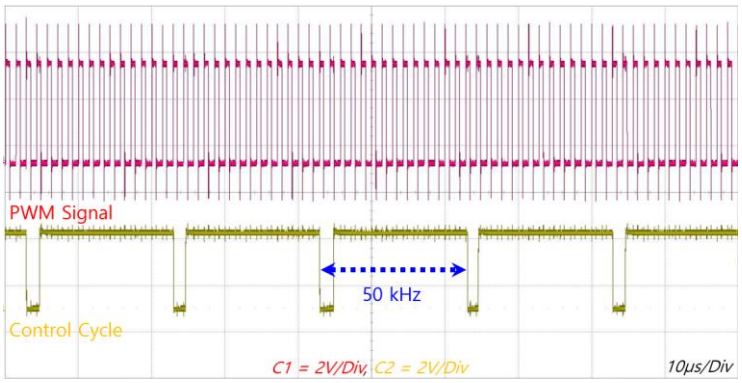
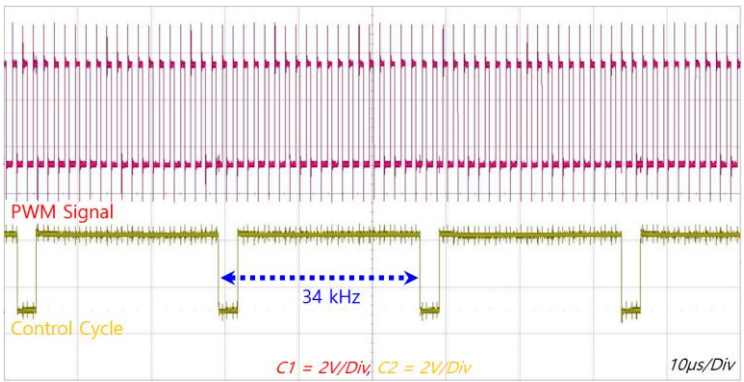


Fig. 12 Digital control block diagram of the proposed LLC resonant converter.



(a)



(b)

Fig. 13. Limited processing speed of a commercial PWM controller: (a) PI controller case, (b) lead-lag controller case.

The dominant time delay of the digital controller is composed of a low pass filter delay, the processing time delay of a zero-order-hold (ZOH) and the controller's computation time such as the feedback compensation, the PWM generation, and the ADC speed. In this paper, the TMS320F28335 is used as a commercial digital controller which has 150 million instructions per second (MIPS). The measured control bandwidth of the feedback loop implemented by this digital controller is 50 kHz, which is 20 times slower than the 1 MHz switching frequency, as shown in Fig. 13 (a). Therefore, the small signal model has to consider the controller's time delay which causes control performance degradation at the 1 MHz switching frequency.

The transfer function considering the controller's time delay can be expressed as follows:

$$G_{cont,d}(s) = G_{comp,d}(s) \cdot G_{ADC,d}(s) \cdot G_{PWM,d}(s) = e^{-s \cdot T_{comp}} \cdot e^{-s \cdot T_{ADC}} \cdot e^{-s \cdot T_{PWM}} = e^{-s \cdot T_{cont}} \cong \frac{1 - s \cdot \frac{T_{cont}}{2}}{1 + s \cdot \frac{T_{cont}}{2}} \tag{45}$$

where $G_{cont,d}(s)$ is the entire control time delay of the digital controller, $G_{comp,d}(s)$ is the computation time delay of the controller, $G_{ADC,d}(s)$ is the ADC time delay, and $G_{PWM,d}(s)$ is the PWM generation time delay. The time delay of the ADC and the PWM generation can be assumed by constant values of T_{comp} and T_{ADC}, respectively, based on the digital controller's specification. In addition, the exponential function can be transformed to the constant function using pade's approximation. However, comparing with Fig 13 (a) and (b), the computational time delay can change by the computation burden of the controller, which is affected by control complexity. Fig. 14 shows the time delays in the digital signal processor.

The ZOH time delay can be calculated as follows:

$$G_{ZOH,d}(s) = \frac{1 - e^{-sT_{ZOH}}}{sT_{ZOH}} \cong \frac{1}{1 + \frac{sT_{ZOH}}{2}} \tag{46}$$

where $G_{ZOH}(s)$ is the ZOH time delay and T_{ZOH} is the discrete sampling time. Even though the ADC performance of target DSP has a 80-ns conversion rate, the DSP has a seriously delayed sampling time caused by the long computation time. In addition, the time delay of the digital low pass filter should be considered in the total time delay of the feedback control. The time delay of the digital low pass filter can be described using a two pole system as follows:

$$G_{filter,d}(s) = \frac{T_c}{1 + T_c^2 s^2} \tag{47}$$

where T_c is the cut-off period of the low pass filter. Using (45), (46), and (47), the total time delay of the feedback control, $G_{total,d}(s)$ can be calculated in (48).

$$G_{total,d}(s) = G_{cont,d}(s) \cdot G_{ZOH,d}(s) \cdot G_{filter,d}(s) = e^{-s \cdot T_{cont}} \cdot \frac{1 - e^{-sT_{ZOH}}}{sT_{ZOH}} \cdot \frac{T_c}{1 + T_c^2 s^2} \tag{48}$$

The time delay effect can be applied to the small signal model of the LLC resonant converter as follows:

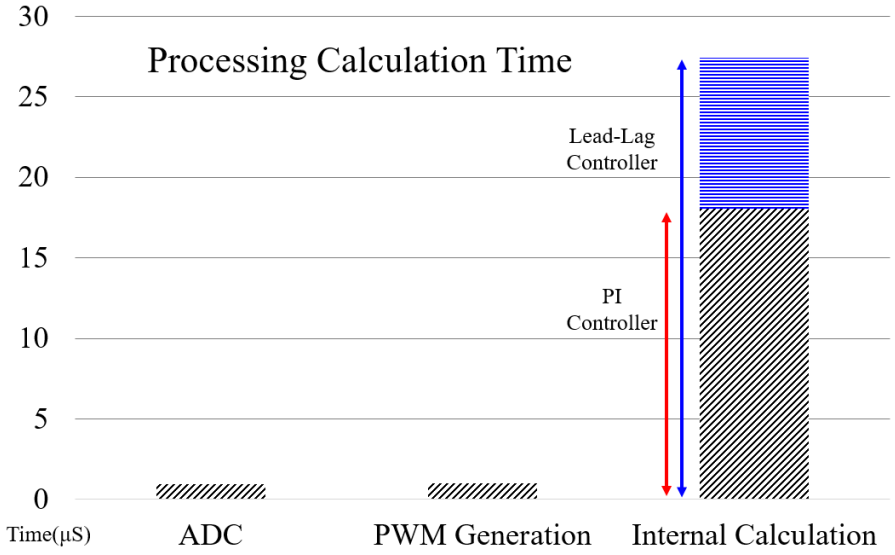


Fig. 14 Computation time in the digital controller.

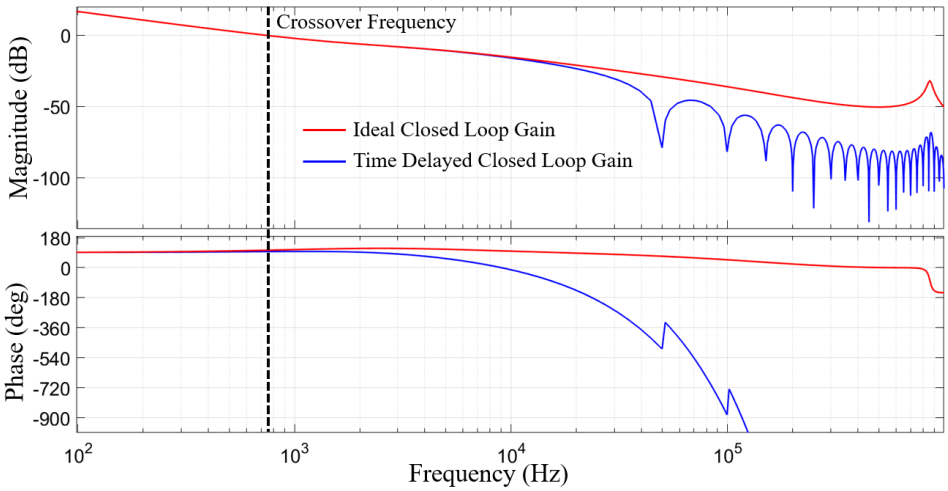


Fig. 15 Small signal responses of the closed loop gains according to the time delay effect.

$$\begin{aligned} x'(t) &= Ax(t) + Bu(t - T_{cont}) \cdot G_{ZOH}(t) \cdot G_{filter}(t) \\ y(t) &= Cx(t) + Du(t - T_{cont}) \cdot G_{ZOH}(t) \cdot G_{filter}(t) \end{aligned} \tag{49}$$

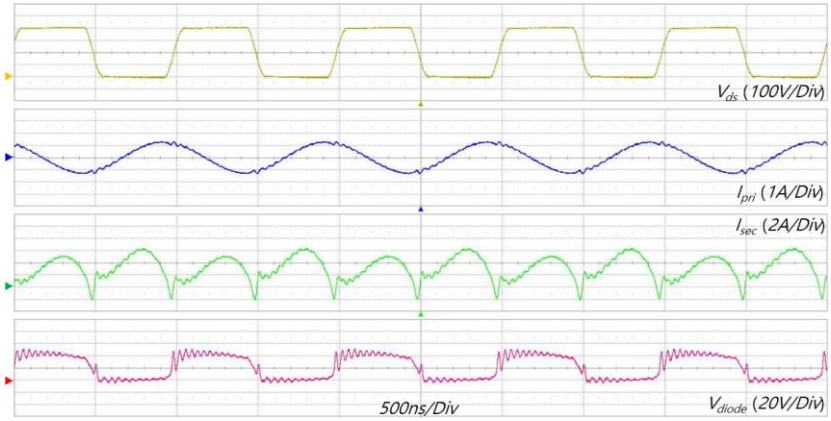
where *A, B, C, D* are the state space parameters, $x(t)$ is the system state vector, $u(t)$ is the control input, and $y(t)$ is the output voltage vector [23]. From (49), the transfer function of the frequency can be derived as follows:

$$\hat{f}_n = \frac{\hat{v}_o}{\hat{\omega}_r} = C(sI - A)^{-1} B \cdot e^{-sT_{cont}} \cdot \frac{1 - e^{-sT_{ZOH}}}{sT_{ZOH}} \cdot \frac{T_c}{1 + T_c^2 s^2} \tag{50}$$

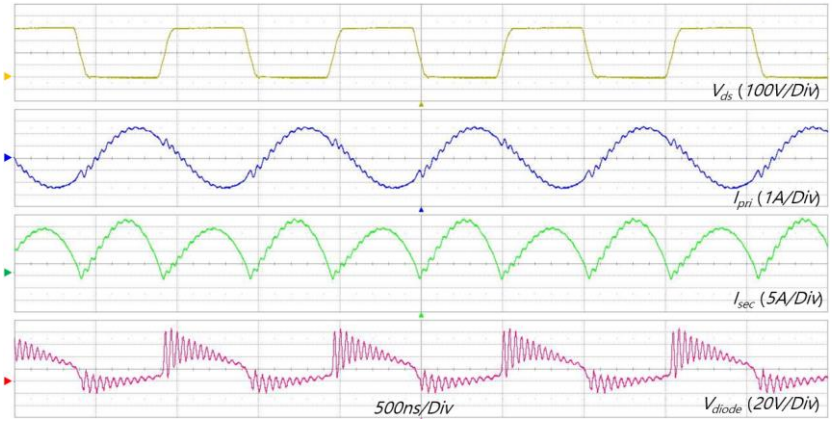
The transfer function shown in (50) is the multiplication of all the time delays combined to the conventional small signal model. The total time delay of the feedback control induces magnitude and phase drops in the bode plot. In Fig. 13 (a), it has a 50 kHz of the sampling frequency and a 25 kHz of the Nyquist frequency. Therefore, the LLC resonant converter operating at the high switching frequency around 1 MHz with the significant feedback control delay cannot have a high crossover frequency which results in insufficient phase margin. In this case, the limited computation speed of the digital controller requires available crossover frequency range which can be obtained by proper feedback compensator design. The cut-off frequency of the digital low pass filter can also be considered for the limited control bandwidth. With the significant time delay of the feedback control at the high switching frequency case, it makes the drastic phase drop before the sampling frequency compared with the magnitude drop. Therefore, the crossover frequency should be practically located at 10 times lower frequency than sampling frequency to avoid drastic phase drop. Fig. 15 shows that the time delayed model has the drastic phase drop before the sampling frequency compared with the conventional model which does not consider the time delay. Therefore, the limited control bandwidth requires lower crossover frequency to obtain proper relative stability. In addition, the cut-off frequency of the low pass filter should be higher than the crossover frequency of the feedback loop gain.

2.4 Experimental Verification

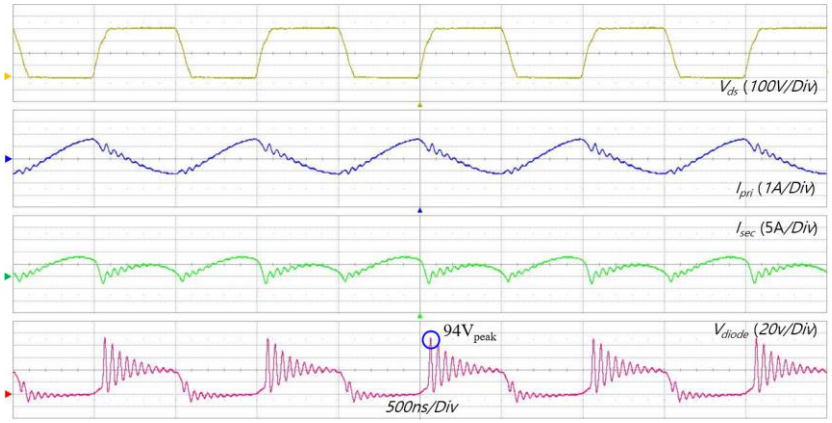
Fig. 16 shows the operational waveforms of the 1 MHz switching frequency LLC resonant converter. The design specifications are 400 V DC input and 20 V DC output voltage. In the case of 12:1 turn ratio, the converter has ZVS capability on the primary MOSFETs and soft commutation on the output rectifier, as shown in Fig. 16 (a) and (b). In the case of 11:1 turn ratio shown in Fig. 16 (c), the converter cannot operate under the soft commutation, which makes high switching loss on the output rectifier.



(a)



(b)



(c)

Fig. 16 Operational waveforms of the prototype 1 MHz LLC resonant converter according to the turn ratio: (a) 3 A light load condition with 12:1 turn ratio, (b) 12 A full load condition with 12:1 turn ratio, (c) 3 A light load condition with 11:1 turn ratio.

At the light load condition satisfying the soft commutation on the output rectifier, the small secondary current induces small secondary side reverse voltage, which is similar to the conventional reverse voltage in (39). At full load condition under soft commutation, the high reverse voltage in the rectifier is induced by the large voltage variation in the secondary leakage inductance. At light load conditions without soft commutation, however, the converter shows higher reverse voltage spikes than at the full load condition with the soft commutation. Therefore, the output rectifier should endure the high reverse voltage spike at the high switching frequency operation. All the design specification of the prototype converter is listed in Table I.

Table I. Design Specifications

Specification	**Value**	
V_{in}	400 V	
Full load	20 V, 12 A	
	Proposed Design	**Conventional Design**
n_{mod}	12	11
L_m	53 μH	45 μH
L_r	7.5 μH	7.6 μH
C_r	1.5 nF	1.5 nF
$L_{sec,leak}$	50 nH	54 nH
C_{diode}	530 pF	530 pF
Resonant Frequency	1.104 MHz	1.125 MHz
$V_{D,mod}$	82 V	114 V
$I_{m,peak\ (2A)}$	1.12 A	1.33 A
Soft Switching	ZVS in the primary	ZVS in the primary
	Soft commutation in the secondary	Non-soft commutation

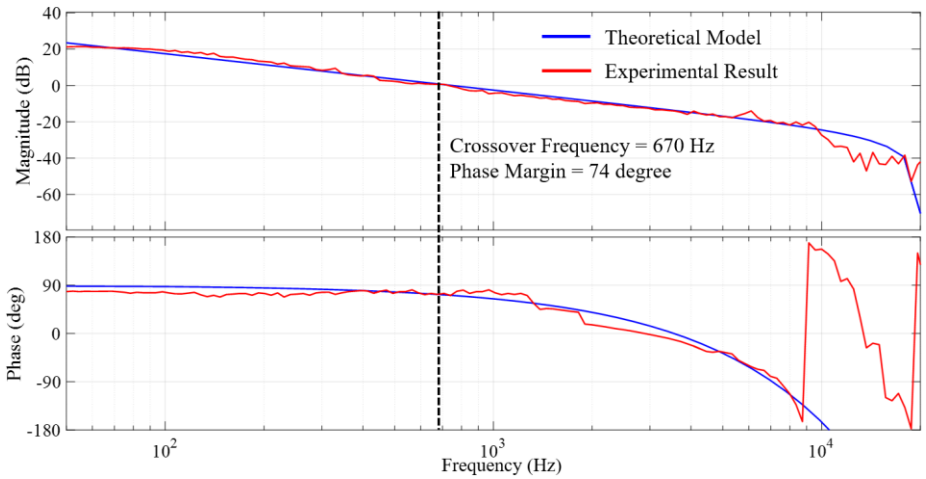
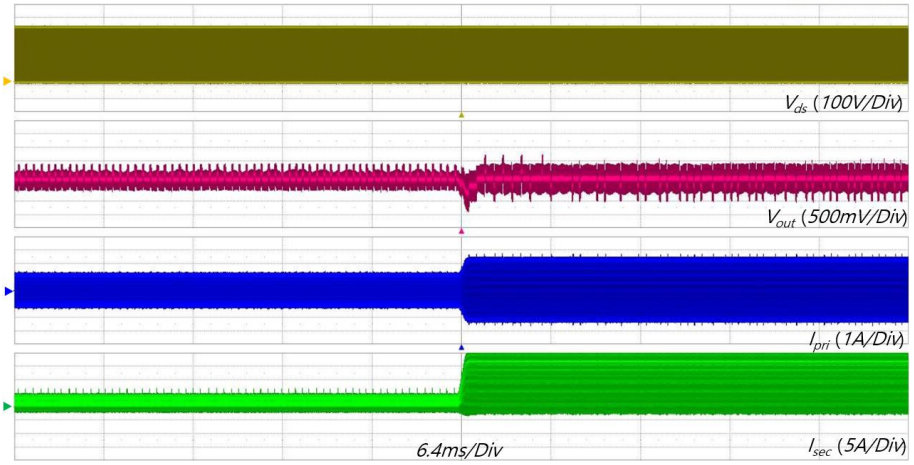
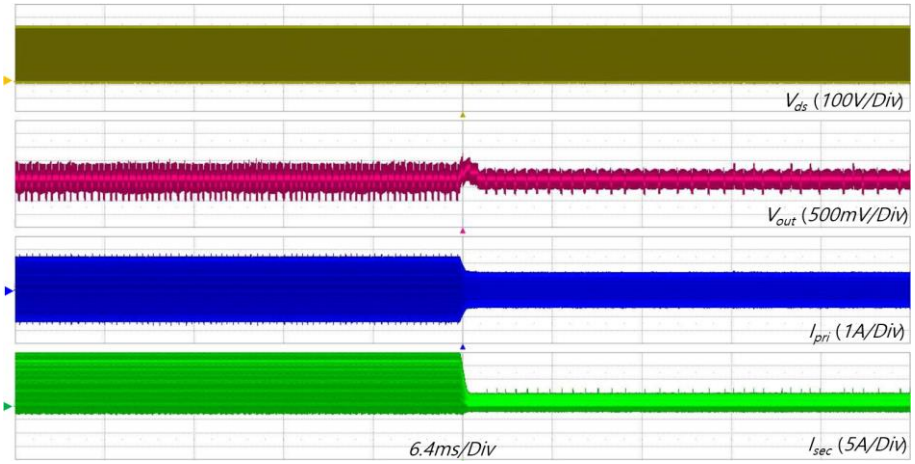


Fig. 17 Theoretical analysis and experimental result of the closed-loop gain of the prototype converter.

In Fig. 17, the closed-loop gain using a PI controller has 74 degree phase margin at the crossover frequency of 670 Hz which can guarantee enough relative stability against noise and disturbance in the converter. The experimental results are well matched with the theoretical analysis. Fig. 18 shows the step load responses of the prototype converter according to the load variation. With respect to the load step-up and load step-down condition, the output voltage variation and the transient time are 2.1 V (1.6 ms) and 1.78 V (1.4 ms), respectively.



(a)



(b)

Fig. 18 Step load response of the 1 MHz LLC resonant converter: (a) from 2 A to 12 A step load change, (b) from 12 A to 2 A step load change.

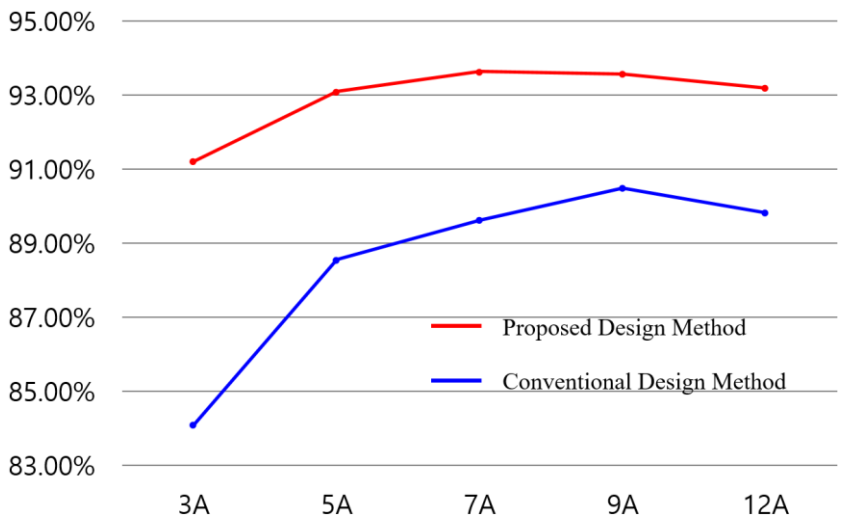


Fig. 19 Power conversion efficiency of the prototype 1 MHz LLC resonant converter.

Fig. 19 shows the comparison of power conversion efficiency according to the design methods. The conventional power converter design shows large primary circulating current and high switching loss in the output rectifier. However, the proposed design improves power conversion efficiency around 7% and 3% at the light and full load conditions, respectively.

III. Output Voltage Regulation Technique

The digitally controlled LLC resonant converter has a limited frequency resolution, since the digital controller is implemented using a limited clock speed to generate the PWM signals. Moreover, the limited frequency resolution can lead to performance degradation at high switching frequencies because a large switching frequency variation can be induced by a single frequency step in the digital signal processor (DSP). For example, a general-purpose DSP (TI TMS320F28335), which is used in this research, provides 150 million instructions per second (MIPS) performance. However, it does not have high enough frequency resolution for a pulse frequency modulation (PFM) operating at several mega-hertz switching frequency. This limited frequency resolution induces high variation in the input-output voltage gain at high switching frequencies, which causes high output voltage ripple in the LLC resonant converter [25]-[27]. Moreover, it results in high fluctuation of the primary- and secondary-side currents, which induces abnormal oscillations and high current stress on the passive components. In this section, the hybrid control algorithm is proposed to obtain the tight output voltage regulation at the high switching frequency operation. From Section II and Section III, the LLC resonant converter operating at high switching frequency is designed to obtain high power conversion efficiency and tight output voltage regulation.

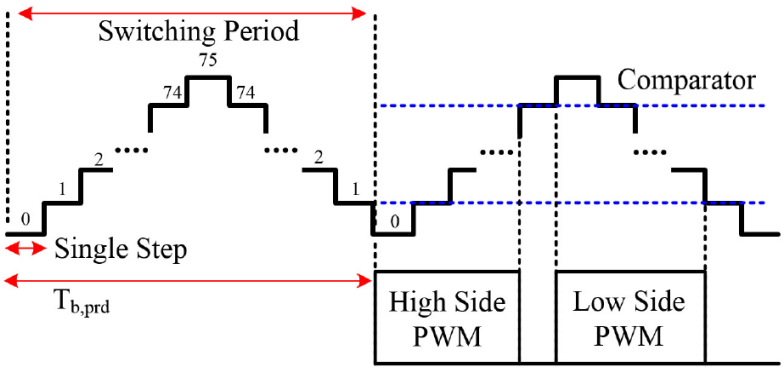


Fig. 20 PWM and PFM generations of the general-purposed DSP.

3.1 Limitation of Controller Resolution in High Switching Frequency

The target DSP (TI TMS320F28335) has a 150 MHz clock speed, which sets the time-based period, $T_{b,prd}$. This period determines the time steps that generate triangular waveforms for implementing the PFM gate signals. Fig. 20 shows that the total number of time steps that determines the switching frequency of the PFM gate signal. The $T_{b,prd}$ of the target DSP can be calculated as follows [28]:

$$T_{b,prd} = \frac{T_s}{2T_{tb,clk}} \tag{51}$$

where $T_{b,prd}$ is the total number of DSP time steps, T_s is the switching period of the power converter, and $T_{tb,clk}$ is the DSP system clock period (1/150 μsec).

From (51), the calculated $T_{b,prd}$ can be used to determine the variation of the switching frequency according to a single bit change in DSP control variables. The switching frequency variation from a single time step change, Δf_s, can be calculated as shown in (52).

$$\Delta f_s = \frac{1}{2T_{tb,clk}}\left(\frac{1}{T'_{b,prd}} - \frac{1}{T_{b,prd}}\right) \tag{52}$$

From (51) and (52), the switching frequency variation increases according to the square of the switching frequency. At 1 MHz switching frequency, $T_{b,prd}$ is 75 and its frequency variation is 13.158 kHz for a single time step change in the DSP. At 100 kHz switching frequency, $T_{b,prd}$, is 750 and its frequency variation is 133.16 Hz for a single step change. Therefore, the PFM frequency resolution of the DSP at 1 MHz switching frequency is 100 times lower than the frequency resolution at 100 kHz. Under the conventional PFM control, the voltage gain of the LLC resonant converter is only affected by switching frequency variations [17]. From (1), significant gain oscillation can be expected due to the poor PFM frequency resolution of the general-purpose DSP.

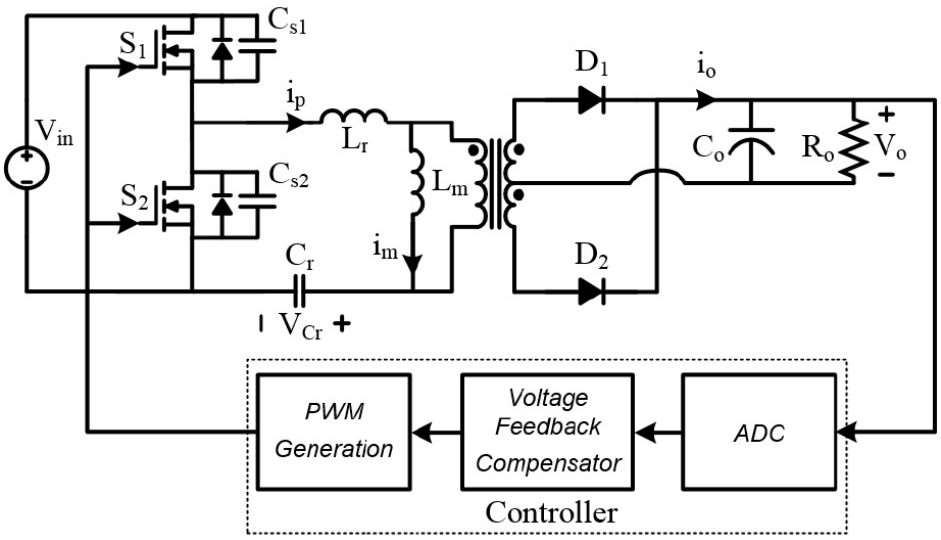


Fig. 21 LLC resonant converter with feedback controller.

The DSP controller for the power converter is composed of an analog-to-digital converter (ADC), a voltage feedback compensator, and a PWM generator as shown in Fig. 21. The performance of the output voltage regulation is determined by available ADC resolution and PFM frequency resolution of the DSP controller. At low switching frequencies, the ADC and the PFM frequency have similar control resolution such that the output voltage is well regulated under load variations. The voltage measurement resolution using the ADC can be expressed as follows [29]:

$$\Delta V_{ADC} = \frac{V_{out}}{2^{N_{ADC}}} \tag{53}$$

where N_{ADC} is the ADC bit number and V_{out} is the output voltage of a power converter. The received output voltage information in the DSP controller is the quantized value from an analog signal, which is based on the bit change of the ADC.

From (1) and (51), the input-output voltage gain according to $T_{b,prd}$ can be expressed as shown in (54).

$$G\left(T_{b,prd}\right) = \left\| H_r\left(\frac{T_{b,prd}^{-1}}{2T_{tb,clk} f_r}\right)\right\| \tag{54}$$

Using (54), the voltage control resolution using the PFM control method can be expressed as follows:

$$\Delta V_{PFM} = \frac{V_{in} G\left(\Delta T_{b,prd}\right)}{2n_p} \tag{55}$$

where n_p is the primary to secondary transformer turn ratio and V_{in} is the input voltage of the power converter. The limited $T_{b,prd}$ makes the large variation of the quantized output voltage and the primary- and secondary-side currents with respect to $T_{b,prd}$ changes.

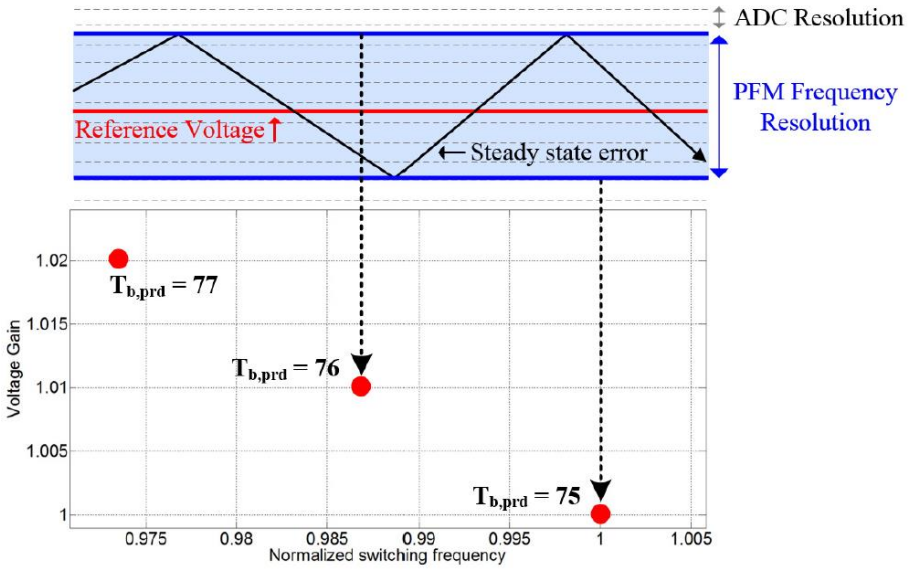


Fig. 22 Variation of input-output voltage gain with limited switching frequency variation.

The calculated ΔV_{ADC} and ΔV_{PFM} are around 4.88 mV and 0.2 V, respectively, at 1 MHz switching frequency in the general-purpose DSP. The output voltage is regulated by the PFM control, which has 20 times lower resolution compared with the ADC and induces high steady state error. Therefore, at high switching frequency, the power converter frequently changes its switching frequency to compensate for accumulated steady-state output voltage error. In turn, this induces larger output voltage ripple compared to the conventional low switching frequency operation. This poor controllability of the

output voltage regulation is illustrated in Fig. 22, which shows the limitation of the PFM frequency resolution, the large switching frequency variation, and the large steady state error of the output voltage according to $T_{b,prd}$. Therefore, low PFM frequency resolution and periodic switching frequency change caused by the steady state error leads to poor output voltage regulation and abnormal current fluctuation on the primary- and secondary-sides.

3.2 PFM-PWM Hybrid Control Algorithm

To overcome the technical issue of the limited frequency resolution in the general-purpose DSP, the proposed hybrid control method contains not only the PFM control but also the PWM control with an intelligent control mode selection algorithm which can determine the proper control mode according to operating conditions. The duty cycle generated by the PWM control method is defined as follows:

$$D = \left(\frac{t_d}{T_s} \right) \cdot 100\% \tag{56}$$

where t_d is the time duration of the duty cycle. Using the Fourier series, the fundamental components of the input voltage can be obtained in (56).

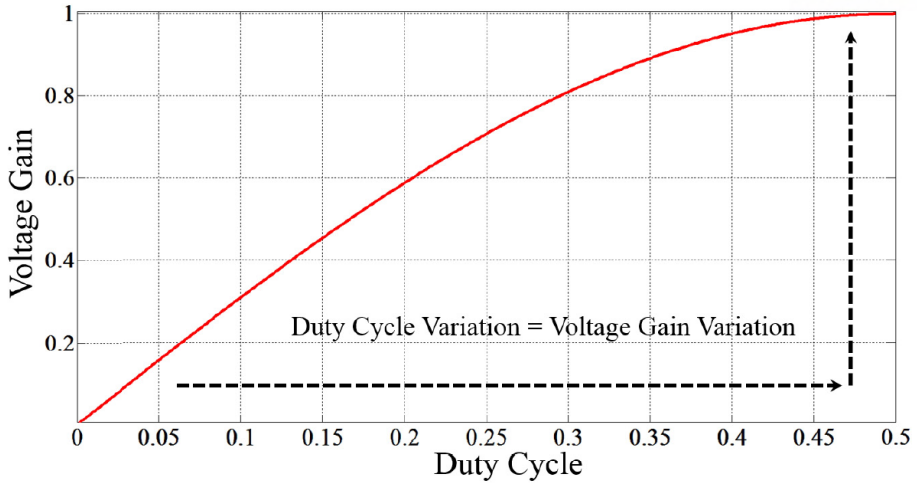
$$V_{in,F} = V_{in} \sin \pi \left(\frac{t_d}{T_s} \right) \tag{57}$$

From (1) and (57), the input-output voltage gain using the PWM and PFM hybrid control method can be derived as follows [30], [31]:

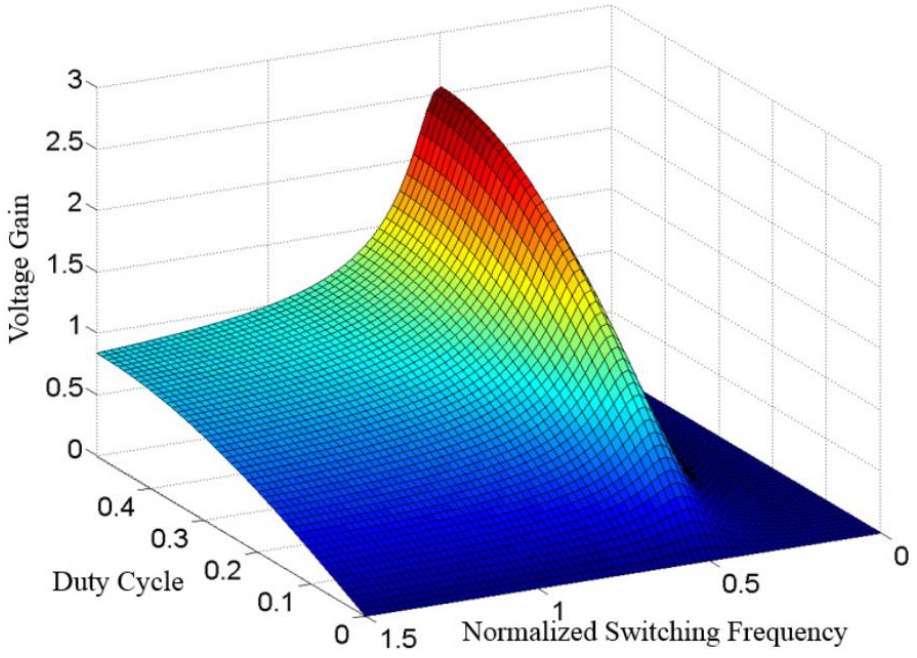
$$\frac{V_o}{V_{in}} = \left\| H_r \left(f_n \right) \right\| \sin \pi \left(\frac{t_d}{T_s} \right) \tag{58}$$

Using (58), the hybrid control method combining the PWM and the PFM control methods can compensate the performance degradation of the output voltage regulation, which is caused by the limited frequency resolution.

Fig. 23 (a) shows the voltage gain curve of the LLC resonant converter with respect to the variation of the duty cycle. It considers not the parallel resonant frequency, but the series resonant frequency, because the series resonant frequency is widely used for design criterion of LLC resonant converter. In (58), the output voltage can be regulated using both the changes of f_n and t_d, which means that there are two degrees of freedom in the output voltage regulation. Fig. 23 (b) shows the gain surface of the proposed PWM and PFM hybrid control algorithm according to the switching frequency and the duty cycle variations. It shows both resonant frequencies, the series resonant frequency and the parallel resonant frequency. Using two control variables of the pulse width and the switching frequency at the same time, the voltage gain can be precisely controlled in the LLC resonant converter, even with poor PFM frequency resolution.



(a)

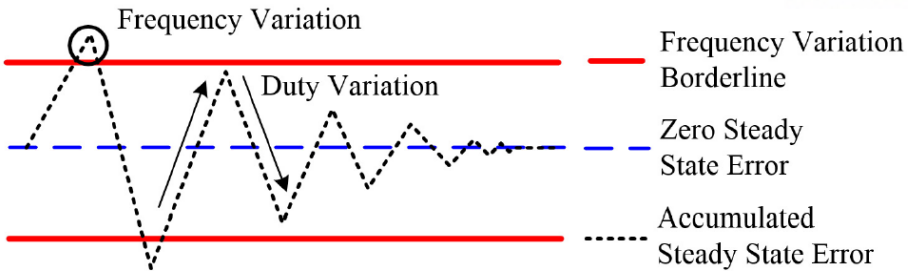


(b)

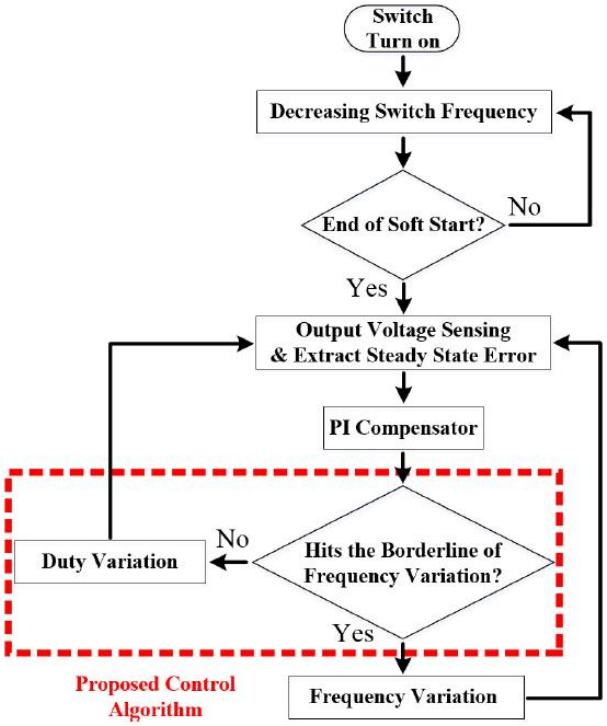
Fig. 23 Voltage gain of the LLC resonant converter: (a) Gain curve according to the duty cycle at the resonant frequency, (b) Gain surface according to the normalized switching frequency and duty.

3.2.A Operational Principle of Hybrid Control

The proposed PWM and PFM hybrid control method can enhance the output voltage regulation performance in the steady state operation using two independent control variables [32]. To implement the combination of PWM and PFM control in the hybrid control method, the priority between the pulse width and the switching frequency must be determined at the specific operating point. The control priority can be determined by the control borderline which separates operational regions of the control variables.



(a)



(b)

Fig. 24 PWM and PFM hybrid control algorithm: (a) Output voltage regulation mechanism, (b) Control flow chart.

Fig. 24 (a) shows the output voltage regulation mechanism of the proposed hybrid control algorithm. There are two red lines, a blue dotted line, and a black dotted line, which show frequency variation borderlines, zero steady state error, and accumulated steady state error, respectively. In steady state operation, the accumulated steady state error should converge to zero in order to regulate the output voltage at the desired value. The frequency variation borderlines indicate switching frequency changes for the output voltage regulation. When the accumulated error is located between two frequency variation borderlines, the output voltage is regulated by the PWM control. However, the duty cycle variation should be limited to guarantee proper resonant operation of the LLC resonant converter. If the accumulated steady state error crosses a borderline, the output voltage will be regulated by the PFM control. Therefore, the priority of the PWM control is higher than the priority of the PFM control; the

output voltage is regulated by switching frequency changes only when the changes in duty cycle cannot regulate the output voltage. In the proposed hybrid control algorithm, the PFM control sets the preliminary operating point using its limited frequency resolution. Then, the PWM control precisely regulates the output voltage using its high control resolution, described in (58).

Fig. 24 (b) shows the control flow chart of the proposed hybrid control method including the intelligent control mode selection algorithm emphasized with the dotted red rectangular in the figure. The conventional PFM control has only a switching frequency control loop which includes the voltage feedback compensator to regulate the output voltage. However, in the proposed hybrid control method, a PWM control block and a control mode selection block are added to minimize the steady state error in the output voltage. Every control cycle, the accumulated steady state error is measured and compared with the frequency variation borderlines to determine the control method. Then, the gate signal of the LLC resonant converter is generated based on the selected control mode: PWM control or PFM control. For the PFM control mode, if the accumulated steady state error exceeds the frequency variation borderline, the switching frequency is changed by a single step change of $T_{b,prd}$ to regulate the output voltage, while the duty cycle is adjusted to the initial duty ratio. After the single step change of $T_{b,prd}$, the PWM control mode starts to regulate the output voltage from the initial duty ratio.

For the hybrid control method, the frequency variation borderlines are practically designed to obtain the enough PWM control area. If the borderline is too narrow, the PWM control area will be insufficient and may not work properly during small load variations, high switching noise in the power converter, or measurement error of the analog to digital converter (ADC). On the other hand, a borderline that is too wide can induce poor dynamic performance during load variation. Therefore, the proper frequency variation borderlines should be designed in a practical manner. In this research, the width of the control borderline is selected as 0.5 (from -0.25 to 0.25), verified by experiments.

The PWM control included in the proposed hybrid control method also has limited control resolution caused by the DSP performance limitation. The DSP has controllable duty cycles determined by a specific $T_{b,prd}$ value, as shown in Fig. 20. For example, 75 $T_{b,prd}$ generates 1 MHz switching frequency and 75 controllable duty cycles. However, the output voltage resolution of the PWM control is almost three times higher than that of the conventional PFM control.

The proposed PWM and PFM hybrid control algorithm is more complex than the conventional PFM control method. In Fig. 24 (b), the control mode selection block and the PWM control block should be added to the PFM control. In steady state operation, however, the computational burden of two additional blocks is not significant compared to the other processing units, such as the ADC, error amplifier, and PWM generation in the DSP.

3.2.B Design Considerations of Hybrid Control

Using the proposed hybrid control method, the control resolution is improved to precisely regulate

the output voltage. From (54) and (57), the improved voltage control resolution using the proposed PWM and PFM hybrid control method can be expressed as shown in (59).

$$\Delta V_{PPH} = \frac{V_{in}}{2n_p} G\left(T_{b,prd}\right) \sin \pi \left(\frac{\Delta t_d}{T_{b,prd}} \right) \tag{59}$$

Equation (59) shows that the additional control variable of $\sin\pi(t_d/T_{b,prd})$ induced from the PWM method makes the high voltage gain steps lower than that of the conventional PFM method which can improve the output voltage regulation performance. Therefore, in (59), the two independent control variables of $T_{b,prd}$ and t_d show higher voltage control resolution compared to the conventional PFM control method.

However, in previous research, this hybrid control method has not yet been adapted for the LLC resonant converter in its steady state operation, because the hybrid method increases controller design complexity by handling two control variables. Moreover, the large dead time duration caused by the proposed hybrid control method can induce ZVS failure in the power MOSFETs. Therefore, the maximum dead time duration and the proper magnetizing inductance should be derived to ensure the ZVS condition over the entire load range. The conventional magnetizing inductance design constraint for the LLC resonant converter can be expressed as follows [32]-[34]:

$$L_m \le \frac{t_{dt} T_s}{16 C_{eq}} \tag{60}$$

where t_{dt} is the dead time duration, C_{eq} is the equivalent capacitance of the power MOSFETs, and L_m is the magnetizing inductance of the transformer. Using (60), the proper value of magnetizing inductance can be obtained for ZVS based on the variations of the switching frequency and the dead time ratio. The required magnetizing inductance to achieve ZVS is illustrated in Fig. 25, which shows that the highest switching frequency and the largest duty ratio condition has the smallest magnetizing inductance value that ensures ZVS over the entire load range. Therefore, the design criteria for the magnetizing inductance depends on the lightest load condition and the largest duty ratio.

The proper magnetizing inductance design is an important factor to achieve ZVS in the power MOSFETs. For example, the duty cycle range is determined by the design value of the magnetizing inductance. A small duty cycle can induce a non-ZVS condition in the power MOSFETs, as shown in Fig. 26. When the non-ZVS condition with large enough dead time occurs, there are three sequential states that occur during the dead time, as shown in Fig. 26 (a) and (b). To turn on *S1* in this half cycle, the primary current charges the output capacitance of *S2* and discharges the output capacitance of *S1* (from t_1 to t_2), which can induce the ZVS operation of *S1*. After this duration, the primary current flows through an antiparallel diode integrated in *S1* (from t_2 to t_3). However, the primary current direction changes during the dead time due to its resonance (from t_3 to t_4). At that time, the primary current can charge the output capacitance of *S1* during the turn-on process of the power MOSFET(t_4). As a result, the primary MOSFETs fails to achieve ZVS operation due to the direction change of the primary current.

The simulation result also shows the non-ZVS operation caused by a small duty cycle (or long dead time duration). Therefore, the minimum duty cycle or the maximum dead time should be limited to achieve the ZVS in the power MOSFET for high power conversion efficiency with small switching losses.

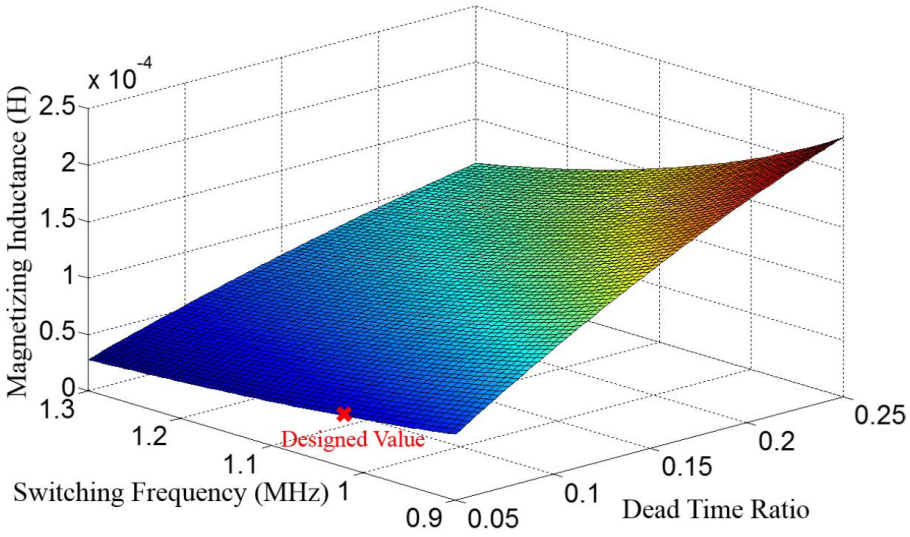


Fig. 25 Magnetizing inductance surface according to switching frequency and dead time for ZVS condition.

The basic ZVS condition of two power MOSFETs, upper side and lower side, are different from each other. For the upper-side MOSFET, the primary current should be negative during the dead time. For the lower-side MOSFET, a positive primary current is required. Using the high side ZVS condition, the primary current of the converter can be expressed as follows:

$$i_p(t) = -i_p(t_1)\cos\omega_r(t-t_1) + \frac{V_x}{Z_r}\sin\omega_r(t-t_1) \tag{61}$$

where t_1 is the turn-off transition time of the lower MOSFET, as shown in Fig. 26 (b), $i_p(t_1) = n_p V_o T_s / 8L_m$, $\omega_r = 2\pi f_r$, $V_x = V_{in}\text{-}V_{cr}(t_1)\text{-}n_p V_o$, and $Z_r = \text{sqrt}(L_r/C_r)$. From (61), the ZVS condition of the upper MOSFET can be calculated as shown in (62).

$$-i_p(t_1)\cos\omega_r(t-t_1) + \frac{V_x}{Z_r}\sin\omega_r(t-t_1) \le 0 \tag{62}$$

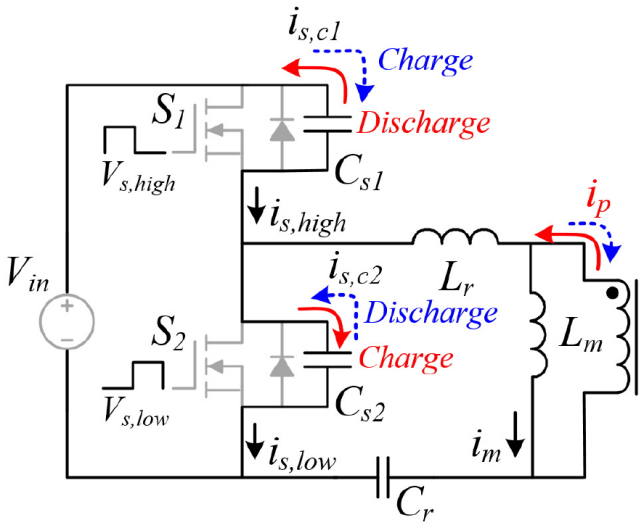
Using (62), the maximum dead time duration can be calculated as follows:

$$t_{dt} \le \frac{\arctan\varphi}{\omega_r} \tag{63}$$

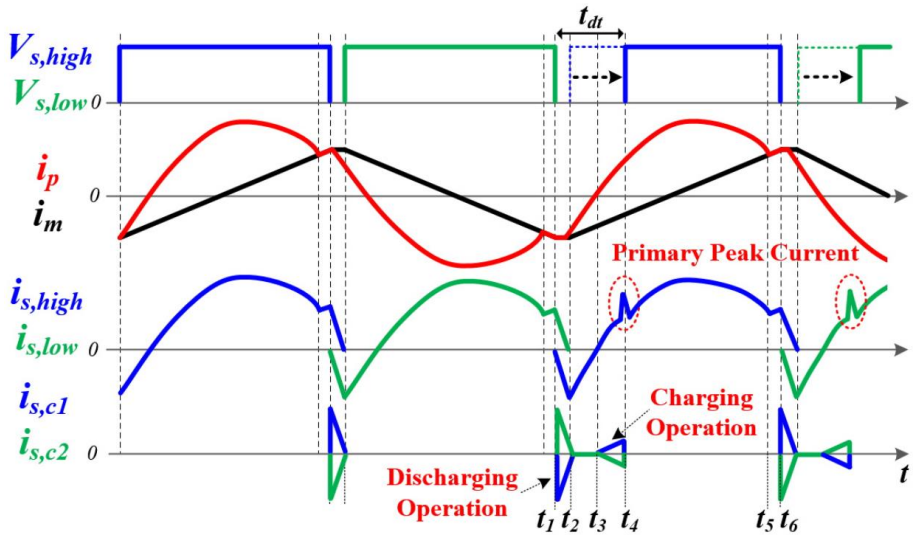
where $\varphi = i_p(t_1)Z_r/V_x$. Using (60) and (63), the proper dead time duration for ZVS can be derived as shown in (64).

$$16C_{eq}L_m f_s \le t_{dt} \le \frac{\arctan\varphi}{\omega_r} \tag{64}$$

The ZVS condition of the primary MOSFETs can be satisfied with both the proper magnetizing inductance and dead time duration using (60) and (64), respectively.



(a)

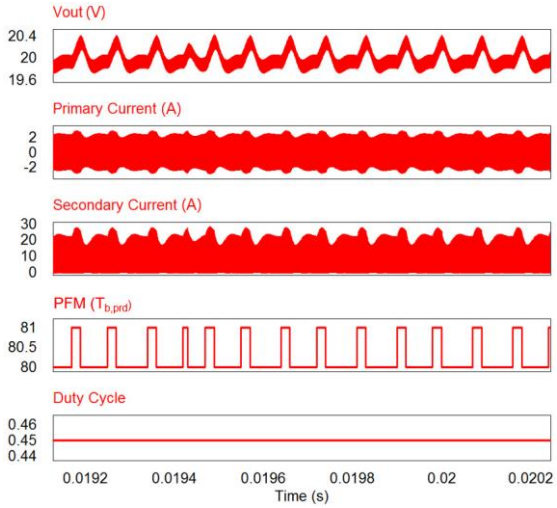


(b)

Fig. 26 ZVS and non-ZVS operation of the primary switches: (a) Mechanism of non-ZVS operation of primary switches, (b) Theoretical waveform of non-ZVS condition.

The design of the duty cycle range is important to achieve high power conversion efficiency using the hybrid control for the entire load condition range. The maximum duty cycle has to assure sufficient dead time to obtain operational stability which protects the systems from a shoot-through fault between high- and low-side power switches. The minimum duty cycle is designed to cover the gain range

between two adjacent PFM frequency steps and to guarantee the ZVS operation of the primary MOSFETs. Having large variation of the duty cycle allows the hybrid control to cover the gain range between PFM frequency steps, but it also increases RMS current on the primary side, which results in high conduction loss [35]. However, a small duty cycle range cannot cover the gain range between two adjacent PFM frequency steps, which induces operational failure of the hybrid control. Therefore, the duty cycle range has to cover one $T_{b,prd}$ change to improve the output voltage resolution using the continuous duty control. In addition, it has to satisfy the ZVS condition using (64). The conventional PFM method shows 1% output voltage fluctuation caused by a single $T_{b,prd}$ step change, while the proposed hybrid control method limits the output voltage fluctuation to 0.38% by using a single duty cycle step change.



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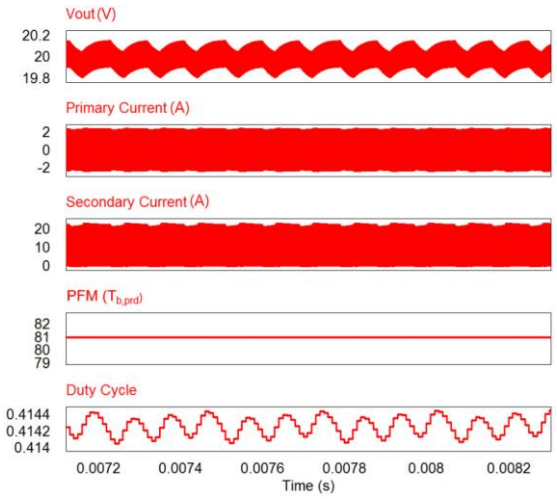
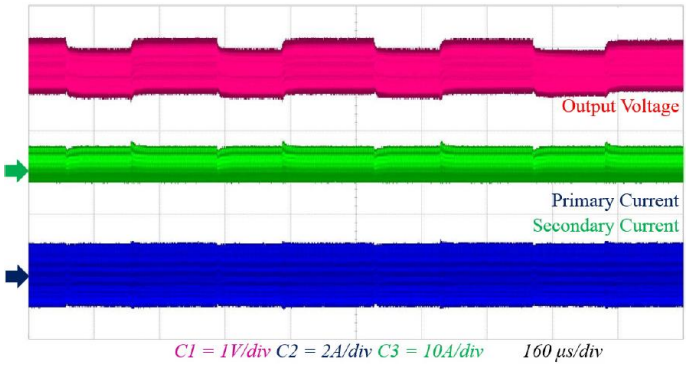


(b)

Fig. 27. Simulation waveforms of the LLC resonant converter: (a) with the conventional PFM control, (b) with the proposed PWM and PFM hybrid control.



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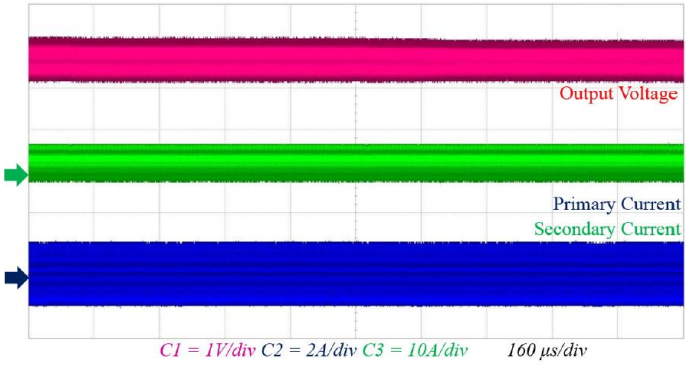

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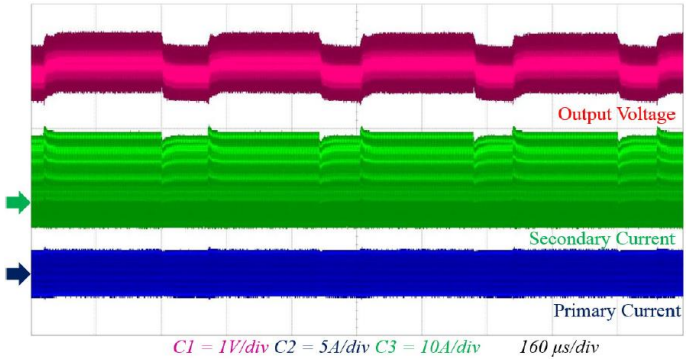

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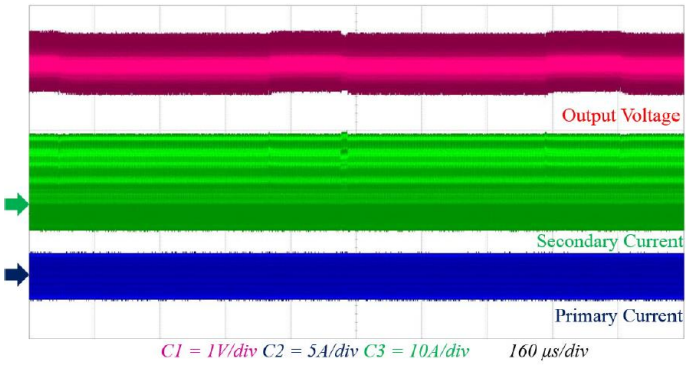


(d)

Fig. 28. Experimental waveforms of the output voltage regulation performance according to load conditions and controllers: (a) 2 A with the PFM control, (b) 2 A with the hybrid control, (c) 12 A with

the PFM control, (d) 12 A with the hybrid control.

3.2.C Simulation and Experimental Results

Fig. 27 shows the simulation results of the output voltage regulation performance in the steady state operation. In Fig. 27 (a), there are periodic output voltage oscillations induced by the limited switching frequency resolution of the conventional PFM control algorithm because it uses only frequency changes modulated by the variation of $T_{b,prd}$. As a result, the primary- and secondary-side currents also have oscillations which are similar to the output voltage ripple. In Fig. 27 (b), however, the output voltage ripple becomes much smaller than in the conventional case because the output voltage is well regulated by the PWM control, which has higher control resolution. In addition, there is smaller current oscillation in the primary- and secondary-sides.

Table II Simulation and Experimental Specifications

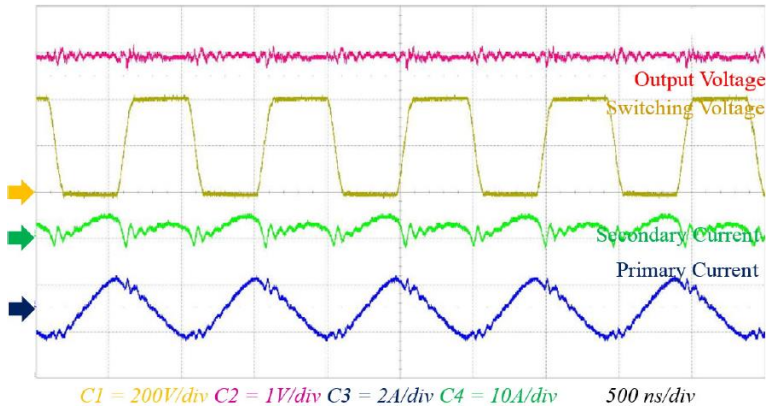
Specification	**Value**
V_{in}	400 V
Vo, Io	20 V, 12 A
L_r	16 μH
C_r	1.5 nF
L_m	49 μH
f_r	1.02 MHz
Borderline	-0.25 to 0.25
Duty Cycle	84% to 90%

Table III Simulation and Experimental Performance Verification

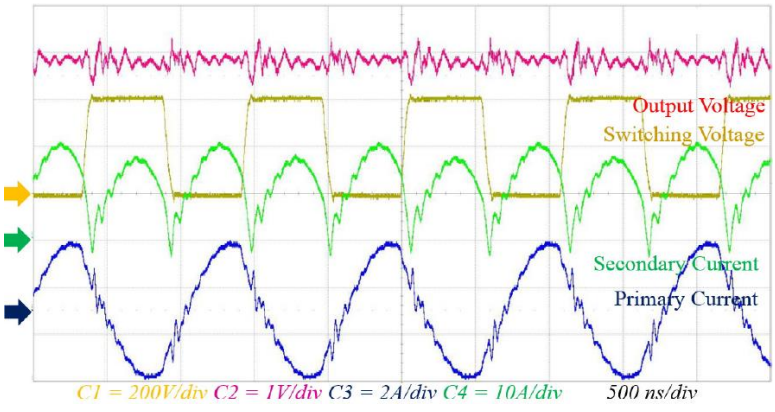
Performance Index	**Conventional PFM**		**Hybrid Method**	
	Simulation	**Experiment**	**Simulation**	**Experiment**
$I_{p,p}$	2.88 A	3.1 A	2.29 A	2.89 A
$I_{s,p}$	24.18 A	24.3 A	21.40 A	21.8 A
$V_{o,r}$	0.70 V	1.67 V	0.35 V	1.14 V

Fig. 28 (a) and (c) show the operational waveforms using the PFM control method according to the load variations, which were experimentally obtained with a 240 W prototype LLC resonant converter operating at 1 MHz switching frequency. The results show high output voltage ripple and high primary- and secondary-side currents due to the frequent switching frequency variation. Fig. 28 (b) and (d) show the operational waveforms during load variations using the proposed PWM and PFM hybrid control

method. In these experiments, the duty range of the proposed hybrid control is limited between 84% and 90% of the entire duty cycle, since this range allows the controller to compensate the drastic gain variation by the $T_{b,prd}$. Compared with Fig. 28 (a) and (c), the proposed hybrid control algorithm shows lower primary- and secondary-side current ripple (around 93% and 90%, respectively), and lower output voltage ripple (around 68%). All the design specifications of the simulation and experiment are outlined in Table II. All simulation and experimental results are summarized in Table III, where $I_{p,p}$ is the primary side peak current, $I_{s,p}$ is the secondary side peak current, and $V_{o,r}$ is the output voltage ripple. From (55) and (59), the output voltage resolution of the PFM control and the PWM control is around 0.2 V (1%) and 0.076 V (0.38%), respectively. However, the power converter has additional output voltage ripple caused by the limited output capacitance and its ESR. Moreover, when the switching frequency and the duty cycle changes, the output voltage may fluctuate during this transient time. Therefore, the experimental results show larger output voltage ripple than the theoretical expectations.



(a)

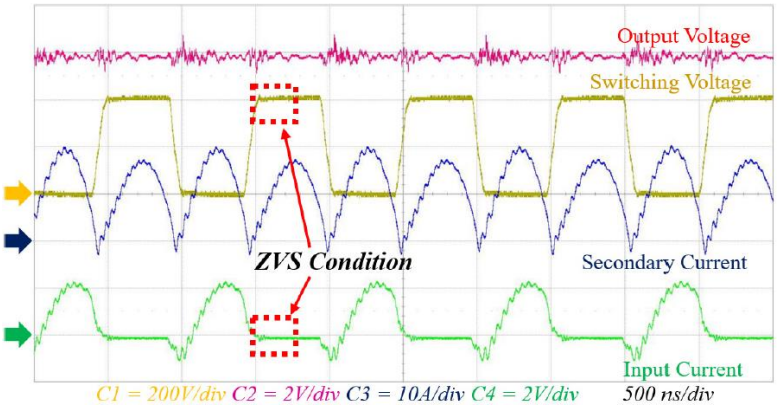


(b)

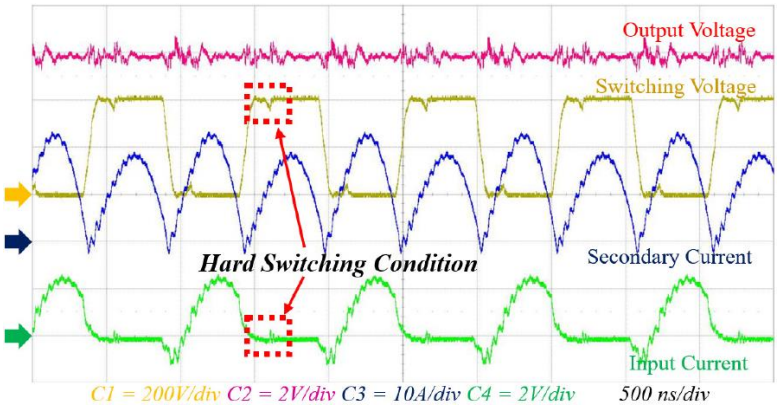
Fig. 29 Experimental waveforms of the LLC resonant converter with the proposed hybrid control method in the steady state operation: (a) 2A light load condition, (b) 12A full load condition.

Fig. 29 shows the experimental waveforms of the prototype converter with the proposed hybrid

control method in steady state operation. Operational waveforms during a light load of 2 A and full load of 12 A are shown in Fig. 29 (a) and (b), respectively. The experimental waveforms show stable operations at a 1 MHz high frequency switching in steady state with ZVS soft switching capability in the primary switches. However, the output voltage shows high frequency ringing induced of parasitic components.



(a)

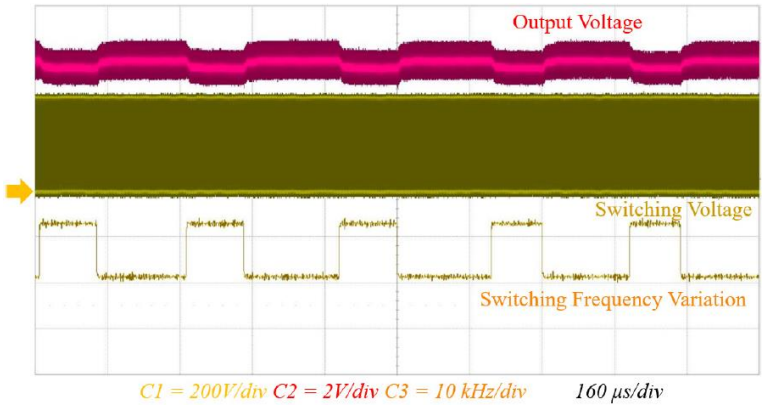


(b)

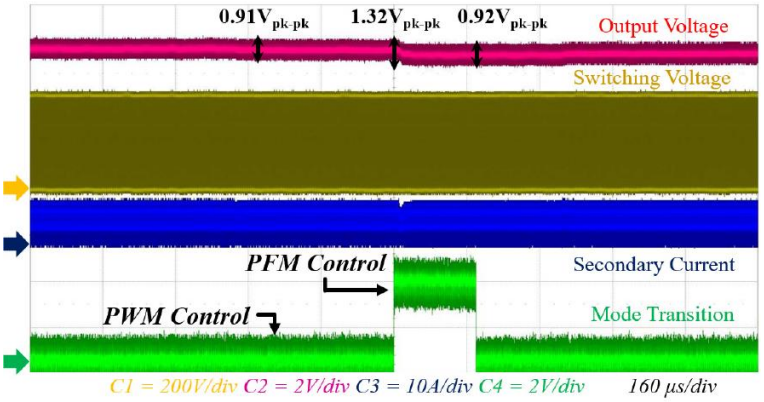
Fig. 30. Experimental waveforms of ZVS and hard switching condition based on the duty cycle: (a) at the minimum duty cycle of the hybrid control (84%), (b) at an improper duty cycle (70%) for hard switching.

From (64), the long dead time duration can induce hard switching operation which results in high switching loss in the primary MOSFETs. Fig. 30 shows the ZVS and the hard switching operations based on the duty cycle range. In Fig. 30, the charging and discharging current of the output capacitance can make undesired current spikes and drain-source voltage drop in the primary MOSFETs. Therefore, the minimum duty cycle of the hybrid control (84% of duty cycle) obtains ZVS operation, while an improper duty cycle (70% of duty cycle), which is smaller than the minimum duty cycle shows hard switching operation in the primary MOSFETs.

Fig. 31 (a) shows experimental results of the output voltage regulation performance using the conventional PFM control at full load. As shown, there are serious output voltage variations starting from when the switching frequency varies. However, in Fig. 31 (b), there are two transition steps changed by the switching frequency and the duty cycle. The duty cycle is determined by a continuous duty cycle control after the single $T_{b,prd}$ is changed by the proposed control mode decision algorithm. In Fig. 31 (b), the output voltage ripple regulated by the proposed hybrid control including the duty cycle control is smaller than that of the conventional PFM control.



(a)

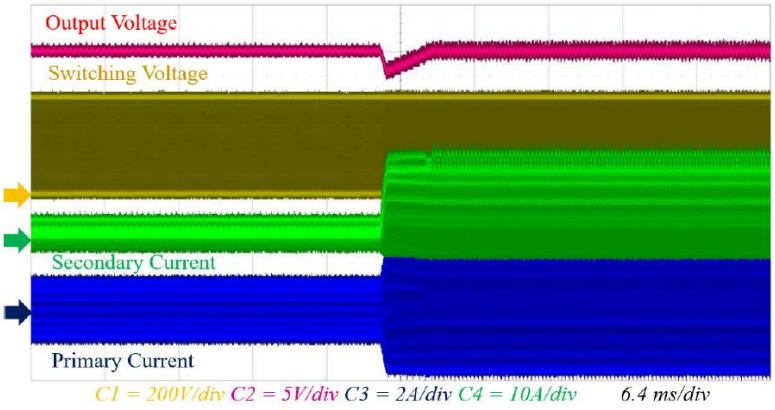


(b)

Fig. 31. Experimental waveforms according to switching frequency variations: (a) using the conventional PFM control method, (b) using the proposed hybrid control method.

The single PI gain is designed to compensate the steady state error of the output voltage. The value of the PI gain was determined through experimental trials and tested over the operating range to ensure proper operation. The step load response of the power converter verifies the stability of the hybrid control method indirectly. Step load responses from 2 A to 12 A and from 12 A to 2 A load are shown in Fig. 32. In Fig. 32 (a) and (b), the conventional PFM control shows relatively fast dynamic performance (4.6 ms during step-up and 4.5 ms during step-down). In Fig. 32 (c) and (d), the proposed

PWM and PFM hybrid control algorithm shows slower dynamic performance (5 ms in step-up case and 9.3 ms in step-down case) because the proposed method requires longer processing time to decide the appropriate PWM and PFM control modes in order to precisely regulate the output voltage. The slow dynamic performance is area of improvement for the proposed hybrid control algorithm, however, the output voltage disturbances at the step load changes are not more serious than that of the conventional PFM method. In addition, the precise output voltage regulation and the stable operations in the primary- and secondary-side currents are significant advantages in steady state operation.



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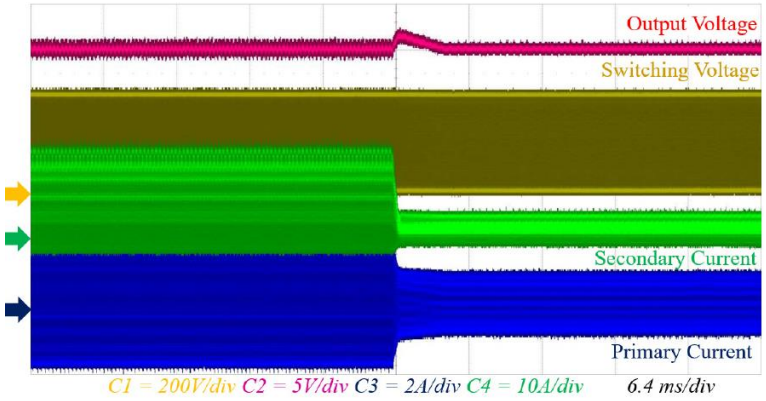

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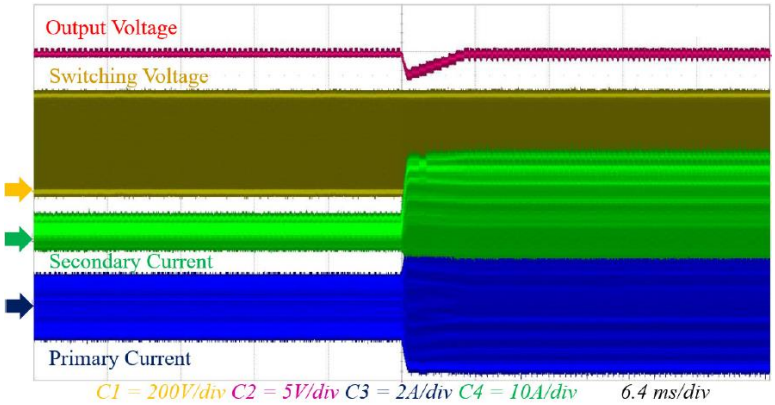

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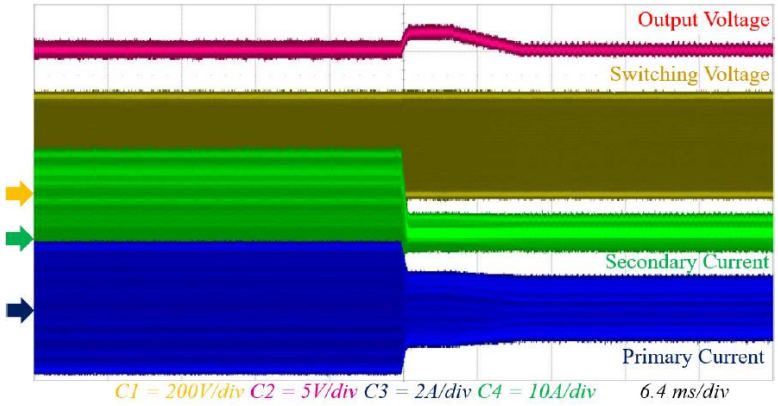


(d)

Fig. 32. Experimental waveforms of step load responses according to load variations and controllers: (a) from 2A to 12A with the PFM control, (b) from 12 A to 2 A with the PFM control, (c) from 2 A to 12 A with the hybrid control, (d) from 12 A to 2 A with the hybrid control.

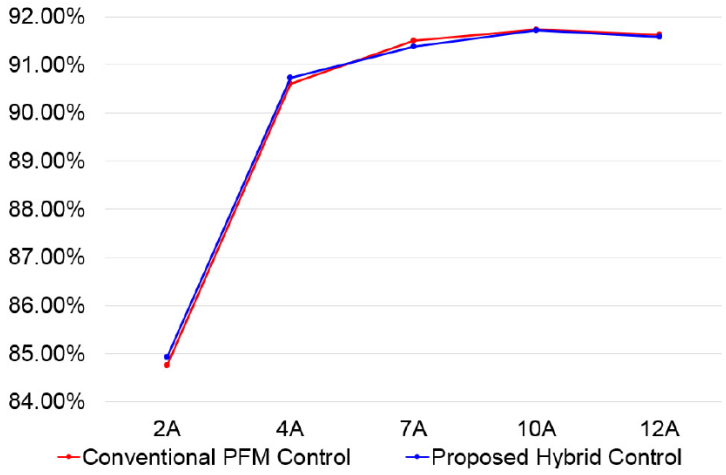


Fig. 33. Efficiency curves of the 240 W prototype converter.

Fig. 33 shows power conversion efficiency according to load variations at 1 MHz switching frequency. There is no difference in power conversion efficiency between the proposed and conventional methods. The efficiency chart shown in Fig. 33 verifies that the proposed PWM and PFM hybrid control algorithm does not affect power conversion efficiency compared to the conventional PFM control because it improves only the output voltage control performance without changing the operating point of the converter.

3.3 FPGA Controller Design

An FPGA controller for an LLC resonant converter is implemented to improve both switching frequency resolution and dynamic performance by utilizing its high speed and intrinsic parallelism. The

improved performance of the FPGA controller is analysed using theoretical methods and compared to that of the DSP controller, and verified through circuit simulation and the experimental signal-level tests using the hardware-in-the-loop (HIL) test system.

3.3.A Switching Frequency Resolution Enhancement

The general-purpose DSP (TI TMS320F28335) and the proposed FPGA (Xilinx XC7A100T) controller have 150 MHz and 450 MHz clock frequency, respectively. The clock speed determines the time step used to generate the triangular waveform that implements the pulse frequency modulation (PFM) gate signals. The time steps can be calculated as follows:

$$T_{b,prd} = \frac{T_s}{2T_{tb,clk}} \tag{65}$$

where $T_{b,prd}$ is the number of time steps, T_s is the switching period, and $T_{tb,clk}$ is the period of the system clock. $T_{b,prd}$ determines the switching frequency resolution by a single bit change in control variables. The switching frequency resolution can be calculated as follows:

$$\Delta f_s = \frac{1}{2T_{tb,clk}}\left(\frac{1}{T'_{b,prd}} - \frac{1}{T_{b,prd}}\right) \tag{66}$$

From (65) and (66), the DSP controller has 75 $T_{b,prd}$ steps and 13.158 kHz switching frequency resolution at 1 MHz switching frequency. The FPGA controller has 225 $T_{b,prd}$ steps and 2.2 kHz frequency resolution. From (65), the input-output voltage gain variation can be derived in terms of $T_{b,prd}$ as follows:

$$G\left(\Delta T_{b,prd}\right) = \left\| H_r\left(\frac{T'^{-1}_{b,prd}}{2T_{tb,clk} f_r}\right) - H_r\left(\frac{T^{-1}_{b,prd}}{2T_{tb,clk} f_r}\right)\right\| \tag{67}$$

where H_r is the voltage gain of the LLC resonant converter and f_r is the resonant frequency. From (67), when the input and output voltages are 400 V and 20 V, the output voltage resolutions of the LLC resonant converter using the DSP and FPGA controllers are 200 mV and 13.4 mV, respectively. They are larger than the sampling resolution, 4.88 mV, of the 12 bit ADC which are used in the controllers. Having lower output voltage resolution than the ADC sampling resolution induces high steady state error in the output voltage regulation. The controller frequently changes the switching frequency to compensate the error, which generates large output voltage ripple and primary- and secondary-side current fluctuation. However, the FPGA controller has 15 times smaller output voltage variation than that of the DSP controller, which induces the primary- and secondary-side current variations.

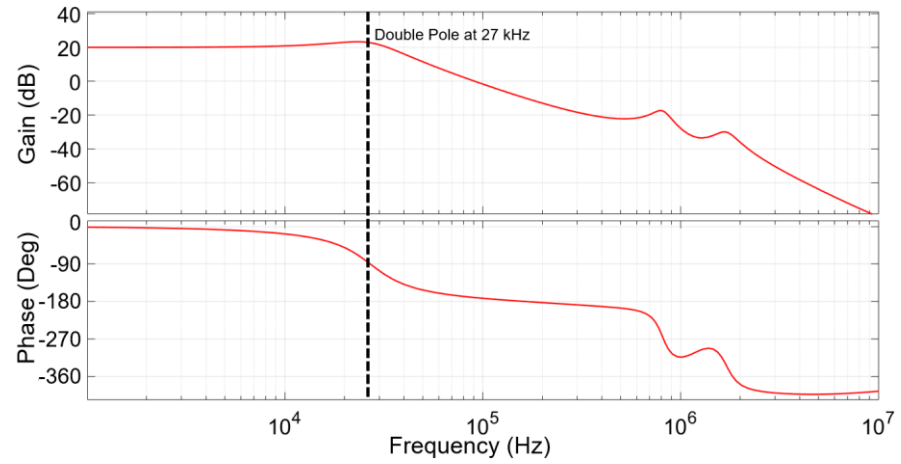
3.3.B Enhancement of Dynamic Performance

The LLC resonant converter operating at high switching frequency has a high crossover frequency

in the open loop transfer function due to the high resonant frequency and small output capacitance. An ideal digital controller completes all the computation processes and updates the switching frequency within a single switching period. However, with a typical digital controller is difficult to achieve the cycle-by-cycle control at high switching frequency due to its limited computational speed. The DSP and FPGA controller require 14 μs time delay (= 72 kHz delayed frequency, f_d) and 2 μs delay for the computation, respectively, to complete a single control process. The transfer function of the time delay can be derived as follows:

$$G_{delay}(s) = \frac{1 - e^{-sT_{delay}}}{sT_{delay}} \tag{68}$$

where T_{delay} is the time delay. It makes the drastic decrease of gain and phase near the delayed frequency. Therefore, the crossover frequency (i.e. control bandwidth) should be sufficiently lower than the delayed frequency to avoid drastic phase drop.



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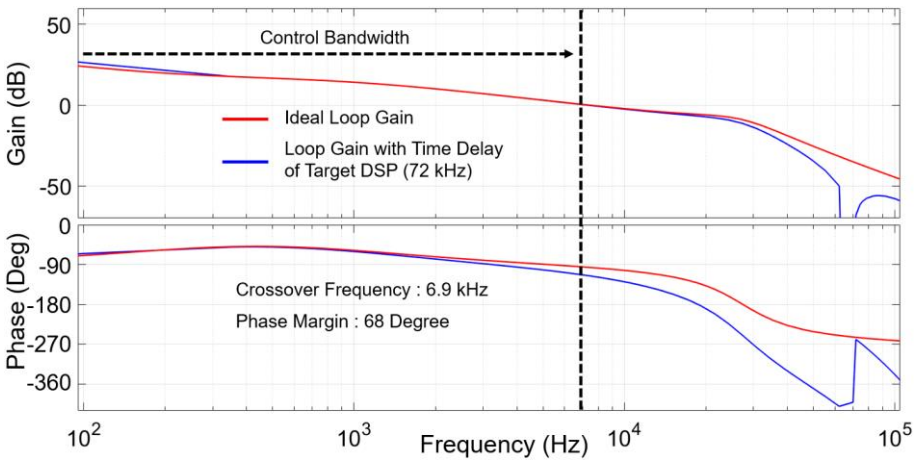

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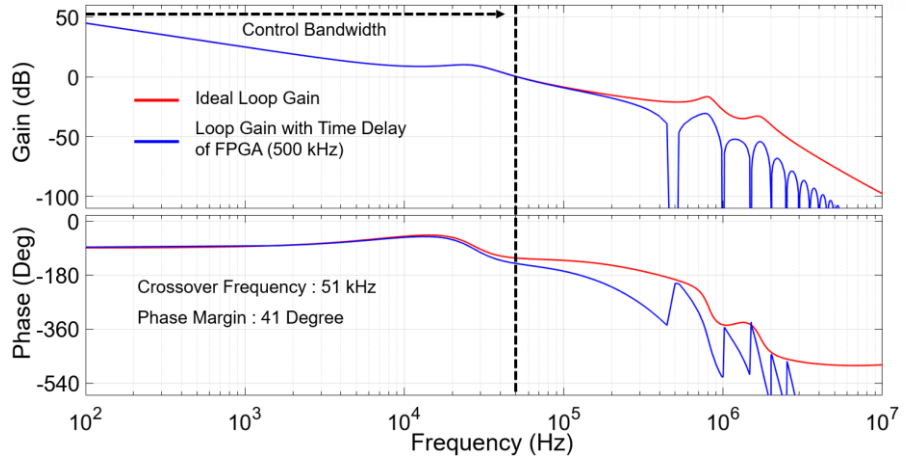


(c)

Fig. 34. Theoretical loop gain according to the controller: (a) Transfer function of the LLC resonant converter, (b) Loop gain of the general-purpose DSP, (c) Loop gain of the designed FPGA controller.

Fig. 34 shows the theoretical transfer function and loop gain of LLC resonant converter using MATLAB. The LLC resonant converter can obtain a high control bandwidth with the first double pole compensation as shown in Fig. 34 (a). However, the DSP controller cannot obtain high control bandwidth because the crossover frequency should be lower than the first double pole frequency to avoid drastic phase drop. On the other hand, the FPGA controller can achieve higher control bandwidth than that of the DSP controller, since the 500 kHz delayed frequency is sufficiently far from the first double pole.

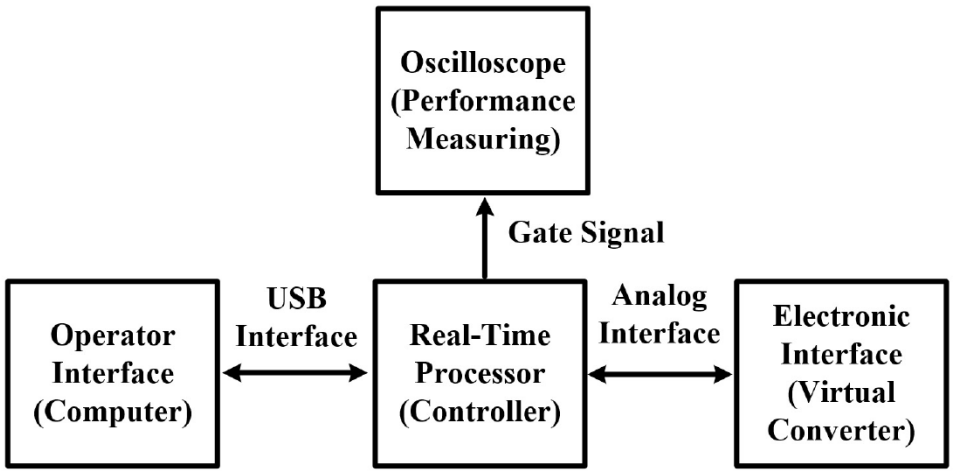


Fig. 35. Hardware-in-the-Loop system for the signal-level test.

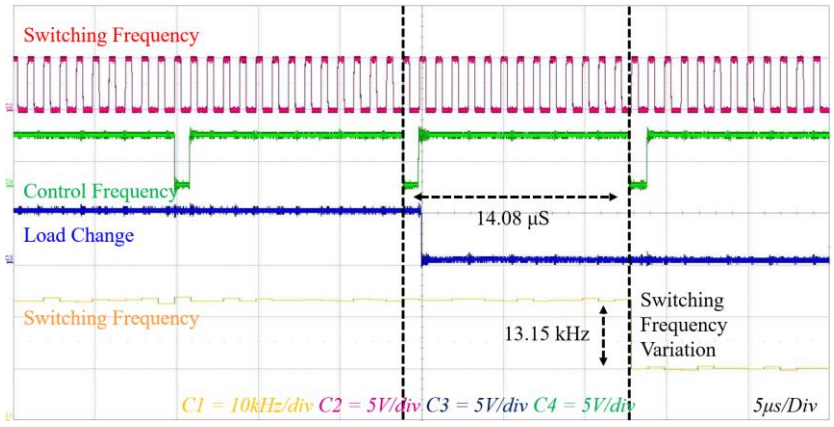
The DSP controller does not require the first double pole compensation, because it has drastic phase drop near the first double pole. A two-pole and one-zero (2P1Z) compensator has a pole at the origin to eliminate steady state error and a single zero to boost the phase margin. The additional pole results in -

20 dB/dec gain drop after the single zero such that the crossover frequency is located before the first double pole. The 2P1Z compensator shows 14 times higher control bandwidth (7 kHz crossover frequency) than that of the PI compensator (495 Hz crossover frequency), as shown in Fig. 34 (b).

The FPGA controller requires the first double pole compensation, because it shows drastic phase drop at high frequency region (500 kHz). A three-pole two-zero (3P2Z) compensator has a single pole at the origin, double zero at the first double pole, and double pole after the crossover frequency to achieve enough phase margin and enough damping at high frequency region. The theoretical results show that the FPGA shows approximately seven times higher control bandwidth (51 kHz crossover frequency) than that of the DSP controller, as shown in Fig. 34 (c).

3.3.C Verification by HIL Tests

Fig. 35 shows the HIL test structure to implement the signal-level test. The HIL test system operates as a virtual converter which changes the measured output voltage according to the load variation. The controller obtains the real-time dynamics of the output voltage measurement through the analog interface, which shows the switching frequency resolution and computation performance [37], [38].



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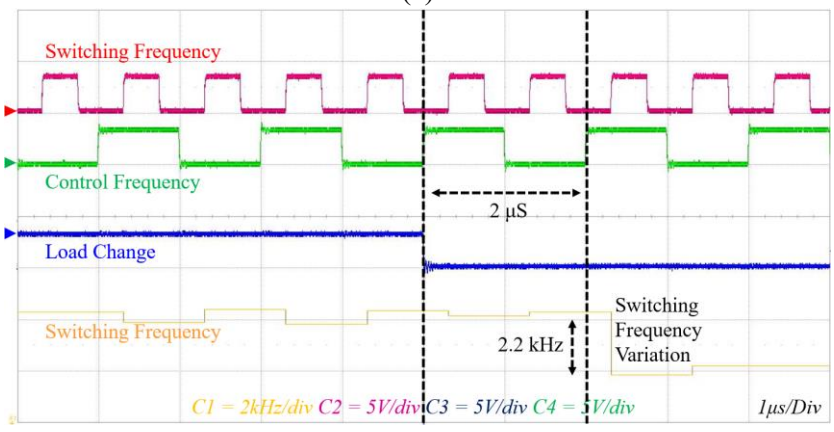
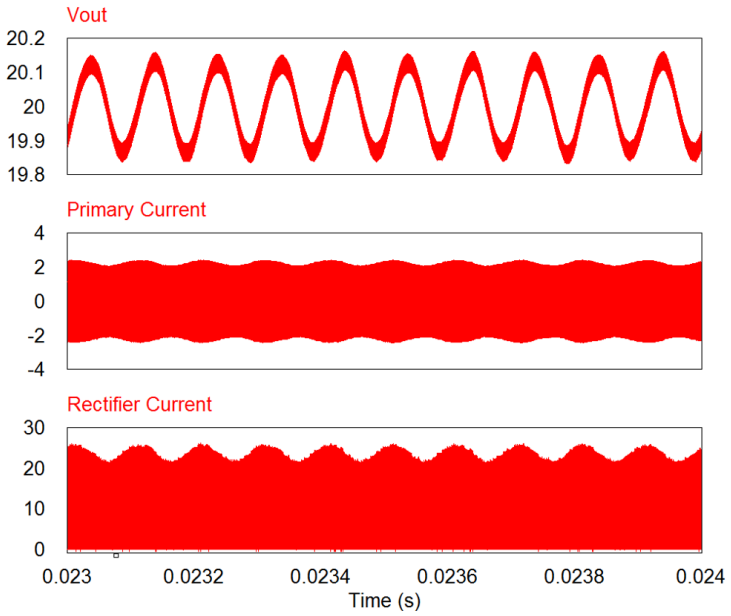


(b)

Fig. 36. Comparison of time delay and switching frequency resolution: (a) Signal-level test with DSP controller, (b) Signal-level test with FPGA controller.

The time delay and switching frequency resolution are measured by experimental signal-level tests shown in Fig. 36. the FPGA controller shows seven times smaller time delay (2 μs) than that of the DSP controller (14.08 μs). In addition, the FPGA controller has approximately 5.9 times higher switching frequency resolution (2.2 kHz) than that of the DSP controller (13.15 kHz). It induces 5.9 times smaller output voltage fluctuation by the limited switching frequency resolution.



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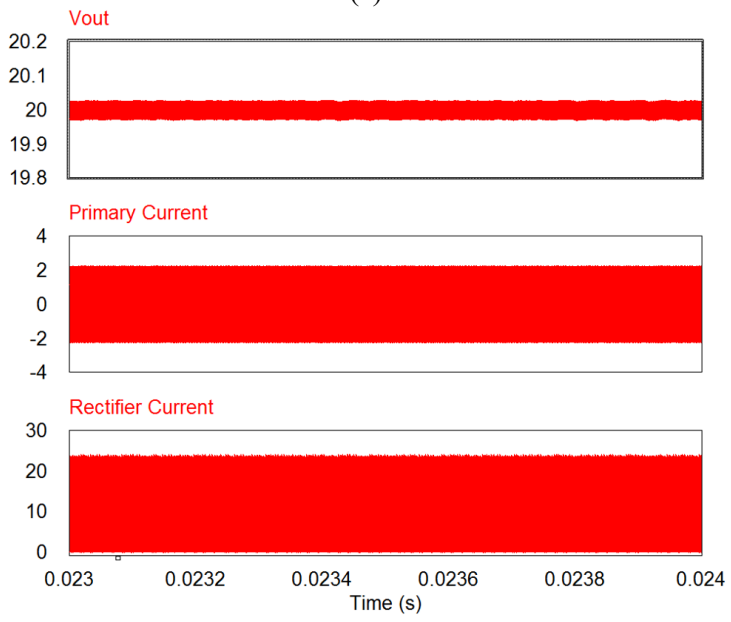
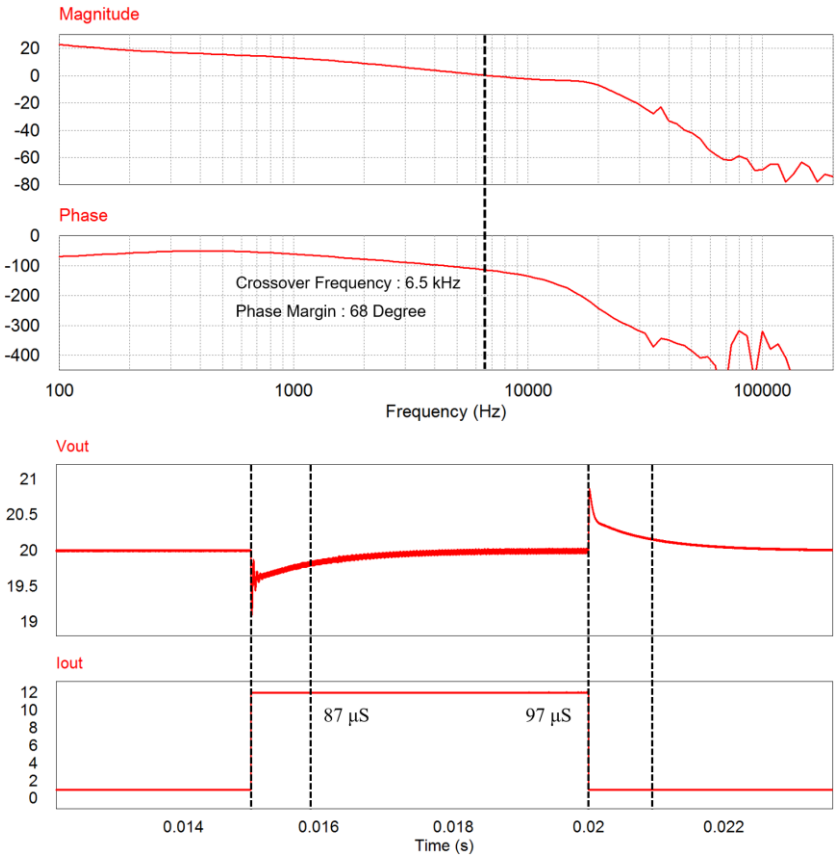


(b)

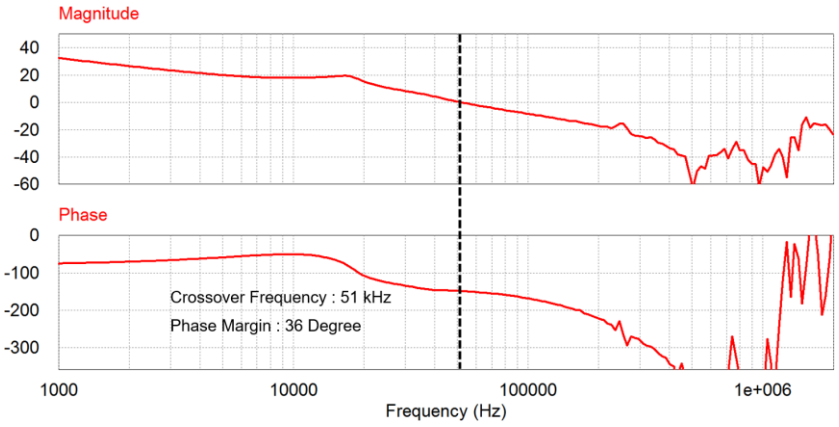
Fig. 37. Simulation results of output voltage ripple according to controller types: (a) DSP controller case, (b) FPGA controller case.

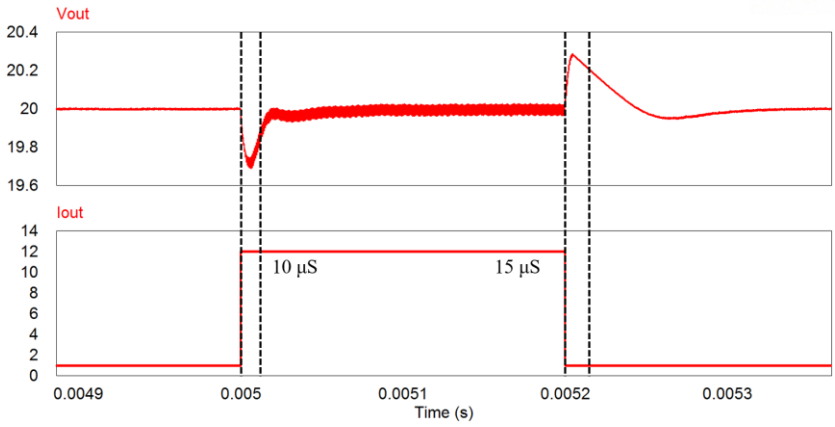
Using the switching frequency resolution and computation time, the simulation model can be

designed to measure the output voltage ripple and small signal response according to the controllers. Fig. 37 shows the output voltage ripple and primary- and secondary-side current variation using PSIM simulation software. The FPGA based converter reduces output voltage ripple (83 %) and primary and secondary-side peak current variation (19.1 % and 16.5 %, respectively) compared with the DSP based converter. All the performance improvements are listed in Table IV, where $V_{o,r}$ is the output voltage ripple, $I_{p,p}$ is the primary side peak current, $I_{s,p}$ is the secondary side peak current, and T_{up} and T_{down} are the load transient time according to load increment and decrement, respectively.



(a)





(b)

Fig. 38 Loop gain and step load response according to controller types: (a) DSP controller case, (b) FPGA controller case.

Fig. 38 verifies theoretical control bandwidth and dynamic performance. The FPGA controller has 51 kHz crossover frequency which is 7.28 times higher than that of the DSP controller. In the time domain, it shows the dynamic performance with output voltage settling time (1 % voltage error) based on the load variations. The settling time of the FPGA controller is 8.7 times (increment) and 6.5 times (decrement) faster than that of the DSP controller, respectively.

Table IV Converter Performance according to Controller Types

Specification	DSP Controller	FPGA Controller
$V_{o,r}$	0.366 V	0.062 V
$I_{p,p}$	2.767 A	2.238 A
$I_{s,p}$	28.549 A	23.838 A
T_{up}	87 µs	10 µs
T_{down}	97 µs	15 µs

In the view point of cost-effectiveness, the implemented FPGA (XC7A100T-1CSG324C) is five times more expensive than the DSP (TMS320F28335). However, the price of the FPGA chip depends on the number of look-up tables (LUT). The implemented FPGA controller uses only 2,069 LUTs, which corresponds 3 % of total LUTs. It also uses one DSP slice out of 240 total DSP slices and 63 slice registers out of 126,800 slice registers. The price of the FPGA can be reduced if we use an FPGA with a smaller number of LUTs. For example, the price of XC7A15T-1FTG256C is similar to that of the DSP without any performance degradation.

IV. Spread Spectrum Technique for EMI Reduction

Previous Section II and Section III shows the increase of power density using the high switching frequency operation. In this section, the power density can be improved with small sized EMI filter. Recently, the electromagnetic interference (EMI) problems has become significant issues in a switching mode power supply (SMPS) to obtain small size, light weight, and high cost effectiveness with high functionality [39]. The electromagnetic compatibility (EMC) standards, such as FCC and CISPR define the limit of conducted emission (CE), which are usually regulated from 150 kHz to 30 Mhz. It requires the careful design of a power converter and its EMI filters. The EMI filter is usually assembled at the front side of the SMPS, which is connected to AC utility lines to reduce the CE noises. To effectively prevent the CE noises, large CM chokes with big capacitors or multistage CM chokes are required, which increases the size and the cost of the EMI filter [40]. Moreover, the value of the Y-capacitor is limited by the safety issues on leakage currents [41]. Several methods have been suggested to reduce the CE noises, such as an electromagnetic band gap (EBG) filter, passive cancellation, and an active EMI filter [42]-[45]. However, these methods require additional components for their implementation, and the size and the cost of the additional components also should be considered.

Spread spectrum technique (SST) has been suggested to effectively mitigates the CE noises without any additional components for the EMI reduction [46]-[49]. All the SST's modulation methods can be implemented with control algorithms using a digital signal processor (DSP) or a field programmable gate array (FPGA), which improves cost-effectiveness of power converter. In previous research, the SST was widely applied to small-sized power supplies such as buck, boost, and flyback converters, since the continuous conduction mode (CCM) operation of those topologies is insensitive to the input-output voltage gain according to the switching frequency variation caused by the SST [50]-[55]. However, available topologies are limited to adopt the SST in terms of tight output voltage regulation. The limited topologies impose restrictions on their available applications.

Resonant converters are widely used to various industrial applications, such as lightings, TVs, computers, and home appliances. In addition, the resonant converters show high power conversion efficiency at the high switching frequency operation because of their soft-switching capability. However, the resonant converters are sensitive to the input-output voltage gain according to the switching frequency variation caused by the SST. In [55], the SST is applied to the series resonant inverter for induction heating (IH) applications. However, the IH application does not require the output voltage regulation. In this research, control and design methods are proposed to implement the SST in the resonant converter.

4.1 PFM-PSM Hybrid Control Algorithm for SST

The spread spectrum has been introduced to mitigate the EMI with several branches' techniques, such as sinusoidal, triangular, Hershey kiss, and random modulation. Fig. 39 shows the EMI reduction using the spread spectrum technique. It has switching frequency variations within the range of f_c-$\Delta f < f_c < f_c$-Δf, where f_c is the carrier frequency and Δf is the frequency deviation of the spread spectrum. The frequency modulation of the carrier frequency due to the spread spectrum is expressed as follows:

$$s(t) = A_o \cos\left(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau) d\tau \right) \tag{69}$$

where A_o is the amplitude of the signal, $-1 \le \xi \le 1$ is the driving signal which expresses the frequency variation for the spread spectrum. The power of $s(t)$ is equal to $A_o^2/2$, which can be scattered using the spread spectrum technique.

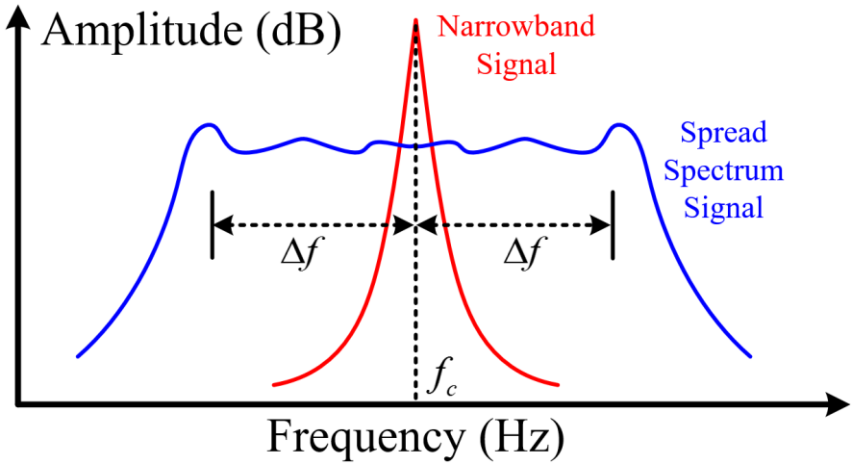


Fig. 39 Comparison between narrowband interfering signal and spread spectrum signal.

In this section, a hybrid control method using the PFM and phase shift modulation (PSM) is proposed to reduce the EMI noise emission as well as to regulate the output voltage of the LLC resonant converter. The triangular modulation is used as the spread spectrum technique. The PFM determines the carrier frequency of the spread spectrum according to the load variations. The instantaneous switching frequency is determined by the triangular modulation, but it can induce large output voltage fluctuation. Therefore, the PSM is applied to compensate the output voltage fluctuation according to the switching frequency vibration caused by the spread spectrum. The output voltage regulation and the EMI reduction performance using the spread spectrum are verified using a 500 W prototype LLC resonant converter.

4.1.A Control Algorithm for EMI Reduction

Fig. 40 shows the circuit diagram of the proposed LLC resonant converter which has a full bridge structure to implement the PSM [56]. It has the PFM and PSM controller to regulate the output voltage under the spread spectrum. After the PFM and PSM controller, the spread spectrum generator implements the triangular frequency modulation. The conventional PFM controller changes the switching frequency to compensate the output voltage variation according to the load variation. However, it is equal to the carrier frequency variation of the spread spectrum technique. The switching frequency variation mixed by the PFM and the spread spectrum cannot achieve the designed EM noise reduction as well as the output voltage regulation. In this paper, a hybrid control method is proposed, which has two operational modes to achieve the EM noise reduction and the output voltage regulation at the same time. First mode is the steady state operation, and the second mode is the transient operation.

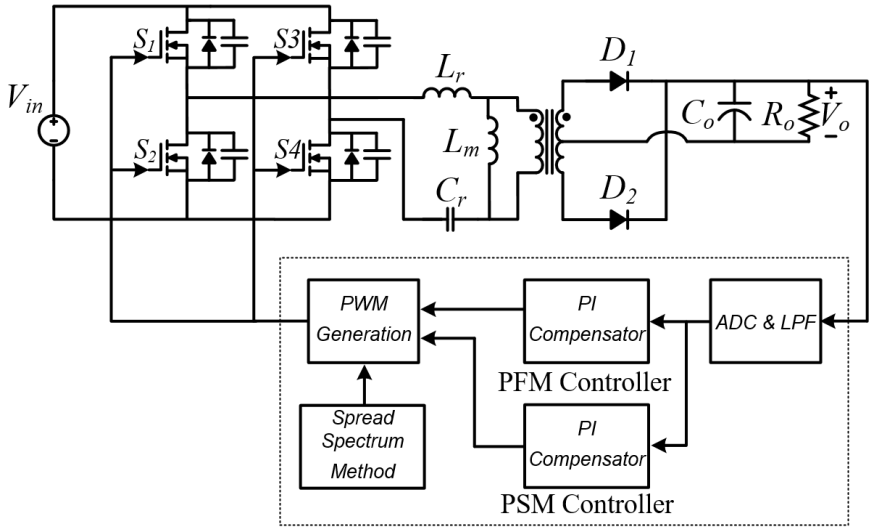
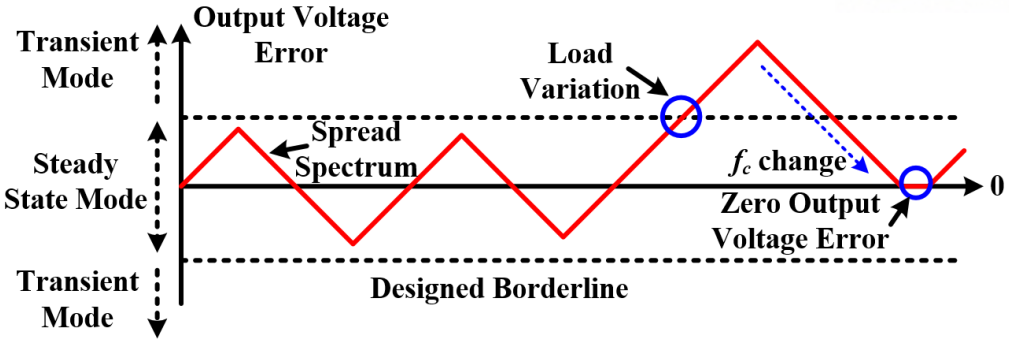


Fig. 40 Scheme of LLC resonant converter for spread spectrum technique.

Fig. 41 (a) shows the output voltage error variation in the proposed control algorithm. The proposed control algorithm has the borderline to the output voltage error to determine the operational modes. In the steady state mode, the triangular frequency modulation changes the switching frequency to implement the spread spectrum. The PSM only operates to regulate the output voltage of the LLC resonant converter. The PFM does not operate in this mode because of the triangular frequency modulation for the spread spectrum. Therefore, the controller regulates the output voltage using the PSM under the spread spectrum with the triangular frequency modulation. The reduction of EMI peak using the spread spectrum was introduced in [46]. The large switching frequency variation($\triangle f$) and the low triangular modulation frequency (f_m) can reduce the peak EMI value. Fig. 41 (b) shows the relative peak level reduction according to the $\triangle f/f_m$ ratio. In this paper, the designed EMI peak reduction is 14 μdB less than no spread spectrum case.



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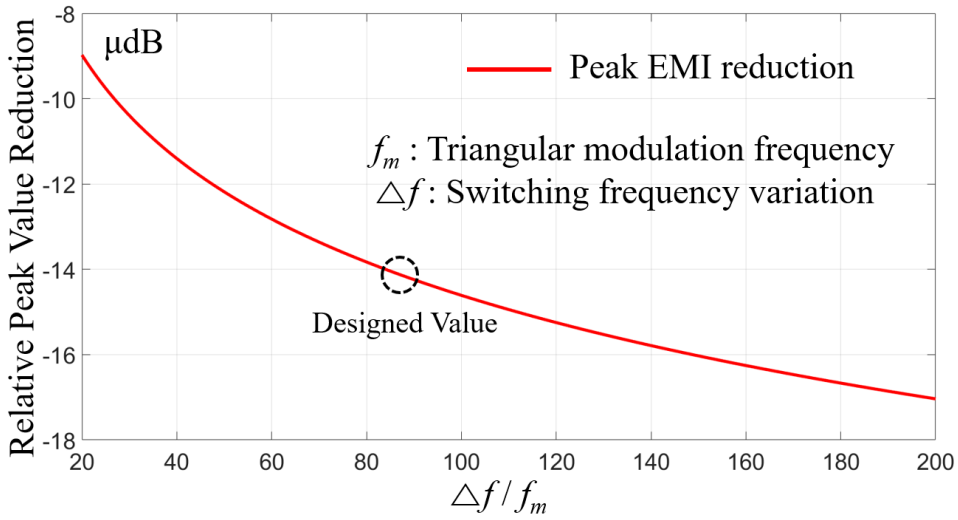

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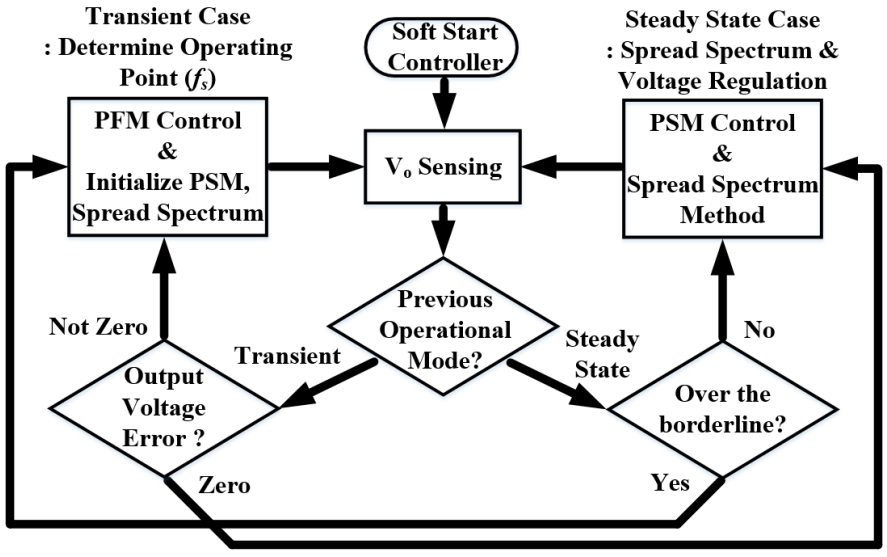


(c)

Fig. 41 Proposed control algorithm: (a) Output voltage error variation, (b) Peak conducted EMI level according to $\triangle f/f_m$ ratio, (c) Control sequences.

If the output voltage error is over the borderline, the controller operates in the transient mode. In this mode, the PFM rearranges the carrier frequency to regulate the output voltage, because the PSM has

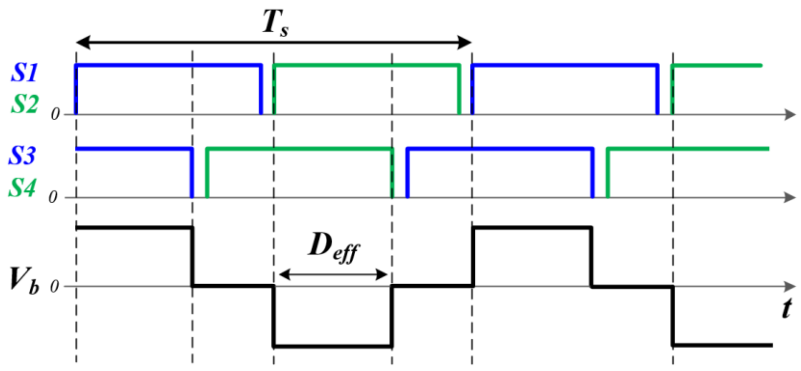
limited output voltage regulation range. In addition, small phase shift induces small circulating power and rms current. The PSM and the triangular frequency modulation does not operate in the transient mode but initialize these values. If the output voltage error is converged to zero, the controller operates in the steady state mode. Fig. 41 (c) shows the block diagram of the proposed control algorithm. It also shows two operational conditions to implement the spread spectrum technique and the output voltage regulation.

4.1.B Output Voltage Regulation

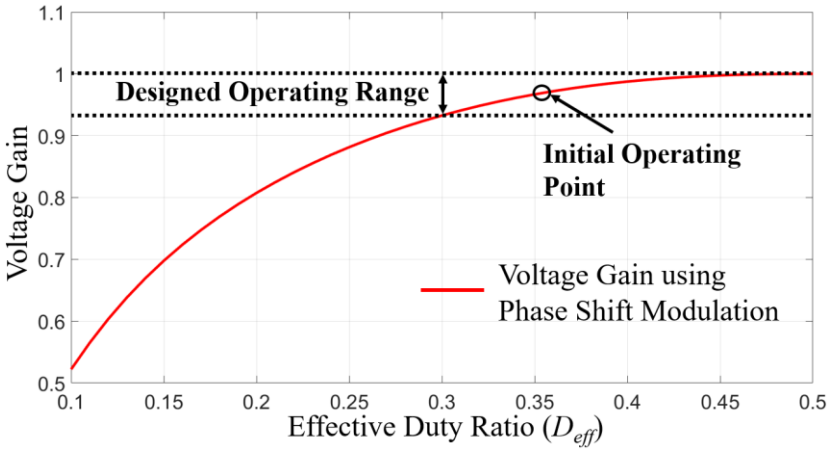
The LLC resonant converter using only the spread spectrum technique shows the maximum output voltage variation which can be derived as follows:

$$\Delta V_{o,\max} = \frac{G(f_s + \Delta f_{\max}) \cdot V_{in} - G(f_s - \Delta f_{\max}) \cdot V_{in}}{n} \tag{70}$$

where $G(f)$ is the converter's input-to-output voltage gain, V_{in} is the input voltage, Δf_{max} is the maximum switching frequency variation, and n is the transformer's turn ratio. It shows that the large switching frequency vibration from the triangular frequency modulation of the spread spectrum can induce serious output voltage variations without any compensating techniques.



(a)



(b)

Fig. 42 PSM control method: (a) Operational waveform, (b) Voltage gain.

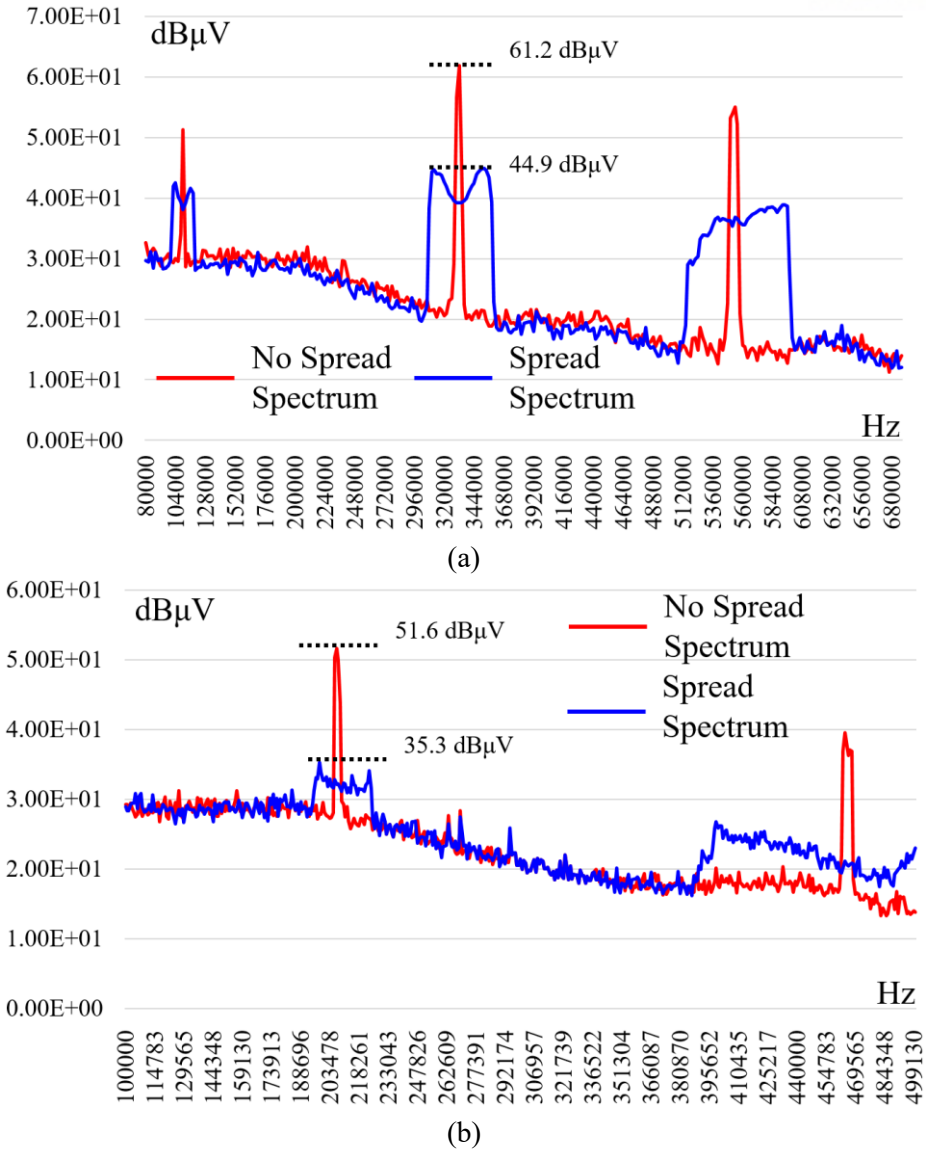


Fig. 43 Reduction of EMI noise: (a) Common mode noise, (b) Differential mode noise.

The PSM is adopted to compensate the output voltage fluctuation caused by the spread spectrum in the steady state operation. The PSM's voltage gain can be derived as follows:

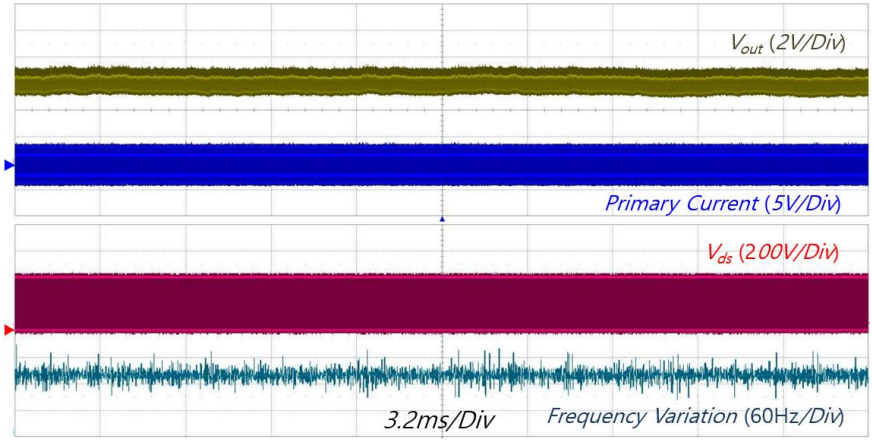
$$G(d_{eff}) = \frac{1-\cos\left(2\pi d_{eff} / f_n\right)}{1+\frac{4Q}{\pi f_n}-\frac{\pi^2 d_{eff}}{k f_n^2}\left(\frac{1}{2}-d_{eff}\right)+\cos\left(\frac{2\pi d_{eff}}{f_n}\right)\left[\frac{4Q}{\pi f_n}+\frac{\pi^2 d_{eff}}{k f_n^2}\left(\frac{1}{2}-d_{eff}\right)-1\right]+\frac{\pi d_{eff}}{k f_n}\sin\left(\frac{2\pi d_{eff}}{f_n}\right)} \quad (71)$$

where d_{eff} is the amount of the phase shift using the PSM, f_n is the normalized frequency ($f_s/f_{s,n}$), $f_{s,n}$ is the reference switching frequency, k is the magnetizing and the resonant inductance ratio (L_m/L_r), and Q is the quality factor. Fig. 42 (a) and (b) show the operational waveforms and the voltage gain of the PSM, respectively. In Fig. 42 (b), the PSM can achieve only step-down in the output voltage. The initial operating point of the PSM is important to compensate the output voltage error according to the spread

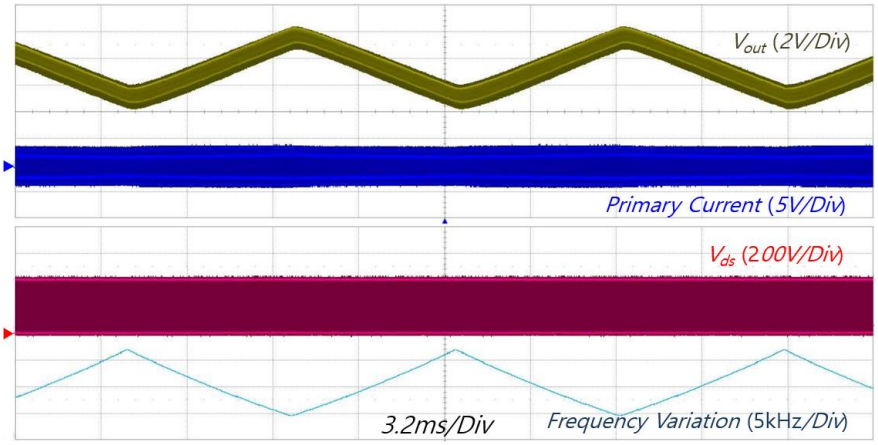
spectrum, because it requires both the step-up and step-down capabilities in the output voltage. The required voltage gain using the PSM can be derived as follows:

$$G_{re} = G(f_c + \Delta f) \cdot G(d_{eff,\max}) = G(f_c - \Delta f) \cdot G(d_{eff,\min}) \tag{72}$$

where $d_{eff,min}$ and $d_{eff,max}$ is the minimum and maximum effective duty ratio, respectively, and G_{re} is the required voltage gain. The initial operating point can be derived as $G(d_{eff,ini}) = \{G(d_{eff,max}) + G(d_{eff,min})\}/2$.



(a)



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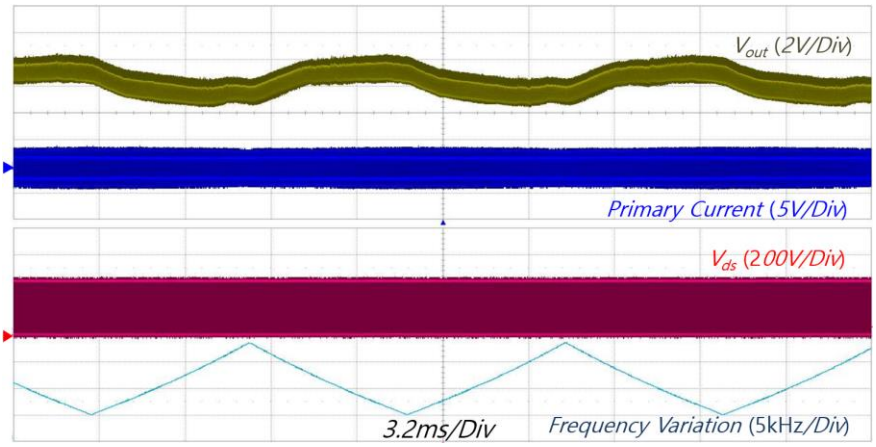

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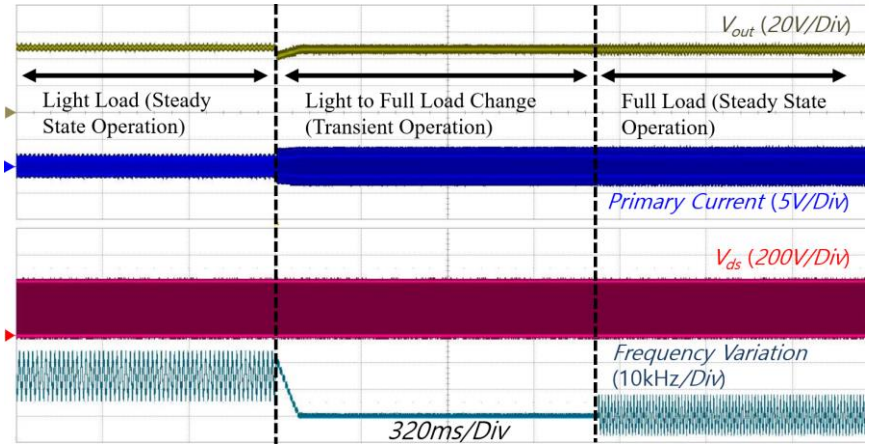


(d)

Fig. 44 Operational waveforms: (a) No spread spectrum, (b) Spread spectrum without compensation, (c) Spread spectrum with compensation, (d) Mode transition.

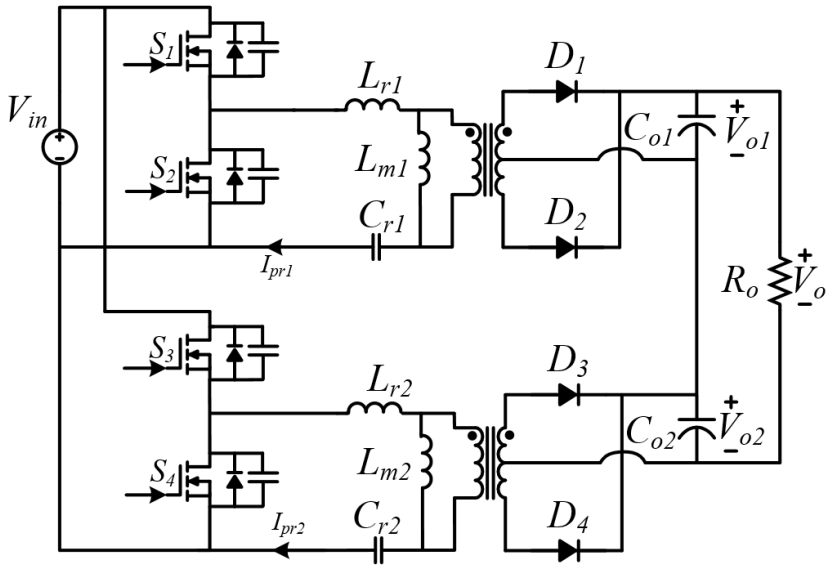
4.1.C Experimental Results

Fig. 43 (a) and (b) show the peak common mode and differential mode noises, respectively. The spread spectrum technique using the triangular modulation reduces the EM noise effectively. The specification of the power converter and the spread spectrum technique used in the experiment is described in Table V. Fig. 44 shows the comparison of the output voltage regulation performance. If the PSM is not used to compensate the output voltage ripple according to the spread spectrum, the LLC resonant converter has 2.6 times higher output voltage ripple than the no spread spectrum case as shown in Fig. 44 (b). However, the PSM compensation has 0.58 times smaller output voltage ripple than the no compensation case as shown in Fig. 44 (c), which is 1.5 times higher output voltage ripple than the no spread spectrum case. Table VI shows the comparison of the output voltage fluctuation and the EM noise. Fig. 44 (d) shows mode change cases between the steady state and the transient modes.

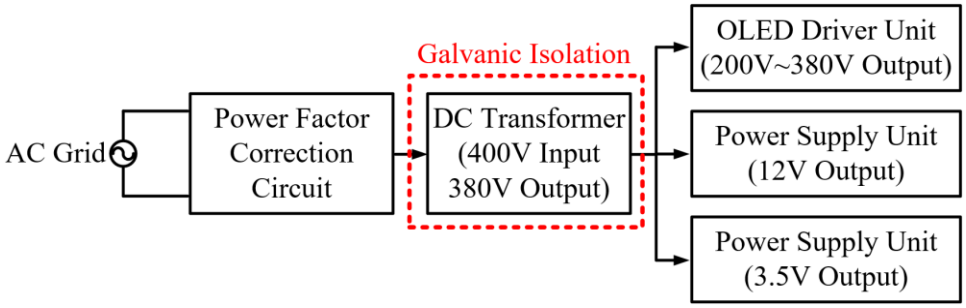
4.2 Enhanced Phase Shift Algorithm for SST

In this section, a parallel-series LLC resonant converter using an enhanced phase shift algorithm of the frequency modulation of the SST is proposed to suppress the EM noise emission as well as to tightly regulate the output voltage [57]. The PFM determines the carrier frequency of the spread spectrum according to the load variations. The triangular modulation is applied to the SST to obtain performance balance between the EMI reduction and easy of implementation. In addition, the parallel-series structure and the proposed phase shift algorithm can mitigate the output voltage fluctuation according to the SST. Using the proposed methods, the SST can be continuously applied to the converter, which does not depend on the load variation. The operational principles of the proposed parallel-series LLC resonant converter employing the phase shift algorithm, and the reduction of the output voltage fluctuation will be analyzed to obtain design considerations and to estimate performance improvements. The output voltage regulation and the EMI reduction performances using the SST will be verified using a 600 W

prototype parallel-series LLC resonant converter.



(a)



(b)

Fig. 45 Schematic of the proposed converter and system: (a) parallel-series LLC resonant converter, (b) entire input power structure of OLED TV.

Fig. 45 (a) shows the schematic of the parallel-series LLC resonant converter which has a parallel connection on the primary side and a series connection on the secondary side. The target application of the converter is a DC transformer for flat panel display (FPD) applications, especially an organic LED (OLED) TV, which has the specification of 400 V input voltage and 380 V output voltage. Fig. 45 (b) shows the entire input power structure of the OLED TV, which requires the DC transformer to achieve a galvanic isolation between the AC grid to the TV side. In addition, the OLED driver requires high output voltage (380 V) and low output current (1.58 A).

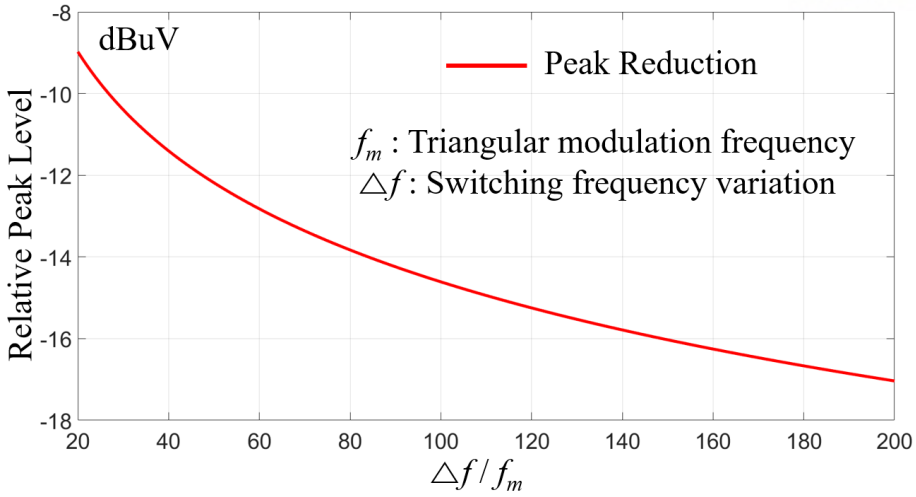


Fig. 46 Relative peak level of conducted emission EMI according to $\triangle f/f_m$.

4.2.A Compensation Algorithm for Output Voltage Regulation under SST

The SST can reduce the peak values of the EM noise. Using wide switching frequency variation ($\triangle f$) and low triangular modulation frequency (f_m), the converter employing the SST can obtain high EMI reduction performance. Fig. 46 shows the reduction of relative peak levels of conducted emission EMI according to $\triangle f/f_m$ ratio. In this study, the desired reduction level of the EMI peak is 10 dBuV comparing with the case without the SST.

The SST requires wide switching frequency variation to reduce the EM noise. The LLC resonant converter has serious output voltage fluctuation caused by the SST, since the voltage gain of the converter is determined by the switching frequency. The voltage gain of the LLC resonant converter can be derived as follows:

$$G(f_n)=\left|\frac{\lambda^{-1}f_n^{\,2}}{\left(\lambda^{-1}+1\right)f_n^{\,2}-1+j\left(f_n^{\,2}-1\right)f_n^{\,-1}}\right| \tag{73}$$

where λ is the resonant inductance and magnetizing inductance ratio and f_n is the normalized frequency. The output voltage variation according to the SST can be derived as follows:

$$\Delta V_{o,\max}=\frac{G\left(f_c+\Delta f_{\max}\right)\cdot V_{in}-G\left(f_c-\Delta f_{\max}\right)\cdot V_{in}}{n} \tag{74}$$

where $G(f)$ is the input-to-output voltage gain of the LLC resonant converter, V_{in} is the input voltage, $\triangle f_{max}$ is the maximum switching frequency variation, and n is the transformer's turn ratio. It shows that the wider switching frequency variation induces the larger output voltage fluctuation.

Fig. 47 (a) shows the theoretical operating waveforms of the switching frequency variation and the output voltage fluctuation of the converter according to the SST. In this case, the power converter uses a conventional in-phase modulation on the SST. All the switching legs have the same pattern for the switching frequency variation, which induces the same fluctuation shape of the output voltage (V_{o1} and

V_{o2}). It becomes the sum of V_{o1} and V_{o2} because of the series connection in the secondary output. The output voltage fluctuation of the parallel-series LLC resonant converter employing the SST can be derived as follows:

$$\Delta V_{o,c} = \left[G(f_c - \Delta f) - G(f_c + \Delta f)\right]\frac{V_{in}}{n_1} + \left[G(f_c - \Delta f) - G(f_c + \Delta f)\right]\frac{V_{in}}{n_2} \tag{75}$$

where $\Delta V_{o,c}$ is the output voltage fluctuation under the conventional in-phase modulation, and n_1 and n_2 are the transformer turn ratios. Therefore, the same variation of V_{o1} and V_{o2} induces serious output voltage fluctuation without any compensation method.

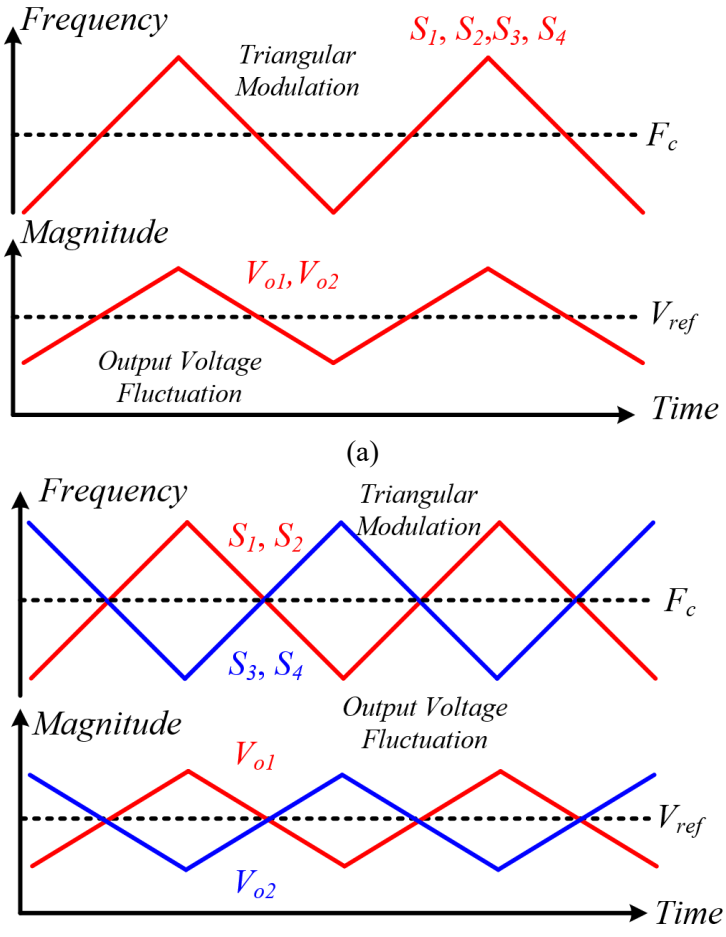


Fig. 47 Theoretical operating waveforms of the parallel-series LLC resonant converter employing the SST: (a) with the conventional in-phase modulation, (b) with the proposed phase shift algorithm.

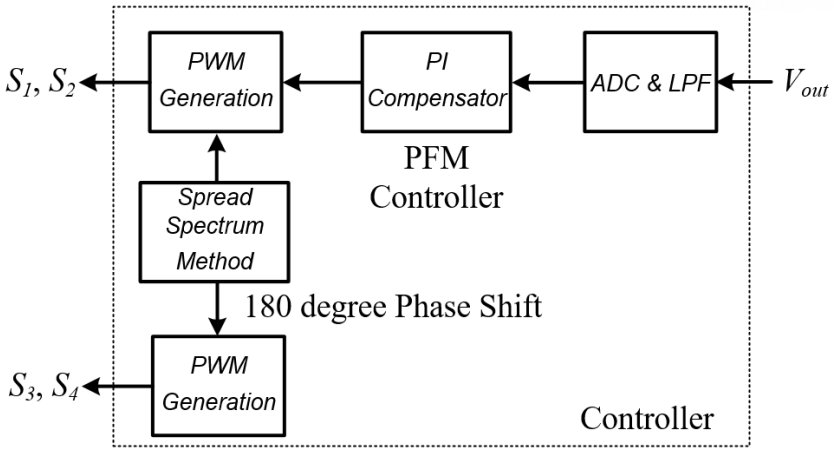
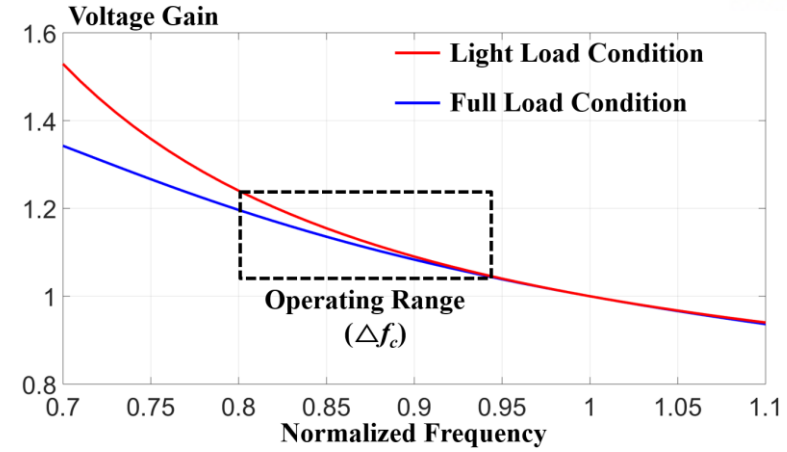


Fig. 48 Control block diagram of the proposed phase shift algorithm and SST.

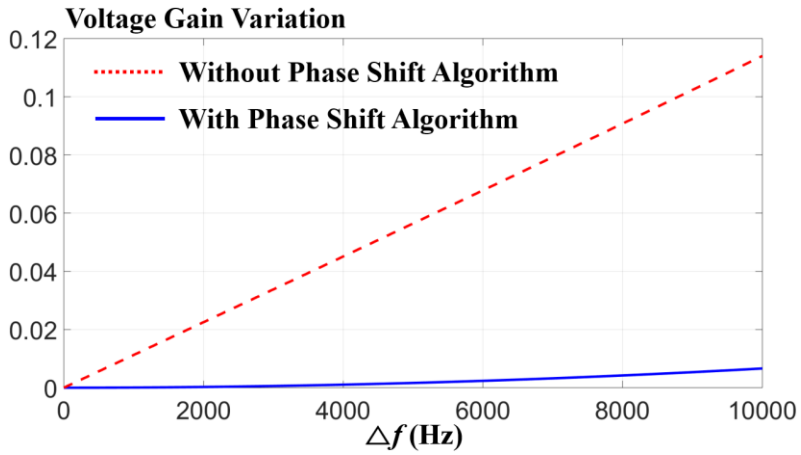
The parallel-series structure of the converter and the phase shift algorithm of the SST can solve this output voltage fluctuation problem under the spread spectrum operation. The parallel-series structure can independently control each output voltage of V_{o1} and V_{o2}. In addition, the performance of the output voltage regulation is determined by out of phase between V_{o1} and V_{o2}. Fig. 47 (b) shows the theoretical operating waveforms of the proposed phase shift algorithm and the output voltage fluctuation. The first converter shows in-phase switching pattern of the SST. The second converter shows 180° phase shifted switching pattern of the SST. The phase shifted switching pattern generates 180° phase shifted voltage variation according to the first converter. When n_1 and n_2 are same turn ratio, the output voltage fluctuation using the proposed algorithm and structure can be expressed as follows:

$$\Delta V_{o,p} = \left[\frac{G(f_c + \Delta f) + G(f_c - \Delta f)}{2} - G(f_c) \right] \frac{V_{in}}{n} \tag{76}$$

where $\triangle V_{o,p}$ shows the amount of the voltage variation using the proposed algorithm and structure, which is ideally compensated to zero. Fig. 48 shows the control block diagram of the proposed phase shift algorithm of the SST to mitigate the EM noise and to improve the output voltage regulation. The digital controller (TI TMS320F28335) is used to implement the proposed phase shift algorithm and the SST.



(a)



(b)

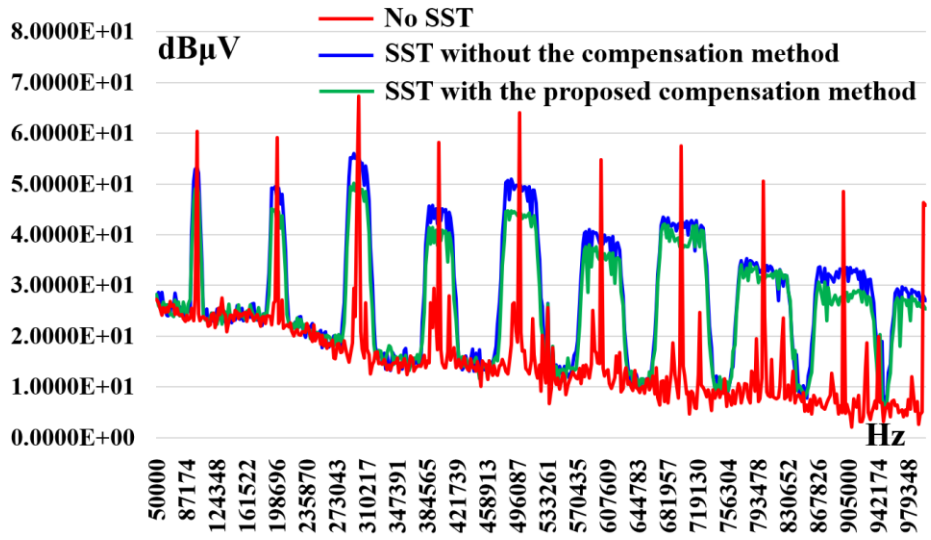
Fig. 49 Comparison of voltage gain variations: (a) non-linear characteristic of voltage gain according to load and operating frequency. (b) according to compensation by phase shift algorithm.

4.2.B Design Considerations of Voltage Gain

The voltage gain of the LLC resonant converter is non-linear. The proposed phase shift algorithm for the SST cannot make the output voltage ripple zero. The analysis of the output voltage variation according to the SST is significant to design the resonant network of the converter. Fig. 49 (a) shows the non-linear voltage gain curve of the LLC resonant converter, which operates under a specific switching frequency range to regulate the output voltage. The voltage gains show different slope according to load conditions. Using (75) and (76), Fig. 49 (b) shows the voltage gain variation using the proposed phase shift algorithm comparing with the conventional in-phase modulation case. The voltage gain variation with the conventional in-phase modulation is ten times larger than that with the proposed phase shift algorithm. In addition, they show the larger output voltage fluctuation under the wider frequency variation caused by the non-linear characteristic of the voltage gain.

4.2.C Experimental Results

Fig. 50 (a) and (b) show the quasi peak values of common mode and differential mode conducted emission EM noises, respectively. From Fig. 50, using the SST, all the EMI can effectively be reduced. Table VII describes detail specifications of the 600 W prototype parallel-series LLC resonant converter and the employed SST used in the experiments. Fig. 51 illustrates experimental operating waveforms of the prototype converter according to the SST. Fig. 51 (a) shows the operating waveforms under the conventional in-phase modulation, which has the same operating pattern of the SST and no difference to each other converter. Fig. 51 (b) shows the operating waveforms using the proposed phase shift algorithm of the SST, which has a 180° phase shift between two converters. Fig. 52 shows the output voltage regulation performance according to the operating cases. Fig. 52 (a), (b), and (c) show the steady state operating waveforms of no SST, using the SST using the conventional in-phase modulation, and using the SST using the proposed phase shift algorithm, respectively. Without the SST, the output voltage ripple is 2.425 V. Using the SST using the in-phase modulation, the voltage ripple is 15.511 V which is 6.39 times higher than no SST case. Using the SST with the proposed algorithm, the voltage ripple is 3.876 V which is four times smaller than the in-phase modulation case. Table VIII shows the performance comparison of the EMI reduction and the output voltage regulation using the SST with the proposed algorithm.



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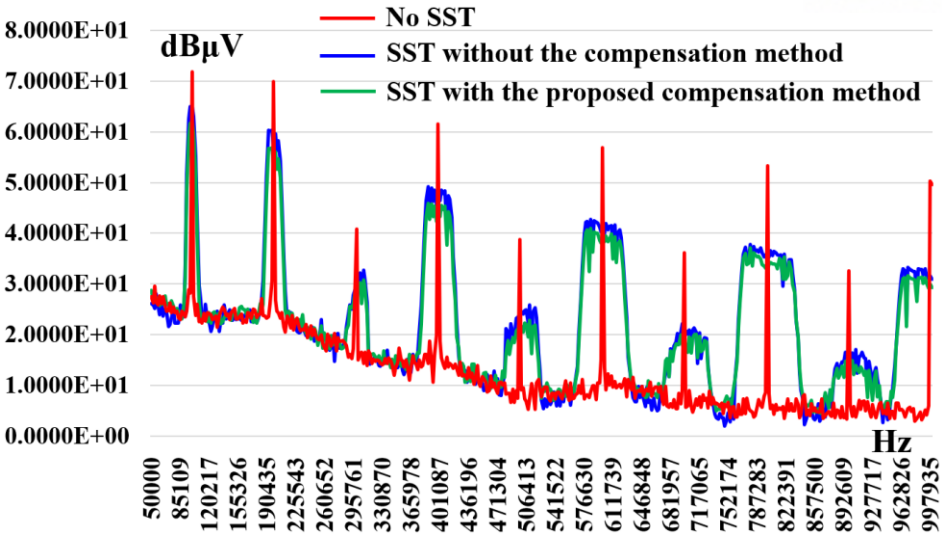
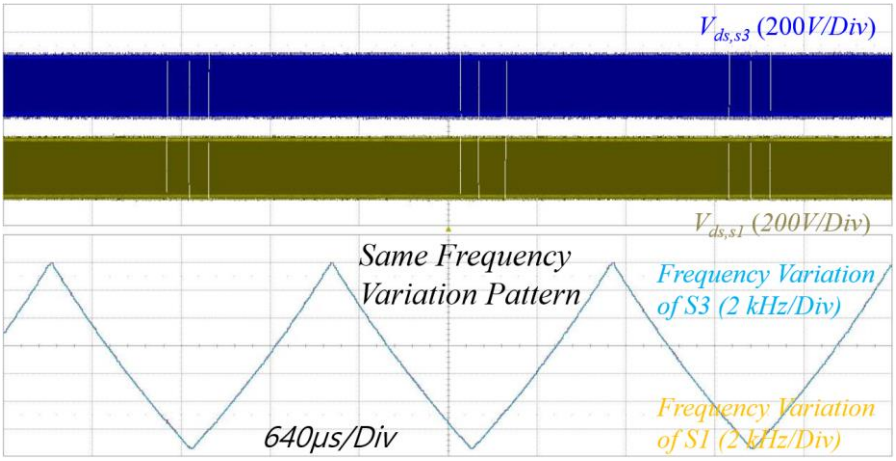


(b)

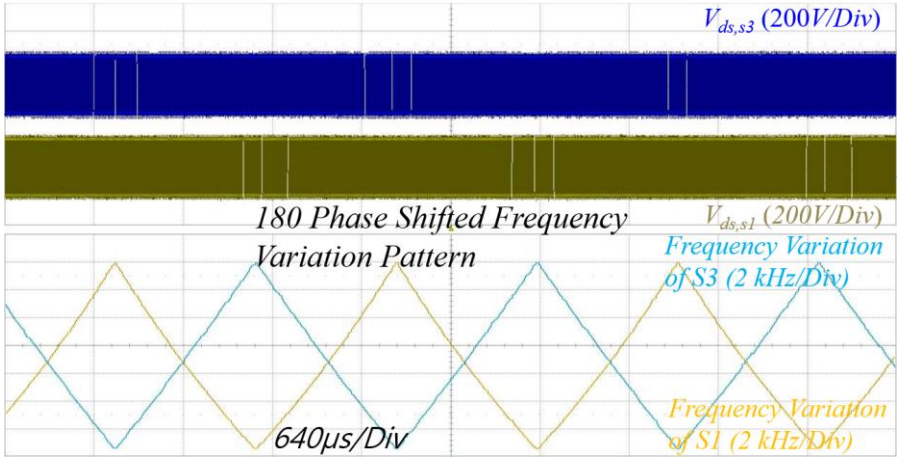
Fig. 50 Experimental measurements of CE noise reduction performance: (a) Common mode noise, (b) Differential mode noise.

Table VII Designed Specification

Specification	
Input Voltage	400 V
Load Condition	380 V, 1.58 A
Resonant Capacitor	36 nF
Resonant Inductance	83 uH
Magnetizing Inductance	290 uH
Δf	13.5 kHz
f_m	450 Hz

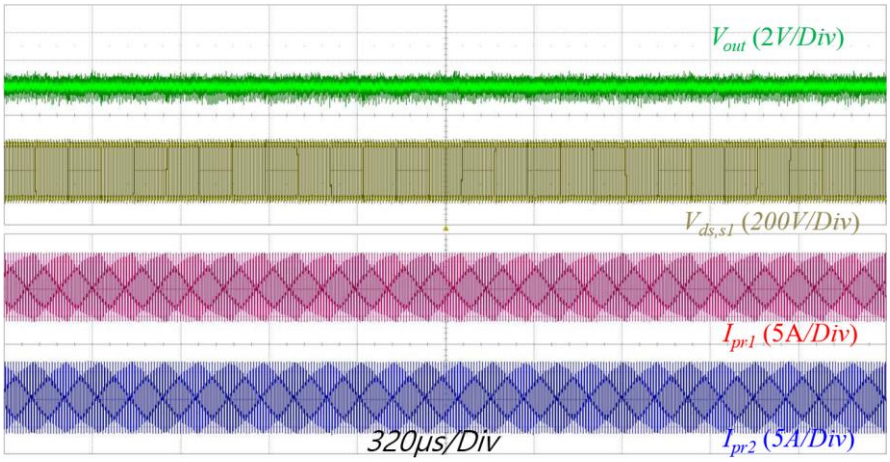


(a)

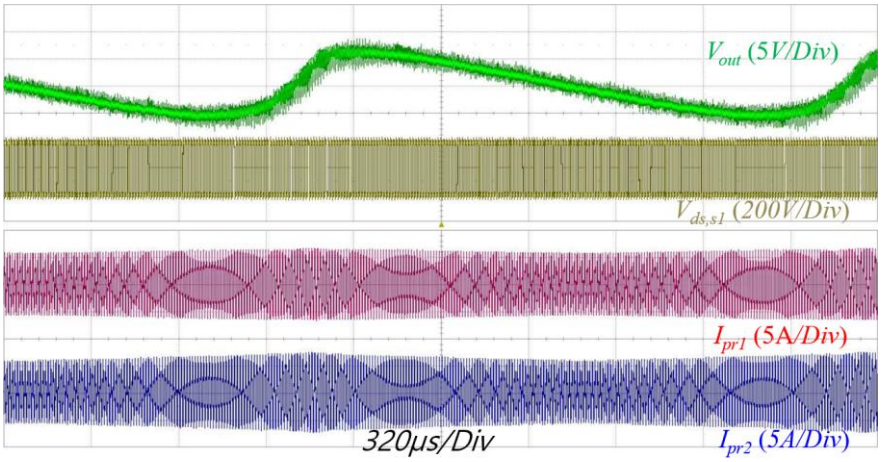


(b)

Fig. 51 Experimental operating waveforms using SST: (a) with in-phase modulation, (b) with the proposed phase shift algorithm.



(a)



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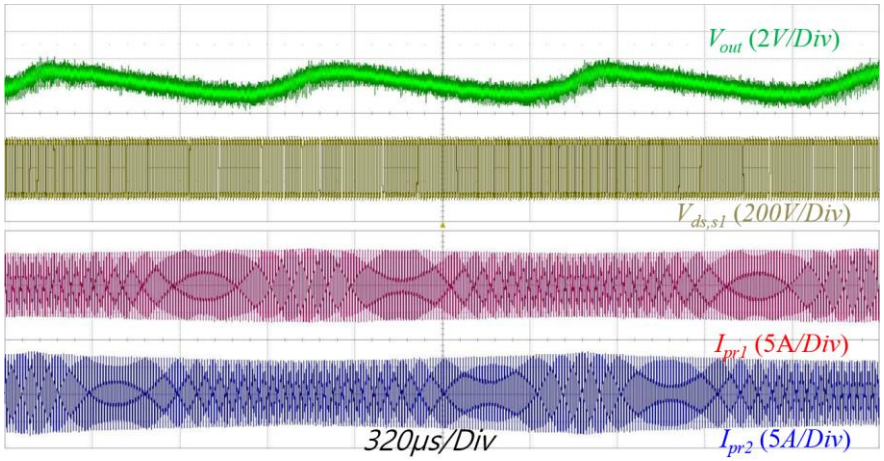


(c)

Fig. 52 Experimental waveforms of output voltage, switch voltage, primary and secondary currents: (a) No SST, (b) Using SST with in-phase modulation, (c) Using SST with the proposed phase shift algorithm.

Table VIII Performance Comparison of EMI Reduction and Output Voltage Regulation

Measured Results	No SST	SST with in-phase modulation	SST with phase shift algorithm
Peak CM noise	67.2 dBμV	54.9 dBμV	50.1 dBμV
Peak DM noise	71.7 dBμV	64.9 dBμV	61.9 dBμV
Output voltage ripple	2.425 V_{pp}	15.511 V_{pp}	3.876 V_{pp}

4.3 APWM HB Resonant Converter under SST

In this section, a half-bridge (HB) resonant converter using an asymmetric pulse-width modulation (APWM) is proposed to achieve both the size reduction of the EMI filters using the SST and the tight output voltage regulation [58]. The design methodology of its resonant tank will be analyzed to properly implement the SST and the tight output voltage regulation at the same time. In addition, zero voltage switching (ZVS) capability of the primary switches will be analyzed to obtain the high power conversion efficiency under the SST. The SST will be designed to satisfy the required output voltage regulation and to reduce the EM noise. The size reduction of the input EMI filters will be demonstrated by experimental results with SST to improve the power density of the resonant converter. The performance of output voltage regulation and EM noise reduction will be verified with 100 W prototype HB resonant converter. All the experimental results are measured with respect to standard EMI test condition.

The target application is a small sized power supply for the home appliances which requires the rated power of 100 W and 20 V (6%) output voltage. This structure effectively shows the EM noise reduction of target DC-DC converter using the SST without the EM noise of active PFC circuit. The HB resonant converter has soft switching capability on the primary side power switches, which can obtain high power conversion efficiency to implement high switching frequency operation for its high power density. In addition, the HB resonant converter employing the APWM can obtain small voltage fluctuation according to the switching frequency variation.

4.3. Spread Spectrum Design

The reduction of the EM noises is determined by the switching frequency variation ($\triangle f$) and the modulation frequency (f_m) of the SST, which can be described as a modulation index ($m_f = \triangle f/f_m$). The modulation method of the SST is selected to the triangular modulation. Fig. 53 shows the theoretical reduction of the EM noises using the triangular modulation according to m_f, which describes the EM noise reduction at the switching frequency. High order harmonics have high modulation index ($h \cdot m_f$) compared with that of the carrier frequency (m_f), which is effective to reduce the high frequency harmonics. From Fig. 53, the higher m_f shows the greater reduction of the EM noises, which can reduce the size of EMI filters.

The f_m is higher than the resolution bandwidth (RBW) of EM noise measurement to achieve noise reduction. The standard RBW for 150 kHz to 30 MHz is 9 kHz in industrial area. In this research, the spectrum analyzer (9320B, Keysight) used in the experiments has 10 kHz RBW. The f_m is designed to 11 kHz with ten percent design margin. The $\triangle f$ determines the EM noise reduction. However, the large EM noise reduction requires larger switching frequency variation which can induce the larger output voltage fluctuation. Therefore, the reduction of the EM noises is determined by the available switching frequency range changed by the SST. The available switching frequency range can be designed by considering the specification of the output voltage fluctuation.

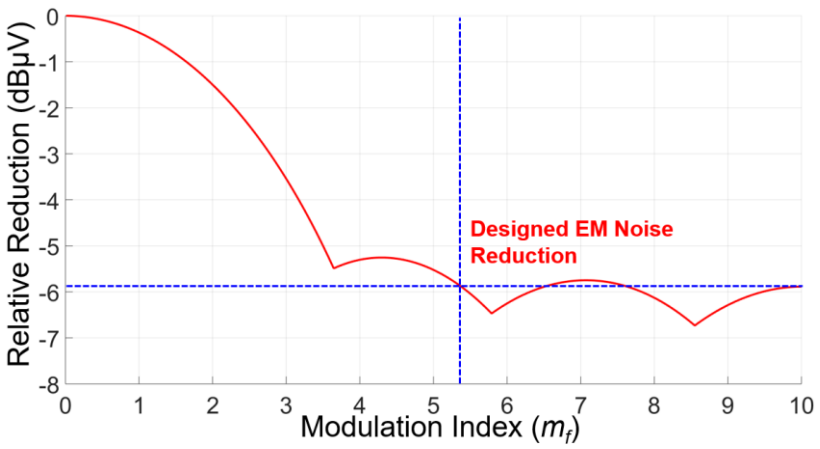
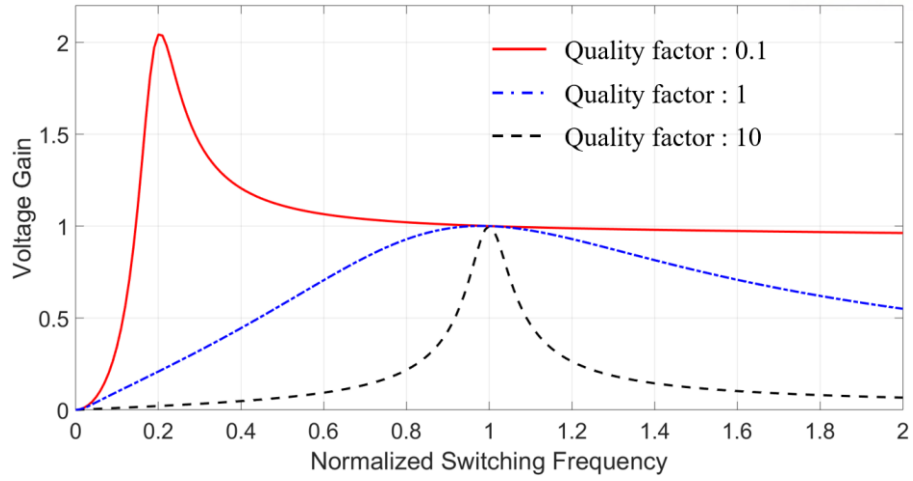
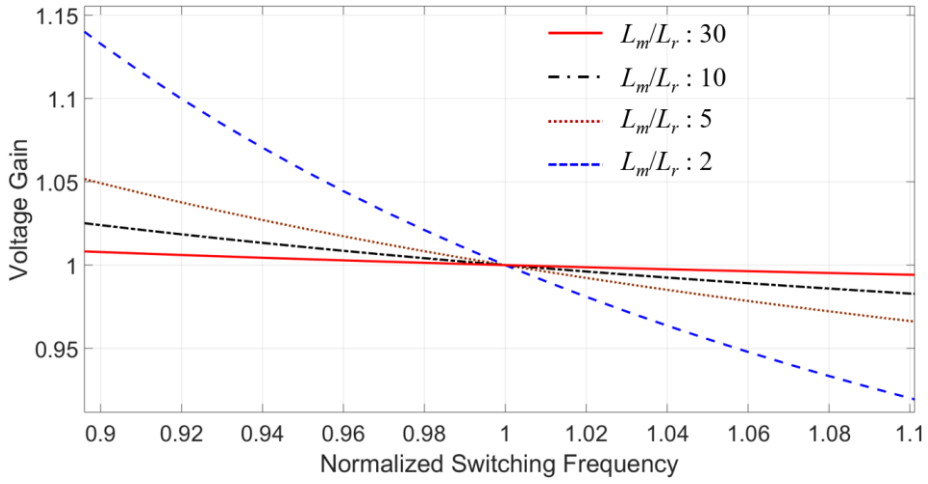


Fig. 53 EM noise reduction according to the modulation index (m_f).



(a)



(b)

Fig. 54 Input-output voltage gain curves: (a) according to quality factor, (b) according to L_m/L_r ratio.

4.3.B Power Stage Design for Tight Output Voltage Regulation

The SST requires large switching frequency variation to reduce the EM noises, which can generate the input-output voltage gain fluctuation. The input-output voltage gain according to the switching frequency variation can be derived as follows:

$$G(f_n)=\left[\left(1+\frac{L_r}{L_m}-\frac{L_m}{L_r f_n^{\,2}}\right)^2+Q^2\left(f_n-\frac{1}{f_n}\right)^2\right]^{-\frac{1}{2}} \tag{77}$$

where f_n is the normalized frequency using the resonant frequency, L_m is the magnetizing inductance, L_r is the resonant inductance, and Q is the quality factor. From (77), the voltage gain fluctuation caused by the SST can be derived as follows:

$$\Delta G(f_n)=G\left(\frac{f_c+\Delta f_{\max}}{f_r}\right)-G\left(\frac{f_c-\Delta f_{\max}}{f_r}\right) \tag{78}$$

where $G(f_n)$ is the input-output voltage gain according to the switching frequency, f_c is the carrier frequency, f_r is the resonant frequency, and Δf_{max} is the maximum switching frequency range. The voltage gain variation according to the switching frequency variation of the SST is determined by the design of the resonant tank. From (77) and (78), the smaller input-output voltage gain fluctuation can obtain the tighter output voltage regulation.

The resonant tank of the HB resonant converter consists of L_m, L_r, and resonant capacitance (C_r). The resonant components and load condition determine the quality factor which decides the shape of the voltage gain according to the switching frequency. Using (77), Fig. 54 (a) shows the voltage gain curves according to the quality factor. The higher quality factor has the wider voltage gain variation near the resonant frequency (f_{r1}) according to the values of L_r and C_r. The voltage gain variation near the resonant frequency is proper for the pulse frequency modulation. However, it has large output voltage fluctuation using the SST. The lower quality factor shows the flatter voltage gain near the resonant frequency, which has small voltage gain variation using the SST near the resonant frequency. Under the rated load condition, the smaller resonant inductance and the bigger resonant capacitance are required to obtain the smaller output voltage fluctuation according to the switching frequency variation.

The magnetizing inductance is significant to obtain the small input-output voltage gain fluctuation caused by the switching frequency variation of the SST. Fig. 54 (b) shows voltage gain curves according to L_m/L_r ratio. The smaller L_m/L_r ratio induces the higher resonant frequency (f_{r2}) according to the values of L_m, L_r, and C_r, which is closed to the resonant frequency (f_{r1}). It has large voltage gain variation near f_{r1} according to the switching frequency variation caused by the SST. The higher L_m/L_r ratio induces the larger frequency difference between f_{r1} and f_{r2}. It makes small voltage gain variation according to the switching frequency variation caused by the SST. Therefore, the larger magnetizing inductance can obtain the tighter output voltage regulation under the spread spectrum operation.

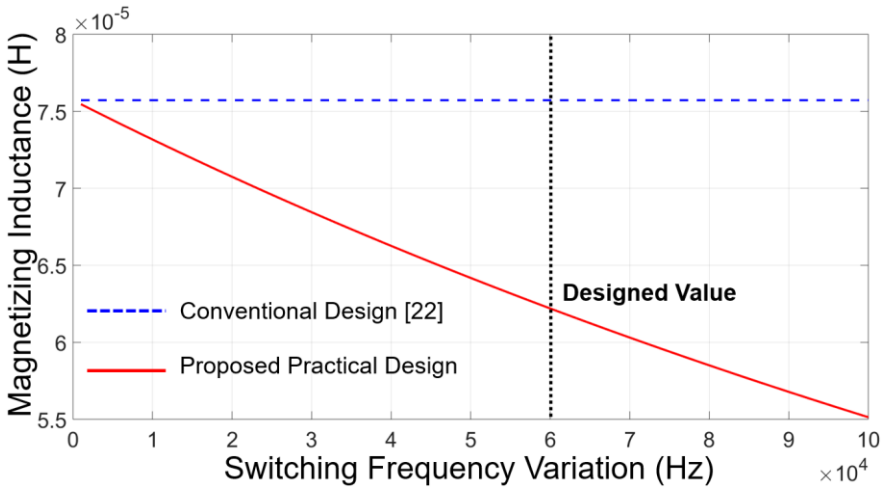


Fig. 55 Maximum magnetizing inductance curves for ZVS capability according to switching frequency variation.

4.3.C Magnetizing Inductance Design for ZVS Capability

The larger magnetizing inductance can obtain the smaller voltage gain variation caused by the switching frequency variation of the SST. However, it can lose the ZVS capability on the primary side power switches. The maximum magnetizing inductance without losing the ZVS capability can be derived as follows:

$$L_m \le \frac{R_{o,\min} \cdot t_{s,\min}}{2} \tag{79}$$

where $R_{o,min}$ is the minimum load resistance [$= n^2 \cdot (V_o/I_o)$], n is the turn ratio, V_o is the output voltage, I_o is the load current, and $t_{s,min}$ is the minimum turn-off duration of S_2. However, it does not consider the switching frequency variation. The HB resonant converter using the SST should consider the maximum switching frequency to obtain the maximum magnetizing inductance which can guarantee the ZVS capability. The proposed minimum turn-off duration can be derived as follows:

$$t_{s,\min} = \frac{D_{s2,\max}}{\left(1 + \frac{2nC_sV_{in}}{I_{o,\max}t_{dt,\min}}\right) \cdot \left(f_c + \Delta f_{\max}\right)} \tag{80}$$

where $D_{s2,max}$ is the maximum duty ratio of S_2, C_s is the parasitic capacitance of the primary switches, V_{in} is the input voltage, $I_{o,max}$ is the maximum output current, and $t_{dt,min}$ is the minimum dead-time duration at the maximum switching frequency. The magnetizing inductance can be designed using (79) and (80) to achieve the tight output voltage regulation and to obtain the ZVS capability.

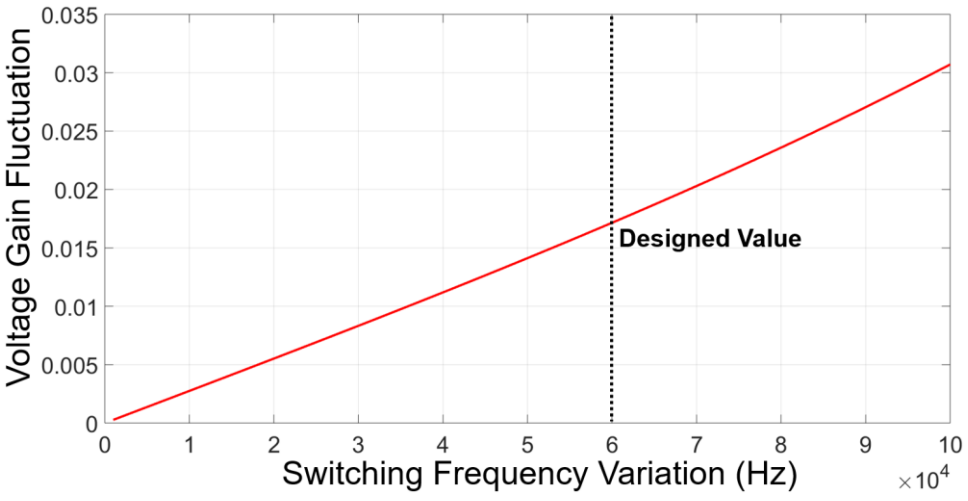


Fig. 56 Voltage gain fluctuation according to switching frequency variation.

4.3.D Practical Design Guides

The output voltage regulation performance is determined by the switching frequency variation ($\triangle f$) caused by the SST. In this research, the resonant frequency is 450 kHz which is the carrier frequency

of the SST. The V_{in} is the AC grid voltage (220 $V_{ac,rms}$) which makes the DC link voltage of 310 $V_{dc,link}$. The transformer turn ratio is eight. The $D_{s2,max}$ is 0.6 with enough margin to regulate the output voltage (20 V). The dead time of t_{dt} has five percent of the switching period. The primary switches use GaN MOSFETs (GS66508P, GaN Systems), which has 142 pF of its output capacitance. With those specifications and (79), Fig. 55 shows the maximum magnetizing inductance curves according to the switching frequency variation caused by the SST. The larger switching frequency variation requires the smaller magnetizing inductance to obtain the ZVS capability, which induces the larger output voltage fluctuation according to the switching frequency variation.

The higher coupling coefficient (k_c) of the transformer can obtain the smaller resonant inductance. According to the coupling coefficient, the resonant inductance can be determined by the magnetizing inductance. In addition, the resonant capacitance can be decided by the resonant inductance and the resonant frequency. From (78) and (79), Fig. 56 shows the input-output voltage gain fluctuation according to the switching frequency variation caused by the SST. The higher switching frequency shows the larger output voltage fluctuation. The switching frequency variation caused by the SST can be designed to satisfy the desired regulation range (6%) of the output voltage.

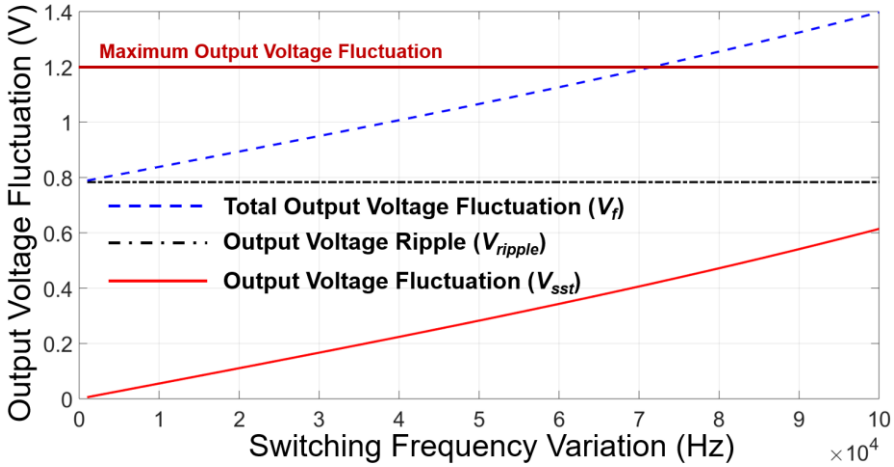


Fig. 57 Output voltage ripple and fluctuation according to switching frequency variation.

The total output voltage fluctuation is the sum of the output voltage ripple caused by the converter's switching activity and the output voltage fluctuation caused by the SST, which can be derived as follows:

$$V_f = V_{ripple} + V_{sst} \tag{81}$$

where V_{ripple} is the output voltage ripple and V_{sst} is the output voltage fluctuation according to the SST. The output voltage ripple V_{ripple} can be derived as follows:

$$V_{ripple} = \frac{D_{\max} T_s I_{peak}}{2C_o} + I_o R_{esr} \tag{82}$$

where I_{peak} is the secondary side peak current, C_o is the output-stage capacitance, and R_{esr} is the effective

series resistance of the output capacitor. Fig. 57 shows the total output voltage fluctuation derived by (81) and (82). The output voltage ripple is the constant value determined by the output-stage capacitance and the switching characteristics. As shown in Fig. 57, the switching frequency variation is limited by the maximum output voltage fluctuation.

Table IX Designed Specification

Specification	
Input Voltage	311 $V_{dc,link}$
Load Condition	20 V, 5 A
Resonant Capacitor	65.8 nF
Resonant Inductance	1.9 uH
Magnetizing Inductance	61 uH
Δf	60 kHz
f_m	11 kHz

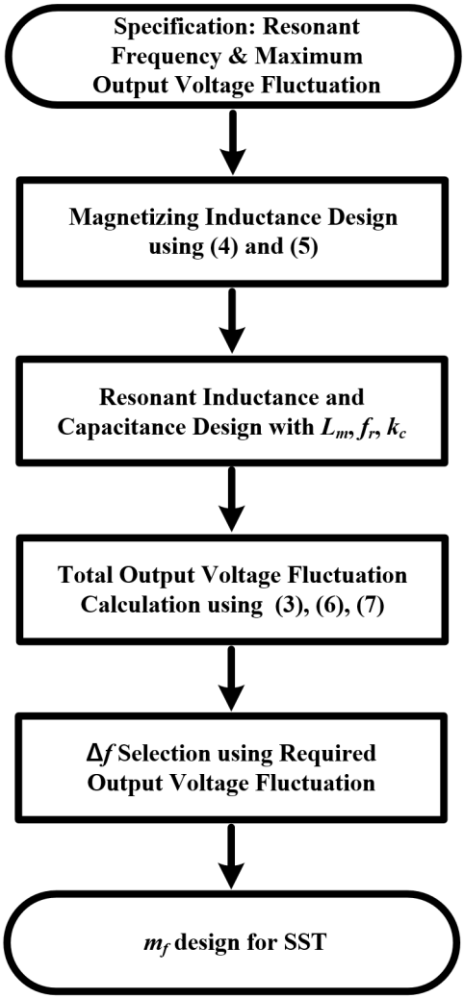


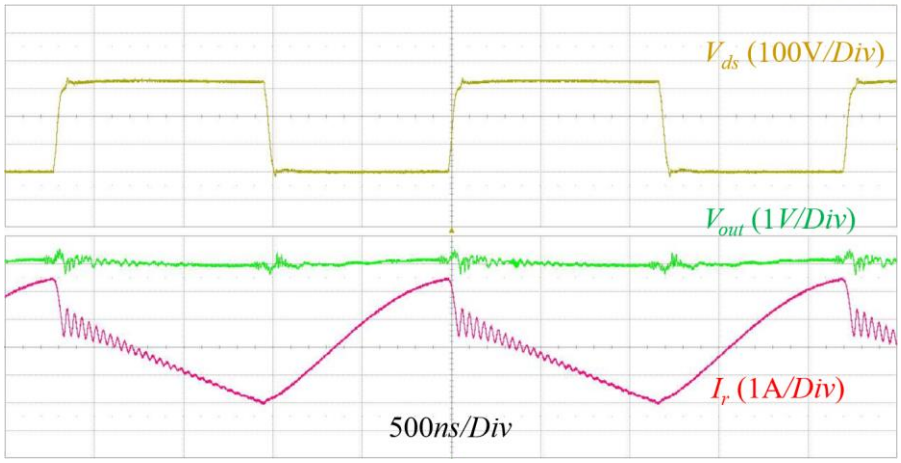
Fig. 58 Design flow chart of power stage and SST for the proposed HB resonant converter.

The switching frequency variation ($\triangle f$) of the SST is 60 kHz to obtain good output voltage regulation performance, as shown in Fig. 56. From f_m and available $\triangle f$, m_f is 5.45 as shown in Fig. 53. The designed SST can reduce the EM noises around 8 dBμV. In addition, the power converter can satisfy the desired output voltage regulation performance with ±2.8% output voltage fluctuation. Table IX shows the specification of the designed power converter and the SST. Fig. 58 shows the design flow chart of the power stage and the SST. The resonant tank is selected to obtain the desired output voltage regulation performance. The SST can be designed to obtain both the desired output voltage regulation performance and the enough EM noise reduction.

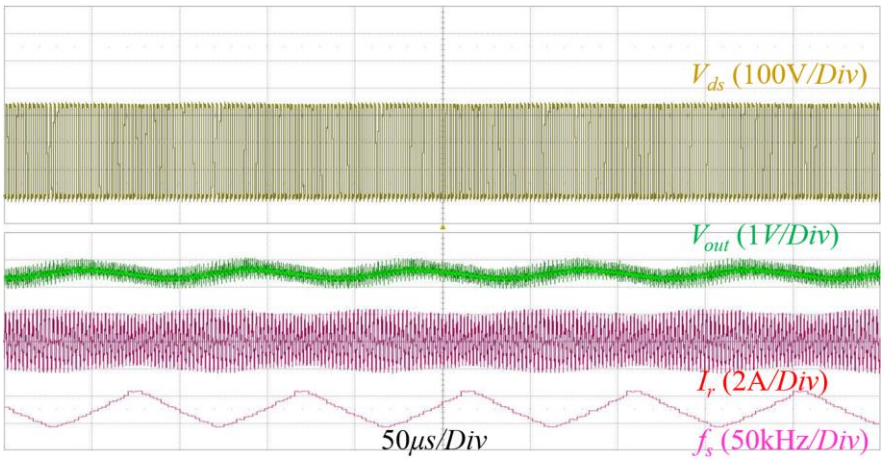
4.3.E Experimental Results

Fig. 59 shows the prototype converter and measuring setup. It configured with the oscilloscope (610Zi, Teledyne Lecroy), electric load (PLZ1004WH, KIKUSUI), LISN (LN2-16N, EMCIS), and spectrum analyzer (9320B, Keysight). This experimental setup can satisfy the CE measuring standard. Fig. 60 shows the steady-state waveforms operating at the full load condition. Fig. 60 (a) shows the ZVS operation of the power switches and output voltage ripple of 839 mV. Fig. 60 (b) shows the operating waveforms using the SST, which has switching frequency variations caused by the triangular modulation. Fig. 60 (c) shows the operating waveforms without the SST, which has no switching frequency variation. The output voltage ripple with the SST is around 1.12 V_{pp}, which is 1.3 times higher than no SST condition.

Fig. 59 Experimental setup of 100 W prototype power converter.



(a)



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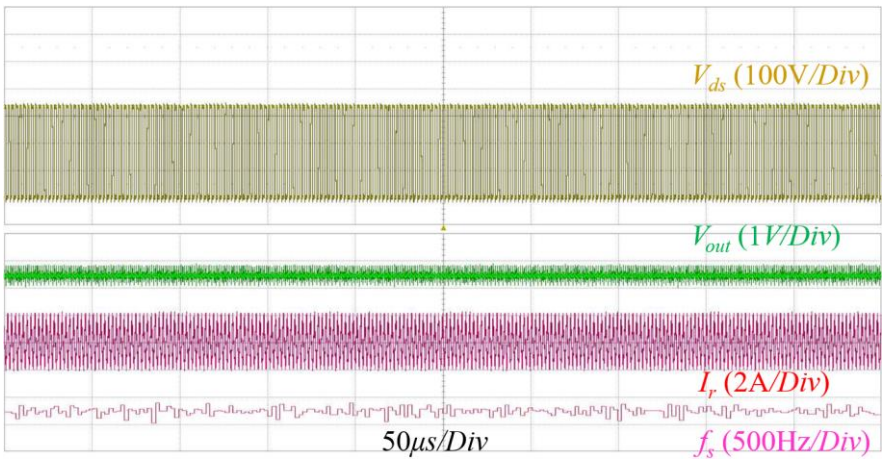


(c)

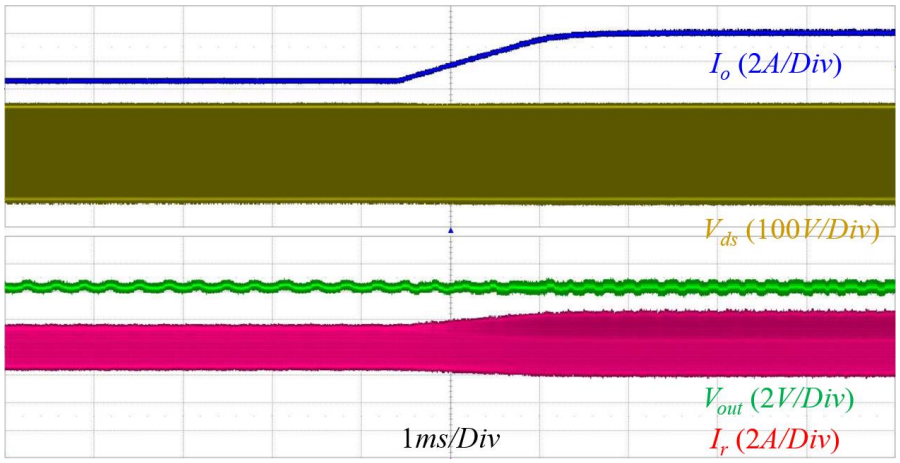
Fig. 60 Steady state operating waveforms of the APWM resonant converter: (a) Output voltage ripple and ZVS operation, (b) With SST, (c) Without SST.

In [54], the hybrid modulation is applied to the LLC resonant converter, which has the discontinuous operation of the SST. It has high peak EM noises under the load transient condition. Fig. 61 shows the

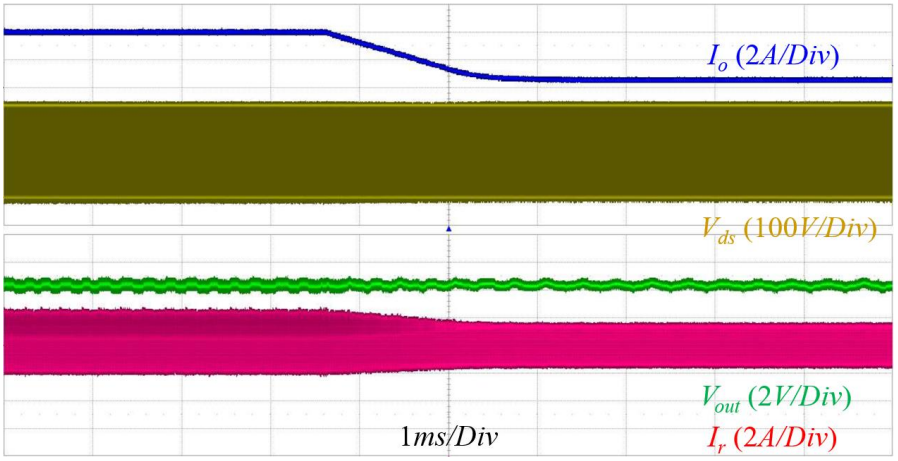
dynamic responses of the HB resonant converter using the APWM with and without the SST. Fig. 61 (a) and (b) show the load change response without the SST. Fig. 61 (c) and (d) show the load change response with the SST. The HB resonant converter using the APWM has the continuous SST operation, which has no high peak EM noises under the load transient condition. In addition, it has tight output voltage regulation during the load transient operation. Table X shows the output voltage ripple in the steady-state operation and under the load transient condition with and without the SST. The steady state operation can satisfy the required output voltage regulation performance (6%).

Table X Output Voltage Regulation Performance

Output voltage ripple	No SST	SST
At the steady state operation	839 mV_{pp} (4.2 %)	1.127 V_{pp} (5.5 %)
At the load transient operation	1.33 V	1.47 V



(a)



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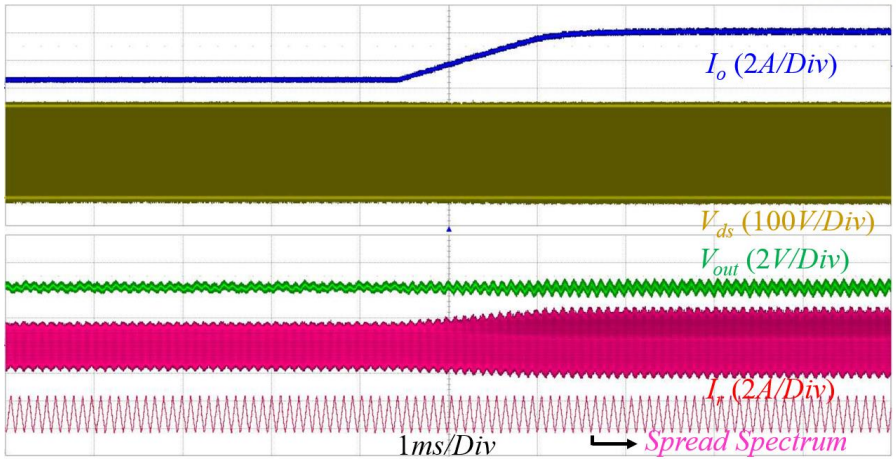

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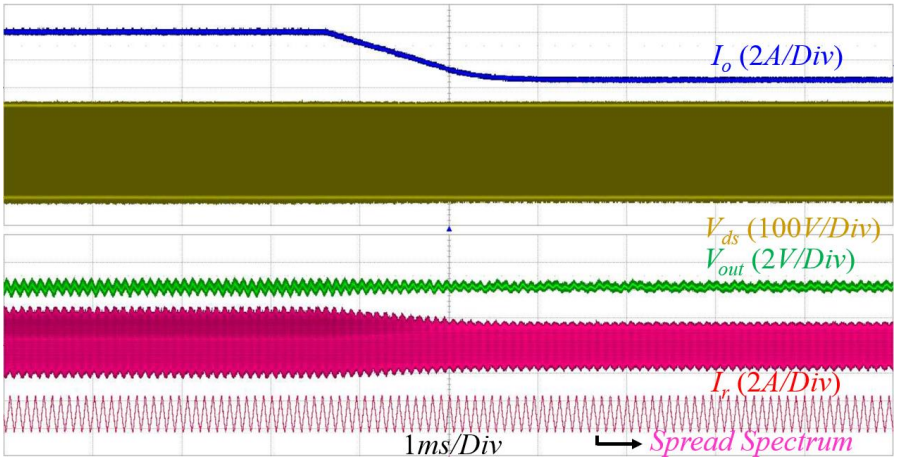
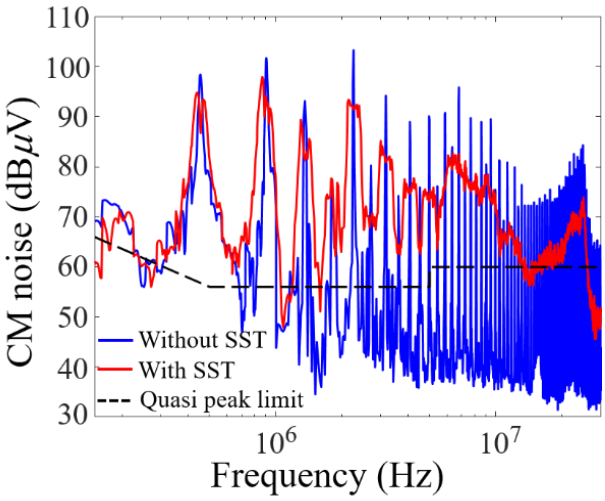


(d)

Fig. 61 Operating waveforms of dynamic responses: (a) Light (10%) to full (80%) load change without the SST, (b) Full to light load change without the SST, (c) Light to full load change with the SST, (d) Full to light load change with the SST.

The CE noises from the proposed power converter are measured from 150kHz to 30MHz using the CE test standard setup. The CM/DM noise separator (EA-2100, EMCIS) is also used to analyze the CM and DM noise characteristics. The measured CM and DM noises are shown in Fig. 62 (a) and (b), respectively, as well as the total CE noise at ac power line depicted in Fig. 62 (c). Before the installation of the EMI filter, conducted emissions with and without the SST operation have been compared. The critical peak values at the fundamental frequency and the harmonics of 450 kHz are meaningful where it is the switching frequency of the HB resonant converter. The SST operation achieves the CE reduction by 5 to 20dB in the overall frequency range of the CE test for both the CM and DM noises. Especially, the SST operation tends to reduce more CE noises at the high frequency range which is higher than 1 MHz.



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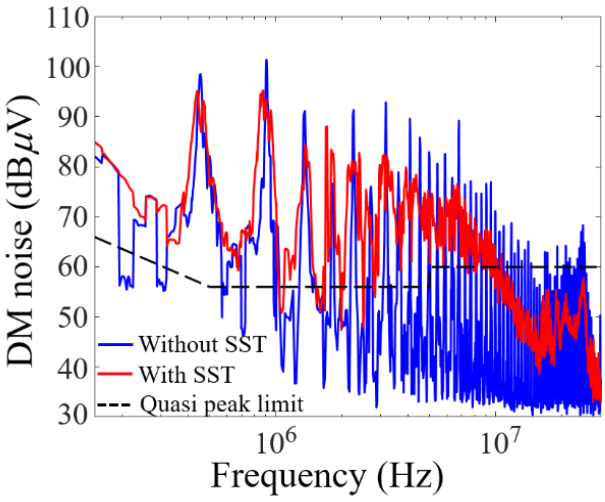

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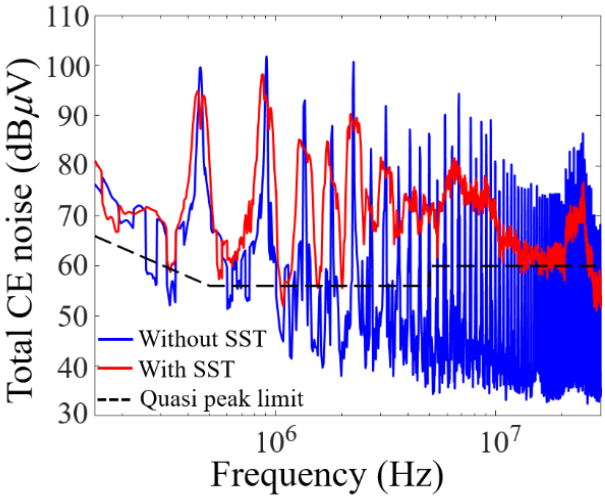


(c)

Fig. 62 Measurement results of CE noises without EMI filters: (a) CM noise, (b) DM noise, and (c) total CE noise at an ac power line.

Even though the SST operation can reduce both the CM and DM noises, the amount of the noise

reduction is still not enough to satisfy the quasi-peak limit of the CISPR- Class B regulation standard, as shown in Fig. 62 (c). To achieve more noise reduction by using the SST, $\triangle f$ should be increased but the increment of $\triangle f$ can degrade the output voltage regulation performance. Therefore, applying EMI filters with the SST can efficiently perform enough CE noise reduction. To design the EMI filter properly, the noise source impedance of the proposed resonant converter should be obtained by a simple method described in [59], which utilizes the amounts of measured CE noises with and without a reference impedance. The magnitude of the CM and DM noise source impedance at 450 kHz was extracted as 1.9 kΩ and 9Ω, respectively. Based on the information of the extracted noise source impedance, the single stage EMI filter has been designed as shown in Fig. 63 (a). The designed single stage EMI filter consists of a 2.2 μF X-capacitor, a CM choke, and a pair of 4.7 nF Y-capacitors, where the CM choke has 3 mH inductance at 100 kHz. Additionally, two stage EMI filter has been designed by adding the same 2.2 μF X-capacitor and 3 mH CM choke as shown in Fig. 63 (b) to compare the noise attenuation performance between the single stage filter with the SST and the two stage filter without the SST.

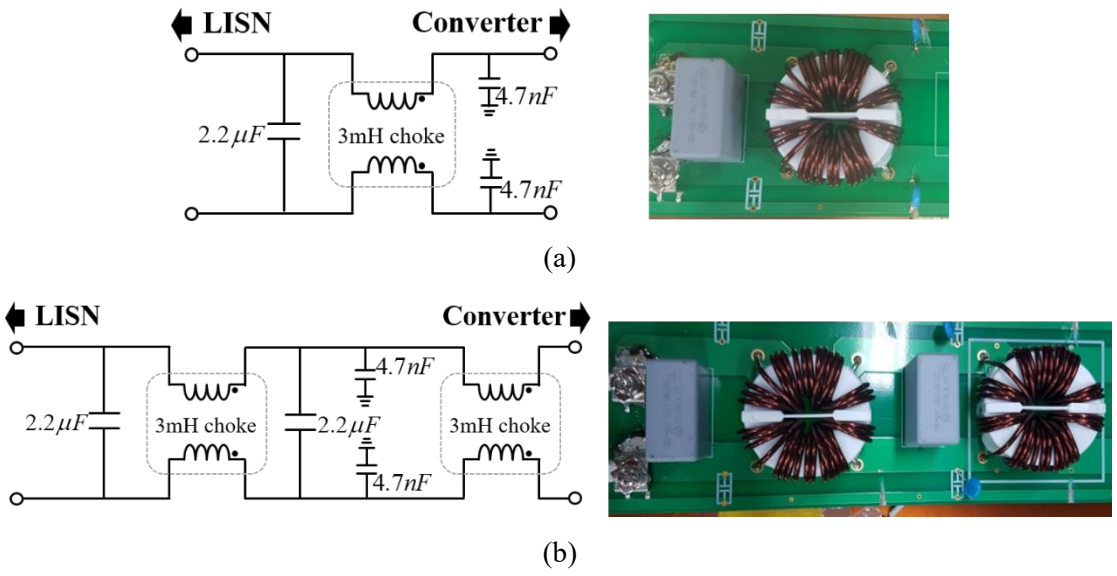
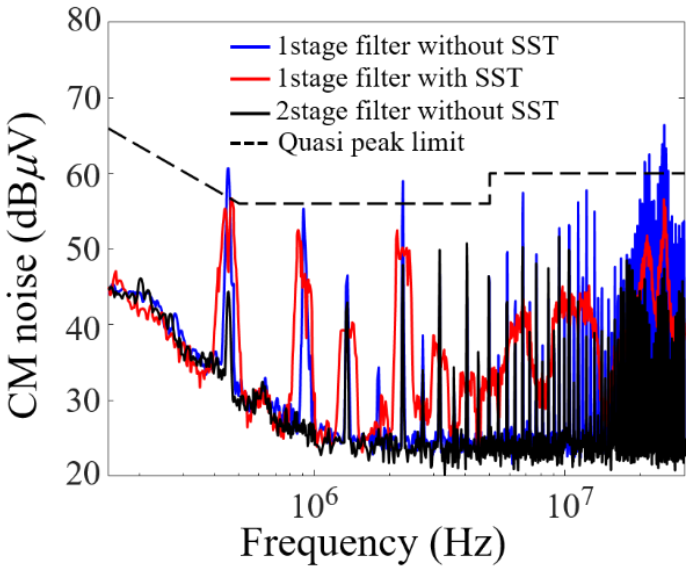


Fig. 63 Circuit diagram and photograph of designed EMI filters: (a) Single stagestructure and (b) Two stage structure.

The designed EMI filter has been installed in front of the proposed HB resonant converter, and the measured CM, DM, and total CE noises are shown in Fig. 64 (a), (b), and (c), respectively. In Fig. 64 (a), the CM noise peaks at 450 kHz, 2.3 Mhz, 20 Mhz, and 25 Mhz are still higher than the quasi-peak limit of the CE regulation standard when only the single stage filter is installed without the SST operation. In addition, the DM noise peaks at 450 kHz and 900 kHz are also higher than the regulation standard as shown in Fig. 64 (b). By adding one more CM choke and X-capaictor, two stage filter can

sufficiently reduce the conducted emission below the quasi-peak limit for both the CM and DM noises, however, it significantly increases the size and cost of the EMI filter as shown in Fig. 63. In addition, the noise attenuation performance of high frequency range over a few MHz can be worse than an expected designed value since the parasitic impedance and mutual coupling between the components of the EMI filter can critically degrade the noise attenuation performance at the high frequency range [60], [61].



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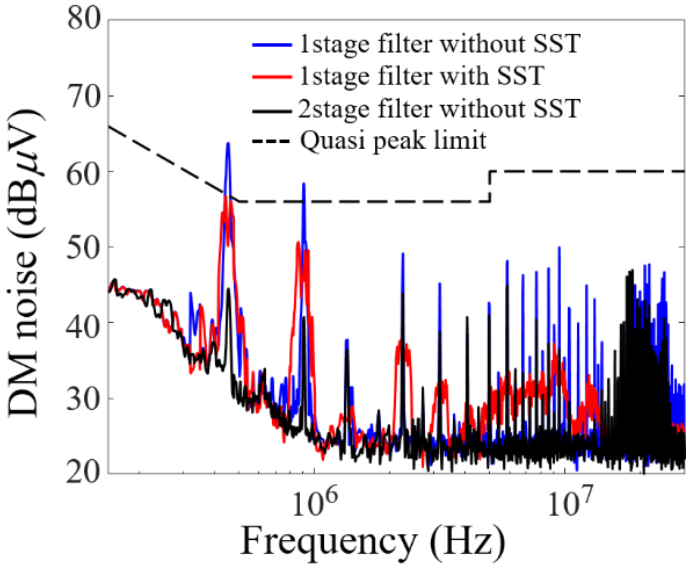

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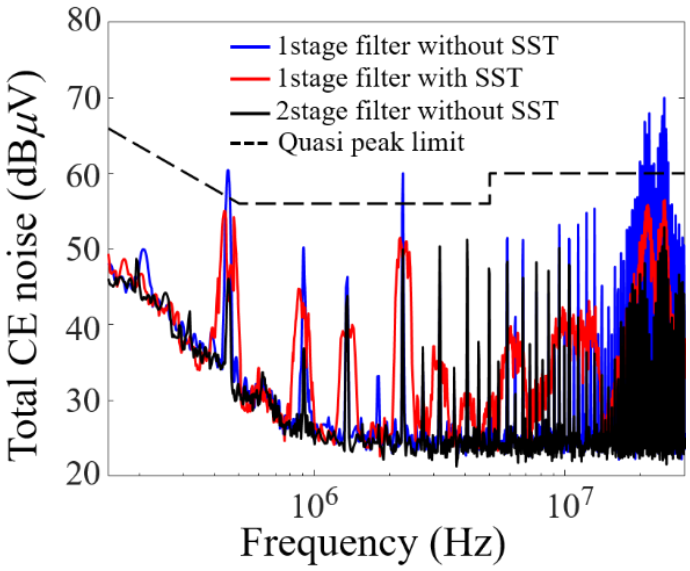

(c)

Fig. 64. Comparison of measured CE noises according to EMI filter stages and SST operations: (a) CM noise, (b) DM noise, and (c) total CE noises at a ac power line.

In the case of the single stage filter with SST operation, however, both the CM and DM noise can be efficiently reduced without any additional components on the EMI filter as shown in Fig. 64 (a) and (b). Moreover, the noise reduction by the SST operation have great effect at high frequency over few MHz, then the CE result of the single stage filter with SST operation have similar or better performance comparing with the CE result of 2 stage filter without SST operation. Thus, the total CE level at a power line is managed under limit of the CE regulation without any additional components from 1 stage EMI filter by applying the SST operation, as shown in the Fig. 64 (c). Therefore, the SST can effectively reduce the size and cost of the EMI filter.

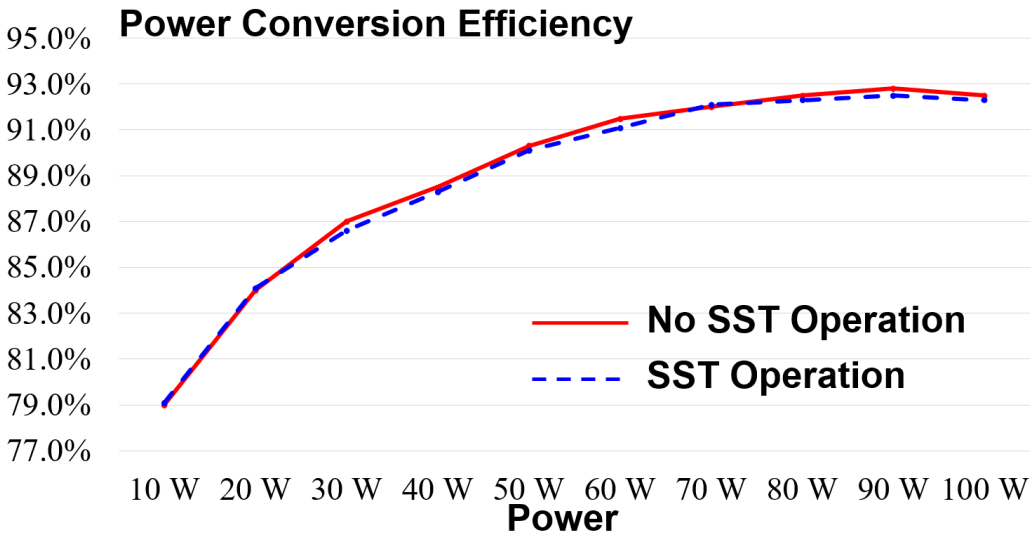

Fig. 65 Power conversion efficiency according load variation with and without the SST.

The power conversion efficiency of the HB resonant converter using the APWM is shown in Fig. 15. From Fig. 65, the spread spectrum operation does not affect to the power conversion efficiency in the steady-state of the power converter.

The SST has disadvantage on the lifetime of the output capacitor, because the SST induces the output voltage fluctuation. It makes output current ripple on the output rectifier. The high output current ripple induces the high temperature on the output capacitor, which makes the fast dry-out of the output capacitor. The heat rise of the capacitor can be derived as follows:

$$\Delta T_c = \frac{I_{ripple}{}^2 R_{esr}}{\beta S} \tag{83}$$

where I_{ripple} is the output current ripple, R_{esr} is the parasitic resistance of the output capacitor, S is the surface of the capacitor, and β is the heat radiation factor. The SST induces the output current fluctuation according to the output voltage fluctuation. However, the proposed control algorithm can improve the lifetime of the output capacitor with the tight output voltage regulation. In addition, the small ESR has small temperature rise at the high switching frequency operation.

V. Summary

5.1 Power Stage Design for 1 MHz LLC Resonant Converter

The high switching frequency converter can be optimized to achieve smaller power loss and high power density. In aspect of power stage, the parasitic components make side effects which induces undesired operating waveforms. The differences between conventional switching frequency and high switching frequency should be reflected to the power stage design. The power stage operating at MHz switching frequency is analyzed to obtain the soft commutation of secondary diodes and small voltage spike on the secondary diode. The time delay effect by the limited DSP computation performance is analyzed to design the loop gain of the high frequency LLC resonant converter.

5.2 PFM-PWM Hybrid Control and FPGA Controller for High Switching Frequency Operation

The limited resolution of DSP makes the large output voltage ripple by the large switching frequency variation at high switching frequency condition. The PFM-PWM hybrid control algorithm is proposed to suppress the output voltage ripple by the switching frequency variation. The operational principle and the power stage design methodology are analyzed to implement the proposed control algorithm. In addition, the FPGA controller is proposed to reduce the output voltage ripple and improve the dynamic performance. The high performance FPGA makes high switching frequency resolution and fast computation speed compared with general purposed DSP. The LLC resonant converter can achieve well-regulated output voltage and fast dynamics with high performance FPGA.

5.3 EMI Reduction Methods for Resonant Converters

The EMI noise reduction is necessary to obtain the high power density of the power converter and high cost-effectiveness with small sized EMI filter. The spread spectrum technique is one of solution to reduce the EM noise of power converter. However, the large switching frequency variation makes large output voltage fluctuation. The several control algorithms and design methods are proposed to implement the SST at the resonant converter. The control algorithms can improve the EM noise reduction and output voltage regulation. The design method verifies the EM noise reduction with small sized EMI filter.

VI. Conclusion and Future Work

6.1 Conclusion

In this thesis, three research topics are introduced to improve the performance of high frequency resonant converter. The equivalent model of LLC resonant converter is analyzed to obtain the high power conversion efficiency at the 1 MHz switching frequency. The resonant tank and power stage are designed from the modified equivalent model of LLC resonant converter. In addition, the feedback loop is designed with the consideration of the time delay effect of digital controller. In terms of output voltage regulation, the limited PWM resolution makes poor output voltage regulation performance at high switching frequency. The PFM-PWM hybrid control algorithm is introduced to obtain the tight output voltage regulation at the 1 MHz switching frequency. The operational principles and design methodology are analyzed to obtain the high power conversion efficiency, the stability, and the output voltage regulation performance. In terms of EMI issue, the spread spectrum technique (SST) is applied to the resonant converter to reduce the electromagnetic interference (EMI), which also improves the power density of the power converter with small EMI filter size. However, the wide switching frequency variation induces the large output voltage fluctuation on the resonant converter. In this thesis, several control algorithms are introduced to achieve tight output voltage regulation and EMI reduction, simultaneously. All the proposed design considerations and control algorithms are verified with the simulation and experimental results.

6.2 Future Work

1. AC-DC Converter with SST

In this thesis, the SST is applied to DC-DC resonant converters. However, the EMI reduction on the AC-DC converter is necessary to suppress the EM noise in terms of the total power conversion system. In the future work, the AC-DC converter with the high switching frequency and the high power conversion efficiency will be developed to implement the SST.

2. Power Line Communication (PLC) using SST

The power converter with the SST is the dual functional system, which includes the power transmission with output voltage regulation and the EM noise reduction. However, this system can increase the functionality with power line communication using the SST. In the future work, the SST is applied to the converter for the EM noise reduction and the PLC.

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