Master's Thesis

Measurement and Analysis of IC Jitters and Soft Failures due to System-level ESD

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Abstract

Human touches to ground metal of electronic systems can cause electrostatic discharge (ESD)-induced soft failures without causing physical damage. If a number of data are lost due to ESD-induced noises, then a system freeze, fault, or reboot can occur, and user intervention is required to restore normal system operations. Such malfunction of a system is called system-level ESD soft failures that become more serious as the speed of electronic devices increases and their size becomes more compact. Achieving immunity of systems and integrated circuits (ICs) against soft failures due to system-level ESD is an important design goal.

In this thesis, two specific circuits whose soft failures can be fatal to whole system are investigated. One of them is a delay-locked loop (DLL) and the other is a sense amplifier flip-flop (SAFF). The DLL is widely used to compensate the timing of high-speed data communications. The SAFF is commonly used as an input receiver for address and command in a DRAM. The DLL and SAFF were designed and fabricated in a 180-nm CMOS process. They are mounted in each simplified design of dual in-line memory module (DIMM) by chip on board (COB) assembly and the DIMMs are mounted on each simplified motherboard.

The input and output voltages of the DLL under ESD-induced noises were measured, and the average values of peak-to-peak jitter and jitter durations of the DLL clock were obtained from repeated measurements. The effects of the VDD-GND decoupling capacitors and a bias decoupling capacitor were investigated. The measured DLL output are reproduced in SPICE simulations using the measured DLL input voltages, and the root causes of the jitter are investigated. Additionally, measurements are conducted in a frequency domain to find the relationship between the power-ground impedance and noises.

The soft failures of the SAFF due to system-level ESD were investigated under the ESD injection level of 3, 5, and 8 kV. ESD test case without and with VDD-GND decoupling capacitors (de-caps) were investigated. The measurements were conducted 50 times with each test case above. The noise voltages and the soft failure ratio of the SAFF were obtained. SPICE simulation was conducted to validate the results by using measured noise voltages and root causes of the soft failures.

Contents

List of Figures

List of Tables

Nomenclature

CLK	Clock
CML	Current Mode Logic
CP	Charge pump
De-cap	Decoupling capacitor
DIMM	Dual-inline memory module
DLL	Delay-locked loop
DQ	Data
DQS	Data strobe
DRAM	Dynamic random-access memory
ESD	Electrostatic discharge
FFT	Fast fourier transform
GRP	Ground reference plane
IC	Integrated circuit
I/O	Input and output
PCB	Printed circuit board
PD	Phase detector
PSRR	Power supply rejection ratio
SAFF	Sense amplifier flip-flop
SODIMM	Small outline dual in-line memory module
S-parameter	Scattering parameter
SPICE	Simulation program with integrated circuit emphasis
TIE	Time interval error
VCDL	Voltage-controlled delay line
VNA	Vector network analyzer

I. Introduction

1.1 Introduction to ESD-induced soft failures

Mobile electronic devices such as cell phone and a laptop PC are popularly used. As usage of the devices increases, electrostatic discharge (ESD) due to human touch gets more serious. The ESD noise in a system can distort important data, which could make soft failures at system-level such as malfunction and kernel panic. Our laptop is easily exposed to ESD events, since input and output (I/O) ports are placed at the side of the laptop. The I/O ports are frequently touched by their hands. The situation is described in Fig. 1. The currents and charges excited by ESD event could make noise voltage on a signal, as described in Fig. 1, and significant data would be distorted. Investigation of proper solutions to reduce the ESD noises and malfunction of IC, soft failure, is needed. Decoupling capacitors (de-caps) are usually utilized between power and ground plane of a printed circuit board (PCB) to decrease impedance of VDD-GND and ESD-induced noises [1].

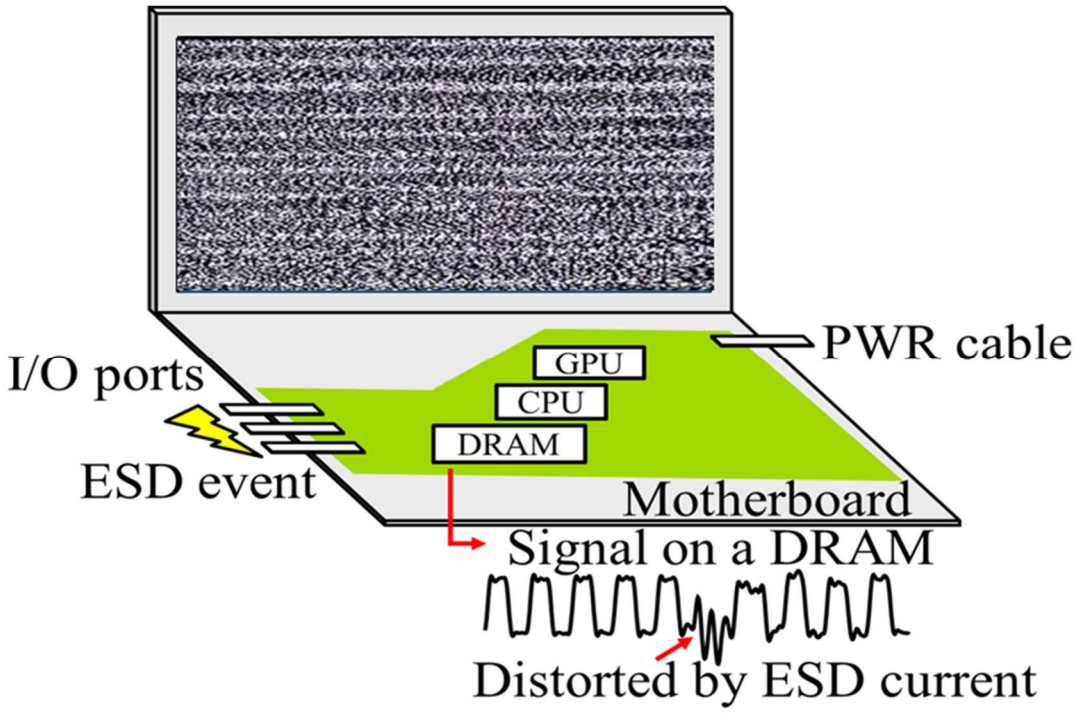


Fig. 1. Scenario of system-level ESD-induced soft failure due to a human touch

ESD is injected by an ESD generator which resembles the situation that a human handling a metal such as USB injects ESD through the metal. Manufactured ESD generators should comply an international standard called IEC 61000-4-2 [2].

Depending on discharge methods, ESD event is divided into air discharge and contact discharge. Air discharge represents discharge phenomena without contact with its victim. The ESD current flows

to the system through the air. On the other hand, contact discharge has contact area on its victim and ESD current flows into the system directly. It is difficult to repeat the experiment maintaining the same conditions of ESD event with air discharge because the air discharge is very sensitive to the speed and angle of approach to the victim [3]. However, the experiment can be reproduced in almost the same conditions by using contact mode discharge [4]. In this thesis, system-level ESD would be injected over hundreds of times, so the contact discharge was selected as an ESD injection method using EM test DITO [5] in Fig. 2.

Fig. 2. ESD generator, EM test DITO

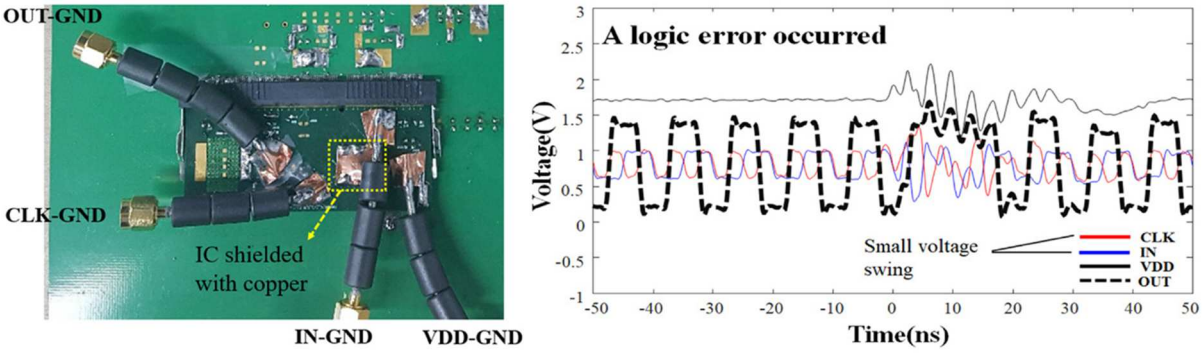
1.2 Previous researches

Many studies on ESD-induced soft failures have been conducted, as follows. The transient performance of power-rail ESD clamp circuits were investigated during power-off and power-on [6]. Soft failures of local interconnect network (LIN) communications were characterized [7]. On-chip ESD detectors observing power, ground, and data signal with different threshold voltages were developed [8]. Methods to detect secondary ESD events were proposed [9]. A structure to increase immunity of a mobile product against system-level ESD by controlling a secondary ESD path was proposed [10]. An efficient way to check the ESD susceptibility of ICs was proposed [11]. Soft failures due to ESD events on a USB connector under different cable and metallic enclosure conditions were studied [12]. System-level ESD noises and failures of wearable devices were modeled and investigated [13]-[14]. The effects of system-level ESD on a wireless router were also investigated [15].

The operation of a complete system is so complicated that identifying the exact root causes of a system soft failure, such as a kernel-panic, the so-called blue screen, is quite difficult. The root causes of ESD-induced soft failures in a tablet were investigated with measurements and full wave simulations in [16]. Soft failures of mobile electronic devices and the improvement solutions have been investigated in [17]. In FPGA, microcontrollers, and microprocessors, soft failures such as program resets and data corruption have been investigated in [18]. ESD soft failures of a CPU with different CPU loadings, clock frequencies, and power distribution network (PDN) impedances were also investigated [19]. Soft failures of a complex system, which consists of many subsystems such as

a variety of sensors in a robot, were investigated [20]. Soft failure of a system on a chip with USB interface was investigated [21]. It was found that ESD-induced noise on input, output, and power pads can cause soft failures [22].

There were previous researches about soft failure of ICs in DRAMs as shown in table 1. In 2011, new designs of flip-flops were proposed to improve immunity of flip-flops against ESD [23]. In 2015, modeling methodology was proposed to predict ESD immunity of D flip-flop [24]. In 2019, statistical operation errors of specific circuit blocks due to a system-level ESD were accurately modeled and reproduced in SPICE transistor-level simulations [25]-[26]. In [25], An IC with simple circuit blocks, like D-flip flop, was fabricated and mounted in a simplified memory module and motherboard structures, which mimic real dynamic random-access memory (DRAM) in a dual inline memory module (DIMM) in Fig. 3 (a). In Fig. 3 (b), measured noise voltages with output logic error. Because all voltages and currents at every circuit node inside the IC can be observed in SPICE simulations, it can be used to identify how ESD-induced noises can result in a functional logic error.



(a) (b)

Fig. 3. (a) Setup for measuring ESD-induced noise (b) measured voltage and output error [25]

Table 1. Previous Researches

Title	Novel Soft Error Robust Flip-Flops in 65nm CMOS	ESD Immunity Prediction of D Flip-Flop in the ISO 10605 Standard Using a Behavioral Modeling Methodology	Measurement and Analysis of Statistical IC Operation Errors in a Memory Module Due to System-Level ESD Noise	**This work**
Authors	David J. Rennie	Guangyao Shen	Myeongjoon Park	Myeongjo Jeong
Publish (year)	IEEE Transactions on Nuclear Science (2011)	IEEE Transactions on Electromagnetic Compatibility (2015)	IEEE Transactions on Electromagnetic Compatibility (2019)	A master's thesis (2019)
Main Contribution	Soft-error robust flip-flops have been introduced	Proposal of a model to predict ESD immunity	Analysis of statistical logic error of D flip-flop due to system-level ESD	Analysis of system-level ESD-induced jitter and soft failure in ICs

1.3 Objectives of this thesis

In this thesis, a DLL and sense amplifier flip flop are investigated to find root causes of whole system level soft failure. In a DRAM, the DLL is used to compensate unwanted delay in data communications and the SAFF is used as command and address receiver. For investigation, they were fabricated with a 180-nm CMOS process and placed on each designed DIMM by COB. Motherboards of a laptop PC were designed in simple form for them. The DIMM and motherboard are similar to [25].

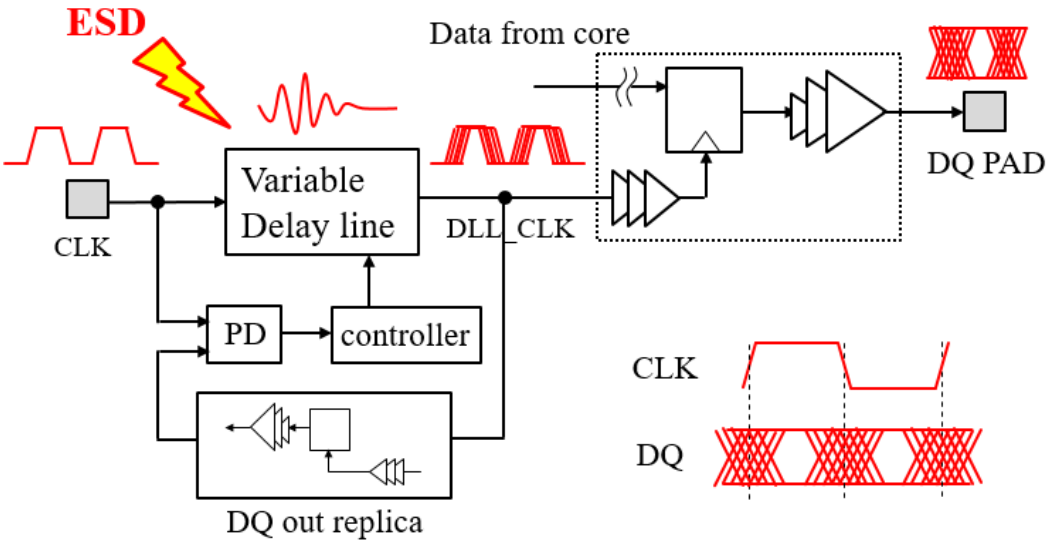
In section II, system-level ESD-induced jitter in the DLL was measured and analyzed under 3, 5, and 8 kV ESD events. Peak-to-peak jitter and jitter duration of the DLL output clock were obtained and averaged with 40 times measurements per each ESD level. To find out the effect of stability of VDD and bias voltages, decoupling capacitors were utilized. To analyze the results in detail and find root causes of the jitter, SPICE simulation was conducted with the measured voltages. Using vector network analyzer, power-ground impedance of the device on the test (DUT) was obtained in frequency domain to find relationship between the impedance and ESD-induced noises.

In section III, soft failures of a SAFF due to system-level ESD were investigated under 3, 5, and 8 kV ESD events. To find out the effect of stability of VDD, two test conditions were organized. One is a case without VDD de-cap and the other is a case with VDD de-caps. In experiments, 50 times ESD events were injected per each ESD level and test condition. Input and output voltages and ratio of the SAFF's soft failure were measured. To analyze and find root causes of soft failure, SPICE simulation was conducted with the measured voltages.

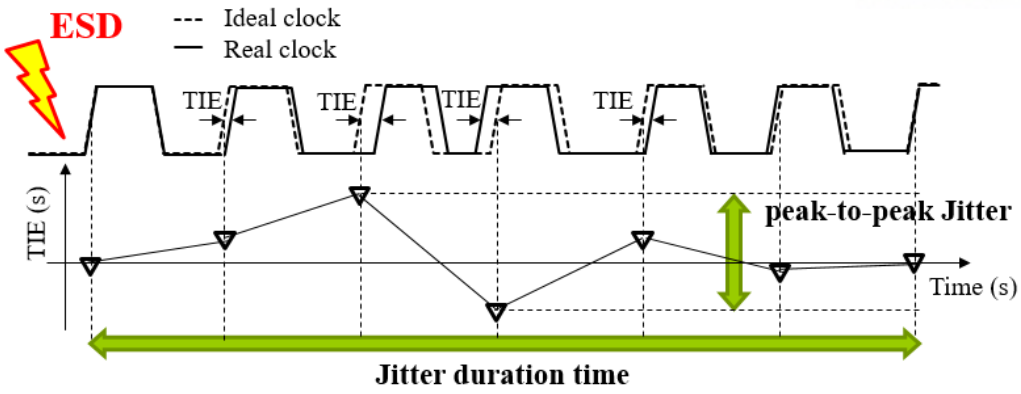
II. System-level ESD-induced Jitter in a Delay-locked Loop (DLL)

2.1 Introduction to a DLL

Delay-locked loops (DLL) have been widely used since 2000 to satisfy high operating speed requirements in DRAMs [27]. DLLs consist of a variable delay line, a phase detector, a delay controller, and a replica circuit. Most of the double data rate (DDR) DRAMs use DLL clocks in output latches to output the data (DQ) and data strobe (DQS). As shown in Fig. 4 (a), the role of the DLL is to compensate for the internal delay in order to align the data output time with the rising edge of the external CLK. The DQS's rising edge output access time from the rising edge of CK, tDQSCK, is an important speed performance parameter of a DRAM. The supply or signal voltage fluctuation induced by an ESD event can cause a serious jitter at the DLL clock and thus a skew at tDQSCK, as depicted in Fig. 4 (a), which heavily impacts the system performance. The peak-to-peak jitter of the DLL clock can be obtained from the peak-to-peak time interval error (TIE) value between the ideal clock and the real clock, as shown in Fig. 4 (b) [28]. In addition to the peak-to-peak jitter, the jitter duration time would be also important. If the DLL jitter lasts long or the DLL falls into an unlocked status due to ESD noises, then a lot of the DQ data can be lost during the communication with the DRAM controller. Therefore, we can reasonably suspect that the DLL jitter caused by system-level ESD noises might be one of the culprits of the DRAM soft failures.



(a)



(b)

Fig. 4. Diagram of (a) a DRAM at input terminal, DQ and DQS (b) time interval error, peak-to-peak jitter, and jitter duration time

2.2 Design and experiments for system-level ESD tests of DLL

2.2.1 Designed DLL IC

DLLs are largely divided into three types: analog, digital, and mixed [27]. Analog types with current mode logic (CML) delay lines have a good power supply rejection ratio (PSRR) with jitter, but they have slower wake-up time and higher power consumption compared with digital controlled DLLs. In this thesis, the effect of system-level ESD noises on an analog type DLL is investigated. Detailed circuits of the designed analog DLL are based on [29] and [30]. In [30], the analog DLL was utilized as a core DLL in a semi-digital dual DLL to provide multiphase clocks with an unlimited phase range.

The designed DLL comprises a voltage-controlled delay line (VCDL), phase detector (PD), charge pump (CP), and self-bias circuit, as shown in Fig. 5. The circuit schematics of a delay cell, PD, and CP are also shown in Figs. 6(a), (b), and (c), respectively. The delay of a delay cell is controlled by adjusting the resistance of PMOS loads through ‘Vbp’ and ‘Vbn’ bias signals [30] and [31]. The PD generates ‘up’ and ‘dn’ signals to control the CP by detecting the phase difference between the input and output clocks (ref and slave) of the VCDL [32]. As shown in Fig. 6(c), the charge pump receives the ‘up’-‘dn’ signals from the PD and generates the ‘CP_{OUT}’ signal, which is then converted to ‘Vbp’ and ‘Vbn’ bias voltages through the self-bias circuit for control of the VCDL delay. The analog bias voltage, Vbias, is utilized in the analog unity gain buffer for CP_{OUT} and differential clock buffers.

The DLL generates two output signals, DLL_CLK and $CP_{OUT,BUF}$, the latter of which is a buffered output of CP_{OUT} though the unity gain buffer. In the initial DLL locking state, the VCDL is reset to have the shortest delay with the lowest level of ‘CP_{OUT}’. During the locking procedure, the VCDL delay keeps increasing until the ‘ref’ and ‘slave’ phases are aligned as 0° and 360°, because no replica circuit is included in the feedback path. After the DLL is locked, equally phase-shifted clocks per every 25.7° (=360°/14) become available from the internal nodes of VCDL.

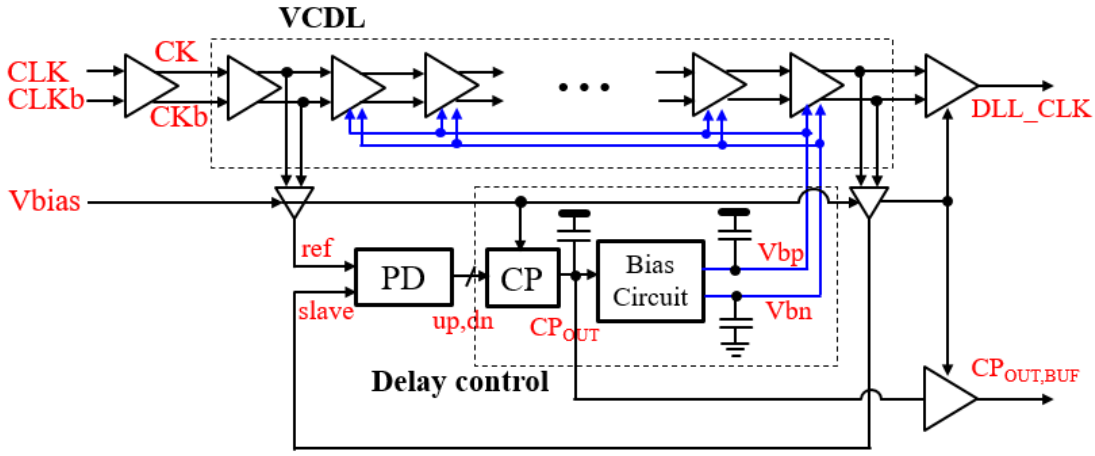
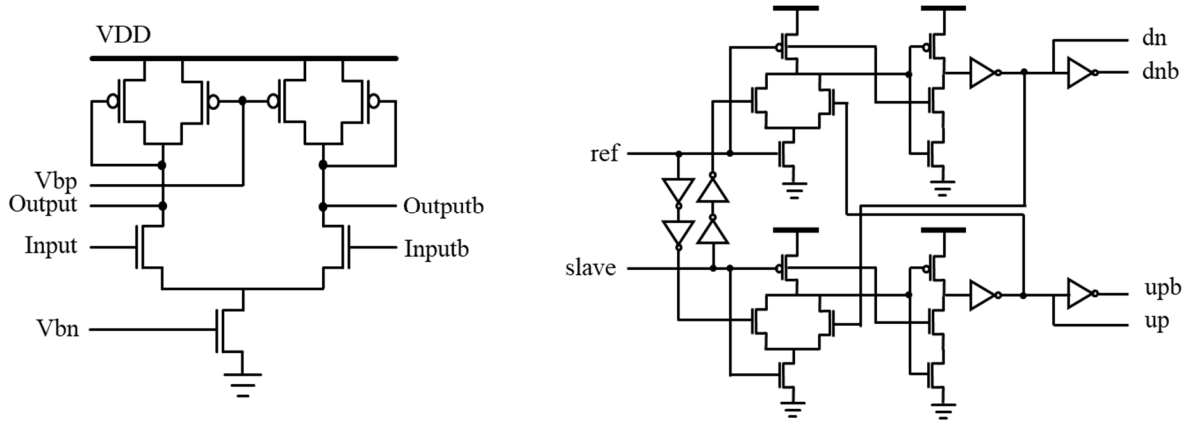


Fig. 5. Overall block diagram of the designed analog DLL



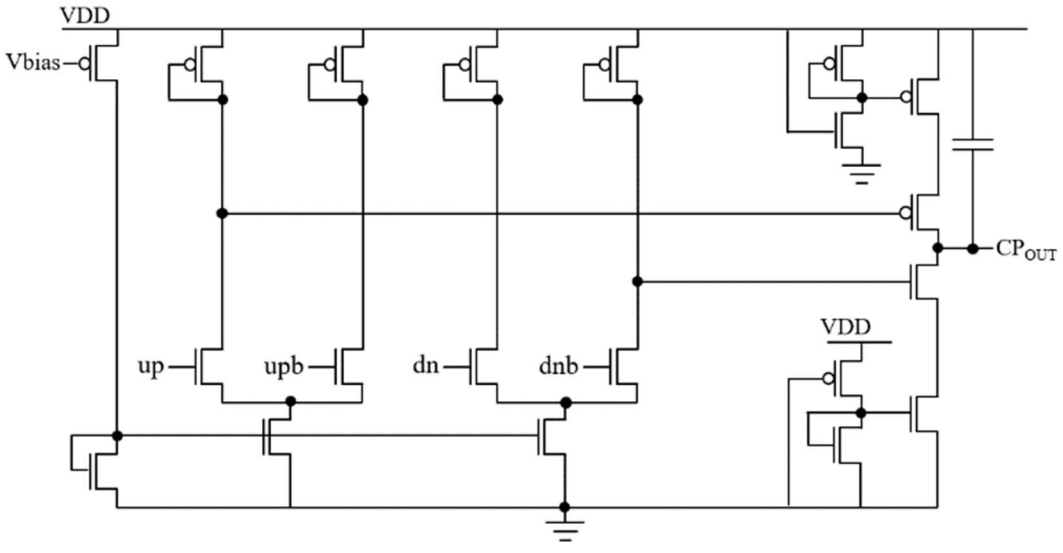


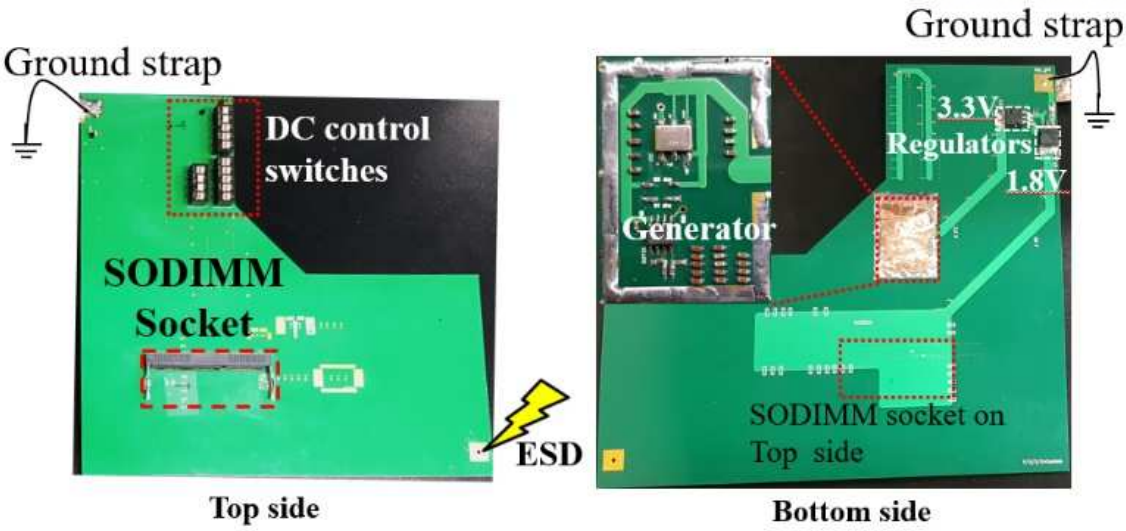
Fig. 6. Circuit schematics of (a) a delay cell in the VCDL [29] (b) phase detector [32] (c) charge pump

2.2.2 Measurement setup and normal operation of the DLL IC

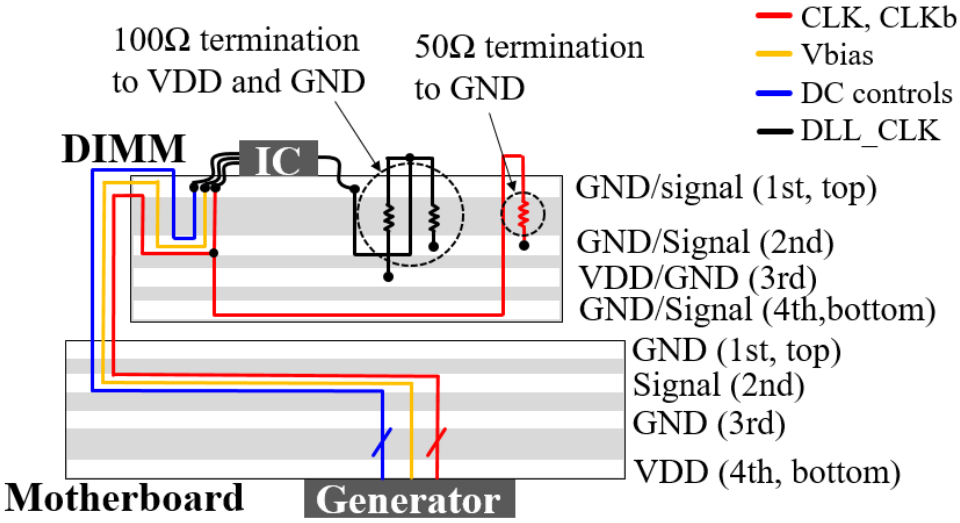
The designed analog DLL IC was fabricated in a 180-nm CMOS process and assembled in simplified motherboard and DIMM structures mimicking a real laptop personal computer (PC) structure, as shown in Fig. 7. The overall structures are basically the same as those in [25] and [26]. As shown in Fig. 7(a), a 3.3V regulator supplies the power for an oscillator that generates 200 MHz differential clocks (CLK, CLKb) for the DLL IC. The other regulator supplies 1.8-V power (VDD) to the IC. Several DC control signals, such as DLL Reset and the dc bias voltage (Vbias), were also supplied from the motherboard to the IC. The signal generating parts of the motherboard were shielded with copper tape to avoid malfunctions during ESD tests.

For impedance matching, CLK and CLKb were terminated to the GND through 50-Ω resistors at the DIMM, and DLL_CLK was terminated to VDD and GND through two 100-Ω resistors. The motherboard and DIMM were connected by a small-outline DIMM socket. The cross-section view of the structures and signal connections are shown in Fig. 7(b).

The DLL IC was mounted on the DIMM by chip-on-board (COB) assembly, and also was shielded with copper tape to avoid direct ESD-field coupling to wire-bonds and IC. The six important inputs and outputs (CLK, CLKb, Vbias, VDD, $CP_{OUT,BUF}$ and DLL_CLK) were simultaneously measured on the DIMM using two synchronized oscilloscopes. As shown in Fig. 7(c), the five signals, except for $CP_{OUT,BUF}$, were measured using semi-rigid coaxial cables, where a 470-Ω resistor was added in series to realize a 520 Ω high impedance probe [33]. The soldering points were shielded with copper tape, and lots of ferrite beads were installed on the rigid cables to prevent common-mode current flow during ESD tests. On the other hand, because the output impedance of the internal analog buffer generating the $CP_{OUT,BUF}$ is comparable to 520 Ω, the $CP_{OUT,BUF}$ waveform was measured using another high-impedance probe with a much larger input impedance of 2.2 MΩ.



(a)



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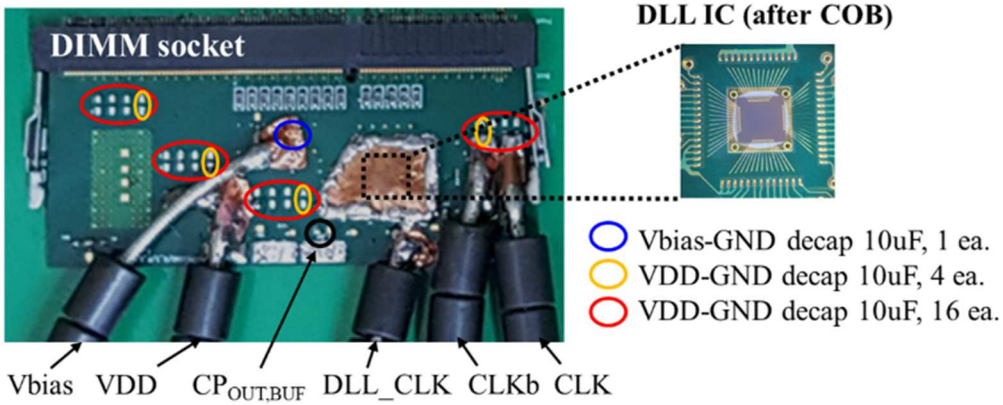


(c)

Fig. 7. (a) Overall test structure (b) a cross-section view of the signal connection between motherboard and DIMM (c) DLL IC and measurement cables on the simplified DIMM

Six cases of DIMM structures were tested depending on the decoupling capacitors on the DIMM. From Case 1 to Case 3, different numbers of VDD-GND de-caps with 10 uF each were employed. From Case 4 to Case 6, a 10 uF Vbias-GND de-cap was additionally employed to investigate the importance of stabilization of the bias voltage for internal analog buffers. The test conditions are summarized in Table 2. The position of the VDD-GND and Vbias-GND de-caps are marked in Fig. 7(c).

Table 2. Test Conditions

	Case1	Case2	Case3	Case4	Case5	Case6
VDD-GND DIMM de-cap (10uF)	-	4 ea	16 ea	-	4 ea	16 ea
Vbias-GND DIMM de-cap (10uF)	-	-	-	1 ea	1 ea	1 ea

Prior to the measurements taken under the ESD event, the normal operation of the DLL IC without any ESD event was measured in Case 1. The DLL locking process can be observed from the outputs of $CP_{OUT,BUF}$ and DLL_CLK. As shown in Fig. 8(a), the measured voltage of $CP_{OUT,BUF}$ starts with the lowest level after the DLL is reset. When the locking is in progress, from about 1us to 5.5us, the $CP_{OUT,BUF}$ keeps increasing to increase the VCDL delay. The DLL_CLK eye diagram can be also obtained by accumulating the measured waveform per each half period. The eye diagram during the locking process from 1us to 5.5us is plotted in Fig. 8(b), which shows that the phase of the DLL_CLK changes continuously because of the increased delay of VCDL. After the DLL is locked, however, a much longer waveform for 20 us shows quite a clean eye diagram, as shown in Fig. 8(c).

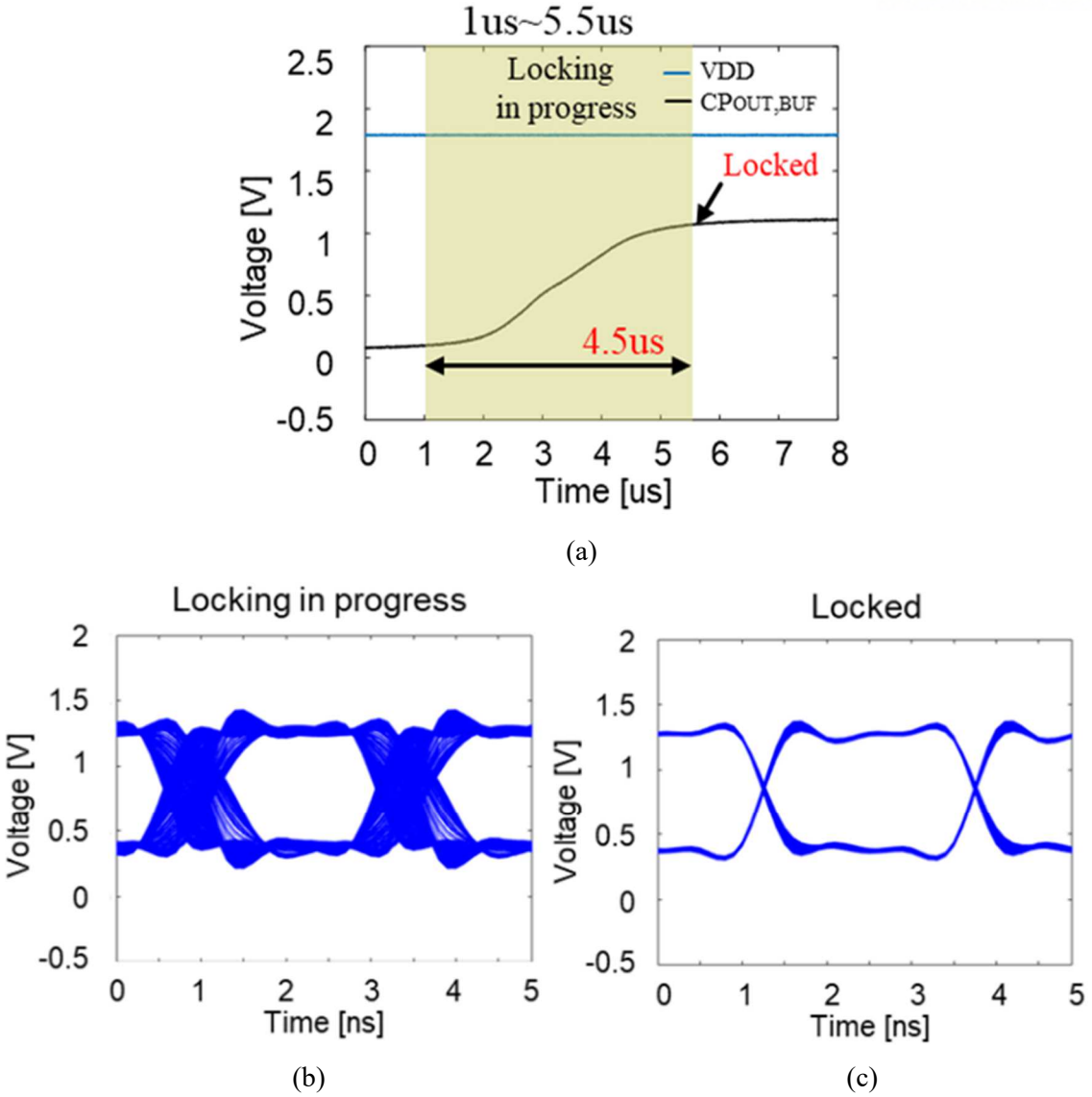
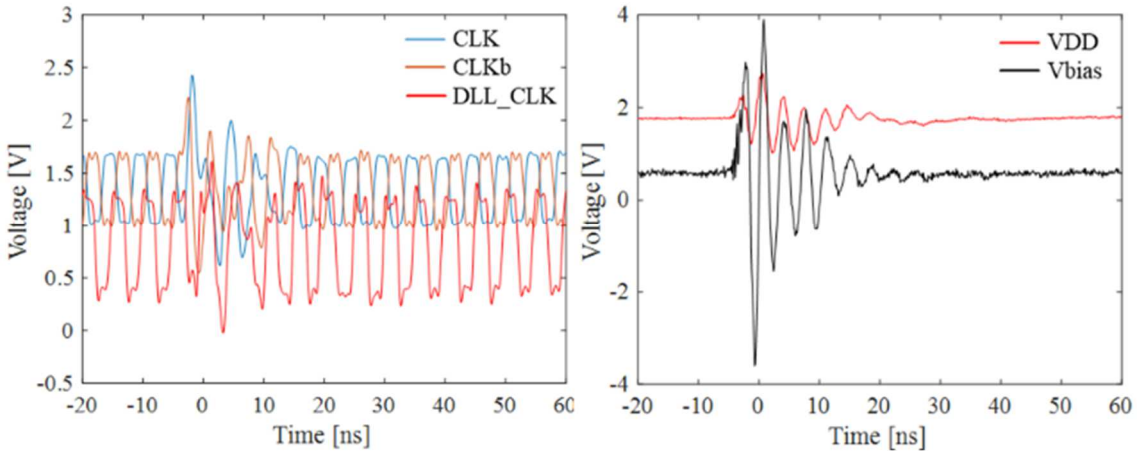


Fig. 8. Measured voltage waveforms in Case 1 without ESD (a) $CP_{OUT,BUF}$ after the DLL is reset (b) eye diagram of DLL_CLK during the locking process (c) eye diagram of DLL_CLK for 20 us after the DLL is locked

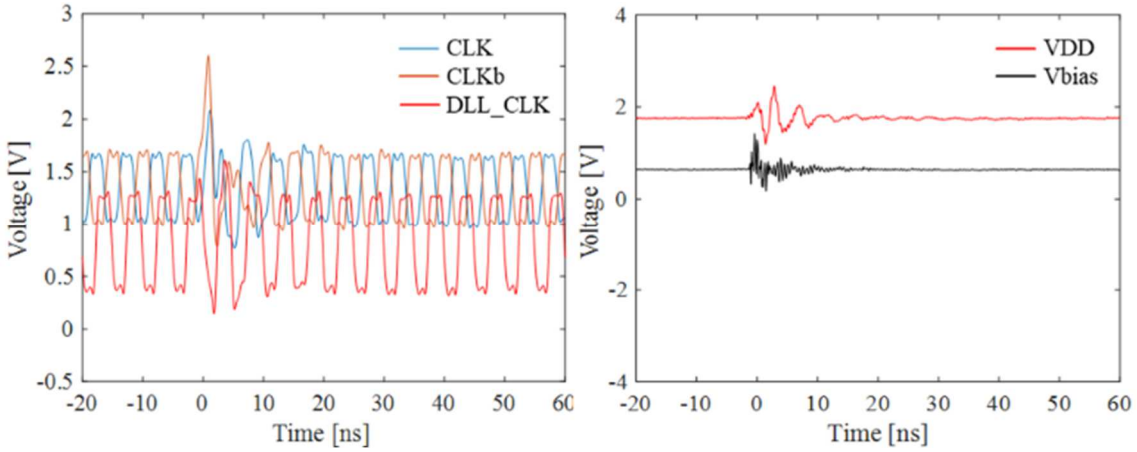
2.2.3 Measurement of DLL operation under ESD events

Next, the effects of the system-level ESD event on the DLL operation were investigated using measurements. For the measurements with good repeatability, ESD events were injected as contact discharge into the GND pad at one corner of the motherboard, as shown in Fig. 7(a). The GND straps of the motherboard and ESD gun were connected to a ground reference plane (GRP) on the floor. As explained earlier, the five signals (VDD, Vbias, CLK, CLKb, and DLL_CLK) were measured through semi-rigid cables using two synchronized oscilloscopes, but the $CP_{OUT,BUF}$ could not be correctly measured under ESD tests because the direct coupling of ESD fields to the 2.2 MΩ high-impedance probe structure was too strong.

The 3-, 5-, and 8-kV ESD levels were tested for every case. As examples, the measured voltage waveforms under 8-kV ESD events in Case 1 and Case 5 were plotted in Figs. 9(a) and (b), respectively. CLK, CLKb, and DLL_CLK deviated from their ideal shapes. In Case 1, VDD and Vbias had huge fluctuating noises, whereas the VDD and Vbias noises were effectively reduced by four VDD-GND de-caps and a Vbias-GND de-cap in Case 5.



(a)

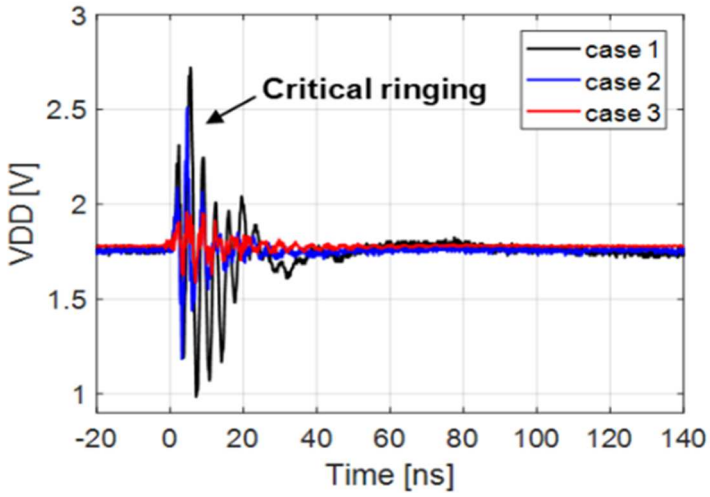


(b)

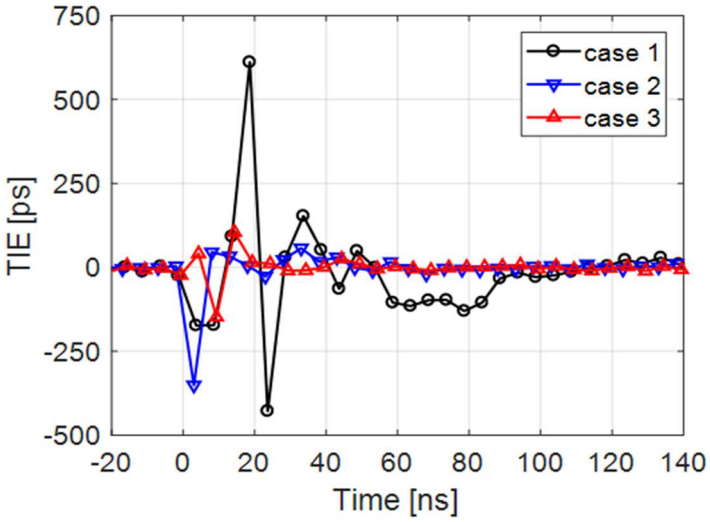
Fig. 9. Measured voltage waveforms under 8-kV ESD (a) case 1 (b) case 5

To compare the results regarding the existence of VDD-GND de-caps clearly, the measured VDD noises and TIEs of the DLL_CLK for Cases 1, 2, and 3 were plotted in Figs. 10 (a) and (b), respectively. As the number of VDD de-caps increases, the huge ringing noises are greatly suppressed. Also, the peak-to-peak jitter and jitter duration time of DLL_CLK clearly decreases. In Case 1, without any VDD-GND de-caps on the DIMM, the peak-to-peak jitter is about 1039 ps and the TIE remains larger than 100 ps for about 80 ns. For convenience, from now on, the jitter duration time is defined as the time period where TIE is larger than 100 ps. For example, if the jitter tolerance allowing for a correct data sampling is 100 ps, then data communication would be impossible for the time duration of 80 ns (16 cycles of 200-MHz clock) due to the system-level ESD noise. It can cause lots of data loss and eventually a soft failure of the whole system. The TIE of Case 2 with four VDD-

GND de-caps became stable within 5 ns and the peak-to-peak jitter was 408 ps. In Case 3, with sixteen VDD-GND de-caps, TIE became stable by 5 ns and the peak-to-peak jitter is 253 ps. The eye diagrams of DLL_CLK in the three cases were also plotted in Fig. 10(c). The EYE diagrams were obtained from the measured waveforms from 100 ns before- to 20 us after- the ESD injection (about 4000 periods of 200-MHz clock). As the number of VDD de-caps increases, the eye diagram gets clearer and approaches the clean eye of Fig. 8(c).



(a)



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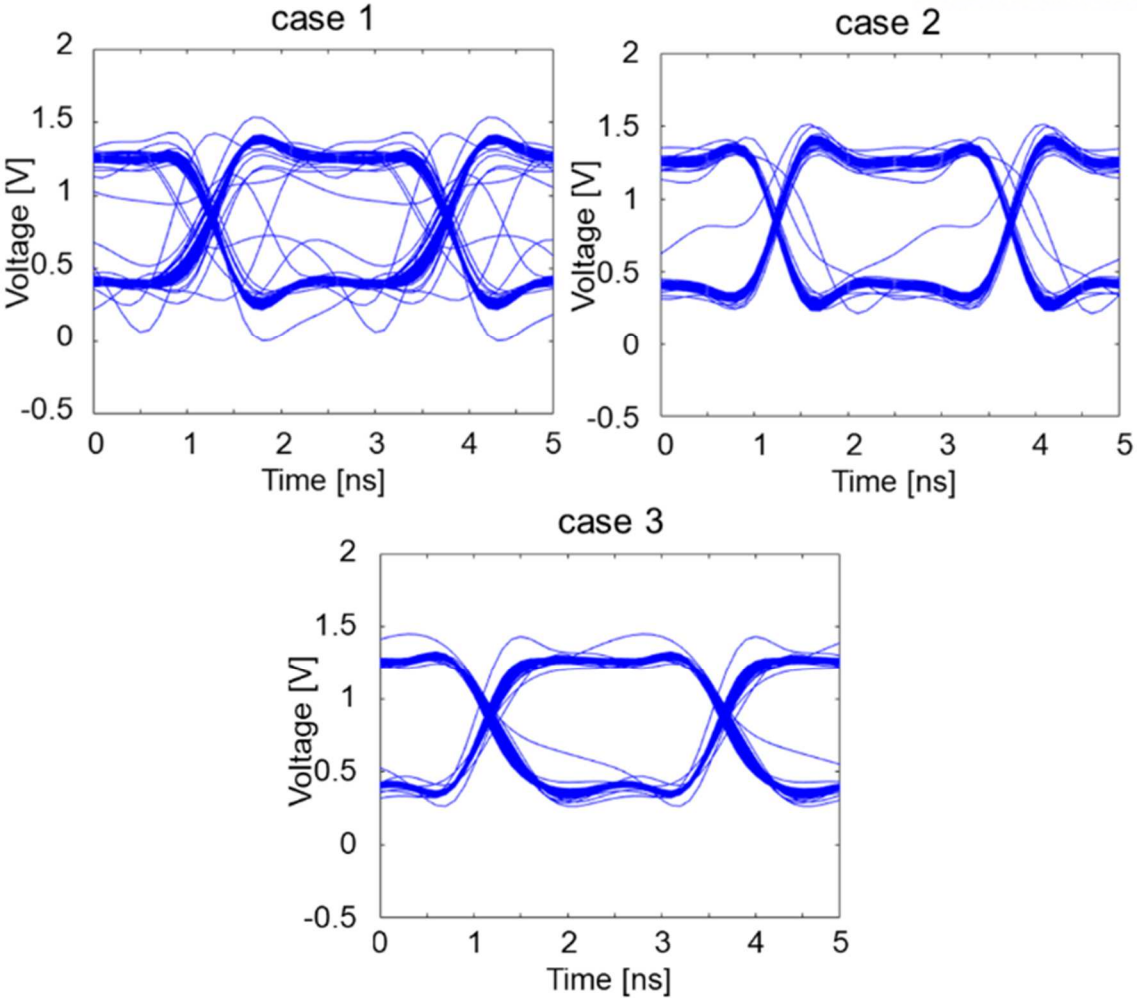


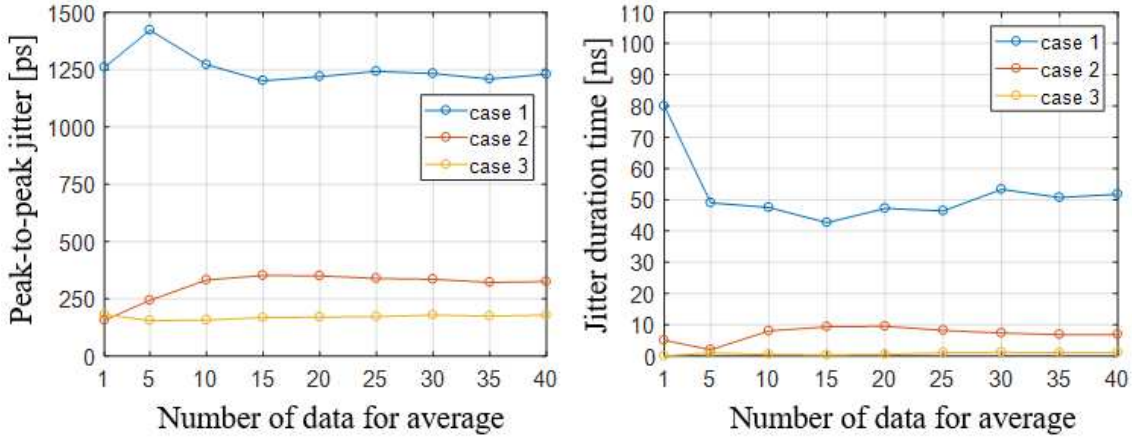
(c)

Fig. 10. Measurement results of Case 1, 2, and 3 under 8-kV ESD (a) VDD noises (b) TIE of DLL_CLK (c) eye diagram of DLL_CLK

For the simple flip-flop circuits in [25] and [26], the ESD-induced disturbance sometimes resulted in a soft failure but sometimes did not, depending on the disturbance timing. Similarly, the values of VDD noise, peak-to-peak jitter, and jitter duration time of the DLL are not exactly the same among the repeated tests because of the different ESD event timing regarding the clock phase. If the number of repeated tests is sufficient, however, their average values would statistically converge. In Figs. 11(a) and (b), the average values of peak-to-peak jitter and jitter duration time of three cases under 8 kV ESD were plotted according to the number of repeated tests. As the number of tests increases, the average values were converging and 40 times repeated measurements seem to allow for a sufficient convergence in any case. The averages of VDD noise, peak-to-peak jitter, and jitter duration time from 40 repeated tests per each case are summarized in Figs. 12 (a), (b), and (c). Comparing Case 1, 2, and 3 in Figs. 12 (b) and (c), the VDD-GND de-caps are very effective in reducing the peak-to-peak jitter and jitter duration time induced by ESD. The VDD-GND de-caps also reduce the VDD noises,

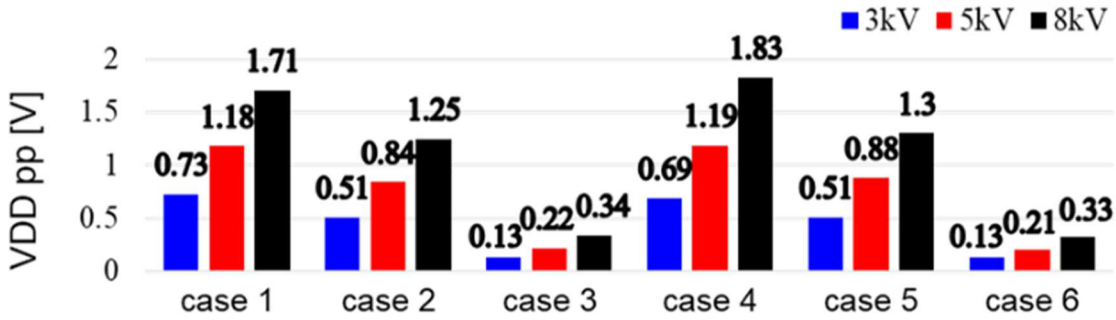
as shown in Fig. 12(a), but have even more effects on the jitter reduction.

On the other hand, as shown in Fig. 12(d), the Vbias-GND de-cap greatly reduces the noise fluctuation in Vbias voltage, but has no clear effects on the reduction of jitter. If comparing Case 1 with Case 4 in Fig. 12(b), the Vbias-GND de-cap is a bit effective for reducing peak-to-peak jitter, but that is always not the case. The jitter duration time is rarely affected by the Vbias-GND de-cap, as shown in Fig. 12(c). In summary, stabilizing the VDD voltage is crucial to improving the immunity of DLL against system-level ESD; however, stabilizing the bias voltage for analog buffers inside DLL has little effect.

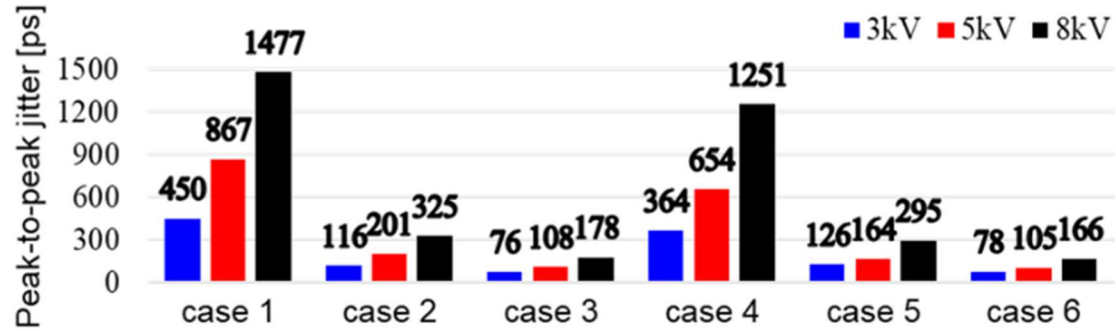


(a) (b)

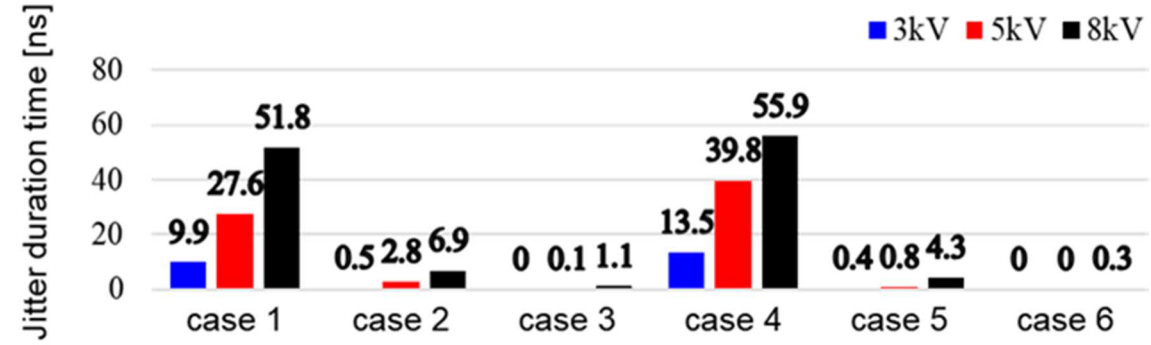
Fig. 11. Average values from repeated measurements under 8 kV ESD (a) peak-to-peak jitter (b) jitter duration time



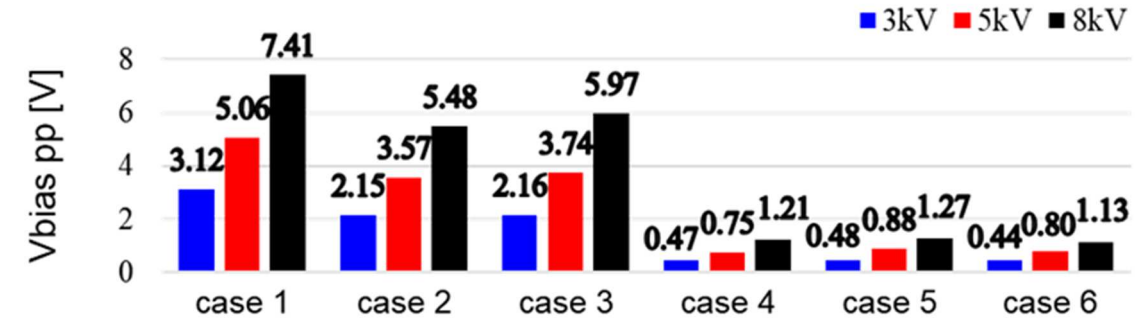
(a)



(b)



(c)



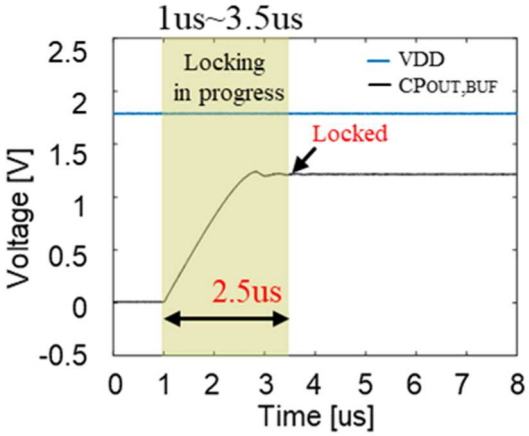
(d)

Fig. 12. Average values from 40 repeated measurements per each case (a) VDD fluctuation (b) peak-to-peak jitter (c) jitter duration time (d) Vbias fluctuation

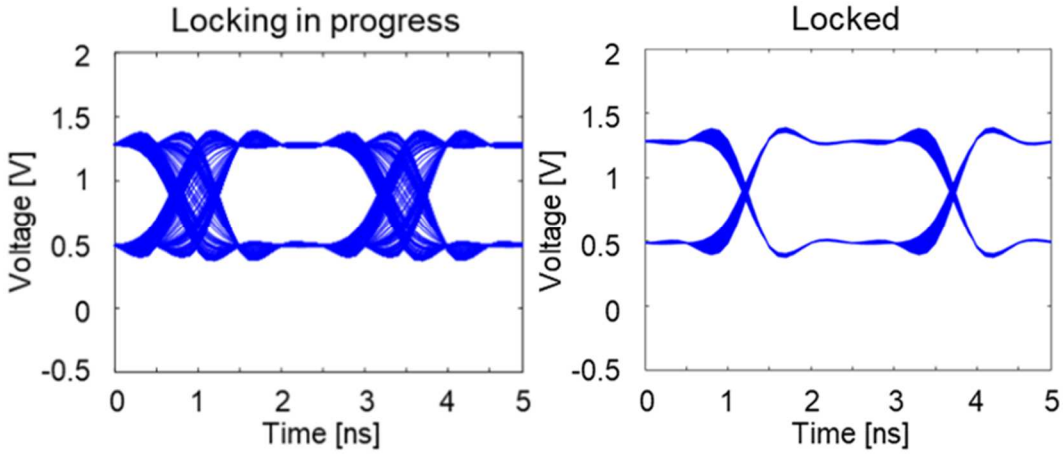
2.3 Validation and analysis by SPICE simulation

2.3.1 Validation by SPICE simulations

The measured results can be validated and analyzed using SPICE simulations of the DLL IC by applying the measured input voltages. First, the simulated outputs of the DLL during normal locking procedure were plotted in Fig. 13. Similarly to Fig. 8, the $CP_{OUT,BUF}$ and eye diagrams of DLL_CLK during and after the locking process were plotted. The simulated DLL locking time was quite shorter than the measured one, because on-chip parasitic resistance and capacitance were not included in the simulation, and the CP can draw a larger current per cycle. The simulated voltage level of $CP_{OUT,BUF}$ after the DLL locked was also a bit higher than the measured one, because the delay due to the parasitic R-C in real measurements should be compensated for by a higher CP_{OUT} level in simulations. As shown in the eye diagrams of Figs. 13 (b) and (c), the DLL_CLK phases gradually change during the locking process, but remain constant after being locked.



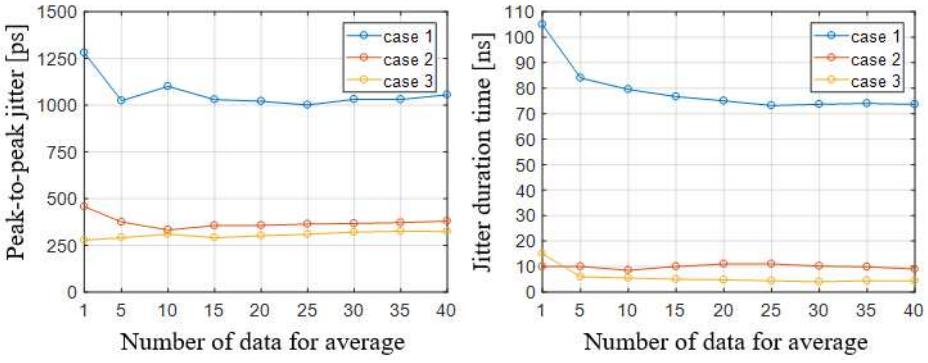
(a)



(b) (c)

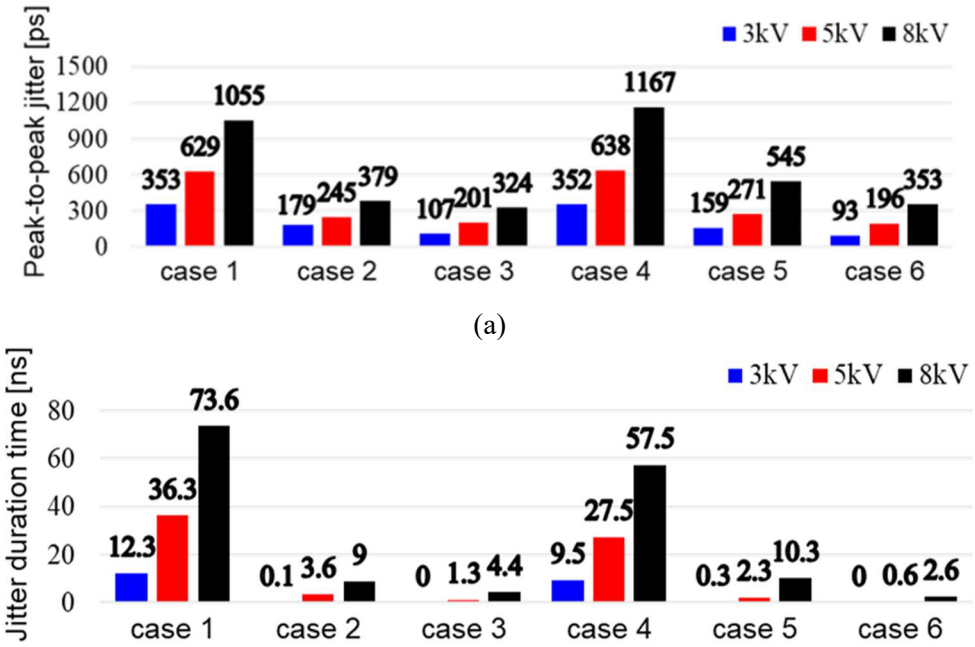
Fig. 13. Simulated voltage waveforms in Case 1 without ESD (a) $CP_{OUT,BUF}$ after the DLL is reset (b) eye diagram of DLL_CLK during the locking process (c) eye diagram of DLL_CLK for 20 us after the DLL is locked

Next, simulations under ESD events were also conducted by applying the measured CLK, CLKb, Vbias, and VDD voltages under ESD events as simulation inputs. The input voltages obtained from 40 repeated measurements were utilized for 40 simulations, respectively. The 40 DLL_CLK simulation outputs were obtained. As shown in Fig. 14, the average peak-to-peak jitter and jitter duration time of the simulated DLL_CLK converged as the number of repeated simulations increased. The average values obtained from the 40 simulations per each case are summarized in Fig. 15. The simulated jitters show quite similar trends to the measured jitters of Fig. 12. The VDD-GND de-caps are very effective in reducing the peak-to-peak jitter and jitter duration time induced by ESD events, but the Vbias-GND de-cap shows no clear effects also in the simulation. As a result, the measurement setup and results were well validated by the SPICE simulations.



(a) (b)

Fig. 14. Average values from repeated simulations under 8kV ESD (a) peak-to-peak jitter (b) jitter duration time



(a)

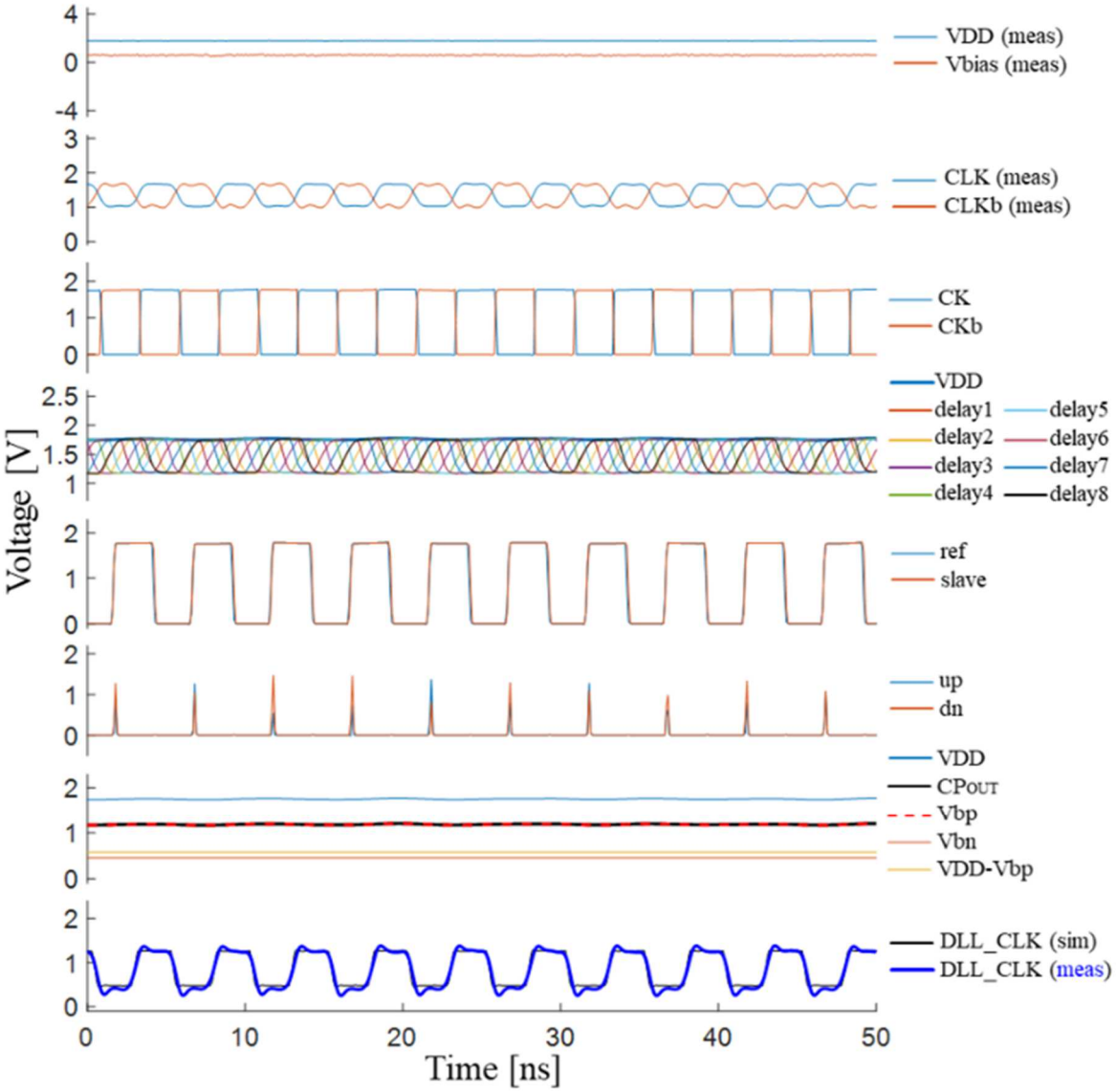
(b)

Fig. 15. Average values from 40 repeated simulations per each case (a) peak-to-peak jitter (b) jitter duration time

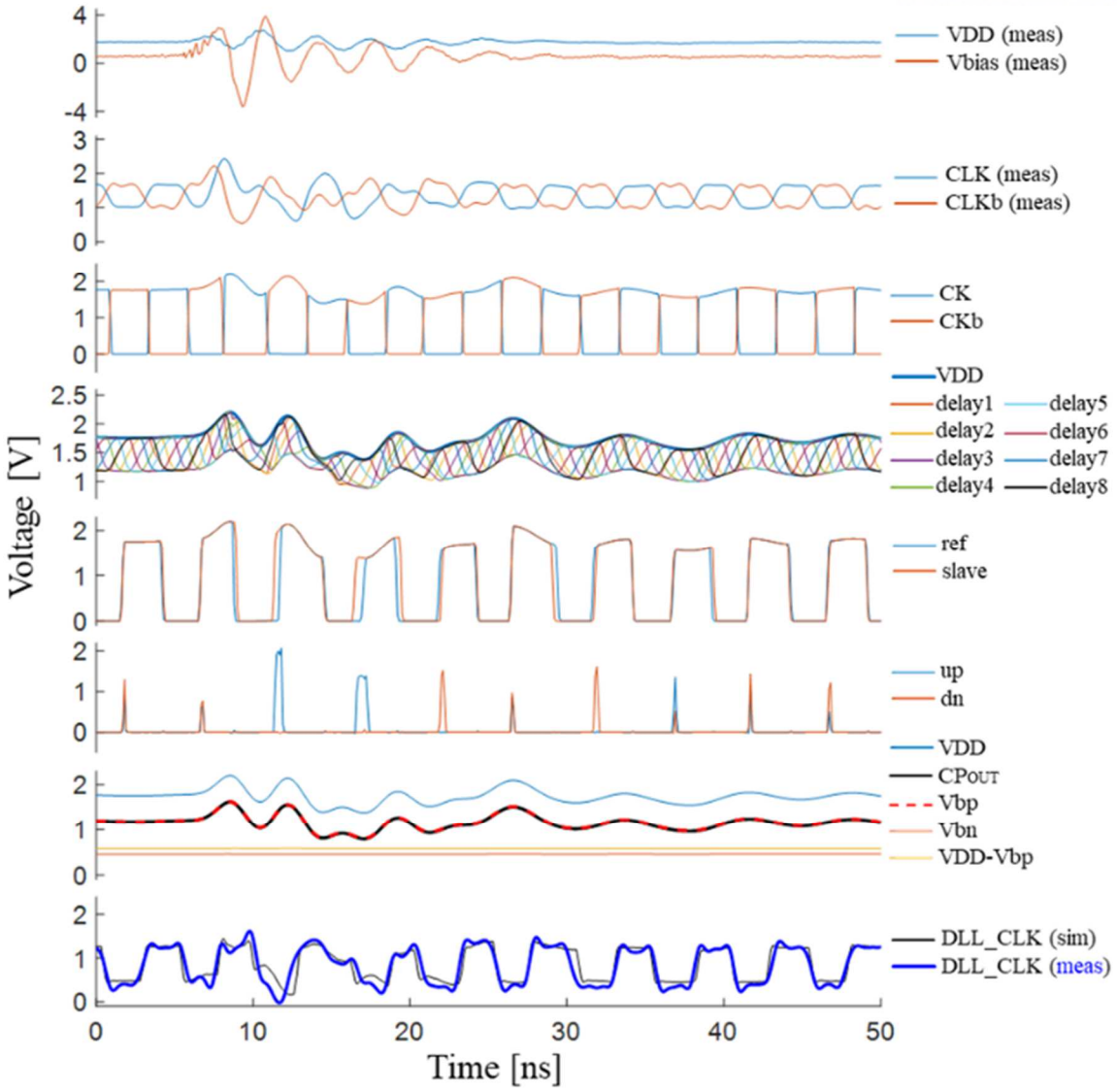
2.3.2 Analysis of DLL jitter by simulations

The root causes of the huge jitter on the DLL clocks due to system-level ESD can be analyzed in the SPICE simulations by observing how the signals inside the IC were distorted. The measured voltage noises were applied as four inputs (VDD, Vbias, CLK, CLKb) for the simulation, and the simulated voltages at internal nodes of the DLL IC were plotted in Fig. 16. Fig. 16 (a) shows the normal operation without any ESD events when the DLL is locked. The ‘ref’ and ‘slave’ clocks have the same phases, and the ‘up’ and ‘dn’ signals have short pulses with the same duration. The delay1 to delay8 represent the equally phase-shifted internal clocks in the VCDL. Fig. 16 (b) shows Case 1 under an 8kV ESD. Despite the large noises at CLK and CLKb, the differential clocks were well transmitted to the internal nodes (CK, CKb) through the input differential clock buffer. However, the phase spacing between the internal clocks inside the VCDL (delay1~8) were greatly distorted by the VDD fluctuation. During the time when a large VDD noise exists, the DLL lost the locked condition, and the VCDL output contains huge jitter. In Fig. 16, the DLL_CLK waveforms obtained from the SPICE simulations were overlaid with the measured ones in a blue color, which shows quite a good agreement. The shape and trend of the distortion of the DLL clock due to the ESD event were reproduced well in the SPICE simulations.

In [26], the robustness of the sense-amplifier flip-flop against VDD noises was much better than that of the static D flip-flop because of its differential operating nature. The logic operation of differential amplifiers is known to be robust against VDD noises. In the DLL, the jitter is the main interest because the role of a DLL is to align the clock edges at the correct timing for accurate data sampling. Although the analog DLL in this thesis has a relatively good PSRR with jitter by using differential CML delay lines as compared with digital DLLs, considerable jitters were still generated at the output clocks of VCDL due to the VDD noises. The fluctuation of VDD due to ESD directly decreases the voltage headroom for the outputs of delay cells. Furthermore, because the outputs of a delay cell are the inputs for the next delay cell, the effects of the distorted outputs keep spreading between delay cells.



(a)



(b)

Fig. 16. Voltages at internal nodes of DLL under the locked condition (a) without ESD (b) with an 8-kV ESD in Case 1

Even though the differential VCDLs were greatly affected by the ESD-induced VDD noise, the DLL did not lose the locked condition forever but recovered quickly as the VDD noise decreased. This can be explained as follows. As shown in Fig. 16(b), the Vbp and CP_{OUT} have the same noises as the VDD because of their on-chip MOSFET capacitors connected to VDD. The voltage difference between VDD and Vbp, which is the most important delay-control parameter in the delay cell of Fig. 6 (a), is rarely affected by the ESD events. Although the contaminated 'ref' and 'slave' clocks distort the 'up' and 'dn' signals for the charge pump, the distortions of 'up' and 'dn' do not last long enough to sufficiently change the clock phases. Thus, as the VDD voltage becomes stable, the DLL can return to the locked condition with the maintained amount of (VDD – Vbp). Therefore, reducing the time

duration and magnitude of the VDD fluctuation is the most effective solution allowing for the DLL clocks to have small jitter and recover quickly.

2.3.3 Investigation of DLL jitter by SPICE simulation

To validate the importance of VDD noise, the VDD voltage was forced to be constant in the SPICE simulation, while other measured input voltages (Vbias, CLK, CLKb) under the ESD were kept utilized. After the VDD was fixed at 1.8V, as shown in Fig. 17, the internal clocks in the VCDL became very stable all the time even with the noises at other input voltages (CLK, CLKb, and Vbias). As a result, it turned out the main root cause of the unequally phase-shifted clocks was the reduction of voltage headroom in the VCDL delay cells due to the ESD-induced VDD drop. Also, the difference between VDD and Vbp was stable and the locked condition was well maintained.

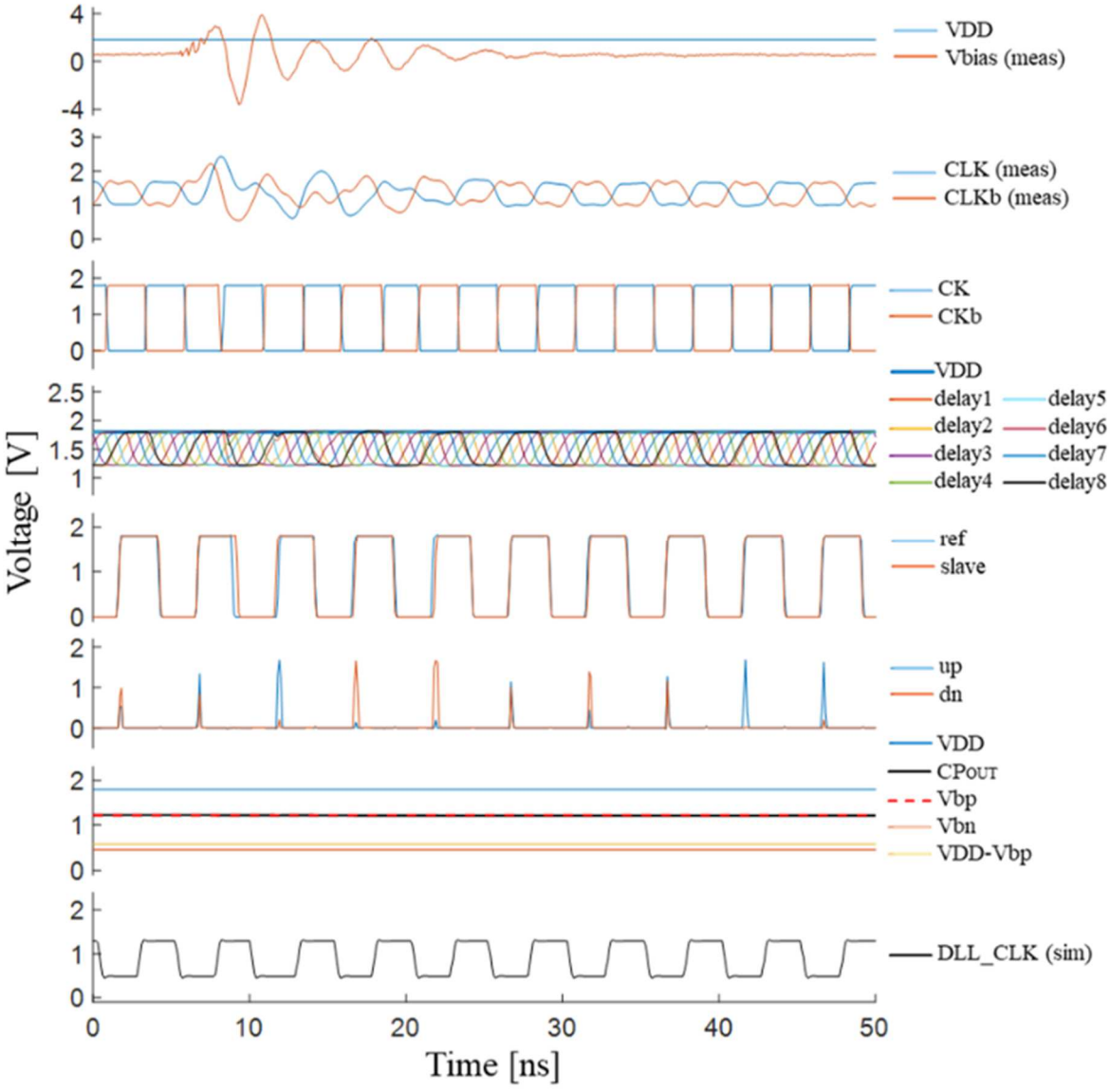
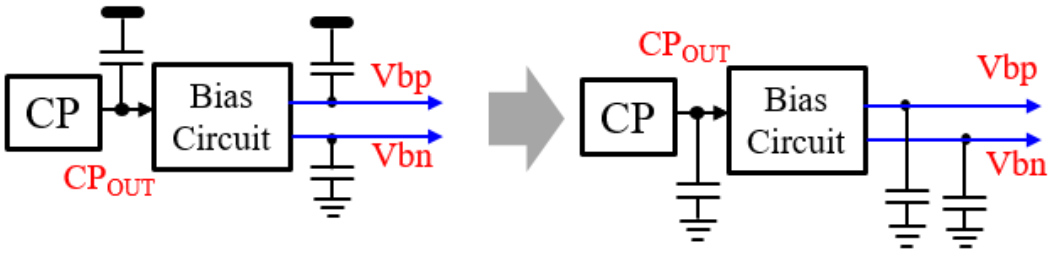
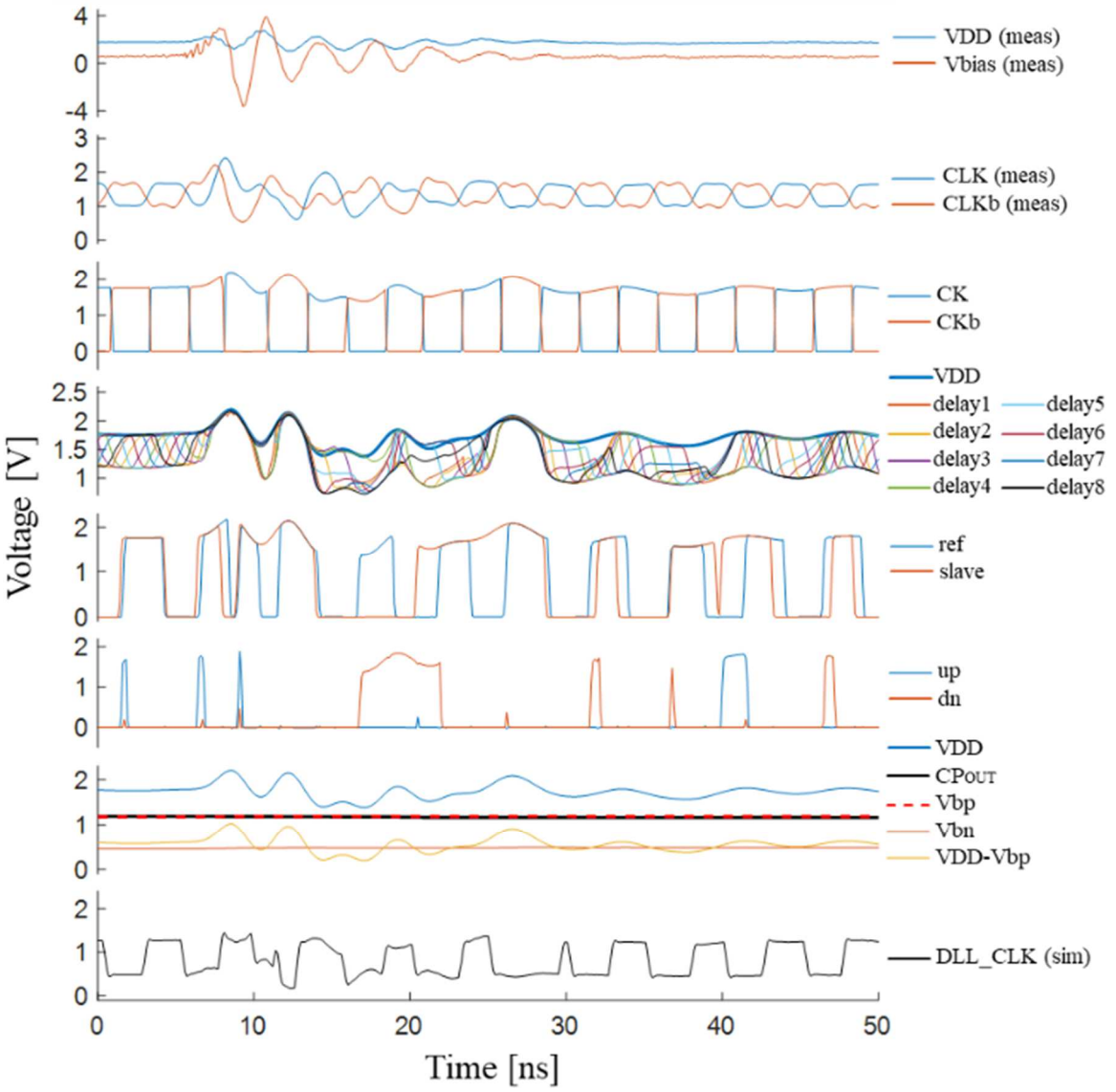


Fig. 17. Voltages at the DLL when only VDD was fixed to a constant voltage

In addition, another SPICE simulation test was conducted to validate the importance of maintaining the amount of (VDD – Vbp). Previously, in Fig. 16 (b), the voltage difference between VDD and CP_{OUT} was maintained by the PMOS capacitors connected to VDD. As shown in Fig. 18 (a), the PMOS capacitors at the CP_{OUT} and Vbp nodes were replaced with NMOS capacitors connected to GND in the simulation test. By doing that, the CP_{OUT} and Vbp voltages with regard to GND became stable during ESD event, as shown in Fig. 18 (b). However, the internal clocks in the VCDL (delay1 ~ delay8) became much more severely distorted than those in Fig. 16 (b). As a result, the DLL_CLK was also more distorted and its peak-to-peak jitter and jitter duration time were all increased. It is because the delay-control parameter, (VDD-Vbp), has the same huge variation as the VDD noise. The configuration of on-chip capacitors for the CP and delay cell's bias circuit has critical effects on the immunity against the system-level ESD.



(a)



(b)

Fig. 18. (a) Replacement of PMOS cap with NMOS cap for the CP and delaycell's bias circuit (b) Voltages at the DLL

2.4 Analysis of VDD-GND noise using measurement of impedance parameters and ESD current

The VDD noise due to system-level ESD was significantly reduced by employing VDD-GND de-caps, which results in the improved jitter characteristics of DLL_CLK. To understand the effects of the VDD de-caps in frequency domain, the Z-parameters were extracted from the measurements using a vector network analyzer (VNA). As shown in Fig. 19, the signal pin of the SMA connector at Port 1 was soldered to the GND pad of the motherboard for ESD injection, and its ground was soldered to a ground strap and simplified ESD gun body. The ground strap was connected to the GRP. The body was made of a simple hollow aluminum cylinder. The signal pin and ground of the semi-rigid cable at the Port 2 were soldered to VDD and GND of the DIMM, respectively. The overall setup for the Z-parameter measurements is basically the same as those in [25].

The measured Z-parameters of Cases 1, 2, and 3 are plotted in Fig. 20. The Z21 parameter represents the VDD noise on the DIMM caused by the injected current at Port 1, while the Z22 represents the input impedance at Port 2. The Z22 and Z21 parameters have peaks at the same frequencies, which is attributed to resonances. As already analyzed and modeled in [25], in Case 1, the first resonance peak at a lower frequency is caused by the IC's on-chip capacitance and the inductance of the current path along the DIMM socket and motherboard. The second resonance peak at a higher frequency is attributed to the VDD plane capacitance of DIMM and the inductance between the DIMM and DLL IC. In Cases 2 and 3, the first resonance peak moved to a higher frequency because the DIMM de-caps provided a lower inductance path, replacing the inductance path along the socket and motherboard. The second resonance peak also moved to a higher frequency as the inductance of the DIMM de-caps were added in parallel, resulting in a reduction of the inductance that resonates with the plane capacitance of DIMM.

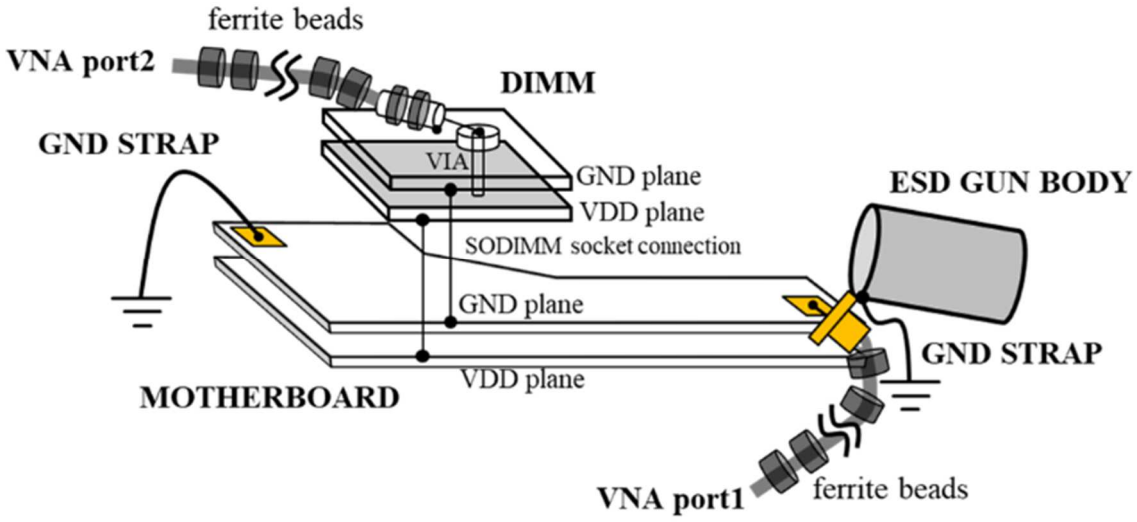


Fig. 19. Setup and port conditions for the frequency-domain measurements using a VNA

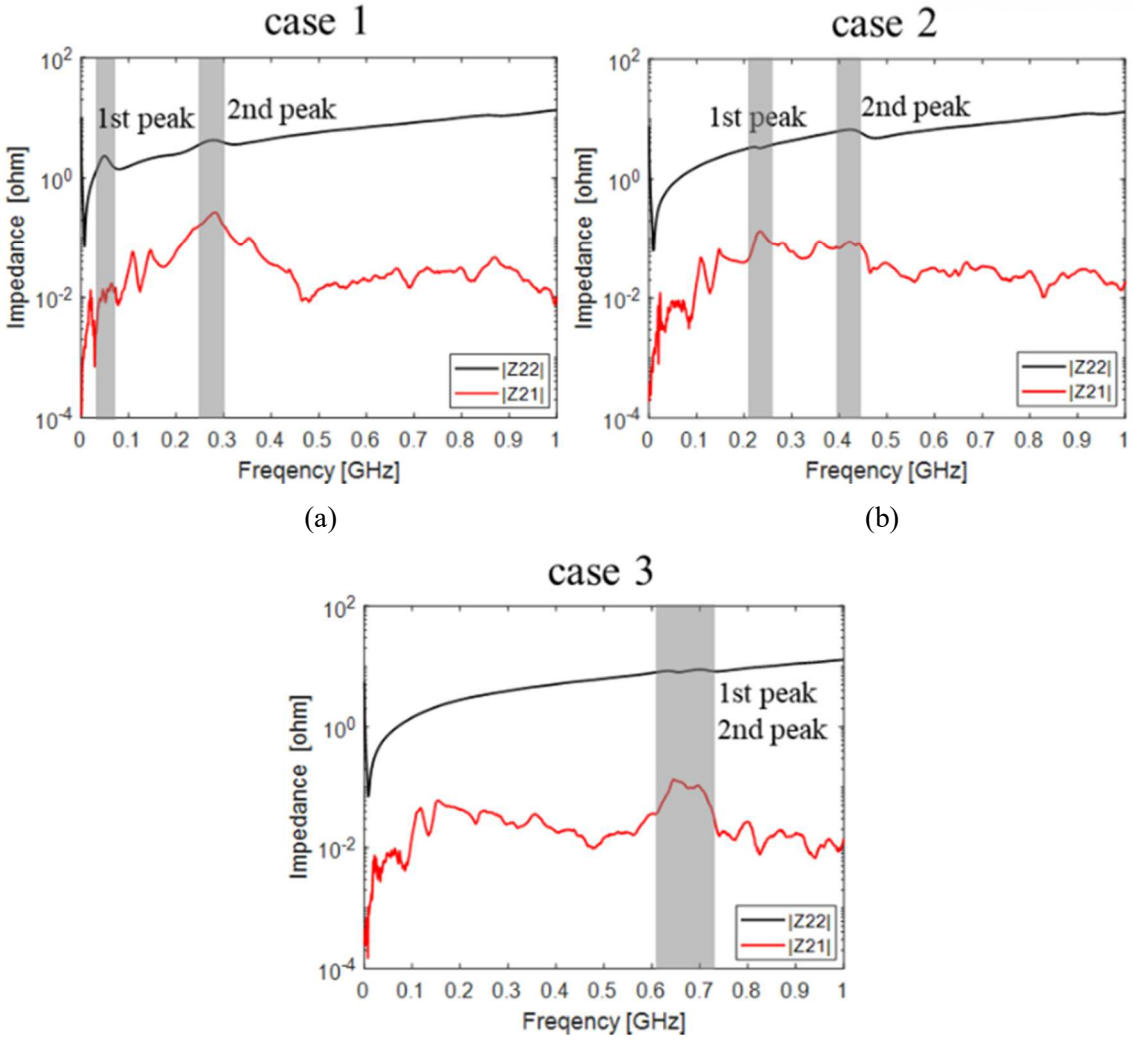


Fig. 20. Measured Z22 and Z21 parameters (a) Case 1 (b) Case 2 (c) Case 3

The frequency spectra of the transient VDD noise due to ESD can be calculated by multiplication of the measured Z21 parameter and the frequency spectra of ESD injection current. The transient ESD injection current was separately measured using a current probe, and its spectra were obtained by fast-Fourier-Transform (FFT). The time-domain VDD waveform is then obtained by inverse-FFT from the calculated frequency spectra of VDD noise. The procedure was also already demonstrated in [25]. In Fig. 21, the VDD waveforms reconstructed using Z21 parameters were compared with those directly measured using the oscilloscope, which shows reasonable agreements between each other. For easy comparison, a dc 1.8V was subtracted from the voltages measured using the oscilloscope.

In Case 1, the critical ringing frequency at the time-domain VDD noises was about 200 ~ 300 MHz, which corresponds to the second resonance peak in Fig. 20 (a). In Case 2 or 3, the second resonance frequency moved to 420MHz or above, which resulted in a significant decrease in the VDD noise. If a resonance peak in Z-parameters moved to a higher frequency, the resultant VDD noise would decrease because low- frequency components are predominant in the ESD current.

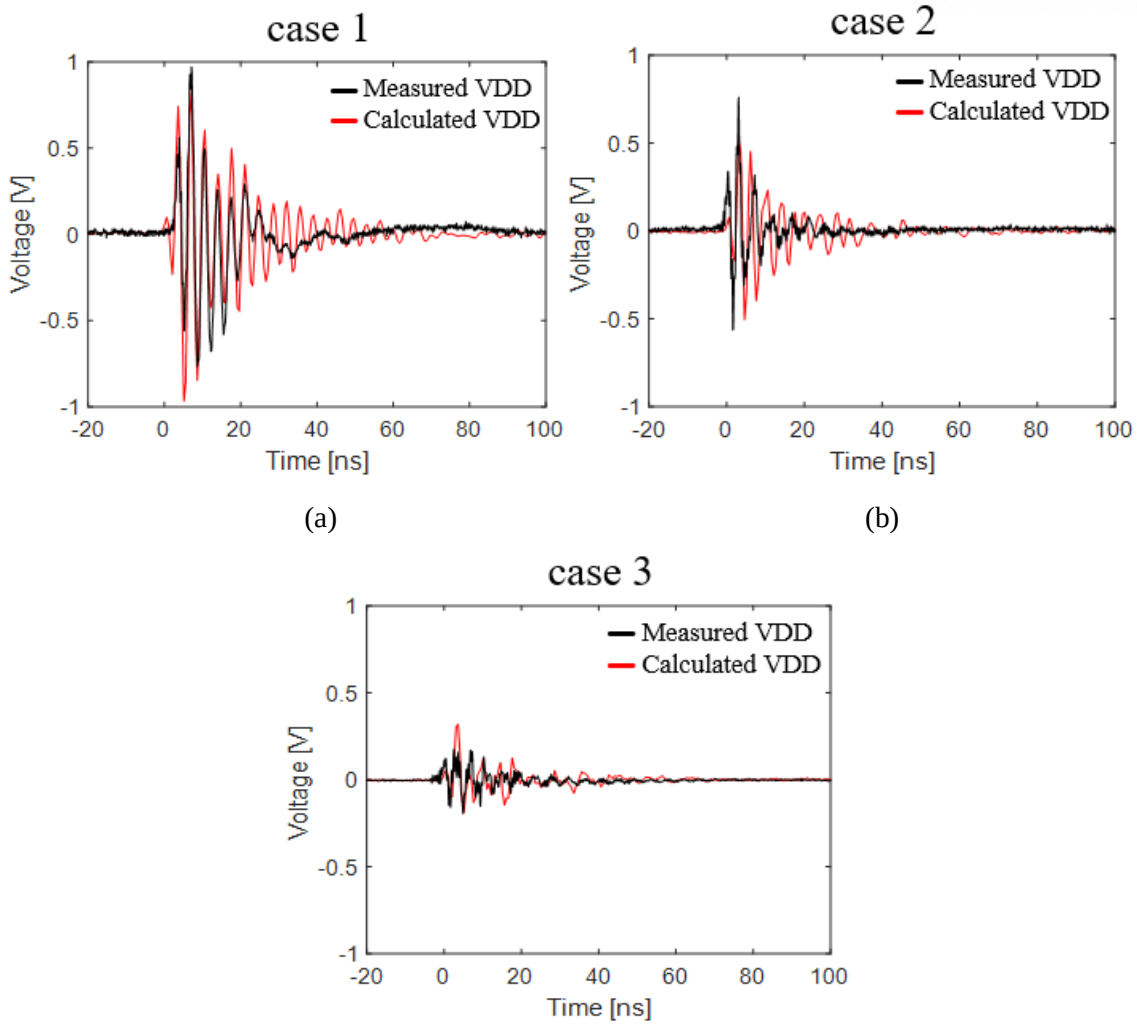


Fig. 21. Comparison between the VDD waveforms reconstructed using Z21 parameters and those directly measured using an oscilloscope (a) Case 1 (b) Case 2 (c) Case 3

2.5 Conclusion

System reboots and freezing problems of end-user electronic devices such as laptop PCs and mobile phones due to system-level ESD are great threats to system stability. Because a DLL plays an important role that compensates the data communication timing in DRAM, the ESD-induced DLL jitter might be one of the culprits of system-level ESD-induced soft failures. In this thesis, a typical analog DLL was tested under 3-, 5-, and 8-kV ESD events with a simplified laptop motherboard and DIMM structures. The DLL IC was fabricated in a 180-nm CMOS process and mounted on the DIMM. The input and output voltages with ESD-induced noises were measured using two synchronized oscilloscopes. The average values of peak-to-peak jitter and jitter duration time of the DLL clock induced by ESD events were obtained from repeated measurements and compared with simulated ones, which were obtained by applying the measured input voltages as SPICE simulation inputs. The correlation between the VDD noise and the jitter of DLL clock were investigated. The stabilization of the VDD voltage by employing VDD de-caps was very effective in reducing the ESD-induced jitter of the DLL clock, while employing a bias de-cap was not important. To discover and validate the root causes of the DLL clock jitter, SPICE simulations were conducted with various conditions. The huge jitter was attributed to the reduced voltage headroom in the delay cells of VCDL due to ESD-induced VDD drop. Also, maintaining the amount of delay control parameter, (VDD-Vbp), was crucial for stable operation of the DLL under ESD events. To analyze the effects of VDD de-caps on the ESD-induced VDD noise, which is critical to jitter, the impedance parameters were extracted from the measurements using a VNA in the frequency domain. The time-domain VDD noise was also successfully reconstructed from the measured Z21 parameter and ESD injection current, which validates the measurements and analysis. In summary, it was found that lots of data losses or soft failures can occur due to the DLL jitter induced by system-level ESD even though the DLL does not lose the locked condition.

III. System-level ESD-induced Soft Failure of a Sense Amplifier

3.1 Operation of a sense amplifier flip-flop

In Fig. 22, designed SAFF's schematic is depicted. The rectangles express the pads on the SAFF IC and PCB, respectively. The pads are connected through wire-bonds. Each wire-bond is dominantly considered as its inductance. For on-chip ESD protection, diode-connected MOSFETs are utilized at signal pads. The full-swing CLK is utilized by buffering external small-swing CLK with the inverter buffers, whereas the small-swing IN, input signal, is directly applied to the gate of the MOSFET. The operation of the SAFF are described as follows [34]. When the CLK is low, the n4 (S) node and n5 (R) node are pre-charged to the VDD level, and the output level of the latch is maintained according to the Table 3. At the rising edge of the internal CLK, if the IN is higher than the Vref voltage, current is conducted dominantly through a path that is formed from n4, n2, and n1 to the ground. The n4 node would be discharged to ground, n5 node voltage is remained. Therefore, the latch would produce low Q (OUT). If the IN voltage is lower than the Vref voltage at the rising edge of the CLK, the latch would output high Q (OUT), oppositely.

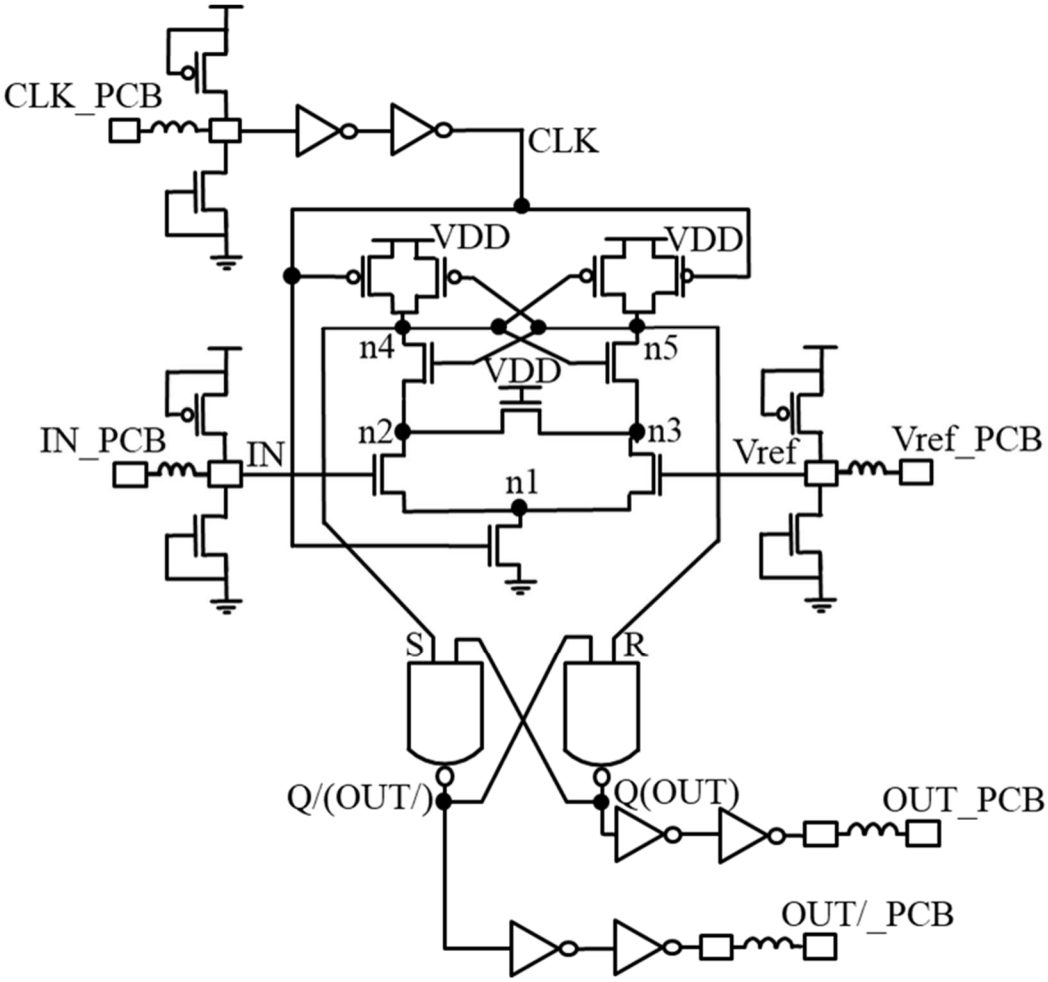


Fig. 22. Circuit schematic of a SAFF

Table 3. Truth Table of the SR Latch

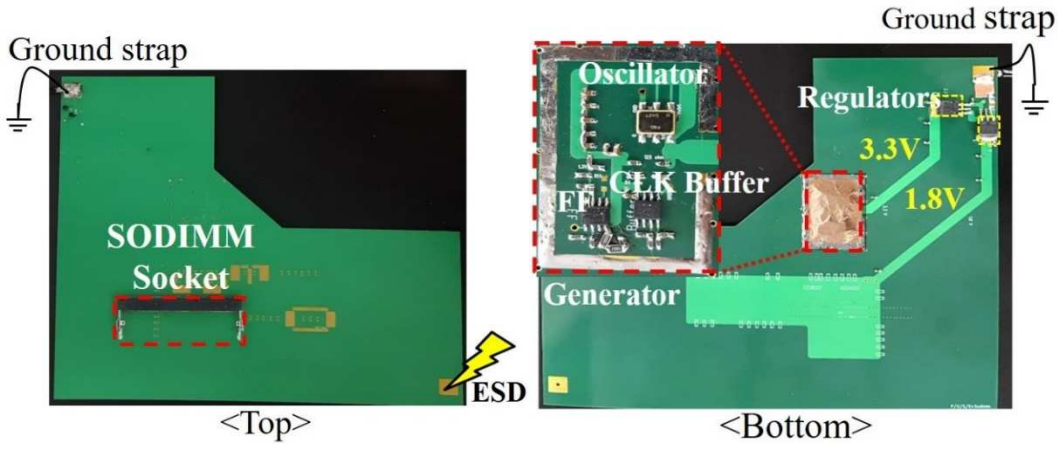
S	R	Q	Q/
0	0	1	1
0	1	0	1
1	0	1	0
1	1	HOLD	

3.2 Design and experiments for system-level ESD tests of a SAFF

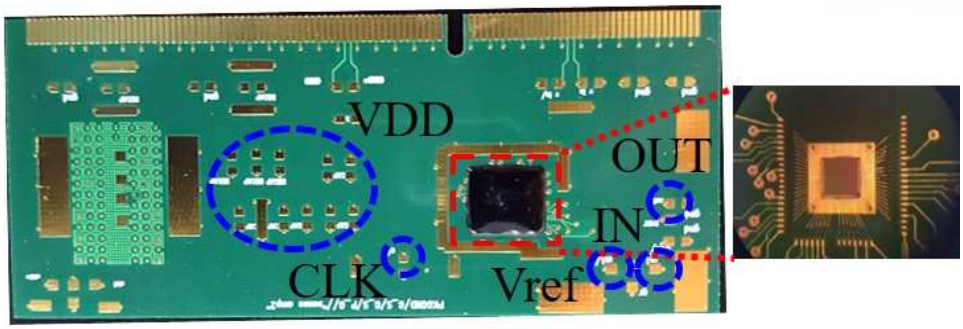
3.2.1 Designed motherboard and DIMM

A laptop PC's motherboard and DIMM were designed in simpler form as shown in Fig. 23 (a) and (b). An dc supply applies 6V dc power to regulators on the board. One regulator applies 3.3V to the motherboard's generator and the other supplies 1.8V to the IC on the designed DIMM. The generator produces input signals for the IC such as CLK, IN, and Vref. The CLK is a 200-MHz clock signal, IN is a 100-MHz rectangular and periodic signal, and Vref is a dc bias voltage for input reference. The pseudo differential inputs consist of the IN and Vref for the SAFF. The VDD is the 1.8V power and OUT and OUT/ are the differential outputs of the circuit.

VDD, CLK, IN, Vref, and OUT are measured at the measurement points on the DIMM as shown in Fig. 23 (b). The designed SAFF is fabricated in a 180-nm CMOS process. By the COB assembly, the IC is mounted on the designed DIMM. As shown in Fig. 23 (c), signal trace layout of the DIMM and motherboard is described with 4-layer PCB with FR-4. In Fig. 23 (d), the detail of circuit structure and connection is described. All signal traces are fabricated to be 50 Ω characteristic impedance. For impedance matching, the CLK and IN are connected to GND with 50 Ω resistors on the DIMM, and the OUT and OUT/ are connected to power and ground by using 100 Ω resistors and swing at a half of 1.8 V.



(a)



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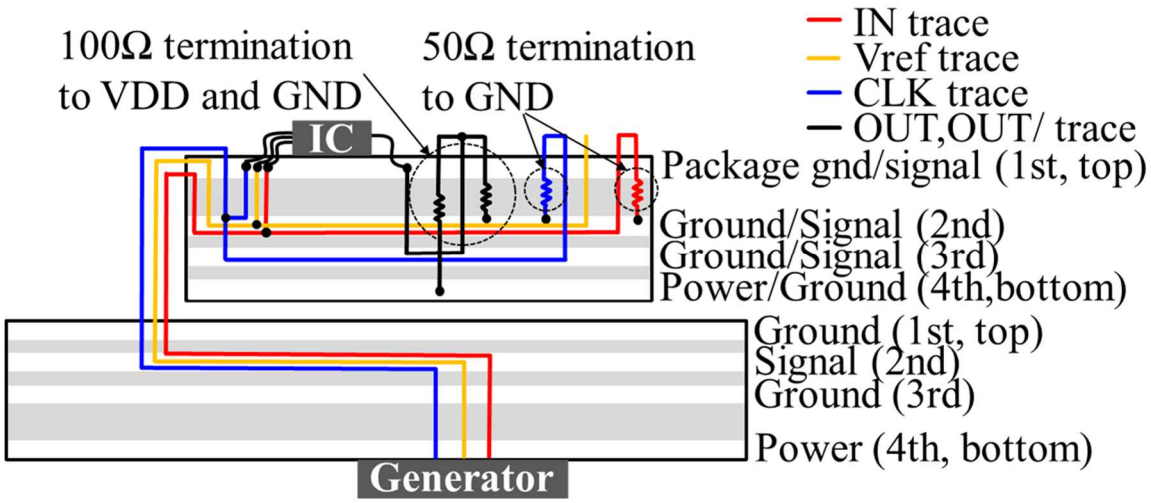
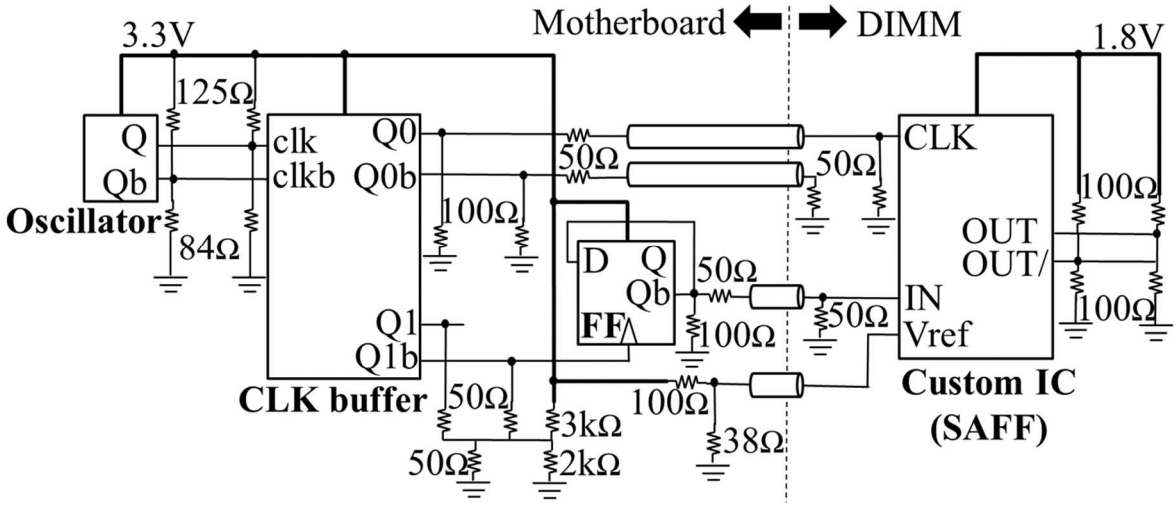


(c)

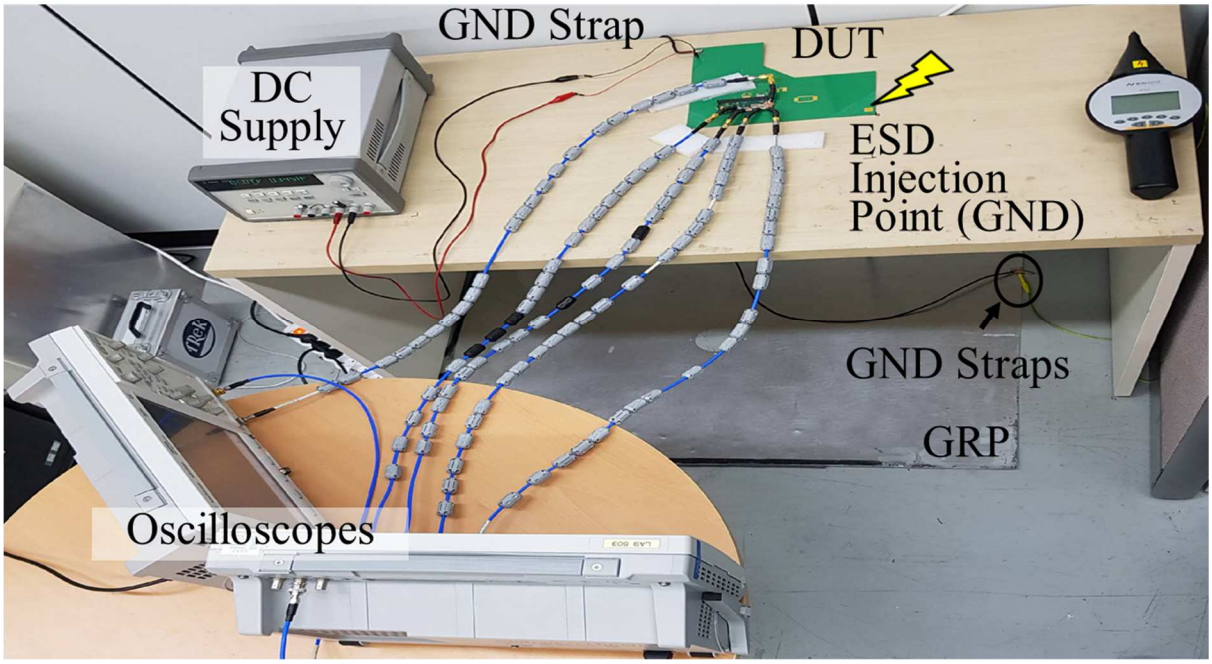


(d)

Fig. 23. (a) Motherboard (b) IC and DIMM (c) signal trace layout (d) diagram of the circuits

3.2.2 Measurement setup

In Fig. 24, test setup for ESD event is provided. By using two synchronized oscilloscopes, IN, Vref, OUT, CLK, and VDD voltage were simultaneously measured. At the corner of the ground plane of the motherboard, ESD injection point is placed. Coaxial rigid cables with ferrite cores that decrease common mode noise due to ESD is utilized at the measurement points, as shown in Fig. 24 (b). Copper tape is used to shield the measurement points. To construct high impedance probe, each signal pin of the rigid cable is soldered with 470Ω resistor in series so it is a 10:1 probe [33]. Power and ground on the DIMM have four pad positions to utilize four 10-uF de-caps between them.



(a)

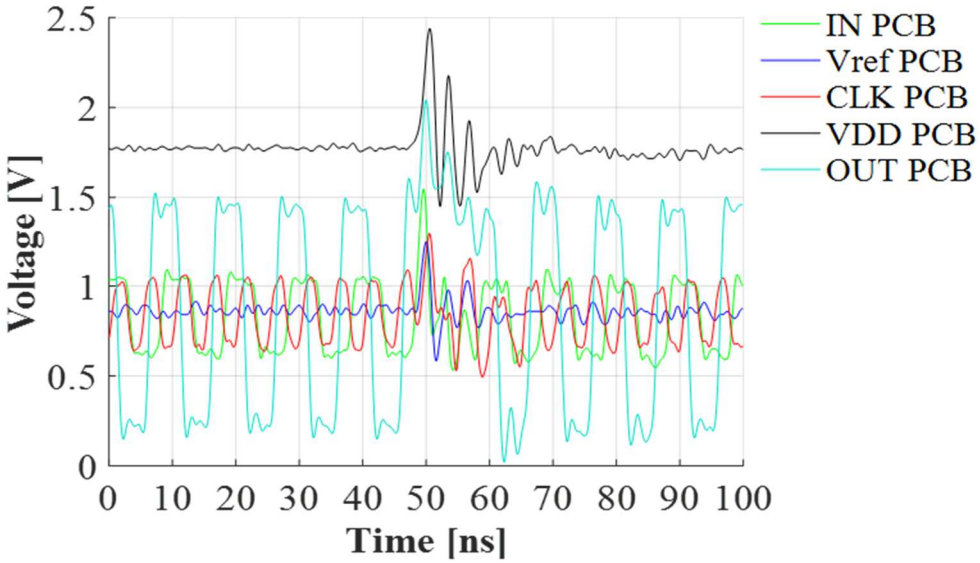
(b)

Fig. 24. (a) Test setup for ESD events (b) measurement points and de-cap positions on the DIMM

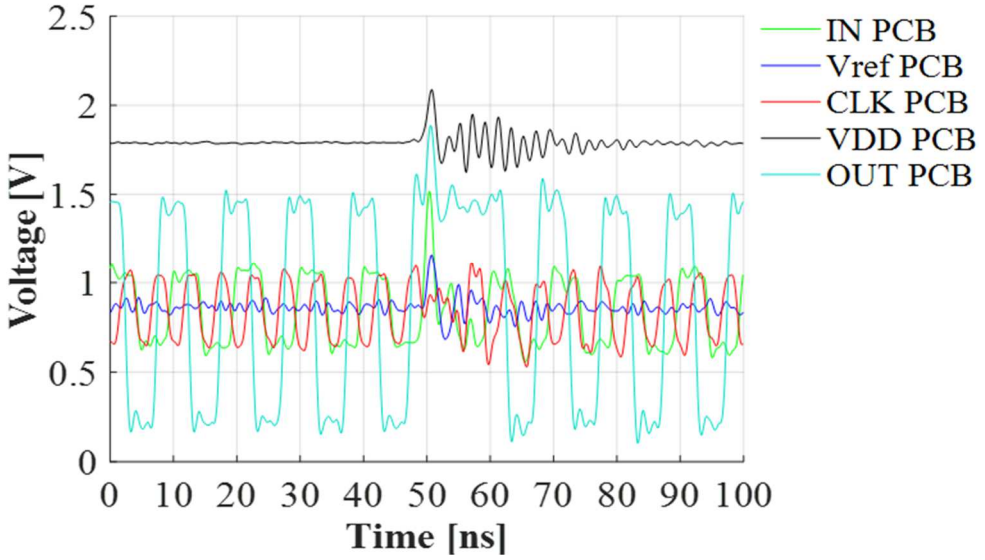
3.3 Measurement results

According to presence of the four 10-uF SMD de-caps on the DIMM, two experiment cases were designed and compared. For the two cases, ESD was excited 50 times with ESD voltage level, 3, 5, and 8 kV, respectively, and all noise voltages were obtained simultaneously. As examples, in Fig. 25 (a) and (b), two cases without any decoupling capacitors and with four decoupling capacitors, respectively, were compared with the measured noise voltages including soft failure due to a 5-kV ESD. The lost proper state of OUT is clearly observed in Fig. 25 (a). The OUT should be low around 55ns because the OUT is periodic. And its duration also is somewhat distorted due to the injection of ESD. The case with distorted OUT duration only was not considered as a soft failure since the duration distorts ambiguously and widely. Therefore, only reversed logic state of OUT was considered as soft failures. The decoupling capacitors on the DIMM hugely reduce the noise on VDD but do not remove OUT logic error as shown in Fig. 25 (a) and (b).

During the repeated 50 times ESD tests for each case, the soft failures' occurrence ratio is summarized in Fig. 26 (a). That of the static flip-flop IC was obtained previously with the similar test conditions in [25] and the results were brought in Fig. 26 (b) for comparison. Without any de-caps case, the SAFF has a much greater immunity against ESD than the static flip-flop IC. The 10uF de-caps were very effective in decreasing soft failures of the static flip-flop, however; they are not effective for the SAFF. To find and analyze the reasons, SPICE simulations were utilized by using measured noise voltages.

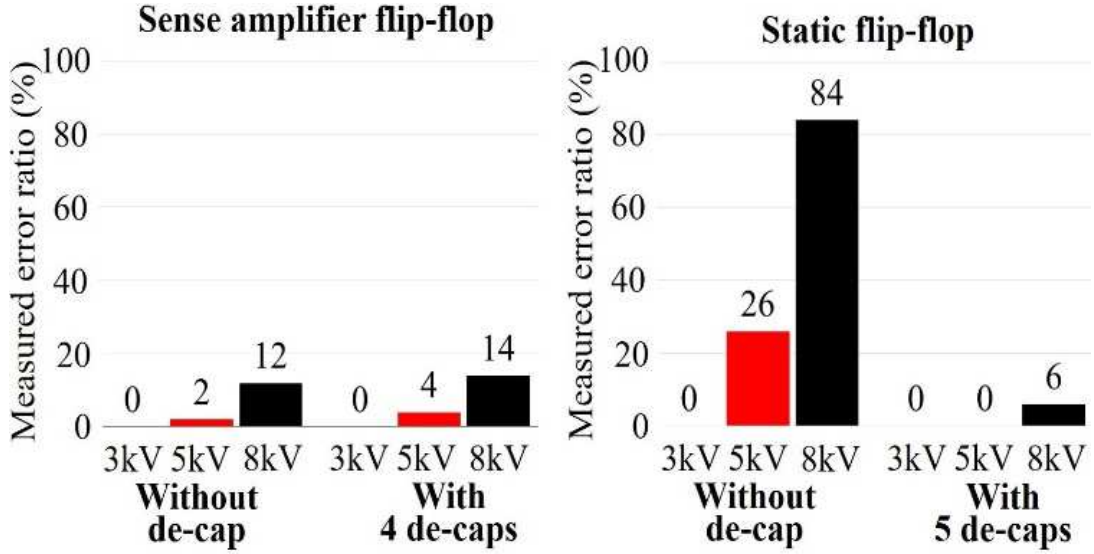


(a)



(b)

Fig. 25. Measured noise voltages due to a 5-kV ESD for the two cases (a) without any power-ground decoupling capacitors (b) with four 10uF power-ground decoupling capacitors



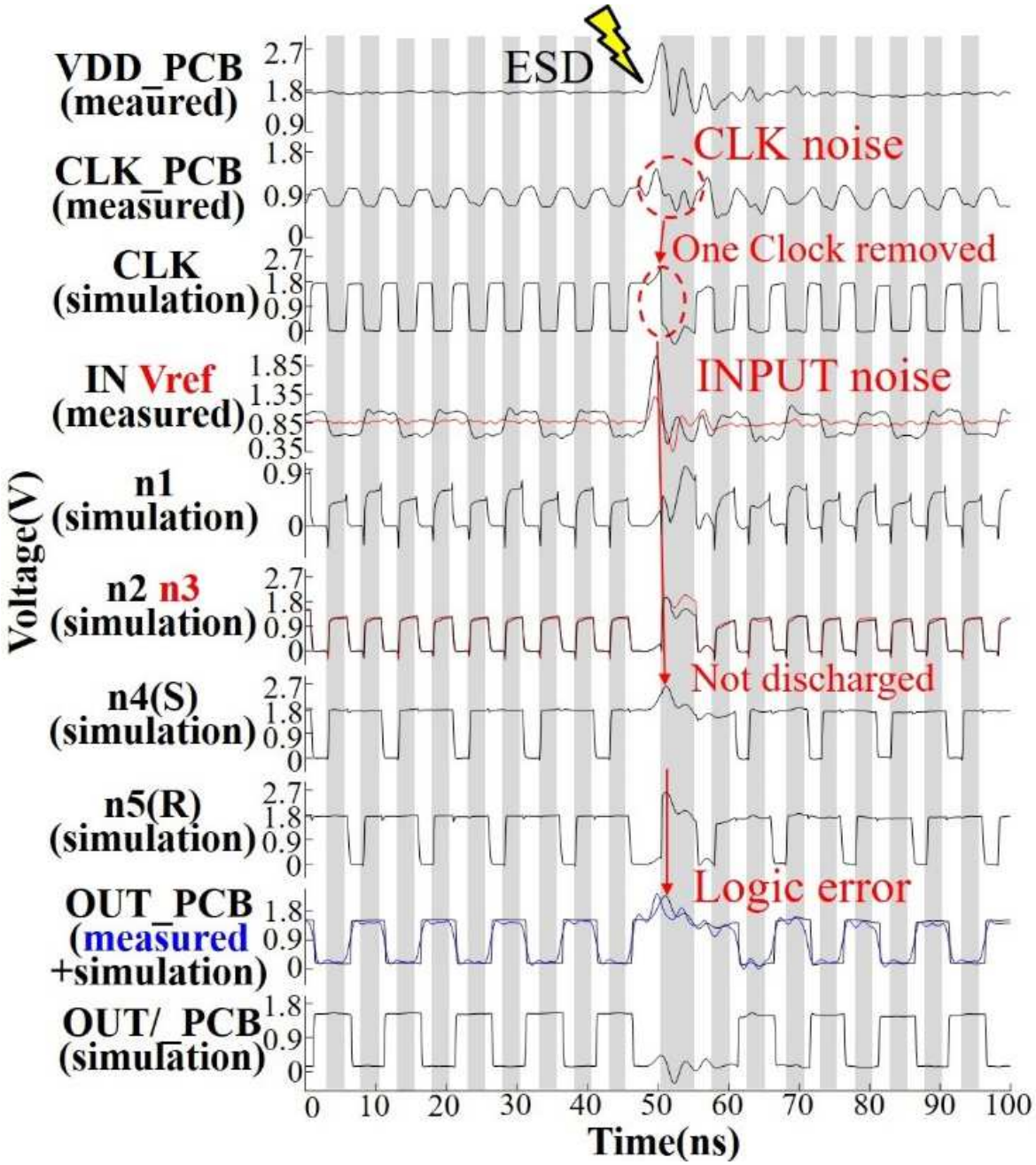
(a) (b)

Fig. 26. Experimental soft failure occurrence ratios of (a) a sense amplifier flip-flop case (b) a static flip-flop case [25]

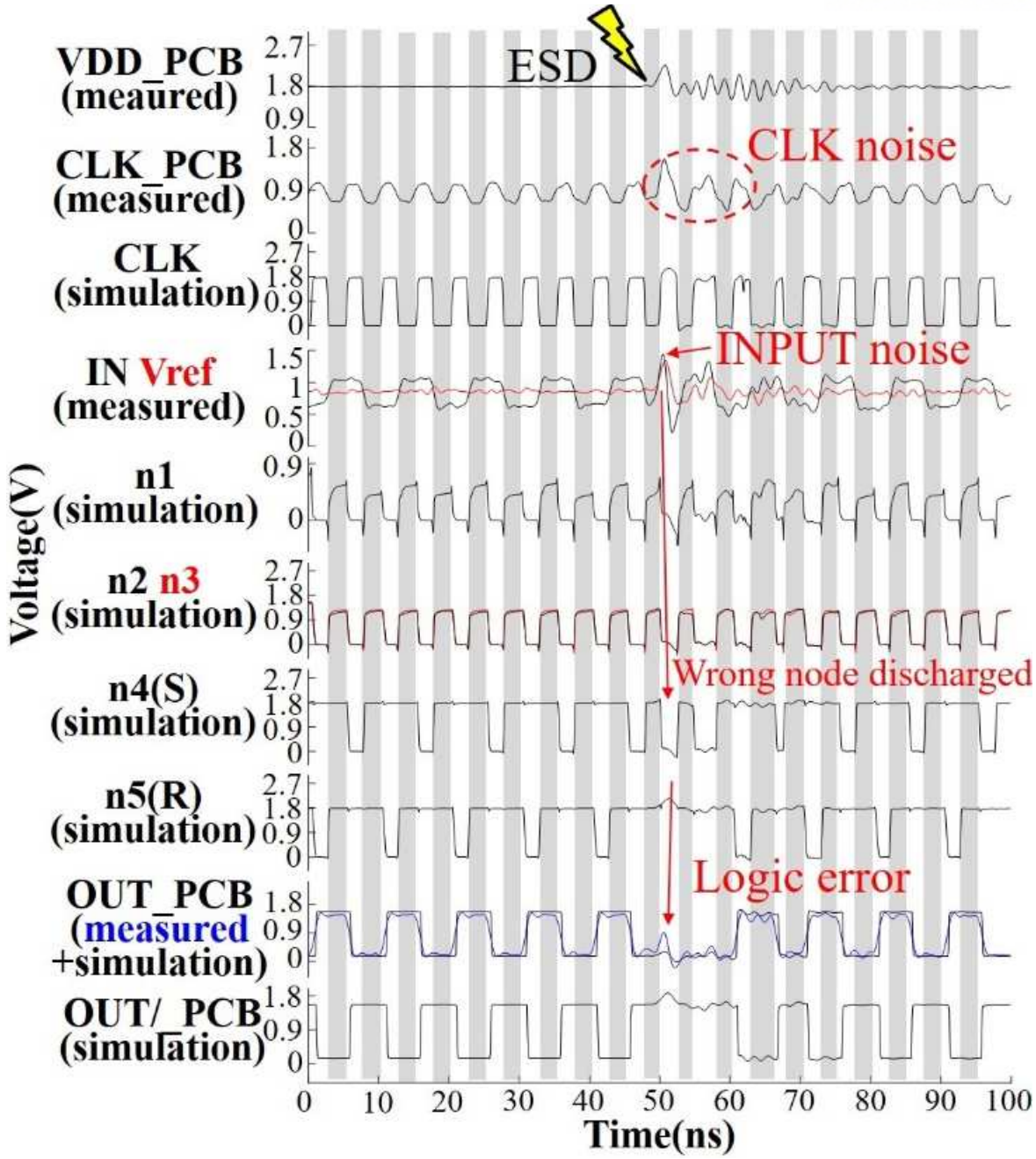
3.4 Validation and analysis by SPICE simulation

With the SPICE device library, the post-layout SPICE simulations of the SAFF IC in Fig. 22 was conducted. The parasitic resistance and capacitance from the on-chip interconnecting metal lines were included in the simulations. Since inductance of the wire-bond at pads is dominant in the modeling the bonds characteristics, the bonds are modeled as inductors. From the geometry of the wire-bonds, the

inductances of them were calculated. The measurement points of noise voltages close to the SAFF IC, so the IN, Vref, CLK, and VDD were used as input voltages for the simulation. From the circuit simulation, the noise voltage at internal nodes of the SAFF could be obtained. As shown in Fig. 27, the measured OUT and simulated OUT have a good agreement. With the simulation, the measured soft failures can be validated and analyzed.



(a)



(b)

Fig. 27. SPICE simulation results that show soft failure mechanisms (a) without any VDD-GND decoupling capacitors (b) with four 10uF VDD-GND decoupling capacitors

The measured and simulated node voltages under 8-kV ESD for the two cases without- and with-the decoupling capacitors are shown in Fig. 27 (a) and (b), respectively. The root causes of the soft failure can be analyzed with simulated node voltages of the SAFF IC. The relative voltage relation of the IN and Vref is flipped due to the 8-kV ESD event, and the CLK rising edges' timing is also distorted. As shown in Fig. 27 (a), one CLK is removed due to ESD noise, so node n4(S) and node n5(R) are not discharged. Therefore, the OUT is not refreshed. In Fig. 27 (b), the flipped relation of

the IN and Vref voltage due to ESD is captured by the rising edge of CLK. Therefore, a wrong node would be discharged among n4 (S) and n5 (R) through a wrong current path, which produce a soft failure. The CLK noise and the differential input noise voltage at IN and Vref node have dominant attribution of the system-level ESD-induced soft failures of the SAFF. On the other hand, the common mode noise at the IN and Vref voltage has little effects on the operation of the SAFF IC, as can be expected. Also, because the IN and Vref voltage signals do not pass any inverter buffers which are sensitive to VDD noise, the SAFF has a sufficiently high immunity against the VDD noise. Therefore, the reduction of the VDD noise voltage by utilizing the decoupling capacitors does not result in any further reduction of the SAFF soft failures, as can be seen at Fig. 26 (a). On the other hand, the static flip-flop has a single-ended input signal, which passes through input inverter buffers. The VDD noise voltage due to the ESD critically affects the operation of the input buffers, which produce a high soft failure occurrence ratio, as shown in Fig. 26 (b). After decreasing the VDD noise voltage by the decoupling capacitors, the soft failure ratio of the static flip-flop is drastically decreased.

3.5 Conclusion

The sense amplifier flip-flop, which is commonly used as a command and address receiver of DRAM, was designed in the simplified DIMM and motherboard structures of a laptop. The system-level ESD-induced soft failures were measured under the ESD events of 3-, 5-, and 8-kV. The two test cases without- and with- the VDD-GND decoupling capacitors on the designed DIMM were compared. The experiments were conducted 50 times per each ESD test condition. The noise voltages and the soft failure occurrence ratio of the SAFF IC were measured. The mechanisms of the SAFF's soft failures were investigated by SPICE simulations by using the measured input noise voltages. The SAFF itself has already a high immunity against the common-mode noise of input voltages and VDD noise, compared to the static flip-flop. Therefore, the decoupling capacitors on the DIMM do not provide any further reduction of the SAFF's soft failures occurrence ratio. However, the VDD de-caps should be still necessary for other single-ended circuit blocks in a whole system. They are also needed to decrease the IC self-generated switching noise.

IV. Conclusion and Summary

In this thesis, system-level ESD-induced soft failures of two specific circuits were investigated. One is the delay-locked loop that compensates communication mismatch in the DRAM, and the other is the sense amplifier flip-flop that is commonly used as an input receiver of DRAM. They were fabricated with 180-nm CMOS process and mounted on simplified DIMM by COB and each DIMM was placed on each designed motherboard of a laptop PC. The system-level ESD-induced soft failures were tested under the ESD events of 3, 5, and 8 kV.

First, an analog DLL was tested under six test cases that consist of different number of VDD-GND and Vbias-GND de-caps. In each case, the DLL was tested 40 times to obtain statistical results. The average values of peak-to-peak jitter and jitter duration time of the DLL clock induced by ESD events were obtained from repeated measurements and compared with simulated ones, which were obtained by applying the measured input voltages as SPICE simulation inputs. The correlation between the VDD noise and the jitter of DLL clock were investigated. The stabilization of the VDD voltage by employing VDD de-caps were very effective in reducing the ESD-induced jitter of the DLL clock, while employing a bias de-cap was ambiguous. To discover and validate the root causes of the DLL clock jitter, SPICE simulations were conducted with various conditions. The huge jitter was attributed to the reduced voltage headroom in the delay cells of VCDL due to ESD-induced VDD drop. Also, maintaining the amount of delay control parameter, (VDD-Vbp), was crucial for stable operation of the DLL under ESD events. To analyze the effects of VDD de-caps on the ESD-induced VDD noise, which is critical to jitter, the impedance parameters were extracted from the measurements using a VNA in the frequency domain. The time-domain VDD noise was also reconstructed from the measured Z21 parameter and ESD injection current, which validates the measurements and analysis.

Second, the SAFF was tested under two cases without- and with- the DIMM decoupling capacitors. The experiments were repeated 50 times per each test condition by using contact discharge while the voltages and the soft failure ratio of the SAFF were measured. The mechanism of the SAFF soft failure was investigated by SPICE simulations using the measured input voltages. The SAFF itself has already a high immunity to the common-mode noise of inputs and VDD noise. Thus, the de-caps on the DIMM do not provide a further reduction of the SAFF soft failures. However, the VDD de-caps should be still necessary for other single-ended circuits in the system to reduce IC switching noise.

In summary, the simple circuit blocks such as D-flip-flop and sense amp have only a few temporal logic errors occurred due to the ESD noises. Since a real product IC usually uses error-correcting-code (ECC) circuits, it is hard to believe that only a few data losses cause a fatal system freeze, fault, or reboot. A more long-lasting malfunction of a critical circuit block would cause the system failures. Lots of data losses or soft failures can occur due to the DLL jitter induced by system-level ESD even though the DLL does not lose the locked condition.

REFERENCES

[1] Industry Council on ESD Target Levels, White Paper 3: System Level ESD, Part II: “Implementation of Effective ESD Robust Designs”, Sept. 2012.

[2] Electromagnetic Compatibility (EMC)—Part 4-2: Testing and Measurement Techniques—Electrostatic Discharge Immunity Test, IEC Standard 61000-4-2 Ed. 2.0, Dec. 19, 2008.

[3] Y. Xiu, S. Sagan, A. Battini, X. Ma, M. Raginsky and E. Rosenbaum, "Stochastic modeling of air electrostatic discharge parameters," 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, 2018, pp. 2C.2-1-2C.2-10.

[4] S. Yang and D. J. Pommerenke, "Effect of Different Load Impedances on ESD Generators and ESD Generator SPICE Models," in IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 6, pp. 1726-1733, Dec. 2018.

[5] ESD simulator DITO, EM test, [Online]. Available: https://www.emtest.com/products/product/135120100000010183.php. [Accessed May. 6. 2019].

[6] G. Lu, Y. Wang, Y. Wang and X. Zhang, "Insights Into the Power-Off and Power-On Transient Performance of Power-Rail ESD Clamp Circuits," IEEE Transactions on Device and Materials Reliability, vol. 17, no. 3, pp. 577-584, Sept. 2017.

[7] F. Escudié, F. Caignet and N. Nolhier, "LIN communication behaviours against ESD events," 2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE, Angers, 2017, pp. 1-6.

[8] T. Ostermann, "Usage of ESD detector circuit for analyzing soft failures in IC cores," 2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI), Brest, 2018, pp. 1-4.

[9] S. Marathe, G. Maghlakelidze, H. Rezaei, D. Pommerenke and M. Hertz, "Software-Assisted Detection Methods for Secondary ESD Discharge During IEC 61000-4-2 Testing," IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 4, pp. 1129-1136, Aug. 2018.

[10] J. Park, J. Lee, C. Jo, B. Seol and J. Kim, "A Cost-Effective Structure for Secondary Discharge Control to Improve System-Level ESD Immunity of a Mobile Product," IEEE Transactions on Electromagnetic Compatibility.

[11] A. Hosseinbeig, O. H. Izadi, S. Shinde, D. Pommerenke, H. Shumiya, J. Maeshima and K. Araki, "A study on correlation between near-field EMI scan and ESD susceptibility of ICs," 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI), Washington, DC, 2017, pp. 169-174.

[12] P. Wei, J. Meiguni and D. Pommerenke, "System-level design for ESD protection on multiple IO interfaces," 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, 2018, pp. 2C.1-1-2C.1-8.

[13] J. Zhou, K. Ghosh, S. Xiang, X. Yan, A. Hosseinbeig, J. Lee and D. Pommerenke, "Characterization of ESD Risk for Wearable Devices," IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 5, pp. 1313-1321, Oct. 2018.

[14] J. Park, J. Lee, C. Jo, B. Seol and J. Kim, "A Proto-type ESD Generator for System Immunity Test of Wearable Devices," 2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Reno, NV, 2018, pp. 1-6.

[15] X. Liu, O. H. Izadi, G. Maghlakelidze, M. Pommerenke and D. Pommerenke, "A Preliminary Study of ESD Effects on the Process Calls Tree of a Wireless Router," 2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI), Long Beach, CA, 2018, pp. 408-413.

[16] A. Hosseinbeig, O. H. Izadi, S. Solanki, T. D. Lingayat, B. P. Subramanya, A. K. Vaidhyanathan, J. Zhou and D. Pommerenke, "Methodology for Analyzing ESD-Induced Soft Failure Using Full-Wave Simulation and Measurement," IEEE Transactions on Electromagnetic Compatibility, vol. 61, no. 1, pp. 11-19, Feb. 2019.

[17] K. H. Kim and Y. Kim, “Systematic Analysis Methodology for Mobile Phone's Electrostatic Discharge Soft Failures”, IEEE Trans. Electromagn. Compat., vol. 53, no. 3, pp. 611-618, Aug. 2011.

[18] S. Vora, R. Jiang, S. Vasudevan and E. Rosenbaum, “Application level investigation of system-level ESD-induced soft failures”, EOS/ESD 2016, pp. 1-10.

[19] O. H. Izadi, A. Hosseinbeig, D. Pommerenke, H. Shumiya, J. Maeshima and K. Araki, "Systematic analysis of ESD-induced soft-failures as a function of operating conditions," 2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC), Singapore, 2018, pp. 286-291.

[20] A. Patnaik, W. Zhang, R. Hua, L. Chuang, A. Huang, H. Lin, B. Tseng and D. Pommerenke , "Systematic Evaluation of Soft Failures in System-Level ESD Transient Events," IEEE Transactions on Electromagnetic Compatibility, vol. 60, no. 5, pp. 1263-1269, Oct. 2018.

[21] S. Koch, B. J. Orr, H. Gossner, H. A. Gieser and L. Maurer, "Identification of Soft Failure Mechanisms Triggered by ESD Stress on a Powered USB 3.0 Interface," IEEE Transactions on Electromagnetic Compatibility, vol. 61, no. 1, pp. 20-28, Feb. 2019.

[22] T. Ostermann, "ESD induced EMS problems in digital IOs," 2017 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Linkoping, 2017, pp. 1-6.

[23] D. J. Rennie and M. Sachdev, "Novel Soft Error Robust Flip-Flops in 65nm CMOS," in IEEE Transactions on Nuclear Science, vol. 58, no. 5, pp. 2470-2476, Oct. 2011.

[24] G. Shen, S. Yang, V. V. Khilkevich, D. J. Pommerenke, H. L. Aichele, D. R. Eichel and C.

Keller, "ESD Immunity Prediction of D Flip-Flop in the ISO 10605 Standard Using a Behavioral Modeling Methodology," in IEEE Transactions on Electromagnetic Compatibility, vol. 57, no. 4, pp. 651-659, Aug. 2015.

[25] M. Park, J. Park, J. Choi, J. Kim, S. Jeong, M. Seung, S. Lee and J. Kim, "Measurement and Analysis of Statistical IC Operation Errors in a Memory Module Due to System-Level ESD Noise," IEEE Transactions on Electromagnetic Compatibility, vol. 61, no. 1, pp. 29-39, Feb. 2019.

[26] M. Jeong, J. Park, J. Kim, M. Seung, S. Lee and J. Kim, "Measurement and Analysis of System-level ESD-induced Soft Failures of a Sense Amplifier Flip-Flop with Pseudo Differential Inputs," 2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), Reno, NV, 2018, pp. 1-5.

[27] Hyun-Woo Lee and Chulwoo Kim, “Survey and analysis of delay-locked loops used in DRAM interfaces”, IEEE Transactions on VLSI Systems, vol. 22, no. 4, pp. 701-711, Apr. 2014.

[28] C. Hwang, J. Kim, B. Achkir and J. Fan, "Analytical Transfer Functions Relating Power and Ground Voltage Fluctuations to Jitter at a Single-Ended Full-Swing Buffer," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 3, no. 1, pp. 113-125, Jan. 2013.

[29] J. G. Maneatis and M. A Horowitz, “Precise delay generation using coupled oscillators”, IEEE Journal of Solid-State Circuits, vol. 28, no. 12, pp. 1273-1282, Dec. 1993.

[30] S. Sidiropoulos and M. A. Horowitz, "A semidigital dual delay-locked loop," IEEE Journal of Solid-State Circuits, vol. 32, no. 11, pp. 1683-1692, Nov. 1997.

[31] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1723-1732, Nov. 1996.

[32] H. O. Johansson, "A simple precharged CMOS phase frequency detector," IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 295-299, Feb. 1998.

[33] M. Park, J. Park, M. Seung, J. Choi, C. Lee, S. Lee and J. Kim, "Measurement and modeling of system-level ESD noise voltages in real mobile products," 2016 Asia-Pacific International Symposium on Electromagnetic Compatibility, Shenzhen, 2016, pp. 632-634.

[34] F. Moradi, C. Augustine, A. Goel, G. Karakonstantis, T. V. Cao, D. Wisland, H. Mahmoodi and K. Roy, “Data-dependant sense-amplifier flip-flop for low power applications”, IEEE CICC 2010, pp. 1-4.

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