Aalto University

School of Science

Master's Programme in Advanced Materials for Innovation and Sustainability

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Optimization of materials for microelectronics industry by in-situ coupling of electrical and structural characterization techniques

Master's Thesis

Grenoble, August 12, 2019

Supervisor: Docent Janne Halme

Advisor: Patrice Gergaud, Research engineer, CEA

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ABSTRACT OF MASTER’S THESIS

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In microelectronics industry, one way to improve MOSFET performances is to reduce the gate “propagation” delay, i.e. the time between input and output signal in a transistor, by reducing the contact resistance between the Source/Gate/Drain and the metallic layer. These contacts are obtained by solid-state reaction of a metallic film with the Si substrate. The thermodynamics involved in these reactions are complex, especially for thin films. Thus, for a better understanding of these reactions driving forces, it is important to have a tool that enables the correlation of structural and electrical (here sheet resistance) properties during the formation of these contacts.

The aim of this study is to build a setup that allows the optimization of materials for microelectronics industry by in-situ coupling of electrical (4 points probe method for sheet resistance measurement) and structural (XRD/XRR/Raman spectroscopy) characterization techniques and then to apply and validate the performances, capabilities, limitations of our setup with different materials…

The setup consists on a heating stage that plays the role of a sample holder in a diffractometer/spectrometer while 4 tungsten based points’ probes are positioned on the sample surface and measures its sheet resistance. Both the Temperature Control Unit (TCU) and the SourceMeter are remotely controlled using a python script that reads and writes the TCU temperature and Ramp Rate (RR), and sources current and senses voltage using the SourceMeter.

Various materials that are used in STMicroelectronics high technology chips were characterized using this setup e.g. Ni(Pt), Vanadium, ITO… with a high focus on silicides. This study aims to correlate the evolution of materials electrical and structural properties driven by physical mechanisms investigated in literature review.

First, Ni(Pt) is studied. The in-situ coupling of XRD and sheet resistance measurement showed that the sheet resistance suddenly decreases at ~265°C. It corresponds to the Ni to NiSi phase transition temperature. A Raman spectroscopy analysis performed on a sample that was annealed at this temperature showed also the formation of the Ni_2Si phase, and an XRR analysis showed that this phase possibly nucleates as an interlayer in the Ni/Si interface instead of clusters inside the Ni matrix. The Kissinger method, that estimates the activation energy of the Ni to NiSi phase transition using constant ramp rate annealing, was, for the first time, enabled in our laboratory.

Measurements were performed in air atmosphere because a TiN capping layer was deposited to prevent thermal oxidation issues. The effect of alloying, i.e. metal incorporation in small quantities in the nickel layer, e.g. 10%at Pt, on sheet resistance evolution were investigated. It was shown, using an isothermal annealing, slightly above the phase transition temperature, that the amount of Pt in the Ni remaining layer increases.

Second, Vanadium thin film was also investigated. This material is very sensitive to oxidation. We showed that even with a TiN capping layer, undesired oxidation issues were observed. To check that point, we tried on another sheet resistance measurement setup (not compatible with XRD or Raman spectroscopy) but working in vacuum/inert gas heating chamber.

We can conclude from this study that a specific setup/furnace should be used for further studies, e.g. the effect of various inert gas annealing on microstructure.

Keywords: Silicides, MOSFET, electrical characterization, structural characterization
Language: English

List of symbols and abbreviations

CEA: Commissariat à l'Energie Atomique et aux Energies Alternatives

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

CMOS: Complementary Metal Oxide Semiconductor

XRD: X-rays Diffraction

XRR: X-rays Reflectivity

ITO: Indium Tin Oxide

GST: Germanium-Antimony-Tellurium

EHF: Effective Heat of Formation

BB: Bragg-Brentano geometry

PDF: Powder Diffraction File

F-S: Fuchs-Sondheimer

M-S: Mayadas-Shatkez

MFP: Mean Free Path

GB: Grain Boundary

DHS: Domed Hot Stage

TCU: Temperature Control Unit

HFS: Heating/Freezing Stage

SCPI: Standard Command for Programmable Instruments

GPIB: General Purpose Interface Bus

Bisync: Binary Synchronous Communication

RS: Recommended Standards

FWHM: Full Width at Half Maximum

PAI: Pre-Amorphisation Implant

TCE: Transparent Conductive Electrode

SOI: Silicon On Insulator

RR: Ramp Rate

FFT: Fast Fourier Transform

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Chapter 1

Introduction

As part for MOSFET manufacturing, silicidation is a process that consists on a thermally activated solid state reaction between silicon substrate and a metallic layer. This reaction forms a binary compound M_xSi_y commonly named "silicide". Microelectronics industry has been improving, for many years, chips performances by lowering the contact resistance of these silicides.

It is highly important to investigate the physical mechanisms involved in silicides formation. In a thermodynamics and kinetics point of view, nucleation & growth and diffusion are the two phenomena that drives this type of solid state reactions, and the theory behind is discussed in accordance with literature.

In order to accelerate the optimization process of materials for microelectronics industry, it is important to enable the correlation of electrical properties and microstructural characteristics of materials according to their usage and elaboration conditions.

My work has been focused on in-situ coupling of XRD/XRR/Raman spectroscopy structural characterization techniques and sheet resistance measurement (4 points probe method) electrical characterization technique. The idea is to use both characterization techniques as a complementary tools to investigate the effect of microstructural phenomena e.g. phase transformation, grain growth, thermal expansion… on sheet resistance evolution. The theory behind is discussed in literature review.

In order to make this in-situ coupling possible, a "homemade" setup was built. It consists on a heating stage that plays the role of a sample holder in a diffractometer/spectrometer while 4 tungsten based points' probes are positioned on the sample surface and measures its sheet resistance. Both the Temperature Control Unit (TCU) and the SourceMeter are remotely controlled using a python script that reads and writes the TCU temperature and Ramp Rate (RR), and sources current and senses voltage using the SourceMeter.

Put into the general context, the aims of the master thesis are therefore:

- Build a "homemade" setup of thin films in-situ structural and electrical characterization for a wide range of temperature.
- Validate the setup by performing the first experiments on widely studied materials, e.g. nickel silicide, and compare the results with literature.
- Study thin film materials that are highly relevant for microelectronics industry, with a high focus on silicides:
  - Nickel Silicide is used as a contact material in CMOS technology, mainly for its low resistivity and high thermal stability.
  - Vanadium Silicide is a superconducting material that has a high potential in quantum computing applications, due to its high critical temperature.

This thesis is organized as fellows, Chapter 2 is a literature review of the physical background behind solid state reaction of silicides, as part of MOSFETs manufacturing process, and the effect of silicide microstructure on sheet resistance evolution. In Chapter 3, the working principle of each characterization technique that is involved in this study is explained, and how the in-situ coupling is enabled by the instrumentation and programming. Chapter 4 is dedicated to results and discussion of the listed materials study, and raises related challenges and how to overcome them.

Chapter 2

Literature review

The topic of this study is fully related to materials for microelectronics industry. Thus, it is highly important to have enough understanding of these materials usage, characterization, properties… This chapter is dedicated to investigating the theory behind the physical mechanisms involved in solid state reaction while silicide formation, as part of MOSFETs manufacturing process, and the effect of silicide microstructure on sheet resistance evolution.

The process of silicide formation involves the reaction of a thin metallic film with silicon through annealing. This process is named "salicidation", and it refers to self-aligned silicidation. When a metallic layer is deposited on a silicon substrate, a metal/silicon interface is created and a thermally activated solid state reaction occurs upon annealing. Salicidation process is shown in Figure 2.1. As reported previously, silicide is used as a contact material between the Source/Gate/Drain and the metallic layer. In MOSFET technology, the gate role is to regulate the electrons flow between the source and the drain by applying a current that creates charge carriers.

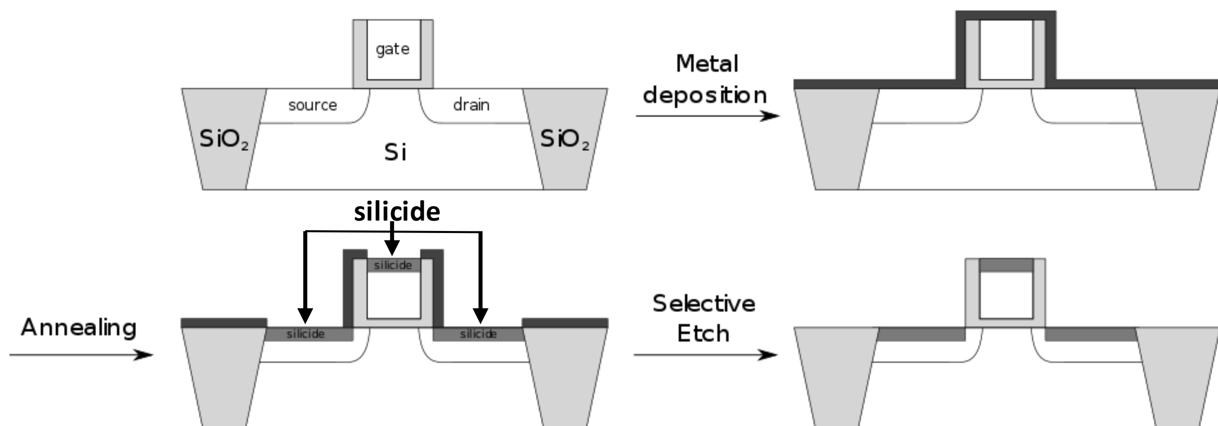


Figure 2.1: Salicidation process [18]

Upon annealing, physical mechanisms that drives solid state reaction in silicide are multiple and complex. In the following, I introduce reactions that are driven by the two main and well understood phenomena: diffusion and nucleation & growth.

As my work focuses on silicides, thin film materials that are highly relevant for microelectronics industry were studied:

- Nickel Silicide is used as a contact material in CMOS technology, mainly for its low resistivity and high thermal stability.
- Vanadium Silicide is a superconducting material that has a high potential in quantum computing applications, due to its high critical temperature.

Nucleation and growth

In thermodynamics, we call nucleation and growth the transformation of a homogeneous phase to a mixture of two phases. Let's consider two pure compounds M and Si. If we put M and Si in contact and start heating, an intermetallic binary compound M_xSi_y is formed. Its nucleation occurs first followed by its growth.

The driving force of a phase transformation is quantified by the change in Gibbs free energy ΔG (J) in equation (2.1) [19].

$$\Delta G = \Delta H - T\Delta S \tag{2.1}$$

ΔH: standard heat of formation

T: temperature

ΔS: change in entropy associated with the phase transformation

Since the change in entropy ΔS is small in solid-state phase transitions, ΔH is almost equal to ΔG.

Moreover, the change in Gibbs free energy associated with the creation of a nuclei has surface and volume contributions, and the equation becomes (2.2) [19].

$$\Delta G = (\Delta g_v + \Delta g_{el})V + \Upsilon A \tag{2.2}$$

Δg_v: chemical driving force in J/m^3 (> 0), makes the transformation possible

Δg_{el}: elastic energy in J/m^3 (< 0), cost of forcing a nuclei of volume $(1+\varepsilon)V$ in a cavity of volume V

Υ: interfacial energy in J/m^2, depends on the phase shape and nature of interface

If we suppose that the cluster formed has spherical shape, the change in free energy becomes (2.3) [19].

$$\Delta G(R) = \frac{4}{3}\pi R^3(\Delta g_v + \Delta g_{el}) + 4\pi R^2 \Upsilon \tag{2.3}$$

Thus, from $\frac{d\Delta G}{dR} = 0$, one can derive the limit of stability or the activation barrier ΔG^* (2.4) [19] i.e. the energy that has to be provided to create a cluster of critical radius R^* (2.5) [19] from the solid solution.

$$\Delta G^* = \frac{16\pi}{3}\frac{\Upsilon^3}{(\Delta g_v + \Delta g_{el})^2} \tag{2.4}$$

$$R^* = -\frac{2\Upsilon}{\Delta g_v + \Delta g_{el}} \tag{2.5}$$

With the ΔG^* value, one can estimate the growth rate J (2.6) [19], i.e. number of new clusters per unit time and per unit volume in m^{-3}s^{-1}, which is proportional to the probability to pass the activation barrier.

$$J \; \alpha \; exp(-\frac{\Delta G *}{kT}) \tag{2.6}$$

We see later in the text, how to estimate the activation barrier of a phase transition, also called "Activation energy (E_A)", with the Kissinger method, and its effect on the phase microstructure.

Diffusion

In solid-state phase transitions, diffusion is a term used in chemical kinetics and means that atoms are in movement in the material, from a high concentration to a low concentration region.

While moving, atoms can occupy two types of crystal sites: interstitial and substitutional, as illustrated in Figure 2.2. Interstitial mechanism is due to the jump of atoms from an “in between” site to another while substitutional is the occupation of an “empty” site i.e. vacancy by an atom.

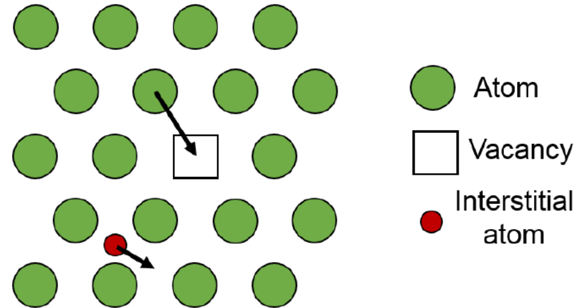


Figure 2.2: Interstitial and vacancy mechanisms [7]

First phase formation and sequential growth

Now that we have understood the physical mechanisms behind solid-state reaction in silicides, let's go deeper and see which phases forms during silicide annealing. In general, a sequential M_xSi_y phases' formation is observed, from M-rich to Si-rich phase. A prediction of the first phase to form and the sequential growth is enabled by the Effective Heat of Formation (EHF) model [1]. Based on a recalculation of the standard enthalpy of formation *ΔH* that takes into account the atomic ratio at the metal/silicon interface as derived in equation (2.7) [1], this model sequences the formation of the binary compounds that are discernable in the M-Si phase diagram. In practice, only the formation of congruent phases occurs, i.e. phases, when melted, forms a liquid of the same composition.

$$\Delta H'_{eff} = \Delta H^0 \frac{effective\ concentration\ limiting\ element}{compound\ concentration\ limiting\ element} \tag{2.7}$$

In the Ni-Si phase diagram, among all its phases, NiSi is the silicide that is targeted in CMOS technology, mainly for its low resistivity, as shown in column 2 of Table 2.1.

	Electrical resistivity ($\mu\Omega\,cm$)	Mass density ($g\,cm^{-3}$)	Electron density (nm^{-3})
Ni	7	8.91	2500
Ni_2Si	27	7.51	2140
NiSi	17	5.97	1750
$NiSi_2$	40	4.8	1410

Table 2.1: Nickel silicides and respective resistivity values [8]

As an example, a plot of $\Delta H'_{eff}$ versus the concentration gives the typical EHF diagram for the Ni-Si system as shown in Figure 2.3.

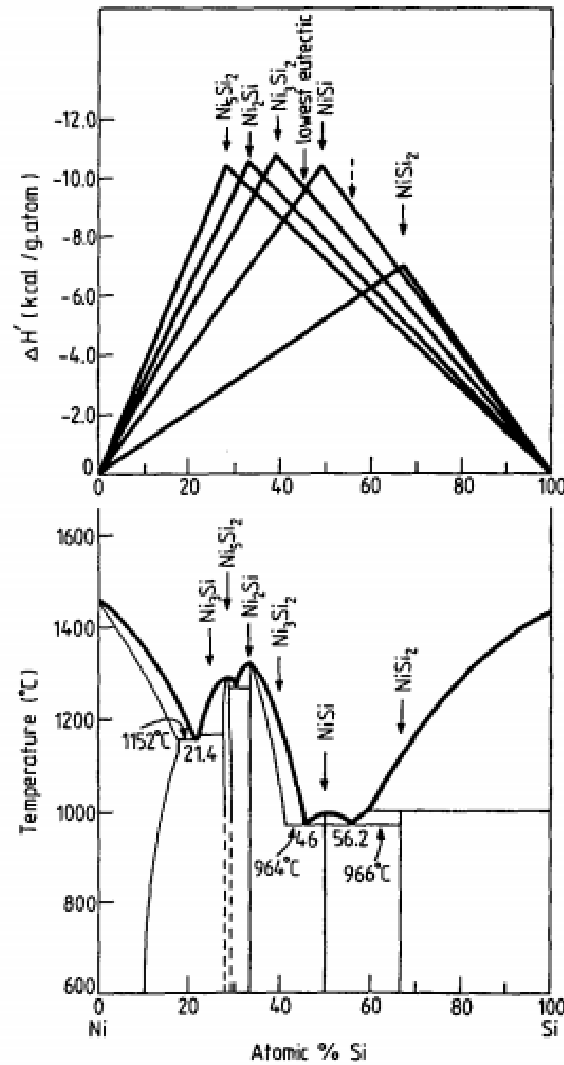


Figure 2.3: Effective Heat of Formation (EHF) diagram for Ni-Si system [1]

In this study as well as in other scientific articles [3][5][12], it has been shown with in-situ XRD, i.e. XRD analysis while heating the sample, that the first phase to form is a Ni-rich phase and the sequential growth is as following in column 1 of Table 2.2. It column 2, we can see that the more we heat, the more Si diffuses in Ni, which explains the increase of Si composition in the phase sequence.

Phase	Si composition (at.%)	Crystal	Space Group
Ni	0	Face-Centered Cubic	Fm3m
δ-Ni_2Si	33	Orthorhombic	Pnma
θ-Ni_2Si	33-42	Hexagonal	$P6_3/mmc$
NiSi	50	Orthorhombic	Pnma
α-$NiSi_2$	66	Face-Centered Cubic	Fm3m
Si	1	Face-Centered Cubic	Fd3m

Table 2.2: Sequential growth of Ni-Si system [7]

Microstructure and electrical conductivity

From the compromise between low activation enegy and low resistivity, it is now obvious that microstructure plays a key role in MOSFET performances' optimization. We see in this part the definition of electrical resistivity and the models that shows the effect of microstructure on its value.

Electrical conductivity σ (S/m) defines the ability of materials to transport electricity. Electrical resistivity ρ (Ωm) is its reciprocal (2.8) [20].

$$\sigma = \frac{1}{\rho} \tag{2.8}$$

A generalisation of Ohm's law in materials science uses electrical conductivity as following (2.9) [20]:

$$J = \sigma E \tag{2.9}$$

J: Current density at a given location in a resistive material.

E: Electric field at that location.

Electrical conductivity is driven by carriers density and mobility (2.10) [20]:

$$\sigma = en\mu \tag{2.10}$$

e: Elementary charge.

n: Carriers density.

μ: Carriers mobility.

Electrical resistance R is derived from resistivity by considering geometry as following (2.11) [20]:

$$R = \rho \frac{l}{A} \tag{2.11}$$

l: length of the conductor in m

A: cross-sectional area of the conductor in m^2

In microelectronics industry, sheet resistance (R_s) in Ω/sq (2.12) [20] is used to measure the resistivity of conductive thin films:

$$R_s = \frac{\rho}{t} \tag{2.12}$$

t: Film thickness

The film thickness, as well as other film characteristics, plays a role in sheet resistance evolution, which can be increased by increasing the electron scattering i.e. lowering the electrons Mean Free Path (MFP). Electron scattering is due to any local breaking of the crystal potential periodicity.

The crystal periodicity can be broken either by phonons (atoms vibration around a fixed position due to heating) or local crystal defects (Grain Boundaries (GB), dislocations, surfaces, interfaces…).

In the case of thin films, two models describe how electron scattering due to microstructure Mayadas-Shatkez (M-S) (2.13) [20] and surface Fuchs-Sondheimer (F-S) (2.14) [20] influences resistivity:

Mayadas-Shatkez (M-S):

$$\frac{\rho}{\rho_{Bulk}} \sim 1 + 1.33 * \frac{\lambda_{Bulk}}{d} \left(\frac{R}{1-R}\right) \tag{2.13}$$

P_{Bulk}: resistivity of bulk single crystal

d: mean grain size

λ_{Bulk}: MFP in bulk single crystal

R: probability of reflection at GB ~ 0.5

Fuchs-Sondheimer (F-S):

$$\frac{\rho}{\rho_{Bulk}} \sim 1 + \frac{3\lambda_{Bulk}}{8t}(1-p) \tag{2.14}$$

P_{Bulk}: resistivity of bulk single crystal

t: film thickness

λ_{Bulk}: MFP in bulk single crystal

p: fraction of specular surface collision ~ 0.4

Finally the total resistivity is the sum of all the contributions (2.15) [20]:

$$\rho = \rho_{impurities} + \rho_{defects} + \rho_{temperature} + \cdots \tag{2.15}$$

Among the benefits of in-situ coupling of XRD and sheet resistance measurement, The Full Width at Half Maximum (FWHM) of an XRD peak is an interesting data because it enables the estimation of the mean grain size of a certain phase through Scherrer equation (2.16) [33]. The evolution of the grain mean size with the annealing temperature explains the effect of microstructure on electrons mean free path λ_{mfp} i.e. scattering with grain boundaries. Scherrer equation is limited to nano-scale particles (< 0.1 µm).

$$\tau = \frac{K\lambda}{\beta\cos(\theta)} \tag{2.16}$$

τ: mean grain size

K: shape factor ~ 0.9

λ: X-ray wavelength 1.5418 Å

β: Full Width at Half Maximum (FWHM)

ϑ: Bragg angle

The dependance of sheet resistance on materials microstructure highlights the interest of in-situ coupling of electrical and structural characterization techniques. The idea is to use both characterization techniques as a complementary tools to investigate the effect of microstructural phenomena e.g. phase transformation, grain growth, thermal expansion… on sheet resistance evolution, in accordance with the physical mechanisms discussed previously. To illustrate the complementarity of these techniques, since XRD only shows the formation of crystalline phases, it is possible to use Raman spectroscopy to investigate the formation of amorphous ones, if any.

To summerize this part, electrical resistvity of a certain phase is highly dependent on its microstructure. In chapter 3 and 4, we see how to investigate the microstructure of various thin film materials using structural characterization techniques, and correlate the results with sheet resistance evolution. As it is mentioned earlier, the material of interest for contacts in CMOS technology is Nickel Silicide.

Chapter 3

Experimental techniques

In this chapter, I explain the working principle of each characterization technique that is involved in this study, and how the in-situ coupling is enabled by the instrumentation and programming.

In order to make this in-situ coupling possible, a "homemade" setup was built. It consists on a heating stage that plays the role of a sample holder in a diffractometer/spectrometer while 4 tungsten based points' probes are positioned on the sample surface and measures its sheet resistance. Both the Temperature Control Unit (TCU) and the SourceMeter are remotely controlled using a python script that reads and writes the TCU temperature and Ramp Rate (RR), and sources current and senses voltage using the SourceMeter.

Structural characterization

The term "structural characterization" gathers in a broad way all the techniques by which the structure of a material is investigated. This study only focuses on X-Rays Diffraction (XRD), X-Rays Reflectivity (XRR) and Raman spectroscopy. The working principle of each technique is briefly explained in the following.

X-Rays Diffraction (XRD)

A monochromatic incident beam (light) arrives on a sample. This wave is scattered by the atoms and a diffraction peak is obtained. XRD principle is shown in Figure 3.1.

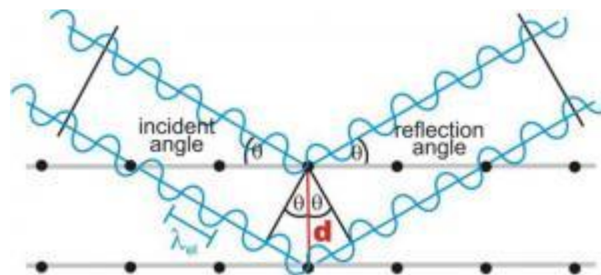


Figure 3.1: XRD principle [21]

The constructive interferences i.e. diffraction peak are observed only if Bragg's law (3.1) [21] is satisfied:

$$2dsin(\theta) = n\lambda \quad (3.1)$$

d: interplanar spacing

ϑ: incidence angle

n: diffraction order

λ: wavelength

The most used geometry in diffractometers is the symmetrical ϑ-2ϑ or Bragg-Brentano (BB) configuration as shown in Figure 3.2. It offers high resolution and high beam intensity analysis. Its drawbacks are the need for very precise alignment and well prepared samples.

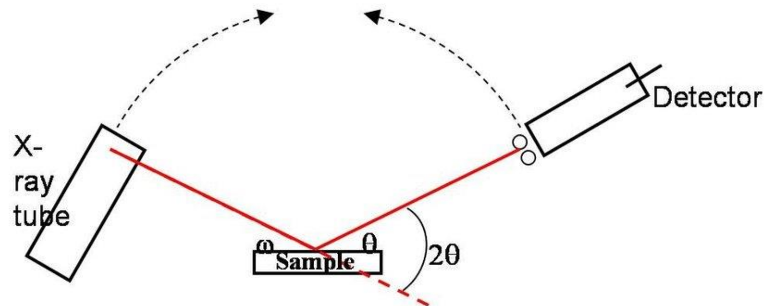


Figure 3.2: Bragg-Brentano geometry [22]

The result of an XRD scan is a diffractogram i.e. intensity vs. 2ϑ plot that represents a certain number of peaks corresponding to the family of planes of the crystalline phases contained in the material. A family of planes has 3 indices (hkl) called Miller indices e.g. Ni(111).

These peaks can be fitted and compared with the Powder Diffraction File (PDF) cards, e.g. Ni 01-077-9326, to investigate which materials/phases are contained in the sample.

One of the main goals of this master thesis is to perform an in-situ XRD analysis to observe peaks intensity, position and Full Width at Half Maximum (FWHM) evolution during annealing. It is a way to investigate phase transformations in solid state materials. The peak broadening enables to estimate the mean grain size through Scherrer equation (2.17) [33], and the area under the peak is related to the volume of diffracting grains for a specific phase, assuming no texture evolution into the material.

X-Rays Reflectivity (XRR)

As in XRD, the sample is exposed to a monochromatic X-Rays source. In the configuration in Figure 3.3, light is coming in at a very small incident angle (also called grazing angle) $\vartheta > \vartheta_c$, where ϑ_c is the critical angle under which all X-Rays are reflected.

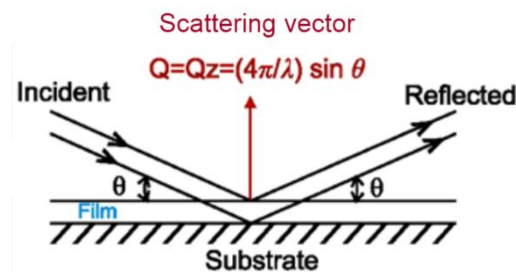


Figure 3.3: XRR principle [23]

As Bragg's law in XRD, an equivalent equation (3.2) [24] can be used in XRR to derive the layer thickness.

$$2t\sin(\theta) = n\lambda \tag{3.2}$$

t: layer thickness.

X-rays are then partially reflected at each interface and has constructive interferences that creates a reflectometry pattern as in Figure 3.4 i.e. reflected intensity versus reflection angle ϑ (or scattering vector Q) plot. XRR determines accurately film thickness through the interferences (also called Kiessig fringes) that presents periodic oscillations.

Three main information can be extracted from XRR:

- Thickness of thin films and multi layers through oscillation period.
- Surface and interface roughness through the trend slope of the plot.
- Surface density gradients and layer density through the critical angle ϑ_c, where ϑ_c is the critical angle under which all X-Rays are reflected.

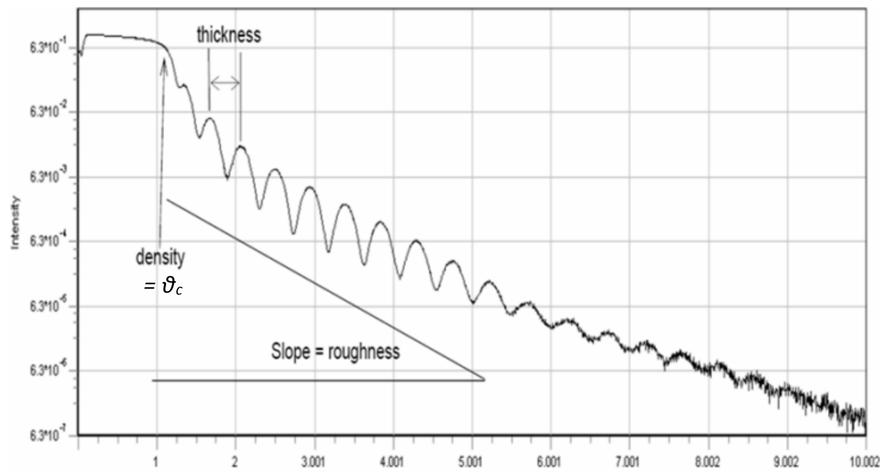


Figure 3.4: Interferences pattern provided by XRR [24]

Raman spectroscopy

Raman spectroscopy is a non-destructive characterization technique that enables a deeper investigation of the presence of a molecule in the material. A molecule can be identified by its vibrational mode.

In Figure 3.5, the sample is exposed to a monochromatic laser beam. Inelastically scattered light is analyzed by detector and the intensity difference between the incident and the scattered wave gives information about the presence of a certain molecule.

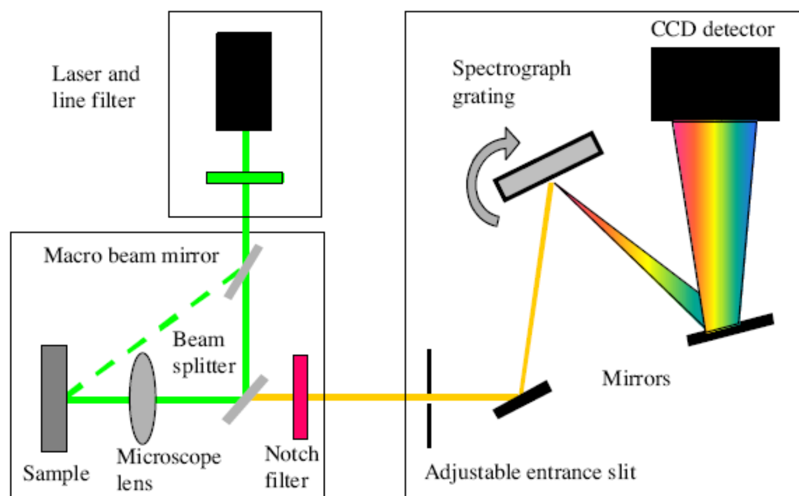


Figure 3.5: Principle of Raman spectroscopy technique [25]

The "Notch filter" only collects the Raman scattered light i.e. inelastic wave, also called Stockes light.

The difference or the Raman shift (Δv in cm^{-1}) is expressed as wavenumber in equation (3.3) [26]:

$$\Delta v = \frac{1}{\lambda 0} - \frac{1}{\lambda} \tag{3.3}$$

λ_0: excitation wavelength

λ: Raman spectrum wavelength

Wavenumber is directly related to energy (E) through wavelength (λ) by Planck-Einstein relation (3.4) [26]:

$$E = \frac{hc}{\lambda} \tag{3.4}$$

h: Planck constant

c: speed of light in vacuum

To remind, all these structural characterization techniques are aimed to be performed on a sample that is annealed by a heating stage while a 4 points probe tip measures its sheet resistance. Which brings us to the electrical characterization technique part.

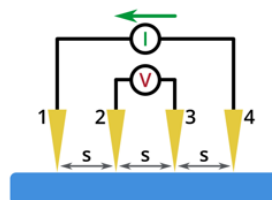
Electrical characterization

Structural properties has multiple effects on the electrical behavious of a thin film material, including sheet resistance (R_s), which can be measured by the 4 points probe electrical characterization technique.

Sheet resistance measurement using the 4 points probe method is shown in Figure 3.6. It consists on sourcing current (I) by the two outer probes and sensing voltage (V) by the two inner ones. The sheet resistance is calculated using equation (3.5) [28]. In order to minimize measurement errors, the distance between the probes should be small compared to the sample dimensions and the probes should not be positioned close to the sample borders [15].

$$R_s = k\frac{V}{I} \tag{3.5}$$

k: correction factor that depends on the distance between the points and the thickness of the film.



SOURCE: Current (I) between 1 & 4

SENS: Voltage (U) between 2 & 3

=> Rs = f(U/I)

Figure 3.6: the 4 points probe method [28]

The influence of the correction factor (*k*) on sheet resistance measurement validity was investigated by Albers and Berkowitz [36]. The dependence of the correction factor on the distance between the points and the thickness of the film is estimated by equation (3.6) [36].

$$k = \frac{ln(2)}{ln\left(\frac{sinh(\frac{t}{s})}{sinh(\frac{t}{2s})}\right)} \tag{3.6}$$

t: film thickness

s: distance between the probes

The correction factor (*k*) curve is plotted versus the film thickness to the distance between the probes ratio (*t/s*) in Figure 3.7. One can conclude that measurements are valid as long as *t* << *s*.

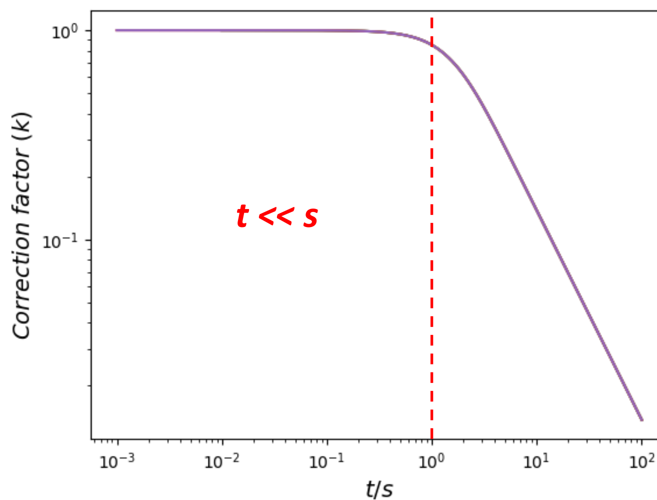


Figure 3.7: correction factor versus film thickness to the distance between the probes ratio

In addition to the linear 4 points probe method, sheet resistance measurement is also possible using square four probes, Van der Pauw and linear Van Der Pauw methods [15]. Each one has its advantages and drawbacks but it seems from Figure 3.8 that the linear 4 probes is the most suitable for this study because it has a good compromise between standard error and sensitivity when the probes alignment and equidistance are verified.

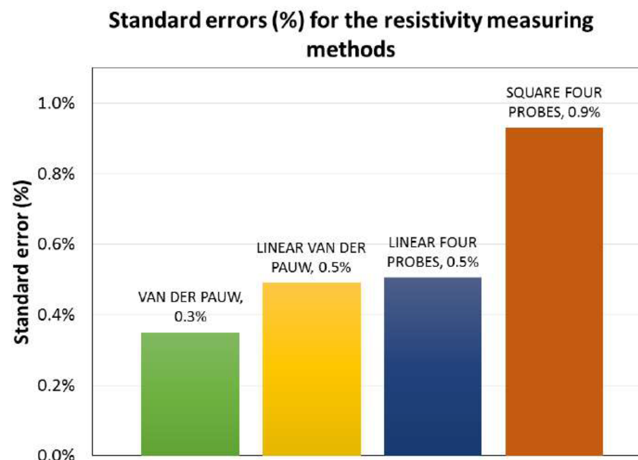


Figure 3.8: Standard error of 4 points probe techniques [15]

Now that all the characterization techniques were exposed, the aim is to couple the 4 points probe and XRD/XRR/Raman spectroscopy using the instrumentation available in the laboratory. In the next paragraph, we see which equipment were used and how the “homemade” setup was implemented.

Instrumentation and Programming

Our setup, in Figure 3.9, consists on an Anton Paar DHS 1100 heating stage and its Eurotherm 2600 Temperature Unit Control (TCU). It enables to perform measurements in vacuum/inert gas atmosphere by adding a dome that closes the heating stage, but makes impossible to position the probes.

Figure 3.9: a) Anton Paar DHS 1100 heating stage and b) Eurotherm 2600 TCU [29][30]

4 tungsten based points’ probes are positioned on the heating stage, as shown in Figure 3.10, where the sample is annealed. In Figure 3.11 it seems that the larger the distance between the probes, the deeper the current penetrates into the film. Thus, the sheet resistance value may also has a substrate contribution. Since the dome is impossible to be added, the sheet resistance measurements were performed in air atmosphere.

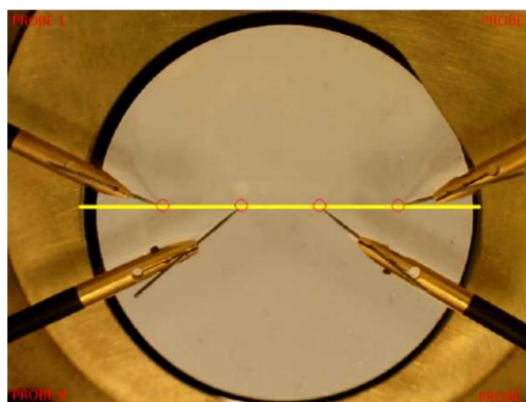


Figure 3.10: 4 points probe on the heating stage [15]

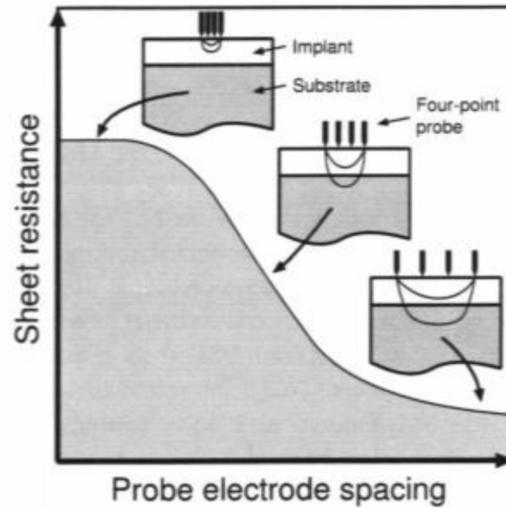


Figure 3.11: current penetration in the film as a function of the distance between the probes [37]

The probes wires are then plugged as shown in Figure 3.6 to a Keithley 2410 SourceMeter that sources current (*I*) and measures voltage (*V*) using a python script. This equipment is connected to the computer GPIB port and needs to be programmed using the Standard Commands for Programmable Instruments (SCPI) [9]. A *V*(*I*) curve is plotted as shown in Figure 3.12 and the sheet resistance value is extracted from its slope. The measured *V*(*I*) data are fitted by a polynomial of degree 1 and an absolute error is calculated to make sure that the sample has an ohmic behavior i.e. the *V*(*I*) curve is a straight line (absolute error = 0).

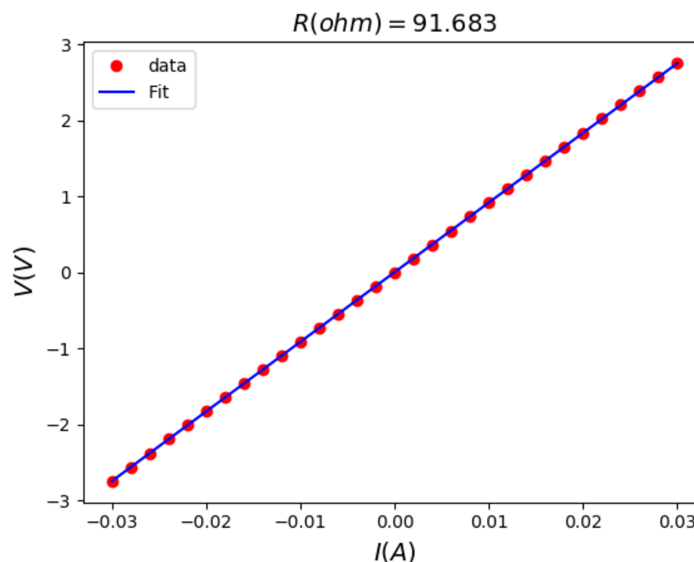


Figure 3.12: Applied current (*I*) vs. measured voltage (*V*)

I also used python to remotely control the Eurotherm 2604 TCU. It is programmable using Binary Synchronous Communications (Bisync) [10] and is connected to the computer RS232 serial port. I can read and write the temperature and the Ramp Rate (RR) of the Eurotherm 2604 TCU. To read the temperature, a byte of start and a byte of end has to be given. To write a temperature, a byte of check is calculated and added to the bytes sequence [38]. The libraries visa and pySerial has been chosen to enable using SCPI and Bisync standards respectively with python.

The working principle of the instrumentation is as following. The user starts by adjusting the suitable SourceMeter parameters, i.e. start current, end current, current step and protection voltage, then he chooses the annealing temperature the TCU has to reach and the ramp rate. While reaching this temperature, the SourceMeter measures the sample sheet resistance every 2.5 s and its value, as well as the instantaneous temperature, time and error, are written in a previously named text file, that is used to plot data. A high error value may be due either to the non ohmic behavior of the sample, as explained earlier, or to the tungsten based points' damage caused by burning and/or oxidation. If this last issue is encountered, it can be handled by a simple cleaning of the points using acetone and paper.

I decided to put in appendix the python scripts that enables the Temperature Control Unit and the SourceMeter remote control. I believe it can be very helpful in case someone wants to rebuild our "homemade" setup. These scripts were implemented using the Keithley 2400 and Eurotherm 2600 datasheets [9][10] and the work of Markus Rosenstihl [38].

Chapter 4

Results and discussion

Chapter 4 gathers the results and discussion of the study of thin film materials, with a high focus on silicides, that interests microelectronics industry and has a the potential to be used in its high technology products' manufacturing process:

- Nickel Silicide is used as a contact material in CMOS technology, mainly for its low resistivity and high thermal stability. It is well known in microelectronics and used here as a standard "material" to check the setup reliability.
- Vanadium Silicide is a superconducting material that has a high potential in quantum computing applications, due to its high critical temperature.

As my work focuses on silicides, in addition to enabling in-situ coupling of electrical and structural characterization techniques, one way to increase silicide based chips' performances is investigated: Alloying i.e. metal incorporation in small quantities in the nickel layer, e.g. 10%at Pt, in order to optimize the silicide resistivity and thermal stability by preventing nickel agglomeration.

Nickel (Platinum) Silicide

I started my work with the material shown in Figure 4.1. Nickel (Platinum) Silicide thin films are widely studied and scientific publications are available. This choice enables to validate the “homemade” setup by comparing the results with literature.

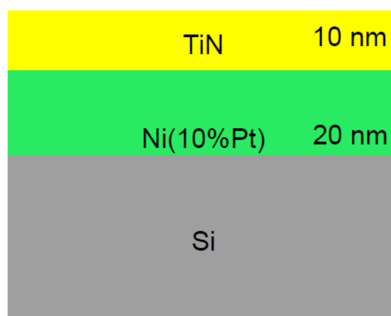


Figure 4.1: Nickel (Platinum) Silicide thin film

From Ni-Si binary system literature review [3][5][12], it seems that three phases are expected to form upon annealing in different temperature domains. One should easily discern in an in-situ XRD diffractogram the Ni, θ-Ni_2Si, δ-Ni_2Si and NiSi peaks.

To validate the formation of the previously cited phases, an in-situ XRD analysis was performed for a temperature range of [35°C-550°C] in air atmosphere as shown in Figure 4.2. In practice, the furnace maintains the temperature every 5°C during 4 mn, the time that an XRD scan needs to be executed. The result is perfectly in harmony with the literature and the PDF cards except one detail; in studies where the nature, amount and thickness of the alloying element are different (here it is 20 nm Ni 10%at Pt), the δ-Ni_2Si phase may form before θ-Ni_2Si. Ni(Pt) thin films are knows to be highly textured [35], which explains why we don’t observe all the diffraction peaks of each phase. This is one of the motivations for the coupling with Raman spectroscopy to confirm the formation of a certain phase. Moreover, the TiN capping layer prevents thermal oxidation of Ni(Pt) but has no footprint on the diffractogram. It may happen to observe TiN peaks at 35° and/or 42° for higher capping layers’ thicknesses.

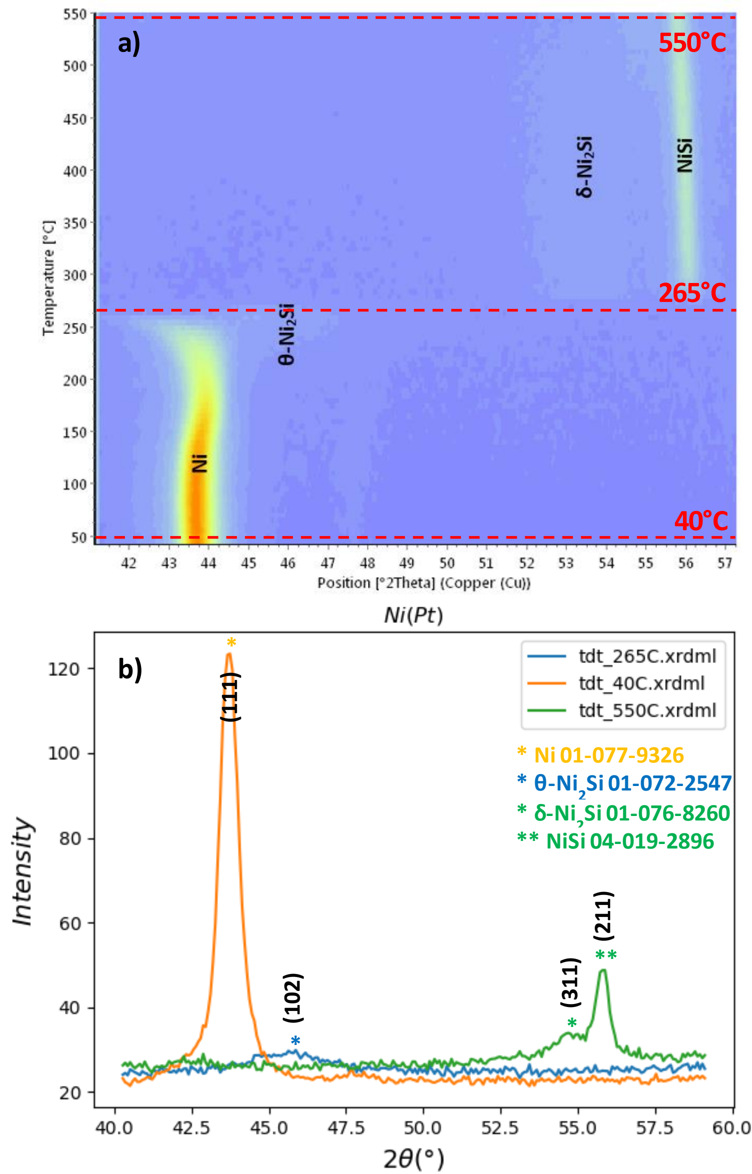


Figure 4.2: in-situ XRD of Ni(Pt) a) from 40°C to 550°C. b) at 40°C, 265°C and 550°C

Our phase sequance, as shown in Figure 4.3, is in agreement with the in-situ XRD result proposed in this publication by F. A. Geenen et al. [3], where temperature domains of existence of the different phases were highlighted for a 9nm Ni(10%Pt) sample.

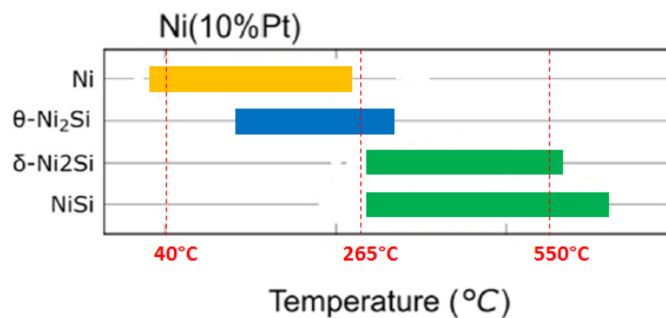


Figure 4.3: temperature domains of existence of the different phases

Platinum incorporation in the nickel metallic layer

In many studies [5][12][16], another metallic element e.g. Pt, Pd, Co have been incorporated into the nickel layer in low concentration (< 10%at). Its amount and the alloy layer's thickness has a significant effect on sheet resistance value, on the first silicide to form (θ or δ-Ni_2Si) [7] and on the NiSi phase thermal stability by delaying the formation of the undesired high resistance $NiSi_2$ phase [16].

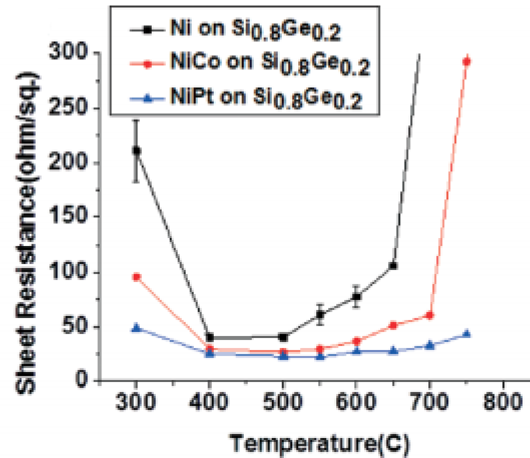


Figure 4.4: sheet resistance of silicide made by Ni, NiCo and NiPt on $Si_{0.8}Ge_{0.2}$ substrate [16]

C-H. Cheng and C-L Hsin [16] studied the effect of the incorporation of 10%at Co and Pt in Ni on Si and on $Si_{0.8}Ge_{0.2}$ substrates. The results in Figure 4.4 shows that the incorporation of alloying elements improves significantly the silicide sheet resistance, and its thermal stability by delaying the formation of the undesired high resistance $NiSi_2$ phase.

The incorporated nickel silicide studied in Chapter 3 is a 20nm thick Ni layer with 10% atomic fraction of Pt: Ni(10%at Pt), that is currently used in STMicroelectronics MOSFET manufacturing process.

To go further in the in-XRD data analysis, it may be interesting to investigate the evolution of Ni(111) peak (or any other peak) with annealing temperature by a Peak fitting XRD data [11]. The Ni(111) $K\alpha_1$ peak parameters i.e. intensity, position and Full Width at Half Maximum (FWHM) are plotted versus annealing temperature and results are presented in Figure 4.5.

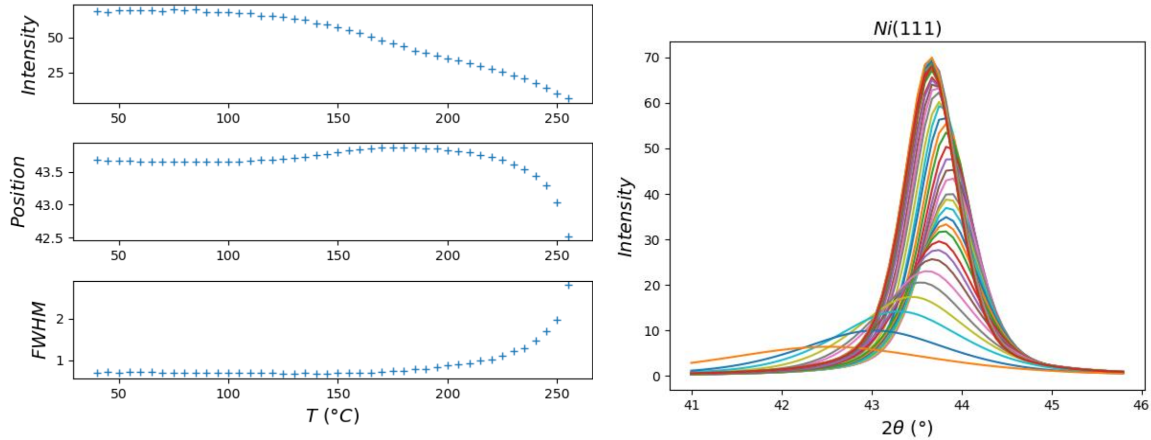


Figure 4.5: Evolution of Ni(111) peak parameters with annealing temperature

The Ni(111) peak intensity decreases with annealing temperature because the amount of the Ni phase in the microstructure decreases in favor of θ-Ni_2Si, δ-Ni_2Si and NiSi phases nucleation & growth.

Annealing usually lowers the peak position ϑ i.e. increases the interplanar *d*-spacing due to the thermal expansion effect. Here, this effect is not clearly observed because the rising amount of Pt in the remaining Ni layer also contributes to the evolution of the interplanar *d*-spacing through the increase of the lattice parameter.

From Scherrer equation (2.17), we can estimate the Ni(111) phase initial mean grain size at 12.54 nm. Then the grain size starts reducing at ~150°C until its final value, at ~255°C, estimated at 3.18 nm.

While performing the in-situ XRD analysis, I identified in Figure 4.2 three interesting temperatures where the peaks of the Ni, θ-Ni_2Si, δ-Ni_2Si and NiSi phases are intense. Since the Ni_2Si phase peak intensity is weak, it may be challenging to observe because of a high signal to noise ratio. Thus, in order to confirm the formation of the Ni_2Si phase, a Raman spectroscopy (wavelength: 647nm, power: 4mW, acquisition time: 10mn) was performed on three samples that were annealed up to 40°C, 265°C and 550°C using the same furnace and the results are shown in Figure 4.6. Indeed, the identification of the δ-Ni_2Si phase (orthorhombic) is confirmed by the peak at 140 cm^{-1} in the 265 °C curve, in accordance with the results of P.S. Lee et al. [4]. The NiSi phase is also clearly identified by the peaks at 200 cm^{-1} and 220 cm^{-1} in the 265°C and 550°C curves.

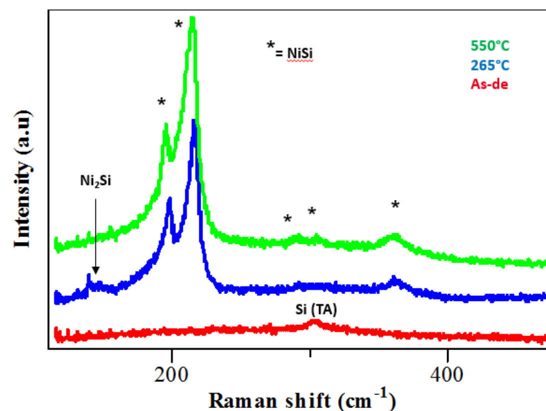


Figure 4.6: post annealing Raman spectroscopy for as-deposited, 265°C and 550°C samples

Moreover, in order to investigate the nucleation & growth of the Ni_2Si phase, i.e. to know whether it nucleates as clusters inside the Ni matrix or as an interlayer at the level of the Ni/Si interface, an XRR analysis was performed on a sample that was annealed up to 260°C and the results are shown in Figure 4.7. In fact, one can observe at least three periodic oscillations in the interferences pattern. Each period corresponds to one layer and its thickness can be derived from the XRR Bragg's law (3.2). However, using the XRR Fast Fourier Transform (FFT), it seems that the TiN, Ni_2Si and NiSi layers are discernable by XRR. Thus, it is possible that the Ni_2Si phase nucleates as an interlayer at the level of the Ni/Si interface, as seen in other studies [12]. Further investigation using in-situ XRR is needed to establish a more satisfying conclusion.

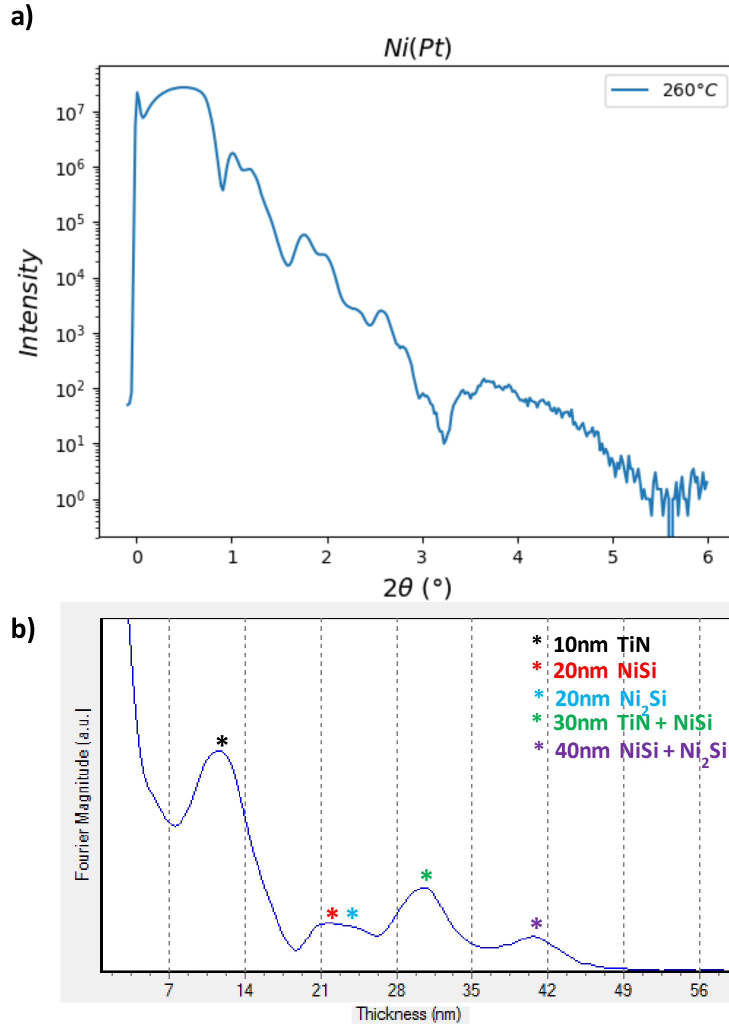


Figure 4.7: a) XRR analysis of Ni(Pt) sample annealed at 260°C and b) its FFT transform

With the "homemade" setup I built according to Figure 3.6, I also measured the sheet resistance of an Ni(Pt) sample in a temperature range of [35°C-300°C] in the same ramp rate and atmosphere conditions as in XRD, and the results are shown in Figure 4.8. This experiment shows the interest of the in-situ coupling of XRD and sheet resistance measurement. In fact, the linear sheet resistance increase at low temperature is believed to be due to the thermal motion, i.e. phonons contribution to the sheet resistance evolution as explained in the experimental part, because the sample annealing is performed with a constant ramp rate. Followed by a more rapid increase at ~150°C that is belived to be due to the formation of the high resistance θ-Ni_2Si phase and the Ni(111) phase mean grain size reduction observed in Figure 4.5. Then, a suddent decrease in sheet resistance value is noticed at ~265°C and corresponds to the Ni to NiSi phase transition, which activation energy was estimated at 2.567 eV, usinig the Kissinger method for various ramp rates between 5°C/min and 50°C as explained by E.G. Colgan et al [2]. Sheet resistance values are in accordance with those found in similar studies [5][12].

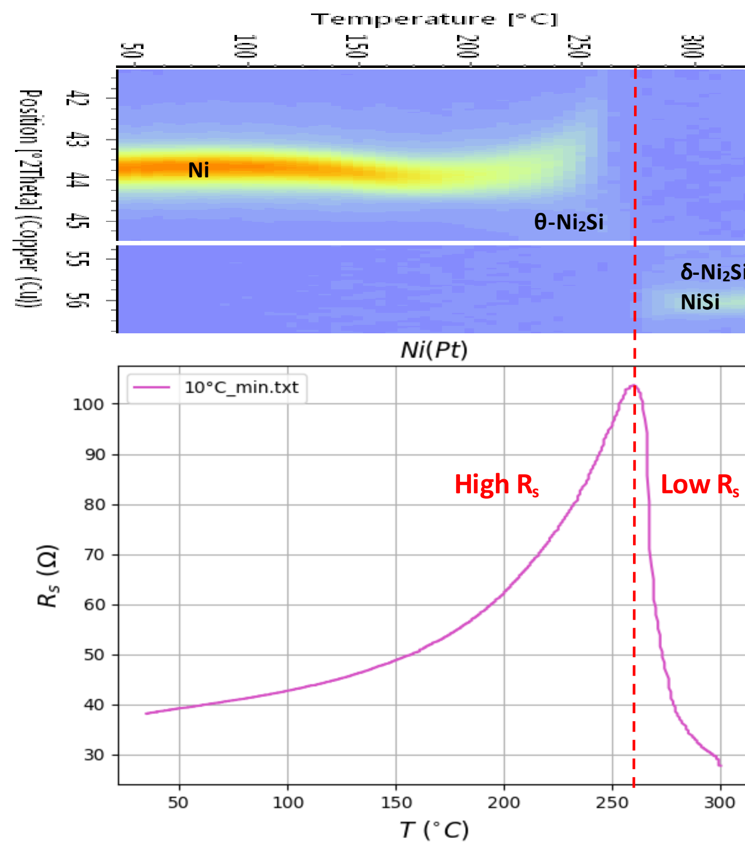


Figure 4.8: in-situ sheet resistance of Nickel (Platinum) Silicide

Estimation of activation energy by the Kissinger method

Silicide formation by diffusion can occur either by lattice diffusion (high activation energy ~ 2.5 eV) or by grain boundary diffusion (low activation energy ~ 1.5 eV) [13].

In brief, a silicide that is formed by grain boundary diffusion is less energy consuming but it implies a higher density of microstructural defects and thus, increases resistivity by reducing the electrons mean free path through grain boundary scattering.

Obviously, it would be perfect to form a defects-free silicide because it has a lower resistivity and implies a higher MOSFET performances but it will have a higher cost in terms of formation energy. Thus, a compromise between low activation energy (i.e. energy saving while silicide formation) and low resistivity (i.e. good performances of the contact material) has to be taken in an industrial process point of view.

The Kissinger method consists on performing sheet resistance measurements for various ramp rates (RR) in C°/min. In Figure 4.9, One can easily notice that the temperature of NiSi formation increases with the ramp rate i.e. the temperature at which the sheet resistance suddenly decreases. This temperature is determined by the minimum in sheet resistance' first derivative $\frac{dR_S}{dT}$ as following:

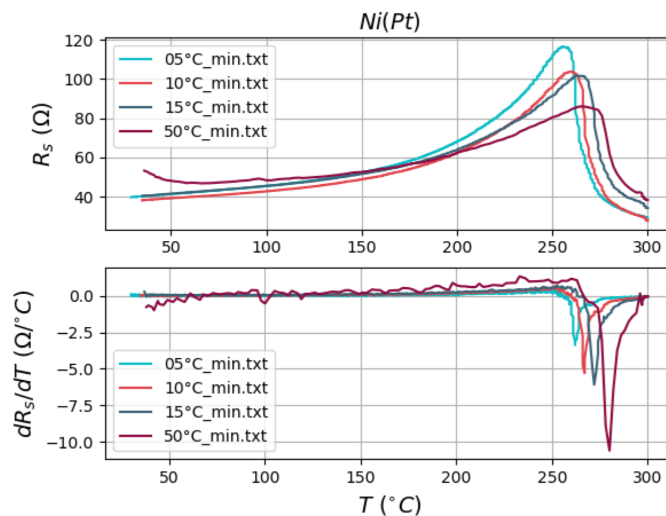


Figure 4.9: sheet resistance and its derivative in accordance with annealing temperature

The minimun of each $\frac{dR_s}{dT}(T)$ curve gives one (RR, T) point of the Kissinger plot, which is given by equation (4.1) [2]. The activation energy is given by its slope as shown in Figure 4.10:

$$ln\left(\frac{RR}{T^2}\right) = -\frac{E_A}{k} * \frac{1}{T} - ln(\frac{x^2 E_A}{kK_0}) \quad (4.1)$$

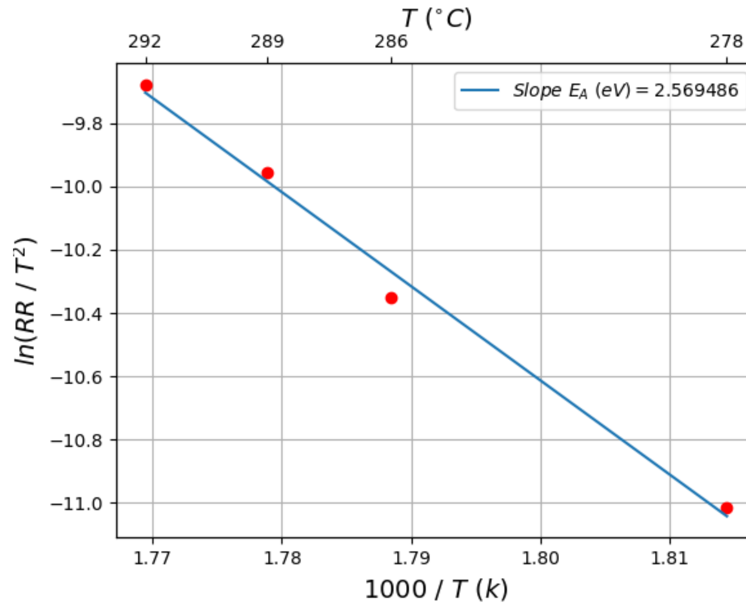


Figure 4.10: Kissinger plot

The Kissinger method is an estimation of the activation energy of a certain phase transition. Thus, its value may be slightly different from values obtained by other techniques e.g. Arrhenius plot that uses the reaction rate coefficient $k = A\exp(-\frac{E_A}{RT})$.

This Ni to NiSi phase transition can also be activated using an isothermal annealing slightly above the transition temperature. In fact, an in-situ sheet resistant measurement of a sample annealed at 240°C highlights the effect of Pt incorporation in Ni layer. Since Ni is progressively consumed while θ-Ni_2Si formation, the thickness of Ni layer decreases and the alloy becomes more rich in Pt because the Ni lattice parameter increases due to the incorporation of a larger alloying element. In Figure 4.11, the increase of sheet resistance is due to the formation of the high resistance θ-Ni_2Si phase, the Ni(111) phase mean grain size reduction, and possibly to the rising amount of Pt in the remaining layer of Ni. Then the Ni to NiSi phase transformation decreases the sheet resistance value. Similar study has been conducted by M. Putero and D. Mangelinck on Ni(6%at Pd) [5].

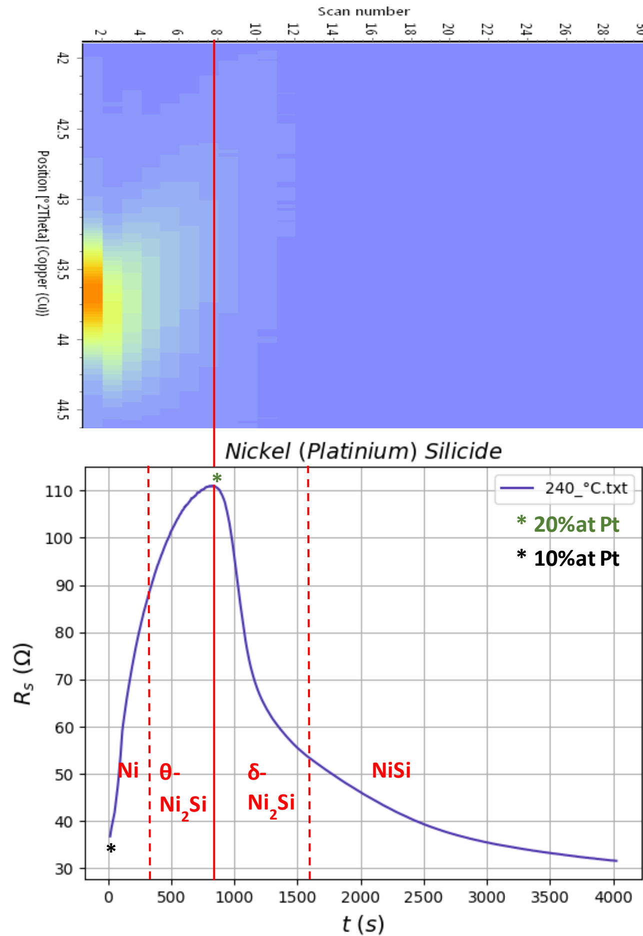


Figure 4.11: in-situ sheet resistance of Nickel (Platinum) Silicide annealed at 240°C

The maximum amount of Pt in Ni (~ 20%at) was determined using Vegard's law (4.2) [34] because Ni and Pt have the same FCC crystallographic structure.

$$a_{A_{1-x}B_x} = (1-x)a_A + xa_B \tag{4.2}$$

a: Lattice parameter

AB: Binary compound

x: atomic fraction

The previous measurements were performed in air atmosphere for the probes positionning reasons mentionned earlier. In order to make sure that atmospheric conditions has no impact on our results, I tested the Ni(Pt) sample in a “real” sheet resistance measurement in vacuum atmosphere. In fact, to prevent the formation of metal oxide(s) upon annealing, an in-situ sheet resistance measurement in primary vacuum atmosphere is enabled by the system in Figure 4.12. It consists on an INSTEC hot stage probing system in vacuum/gas atmosphere and measures the sheet resistance using Van Der Pauw method. The ramp rate can be increased up to 100°C/min. After the stage is closed, two taps enables gas and vacuum (up to 10^{-2} mbar) arrivals control.

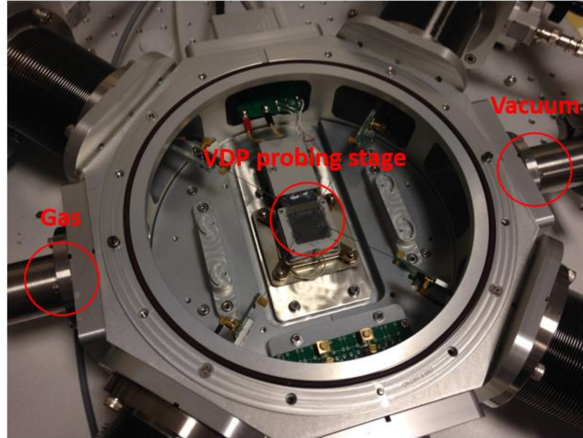


Figure 4.12: INSTEC hot stage probing system in vacuum/gas atmosphere

Results for nickel (platinum) silicide in Figure 4.13 are identical to the sheet resistance measurements performed in air atmosphere except one obvious difference; the Ni to NiSi phase transition temperature is almost 100°C higher in vacuum atmosphere. It can be due to two phenomena:

- The displayed temperature may change from each furnace manufacturer to another e.g. because the position of the thermocouple can influence the measured value.
- While annealing in vacuum atmosphere, there is no convection contribution to the thermal transfer. Thus, the heating occurs only by conduction and radiation.

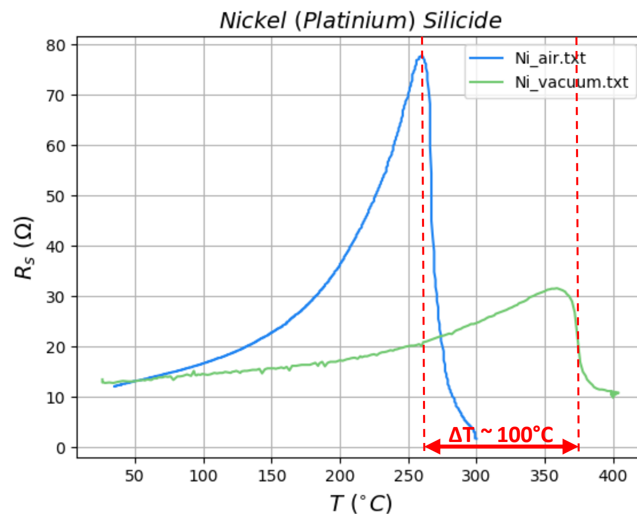


Figure 4.13: in-situ sheet resistance of nickel (platinum) silicide in vacuum atmosphere

To conclude, annealing in vacuum atmosphere has possibly an effect on Ni to NiSi phase transition temperature i.e. activation energy and microstructure. It also showed that there are no thermal oxidation issues in air atmosthere as it was noticed for vanadium silicide in the following.

Vanadium Silicide

Vanadium Silicide is a superconducting material that has a high potential in quantum computing applications, due to its high critical temperature. As shown in Figure 4.14, the effect of adding an interlayer between metal and silicon substrate was investigated. Traditionally, SiO_2, famously known as Silicon On Insulator (SOI) technology, is used to reduce the parasitic device capacitance.

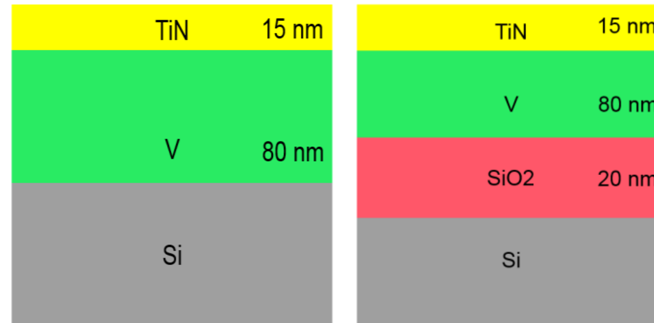


Figure 4.14: Vanadium Silicide thin film

A prediction of the first phase to form and the sequential growth is enabled by the Effective Heat of Formation (EHF) model [1]. According to this model, the first phase to form is the congruent one with the greatest heat generated per unit change in the concentration of the limiting element from the liquid minimim, ΔH'.

The EHF model tells us that in the absence of any other factors e.g. amorphization, impurities, oxide barrier…, VSi_2 will form first, and then V_5Si_3. Since V_5Si_3 has a lower (more negative) enthalpy than V_3Si per total number of atoms, V_3Si will not form when both Si and V are available. However, if the diffusion of Si is limited e.g. because all Si in the system has been consumed, or because Si binds to oxygen, then V_3Si may form because the energy gain per atom Si, i.e. the slope from the bottom-right in the EHF diagram, is still greater than it is for V_5Si_3. Particular interest is given to the V_3Si superconductive silicide due to its high critical temperature.

Similarly to the experiments performed on nickel (platinum) silicide, I performed on the vanadium sample an in-situ XRD analysis from ambiant temperature to 600°C and didn't noticed any silicide formation. A grey/green deposits were observed on the sample surface and a post annealing XRD analysis showed that only V_2O_5 oxide forms. This confirms that vanadium is a very oxophilic chemical element [6] and that the TiN capping layer is not enough to prevent its thermal oxidation compared to Ni(Pt).

In order to confirm vanadium oxide(s) formation at high temperature, an in-situ sheet resistance measurement was performed on a vanadium silicide sample in the same ramp rate conditions as in XRD. Figure 4.15 shows a sudden formation of a very resistive phase(s) at 525°C, that possibly conrresponds to vanadium oxide(s). Thus, in order to prevent the vanadium thermal oxidation, all experiments must be performed in non-air atmosphere. F. Ziegler et al [6] suggested to perform in-situ XRD analysis in He atmosphere plus a Ti getter to remove the remaining oxygen particles.

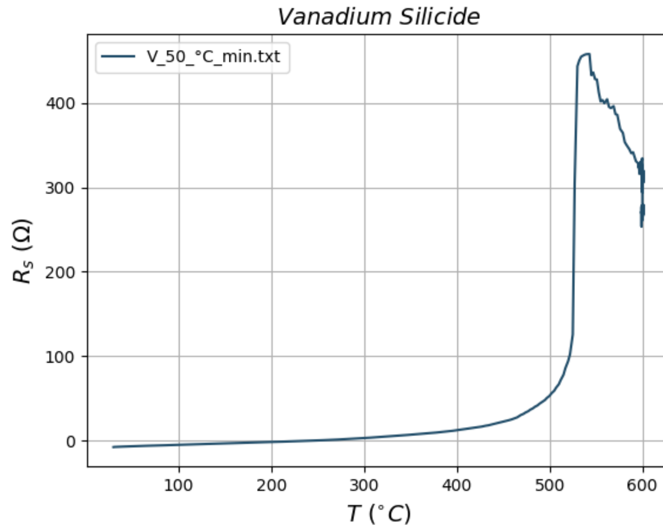


Figure 4.15: in-situ sheet resistance of vanadium silicide in air atmosphere

To overcome the previously noticed vanadium thermal oxidation issues, an in-situ XRD analysis was performed on the vanadium sample from ambiant temperature to 1100°C in vacuum atmosphere. One can easily identify in Figure 4.16 the VSi_2 phase formation after 600°C, in accordance with its PDF card. This confirms the EHF model prediction that VSi_2 is the first silicide to form.

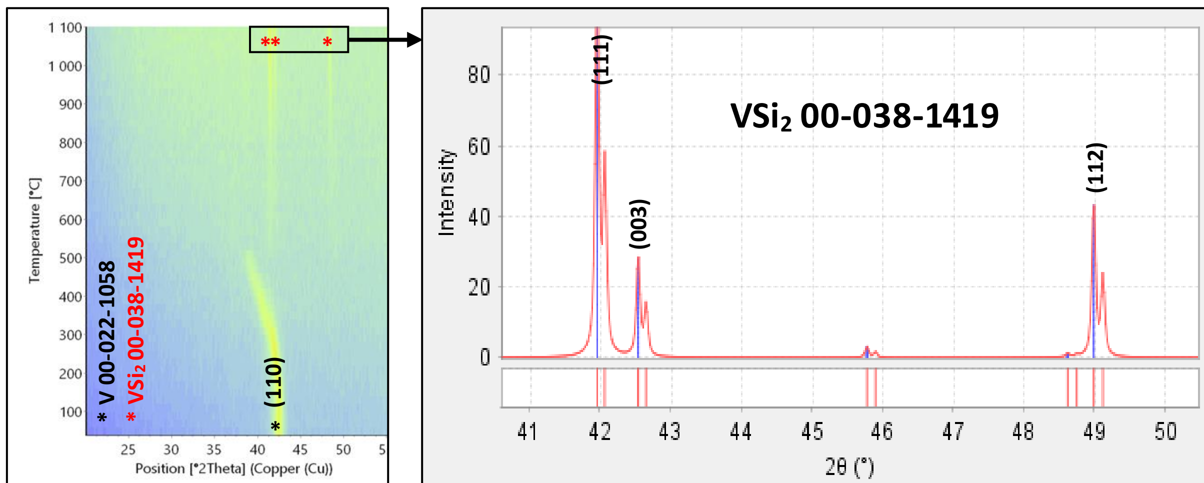


Figure 4.16: in-situ XRD of vanadium silicide in vaccum atmosphere

As briefly introduced earlier, in-situ sheet resistance measurement can also be performed in vacuum atmosphere using the INSTEC hot stage probing system. Figure 4.17 shows the results for the vanadium silicide sample. The sheet resistance evolution is totally different than the measurement in air atmosphere. This confirms that thermal oxidation is a major issue in in-situ analysis of vanadium based thin films. A linear sheet resistance increase at low temperature is believed to be due to the thermal motion, i.e. phonons contribution to the sheet resistance evolution as explained in the experimental part, because the sample annealing is performed with a constant ramp rate. Then the interplannar *d*-spacing increase, i.e. the V(110) peak position shift in Figure 4.18 due to the thermal expansion, decreases the sheet resistance value, in accordance with F-S electron surface scattering model, until it became constant around 800°C upon VSi_2 is formation.

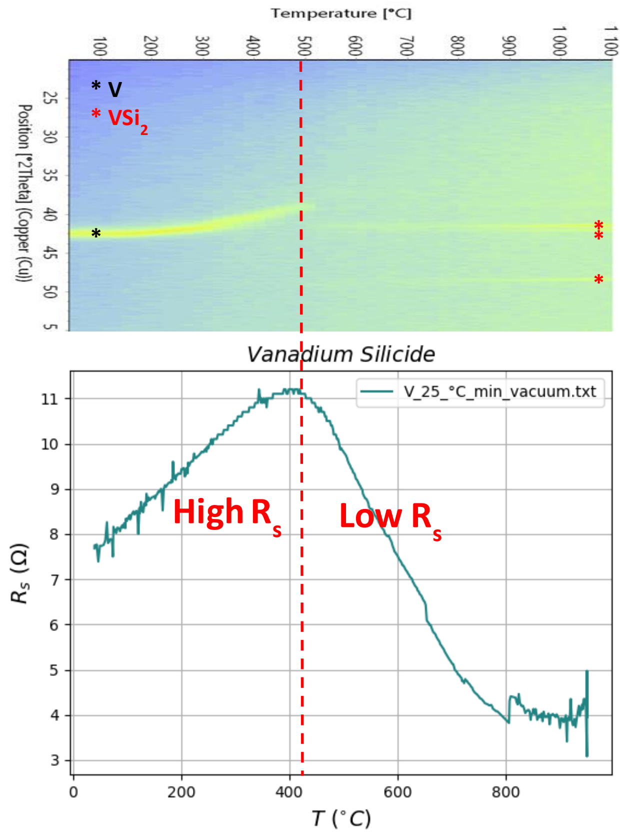


Figure 4.17: in-situ sheet resistance of vanadium silicide in vacuum atmosphere

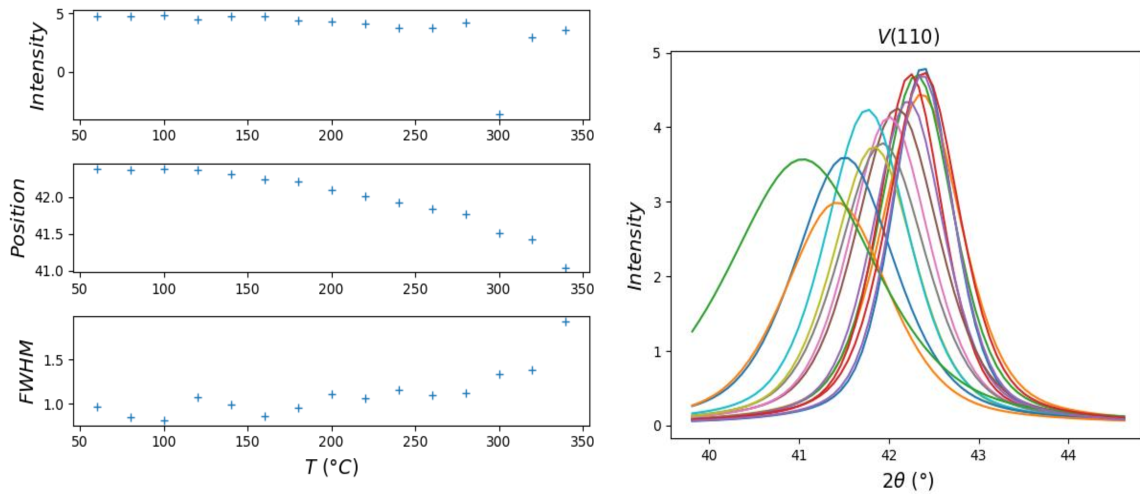


Figure 4.18: evolution of V(110) peak parameters with annealing temperature

Chapter 5

Conclusions

The aim of this master thesis, is to correlate the electrical and structural properties of materials of high interest in microelectronics industry by in-situ coupling of electrical and structural characterization techniques. In order to make this in-situ coupling possible, a “homemade” setup was built. It consists on a heating stage that plays the role of a sample holder in a diffractometer/spectrometer while 4 tungsten based points’ probes are positioned on the sample surface and measures its sheet resistance. Both the Temperature Control Unit (TCU) and the SourceMeter are remotely controlled using a python script that reads and writes the TCU temperature and Ramp Rate (RR), and sources current and senses voltage using the SourceMeter.

Our setup is composed of an Anton Paar DHS 1100 heating stage and its Eurotherm 2600 Temperature Unit Control (TCU). It enables to perform measurements in vacuum/inert gas atmosphere by adding a dome that closes the heating stage, but makes impossible to position the probes. The 4 tungsten based points’ probes are positioned on the heating stage where the sample is annealed. It seems that the larger the distance between the probes, the deeper the current penetrates into the film. Thus, the sheet resistance value may also has a substrate contribution. Since the dome is impossible to be added, the sheet resistance measurements were performed in air atmosphere.

The working principle of the instrumentation is as following. The user starts by adjusting the suitable SourceMeter parameters, i.e. start current, end current, current step and protection voltage, then he chooses the annealing temperature the TCU has to reach and the ramp rate. While reaching this temperature, the SourceMeter measures the sample sheet resistance every 2.5 s and its value, as well as the instantaneous temperature, time and error, are written in a previously named text file, that will be used to plot data. A high error value may be due either to the non ohmic behavior of the sample, as explained earlier, or to the tungsten based points’ damage caused by burning and/or oxidation. If this last issue is encountered, it can be handled by a simple cleaning of the points using acetone and paper.

In-situ measurements in non-air atmosphere can be performed using a more sophisticated setup. LINKAM (UK) developed a system, in Figure 5.1, consisting on a heating stage that has a gas tight environment and seems to be very interesting to perform sheet resistance measurements in vacuum/inert gas atmosphere, which is not possible with our setup because of the Anton Paar DHS 1100 dome. It was decided at the end of the thesis to buy that system.

Figure 5.1: LINKAM HFS probe stage [31]

Our “homemade” setup was used to study materials that are used in microelectronics industry high technology products manufacturing process, e.g. nickel silicide, vanadium silicide, ITO… with a high focus on the NiSi silicide, which is used as a contact material in CMOS technology, mainly for its low resistivity.

The Ni to NiSi phase transition activation energy can be derived from the Kissinger method by performing in-situ sheet resistance measurement for various annealing rate values. In this study, an activation energy of 2.567 eV was computed. This value is characteristic of lattice diffusion driven phase transitions, which means that the phase formed is poor in structural defects but has a high cost in energy.

It was shown, using in-situ sheet resistance measurement, that Pt incorporation (but also Co and Pd in other studies) in small quantities improves significantly the silicide thermal stability by delaying the formation of the high resistance $NiSi_2$ silicide. With an isothermal in-situ sheet resistance measurement, it was also shown that the amount of Pt in the remaining Ni layer increases upon annealing.

In-situ sheet resistance measurements of vanadium required vacuum atmosphere due to thermal oxidation issues. The results were correlated with in-situ XRD data. The sheet resistance evolution for vanadium is mainly due to thermal expansion i.e. film thickness increase as reported in F-S model until vanadium silicide formation at high temperature.

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```python
# -*- coding: utf-8 -*-
"""
Created on Tue Jul 23 16:18:45 2019

@author: RE256379
"""

import time,datetime
import visa
import numpy as np
import matplotlib.pyplot as plt
from Rs_and_DHS import *


# Form Manual p. 127
# Meas Ref & Zero = 2 x NPLC / Line Frequency
# NPLC is the present speed setting (0.01 to 0.1 PLC). (0.4 ms to 4ms )

#
def V_I_CURVE(SENS_VOLT_PROT,
              SOUR_CURR_START,
              SOUR_CURR_STOP,
              SOUR_CURR_STEP,
              INST):
#
    INST.write(':ROUT:TERM REAR')
    print(INST.query(':ROUT:TERM?'))
    INST.write(':SENS:FUNC:CONC OFF')
    INST.write(':SOUR:FUNC CURR')
    INST.write(':SENS:FUNC "VOLT:DC"')
    INST.write(':SENS:VOLT:PROT %f'%SENS_VOLT_PROT)
    INST.write(':SOUR:CURR:START %f'%SOUR_CURR_START)
    INST.write(':SOUR:CURR:STOP %f'%SOUR_CURR_STOP)
    INST.write(':SOUR:CURR:STEP %f'%SOUR_CURR_STEP)
    INST.write(':SOUR:CURR:MODE SWE')
    INST.write(':SOUR:SWE:RANG AUTO')
    INST.write(':SOUR:SWE:SPAC LIN')
    TRIG_COUN = int(SOUR_CURR_STOP / SOUR_CURR_STEP * 2 +1)
    INST.write(':TRIG:COUN %f'%TRIG_COUN)
    INST.write(':TRIG:DEL 0')

    INST.write(':SOUR:DEL 0')
#     INST.write(':SOUR:DEL:AUTO ON')

    INST.write(':OUTP ON')
    #time.sleep(5)

    INST.timeout = 20000
    raw = INST.query_ascii_values(':READ?')
    #time.sleep(30)
    INST.write(':OUTP OFF')


    #I = np.arange(0,.1,0.01)
    Vm   = np.array([raw[i*5] for i in range(TRIG_COUN)])
    Idut = np.array([raw[i*5+1] for i in range(TRIG_COUN)])
    return [Vm, Idut]


#
def MeasureR( SENS_VOLT_PROT,
```

```
                  SOUR_CURR_START,
                  SOUR_CURR_STOP,
                  SOUR_CURR_STEP,
                  INST):
    '''
    v0.1
    timestamp .... time estimation of measure
    '''
    t0 = time.time()
    data = V_I_CURVE(SENS_VOLT_PROT, SOUR_CURR_START, SOUR_CURR_STOP, SOUR_CURR_STEP,INST)
    timestamp =  (time.time() -t0)
    p = np.polyfit(data[1],data[0],1)
    R = p[0]
    err = np.sqrt(np.sum(abs(data[0]**2 - np.polyval(p,data[1])**2)))
    return (timestamp,R,err)


# ##############
rm = visa.ResourceManager()
rm.list_resources()
('ASRL1::INSTR', 'ASRL2::INSTR', 'GPIB0::15::INSTR')
inst = rm.open_resource('GPIB0::15::INSTR')
print(inst.query("*IDN?"))

# Parameter selection
nsave ='V_SiO2_iso400.txt'

# Elect parameter
freq = .2
SENS_VOLT_PROT   = 30
SOUR_CURR_START = -.03
SOUR_CURR_STOP   = .03
SOUR_CURR_STEP   = 10E-4*2
# Thermal parameter
Consigne = 500
RampRate = 500

# Header
header = '#Sample name: %s\n#Date: %s\n'%('S1',datetime.datetime.now())
header = header + '#ComplianceV = %.2f\n#I_start(Amp) = %.5f\n#I_end(Amp) = \
                  %.5f\n#I_step(Amp) = %.5f\n#RampRate = %i\n' \
                  %(SENS_VOLT_PROT,SOUR_CURR_START,SOUR_CURR_STOP,SOUR_CURR_STEP,RampRate)

with  open(nsave,'w') as f:
    f.write('%s'%header)
    f.write('#T(Celsius)\tRs(ohm/sq)\terr\t\t Power\t\t Time (s)\n')



# Init main
Rs, T=[],[]
t0  = time.time()

# Estimation R measurment time with chosen parameters
(timestamp,R,err) = MeasureR(SENS_VOLT_PROT   = SENS_VOLT_PROT,
                             SOUR_CURR_START = SOUR_CURR_START,
                             SOUR_CURR_STOP   = SOUR_CURR_STOP,
                             SOUR_CURR_STEP   = SOUR_CURR_STEP,
                             INST = inst)

print('Estimation Rs time (s)%f'%timestamp)
```

```
# Wake-up
#for i in range(5):
#    (tt,R,err) = MeasureR(SENS_VOLT_PROT  = SENS_VOLT_PROT,
#                          SOUR_CURR_START = SOUR_CURR_START,
#                          SOUR_CURR_STOP  = SOUR_CURR_STOP,
#                          SOUR_CURR_STEP  = SOUR_CURR_STEP,
#                          INST = inst)

#
SetRampRate(RampRate=RampRate)
SetTemp(Temp=Consigne)

temperature = GetTemp()
#while temperature<Consigne:
while True:
    (timestamp,R,err) = MeasureR(SENS_VOLT_PROT  = SENS_VOLT_PROT,
                                 SOUR_CURR_START = SOUR_CURR_START,
                                 SOUR_CURR_STOP  = SOUR_CURR_STOP,
                                 SOUR_CURR_STEP  = SOUR_CURR_STEP,
                                 INST = inst)
    print('%.1f\t%.2f\n'%(temperature,R))
#    time.sleep(tt*1.1)
    temperature = GetTemp()
    power       = GetPower()
    t = time.time()-t0
    with  open(nsave,'a') as f:
        f.write('%i\t%.3f\t\t%.5f\t\t%.3f\t\t%.3f\n'%(temperature,R,err,power,t))
```

```python
# -*- coding: utf-8 -*-
"""
Created on Tue Jul 23 16:18:45 2019

@author: RE256379
"""
import time, datetime
import visa
import numpy as np
import matplotlib.pyplot as plt
import serial,binascii,time
from functools import reduce
import operator




def GetTemp(verbose=True):
    if Euro.is_open is not True:
        Euro.open()
    # v0.1 N.V. 5/04/2019
#    Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
    byte=b'\x040011PV\x05'
    Euro.write(byte)
    time.sleep(.1)
    hh = Euro.read_all()
    Euro.close()
    Temp = float(str(hh).split('PV')[1].split('\\x03')[0])
    if verbose == True:
        print('Temp(C) = %.1f'%Temp)
    return Temp

#
def GetPower(verbose=True):
    if Euro.is_open is not True:
        Euro.open()
    # v0.1 N.V. 5/04/2019
#    Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
    byte=b'\x040011OP\x05'
    Euro.write(byte)
    time.sleep(.1)
    hh = Euro.read_all()
    Euro.close()
    Power = float(str(hh).split('OP')[1].split('\\x03')[0])
    if verbose == True:
        print('Power(percent) = %.1f'%Power)
    return Power

def GetRampRate(verbose=True):
    if Euro.is_open is not True:
        Euro.open()
    # v0.1 N.V. 5/04/2019
#    Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
    byte=b'\x040011RR\x05'
    Euro.write(byte)
    time.sleep(.1)
    hh = Euro.read_all()
    Euro.close()
    Temp = float(str(hh).split('RR')[1].split('\\x03')[0])
    if verbose == True:
```

```python
        print('Temp(C) = %.1f'%Temp)
    return Temp

def SetTemp(Temp):
    if Euro.is_open is not True:
        Euro.open()
    # v0.1 N.V. 5/04/2019
    bcc =(reduce(operator.xor, map(ord,"SL%i\x03"%Temp)))
    data = bytes('\x040011\x02SL%i\x03%c'%(Temp,bcc),encoding='utf-8')
#     Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
    Euro.write(data)
    Euro.close()

def SetRampRate(RampRate):
    if Euro.is_open is not True:
        Euro.open()
    bcc =(reduce(operator.xor, map(ord,"RR%i\x03"%RampRate)))
    data = bytes('\x040011\x02RR%i\x03%c'%(RampRate,bcc),encoding='utf-8')
#     Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
    Euro.write(data)
    Euro.close()



#


# ##############
Euro = serial.Serial('COM1',baudrate=9600,parity= 'E',bytesize=7,stopbits=1)
```