# MULTICRYSTALLINE SILICON THIN FILMS GROWN DIRECTLY ON LOW COST SODA-LIME GLASS SUBSTRATES

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**Abstract**

Liquid phase crystallization of silicon is a promising technology platform to grow multi crystalline silicon thin films on foreign substrates. For solar cell application it has already been demonstrated that open circuit voltages of up to 661 mV [1] and efficiencies of up to 15.9 % [2] can be achieved on a silicon layer of a few microns only. However, while the quality of the material has been continuously improved, the cost factor of the utilized substrate has been given little attention. The present work focuses on the technology transfer from technical glass substrates to low cost soda-lime glass substrates to become more attractive for commercial applications. We demonstrate first liquid phase crystallized silicon layer on soda-lime glass substrate and show that the layer adhesion by the more than twice as large expansion coefficient of soda lime glasses compared to the established technical glasses has a significant influence on various processing options and countermeasures to overcome adhesion issues have to be considered. Furthermore, we investigate the electrical performance of the resulting absorber material for silicon thin film solar cells and report our first results on the electrical performance in terms of open circuit voltages, Hall mobility's and effective minority carrier lifetimes.

*keywords:* *multicrystalline silicon*
*soda-lime glass*
*laser crystallization*
*thin films*

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## 1 Introduction

Silicon forms the basis of many modern technologies and has found its way into applications such as microelectronics, sensor technology and the solar industry. Although the market is clearly dominated by silicon wafer technology, thin silicon of arbitrary thickness fabricated directly on large area glass substrates offers some distinctive advantages within the above-mentioned applications. However, mainly the display industry has successfully commercialized the silicon thin film technology. Here the excimer laser annealing (ELA) [3,4] process for the silicon refinement represents the state of the art for the backplane fabrication. In the photovoltaic field, there were also attempts to produce thin silicon directly on large area substrates. Techniques such as solid phase crystallization (SPC) [5,6], metal induced crystallization (MIC) [7,8] and zone melting recrystallization (ZMR) [9,10] have been developed. Nevertheless, apart from a brief digression of the SPC technology [5], none of the technologies was able to compete commercially on a long term. A major challenge of the furnace-based (SPC, MIC) and lamp-based (ZMR) processes was the limited thermal endurance of the utilized substrates due to areal heating ultimately resulting in a severely limited processing range. In contrast, the vast development of high power continuous wave laser systems and their use for material refinement enabled significantly higher levels of process control by providing excellent spatial and temporal intensity control and, in conjunction with beam shaping optics, ultra-thin line profiles with high uniformity and a large depth of focus. As a result, the overall thermal load on the substrates can be significantly reduced and new opportunities in material processing became available. Additionally, the utilization of line-shaped laser systems enables in-line processing capability and a seamless scalability. As a consequence, the ZMR technology has evolved into the liquid phase crystallization technology (LPC) [11]. Continuous research progressively improved the LPC fabricated silicon material quality. An open circuit voltages of up to 661 mV [1], which is just 2 % below the current world record cell for multi crystalline silicon wafer technology [12,13], could be demonstrated. Also a solar cell efficiency of 15.9 % was shown [14]. In addition to the material quality, the cost aspect must be taken into account, since the technology has hitherto been based on costly technical glass substrates [15]. In this article, we examine the technology transfer from technical glass to soda-lime glass.

## 2 Experimental

Before the deposition of silicon on soda-lime glass and the subsequent liquid phase crystallization, we undertook a preliminary investigation of the relevant basic physical properties of several soda-lime glass substrates from different manufacturers. By rapid thermal annealing (RTA) we determined the thermal behavior of the various soda-lime glass substrates and identified suitable deposition condition in terms of temperature ramp-up and maximum hold temperature. Furthermore, we measured the optical reflectance ($R$) and transmittance ($T$) with an UV/Vis-spectrometer in the range of 300 – 1200 nm with a resolution of 5 nm. Using both spectra, R and T, we calculated the resulting absorbance ($A$).

For the subsequent second part of our investigation, we selected the most suitable glass based on the results of the preliminary tests. The 100·100 mm² sized substrates got labeled and cleaned with an alkaline cleaning agent and deionized water at elevated temperatures in an industrial dishwasher. Deposition was performed using an integrated plasma enhanced chemical vapor deposition (PECVD) and electron beam physical vapor deposition (EBPVD) cluster tool. First of all an intermediate layer triple stack of $SiO_x/SiN_x/SiO_xN_y$ was deposited via PECVD. The layer stack simultaneously served as a diffusion barrier, antireflection coating and as a passivation layer. Further details on the development and deposition process of the intermediate layer stack are described in literature [16]. With the intermediate layer deposition completed we then applied the

silicon absorber layer by high-rate electron beam evaporation. As a dopant source, a very thin phosphorous-doped silicon layer ($N_D \sim 10^{19}$ cm$^{-3}$) was deposited with the PECVD on top of the silicon absorber layer. Finally, a 50 nm thick PECVD $SiO_x$ capping layer was deposited to protect the absorber from contamination by handling the samples outside of the vacuum and during the subsequent crystallization process.

Prior to crystallization, the 100·100 mm² sized substrates were cut into smaller samples of 20·50 mm² and were pre-heated on an integrated heating stage ($T_{sub}$) at the crystallization laser tool to reduce thermal stress during the liquid phase crystallization of the silicon absorber layer. Crystallization source is a custom made high power, space and wavelength multiplexed direct diode system with a center wavelength of $\lambda_{Laser}$ = 808 nm and a beam shaping optic to create a 31 mm top-hat line with a gaussian profile across the minor axis at a 1/e² of 0.301 mm. The optical intensity of the laser ($I_{opt}$) and the scanning velocity ($v_{scan}$) can be adjusted within 0.3 – 11 kW/cm² and 0.1 – 100 mm/s, respectively. The maximum achievable $T_{sub}$ is 750 °C. For a successful liquid phase crystallization on the selected soda-lime glass, the crystallization parameters were varied to identify a stable process window.

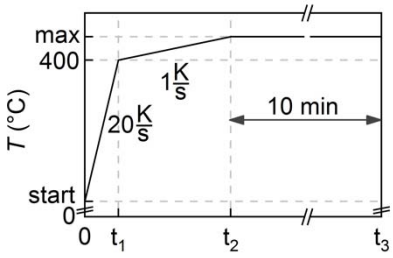
Solar cell test devices are fabricated on the crystallized silicon layers. Therefore, the $SiO_x$ capping layer is removed with a 2 % HF-solution before a bulk and interface passivation in a hydrogen plasma is applied [17]. Afterwards, several nanometers of the silicon absorber are etched off to remove plasma induced surface defects using a poly silicon wet etch consisting of $HNO_3$. $H_2O$ and HF [50:20:1 vol. %]. Next, a standard RCA cleaning procedure is performed [18]. The heterojunction is prepared with a low-temperature PECVD cluster tool by depositing a hydrogenated intrinsic and p-doped amorphous silicon emitter layer stack (a-Si:H(i,p$^+$)). Subsequently, a reactive sputtered ITO layer is deposited as a transparent conductive oxide layer (TCO) with a thickness of 80 nm on top of the emitter layer. While adhesive Kapton circles were used to mask the active area of the consequent solar cells, unmasked areas were etched in a 2 % HF solution and in the poly silicon etch to locally remove the ITO and the a-Si:H(i,p$^+$) emitter. The absorber contacts are formed by thermal evaporation of a 5/200 nm Ti/Ag layer stack. Finally, the Kapton circles are carefully removed to unmask the active area of the solar cell.

The resulting solar cells are measured in substrate configuration with a sun simulator and the basic cell parameters are derived. Moreover, selected samples are cut into 5·5 mm² specimens and are coated with silver contacts to measure the doping concentration and carrier mobility at room temperature with a Van der Pauw Hall setup. Additionally, several transient PL measurements are performed to calculate the average minority carrier lifetime of the material as described in literature [19]. Excitation source for the measurements is a 500 nm dye laser with a spot size of approximately 100 µm, a laser fluence of 11 µJ and a pulse duration of 3 ns. For detection, a silicon avalanche photodiode and a digital oscilloscope with ns time resolution are used.

## 3 Results and Discussion

### 3.1 Substrate selection

Five soda-lime glass (SLG) substrates were investigated, which are significantly lower in price than the two technical glasses (TG) already established for the LPC process and which, according to the manufacturer, exhibit an enhanced transmission compared to conventional soda-lime glass (e.g. window glass). Furthermore, the thermal and optical properties were characterized to identify the most suitable SLG substrate.




| ID | $T_{max}$ (°C) |
|---|---|
| TG 1 | 640 |
| TG 2 | 700 |
| SLG 1 | 550 |
| SLG 2 | 600 |
| SLG 3 | 650 |
| SLG 4 | 550 |
| SLG 5 | 550 |

*Figure 1: The general temperature profile (graph) applied to all investigated substrates and the maximum temperature values (table) of the individual substrates experimentally determined by successive repetition of the experiment until substrate deformation is observed.*

The graph in Figure 1 depicts the general temperature profile applied to all investigated substrates. The profile starts with a fast heat-up ramp of 20 K/s until a temperature of 400 °C is reached. Subsequently a second heat-up ramp of 1 K/s is applied until the temperature $T_{max}$ is reached. Afterwards $T_{max}$ is kept constant for an idle-time of 10 minutes before the system is switched off cooling down with rates of up to 5 K/s. The heat-up ramps simulate the later deposition environment of the precursor layers, while the idle temperature $T_{max}$ determines the maximum temperature that can be applied before damaging the substrates. $T_{max}$ of the individual substrates was determined by successive repetition of the experiment at increasing temperatures until a deformation of the substrate by gravitational bending is observed.

The table of Figure 1 shows the experimentally determined $T_{max}$ of two technical glass substrates and five low cost, low iron soda-lime glass substrates. The TG-substrates exhibit a high temperature stability of 640 °C and 700 °C, while the SLG-substrates are already damaged by deformation at temperatures as low as 550 °C. Only exception is the third SLG-substrate, which has similarly good thermal properties as the technical glasses with a $T_{max}$ of 650 °C.

The deposition temperature is a critical parameter and is limited by the $T_{max}$ of the individual substrates. Raman measurements of silicon thin films crystallized on technical glass substrates have shown that the crystallinity of the as-deposited silicon layers increases from approximately 0 % up to 80 % and 95 % at deposition temperatures of 200, 400 and 600 °C, respectively. This was accompanied by a minor increase of the tensile strain of the silicon layers after deposition due to an expansion coefficient mismatch between the TG substrates and the silicon layers. Most importantly however, it was shown that elevated deposition temperatures are beneficial for the resulting material quality after the liquid phase crystallization process, as not only the crystal growth was improved but also pinholes and micro-cracks were avoided [20].

In Figure 2, the results of the optical measurements of the substrates in the wavelength range between 300 nm and 1200 nm are plotted for the reflectance (grey) and the absorbance (white) as the integrated relative loss. The reflection of all substrates is very similar with approximately 8 % on average. Exceptions are the TG-1, which convinces with only

7 % average reflection. In strong contrast, the SLG-5 substrate had an elevated reflection of 11 % on average. For absorption, the TG substrates perform best with values below 1 %, while only two of the SLG substrates reached similarly good values. The other three SLG substrates had a parasitic absorption greater than 3 %. Since all substrates had a thickness of roughly 3 mm except for the TG-2, which was 1.1 mm thick, the absorption curves can be directly compared.

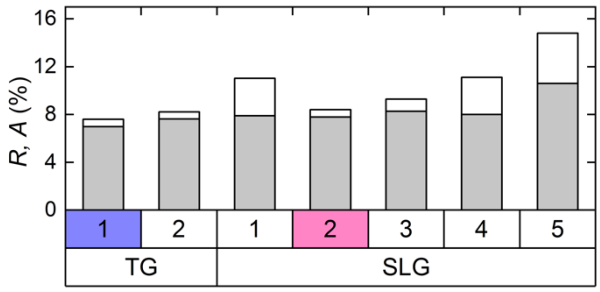



*Figure 2: shows the integrated (gray) reflectance R and (white) absorbance A in the wavelength range of 300 nm to 1200 nm for 2 technical glass (TG) and 5 low cost low iron soda-lime glass (SLG) substrates. The blue and red box mark the best performing substrate within each category.*

Figure 3 shows the spectral reflectance (left graph) and absorbance (right graph) for the best performing TG-substrate (blue curve) and SLG-substrate (red curve). Due to the slightly increased refractive index of SLG-substrates in general, the reflection curves are uniformly shifted. In case of the SLG-2 this shift is approximately 1 % (absolute) towards higher values compared to the TG-1. The absorption on the other hand is almost identical in the range of 300 - 600 nm but increases for the SLG-2 in the near infrared range. This broad and strong increase in absorption is caused by non-oxidized divalent iron [21,22]. Even though all of the SLG-substrates are supposed to be low iron substrates, we still observe severe differences between them.

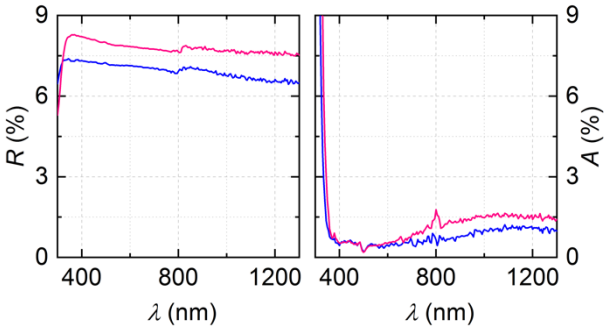



*Figure 3: (left) Reflectance R spectra and (right) absorbance spectra A of the best performing technical glass substrate TG-1 (blue curve) and low cost, low iron soda-lime glass substrate SLG-2 (red curve) of Figure 2.*

### 3.2 LPC-Process

Based on the results presented above we decided to use SLG-2 for further investigations. This low iron soda-lime glass from Saint Gobain glass named SGG Diamant was selected not only for its good optical and thermal properties, but also as it is one of the cheapest SLG-substrates in our comparison with one order of magnitude below the cost of the TG-substrates. SLG-3 is also a promising candidate but was put aside for further investigations due to a higher price. As a reference, we co-processed in all subsequent experiments the TG-1 substrate from SCHOTT Technical Glass Solutions named Borofloat 33.

First of all, we reduced the temperatures of the intermediate layer deposition from 600 °C to 500 °C and the silicon precursor deposition from 635 °C to 450 °C. Those temperatures were chosen based on the determined $T_{max}$ values of the SLG-2 (refer to Figure 1). The buffer of approximately 100 °C is used to protect the deposition tool and substrates from any possible damages.

We deposited silicon precursor layers of $d$ = 6, 8, 10 and 12 µm thickness. Subsequently the ability to laser crystallize the as-deposited layers was tested. The commonly used substrate pre-heating temperature ($T_{sub}$) of 700 °C was reduced to 600 °C, while the optical laser intensity ($I_{opt}$) and the scanning velocity ($v_{scan}$) were varied to determine the LPC process window for all investigated thicknesses.

Figure 4 depicts the phase diagram for the crystallization of a 6 µm thick silicon layer (left graph) and a 12 µm thick silicon layer (right graph). The diamonds indicate the threshold intensity to initiate the LPC process, while the squares display the upper intensity limit before dewetting of the silicon occurs. As expected, the $I_{opt}$ needs to be raised as $v_{scan}$ increases. The material thickness in turn has only a minor influence on the processing parameters due to the nonlinear absorption of the IR-laser light within the silicon layer. At elevated scanning velocities, we even observe a larger intensity range with a higher maximum intensity for the 6 µm thick layers.

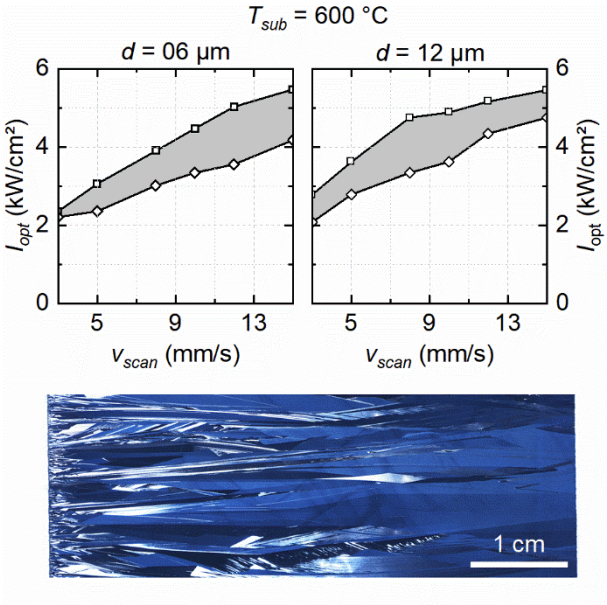



*Figure 4: Phase diagram for the crystallization of (left) 6 µm and (right) 12 µm thick silicon on SLG-2 substrates. Prior to crystallization the temperature of the specimens was set to 600 °C. The optical laser intensity ($I_{opt}$) is depicted as a function of the scanning velocity ($v_{scan}$). The diamonds and squares outline the process window for obtaining multi crystalline Si films with large crystal grains (grey region).The micrograph (bottom) exemplarily depicts a textured 12 µm silicon layer on a TG-1 substrate to visualize the resulting crystal structure after LPC processing. Crystallization was performed from left to right.*

Former experiments have shown that the crystallization parameters effect the final material quality [23]. In detail especially slow $v_{scan}$ improve the microstructural properties of

the silicon layer. On the other hand, the substrates are exposed to a higher thermal load as $v_{scan}$ is reduced and will eventually be damaged. While TG-substrates can be crystallized with $v_{scan}$ as low as 1 mm/s, SLG-2 substrates are already damaged at scanning velocities of $v_{scan}$ < 3 mm/s. Thus, substrate damage represent a fundamental limitation on the process window.

After the boundary conditions and the process windows have been determined, SLG-2 specimens and TG-1 references were fabricated with the thicknesses described before and crystallized at different scanning velocities of $v_{scan}$ = 3, 5, 8, 10, 12, 15 mm/s, while the laser intensity was adjusted to the lower crystallization threshold intensity to protect the substrates from unnecessary thermal load. However, it turns out that occasional spalling of the silicon layer (sometimes even attached to a few microns of glass) occurs shortly after the crystallization process. This island like spalling increases with time after crystallization of the samples. Figure 5 depicts a 12 µm silicon layer on a SLG-2 substrate crystallized at $v_{scan}$ = 5 mm/s. The micrograph exemplarily shows the silicon glass sample after $t$ = 1, 24, 168 h.

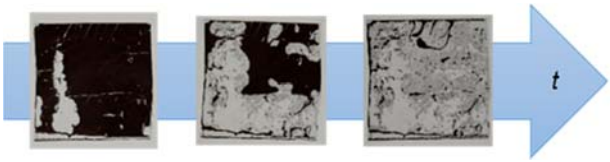



*Figure 5: Micrograph of a 12 µm silicon layer on a SLG-2 substrate crystallized with an 808 nm continuous wave line laser at a scanning velocity of $v_{scan}$ = 5 mm/s. The images were recorded 1 h, 1 day and 1 week after LPC-processing. The sample size was approximately 5 cm².*

A more comprehensive summary of all results is depicted in Figure 6. It shows the adhesion properties of all investigated thicknesses and scanning velocities as a function of the storage time of the samples after processing. Samples with excellent adhesion are marked violet, while occasional spalling is marked yellow and an almost complete peel-off is marked red.

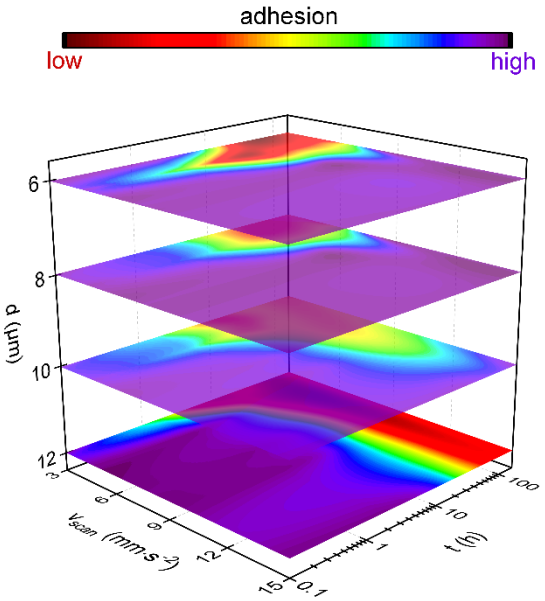



*Figure 6: Adhesion properties of laser crystallized silicon with thickness (d) on a SLG-2 substrate as a function of the scanning velocity of the laser ($v_{scan}$) and the sample storage time after crystallization (t).*

As can be seen in Figure 6, the 12 µm thick Si layers peeled-off from the SLG-2 substrate at the latest after one day, although they showed no signs of it directly after crystallization, with the exception of the samples crystallized at $v_{scan}$ = 3 mm/s. At a smaller thickness of $d$ = 10 µm the $v_{scan}$ = 15 mm/s had a high adhesion independently of the storage time. However, at lower $v_{scan}$ spalling is observed, which initiates earlier and becomes more severe as the scanning velocity is lowered. A further reduction of the silicon thickness to 8 µm increases the range of high adhesion. While directly after crystallization all $v_{scan}$ worked, layers crystallized at 3, 5 and 8 mm/s still peeled-off or at least showed occasional spalling after a few days. At a layer thickness of 6 µm this general trend maintained even though scanning velocities of 8 mm/s became accessible for material crystallization.

In summary, contrary to technical glass soda-lime glass exhibits spalling after crystallization. Spalling decreases with increasing laser scanning velocity and decreasing silicon thicknesses. As the expansion coefficient mismatch between the glass substrate and the silicon coating (the expansion coefficient of silicon is $\alpha_{Si} \sim 2.6 \cdot 10^{-6} \mathrm{K}^{-1}$) is much larger for soda-lime glasses ($\alpha_{SLG} \sim 8.5 \cdot 10^{-6} \mathrm{K}^{-1}$) compared to technical glasses ($\alpha_{TG} \sim 3.3 \cdot 10^{-6} \mathrm{K}^{-1}$) we attribute the SLG adhesion problems to a thermal expansion mismatch as a root cause. This is for example indicated by decreasing spalling effects at higher laser scanning velocity due to decreasing energy input per time which minimize mismatches and thermal stresses between substrate and silicon.

For future applications of silicon on low cost SLG substrates the following avenues for improvement are available:

(a) A further reduction of the silicon thickness to improve the adhesion and thus provide a larger process window.
(b) The optimization of the intermediate layers towards a stress reducing buffer layer to enable the crystallization of thicker silicon layers and provide a larger process window.
(c) Thermal post-crystallization treatment to subsequently reduce the stress and thus ensure improved adhesion.
(d) Selection of a SLG with a better matching thermal expansion coefficient without being more expensive than the usual market price for SLG.

The application for silicon on SLG will eventually determine which measures are most suited to improve adhesion. For example, the application “solar cell” will discourage avenue (a) in order to keep the absorption of sun light inside the silicon layer high and focus on avenues (b) and (d), while avenue (c) although technically possible is likely to increase costs and therefore appears less attractive for this application.

### 3.3 Solar cells

As a consequence of the decreasing adhesion with increasing silicon thickness first devices were fabricated on a 6 µm thick silicon absorber crystallized at $v_{scan}$ of 8, 10 and 15 mm/s. We measured the open circuit voltage ($V_{OC}$) with the sun simulator. The $V_{OC}$ depends on the photo current ($J_{SC}$) and the dark saturation ($J_0$) current. While the latter is a measure of the recombination in the solar cell and may change by orders of magnitude the $J_{SC}$ typically only changes within a small range. Therefore, the $V_{OC}$ is besides the $J_0$ a good indicator for the assessment of the electrical material quality.

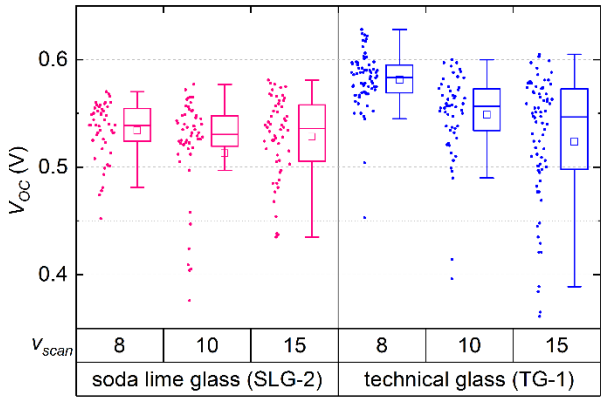



*Figure 7: Open circuit voltage ($V_{OC}$) of solar cells fabricated on a (left) SLG-2 substrate and a (right) TG-1 substrate. The crystallization of the 6 µm absorber layers were performed with an 808 nm continuous wave line laser operated at scanning velocities of $v_{scan}$ = 8, 10, 15 mm/s. Prior to crystallization the temperature of the specimens was set to 600 °C.*

Figure 7 depicts the measured $V_{OC}$ values of solar cells fabricated either on a SLG-2 (left) or on a TG-1 (right) substrate as a function of $v_{scan}$. Each sub-category consists of 50+ cells to have a reliable statistic. The average $V_{OC}$ of the cells processed on the SLG-2 substrate were 534, 513 and 528 mV for $v_{scan}$ of 8, 10 and 15 mm/s respectively. Peak values were almost identical with 580 ± 9 mV. The cells processed on a TG-1 substrate exhibited average $V_{OC}$ of 581, 549 and 524 mV. The best $V_{OC}$ results were achieved at 8 mm/s with values of up to 628 mV. Although the average $V_{OC}$ at $v_{scan}$ = 15 mm/s is comparable on the respective substrates, the difference increases continuously up to 47 mV at a $v_{scan}$ of 8 mm/s. So, while the material quality of the TG-1 substrate improves and the standard deviation decreases as the scanning velocity of the laser is reduced there is no specific trend observed for the cells fabricated on SLG-2 substrates. Neither the average values nor the standard deviations are affected by the crystallization velocity in stark contrast to LPC-processed devices on technical glass substrates [23]. It is likely, that the absence of this usual trend for liquid phase crystallized absorbers is caused by the expansion coefficient mismatch between substrate and silicon.

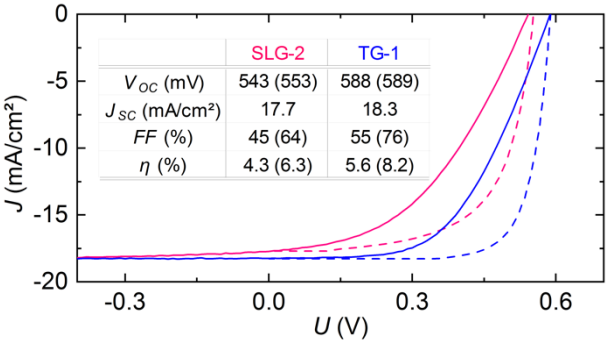



*Figure 8: Representative current-voltage characteristic of a solar cell processed on a (red curves) SLG-2 substrate and a (blue curves) TG-1 substrate. The solid lines indicate the results of the sun simulator while the dashed lines have been measured using the SunsVoc method. The table inset lists the cell characteristics with the SunsVoc values in brackets.*

Figure 8 depicts a representative IV-curves of solar cells processed with a scanning velocity of 8 mm/s on a SLG-2 (red) and a TG-1 (blue) substrate. The solid lines have been measured with a sun simulator, while the dashed lines are the corresponding SunsVoc curves. The table inset of Figure 8 lists the characteristic values of each cell and in brackets the results of the SunsVoc measurement.

Both, the cell on the SLG-2 and the one on the TG-1 substrate have a $V_{OC}$ near the average with values of 543 mV and 588 mV, respectively. Due to the lack of any light trapping features and an absorber thickness of 6 µm the $J_{SC}$ only reaches values of 17.7 mA/cm² and 18.3 mA/cm². The fabricated cells possess an inherently high series resistance due to the simple cell design with the absorber contacts outside of the active cell area. This leads to a poor fill factor of 45 % and 55 % for the SLG-2 and the TG-1 cell and results in an efficiency of 4.3 % and 5.6 % respectively. The fill factor difference between the sun simulator and SunsVoc measurement provides the loss caused by the aforementioned series resistance [24,25]. The difference in fill factor is comparable for the cell processed on a SLG-2 and on a TG-1 substrate and amounts to 19 % and 21 %, respectively. This is expected as the device structure of both is identical. The efficiency potential without series resistance amounts to 6.3 % and 8.2 %. In addition to the increased series resistance, a low shunt resistance is observed for the cell on a SLG-2 substrate, which in addition to the lower $V_{OC}$ leads to the lower performance compared to the cell on the TG-1 substrate.

*Table 1: Average carrier density ($N_{Hall}$), Hall mobility ($\mu_{Hall}$) and effective minority carrier lifetime ($\tau_{PL}$) of a silicon layer crystallized at 8 mm/s on either a SLG-2 or a TG-1 substrate.*

| | SLG-2 | TG-1 |
|---|---|---|
| $N_{Hall}$ (cm$^{-3}$) | 1.9·10$^{17}$ | 1.8·10$^{17}$ |
| $\mu_{Hall}$ (cm²/V·s) | 286 | 407 |
| $\tau_{PL}$ (ns) | 112 | 180 |

The corresponding material properties of the 8 mm/s crystallized layers were determined by Hall and transient PL measurements. From the measurements, we derived the majority carrier density ($N_{Hall}$), Hall mobility ($\mu_{Hall}$) and the effective minority carrier lifetime ($\tau_{PL}$) as shown in Table 1. Each value is the average of five measurements taken at different sites of the specimens. According to the Hall measurements, the carrier density is in the range of 1.8 – 1.9·10$^{17}$ cm$^{-3}$ independently of the utilized substrate. This indicates that the intermediate layer successfully prevents the diffusion of impurities from the soda-lime glass substrate into the silicon, even though the content of possible contaminants within the SLG substrates in general is increased compared to technical glasses.

The Hall mobility values of the silicon layers crystallized on a SLG-2 substrate are 30% lower as those crystallized on the TG-1 substrate. According to the Caughey model [26] we reach values of 50 % of the maximum mobility compared to mono crystalline silicon for the SLG-2 and 70% for the TG-1 substrate, respectively. The same trend is observed for the $\tau_{PL}$. While the average $\tau_{PL}$ on a SLG-2 substrate is 112 ns it increases to 180 ns on a TG-1 substrate. The low lifetime is expected [27] since the determined carrier concentration is high.

## 4 Summary

From a cost perspective, the LPC technology transfer to soda-lime substrates has been a huge leap towards applications which require high quality material at low costs. The parameter space to fabricate the multicrystalline silicon thin films on a soda-lime

substrate is robust and offers a wide processing range. Nevertheless, there are further investigations required to address the encountered problems caused by the thermal expansion coefficient mismatch. Doing so could improve the adhesion of the silicon layers to crystallize silicon films beyond 10 µm thickness and provides the opportunity to process the material at scanning velocities below 8 mm/s.

Although the general feasibility has been demonstrated, it will be inevitable for photovoltaic application to integrate light trapping features and to refer to thicker layers by further investigating the avenues presented in section 3.2. In addition, the origin of the reduced material quality in terms of lower Hall mobility's, shorter effective minority carrier lifetimes and the generally lower $V_{OC}$ of cells processed on SLG-compared to TG substrates needs to be investigated in order to achieve comparable values as the case on the established technical glass substrates.

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