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Receptores de rádio-frequência melhorados e disruptivos

Enhanced and Disruptive Radio-Frequency Receivers

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Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Eletrotécnica, realizada sob a orientação científica do Prof. Doutor Arnaldo Silva Rodrigues de Oliveira, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e do Prof. Doutor Nuno Miguel Gonçalves Borges de Carvalho, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Dedico este trabalho à minha família, e em especial à minha avó.

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Palavras-Chave

Rádios Definidos por Software (SDR), Recetores Digitais, Conversores Analógico-Digital (ADCs), Pré-distorção Digital (DPD), Agregado de Células Lógicas Programáveis (FPGA)

Resumo

Este doutoramento endereça principalmente a componente de receção de um transcetor de rádio-frequência (RF), focando-se em arquiteturas de receção de amostragem em RF. Estas são assim consideradas como sendo as mais promissoras para o futuro, em termos de desempenho, largura de banda e agilidade, de acordo com o conhecido conceito de Rádios Definidos por Software (SDR). O estudo considera o uso dos recetores de RF em modo *standalone*, i.e., recebendo dados desconhecidos provenientes da antena, e também quando usados como caminho de observação para aplicação de linearização de amplificadores de potência (PAs) via pré-distorção digital (DPD), pois atualmente esta é uma técnica fundamental para aumentar o desempenho geral do sistema.

Em primeiro lugar, os conversores analógico-digital de RF são estudados e caracterizados para perceber as suas limitações quando usados em cenários de DPD. Um método de caracterização e pós compensação digital é proposto para obter melhorias de desempenho.

Em segundo lugar, um novo recetor pulsado de um bit baseado em Modulação de Largura de Pulso (PWM) e implementado em Agregado de Células Lógicas Programáveis (FPGA) é endereçado, visando agilidade em frequência, largura de banda analógica e integração de sistema, tirando proveito da implementação em FPGA. Este recetor foi otimizado com base no modelo comportamental teórico da modulação PWM, maximizando a relação sinal-ruído (SNR) e a largura de banda. O recetor otimizado foi posteriormente avaliado num cenário 5G de uma arquitetura C-RAN e também num cenário em que serve de caminho de observação para DPD.

Finalmente, um breve estudo relativo a caminhos de observação de DPD no contexto de transmissores multi-antena é também apresentado.

Este doutoramento contribui com vários avanços no estado da arte de recetores SDR e no conceito de SDR DPD.

Keywords

Software Defined Radio, Digital Receivers, Analog-to-Digital Converters, Digital Predistortion, Field Programmable Gate Array

Abstract

This Ph.D. mainly addresses the reception part of a radio front end, focusing on Radio Frequency (RF) sampling architectures. These are considered to be the most promising future candidates to get better performance in terms of bandwidth and agility, following the well-known Software-Defined Radio (SDR) concept. The study considers the usage of an RF receiver in a standalone operation, i.e., used for receiving unknown data at the antenna, and when used as observation path for Power Amplifier (PA) linearization via Digital Predistortion (DPD), since nowadays this represents a mandatory technique to increase overall system's performance.

Firstly, commercial available RF Analog-Digital-Converters (ADCs) are studied and characterized to understand their limitations when used in DPD scenarios. A method for characterization and digital post-compensation to improve performance is proposed and evaluated.

Secondly, an innovative FPGA-based RF single-bit pulsed converter based on Pulse Width Modulation (PWM) is addressed targeting frequency agility, high analog input bandwidth, and system integration, taking profit of an FPGA-based implementation. The latter was optimized based on PWM theoretical behavior maximizing Signal-to-Noise-Ratio (SNR) and bandwidth. The optimized receiver, was afterwards evaluated in a 5G C-RAN architecture and as a feedback loop for DPD.

Finally, a brief study regarding DPD feedback loops in the scope of multi-antenna transmitters is presented.

This Ph.D. contributes with several advances to the state-of-the-art of SDR receiver, and to the so-called SDR DPD concept.

Contents

List of Figures

List of Tables

List of Acronyms

2-D	Two Dimensional
ACPR	Adjacent Channel Power Ratio
ADT	All-Digital Transmitters
ADC	Analog to Digital Converter
AWG	Arbitrary Waveform Generator
BER	Bit Error Rate
CAPEX	Capital Expenditures
CU	Central Unit
C-RAN	Centralized-Radio Access Network
CM	Cross-Modulation
CO-MPM	Cross-Over Memory Polynomial Model
DSM	Delta Sigma Modulation
DDS	Digital Direct Synthesizer
DDC	Digital Down-Conversion
DPD	Digital Predistortion
D-RoF	Digital Radio-over-Fiber
DSP	Digital Signal Processor
DAC	Digital to Analog Converter
DUC	Digital Up-Conversion
DCR	Direct Conversion Receiver
E/O	Electro/Optical
EVM	Error Vector Magnitude
FPGA	Field Programmable Gate Array
FoM	Figures of Merit
FIR	Finite Impulse Response
GMPM	Generalized Memory Polynomial Model
IC	Integrated-Circuit
IF	Intermediate Frequency
IMD	Intermodulation Distortion
LS	Least Squares
LC	Linear-Crosstalk
LO	Local Oscillator
LUT	Lookup Table
LNA	Low Noise Amplifier
LPE	Low Pass Equivalent
LB	Lower Band
M2M	Machine to Machine Communications

MPM	Memory Polynomial Model
MGT	Multi Gigabit Transceiver
MIMO	Multiple-Input Multiple-Output
MS	Multi-sine
NLC	Non-Linear-Crosstalk
NCO	Numerical Controlled Oscillator
NZ	Nyquist Zone
OPEX	Operational Expenditures
PA	Power Amplifier
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
QoE	Quality of Experience
QoS	Quality of Service
RF	Radio Frequency
RoF	Radio-over-Fiber
RRH	Remote Radio Heads
SIPO	Serial In- Parallel Out
SNR	Signal to Noise Ratio
SISO	Single-Input Single-Output
SFP	Small Form-factor Pluggable
SDR	Software Defined Radio
SEC	Stochastic Ergodic Converter
SAR	Successive Approximation Register
SMPA	Switched Mode Power Amplifier
SoC	System-on-Chip
UB	Upper Band
VGA	Variable Gain Amplifier
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
VHDL	VHSIC Hardware Description Language
VCO	Voltage Controlled Oscillator

1. Introduction

1.1. Background and motivation

Since the beginning of this century, a phenomenal growth of mobile communications standards and technologies has been witnessed. Currently, this unprecedented growth is being mainly driven by the huge amount of bandwidth required to answer to the costumers' strong demands on video and multimedia services. To support this ever increasing bandwidth requirements, several successive generations of mobile communications standards have been deployed, from the highly successful GSM (2G) to the current 4G or LTE-A networks. However, currently low power and low bitrate communications are needed for the implementation of the so-called Internet of Things (loT) and, at the same time, very high speed communications are required for the bandwidth-hungry multimedia services. These aspects are two of the main driving forces for the development of the next generation of mobile networks: the so-called 5G. Although many technological aspects are still under debate for the next generation mobile communications it is expected to be delivered around 2020. 5G networks will act as an integrator of the previous standards and it will create a new paradigm in which there will be coexistence of ultra-low power and low-bit rate communications (IoT) with high data rate communications (100Gbps) under high Quality of Service (QoS) and high Quality of Experience (QoE) constraints [1].

In fact, according to current trends, and in addition to the required high data rates, 5G networks will be characterized by cooperative operation between different technologies and heterogeneous networks, denser base station deployments, improved power efficiency and higher levels of connectivity among devices to support the IoT. Therefore, the telecommunications' academia and industry are searching for solutions to deploy 5G networks in an efficient way, capable to answer the previous requirements without significant additional Capital Expenditures (CAPEX) and Operational Expenditures (OPEX) costs for the operators [1]. Several technologies, such as C-RAN (Cloud-Radio Access Network) and small/pico-cell deployment, Massive-MIMO, Software Defined Radio (SDR) and mm-Wave are being pointed out as promising enablers of 5G networks covering a wide range of research topics [1], [2].

Nonetheless, and even considering that the technological characteristics of 5G are still not completely defined, there are key requirements that are common to any past and future standard such as: medium/high power capability, energy efficiency, linearity, bandwidth, radio-frequency (RF) agility in terms of transmission carrier, multi-standard capability, integration/miniaturization and last but not the least important, cost of the devices. All these aspects are constant key optimization targets of the communications sector, mainly in the radio field, which is the focus of this Ph.D. thesis. Regarding these requirements, high power, linearity and efficiency are always highly correlated aspects,

due to the challenges associated with the design of linear and efficient power amplifiers (PAs) [3], [4]. To increase efficiency, PAs are usually operated close to their compression point, which creates non-linear distortion, generating new frequency components (that cannot be radiated) and degrading the in-band signal information. Due to this, techniques of pre-distortion and linearization are often employed, either implemented in digital or analog domain, to simultaneously achieve a linear and efficient system [5]–[7]. This, together with bandwidth and frequency agility are typically the most important metrics in an RF transmitter. On the other hand, receiver's most critical characteristics are usually dynamic range, sensitivity, frequency agility and bandwidth. The dynamic range is fundamental to define the receiver's maximum achievable signal-to-noise ratio (SNR) and the sensitivity allows to characterize the minimum signal power that can be successfully decoded at the receiver's antenna. Both these characteristics strongly depend on the Low Noise Amplifier (LNA). Bandwidth and agility are common key points shared between a transmitter and a receiver and are both associated with the well-known Software Defined Radio (SDR) concept introduced by Mitola in [8], which despite being an already old concept, still represents a challenge. The SDR concept envisions a radio in which high bandwidth waveforms can be completely designed in the digital domain and converted directly into the analog domain at a given carrier frequency (f_c) also defined in the digital domain, using high speed digital-to-analog converters (DACs). The same is also valid for the receiver, in which a high bandwidth analog-to-digital converter is used to directly sample the RF signal and to, afterwards, apply all the required signal processing tasks in the digital domain. Currently, SDR transmitters are usually implemented recurring to commercial high speed RF DACs [9], however all-digital transmitters (ADTs) based on pulsed converters [10] represent an important research field, since they are associated with high efficient PA topologies [11] and also due to the high integration that these converters enable. Regarding SDR receivers, usually their design is also performed with resort to RF ADCs [9], however digital topologies based on pulsed converters are also being addressed by academia [12]. Within the SDR topic, digital signal processing devices such as common Digital Signal Processors (DSPs) and Field Programable Gate Arrays (FPGAs) play a very important role, since they provide powerful processing capabilities to handle and process the high bandwidth signals. In fact, in the case of FPGAs, these may be even more important due to the fact that nowadays they are already being used to design integrated SDR transmitters [13]. Figure 1 presents a block diagram of an SDR-based radio-frequency transceiver, which uses an additional receiver as observation path (or feedback loop) for digital predistortion (DPD).

By inspecting Figure 1, one may realize that receiving RF chains are not only used to receive the unknown data that arrives at the antenna, but also to perform PA linearization through DPD, which highlights the RF receiver importance from the system point of view. As already referred previously, DPD is a technique of PA linearization allowing its operation in compression without degrading the signal quality and with benefits of improved efficiency. This technique is based on behavioral modeling, i.e., it requires a set of signals corresponding to the PA input and output *x(t)* and *y(t)*,

respectively, as represented in Figure 1. Due to this reason, an additional receiver (known as observation path or feedback loop) is required to acquire a replica of the PA output *z(n)* and allow the extraction of a behavioral model to characterize and subsequently pre-compensate the PA. As in the case of a normal receiver, the previous highlighted characteristics are also equally important, with exception for the sensitivity since in this case the signal´s power at the output of the PA is high. However, in this type of application, the original signal before the PA is known (*x(t)*), which is an extremely important information that can be used to relax some of the feedback loop requirements. Additionally, as referred in [5], [6] this type of systems should follow the SDR disruptive trends, to reach the so-called SDR DPD system with minimal RF sub-system design and higher integration, through the use of high speed RF converters.

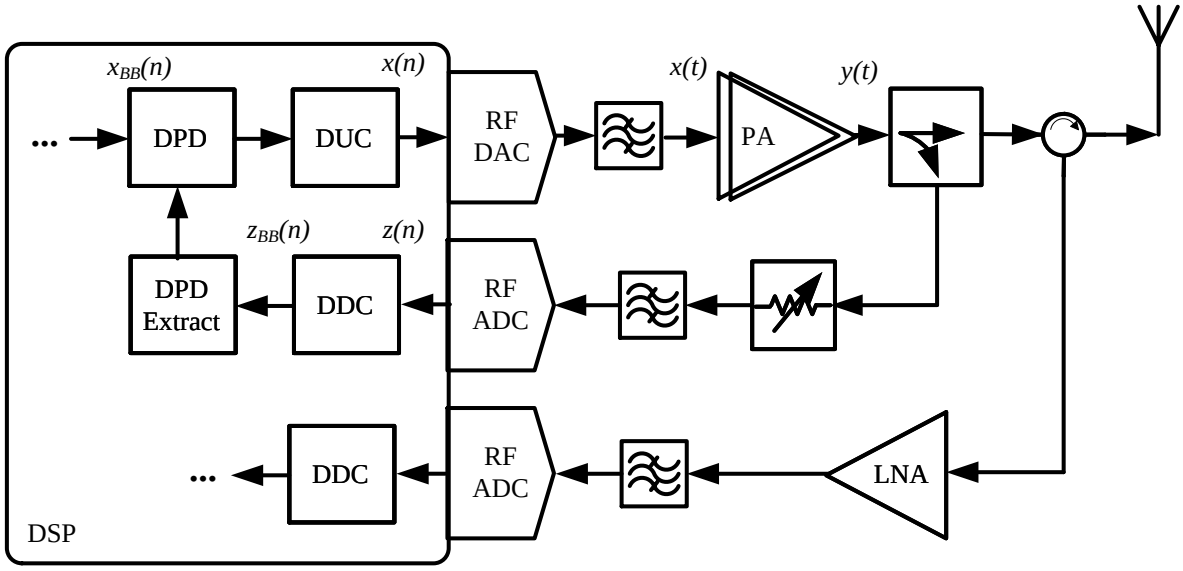


Figure 1 – Block diagram of a conventional radio transceiver based on SDR architecture, using high speed converters and an observation path for DPD.

In conclusion, the main research lines associated with this thesis will be the SDR RF receiver system design and optimization using conventional commercial RF converters and the exploration of disruptive architectures based on pulsed SDR receivers allowing for all-digital SDR platforms. The addressed receivers' target is the normal usage (standalone with antenna) and feedback loop in a DPD scenario, where the relaxation requirements can be further explored to bring costs and energy savings.

1.2. Objective

The purpose of this Ph.D. is to study innovative and disruptive ways to improve the most important Figures of Merit (FoMs) of current radio-frequency systems, mainly in the receiver side. However, as previously explained, a radio receiver is also strongly connected with the transmitter enhancement, mainly due to the linearization techniques using DPD

that require an observation path. Therefore, the main questions that this thesis should answer are:

- *"How can radio receivers be improved in order to provide increased performance to a standalone receiver?"*
    - In the scope of this question, disruptive architectures based on pulsed SDR receivers allowing for all-digital SDR platforms will be studied, designed and evaluated. The main target FoMs in this category are: Error Vector Magnitude (EVM), which is directly correlated with the signal's quality, signal's bandwidth (BW) and frequency agility in terms of carrier frequency.
- *[a]How can a radio receiver be improved to provide enhanced linear and energy efficient transmitters?"*
    - This second question can be seen as a study of the receiver's usage in a specific application scenario of PA linearization using DPD. The target of this study is to relax the requirements of the receivers typically used in DPD. In order to evaluate the proposed techniques in terms of receiver modifications it is important to evaluate metrics associated with DPD. Therefore in this context, it is important to evaluate not only EVM but also Normalized Mean Squared Error (NMSE) that allows to measure the error of the DPD behavioral model, and Adjacent Channel Power Ratio (ACPR), which allows to evaluate the transmitter linearity and to verify if the spectral masks imposed by the regulators are being met.

In short, the main objective of the work developed in the scope of this Ph.D. is to contribute to the advance of the state-of-the-art of SDR receivers capable to be used in a standalone scenario and as observation path for DPD.

1.3. Contributions

The work developed in this Ph.D. brought several contributions for the wireless systems communication community, in the fields of radio frequency receivers and DPD. The published papers, which are presented in the Appendix, strongly support the content of this thesis and are listed as follows:

- [C1] - A. Prata, D. C. Ribeiro, P. M. Cruz, A. S. R. Oliveira, and N. B. Carvalho, "Improving DPD performance by compensating feedback loop impairments in RF ADCs," in *2015 IEEE MTT-S International Microwave Symposium, IMS 2015*, 2015.
- [C2] - A. Prata, A. S. R. Oliveira, and N. B. Carvalho, "An agile and wideband all-digital SDR receiver for 5G wireless communications," in *Proceedings of 18th Euromicro Conference on Digital System Design*, DSD 2015, 2015.

- [C3] - A. Prata, A. S. R. Oliveira, and N. B. Carvalho, "FPGA-based all-digital Software Defined Radio receiver," in *2015 25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015, pp. 1–2.
- [C4] - R. F. Cordeiro, A. Prata, A. S. R. Oliveira, N. B. Carvalho, and J. N. Vieira, "FPGA-based all-digital software defined radio system demonstration," in *2015 25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015, pp. 1–1.
- [C5] - A. Prata, R. F. Cordeiro, D. C. Dinis, A. S. R. Oliveira, J. Vieira, and N. B. Carvalho, "All-digital transceivers — Recent advances and trends," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2016, pp. 233–236.
- [C6] - A. Prata, A. S. R. Oliveira, and N. B. Carvalho, "All-digital Flexible Uplink Remote Radio Head for C-RAN," in *2016 IEEE MTT-S International Microwave Symposium, IMS 2016*, 2016, pp. 1–4.
- [C7] - A. Prata, S. C. Pires, M. Acar, A. S. R. Oliveira, and N. B. Carvalho, "Towards Circulator-Free Multi Antenna Transmitters for 5G," in *2017 IEEE MTT-S International Microwave Symposium, IMS 2017*, 2017, , pp. 1–4.
- [J1] - A. Prata, D. C. Ribeiro, P. M. Cruz, A. S. R. Oliveira, and N. B. Carvalho, "RF Subsampling Feedback Loop Technique for Concurrent Dual-Band PA Linearization," in *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4174–4182, Dec. 2016.
- [J2] - A. Prata, J. C. Santos, A. S. R. Oliveira, and N. B. Carvalho, "Agile All-Digital DPD Feedback Loop," in *IEEE Trans. Microw. Theory Techn., vol. 65, no. 7, Jul. 2017.*
- [J3] - R. F. Cordeiro, A. Prata, A. S. R. Oliveira, J. M. N. Vieira, N. B. Carvalho, "Agile All-Digital RF Transceiver Implemented in FPGA," *in IEEE Trans. Microw. Theory Techn.*, vol. x, no. x, pp. 1–12, 2017.

The paper [C1] was the first publication during this Ph.D. work and is related with the study of the impairments of the feedback loop (receiver) in a DPD scenario. This work allowed to understand the main requirements in terms of flatness of the feedback loop, and how its correction can bring several gains in terms of performance. Following this work, the technique associated with paper [J1] was developed, which focuses on how a feedback loop based on RF sampling receivers can be optimized to allow the simultaneous linearization of a dual-band transmitters using a single feedback loop.

The paper [C2] and [C3] have shown the first steps towards an all-digital FPGA based fully integrated receiver, based on RF PWM. In short, these works allowed to demonstrate that is possible to build a highly flexible all-digital receiver using a single FPGA chip. The paper [C4] is a support of a conference live demonstrator of an all-digital transceiver totally implemented in FPGA. The paper [J2] arises as integration of an all-digital transmitter and receiver in the same FPGA chip, and proposing important

optimizing design methodologies for the receiver part, which allowed to improve the metrics obtained in [C2, C3 and C4]. The paper [C5] summarizes the last advances and current challenges in all-digital transceiver design. In [C6], the proposed receiver was evaluated in a C-RAN scenario, which is a very important topic for 5G networks. Finally, the paper [J3] evaluates the usage of the proposed FPGA-based all-digital RF PWM receiver in a DPD scenario, allowing to reach an agile feedback loop for DPD.

The last contribution was the paper [C7], which focuses on the problems associated with circulator-free multi-antenna transmitters and how to solve them by implementing a digital pre-compensation algorithm.

1.4. Document organization

The thesis document was organized in six main chapters as follows:

1. **Introduction**
   - The first chapter presents the background, motivation, main objective and document organization of this Ph.D. thesis.
2. **State-of-the-Art**
   - In the second chapter an overview of the state-of-the-art regarding SDR RF receivers based on conventional ADCs and pulsed architectures is presented. This chapter contains a system level overview about DPD, highlighting the importance of the receiver (observation path) in such application. Additionally, several important research topics that were addressed within Ph.D. work are identified in this chapter.
3. **RF ADCs enhancement in a DPD scenario**
   - In this chapter the first part of this Ph.D. work is addressed focusing on enhancing the DPD performance by using a suitable characterization and post-compensation of the feedback loop. Additionally, a technique to relax the feedback loop requirements in a dual-band transmission scenario is presented and evaluated.
4. **PWM RF receiver design and applications**
   - The fourth chapter of this thesis presents a disruptive RF PWM all-digital receiver based on FPGA. The receiver's design details are explained and its performance is evaluated in two application scenarios, which include the normal usage (standalone with antenna) and feedback loop in a DPD scenario.
5. **Integration and assessment of DPD feedback loops for multi-antenna systems**
   - In this chapter the last part of this Ph.D. research work is addressed, which focuses on one of the most important topics for 5G: the multi-antenna systems, in which integration and scalability are very important metrics to study and evaluate.
6. **Conclusion and future work**

- The last chapter concludes this thesis document and gives some insights regarding potential future work in this field from the author's point of view.

2. State of the Art

Considering that the focus of this work is on the receiving branch of a radio system it is important to give an overview of its architecture fundamentals from the most traditional ones up to the most recent and disruptive, which is done in the sub-section Traditional RF Receivers Architectures Overview.

Afterwards, a special focus on the RF sampling architectures using both commercial ADCs and pulsed architectures is given, since these are the ones that allow to reach higher flexibility, bandwidth and avoid the analog impairments.

Finally, this chapter is concluded with the application scenario of DPD, by highlighting the importance of the RF receiver in such system. Additionally, a brief overview over DPD concepts and PA linearization is also given.

2.1. Traditional RF receivers architectures overview

Usually, modern RF receivers applied in digital communications can be organized in three different topologies:

1. Direct conversion receiver (DCR), or zero-Intermediate Frequency (IF) receiver, uses an analog I/Q (in phase and quadrature components) demodulator to down convert the signal directly to base band followed by two ADCs to acquire the I/Q components (Figure 2 (a));
2. Down-conversion from RF to IF and IF sampling with digital I/Q down-conversion (DDC) (Figure 2 (b));
3. RF sampling receiver, in which the signal is directly digitized at the RF stage, followed by a fully digital DDC (Figure 2 (c)).

Figure 2 presents a block diagram of the three main categories of RF receivers. The first presented architecture (Figure 2 (a)), is probably the most widely used due to its versatility and acceptance for narrowband communications. However, this architecture comprises problems regarding the imbalance of the analog I/Q demodulator, Local Oscillator (LO) feedthrough, mixer non-linear behavior, and other impairments caused by the analog components such as non-flat gain and non-linear phase response. Nevertheless, some of these impairments may be solved with post-compensation in digital domain after a proper characterization and calibration procedure.

The second architecture (Figure 2 (b)), IF-sampling receiver, does not suffer from I/Q imbalance problems, since I/Q demodulation is performed in digital domain. When I/Q demodulation is digitally implemented, the process is usually known as digital down-conversion (DDC), in which the LO is now a Numerical Controlled Oscillator (NCO) or Digital Direct Synthesizer (DDS). In addition, to avoid the I/Q imbalance problem, the usage of a DDC allows for improved resolution in terms of down-conversion frequency. However, LO feedthrough, mixer non-linear behavior, as also non-flat frequency response

of the analog components are still present. In short, both first and second architectures have flexibility depending on the frequency range of the mixers, have limited bandwidth, and require compensation techniques to mitigate the imbalance as also other analog components non-ideal behavior.

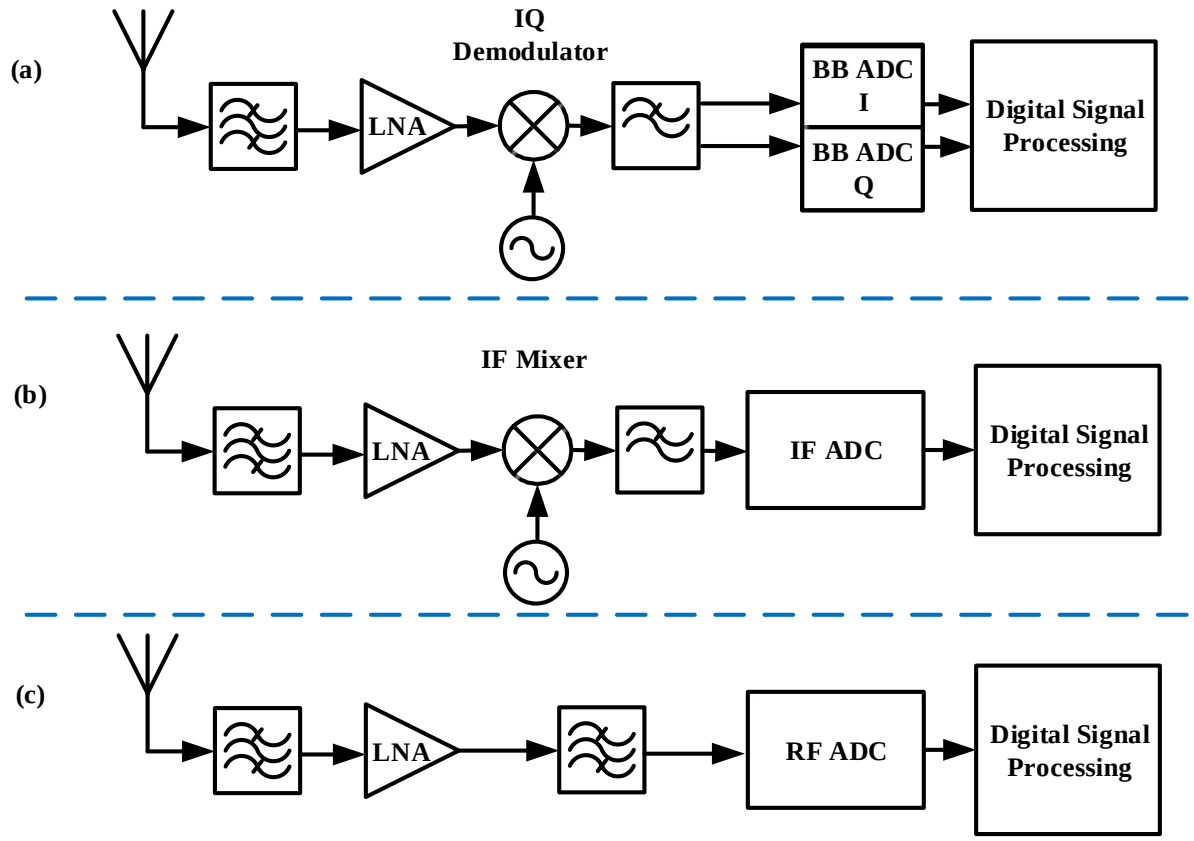


Figure 2 – Block diagram of conventional radio receiver architectures. (a): direct conversion receiver; (b): IF conversion receiver; (c): RF sampling receiver.

The final one (Figure 2 (c)) is closer to the ideal SDR concept [8], with reduced number of analog components and presenting high flexibility and also supporting wideband signals operation. Nevertheless, this architecture requires high-speed ADCs which may be expensive and may present high power consumption. In respect to flexibility and to cope with high bandwidth, this is the preferable architecture, taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches [14]. However, it is important to realize that this architecture may also present non-flat frequency response over a high operation bandwidth, which may require digital post compensation.

2.2. RF ADCs

According to the previous section, it can be understood that to achieve flexibility and wide bandwidth operation, the most suitable RF receiver is the RF sampling architecture, in which the analog-to-digital converter (ADC) is the fundamental system element. In this chapter, the RF ADCs are addressed and separated into two main groups, which are the general purpose commercial available RF ADCs and the pulsed ADCs based on Delta-Sigma Modulation (DSM), Pulse Width Modulation (PWM) or even Pulse Frequency Modulation (PFM).

2.2.1. Comercial RF ADCs

Current commercial RF ADCs have reached the order of a few GHz both in sampling frequency as in input bandwidth [15], [16]. These types of converters can be used in a wide range of applications such as multi-band and multi-mode RF receivers, cellular receivers, phased array radars, electronic warfare, broadband wireless, high-speed digitizers, microwave and millimeter-wave receivers, optical communications, among others. Usually, these wideband on-chip high speed converters are based on flash and interpolated folding architectures [17], which are known for allowing high sampling rates. Additionally, depending on the sampling frequency (f_s) and carrier frequency (f_c) location, these converters can be used in direct sampling ($f_s > 2f_c$ and $f_s > 2BW$) or in bandpass sampling ($f_s < 2fc$ *and* $f_s > 2BW$) configurations, which is a consequence of the well-known Nyquist Theorem [18]. Figure 3, presents a frequency domain illustration of the sampling process depending on the location of the carrier relatively to the sampling frequency, which imposes the Nyquist Zone (NZ) where the signal is sampled from [18]. One may realize that the blue signal (centered at f_{c1}) is originally sampled from the first NZ, while the orange signal (centered at f_{c2}) is sampled from the 3rd NZ, folding afterwards at the first NZ at f_{fold2}. The folding frequency is given by the following expression (1):

$$f_{fold} = \left| f_c - \left\lfloor \frac{f_c}{f_s} \right\rceil f_s \right| \tag{1}$$

where f_{fold} is the folding frequency in the 1st NZ, $|...|$ is the absolute value and $\lfloor ... \rceil$ is the rounding operation towards the nearest integer [19]. One may realize the importance of filtering requirements either in direct sampling and bandpass sampling in order to avoid aliasing effects [18].

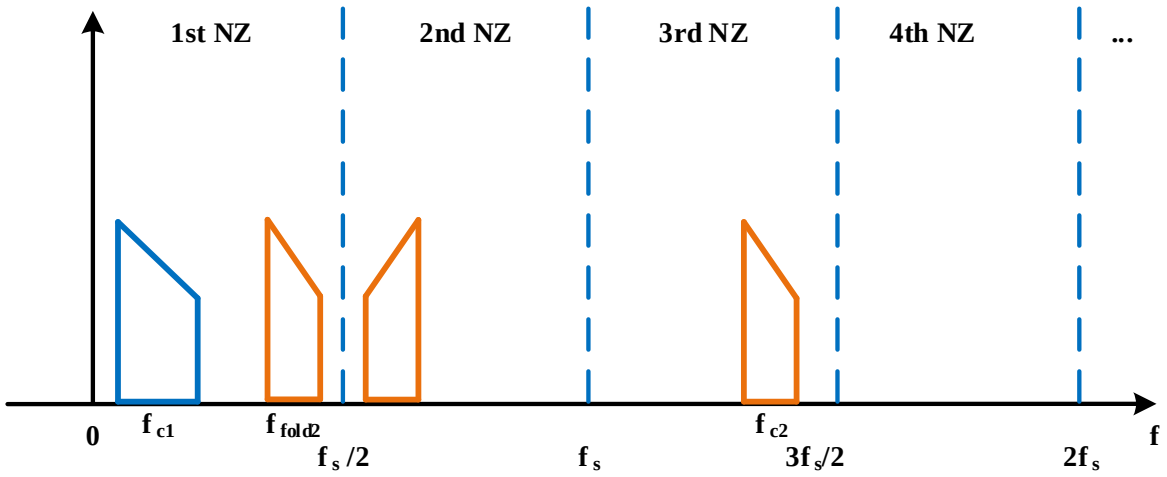
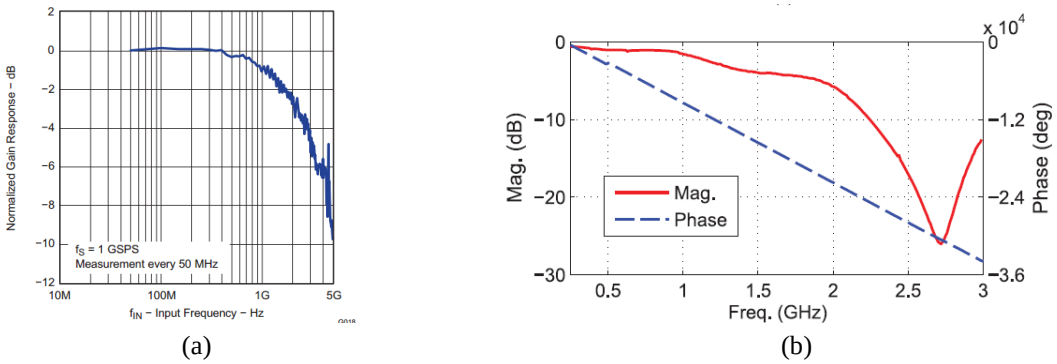


Figure 3 - Frequency domain illustration of the sampling process over different NZs.

To get the maximum performance over wideband operation, the behavior of these converters must be well understood through adequate characterization procedures. In [19]–[22] a measurement setup for linear and non-linear characterization of RF converters has been presented and intensively studied. The proposed measurement platform allows to perform a system characterization from the analog to the digital domain, in the case of ADCs and the opposite in the case of DACs. Interesting results were presented, in which allow to conclude that the performance over several NZs can be quite reasonable in terms of linearity, however presenting some gain non-flatness. Figure 4 presents the frequency response of a 1 GSample RF ADC (ADS5400) designed by Texas Instruments (TI) [23]. Figure 4(a) presents the magnitude response of the ADC presented in the device datasheet and measured by TI. Figure 4(b) presents the ADC evaluation board frequency response in both magnitude and phase measured following the procedures presented in [20]. Regarding the magnitude response, the 3 dB cutoff frequency seems to be similar in both graphs, i.e., around 2 GHz. At frequencies higher than 2 GHz the results from Figure 4(b) present a higher degradation, because it is a measurement of the evaluation board, including losses in the input balun, connectors and transmission lines, while in Figure 4(a) is presented an on chip device measurement. Additionally, it is important to note the phase measurement capability of the method presented in [20], and according to Figure 4(b) it is possible to verify that the RF ADC evaluation board presents a linear phase response.



(a) (b)

Figure 4 –Frequency response of RF ADC ADS5400 from TI [23]**. (a): Magnitude response presented by TI in** [23] **(figure taken from** [23]**). (b): Magnitude and phase response measured and presented in** [20] **(figure taken from** [20]**).**

Nevertheless, the previous non-ideal behavior will impose system performance degradation in terms of Error Vector Magnitude (EVM), demanding for digital equalization, i.e., pre-compensation in the DAC case and post-compensation in the ADC case. The study of the impact of such impairments when these receivers are used in DPD scenarios is one of the tasks of this Ph.D. work.

Last but not least, usually this type of converters are expensive and responsible for a considerable energy consumption reducing the overall system's efficiency [24]. This difference is even more evident when compared to the traditional baseband converters, as was analyzed in [24]. Furthermore, when it is necessary to reach frequencies higher than approximately 4 GHz it is necessary to choose mixer-based architectures, and it is not possible anymore to sample the signal directly with a RF ADC increasing even more the overall system's cost and bill of materials.

2.2.2. Pulsed architectures

As it has been seen so far, at the receiver side, to achieve flexibility and wider bandwidth in the RF chain, the ADC is of paramount importance, by allowing the use of digital signal processing techniques and avoiding analog impairments. In this sub-section analog-to-digital converters based on pulsed architectures, or single-bit converters, which represent a kind of disruptive topologies will be addressed.

Recently there are arising new possibilities to build RF ADCs: based on delta-sigma modulation (DSM) [12], pulse-width modulation (PWM) [25] or pulse frequency modulation (PFM) [26], [27]. All these types of ADCs share the common basis of being single-bit ADCs, i.e., they all deal with a digital pulsed representation of the analog signal. The DSM ADCs are well known in audio applications, where they provide very high resolution [14]. Some research is being done in order to apply these ADCs in the RF world, as presented in [12]. Even though good figures of merit that have been obtained in

[12], the need for a low latency feedback path can impose several limitations in terms of increasing the effective sampling frequency.

The PWM ADCs comprise a single comparator, whose inputs are the analog signal and a known reference (usually a triangular wave), generating a PWM representation of the signal [28]. They are commonly used in low-frequency power applications [28]. Nevertheless, recently they are also being brought to the RF world, as presented in [25]. However, the presented results reveal a weak signal-to-noise ratio (SNR) due to the PWM strong non-linear behavior and make use of high speed comparators, which are high cost components.

A PFM ADC is achieved using a Voltage Controlled Oscillator (VCO) as input for the analog signal [26]. These types of ADCs present high undesirable non linearities related to the VCO behavior, which have been addressed by the scientific community through the use of feedback loops or digital calibration [27].

Due to the highly digital intensive circuit topology of the previously described ADCs architectures they are all promising candidates for modern all-digital receivers' architectures. Additionally, since the previous described architectures have a strong foundation on pulse shaping modulations these topologies are very attractive to be implemented in an FPGA-chip, allowing for higher levels of integration and cost reduction. As already stated, one of the objectives of this Ph.D. work is to take profit of the powerful DSP FPGA capabilities as also its very high speed I/Os in order to build RF ADC converters recurring to the state-of-the-art FPGA chips, similarly to what has already been done for the transmitter case [13], [29], [30]. In fact, to the best of the author's knowledge, this will be the first work trying to build such a type of RF ADC converters using directly an FPGA chip, without any external components. Therefore, due to this reason, and because the PWM converters seem to be the most feasible approach to get such a type of integration, and, as well as to be able to focus on important application scenarios such as DPD, it was decided to focus exclusively in this type of converters. Therefore, the next sub-section addresses the PWM modulation process and presents the state-of-the-art of this type of converters, while the DSM and VCO can be seen as possible future work to follow this thesis.

2.2.2.1. RF-PWM converters working principle

An ADC comprises two main processes: sampling and quantization, corresponding to discretization in both time and amplitude, respectively. In this section the PWM ADC working principle will be addressed focusing in both of these aspects.

A PWM ADC is mainly based on a comparison between two signals: the desired analog signal ($x(t)$) and a reference signal ($r(t)$) (usually triangular or sawtooth), generating a PWM representation of the desired signal ($p(t)$), as presented in the block diagram of Figure 5. Following the comparator there is a register responsible to sample and discretize the PWM signal. Thereafter, the signal is available for further processing in the digital

domain. The comparator has the same behavior as the *sign(...)* function acting as a single-bit quantizer, which can be mathematically expressed as:

$$p(t) = sign\big(x(t) - r(t)\big) \tag{2}$$

in which, *x(t)* is the input signal, *r(t)* is the reference signal and considering the sign function defined as:

$$sign\big(x(t) - r(t)\big) = \begin{cases} -1\,, if\ x(t) - r(t) < 0 \\ +1\ \,, if\ x(t) - r(t) > 0. \end{cases} \tag{3}$$

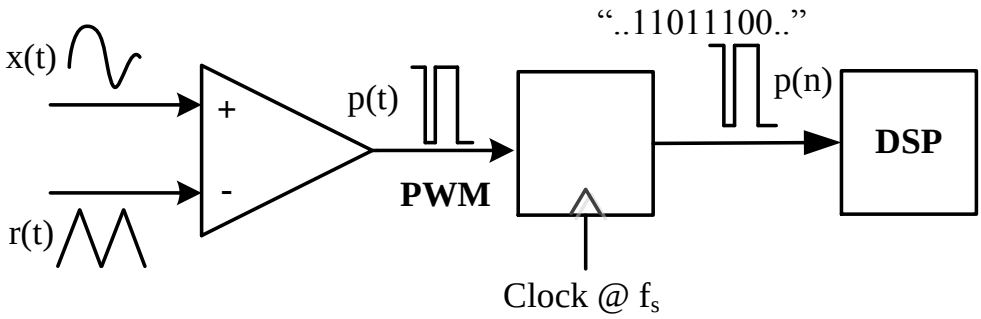


Figure 5 - Basic block diagram of a PWM converter.

Taking into account that the focus of this Ph.D. work is on RF ADC converters it is necessary to impose some modification to the Figure 5 to obtain the RF PWM converter. Figure 6 presents the generic block diagram architecture of a RF PWM receiver, where the signal *x(t)* represents the RF signal received at the antenna after filtering and low noise variable gain amplification (LNA/VGA). The *x(t)* signal is one of the inputs of a comparator, while the other is a reference signal (*r(t)*), producing a PWM representation of the analog signal at the output of the comparator. Following the comparator there is a register responsible to sample and discretize the PWM signal. Thereafter, the signal is available for further processing regarding digital down conversion and filtering in order to recover the baseband signal's information.

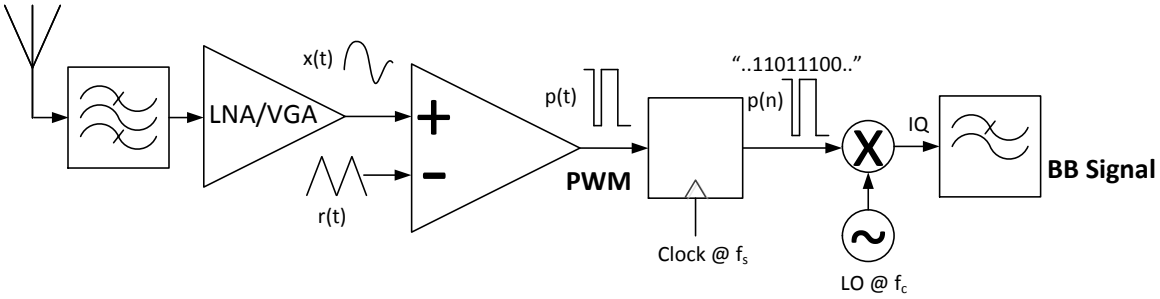


Figure 6 – Diagram of an RF PWM converter.

The proposed way to implement the conversion (PWM) is similar to the stochastic ergodic converter (SEC) presented in [31], which was a popular idea in the '60s to build low cost and low frequency ADCs. However, at the time, due to the lack of enabling technology, the idea was abandoned and sigma-delta converters were preferred [31] . This converter is mainly based on adding a dithering waveform to an analog signal and then feeding it to a single bit quantizer, as it is presented in Figure 7. The theoretical demonstration of this converter can be developed based on statistical quantization theory [32], which shows that if the dithering signal presents uniform distribution, the input signal will be equally quantized, i.e., the mean of the input signal will be contained in the output quantized signal, allowing its recovering. A common selection for the dithering wave is a triangular or sawtooth wave, since both present uniform amplitude distributions [31], [32]. This dithering wave can be directly transposed for the PWM RF ADC, playing the same role as the reference signal (*r(t)*), which should also present uniform amplitude distribution.

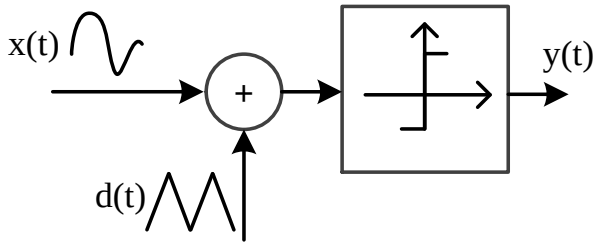


Figure 7 – Block diagram of the stochastic-ergodic converter (figure adapted from [31]**).**

After the quantization process, it is necessary to discretize the signal, that despite of already being represented in two well defined levels, it is not a discrete-time representation. There are at least two ways to discretize this signal: uniformly or not uniformly. The latter leads to a non-uniform sampling process, which is the method used in level-crossing ADCs [31]. However, this requires challenging interpolation methods to restore a uniform sampling rate, which falls out of the scope of this work. The uniform sampling is simpler and can be easily implemented by directly sampling the two-level signal at a constant clock frequency, which should be high enough to register all the

possible PWM transitions. Related to this process, there are two important characteristics, which are the reference frequency (f_r) and the sampling frequency (f_s) of the sampler after the comparator, that define the maximum bandwidth of the signal to be acquired. The latter two variables will also impose the converter's resolution, since the ratio between the effective sampling frequency (f_s) and the reference signal frequency (f_r) indicates the number of PWM levels and therefore, the number of bits of the converter and its signal-to-noise ratio (SNR), as follows:

$$N_{bits} = \log_2 N_{quatization\ levels} = \log_2 \frac{f_s}{f_r} \tag{4}$$

$$SNR = 6.02N_{bits} + 1.76 \tag{5}$$

The previous relationships indicate that the higher the ratio between the sampling frequency and the reference signal, the higher will be the converter effective resolution. Therefore, we may consider that the limit for the f_s will be imposed by the maximum frequency allowed by a given technological process or by a set of requirements such as resolution or power consumption of a certain application. Nonetheless, and without loss of generality, the f_s is assumed to be fixed at the maximum achievable value to provide the maximum resolution. Thereafter, considering an analog signal occupying a given bandwidth (*BW*), it is important to select the minimum reference signal frequency to provide the higher resolution. While a selection of a minimum reference frequency of *2BW* for a sawtooth waveform and of *BW* for a triangular waveform allows achieving the same resolution, it creates a different harmonic content in the PWM spectrum [33]. The sawtooth wave puts the first distortion band closer to the interest band, making the triangular wave a preferable way to acquire the signal and to provide a relaxation of the filtering requirements in the DDC chain. However, due to the uniform sampling imposed at the output of the comparator, this selection is not as trivial as previously stated, since the analog signal (*x(t)*) is an RF signal and not a baseband as usually in this type of converters. The PWM modulation process is highly non-linear, creating a huge amount of distortion. The PWM waveform is a square wave with variable duty-cycle, which presents an infinite spectrum. Therefore, after uniform sampling, aliasing will occur in the first Nyquist Zone (NZ) that may degrade the SNR if the distortion falls into the band of interest. This fact will demand to choose a proper reference signal, depending on the signal to acquire, which is one of the topics that will be addressed in this Ph.D. work, and at the best of the author knowledge has never been addressed focusing RF PWM converters.

After addressing the PWM process is possible to discuss in more detail the only RF PWM receiver published at the time that this Ph.D. started (2013): [25]. In [25] high speed comparators were used to generate the PWM representation and afterwards an FPGA-chip was used to gather the two-level signal and build the remaining receiver. This work does not present any procedure or analysis to get the PWM reference frequency. As already referred, one of the tasks of this Ph.D. work is to obtain the best reference frequency to

optimize the receiver figures-of-merit. Moreover, several other improvements are planned to be studied and implemented during this work, as for instance the usage of the FPGA IOs to be used directly as comparators.

Following similar reasoning, it is also important to refer several past approaches to build FPGA-based converters. In [34], [35], Xilinx released an application note to design a DSM low frequency DAC and ADC using directly the general purpose FPGA IOs. Additionally, Lattice Semiconductor [36] also released a similar application note just for ADCs based on DSM or Successive Approximation Register (SAR). The target of both these applications is low frequency and low bandwidth scenarios, which is exactly the opposite of the RF communication world, in which the carrier frequency is high and the required signal's bandwidth is successively increasing. However, at the same time the current state-of-the-art FPGA IOs sampling rate are increasing being able to reach 28Gbps, which completely changes the paradigm allowing to explore its usage for RF receivers, similarly to what has already been done for the transmitters [10], [13].

2.3. Receiver importance in a DPD scenario

Nowadays, the usage of DPD systems is widely spread over base station cellular infrastructure that use high power amplifiers, in which efficiency and linearity are a mandatory requirement [6]. However, even in mobile terminals low-complexity DPD structures are used to get improved transmission system performance [37], [38].

2.3.1. DPD concept

In order to get the best possible efficiency RF PAs are operated close to the compression or even sometimes a few dB magnitude levels above the 1 dB compression point. Consequently, non-linear in-band and out-band distortion will be generated, degrading the signal quality and emitting signal components in spectrum that may be allocated to other users. The easiest solution to avoid the non-linear distortion generation is to operate the PA in a back-off region, with the inherent drawback of a huge efficiency reduction. Therefore, a possible solution is to apply linearization techniques, in order to somehow modify the PA input signal, to get a distortion- free output while keeping the operation close to the best efficiency point. There are two ways to implement linearization techniques: in analog or in digital domain. Whereas both these ways are currently used, however DPD is more spread over base station cellular communications because it represents a cheaper and more flexible solution rather the analog linearization [5]. The analog linearization is completely out of the scope of this thesis, however if the reader is interested in such a topic more information can be found in [5].

Figure 8, represents a block diagram of the principle of PA linearization using DPD, in which there is a DPD block before the PA that is responsible to apply a given transfer function corresponding to the inverted behavior of the PA distortion that will pre-

compensate for the PA distortion. Following Figure 9(a) it is also possible to understand the different transfer functions of the DPD block and the PA block, in which the PA enters in the compression and the DPD expands the gain to compensate the PA compression, to obtain a linear system [7]. Additionally, Figure 9(b) presents the spectrum of the signal before and after applying DPD, where it is possible to observe the bandwidth expansion due to the PA non-linear behavior (spectral regrowth) and its correction with DPD. This bandwidth expansion limit is usually monitored with a metric defined as Adjacent Channel Power Ratio (ACPR) [39], that measures the ratio between the total power at the adjacent channels (high and low) and the power at the fundamental channel. The current LTE standard imposes an ACPR limit of 45 dBc.

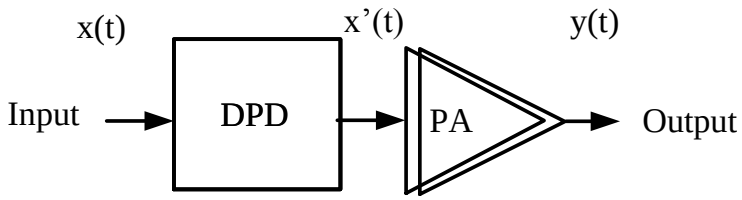


Figure 8 – Block diagram representing the DPD concept.

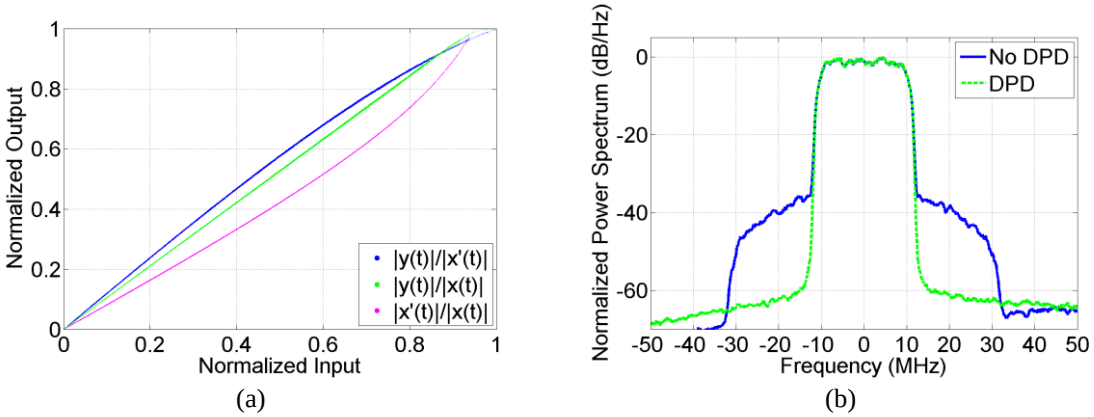


Figure 9 – AM/AM characteristic plot representing the digital predistorter block, the PA and the final linear system (DPD+PA) (a), and Spectrum before and after applying DPD (b).

2.3.2. Receiver role in DPD scenario

In practice, to apply DPD it is required to use a behavioral model, to mimic the inverse of the non-linear PA response. In order to model this inverse behavior, the low pass equivalent (LPE) signal representation of both input (*xBB(n)*) and output (*yBB(n)*) of the PA are required [6], [40], which imposes the need for a system that acquires the PA output, i.e., an RF receiving path. Such a system is usually made of transmitter section with a PA followed by a coupler, that will be a connected to a digital receiving path (known as observation path or feedback loop), as presented in Figure 10. Despite an RF ADC is

represented in Figure 10 any other receiver topology as presented before could be used. This receiver path should be able to sample a replica of the output of the PA without any degradation, i.e., according to Figure 10 the signal $z_{BB}(n)$ should be the closest possible replica of the LPE of $y(t)$. Therefore, it is of paramount importance to have a linear and flat feedback loop to not compromise the DPD performance. Once again it is important to realize that ADCs are also a key element in modern digital communication transmitters, where they play a fundamental role in the feedback loop of DPD architectures. Additionally, the importance of the receiver impairments and its impact on the DPD performance was also evaluated in this Ph.D. work.

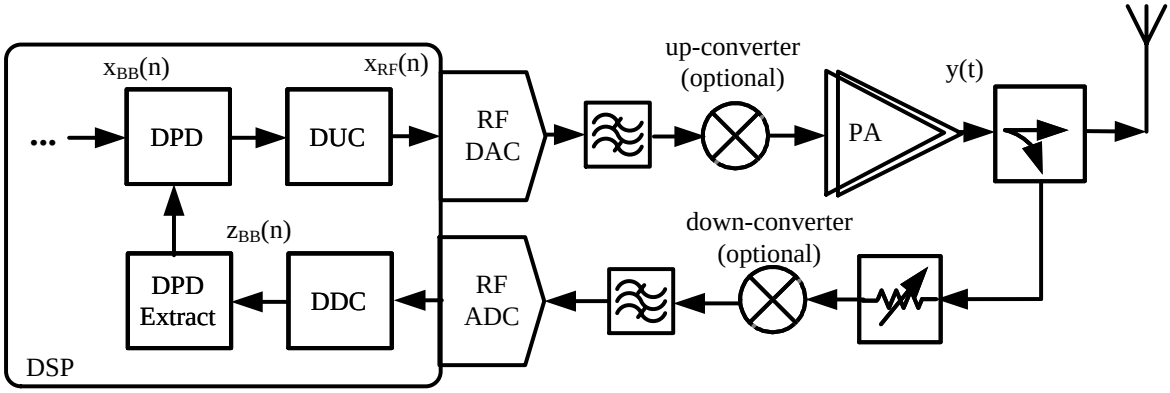


Figure 10 - Block diagram scheme representing a transmitter with feedback loop for DPD.

From the point of view of receiver optimization, which is the focus of this thesis, there are two more important scenarios in which the feedback path plays an important role which are:

- Multi-band applications, in which one PA is used to concurrently amplify two or more different frequency spectrum bands.
- MIMO scenarios, in which multiple transmitter branches are used to concurrently transmit at the same frequency codified signals, with the target of improving the bit error rate (BER) at the receiver side (MIMO transmit diversity mode), or with the target of increasing overall system transmission rate (MIMO spatial multiplexing mode).

2.3.2.1. Concurrent multi-band scenarios

Current wireless communications standards strongly depend on multiple carrier aggregation, in order to increase the communication throughput. In this way, to gather the maximum power efficiency, this has led to the use of a single amplifier for multiple band amplification, instead of using multiple amplifiers tuned at each specific frequency [41], [42]. However, in a multiple band scenario the implementation of DPD algorithms and feedback loops is not as straightforward as in a single band case. Considering a dual-band

scenario, first of all the non-linear contributions are now not only from the intermodulation distortion (IMD) products but also from the cross-modulation (CM) mixtures between the two bands that must be considered in the DPD design, so a 2D (two dimensional) model for the PA is mandatory to get improved performance [43]. Several research works have been done in order to look for effective 2D modeling structures, such as [43], [44] (more details about modeling structure are presented in the next section). Secondly, the feedback loop has now to acquire two bands concurrently at the output of the PA, which is at least twice of the required bandwidth in the single band case. A conventional architecture is usually made of two parallel feedback loops acquiring separately the lower band (LB) and upper band (UB) (Figure 11). This matter was also recently addressed by the scientific community by trying to reduce the needs of two feedback loops. In [45], [46], a single feedback loop strategy is presented by acquiring the multiple bands in different time slots. Another recent contribution in [47] develops a new approach called down-converted carrier co-location (DC^3). However, it requires two external mixers in the feedback path to place both bands at a specific location. Another possibility for the feedback loop is to use RF subsampling ADCs, such as presented in [48], where by changing the sampling frequency of the ADC allows to avoid the aliasing of the different bands, and thus, all the signal components can be recovered. In the scope of this Ph.D. a solution for this problem was also proposed.

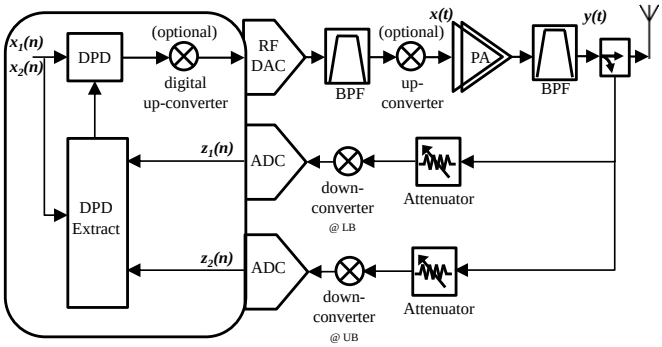


Figure 11 - General block diagram of a dual band wireless transmitter with a conventional feedback loop for dual-band DPD.

2.3.2.2. Multi-antenna scenarios

Multi-antenna transmitters, all considered as MIMO transmitters, inherited all the problems already existent in the common SISO transmitters and present additional ones. For instance, both transmitters are expected to operate at the same frequency to provide either transmit diversity or spatial multiplexing. Thus, it is expectable that the transmitters suffer from interference between each other, due to the leakage of sharing the same LO. Additionally, higher degrees of integration in the same Integrated Circuit (IC) are expected, which will also lead to higher levels of crosstalk between different RF lanes.

Last but not least, the antennas proximity may exacerbate mutual-coupling issues between each other, which can also be seen as crosstalk or interference. This problem will be even worse when considering a higher number of transmitters, as it is expected in the Massive MIMO scenario [1].

Therefore, by considering all the main sources of crosstalk, it is important to understand that linear-crosstalk (LC) and non-linear cross talk (NLC) may occur, as depicted in Figure 12. This separation is done considering that the cross-talk occurring before the PA, will create new distortion components due to the cross-terms between the main signal and the cross-talk. On the other hand, the cross-talk occurring after the PA is usually considered to be linear. However, it is important to state that this may also create non-linear distortion due to the possible load variations at the output of the PA, however this is an open question that falls out of the scope of this thesis.

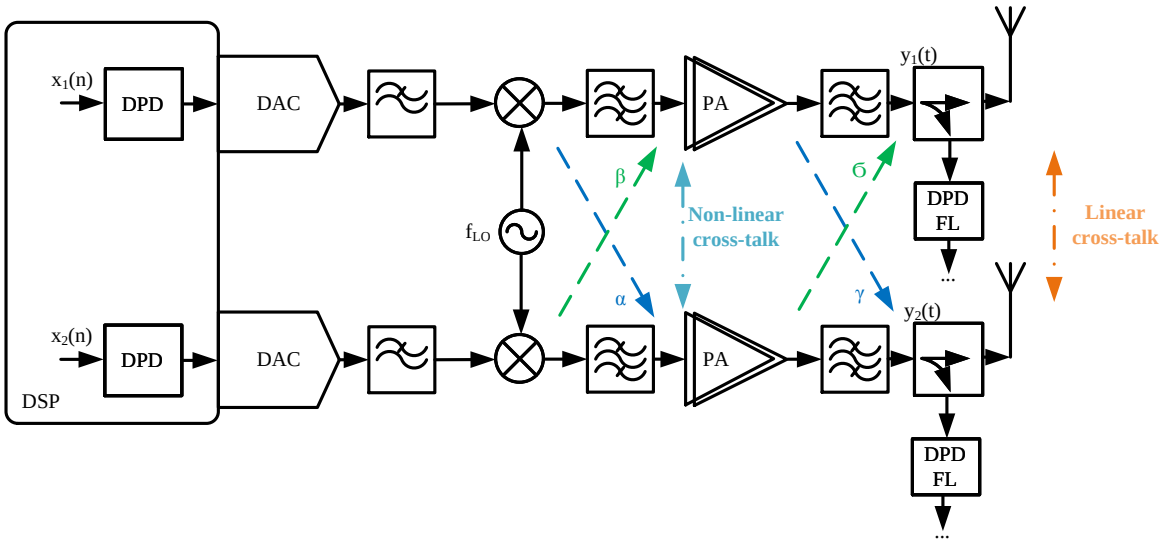


Figure 12 - Block diagram representation of a 2×M transmitter with LC and NLC cross talk. (figure adapted from [50]**).**

Focusing on Figure 12, it is possible to model the output of each PA in the following way:

$$y_1(t) = f_{PA\,1}\big(x_1(t) + \beta x_2(t)\big) + f_{PA\,2}\big(x_2(t) + \alpha x_1(t)\big)б \tag{6}$$

$$y_2(t) = f_{PA2}\big(x_2(t) + \alpha x_1(t)\big) + f_{PA\,1}\big(x_1(t) + \beta x_2(t)\big)\gamma \tag{7}$$

in which $x_1(t)$, $x_2(t)$, $y_1(t)$, $y_2(t)$ are the input/output of PA1 and PA2, respectively, $f_{PA1}(..)$ and $f_{PA2}(..)$ represents the non-linear function of each PA, and the α, β, 6 and γ represent the crosstalk accordingly to Figure 12. The presence of these interactions between lanes requires suitable modeling topologies to fit this problem, that is considerably different from the typical SISO one. In line with this issue, several research works have been proposed to provide a reasonable modeling formulation to efficiently address these problems [49]–[52].

Within this context, the relaxation of the feedback loop requirements is of paramount importance, since it would be desirable not have a one-to-one parity between number of transmitter lanes and number of observation paths for DPD. A simplification in the number of feedback loops or even in their requirements would allow to save costs and to enable scalable Massive MIMO approaches. In this context the work presented in [53] proposed a feedback that would acquire the combination of the PA outputs in a dual MIMO transmitter, instead of the individual feedback per PA. However, only simulation results were presented, which is still far away from the formal validation of this proposal. The study of the DPD feedback loop problem in multi-antenna transmitters was the last topic addressed in this Ph.D. thesis.

2.3.3. DPD models

This sub-section presents a brief summary about the mathematical formulation of one of the most used DPD models, i.e., the Memory Polynomial Model (MPM). Additionally in the Appendix – A - Additional DPD models, the reader may find more details about DPD models, addressing both SISO models for single band PAs, SISO models for dual band PAs and MIMO models for MIMO application scenarios. All the models are presented focusing on a forward model perspective, in which, $x(n)$ is the input of the PA and $y(n)$ its output. However, for DPD purposes an indirect learning architecture (ILA) using post inversion as suggested in [40] was considered.

SISO Memory Polynomial Model

The SISO Memory Polynomial Model (MPM) is usually a quite effective model in terms of tradeoff between complexity and performance and its mathematical formulation is presented as follows [40]:

$$y(n) = \sum_{m=0}^{M} \sum_{k=0}^{\frac{K+1}{2}} h_{(m,k)} x(n-m)|x(n-m)|^{2k} \tag{8}$$

where, *x(n)* is the PA LPE input signal, *y(n)* is the PA LPE output signal, M is the memory depth, K is maximum order of nonlinearity and $h_{(m,k)}$ are the PA forward model coefficients [40].
Considering the matrix notation for the former equation can be elaborated as:

$$\tilde{y} = XH \tag{9}$$

$$X = [X_0 \quad X_1 \quad \dots \quad \dots \quad X_K] \tag{10}$$

$$X_K = [x(0)|x(0)|^{2K} .. \quad x(n-m)|x(n-m)|^{2K} \quad .. \quad x(N)|x(N)|^{2K} .. \quad x(N-m)|x(N-m)|^{2K}]^T \tag{11}$$

, where $\tilde{y}$ is the measured data at the output of the transmitter, N is the total number of signal samples, *X* is the regression matrix containing all the basis function of *x(n)*, and *H* is the matrix containing the model coefficients, which can be solved in a Least Squares (LS) sense [40]:

$$H = (X^H X)^{-1} X^H \tilde{y} \tag{12}$$

In which $(.)^H$ is the Hermitian transpose.
For the case of DPD, the inverse model (H_i) should be obtained in the following way:

$$\tilde{x} = YH_i \tag{13}$$

$$Y = [Y_0 \quad Y_1 \quad \dots \quad \dots \quad Y_K] \tag{14}$$

$$Y_K = [y(0)|y(0)|^{2K} .. \quad y(n-m)|y(n-m)|^{2K} \quad .. \quad y(N)|y(N)|^{2K} .. \quad y(N-m)|y(N-m)|^{2K}]^T \tag{15}$$

, where $\tilde{x}$ is the measured data at the input of the transmitter, *X* is the regression matrix containing all the basis function of *y(n)*, and *H* is the matrix containing the coefficient models, which can again be solved in a LS sense [40]:

$$H_i = (Y^H Y)^{-1} Y^H \tilde{x} \tag{16}$$

Then, after building the regression matrix of the inputs X the pre-distorted replica can be defined as:

$$x_{PD} = XH_i \tag{17}$$

An important note to highlight is the number of coefficients (or basis functions) of the SISO MPM model, that can be given by:

$$N_{Coefs\,MPM} = (M+1)\left(\frac{K+1}{2}\right) \tag{18}$$

2.4. Summary and concluding remarks

In this chapter a state-of-the-art review about RF receivers was presented, in which, RF sampling architectures were considered to be the most promising future candidates to get better performance in terms of bandwidth and agility, following the well-known SDR concept. During this review, several research challenges of these architectures were addressed, considering the usage of a RF receiver in a standalone operation, i.e., used for receiving unknown data at the antenna, and when used as observation path for PA linearization via DPD.

The identified challenges were addressed in this Ph.D. work focusing on innovative and disruptive ways to improve important FoMs of current RF systems.

In summary, the identified research lines are in first place related with commercial available RF ADCs, which will be studied and characterized, to understand their limitations and possible ways to increase their performance within a DPD scenario (chapter 3). Afterwards, a disruptive and innovative FPGA-based RF single-bit pulsed converter based on PWM will be addressed targeting frequency agility, high analog input bandwidth, and system integration, taking profit of the FPGA-based implementation. The latter will also be optimized based on PWM theoretical behavior maximizing SNR and bandwidth. Additionally, the proposed receiver will be implemented and evaluated in a DPD scenario to provide an agile FPGA-based single-bit observation path for PA linearization (chapter 4). Finally, a study to evaluate several alternatives to build DPD feedback loops in the scope of multi-antenna transmitters will also be addressed (chapter 5).

3. RF ADCs enhancement in a DPD scenario

In this chapter, the first part of the work developed during this Ph.D. is addressed, which is related to the study of the receiver role in a DPD scenario, as it was already briefly explained in the chapter 2.3 of the state-of-the-art. During this section the RF receiver (feedback loop) considered for this study is an RF sampling ADC, since the receivers based on this topology are the ones able to provide higher bandwidth and flexibility, and being capable to fulfill the so-called SDR-DPD approach mentioned in [6]. However, some of the proposed techniques presented in this Section are possible to be applied to any type of receiver, as it will be explained later on.

Firstly, this chapter will focus on the study and evaluation of the RF ADCs impairments' impact in a DPD application scenario.

Secondly, the feedback loop based on an RF ADC will be studied in order to try to provide some feedback loop requirements relaxation for a dual-band DPD scenario.

This chapter is supported by paper [C1] regarding the evaluation of the feedback loop impairments' impact in a DPD application scenario, and by paper [J1] concerning the feedback loop requirements relaxation in a dual-band DPD scenario.

3.1. Evaluation and compensation of the RF ADCs impairments' in a DPD scenario

The main objective of this section is to study and evaluate the RF ADCs impairments' impact in a DPD application scenario. As already briefly explained in chapter 2.2.2, the feedback loop is responsible to acquire a replica of the PA output and provide it to the digital domain element responsible for the PA modeling that will extract the pre-distortion block in charge of linearizing the PA. As presented in Figure 10, the input signal *xBB(n)* represents the LPE of the PA input, *y(t)* represents the PA output signal and *yBB(n)* represents the correspondent LPE, and finally *zBB(n)* is the version of *yBB(n)* acquired by the feedback loop. Therefore, in a DPD scenario, such as presented in Figure 10, the DPD considers *zBB(n)* as a perfect representation of *yBB(n)*, in order to extract its parameters. For narrow band signals this assumption is valid. However, for wideband signals the feedback loop impairments will impose some drawbacks, as it will be shown far ahead.

Several research works have already been done to characterize RF ADC's behavior, such as presented in [19]–[22]. Additionally, in [54] ADC's quantization noise, random jitter, and the integral nonlinearity (INL) imperfections were evaluated considering a DPD scenario, revealing results without significant impact in the overall system performance. Nevertheless, there is still a lack in order to understand the consequences of RF ADC's operation in higher NZs regarding the signal integrity as also its possible correction in digital domain. In this way, by characterizing the entire feedback loop with a

function *H(jw)*, it would be possible to apply post-compensation ($H(jw)^{-1}$) to approximate *zBB(n)* to *yBB(n)*, which should improve the DPD performance. The analog components of the feedback loop can be characterized using a vector network analyzer (VNA). However, that is not possible for the ADC, which must be characterized using methods such as presented in [19]–[22].

For this purpose, a compensation model for a commercial RF under-sampling ADC was extracted using a vector signal analyzer (VSA) as a "golden reference". This compensation model mitigates the ADC impairments when compared to the VSA. The feedback loop compensation model extraction focuses in the premise that the signals *zBB(n)* and *yBB(n)* are not exactly equal, as they should ideally be (apart from a difference in amplitude due to the attenuator in the feedback loop). In order to support the previous statement, as also the entire model extraction, measurements of the same signal acquired by an RF ADC (*zBB(n)*) and a VSA (*yBB(n)* - considered to be an ideal reference) will be compared. The signal selected to accomplish the characterization is a multi-sine, since it gives the possibility to excite a wide range of frequencies with only one measurement and gather information from both amplitude and phase. Additional details about the characterization procedure may be found in the paper [C1] presented in the Appendix C.

In order to proceed with the validation of the proposed compensation procedure, it is necessary to introduce the assembled laboratorial DPD setup as presented in Figure 13, in which an arbitrary waveform generator (AWG) (AWG70002A from Tektronix), responsible for the signal generation is followed by the PA. Regarding the feedback loop, the Texas Instruments ADS5400 with 12 bits, 1 GHz of maximum sampling frequency and 2.1 GHz of input bandwidth, was used. The chosen ADC's operating frequency for all measurements was 1 GHz, and the RF interest signal (carrier frequency) was 1.79 GHz (located in the 4th NZ of the ADC). In order to monitor the PA output without exclusively recurring to the feedback loop it was used a Vector Signal Analyzer (VSA). The VSA is a Rohde & Schwarz FSW8, with maximum bandwidth of 320 MHz. The same VSA is used for the characterization procedure previously described. All the setup is remotely controlled via Matlab.

After having all the setup correctly assembled and validated, the feedback loop compensation model was extracted according to the procedure previously described. For the characterization a multi-sine signal with 150 MHz of bandwidth, 5 MHz of fixed spacing between tones, random phases and centered at 1.79 GHz was used. Therefore considering the fixed sampling frequency of 1 GHz in the ADC, the folded frequency in the 1st NZ is at 210MHz. Figure 14 presents the amplitude and phase of the $H(jw)^{-1}$ model. This model can be directly applied to any ADC sampled signal within 1.715 GHz and 1.865 GHz, which corresponds to the multi-sine lower and higher tones. Additionally and despite of this model is being extracted for 150 MHz in the 4th NZ, this procedure could be done for any other ADC frequency band. It is also important to state, that to apply this model in a real modulated signal, an interpolation operation has to be performed.

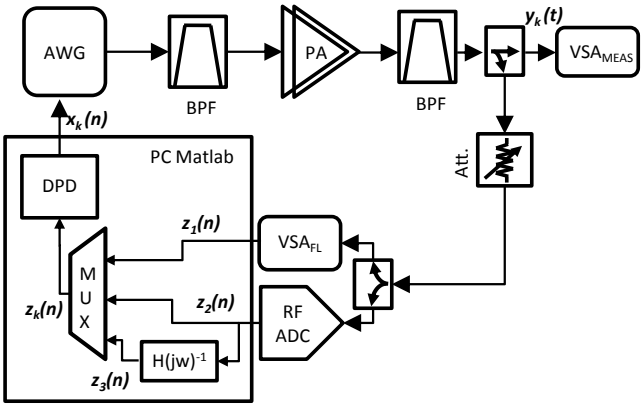


Figure 13 - Block diagram representation of measurement setup for the evaluation and compensation of the RF ADCs impairments in a DPD scenario.

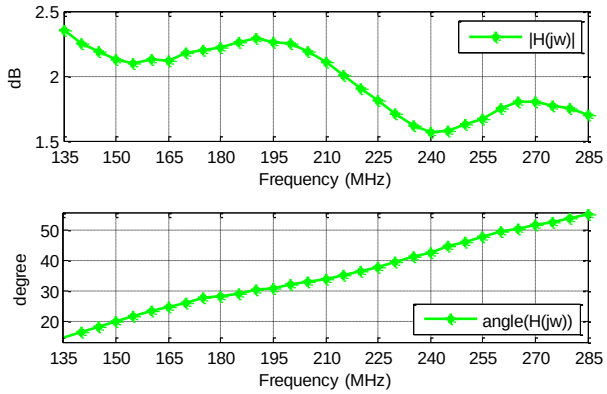


Figure 14 - Frequency domain representation of amplitude and phase of the $H(jw)^{-1}$ compensation model.

In order to show the relevance of the feedback loop compensation model, this will be applied to a DPD scenario (Figure 13), in which three different feedback loops are considered for comparison:

- using the VSA ($z_1(n)$);
- using the RF ADC ($z_2(n)$);
- using the same RF ADC with post compensation ($z_3(n)$, i.e., $z_3(n) = z_2(n).H(jw)^{-1}$).

The power amplifier (PA) block comprises two Mini-Circuits amplifiers. The laboratorial setup assembled for this experiment is presented in Figure 15.

In the DPD experiment, the base band signal is a 50 MHz, 16-QAM modulated signal. Using this bandwidth, the entire signal and its third order distortion are suitable to the model extracted in the previous section. The DPD is also implemented in Matlab, using the well-known MPM model explained in the previous Chapter.

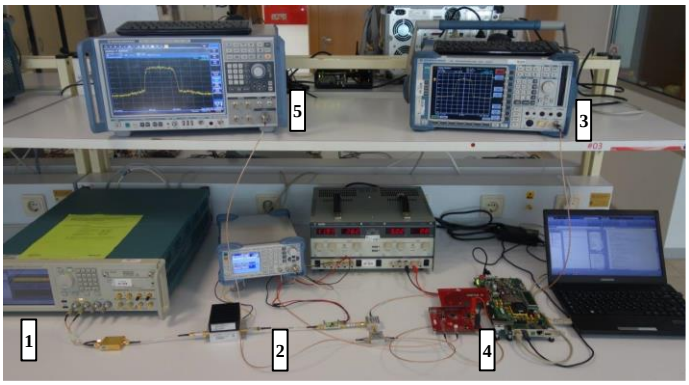
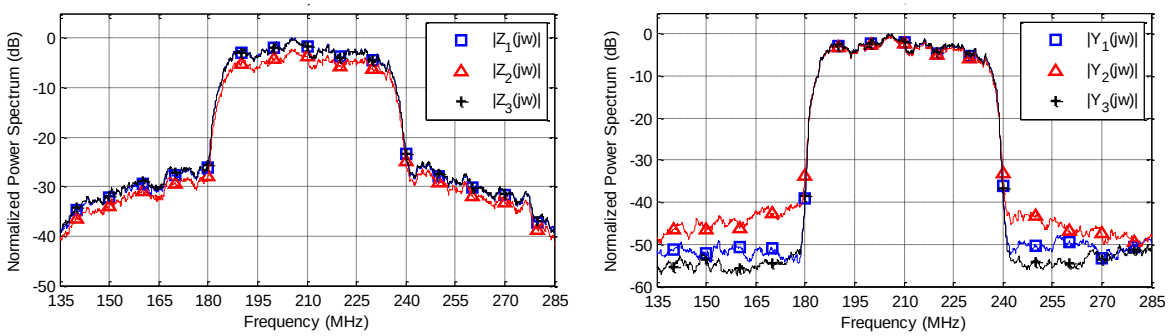


Figure 15 - Photograph of the laboratorial setup (1- AWG; 2- PA; 3- Spectrum Analyzer (SA) to monitor the output of the PA; 4-ADC; 5-VSA for the characterization of the feedback loop).

Figure 16(a) presents the spectrum of the signals $z_1(n)$, $z_2(n)$ and $z_3(n)$, where it is possible to observe differences between the signal captured from ADC ($Z_2(jw)$) and the post-compensated signal ($Z_3(jw)$), which is closer to the VSA signal ($Z_1(jw)$). The same DPD model (with M=5 and K=5) was applied using the signals $z_1(n)$, $z_2(n)$ and $z_3(n)$. Therefore, using a VSA three different signals were captured at the PA output ($y_1(t)$, $y_2(t)$ and $y_3(t)$) for each different pre-distorter output ($x_1(n)$, $x_2(n)$ and $x3(n)$). The results are presented in Figure 16(b), where it is possible to observe that the ACPR of the $y_3(n)$ is greater than in $y_2(n)$, showing a great improvement of DPD performance by applying ADC post compensation. In fact, this experiment shows an improvement of about 9 dB in the total ACPR, by applying post-compensation. Concerning the EVM of the signal there is also a significant improvement of about 1.76%. More details of these improvements are presented in the in the paper [C1].



(a) (b)

Figure 16 – (a): Spectrum of the signals from the three feedback loops. (b): Spectrum of the PA output after applying DPD with each feedback loop.

3.2. RF ADCs enhancement in a dual band DPD scenario

Nowadays, spectrum aggregation scenarios, in which multiple bands can be contiguously on non-contiguously aggregated are a real possibility in the most recent LTE releases [55]. Therefore, scenarios in which one PA deals with a multi-band signal are getting common. In this sub-section, the focus will be on the study of feedback loops using RF subsampling ADCs as a way to improve the concurrent dual-band transmitter's linearization. In this dual-band scenario it is assumed to exist two bands designated by lower band (LB) at the lowest carrier frequency and upper band (UB) located at a higher carrier frequency.

As it has already been addressed in the previous Chapter 2, several new challenges are presented when addressing DPD in dual band scenario. For instance, different 2D modeling topologies are required for improved performance. Additionally, usually two parallel feedback loops are also required as shown in Figure 11. However, the simplification of the feedback loop is being highly addressed by the scientific community, because it is seen as a way to simplify the system architecture and reduce costs, which is highly appreciated if same level of performance is kept. Some of the works already done in this topic were also addressed in Chapter 2.

In this sub-section, it is proposed an architecture based on RF subsampling ADCs, where the sampling frequency is maintained fixed. This process can obviously cause aliasing between LB and UB that will be solved by a characterization procedure based on statistical approximated non-overlapped multi-sines.

Therefore, considering a dual-band scenario presenting a LB and UB that are respectively represented by $x_1(t)$, signal centered at $f_{c1,}$ and $x_2(t)$ centered at f_{c2}. This will originate the signal $x(t)$ given by the summation of $x_1(t)$ and $x_2(t)$, as depicted in Figure 17(a). If this signal passes through the PA, it will cause non-linear distortion (IMD and CM), which will appear in-band and out-of-band (OOB). The OOB distortion can be removed by an analog band-pass filter (BPF), but the in-band cannot be eliminated by the same approach, Figure 17(b).

Therefore, in an RF subsampling feedback loop case with a given sampling frequency (f_s) such that $f_s < min(2f_{c1}, 2f_{c2})$, it is immediate to recognize that overlapping of both the LB and UB may occur in the first NZ. To verify the overlapping occurrence, the first NZ folding frequencies ($f_{c1\text{-}fold}$ and $f_{c2\text{-}fold}$) must be computed using (1).

If there is no overlapping between the LB and UB, the normal procedure of a 2D DPD model can be executed. In contrast, when overlapping occurs the recovery of $z_1(n)$ and $z_2(n)$, which are the sampled versions of $y_1(t)$ and $y_2(t)$, is totally compromised because both signals will fall on top of each other, as shown in Figure 17(c).

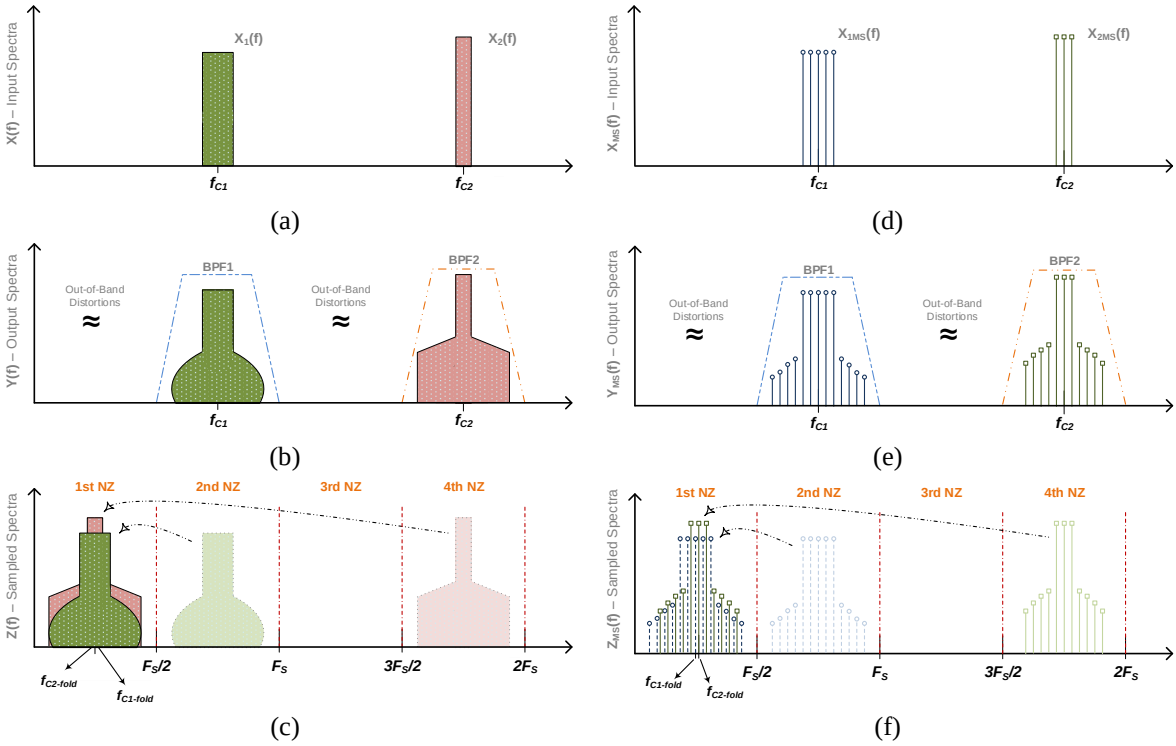


Figure 17 - (a): Spectrum of the signal *x(t)* at the input of the PA. (b): Spectrum of the signal *y(t)* at the output of the PA. (c): Spectrum of the signal *z(n)* acquired by the feedback loop. (d): Spectrum of the signal $x_{MS}(t)$ at the input of the PA. (e): Spectrum of the signal $y_{MS}(t)$ at the output of the PA. (f): Spectrum of the signal $z_{MS}(t)$ acquired by the RF subsampling feedback loop.

To avoid this problem the obvious solutions would be to use two independent feedback loops or to modify the ADC sampling rate in a way that the acquired signals would not be overlapped [48]. However, these solutions represent an increase in the overall system cost and complexity. Another solution is to acquire LB and UB in different time slots to extract the signals for the DPD [45], [46], but this technique loses the real time functionality of the feedback loop. More recently, an alternative solution based in the carrier co-location technique (DC^3) has been proposed in [47], which allows the extraction of the DPD parameters from the overlapped signals. In any case, such an approach will increase the processing capacity needed for the extraction procedure and imposes the use of different local oscillators (LOs) between the transmitter and feedback loop chain.

In alternative, the new proposed solution to overcome the previously mentioned aliasing problem is based on a strategy that replaces the original $x_1(t)$ and $x_2(t)$ modulated signals by statistically approximated non-overlapped multi-sines. The underlying idea of this approach is to choose a suitable placement of the multi-sine frequency bins, avoiding overlapping of LB and UB signals in the extraction procedure.

For this purpose, each multi-sine should present N_1 and N_2 tones with the same fixed separation between tones (Δf) covering a bandwidth BW_1 and BW_2 equal to the channel bandwidth of $x_1(t)$ and $x_2(t)$ signals. Then, it is necessary to verify the overlapping

condition assuming multi-sines to be centered at f_{c1} and f_{c2}, originating folded versions at $f_{c1\text{-}fold}$ and $f_{c2\text{-}fold}$ calculated using (1). If there is any multi-sine tone overlap in this process, it is necessary to shift one of the carriers by a certain offset in frequency given by $\Delta f_{offset} = \Delta f/2$ (leading to the minimum sample acquisition requirement). Figure 18 presents the described procedure.

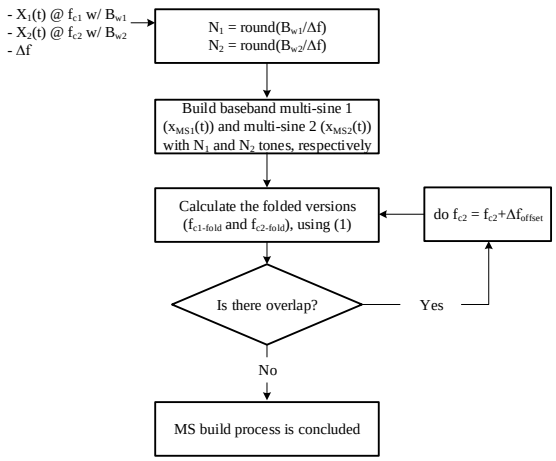


Figure 18 - Flowchart of the procedure for the construction of the non-overlapping multi-sines.

In order to conceptually validate the described procedure, the $x_1(t)$ and $x_2(t)$ modulated signals of Figure 17(a) will be replaced by two multi-sine signals $x_{1MS}(t)$ and $x_{2MS}(t)$ built as previously explained together with a specific statistical shaping. Thus, the signal $x_{MS}(t)$ is the summation of the $x_{1MS}(t)$ with $x_{2MS}(t)$ placed in the desired carrier frequencies, as depicted in Figure 17(d). Consequently, $y_{MS}(t)$ will be the signal at the output of the PA with the non-linear distortion appearing at the same frequencies as in the previous case Figure 17(e), and $z_{MS}(n)$ will be the signal acquired by the RF subsampling feedback loop Figure 17(f).

Focusing on Figure 17(f) it is possible to verify that the multi-sine tones do not overlap, being possible to recover them in the frequency domain by calculating the folded frequencies of each multi-sine tone using (1). This strategy allows obtaining both $z_{1MS}(t)$ and $z_{2MS}(t)$ after the folding mechanism, and thus, to calculate the respective low-pass equivalent (LPE) signals to model the system. Moreover, the kernels determination using the statistical-shaped non-overlapping multi-sines will allow to build a common 2D-DPD extraction process to be applied in the overlapped modulated signal case. Additional details about the statistical-shaped multi-sine design and the proposed procedure may be found in the paper [J1] presented in the Appendix C.

In order to experimentally validate the proposed solution the measurement setup presented in the block diagram of Figure 19 was assembled, which is similar to the one of Figure 13 and Figure 15, since the same laboratorial equipment was used. It is also important to state that the feedback loop was post-compensated according to the

techniques presented in the previous sub-section. Additionally, to perform a comparison with a similar state-of the art method, the same setup was also used to apply the method proposed in [47]. The signals $x_1(t)$ and $x_2(t)$ considered for the experimental test are QPSK modulated signals with symbol rates of 5 MHz and 10 MHz respectively. Therefore, considering that a baseband root raised cosine (RRC) with a factor of 0.25 was used, this implies that the signals will occupy a total channel bandwidth of 6.25 MHz and 12.5 MHz respectively. The carriers for both LB and UB are respectively 910 MHz and 1090 MHz. Since the ADC sampling frequency was set to be 1 GHz and according to (1), this makes the folded frequencies of the modulated signal to overlap in the 1st NZ at 90 MHz.

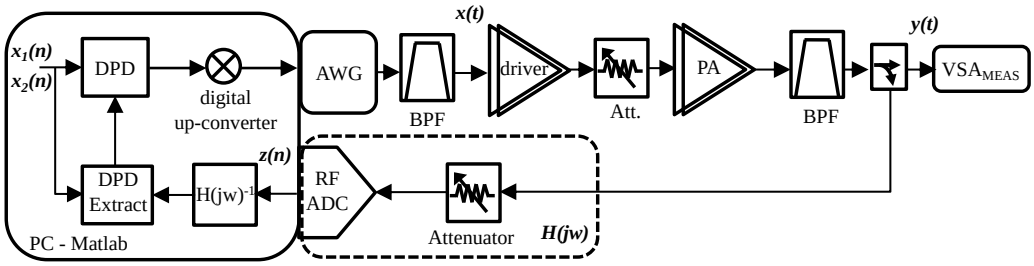


Figure 19 - Block diagram of the measurement setup.

The first validation measurement was performed using the non-overlapped multi-sines, whose details can be found in the attached paper [J1]. After the multi-sine modeling extraction the focus is on the application of the DPD to a modulated signal.

Therefore, after applying the entire modeling technique to modulated signal the 2D-DPD results are presented applying an inverse model of K=7 and M=3. Figure 20 presents the measured results with the VSA at the output of the PA in terms of output spectra, amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM). Moreover, the spectrum results at the output of the PA show the comparison of applying 2D-DPD with the proposed method and with the method of [47]. In fact, by analyzing the total ACPR improvement, one can verify that the proposed method reaches a reduction of 19.98 dBc in the LB and 14.59 dBc in the UB. Whereas the method of [47], is able to reach a reduction of 20.59 dBc in the LB and 13.78 dBc in the UB. More details of lower band ACPR and upper band ACPR, as also EVM can be found in Table 1, for both the proposed method and the method of [47]. A brief comparison in terms of ACPR and EVM performance shows that the proposed method matches the remaining state-of-the-art.

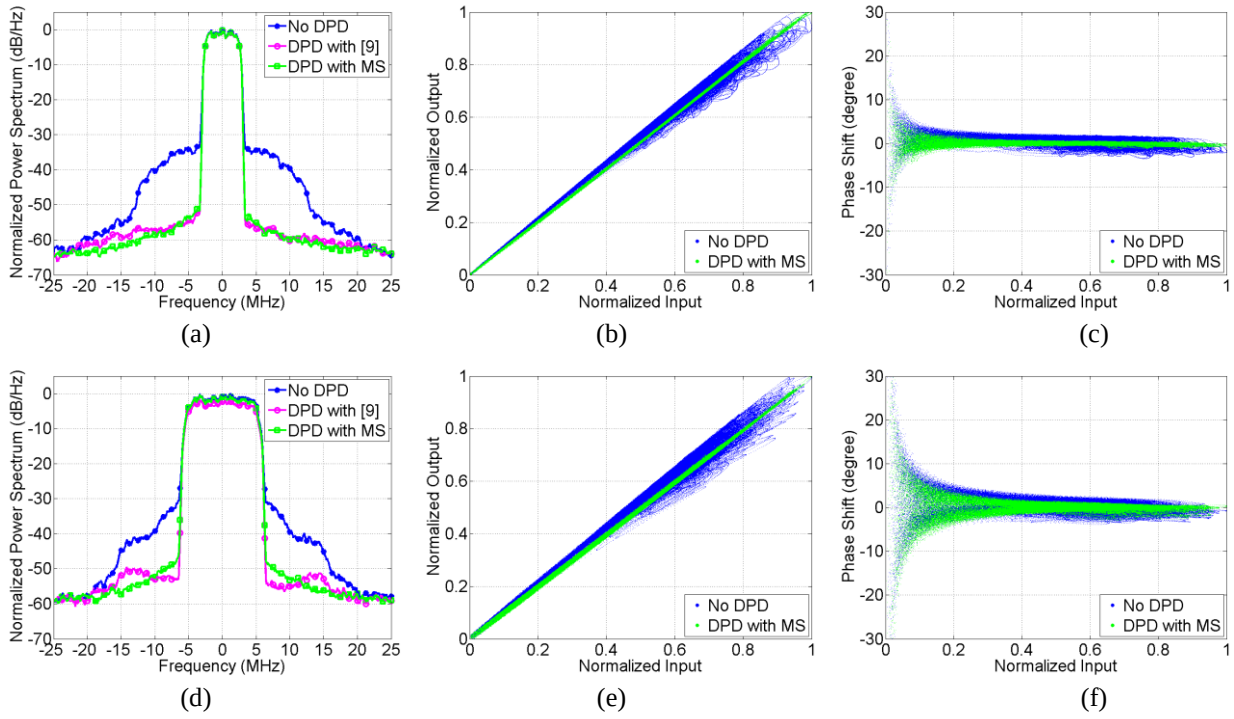


Figure 20 - Dual band DPD results. (a)-(c) Spectrum of the LB signal before and after applying DPD with proposed method and the method of [47]**, AM-AM and AM-PM plots. (d)-(f) Spectrum of the UB signal before and after applying DPD with proposed method and the method of [9], AM-AM and AM-PM plots. (MS – non-overlapped statistical approximated multi-sine method).**

Table 1 - Measurement results of EVM and ACPR before and after applying DPD.

			PA Output		
			before DPD	after DPD with MS	after DPD with [47]
Lower Band	EVM rms (%)		1.59	0.48	0.52
	ACPR (dBc)	Lower	33.29	52.73	53.23
		Higher	33.47	54.09	54.86
		Total	30.37	50.35	50.96
Upper Band	EVM rms (%)		3.52	0.82	0.86
	ACPR (dBc)	Lower	35.85	49.99	48.72
		Higher	35.62	50.68	50.49
		Total	32.72	47.31	46.85

3.3. Summary and concluding remarks

In this first part of this chapter, a linear compensation model to apply in RF ADCs, commonly used in DPD feedback loops has been proposed and validated with measurements. It was shown that the application of this post-compensation model in the feedback loop enables an improvement of DPD performance. This improvement was quantified in terms of EVM and ACPR, showing significant gains. Moreover, this compensation system can also be applied in other use case scenarios in order to improve the signal integrity of any acquired signal.

In the second part of this chapter, a new technique for concurrent dual-band PA linearization using an RF subsampling-based feedback loop was presented. The presented strategy is based on non-overlapped statistical approximated multi-sine design and allows having any pair of LB and UB modulated signals, even when aliasing occurs between these bands in the feedback loop. The obtained results in this second part are considered very promising and similar to other results obtained in other state-of-the-art works such as [47], [48], where similar test conditions signals have been performed.

The main idea of the work presented in the second part of this chapter was to propose a solution when overlapping of different bands occur using RF subsampling ADCs. If overlapping does not occur both bands are directly available in the digital domain and a traditional 2D-DPD methodology can be applied. However, there may be a given pair of LB and UB carrier frequencies, which cause overlapping between both bands. It is important to refer that this overlapping between LB and UB, may produce equal folding carrier frequencies or not. If the folding frequencies are equal (similar situation to the method of [47]), both our method and the proposed in [47] can be used. The method presented in [47] needs to be modified for a situation where the folding carrier frequencies are not equal, however the method proposed within this thesis still works in such situation without any additional modification. The only mandatory aspect is to guarantee the multi-sine non-overlapping condition. Other particular aspect of the comparison with [47], is regarding the requirement of a 2-D cross correlation, whereas the proposed method just needs a simple cross correlation, after recovering the LPE of each multi-sine. When comparing the current work with [48], it is possible to realize that the proposed method does not need to recalculate and change the sampling frequency, which may be a complicated procedure to do in a real-time application.

Finally, scalability is another important advantage of the proposed multi-sine method, allowing its use with more than two bands. Again, it would be mandatory to guarantee the non-overlapping multi-sine condition, which in an N band case would need to be reformulated to $\Delta f_{offset} = \Delta f/N$.

4. PWM RF receiver design and applications

The second part of this Ph.D. work is addressed in this Chapter, which is related to the study of disruptive RF receiver architectures based on pulsed converters, specifically PWM converters. The state-of-the-art regarding this Section was introduced in the Section 2.2.2. The study and evaluation of the proposed RF PWM receiver considers the usage of an RF receiver in a standalone operation, i.e., used for receiving unknown data at the antenna, and when used as observation path for PA linearization via DPD.

Firstly, this Chapter will focus on the feasibility study of the implementation of RF PWM ADCs using state-of-the-art FPGAs. This subsection is supported by the papers [C2, C3 and C4].

The second part of the Chapter targets the optimization of the PWM receiver design based on the mathematical model of the PWM sampling process. This will allow to improve and optimize the receiverk in terms of SNR and bandwidth. This subsection is supported by the paper [C5] and [J2].

Finally, considering the optimized version of the PWM receiver, two important application scenarios will be presented. The first one focuses on standalone operation in a C-RAN architecture, which is considered one of the key enabling technologies for the 5G networks. The second validates the proposed receiver as a feedback loop for DPD. This subsection is supported by the paper [C6] and paper [J3].

4.1. PWM RF receiver design

The first step towards the PWM RF receiver design, such as the one presented in Figure 6, is to evaluate the feasibility of such architecture using the current state-of-the-art FPGAs. Basically, the underlying idea is to make usage of the high speed differential inputs of the FPGA, with current maximum bitrate up to around 28 Gbps, to directly build a comparator, and therefore obtain an RF PWM ADC fully implemented using a single FPGA-chip. The referred inputs are available in the Multi-Gigabit Transceivers (MGTs), which are based on high speed Serializer/Deserializer (SerDes). These are commonly used to implement high speed serial communication links such as SATA, PCIe and recently they have already been used to implement all-digital SDR transmitters as presented in [13], [29], [30]. There are several advantages associated with the exploration of this idea, such as:

- Integration capabilities and reduced bill of materials, since it would be possible to remove the typical ADC device from the RF receiver chain, and depending on the RF carrier, eventually remove the mixer.
- Reconfigurability of the FPGA, which would allow to have a multi-standard radio capable to be real-time adaptive to different protocols and environments.

- Scalability, since one single FPGA presents several MGTs IOs, this would allow to target 5G massive MIMO architectures providing highly integrated systems.
- FPGA processing power and process parallelization, which is one of the most important attributes of FPGA and one of the reasons why they are widely used for DSP tasks within the telecommunication's industry.
- Provide an all-digital transceiver solution, when integrated with the well-known all-digital transmitters [13], [29], [30].

The architecture of the proposed FPGA-based SDR receiver is presented in the block diagram of Figure 21. In this architecture after the antenna there is a bandpass filter in order to select the specific band to receive, which is followed by a Low Noise Amplifier (LNA) with variable gain amplification (VGA) in order to adjust the amplitude of the *x(t)* signal to be less than the *r(t)* signal. Alternatively, the amplitude of *r(t)* can also be changed. After the LNA/VGA there is the FPGA MGT input. The MGT is a quite complex element, however for this purpose it can be simplified as presented in Figure 21, i.e., an input differential buffer followed by a Serial In-Parallel Out (SIPO) block. The latter is responsible for the sampling rate reduction from a high sampling rate (f_s) up to a low sampling rate capable to be dealt in the standard FPGA logic (f_s /*N*). At the SIPO's output there is an N-bit parallel word which represents the PWM signal. This parallel word contains a PWM representation of the *x(t)* signal centered in f_c and sampled at f_s. Afterwards, the signal must be digitally down-converted, filtered and decimated up to a low sampling rate to consequently be possible to demodulate and acquire the signal's information. Since the MGTs operate at GHz frequencies (f_s), a suitable polyphase architecture for the DDC must be designed to become possible to operate an f_s sampling rate inside the FPGA. Regarding the reference signal generation (*r(t)*), this can be performed inside the FPGA using the well-known FPGA-based all-digital transmitter's architectures as presented in [13], [29], [30].

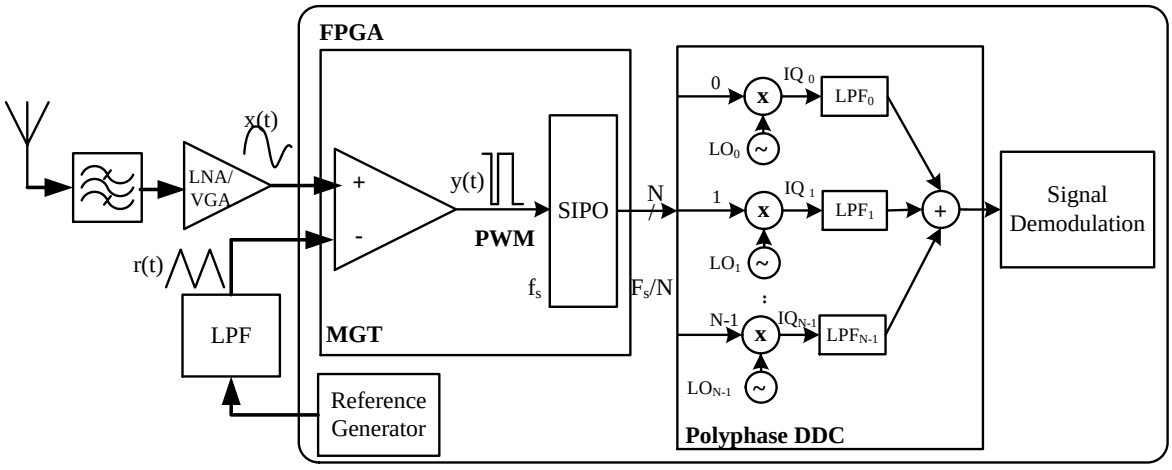


Figure 21 - Block diagram representation of the proposed SDR architecture based on PWM using FPGA.

In order to evaluate the feasibility of the previously proposed idea, a dual channel AWG (AWG70006 from Tektronix) was used to generate the RF signal (*x(t)*) as also the reference signal (*r(t)*) to be used as inputs of the comparator, as represented in Figure 22. Regarding the FPGA, a KC705 development board from Xilinx with a Kintex 7 FPGA, was used. This is equipped with GTX MGT transceivers capable of a maximum bitrate of 12 Gbps. The GTX transceiver was configured to work at a rate of 10 Gbps and to generate a parallel word of 64 bits at the deserializer output. This implies that the polyphase DDC runs in 64 parallel paths at a frequency of 10G/64 = 156.25 MHz. Figure 23 presents a photography of the assembled laboratorial setup.

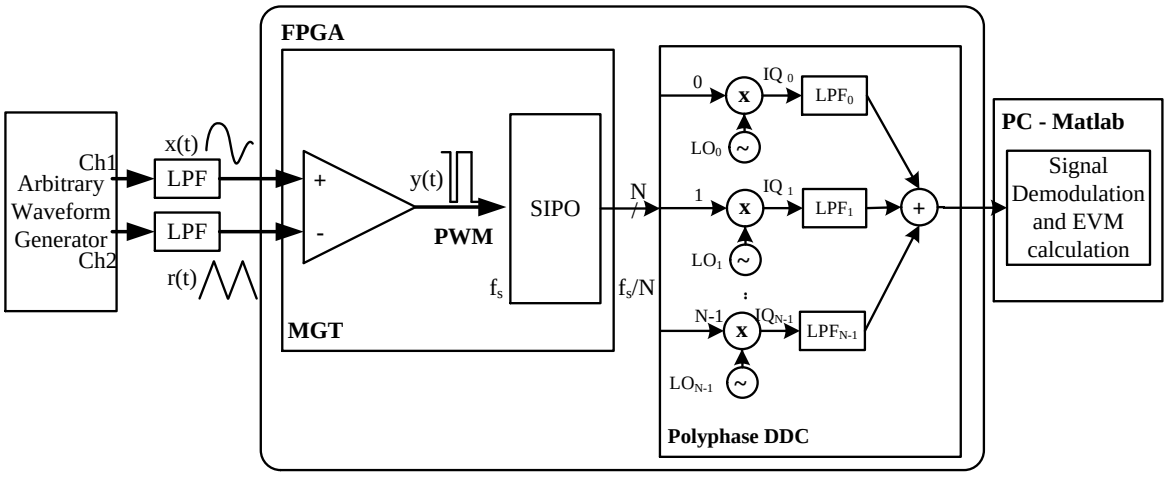


Figure 22 - Block diagram representation of the laboratorial setup to assembled in order to validate the proposed architecture of Figure 21.

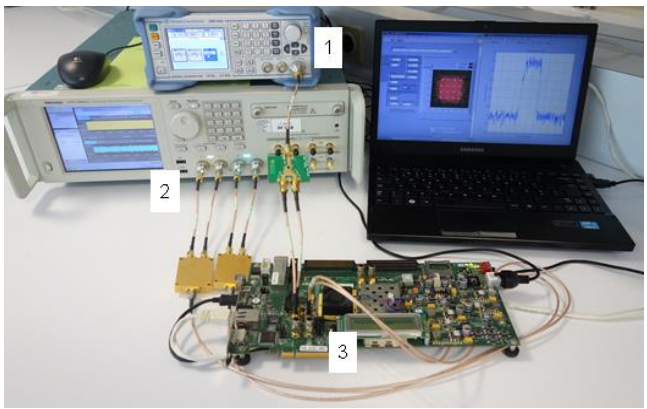
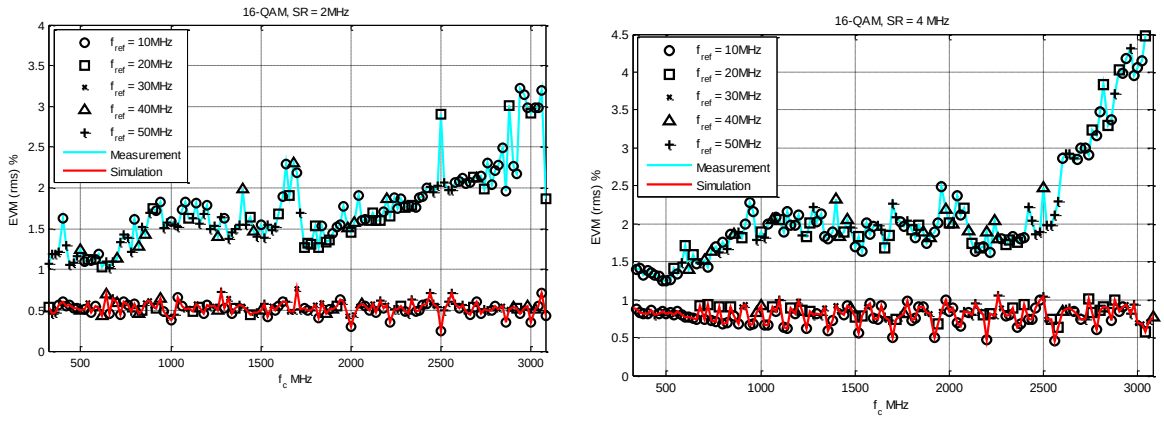


Figure 23 - Photo of the laboratorial setup. 1 - Clock generator; 2- AWG; 3 - KC705 development kit.

With this setup, a sweep over the carrier frequency for the same modulated signal was performed testing at each f_c different reference signals frequencies. This setup allowed to successfully validate the proposed idea. The results of this preliminary evaluation were shared in two conference papers [C2, C3] presented in Appendix C.

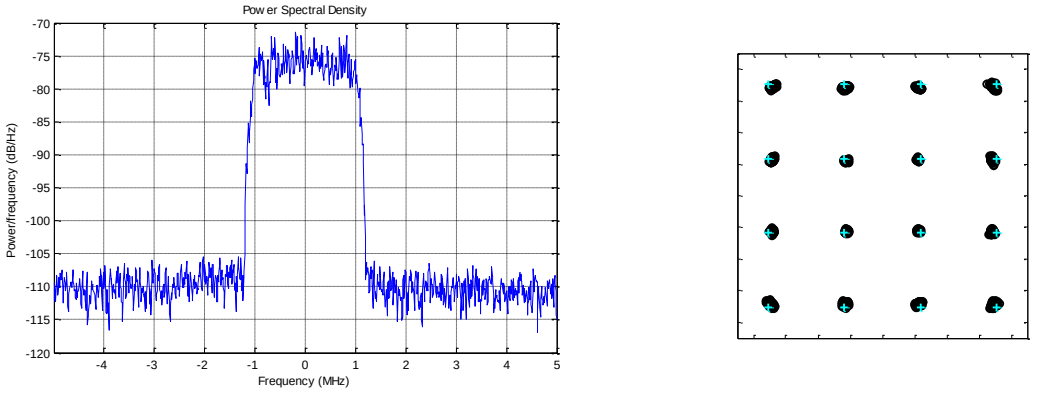
Briefly, in this first evaluation it was shown that a 16-QAM modulated signal with bandwidth up to 4 MHz can be successfully recovered with a reasonable SNR, in about 3 GHz of spectra. Figure 24(a) and Figure 24(b) present simulation and measurement results of the previous described sweeps for 2 MHz and 4 MHz signal bandwidth, respectively. It is important to state that the simulation considered an ideal comparator, which is far from reality, being that the main responsible of such a difference between the simulation and measurement results. However, by inspecting Figure 24(a) it is possible to observe that the simulation results produce an almost constant EVM near 0.5 %, while regarding the measurement results the EVM is always lower than 2 %, i.e., SNR higher than 34 dB, for carrier frequencies below 2.5 GHz. Figure 24(b), shows the same sweep for a 4 MHz, in which it is possible to verify a increase in the obtained EVM, altough is still lower than 2.5 %, which corresponds to 32 dB of SNR. Both the previous presented sweeps present an increase of EVM above 2.5 GHz, that can be explained due to mismatch impairments at the FPGA input, and to non-idealities of the input comparator. Figure 25 presents the baseband spectrum and the constelattion diagram of an acquisition with a 16-QAM 2 MHz signal centered at 1800 MHz with an EVM_{rms} around 1.54 %

The previous results proof the high flexibility of these architecture, while mantaining a reasonable performance in almost 3 GHz of bandwidth. However, it is important to realize that at this stage the RF receiver was not optimized, which will be the focus of the next sub-section.



(a) (b)

Figure 24 - Measured and simulated results of a sweep over the carrier frequency using a 2MHz 16-QAM modulated signal (a) and 4MHz 16-QAM modulated signal.



(a) (b)

Figure 25 – (a): Baseband frequency domain representation of an acquired 2 MHz 16-QAM signal centered at 1800 MHz. (b): Constellation diagram representation of the same acquisition (EVM_{rms} = 1.54 %).

To conclude this sub-section, it is important to state the work developed at this point originated a live demonstrator of an all-digital radio concept, in which the receiving part of that radio was built considering the knowledge presented in this sub-section. The live demonstrator is associated with the paper [C4].

4.2. PWM RF receiver optimization

In this sub-section the focus is on the RF receiver optimization, mainly targeting SNR and bandwidth by studying the PWM modulation process based on the models presented in [33], [56].

Having in mind the diagram of Figure 6, as also the content addressed in section 2.2.2, it is important to recall that the PWM modulation process is highly non-linear, creating a huge amount of distortion. The natural PWM waveform (*p(t)*), waveform immediately after the comparator and before the register, is a square wave with variable duty-cycle, which presents an infinite spectrum, as shown in spectrum before sampling in Figure 26. Then, the single-bit register running at f_s, samples the continuous time *p(t)* waveform, generating a discrete-time *p(n)* PWM waveform. As already mentioned, the relation $f_s > 2f_c$ imposes the signal of interest *x(t)* to be in the first Nyquist zone (NZ). However, the sampling process causes a frequency overlap at the first NZ due to the aliasing of PWM harmonics coming from higher NZs, as shown in Figure 26 after sampling. This aliasing is unavoidable, since an antialiasing filter cannot be included between the comparator and the register, in order to maintain a two-level signal. The use of a binary signal allows to simplify the sampling hardware to a single-bit register. Therefore, an analysis of the *p(t)* PWM spectrum signal should be considered, in order to understand how this overlapping in the signal's band of interest can be avoided.

In [56] a general mathematical model to approximate (2) is presented (19), and is valid for every *x(t)* signals:

$$p(t) = x(t) + \frac{2}{\pi}\sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty}\frac{1}{n}e^{jn\omega_r t}\sin\left(\frac{n\pi}{2}\left(1+x(t)\right)\right) \quad (19)$$

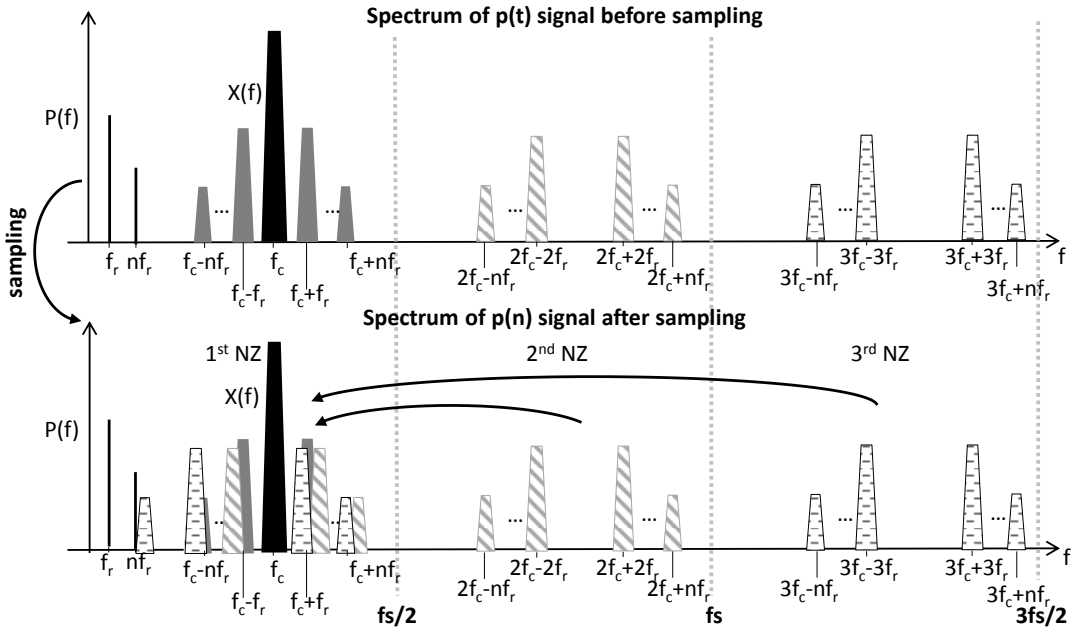


Figure 26 - Conceptual representation of the PWM signal spectrum, in the first three NZs, before and after sampling.

where ω_r is the angular reference signal frequency and *x(t)* is the RF signal that can be described as $x(t) = x_{BB}(t)\sin(\omega_c t)$, where $x_{BB}(t)$ is the baseband signal's complex envelope modulated by a carrier centered at ω_c. The previous expression can be further simplified using well known trigonometric identities, in such a way that is possible to apply Fourier Transform in order to obtain an approximation of the spectrum of the continuous-time RF PWM signal (*p(t)*). In this context, approximation of the spectrum means, that is possible to know the power and central frequencies of each PWM harmonic, as shown in spectrum before sampling in Figure 26. Therefore, considering a certain level of required or imposed SNR for a given bandwidth, it should be guaranteed that the PWM harmonics do not fall over the interest band in the first NZ. For this purpose, knowing this spectrum approximation, it can be developed an algorithm to compute an optimized reference signal frequency that allows to roughly reach a given SNR. The reference signal, f_r, was selected as the control variable of the algorithm, due to the fact that it is intended to let the register sampling frequency f_s fixed, because it leads to a simpler DSP circuitry. This process is explained in detail in Section III.B of the paper [J2] presented in the Appendix C.

In order to exemplify the proposed algorithm, Figure 27 presents the simulation results of the proposed receiver considering an ideal comparator. The simulation was performed considering a carrier frequency of 1650 MHz and a 16-QAM signal with 5 MHz of symbol rate (i.e., a channel bandwidth (*BW*) of 6.1 MHz due to signal generation with a

raised cosine filter with a roll-off of 0.22). The minimum reference ($f_r = 2BW$), which is 12.2 MHz, but in order to have margin for filtering it was used 14 MHz as the minimum reference. The optimized reference after computing the proposed algorithm is 30.9 MHz. As it is possible to verify in Figure 27, the signal's spectrum using the minimum reference frequency presents a degraded SNR when compared with the spectrum with the optimized reference (given by the algorithm). In fact, after computing the EVM of both situations an SNR improvement of 9 dB was verified, which validates the proposed optimization algorithm for reference frequency selection.

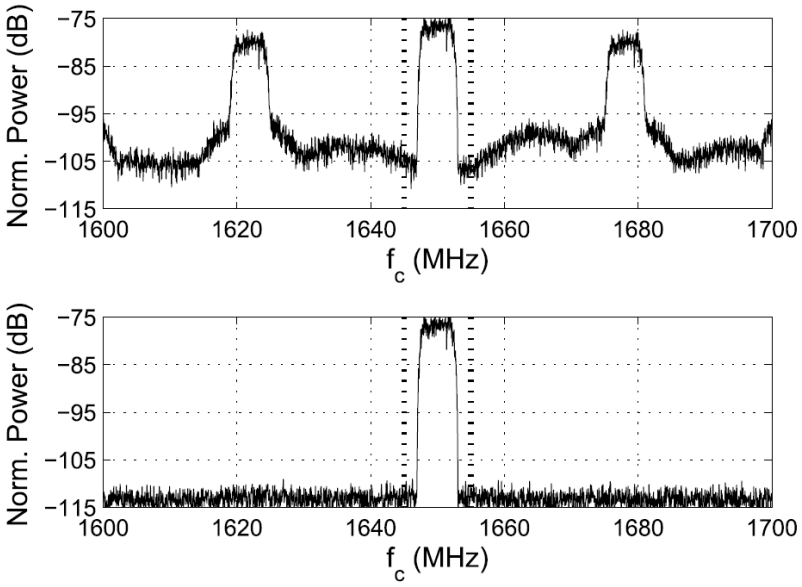


Figure 27 - Receiver simulation results without and with best reference calculation, top and bottom plot, respectively.

Detailed measurements and additional remarks about this technique can be found in paper [J2] presented in the Appendix C. However, similar characterization based on a sweep with AWG and FPGA as previously presented was performed. The FPGA sampling frequency was the same as used in the results presented in the previous section, i.e., 10 GHz. For each carrier frequency, the reference signal frequency was previously optimized, considering the previous optimization algorithm. The EVM sweep results for 2 MHz and 5 MHz symbol rate signals are shown in Figure 28. In both these sweeps, it is possible to see the points that were measured using the minimum reference and optimized reference. The points measured with the minimum reference represent points in which the algorithm was not able to optimize further, simply due to the alias free condition of those carriers. The use of the optimized reference allows for the EVM to be maintained relatively constant for the swept carrier frequencies, despite of the PWM folded harmonics.

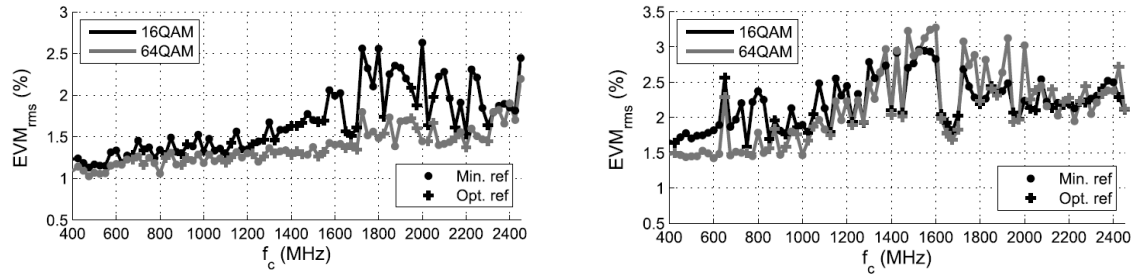


Figure 28 - Receiver EVM measurement. (a) 2-MHz symbol rate signal. (b) 5-MHz symbol rate signal.

When comparing this system with [25], focusing on the 5 MHz signals, it is possible to realize that there were improvements in terms of SNR/EVM. Despite the fact that in [25], the PWM sampling is two times higher to the 10 GHz used in this work, the proposed technique allowed to obtain an EVM lower than 3.5%, whereas in [25], the presented EVM is about 6%. Moreover, when comparing this results with the results presented in the last section, an improvement was also obtained. Both the previous improvements are due to the proposed technique for the reference frequency selection.

Another important metric in terms of receiver evaluation is sensitivity and dynamic range. For this purpose the LNA/VGA should be mandatorily included, which falls out of the scope of this Ph.D. work. However, it is possible to get an estimation of the instantaneous dynamic range transposing the EVM values into SNR by applying the formulation presented in [57]. Therefore, considering that the best and the worse obtained EVM values are, respectively, 1 % and 3.5 %, by applying the previous formulation it is possible to get an SNR between 40 dB and 30 dB. Hence, this leads to an indicative value of the receiver instantaneous dynamic range.

Finally, despite the receiver optimization in the paper [J2], it is also included the integration of the FPGA based receiver with the well-known FPGA based all-digital transmitters. The transmitter design falls out of the scope of this Ph.D. work, however more information about this can be found in paper [J2] as also in [13], [29], [30]. The integration of these works leads to an innovative agile all-radio transceiver, in which the results show the feasibility of this approach as a more flexible alternative to common radio architectures. Additionally, in the paper [C5] such type of integration is also addressed, including initial results of the work described in this section.

4.3. Applications

Bearing in mind the previous optimized version of the PWM receiver, two important application scenarios will now be addressed. The first scenario targets a standalone RF receiver operation in a C-RAN architecture, which is considered one of the key enabling technologies for the 5G networks (supported by paper [C6]). The second

application scenario makes the bridge between the first part of this Ph.D. work and the second part, presenting a feedback loop for DPD using the proposed FPGA-based PWM all-digital receiver (supported by paper [J3]).

4.3.1. Remote PWM RF receiver

As referred in the Introduction of this work, the C-RAN architectures are one of the key enabling technologies for the 5G networks [2]. The main concept of C-RAN is the centralization of the signal processing and management tasks, removing them from the radio access units [2], as depicted in Figure 29. Briefly, this new architecture is based on the following three components:

a) A pool of central units (CUs) that are responsible for the management and signal processing;
b) A set of distributed Remote Radio Heads (RRHs);
c) A high-bandwidth and low-latency optical or microwave transport layer (fronthaul) between the CU and the RRHs.

This centralized architecture brings efficient interference management between RRHs, spectral efficiency, flexibility and support of high data rates [2]. In order, to take the highest profit of the C-RAN paradigm, the RRH should ideally present a simple, low power and low cost architecture.

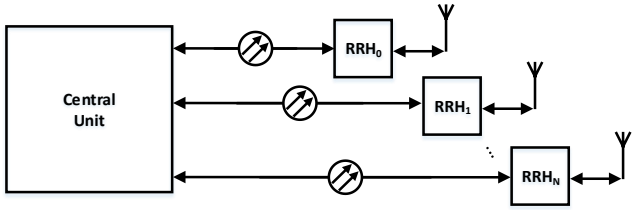


Figure 29 - C-RAN block diagram scheme composed by a CU connected to several RRHs through an optical transport layer (fronthaul).

Actually, this topic related to the RRH is already being addressed by the scientific community. In [58] an all-digital transmitter architecture using delta-sigma modulation (DSM) or PWM based on digital-radio over fiber (D-RoF) with a simple RRH was presented, answering the previous requirements for the RRH downlink section. Additionally, in [59] an entire base station system was presented with a transmitter section similar to [58], and with a receiver chain also based on PWM but without taking full profit of the PWM representation of the analog signal, due to the unnecessary use of conventional analog down-conversion architecture in the CU.

The idea within the work presented in this sub-section is to conceive and design a remoted version of the PWM converter using an electro/optical (E/O) converter based on a small form-factor pluggable (SFP) device.

The proposed receiver architecture for a C-RAN scenario is presented in Figure 30 and it is divided into three main blocks: an RRH, an optical transport layer and the CU. Following the diagram of Figure 30, it is possible to observe that after the antenna, the RRH starts with a bandpass filter responsible to select the bands to receive, followed by an LNA/VGA that performs low noise adaptive gain in order to put the signal level accordingly with the reference waveform (*r(t)*). Since the SFP laser driver presents a high bandwidth differential input, these inputs are used as a comparator. Therefore, both the RF signal *x(t)* and *r(t)* feed the SFP inputs, which will generate a PWM representation of *x(t)* that will drive the optical laser. Then, the optical fiber will carry a two-level optical signal containing the RF signal information within a PWM continuous time waveform. The transport layer is connected to the CU that will receive the optical signal with other SFP receiver, which is responsible to convert the optical signal back to the electrical domain (*p(t)*). The *p(t)* signal is acquired by the high speed inputs of an FPGA-chip, and from that point on, everything is similar to what has already been previously discussed in this Chapter.

In terms of validation and measurement setup, the only difference regarding the setup of Figure 23 is the inclusion of the E/O converter (AFBR-709SMZ from Avago and working at a wavelength of 850 nm) between the AWG and the FPGA, as it can be seen in Figure 31. Figure 32 presents the RF signal spectrum of an acquired 64-QAM 5 MHz signal centered at 1815 MHz and also the signal's constellation diagram.

More details about this work regarding implementation measurements, and comparison with [59] can be found in the paper [C6] presented in the Appendix C.

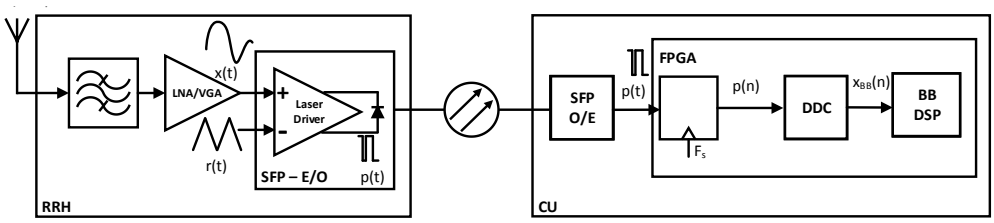


Figure 30 - Comparison between the proposed receiver architecture.

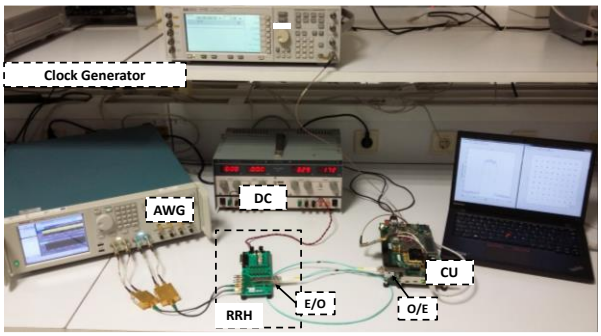
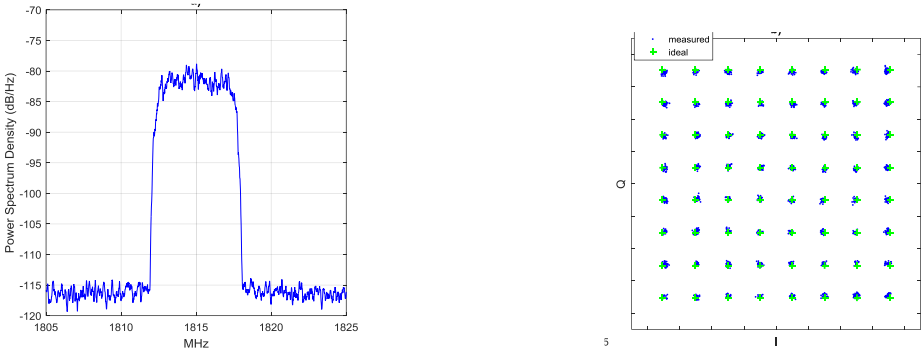


Figure 31 - Photo of the implemented and measurement setup.



(a) (b)

Figure 32 - Acquisition of a 5 MHz 64-QAM modulated signal centered at 1815 MHz. (a): Frequency domain representation; (b): Constellation diagram with EVM_{rms} of 1.43 %, which corresponds to an SNR of 36.9 dB.

4.3.1. Agile PWM-based DPD feedback loop

The final application of the designed PWM receiver is in a scenario of DPD, i.e., using it as a feedback for PA linearization. Additionally, it will also be studied the DPD application using the receiver in a remote scenario, suitable for future C-RAN networks, in which the DPD can be performed in a central unit (CU), far from the PA. The target of the proposed system is both simplicity and high flexibility.

Figure 33(a) presents the proposed block diagram representation of an RF transmitter with an all-digital feedback loop for DPD, in which it is used an FPGA-based RF PWM ADC. By analyzing Figure 33(a) diagram, it is possible to verify that the transmitter section has not been changed, being the same as presented in Figure 10. However, the observation path is now quite simpler than the one in Figure 10. In fact, after the coupler the only required analog component is a variable attenuator in order to avoid the ADC clipping, which is also required in traditional architectures. Thereafter, there is immediately one of the comparator's inputs, while the other is used for the reference waveform *r(t)*. Despite not shown in the diagram the *r(t)* signal can be generated using the FPGA high speed output following similar techniques as presented in [13], [29], [30].

Consequently, after the comparator, in which the signal is sampled at a frequency f_s, an uniform sampling PWM signal containing the signal *y(t)* information is available to be processed digitally. Therefore, by using a DDC at f_c and a low-pass filter (LPF) it is possible to recover a replica of the *y(t)* LPE, represented in the diagram as *z(n)*. Afterwards, all the data is collected to apply a common SISO DPD algorithm as already explained in the previous Chapters.

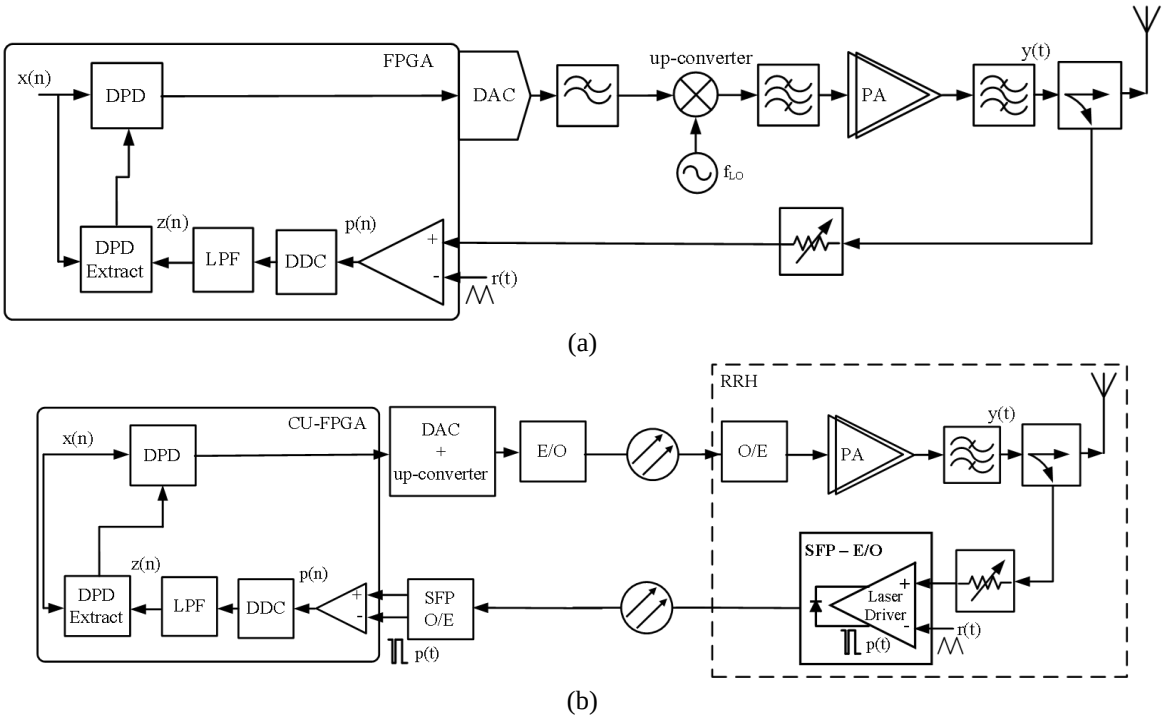


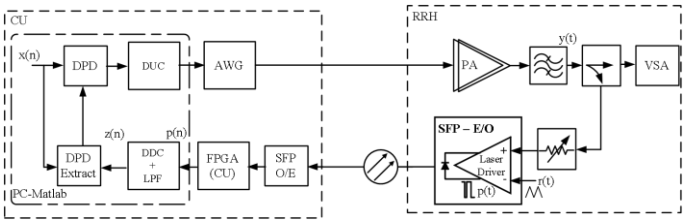
Figure 33 - Block diagram representation of an RF transmitter with an FPGA-based all-digital feedback loop receiver for DPD. (a): feedback loop assembled in conventional architecture and (b): feedback loop assembled in remote architecture based on RRH for C-RAN.

Having in mind the remote C-RAN architecture proposed in the previous sub-section, it is easy to understand that Figure 33(a) scheme can be easily modified to provide remote capabilities with a simple RRH in which the complexity is moved to the CU, as presented in Figure 33(b). Focusing on the proposed feedback loop for PA linearization of Figure 33b), it is possible to realize about the similarities with the previous described architecture of Figure 30 where a Small-Form Factor (SFP) E/O transceiver is again used. Hence, the reference signal *r(t)* and the *y(t)* attenuated signal feed the SFP inputs, consequently producing a PWM representation of *y(t)*, that will drive the optical laser. Afterwards, an optical fiber path transports a two-level optical signal containing the RF signal's information. At the Central Unit, the fiber path is connected to another SFP transceiver, which is used as a photo diode to receive the optical signal and convert it again to the electrical domain *p(t)*, which is then acquired by the FPGA-based all-digital receiver. Afterwards all data is gathered in order to apply a DPD algorithm as explained in the previous Chapters. This architecture enables a new concept of Centralized-DPD, in which several PAs can be remotely linearized by applying DPD at the CU.

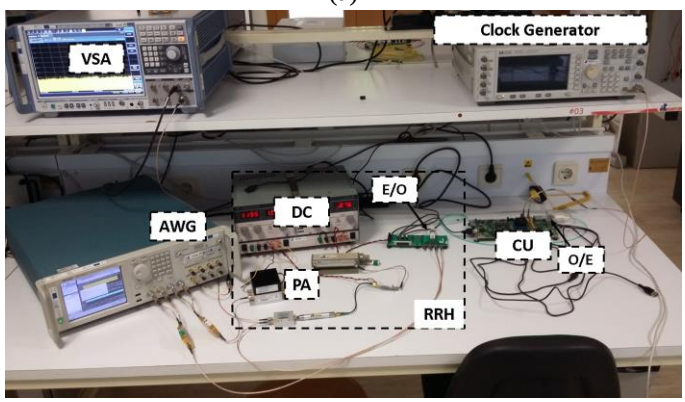
To experimentally corroborate the proposed feedback loop architecture and to mimic the scenario of Figure 33(b), a laboratorial setup was assembled accordingly to the block diagram representation of Figure 34(a). In order to simplify the measurement setup no fiber path was used in the transmitter chain, therefore the AWG is directly connected to the PA. The PA block is made by a Mini-Circuits ZHL-1042J followed by an ERA-4+. Despite not shown in the block diagram, the AWG is also responsible to generate the *r(t)*

signal. The feedback loop receiver comprises an SFP optical transceiver (AFBR-709SMZ from Avago), working at a wavelength of 850 nm. The same SFP is used in the CU. The latter is connected to a medium-range FPGA development board KCU105. The FPGA differential inputs were set to operate at a sampling rate of 16 Gbps. At the output of the PA, a VSA FSW8 from Rohde & Schwarz, was used in order to measure the PA performance before and after applying DPD. Additionally, in order to fairly compare the proposed system, the same VSA was also used to mimic a traditional feedback loop. Figure 34(b) presents a photograph of the assembled laboratorial setup.

The measurements were performed with 16-QAM modulated signals considering different bandwidths such as 5 MHz, 10 MHz and 20 MHz, which are the most commonly used in nowadays wireless cellular communication systems. Each of these signals has 6.1 dB, 6.2 dB and 7 dB of peak-to-average power ratio (PAPR), respectively. Additionally, in order to show the system's flexibility the following carrier frequencies were tested: 700 MHz, 915 MHz, 1800 MHz, 2400 MHz and 3450 MHz. Figure 35 presents the obtained results in terms of spectrum of the signal before and after applying DPD, amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM), for the specific case of a 20 MHz 16-QAM signal centered at 1800 MHz. An ACPR of 48 dBc was achieved both with the proposed feedback loop and the traditional one. More details about this work regarding implementation and all measurements results can be found in the paper [J3], presented in the Appendix C.

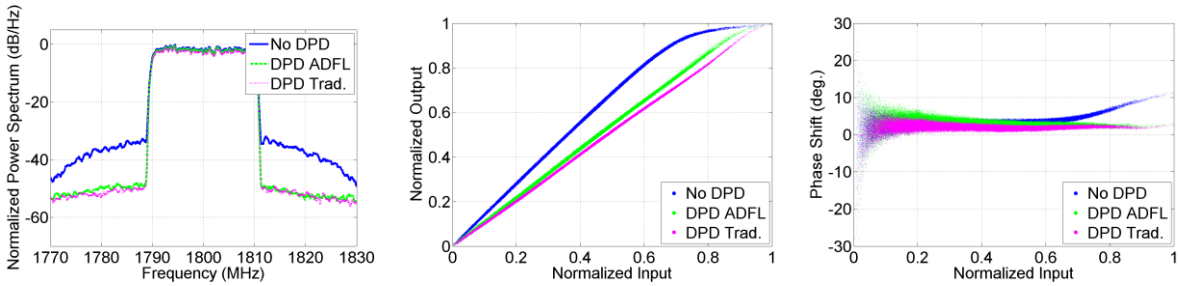


(a)



(b)

Figure 34 – Block diagram of the measurement setup All-digital feedback loop measurement setup (a) and photo of the laboratorial setup (b).



(a) (b) (c)

Figure 35 - DPD results: Spectrum before and after applying DPD with ADFL and with traditional one, AM-AM and AM-PM plots. (a)-(c) Results with f_c at 1800 MHz and BW of 20 MHz. [ADFL – all-digital feedback loop; Trad. – Traditional feedback loop].

4.4. Summary and concluding remarks

This Chapter, together with the supporting papers, presented the design procedure of an FPGA-based RF PWM all-digital receiver. Firstly, the feasibility of designing such a receiver with an FPGA was evaluated, showing promising results in terms of frequency agility as also integration (paper [C2] and paper [C3]). However, at this stage with a behavior still not completely understood.

Therefore, the following work of paper [J3] addressed this topic, explaining the behavior of such converter and proving a procedure to optimize the selection of the reference frequency in order to optimize BW and SNR. Additionally, the integration was also addressed, showing the feasibility of having an all-digital transmitter and receiver integrated in the same FPGA chip, while maintaining reasonable EVM results for 2 and 5 MHz symbol rate signals. The obtained results make this system highly suitable for the future radio transceivers, specifically focusing on the integration of previous standards that operate in sub-2.5-GHz bands. An FPGA was used as an implementation proof of concept, due to its faster verification and deployment capability. Nevertheless, an application specific integrated circuit could also be built following the proposed architecture. However, due to the FPGA's reconfigurability capabilities, an increased degree of flexibility required by SDR applications is added. Within this context, a live demonstrator of an all-digital transceiver was successfully achieved (paper [C4]).

Afterwards, two important applications were shown in which the system is used in a C-RAN scenario serving as a standalone receiver as also DPD feedback loop (paper [C6] and paper [J3], respectively). A C-RAN is a very important topic for 5G networks, but also within this context is very important to consider the system's scalability. In order to perform this evaluation, let us consider the FPGA used in the work of paper [J3], the XCKU040-2FFVA1156E, which is the FPGA chip used in the KCU105 development board. As already previously mentioned, the FPGA I/Os that allow to implement receivers such as the one presented in this work, are commonly known as Multi-Gigabit Transceiver (MGT). Each MGT allows to build a different receiver. The referred FPGA chip contains

20 MGTs, which would allow to implement 20 different feedback loops. This fact is also important for the next chapter regarding massive MIMO systems.

Finally, it is important to state that the main focus of the work was the evaluation of performance and feasibility to provide flexible, agile and integrated all-digital receiver platforms, and that the FPGA was mainly used due to its fast prototyping capabilities. The power consumption of such systems is also a very important metric to be evaluated, which the author recognizes as the main bottleneck regarding the performed evaluation. The use of FPGA development kits makes the evaluation of such metric difficult to perform, since to the best of the author's knowledge, it is not possible to measure the power consumption of a single MGT, at least when the FPGAs are used in development kits. However, the Vivado program, i.e. the integrated development environment for the FPGA project development, provides a power consumption estimation. Therefore, within the project designed for the paper [J3] (with MGTs working at 16 Gbps) and considering an estimation for a single MGT, which is the element responsible for the analog to digital conversion, the amount of power is 342 mW, from 4.5 W of the total FPGA power consumption. It is important to have in mind that the 4.5W of the total FPGA power consumption, consider a usage of 4 MGTs (because MGTs are instantiated in groups of 4, called *QUADS*), BRAM usage for data storage, microprocessor (MicroBlaze) and ethernet cores for the communication with the control computer, clock distribution and remaining control logic. Using this indicative value of 342 mW to perform a comparison with an RF ADC, for example the ADS5400 [23] used in the Chapter 2 that presents a maximum power consumption of 2.15 W, may give a good indication towards power savings in specific applications. On the other hand, the RF ADCs present a highly superior performance. However, this work was a first step, and future improvements regarding the RF PWM converters may be expectable.

5. Integration and assessment of DPD feedback loops for multi-antenna systems

This chapter reports the last topic addressed in this Ph.D. work, regarding integration and DPD feedback loops for multi-antenna systems. As already mentioned in the Introduction of this thesis, multi-antenna transmitter architectures such as beamforming and massive MIMO pose as strong candidates for both 5G and pre-5G (sub 6 GHz bands) systems. The use of these techniques allows an increase in the communication throughput (parallel data streams and interference reduction) [1]. Both these techniques require a large number of concurrent transmitters, which immediately impose several challenges in terms of integration, scalability and cost. The two main targets of this chapter are the integration of multi-antenna systems and the assessment of the implementation of DPD feedback loops in the same context.

The first sub-section of this chapter identifies the circulator as a critical element that prevents the integration and scalability of such type of systems. An analysis about the consequences of the circulator removal is performed and is proposed a technique to enable such possibility. This sub-section is supported by the paper [C7].

In the second sub-section a brief assessment about DPD feedback loops for multi-antenna systems is performed, proposing different architectures to build feedback in these type of systems.

5.1. Circulator free multi-antenna transmitters

In this sub-section are mainly considered multi-antenna transmitters based on Time Division Duplexing (TDD), which is expected to be the case of massive MIMO systems, due to the possibility of sharing channel state information (CSI) [60].

Figure 36 depicts an example of a multi-antenna transmitter architecture based on the current Time Division Duplexing (TDD) LTE MIMO systems. Additionally, two receivers for data and another to perform linearization via DPD are also included. Since the PA requires a stable load to operate properly, a circulator is used to isolate the PA output from the antenna and to reduce the input power level requirements of the switch. However, the future multi-antenna transmitters will not process individual high power but medium power signals. Therefore, an RF switch-based solution becomes feasible (blue part in Figure 36), being possible to remove the circulator and allowing for higher integration, scalability, reduced bill of materials and cost effectiveness. The circulator is usually a bulky device, and its removal was also already considered in [61] in order to achieve integration gains.

However, in the scope of a multi-antenna array transmitters, the circulator removal brings a new problem, which is the PA becomes affected by the mutual coupling between antennas [62]. This phenomenon will produce a variation in the antenna input impedance

(i.e., PA load variation), which will cause the PA to decrease its performance (efficiency and linearity), and degrade the EVM of the transmitted signal. In [63] this problem was already verified in terms of non-linear effects depending on the distance between antennas. In [61] the mutual coupling effects were emulated by directly connecting two PAs using a variable attenuator, and metrics such as ACPR and EVM have been analyzed depending on attenuation.

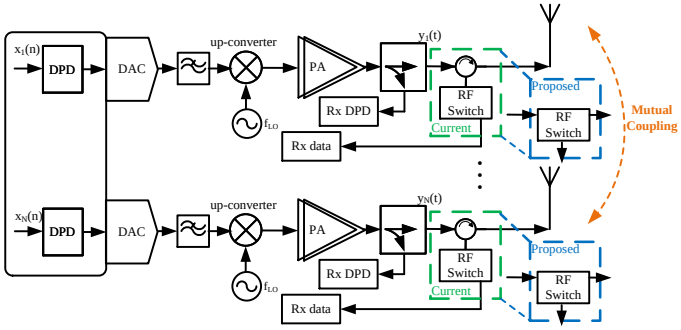


Figure 36 - Multi-antenna transmitter architecture based on conventional approach using circulators together with RF-switches, and proposed architecture using a single RF-switch (blue).

To exemplify the mutual coupling problem in an antenna array we will focus on a 3x3 patch antenna array simulated and designed in CST (Computer Simulation Technology) for f_c = 2.375 GHz with equal horizontal (d_x) and vertical (d_y) distance between patches as depicted in Figure 37(a).

It is important to define the single element input impedance, which is the one of a patch when individually excited. On the other hand, there is the active element input impedance (or scan impedance), which corresponds to the one of a given element when two or more elements are simultaneously excited [62]. This impedance variation depends on several factors such as, array configuration, spacing between elements and the phase difference applied at each element. In [62] it is shown that by knowing the S-parameter matrix of the array obtained with single individual excitations it is possible to find the active input impedance for a given simultaneous excitation.

Therefore, considering the array configuration of Figure 37(a) and by applying the formulation presented in [62], the active input impedance can be computed. Figure 37(b-c) present both the single and active element input reflection coefficient in terms of magnitude and VSWR for the central patch antenna, which is the one more prone to this issue. Additionally, two cases are presented with $d_x = d_y = 0.75\lambda$ and $d_x = d_y = 0.5\lambda$ (d_x and d_y respectively correspond to the horizontal and vertical distance between patches). Focusing on the VSWR, it is possible to verify that at f_c it has suffered a variation from 1 to 1.5 in the 0.75λ case and from 1 to 2 in the 0.5λ case. This will obviously impose a new load to the PA, which, in turn, acts as non-desirable load modulation that will degrade the overall transmitter performance when no isolator is present.

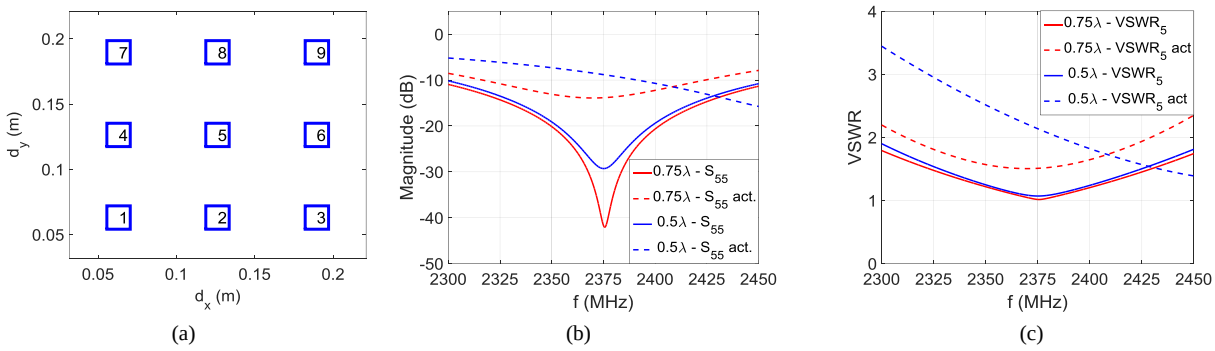


Figure 37 – (a): 3x3 patch antenna. (b)-(c) Single element and active element (dashed line) input impedance in patch 5 in terms of S_{55} (magnitude) and VSWR.

Within this context, a solution to mitigate the previous referred problems based on digital compensation performing both linearization via DPD and also compensation of the mutual coupling effect was proposed and evaluated. However, before presenting the proposed technique it is important to realize that there are also circuit-based techniques to design antennas in order to minimize the mutual coupling effect [64]. Though, as also referred in [64], these solutions are usually complex and may result in narrowband matching performance. Additionally, increasing the space between antenna elements could be considered as the simplest solution. However, this immediately produces a negative impact in both radiation pattern as also in the array physical size, which is even more significant for the sub 6 GHz frequency bands.

The proposed solution target is to eliminate the interference that appears at the load of the PA and cancel the mutual coupling effect and improve the Figures of Merit (FoM), such as efficiency, ACPR and EVM. In fact, the currently existent DPD models for 2 transmitters MIMO scenarios, already allow to compensate for both non-linear and linear cross-talk [49], [50], therefore they can easily be used to implement this process. More details about the proposed solution can be found in the paper [C7], presented in the Appendix C.

To experimentally validate the proposed technique, a measurement setup with two concurrent transmitters was assembled (similar to Figure 36 architecture). This is composed by a dual-channel transmitter from TI (TSW38J84) and an RF ADC also from TI (ADC12J4000). Despite only two antennas were used several VSWR tests were performed. The PA used in each lane is a 6W ultra-compact 2-stages LDMOS MMIC Class-AB PA and the patch antennas were designed for f_c at 2.375 GHz. The coupler was also designed to allow that the transfer function between the input to the coupled port and from the output to the coupled port present the same response. This is mandatory because the feedback loop must acquire a replica of the overall signal presented at the output of the PA (not possible with a standard coupler due to the isolation between the output and the

coupled port). An alternative could be using a bi-directional coupler and a combiner. The signals used during the measurements were 16-QAM modulated signals with 12 MHz bandwidth and approximately 8 dB of peak-to-average power ratio (PAPR). Figure 38 presents a photo of the measurement setup assembled for this laboratorial test.

Several different measurement scenarios were considered as presented in Figure 39. Firstly, a measurement without the presence of any mutual coupling effect in which the PAs are individually (and one at a time) connected to each antenna, Figure 39(a). These measurements will give the best reference FoMs (configuration (a)), and are similar to the ones obtained if a circulator would be used. Secondly, it is necessary to test in a mutual coupling scenario, in which the antennas are placed side-by-side spaced of 0.5λ (configuration (b)), Figure 39(b). This scenario corresponds to a VSWR of about 1.2. The last scenario is solely aimed to test a higher VSWR condition in which the antennas are placed face-to-face (configuration (c)), Figure 39(c).

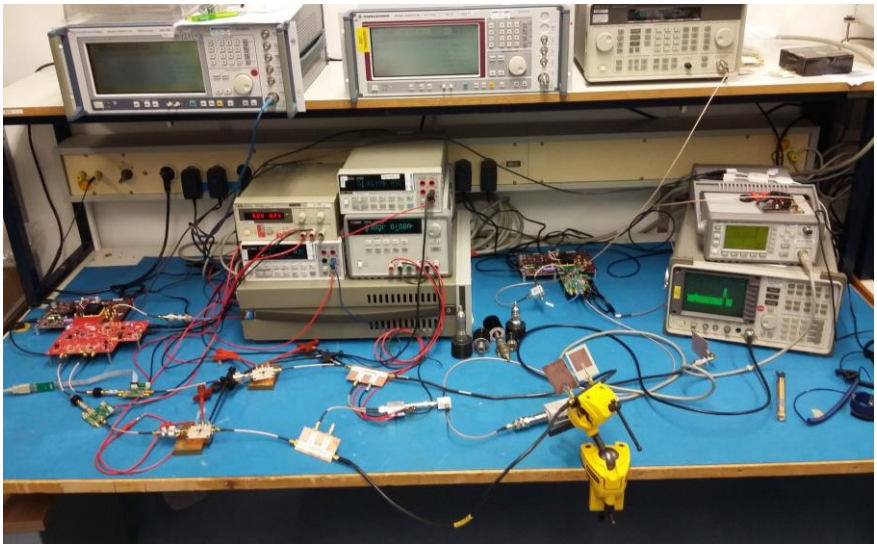
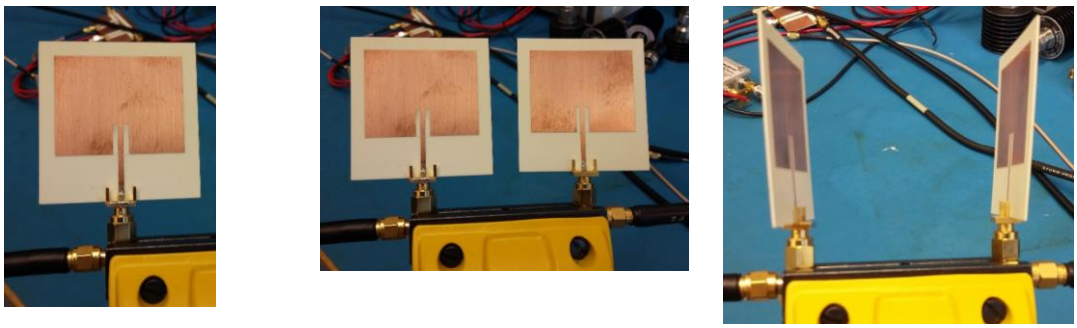


Figure 38 – Photo of the multi-antenna transmitter setup.



(a) (b) (c)

Figure 39 – Photo of the three different configurations used for the antennas to emulate different VSWRs.

Even though this is not a real practical scenario, it allows to mimic the same VSWR existent in the central patch of a 3x3 array antenna. Additionally, several measurements were taken considering no DPD applied, SISO GMP DPD algorithm, MIMO DPD algorithm (equation 1 of paper [C7]) and back-off (BO) scenario (corresponding to the same linearity (ACPR) achieved with DPD).

Table 2 summarizes the obtained measurements results of the most important FoMs, considering the previously described scenarios, for the transmitter 1 (transmitter 2 has similar results).

As expected, in the configuration (a), without any mutual-coupling, both algorithms present similar results. In the configuration (b), light coupling, the MIMO algorithm is able to achieve better FoMs than with a common SISO algorithm. Comparing the MIMO algorithm with the BO operation, it is possible to conclude that despite similar linearity is achieved, the average efficiency using the proposed technique is about 44% higher (12.9% to 23%) and the EVM is lower than 1 %. Moreover, the average efficiency value was restored to the same value as in single antenna excitation (configuration (a)), which means that the interference waveform was completely eliminated. Focusing now on the configuration (c), heavy coupling, one may realize that the SISO model is not even able to reach 45 dBc of ACPR. On the other hand, the proposed method is able to keep reasonable performance in all the FoMs, while keeping the leverage over the BO operation in terms of average efficiency and EVM. Additionally, Figure 40 presents the spectrum of the measured signals at the coupled port of the PA 1 for the configuration (c).

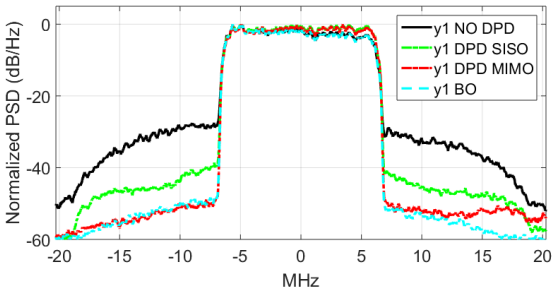


Figure 40 - Spectrum of the signals for each different test at the coupled port.

Table 2 – Summary of results in Tx1. (*) - -not possible to demodulate and measure an EVM value.

	no DPD		SISO DPD		MIMO DPD		BO (7dB)		Cfg.
Pout (dBm)	29.6		25.9		**26.0**		22.0		**a**
Eff. (%)	35.0		23.0		**23.0**		12.9		
ACPR (L/H) (dBc)	30/32		57/57		**57/58**		54/55		
EVM rms (%)	*		1.00		**1.07**		*		
PAPR (dB)	7.6	4.1	10	7.5	**10**	**7.5**	7.6	7.5	
Pout (dBm)	29.6		25.9		**26.1**		22		**b**
Eff. (%)	35.5		22.4		**23.0**		12.9		
ACPR (L/H) (dBc)	30/32		52/53		**55/55**		53/55		
EVM rms(%)	*		5.28		**0.92**		*		
PAPR (dB)	7.6	4.3	10	7.6	**11**	**7.5**	7.6	7.3	
Pout (dBm)	29.9		25.1		**25.9**		22.3		**c**
Eff. (%)	37.9		20.7		**22.0**		14		
ACPR (L/H) (dBc)	29/32		44/45		**52/51**		50/53		
EVM rms(%)	*		*		**1.38**		*		
PAPR (dB)	7.6	4.4	8.9	7.3	**11**	**7.6**	7.6	7.0	

5.2. Brief assessment of DPD feedback loops for multi-antenna systems

In this last topic of the Ph.D. thesis it is intended to briefly address different architectures for DPD feedback paths in the scope of multi-antenna transmitters. These systems are being envisioned to have a large number of antennas.

For example, the National Instruments multi-antenna platforms are capable to reach 128 antennas, and currently represent one of the easiest ways to implement laboratorial prototypes for these type of systems [65], [66] (Figure 41).

Figure 41 – National Instruments massive MIMO platform from [65]**.**

Considering the size scale of the platform presented in Figure 41, it is easy to understand how much it is important to work on integration and scalability issues of this type of systems. While, in the previous sections the integration problem was addressed by trying to provide a solution for the circulator removal, in this section the focus is on the scalability of DPD feedback loops in multi-antenna scenarios.

Figure 42 presents a diagram of a multi-antenna transmitter with one feedback loop path for DPD per PA. Similarly to what was presented in Figure 12, the cross talk (both linear and non-linear) is now an even more obvious problem. Before addressing the feedback issue it is important to realize that applying DPD in such type of systems may be a challenge due to scalability of the models, when intended to compensate both linear and non-linear interferences between concurrent paths. The modeling topic falls out of the scope of this Ph.D. thesis, however this is one the topics addressed in [52].

Focusing on the feedback loop issue, Figure 42, presents one feedback loop per PA, which is a solution that allows to monitor any behavior change in each PA, such as for example temperature, which may not be constant in all the array. Afterwards, in the digital domain, all the data from the output of each PA can be used to suitably model and pre-compensate for any change. In terms of observation, this topology should in theory allow to monitor all the necessary variables to be able to successfully solve the linearization problem of a multi-antenna transmitter. However, considering systems with a large number of transmitters such a solution may not be cost effective and may also prevent integration and scalability. Therefore, it is important to study alternative realizations for the feedback loops.

Some alternative realizations are presented in Figure 43, and can be described as follows:

- Use a time-switched (or time multiplexing) receiver to acquire the data of each transmitter in a different time frame (Figure 43(a)).
    - This solution is in theory feasible, and it can be somehow compared to the solution presented in [46], for 2D scenarios, and sharing some of the same pros and cons. A real time update of the DPD coefficients becomes more difficult, which may have consequences depending on the memory effects of the PA. Additionally, for a large number of PAs it may be not possible to use a single switch, but several switches embracing a group of PAs may be required.
- Use one feedback loop to acquire the combined signal from different transmitters (Figure 43(b)) from [53].
    - In [53], it is proposed to combine all the feedback signals and acquire the combined version. Therefore, using a suitable DPD model it is possible to extract a PD for each PA. However, in [53] only simulations results are considered, which do not totally validate the idea. The work of [53] can also be compared with the work presented in [47] for 2D scenarios, in which two mixers were used to place two different bands at the same frequency that would then be sampled by the same feedback loop. In [47], the needs of a

2D alignment procedure in order to eliminate for the different group delays of the different paths was pointed as one of the drawbacks. In a scenario in which the combiner presents a number of inputs higher than two, this problem may be even higher, demanding for powerful alignment algorithms, and stringent design requirements of flat and similar response between the branches of the combiner. Additionally, as seen in the previous scenario, it could also be possible to envision such a solution with a combiner dedicated to a group of PAs, since it would be very difficult to design a single combiner for a case with a large number of transmitters.

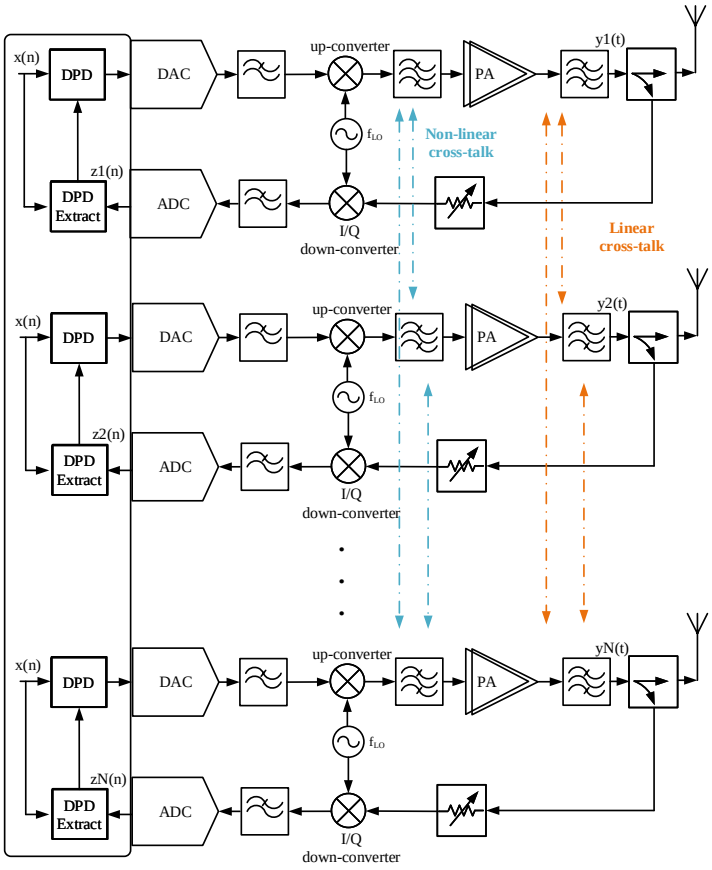


Figure 42 – Multi-antenna transmitter with one feedback loop per PA.

As one may realize, despite being different problems there are several similarities between the works related to the feedback loops in dual-band concurrent transmitters and multi-antenna transmitters. The work presented in this Ph.D. using non-overlapped statistical approximated multi-sine design [67] (paper [J1]), could also be adapted for a multi-antenna transmitter scenario. For this applications to be successful a combiner (or multiple combiners, i.e., considering a combiner per PA group) would be required. In this case the multi-dimensional alignment is not an issue, but massive non-overlapping multi-sine design would be required which may be challenging.

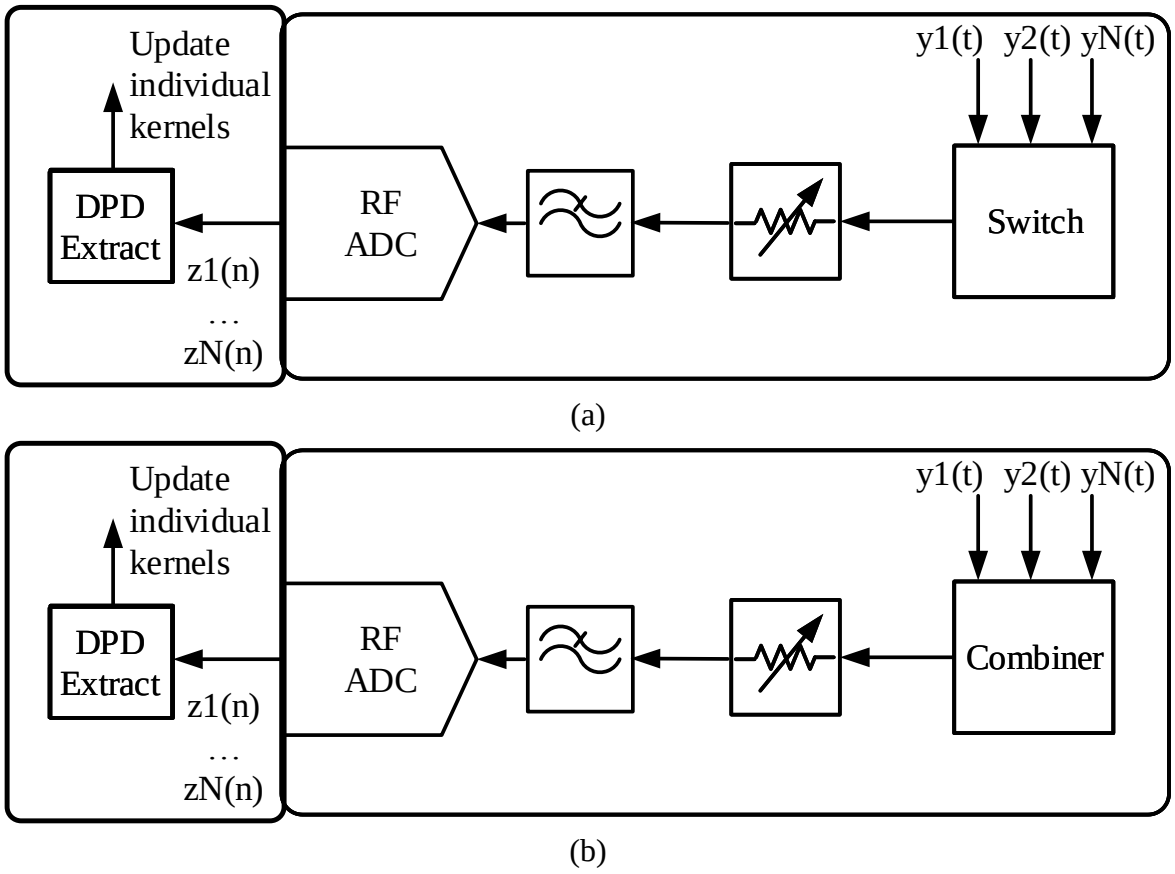


Figure 43 – Proposed alternatives for DPD feedback loops in multi-antenna transmitters: (a) switched feedback loop, (b) combined feedback loop.

All these techniques are valid possibilities for multi-antenna transmitter's feedback loops, however they all require a suitable experimental validation, in order to have a reasonable performance comparison of all the possibilities. Nevertheless, this evaluation puts stringent requirements in terms of laboratorial equipment, since a high number of parallel transmitters is required.

5.3. Summary and concluding remarks

This chapter addressed multi-antenna systems, which represent a very important technology for future 5G systems, focusing mainly on integration (circulator removal) and the architecture of DPD feedback loops.

The problems associated with the circulator removal (to increase integration levels) on multi-antenna transmitters were identified. A solution based on pre-compensation in the digital domain allowing at the same time to linearize and mitigate the mutual coupling effect was proposed and evaluated in a setup with antennas where different VSWRs were

emulated. This solution was able to solve part of the problems that appear with the circulator removal, and poses a first step towards future circulator free RF front ends.

Additionally, in the second part of this chapter an assessment about DPD feedback loops for multi-antenna systems was performed, proposing different possibilities to build DPD feedback loops in this type of systems. A suitable experimental evaluation was not performed, and is considered as a strong line of future work.

6. Conclusion and Future work

6.1. Conclusion

The work developed in the scope of this Ph.D. was focused on the SDR RF receiver system design and optimization using conventional commercial RF converters and the exploration of disruptive architectures based on pulsed SDR receivers enabling all-digital SDR platforms. The addressed receivers were targeted for usage in normal data reception (standalone with antenna) and feedback loop (or observation path) in a DPD scenario, where the relaxation requirements can be further explored to bring energy and cost savings. The focus on the later application scenarios highlights the importance of the developed work and shows its range of validity. This Ph.D. work contributed with several advances in the state-of-the-art that were summarized in this document.

The first chapter of this document presented the main motivations behind the study of this topic, it has introduced the objectives and identified the most significant contributions that have been made.

In the second chapter, a state-of-the-art review about RF receivers was presented, with a focus of their use for receiving unknown data at the antenna, and when used as observation path for PA linearization via DPD. During this review, the important challenges and research topics were identified and addressed in the subsequent chapters.

The third chapter of this document focused on the characterization and post-compensation of the feedback loop, towards increased DPD performance, which originated the publication [C1]. Additionally, a technique to relax the feedback loop requirements in a dual-band transmission scenario was presented and evaluated, which is associated with the publication [J1].

The fourth chapter of this work addressed the study and evaluation of an innovative FPGA-based RF single-bit pulsed converter based on PWM. The proposed receiver brought several advantages in terms of frequency agility and system integration. This research work originated the publications [C2, C3, C4, C5 and C6]. The proposed PWM receiver was optimized based on PWM theoretical behavior maximizing SNR and bandwidth, which is associated with the publication [J2]. Additionally, the proposed receiver was evaluated in a DPD scenario providing a simple and agile observation path for PA linearization. This last work originated the third journal paper associated with this thesis [J3].

The chapter five, focused in one of the most important topics for 5G, i.e., the multi-antenna systems, well known as massive MIMO systems, in which integration and scalability are very important metrics to study and evaluate. This originated the last contribution of this Ph.D. (paper [C7]), which is focused on the problems associated with circulator-free multi-antenna transmitters and how to solve them by implementing digital pre-compensation algorithm.

6.2. Future work

This thesis addressed the RF receiver design and optimization focusing on a normal usage of the receiver, in which the date is unknown and in a scenario used as DPD feedback loop, in which the original transmitted data is known. Therefore, regarding the first point it would be important to consider a future analysis of a receiver designed in a full chain with antenna and LNA, in order to consider FoMs such as sensitivity, which was out of the scope of this Ph.D. work.

Focusing on the designed FPGA-based PWM receiver, it is important to realize that its fundamental element used to build the comparator is the MGT. Usually these elements are implemented in *QUADS*, which present four MGTs. In all the developed work in this thesis, it was always used a single MGT, however it is possible to make use of a full *QUAD*, or even of multiple *QUADS*, targeting different objectives. For example, one objective could be the multi-antenna systems, simultaneously using several MGTs dedicated to each antenna. This topic was already addressed for the transmitter side in [68], and the same could be evaluated for the receiver. On the other hand, multiple MGTs could be used to build time-interleaved converters leading to an increase in BW or SNR. However, one may have to realize the challenges regarding synchronization requirements between MGTs to successfully enable the last two topics.

Finally, as mentioned in the previous chapter of this thesis, the subject of DPD feedback loops in the scope of massive multi-antenna transmitters, was just briefly addressed, several new research lines could be explored and investigated towards the design of efficient and low complex multi-antenna DPD systems.

Appendix – A - Additional DPD models

In this Appendix additional information about DPD models is provided, following the same reasoning as presented in Section 2.2.3.

SISO Generalized Memory Polynomial Model

The SISO Generalized Memory Polynomial Model (GMPM) is another model that presents higher complexity than the aforementioned MPM, due to the inclusion of additional memory cross-terms. This is the most widely used model for PA linearization via DPD and is usually more effective for a certain type of PAs in which the MPM is not effective anymore. The mathematical formulation is presented as follows [40]:

$$y(n) = \sum_{m_1=0}^{M_1} \sum_{m_2=0}^{M_2} \sum_{k=0}^{\frac{K+1}{2}} h_{(m_1,m_2.k)} x(n-m_1)|x(n-m_1-m_2)|^{2k}$$

where, M_1 and M_2 are the memory depths and K is maximum order of nonlinearity [40], [50]. The extraction of the model parameters can be performed following a similar reasoning as previously presented for the MPM model. The number of coefficients of the SISO GMPM model is given by:

$$N_{Coefs\ GMPM} = (M_1+1)(M_2+1)\left(\frac{K+1}{2}\right)$$

2D-MPM

As it was already previously stated, when a dual-band scenario is considered, a new behavioral modeling topology is required to include all the non-linear contributions which are now not only from the IMD products but also from the CM mixtures between the LB and UB. Therefore, to get improved performance a 2D model as presented in [43] is required:.

$$y_{LB}(n) = \sum_{m=0}^{M-1} \sum_{k=0}^{K-1} \sum_{l=0}^{k} h_{LB} x_{LB}(n-m)\,|x_{LB}(n-m)|^{k-l}|x_{UB}(n-m)|^{l}$$

$$y_{UB}(n) = \sum_{m=0}^{M-1} \sum_{k=0}^{K-1} \sum_{l=0}^{k} h_{UB} x_{UB}(n-m)\,|x_{UB}(n-m)|^{k-l}|x_{LB}(n-m)|^{l}$$

where $x_{LB}(n)$, $x_{UB}(n)$and $y_{LB}(n)$, $y_{UB}(n)$ are the LPE modulated signals in the input and output of the PA at the LB and UB respectively, and h_{LB} and h_{UB} are the LB and UB model kernels. Additionally, K is the non-linear model order, M is the model's memory depth and $|...|$ is the absolute value of the complex signal. To extract the model kernels a LS technique can be used, following similar reasoning as presented for the previous MPM model.

CO-MPM

Considering a scenario such as presented in Figure 12, it is possible to model the output of the transmitter 1 ($y_1(n)$) by considering the linear combination of two MPM models with two different inputs $x_1(n)$ and $x_2(n)$ [49]:

$$y_1(n) = \sum_{m=0}^{M} \sum_{k=0}^{\frac{K+1}{2}} h_{11} x_1(n-m)|x_1(n-m)|^{2k} + \sum_{m=0}^{M} \sum_{k=0}^{\frac{K+1}{2}} h_{12} x_2(n-m)|x_2(n-m)|^{2k}$$

Where $x_1(n)$ is the signal to be transmitted in the path 1, $x_2(n)$ is the signal of the path 2, h_{11} is the set of model coefficients of the PA for all the components correlated with $x_1(n)$ and h_{12} is the model of the transmitter considering all the signal components correlated with $x_2(n)$. Therefore, this model is able to identify:

- All the non-linear and linear components of the path 1 just due to the signal $x_1(n)$;
- All the linear cross-talk components of the path 2 into path 1;
- The non-linear fundamental crosstalk components due to leakage of $x_2(n)$ into the path 1.

For the sake of clarity, it is important to show how the model can be extracted. Considering the matrix notation for the previous equation (to simplify the following matrix notation no memory taps were included):

$$\widetilde{y_1} = XH_1$$

$$X = \begin{bmatrix} X_{0,1} & X_{1,1} & \dots & X_{K,1} & X_{0,2} & X_{1,2} & \dots & X_{K,2} \end{bmatrix}$$

$$X_{K,i} = [x_i(0)|x_i(0)|^{2K} \quad x_i(0)|x_i(0)|^{2K} \quad \dots \quad x_i(N)|x_i(N)|^{2K}]^T$$

$$H_1 = [\, H_{11}\, H_{12}]^T$$

, where $\widetilde{y_1}$ is the measured data at the output of the transmitter 1, X is the regression matrix containing all the basis function of $x_1(n)$ and $x_2(n)$, H_1 is the matrix containing the coefficient models h_{11} and h_{12} which can be solved in a LS sense [40]:

$$H_1 = (X^H X)^{-1} X^H \widetilde{y_1}$$

For the case of DPD, the inverse model should be obtained in the following way:

$$x_1 = YHi_1$$

$$Y = \begin{bmatrix} Y_{0,1} & Y_{1,1} & \dots & Y_{K,1} & Y_{K,2} & Y_{K,2} & \dots & Y_{K,2} \end{bmatrix}$$

$$Y_{K,i} = [\widetilde{y_i}(0)|\widetilde{y_i}(0)|^{2K} \quad \widetilde{y_i}(0)|\widetilde{y_i}(0)|^{2K} \quad \dots \quad \widetilde{y_i}(N)|\widetilde{y_i}(N)|^{2K}]^T$$

$$Hi_1 = [\, Hi_{11}\, Hi_{12}]^T$$

, where $\widetilde{y_i}(n)$ is the measured data at the output of the transmitter *i*, Y is the regression matrix containing all the basis function of $\widetilde{y_1}(n)$ and $\widetilde{y_2}(n)$, H_{1i} is the matrix containing the coefficient models h_{i11} and h_{i12} of the PA inverse model which can also be solved in a LS sense:

$$Hi_1 = (Y^H Y)^{-1} Y^H \widetilde{y_1}$$

Then, after building X as in (8) and (9) the pre-distorted replica can be defined as:

$$x_{PD} = XHi_1$$

The number of coefficients of the CO-MPM model is:

$$N_{Coefs} = 2(M+1)\left(\frac{K+1}{2}\right)$$

Appendix – A - Additional DPD models

Appendix – B – MGTs applied for radio receivers

Considering that MGTs are a key element for FPGA-based SDR transceivers, in this Appendix the MGTs are addressed, explaining their working principle, usual applications and the challenges associated to their use in SDR applications.

A MGT (Multi-Gigabit Transceiver) is a high speed single bit Serializer/Deserializer (SerDes), capable to deal with bitrates above 1Gbps. As the name indicates the MGT main function is to transform parallel data in a serial bit stream (transmit mode), and convert the received serial stream to a parallel word (receive mode). However, the MGT capabilities go far beyond a simple SerDes, as it will be shown shortly. The line rate is considered as one of the most important features of an MGT, and nowadays the state-of-the-art is already quite above 1Gbps, namely around 32.75 Gbps [69]. It is important to realize that in the beginning of this Ph.D. the state-of-the-art value regarding line rate was 28 Gbps, and that the values that were used for the FPGA designs developed under the scope of this Ph.D. were 10 Gbps, 12 Gbps and 16 Gbps. The maximum line rates strongly depend on technological processes evolution. The MGT is one of the internal elements of an FPGA, and usually the ones with higher speed are only included in the high-end FPGAs. Considering that in this work Xilinx FPGAs were used, Xilinx MGTs will be considered in the further explanations and examples. However, the author would like to add that other FPGA manufactures present products with similar characteristics.

MGTs are typically used to implement high speed serial communication links such as SATA, PCIe, FPGA-FPGA communication, 10G Ethernet, optical communications (CPRI and GPON) and high speed ADC and DAC interface (JESD204). Recently MGTs were used to design SDR transceivers as presented in [13], [29], [30] and in this thesis, which is an application that is quite far from what MGTs have been originally conceived.

Figure 44 presents the location of the GTX (designation of the Xilinx MGT series associated with the Kintex 7 FPGAs) transceivers inside Kintex-7 XC7K325T FPGA. In fact this was the FPGA used for most of the projects developed in the chapter 4 (4.1, 4.2 and 4.3.1), which corresponds to the papers [C2-C5], [J2]. Observing the Figure 44 it is possible to verify that the MGTs are divided in groups of 4, called *QUADS*, and that a single MGT is represented by the primitive GTXE2_CHANNEL [70].

The detail of a *QUAD* in terms of block diagram is presented in Figure 45. Here it is possible to see that each *QUAD* presents one QPLL (Quad PLL), which is an LC-tank PLL, and additionally, each GTX has a dedicated CPLL (Channel PLL), which is a ring-based PLL that can generate the serial clock only for that specific GTX. Each MGT may select the clock from the common QPLL or from its dedicated CPLL. The main difference between these is related with the clock frequencies that they are able to generate, being the highest frequencies covered by the QPLL. Furthermore, the QPLL has specific frequency ranges of operations, while the CPLL presents higher flexibility but a lower maximum frequency [69]–[71]. As illustrated in Figure 45, the *QUAD* either using CPLL or QPLL requires a reference clock, which is the base clock to generate the high speed serial data

clock. Therefore, the reference clock should present good jitter characteristics, otherwise this may affect the data quality, either in transmit mode and receiver mode [71]. According to the authors experience during several laboratorial assessments, the clock jitter plays a key role when MGTs are used for SDR transceivers. In fact the quality of the clock directly affects the EVM of the signal as also the constellation, where it is easy to distinguish the presence of jitter.

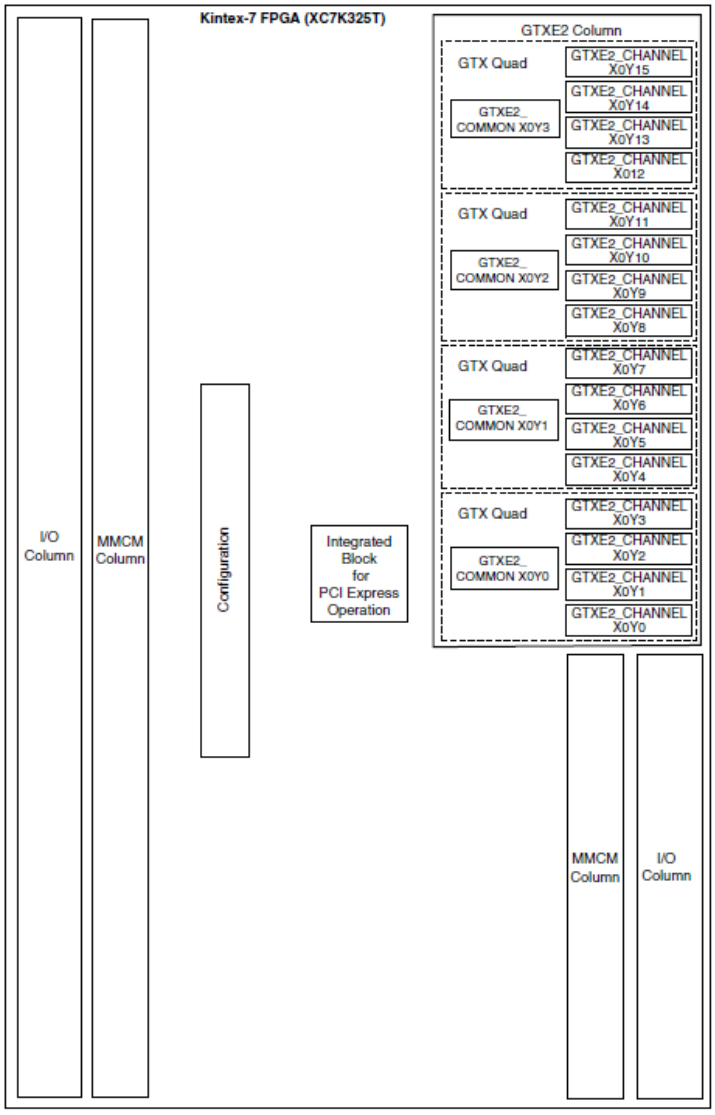


Figure 44 - Location of the GTX transceivers inside Kintex-7 XC7K325T FPGA (figure taken from [70]**).**

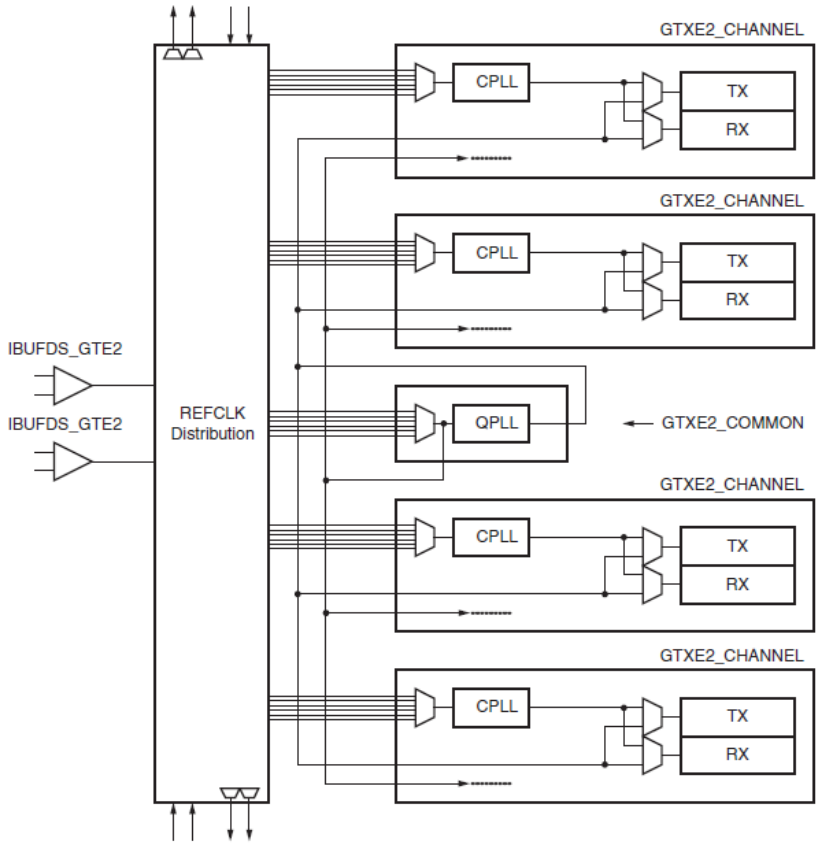


Figure 45 – Block diagram of a GTX transceiver *QUAD* (figure taken from [70]**).**

In Figure 46 the block diagram of the internal structure of the GTX is presented, in which it is possible to realize about all the complexity associated with this element and that is not just a simple SerDes. The top part of the Figure 46 corresponds to the transmit section while the bottom part corresponds to the receive section. Considering the focus of this Ph.D., the transmit section will not be discussed here, and more details can be found in [69]–[71]. Therefore, focusing on the bottom part of the Figure 46, it is shown the comparator, and associated to this it is possible to have some equalization capabilities (Rx EQ and DFE blocks in the Figure 46). These are adaptive linear equalizers mode called the low-power mode (LPM) and a high-performance, adaptive decision feedback equalization (DFE) mode to compensate for high frequency losses in the channel while providing maximum flexibility [70]. All the developed projects were performed without using this equalization capabilities. The next block is called SIPO, where the sampling rate reduction occurs. The blocks until this point compose the receiver PMA (Physical Medium Attachment Sublayer). The subsequent block is called receiver PCS Physical Coding Sublayer (PCS) and contains logic-to-process parallel data and includes FIFO, coding/decoding (8b/10b), scrambling and clock data recovery [70]. These capabilities are usually used in context of the standard MGT usage, therefore it is easy to realize that all these feature were bypassed for the FPGA designs associated to this work.

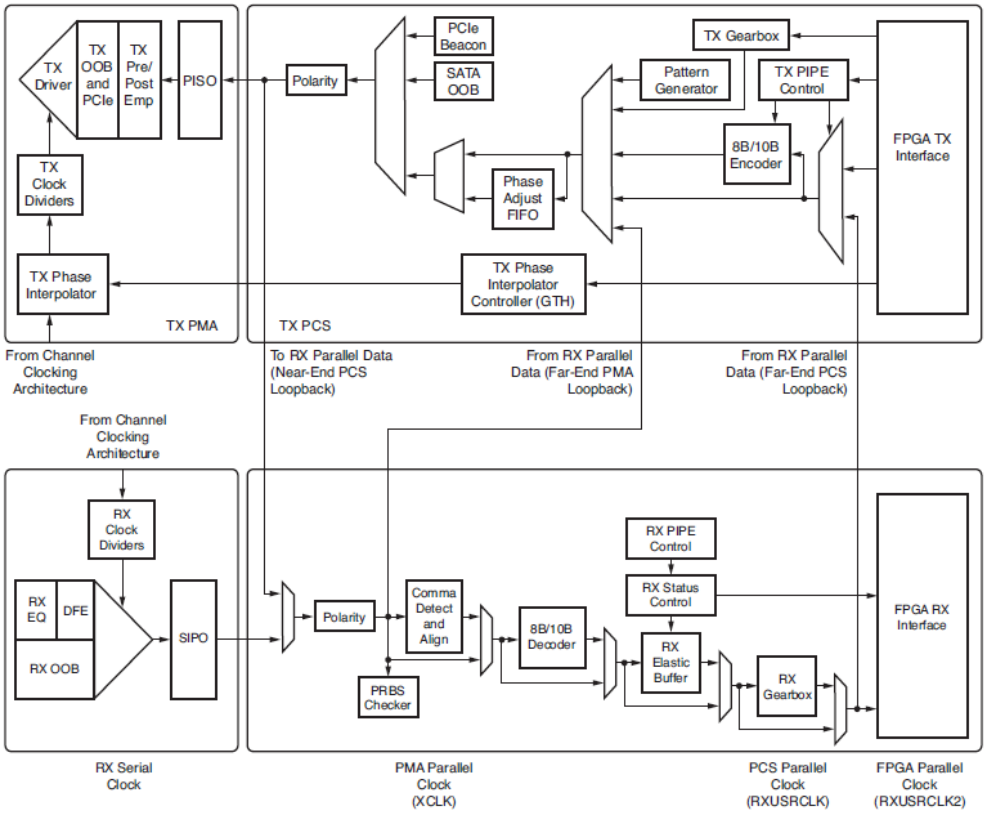


Figure 46 – Block diagram of the GTXE2_CHANNEL primitive, i.e., a single GTX transceiver (figure taken from [70]**).**

Finally, it is important to state that all the different capabilities briefly presented can be configure using a Xilinx IP Core specific for the MGT transceiver (7 Series FPGAs Transceivers Wizard) [70].

Appendix – C - Published papers

Paper C1: Improving DPD Performance by Compensating Feedback Loop Impairments in RF ADCs

[C1] - A. Prata, D. C. Ribeiro, P. M. Cruz, A. S. R. Oliveira, and N. B. Carvalho, “Improving DPD performance by compensating feedback loop impairments in RF ADCs,” in *2015 IEEE MTT-S International Microwave Symposium, IMS 2015*, 2015

Improving DPD Performance by Compensating Feedback Loop Impairments in RF ADCs

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Abstract — In this paper the feedback loop's impairments using radio-frequency (RF) analog-to-digital converters (ADCs) will be studied as a way to improve the digital predistortion (DPD) performance. Specifically, a compensation model for an RF ADC operating in under-sampling regime will be extracted, and applied in a DPD scenario. Significant improvements in the DPD performance will be presented and evaluated in terms of Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM).

Index Terms — RF ADCs, mixed-signal, DPD.

I. Introduction

Mobile communications are in a constant demand for bandwidth. For instance the current LTE-Advance (LTE-A) standard requires a maximum bandwidth of 100 MHz with spectrum aggregation capability that implies additional flexibility [1]. These requirements pose important efforts to build wide and efficient radio-frequency (RF) front ends. In order to achieve flexibility and wider bandwidth there are two fundamental system elements: analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Moreover, to reach adequate power efficiency and meet specific standard spectral masks, digital predistortion (DPD) techniques have a huge importance for telecommunication industry, where RF ADCs are commonly used in the feedback loop.

Current commercial RF ADCs have reached the order of a few GHz both in sampling frequency and also in input bandwidth. Although ADCs are inherently non-linear components, due to their limited number of bits (quantization error) and to the aliasing phenomena, their normal behavior (without clipping the ADC and when restricted to a single Nyquist zone (NZ)) is mainly linear. However, this behavior differs from different NZs and degrades as the input frequency increases. Therefore, since ADCs are a key component in modern digital communication transmitters, where they play a fundamental role in the feedback loop of DPD architectures, this signal degradation is an important case study. In fact, in a DPD scenario, such as presented in Fig. 1, the signal to be linearized is y(t) but the DPD considers z(n) as a perfect representation of y(t), in order to calculate its parameters. For narrow band signals this assumption is valid. However, for wideband signals the feedback loop limitations will impose some drawbacks.

Several research works have already been done to characterize RF ADC's behavior, such as presented in [2]. Additionally, in [3] ADC's quantization noise, random jitter, and the integral nonlinearity (INL) imperfections were evaluated considering a DPD scenario, revealing results without significant impact in the overall system performance.

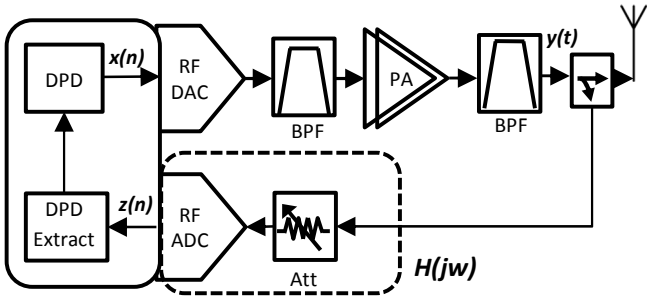

Fig. 1. General block diagram of a wireless transmitter with a feedback loop for DPD.

Nevertheless, there is still a lack in order to understand the consequences of ADC's operation in higher NZs regarding the signal integrity as also its possible correction in digital domain. In this way, by characterizing the entire feedback loop with a function H(jw), it would be possible to apply a compensation ($H(jw)^{-1}$) to approximate z(n) to y(t), which should improve the DPD performance. The analog components of the feedback loop can be characterized using a vector network analyzer (VNA). However, that is not possible for the ADC, which must be characterized using methods such as presented in [2].

In this work, a compensation model for a commercial RF under-sampling ADC will be extracted using a vector signal analyzer (VSA) as a "golden reference". This compensation model will mitigate the ADC impairments when compared to the VSA. In order to validate the advantages of such process, results of Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) in a DPD scenario will be presented. The remainder of this paper is divided as follows. In Section II the compensation model extraction procedure will be explained. In Section III results of the ADC compensation will be presented and discussed focusing on a

DPD scenario. Finally, some conclusions are drawn in Section IV.

II. Feedback Loop Compensation Model Extraction

The feedback loop compensation model extraction focuses in the premise that the signals z(n) and a discretized version of y(t) are not exactly equal, as they should ideally be (apart from a difference in amplitude because of the attenuator). In order to support the previous statement, as also the entire model extraction, measurements of the same signal acquired by a RF ADC (z(n)) and a VSA (y(t) - considered to be an ideal reference) will be compared.

The ADC used in this work is the Texas Instruments ADS5400 with 12 bits, 1GHz of maximum sampling frequency and 2.1 GHz of input bandwidth [4]. The VSA is a R&S FSW8, with maximum bandwidth of 320 MHz. To generate the signal, it was used an Arbitrary Waveform Generator (AWG) AWG70002A from Tektronix. The chosen ADC's operating frequency for all measurements was 1 GHz, and the RF interest signal was centered at 1.79 GHz (located in the 4th NZ of the ADC). All the measurements were acquired and processed by a Matlab routine.

The signal chosen to accomplish the characterization is a multi-sine, since it gives the possibility to excite a wide range of frequencies with only one measurement and gather information from both amplitude and phase. In this way, a measurement with a multi-sine signal with 150 MHz of bandwidth, 5 MHz of fixed spacing between tones, random phases and centered at 1.79 GHz was performed. An embedded trigger was added to this signal in order to synchronize the signals after being captured from the ADC and the VSA, as described in [5]. The results of this measurement are presented in Fig. 2, where it is possible to observe an amplitude difference between the signal acquired by the ADC and the VSA.

The previous measurements contain all the data to extract a linear model within 150 MHz of bandwidth. Considering a frequency domain analysis of the signals presented in Fig. 2, it is possible to compare the magnitude and phase of the signal by just analyzing the interest bins, i.e., the multi-sine tones. Considering the VSA bins as Y(jw) and the ADC bins as Z(jw), the correction model is given by the following expression:

$$H(jw)^{-1} = \frac{|Y(jw)|}{|Z(jw)|} e^{-j \times unwrap(\angle Y(jw) - \angle Z(jw))}. \quad (1)$$

Fig. 3 presents the amplitude and phase of the H(jw)$^{-1}$ model. This model can be directly applied to any ADC sampled signal within 1,715 GHz and 1,865 GHz, which corresponds to the multi-sine lower and higher tones. Additionally and despite of this model is being extracted for 150 MHz in the 4th NZ this procedure could be done for any other ADC frequency band. It is also important to state, that to apply this model in a real modulated signal, an interpolation has to be performed.

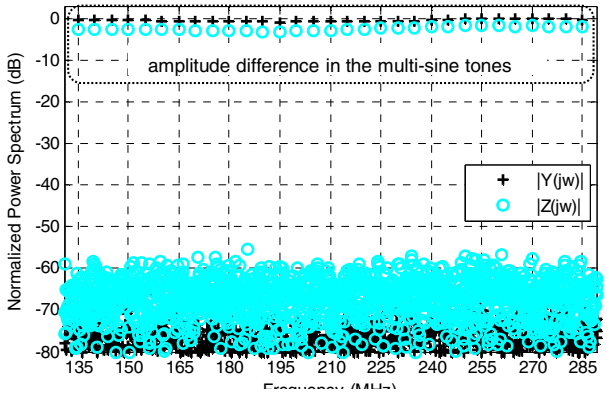

Fig. 2. Frequency domain representation of the multi-sine measurement in both ADC (Z(jw)) and VSA(Y(jw) (folded version in the 1st NZ).

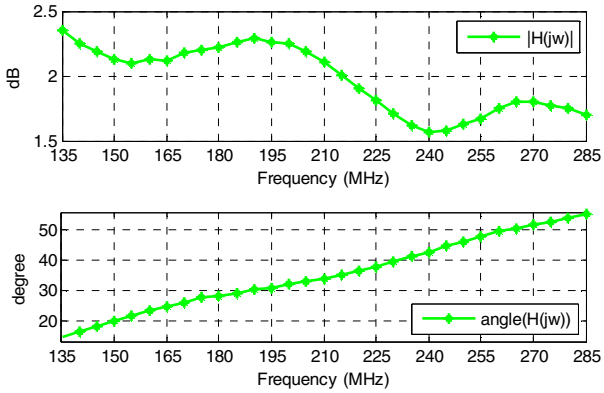

Fig. 3. Frequency domain representation of amplitude and phase of the H(jw) compensation model.

III. RF ADC Post-Compensation In A DPD Scenario

In order to show the relevance of the feedback loop compensation model, extracted in the previous section, this will be applied in a DPD scenario (Fig. 4). In this way, our experiment will compare the DPD performance using signals from three different feedback loops:

- using the VSA (z_1(n));
- using the RF ADC (z_2(n));
- using the same RF ADC with post compensation (z_3(n), i.e., $z_3(n) = z_2(n).H(jw)^{-1}$).

The signal is once more generated in an AWG, which is followed by a bandpass filter to remove the DAC's images. The power amplifier (PA) block is made by two Mini-Circuits amplifiers and a fixed attenuator, performing an overall gain of 22 dB. The laboratorial setup assembled for this experiment is presented in Fig. 5.

In this experiment, the base band signal is a 50 MHz, 16-QAM modulated signal digitally up-converted to 1.79 GHz in Matlab, and then loaded into the AWG. Using this bandwidth, the entire signal and its third order distortion are suitable to the model extracted in the previous section. The DPD is also

implemented in Matlab, using the well-known Memory Polynomial (MP) model [6].

Fig. 6a) presents the spectrum of the signals $z_1(n)$, $z_2(n)$ and $z_3(n)$, where it is possible to observe differences between the signal captured from ADC ($Z_2(jw)$) and the post-compensated signal ($Z_3(jw)$), which is closer to the VSA signal ($Z_1(jw)$).

Consequently, the same DPD model (with M=5 and K=5) was applied using the signals $z_1(n)$, $z_2(n)$ and $z_3(n)$. Therefore, using a VSA three different signals were captured at the PA output ($y_1(t)$, $y_2(t)$ and $y_3(t)$) for each different pre-distorter output ($x_1(n)$, $x_2(n)$ and $x_3(n)$). The results are presented in Fig. 6b), where it is possible to observe that the ACPR of the $y_3(n)$ is greater than in $y_2(n)$, showing a great improvement of DPD performance by applying ADC post compensation. In fact, this experiment shows an improvement of about 9 dB in the total ACPR, by applying post-compensation. Concerning the EVM of the signal there is also a significant improvement of about 1.76%. More details of these improvements are presented in the Table I, in terms of EVM and ACPR, considering this experiment as also results from another experiment with a 64-QAM modulated signal.

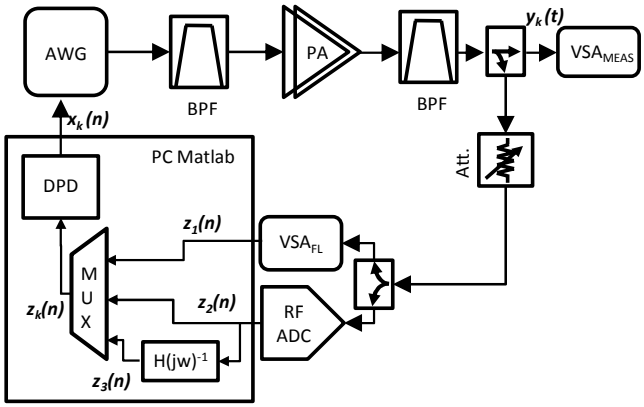

Fig. 4. Block diagram of the laboratory experiment assembled to implement the DPD scenario (k=1,2,3 , depending on the feedback loop).

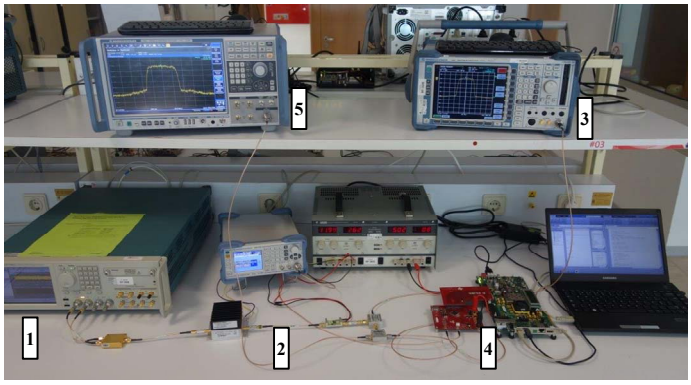

Fig. 5. Photograph of the laboratorial setup (1- AWG; 2- PA; 3- SA_{MEAS}; 4-ADC; 5-VSA_{FL}).

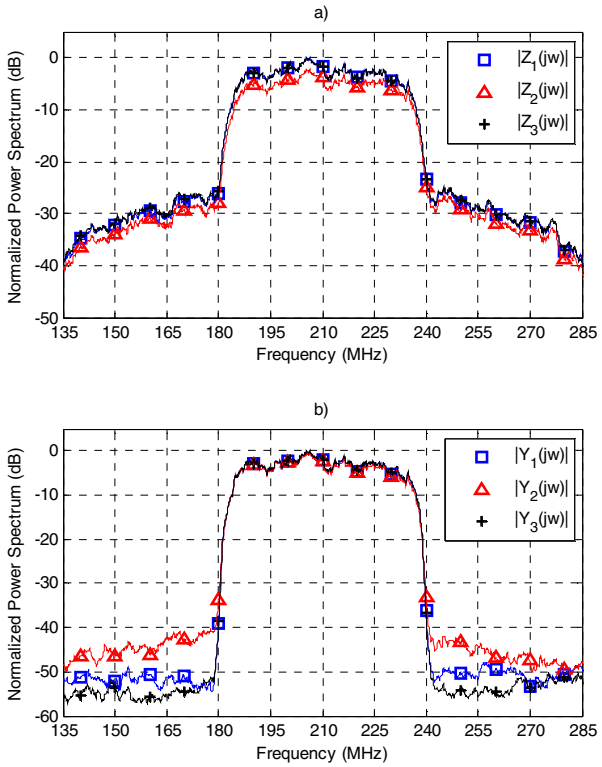

Fig. 6. a) Spectrum of the signals from the three feedback loops. b) Spectrum of the PA output after applying DPD with each feedback loop.

TABLE 1
MEASUREMENTS RESULTS OF EVM AND ACPR USING THE THREE DIFFERENT FEEDBACK LOOPS.

			PA Output		
Signal Modulation	Measurements		y_1	y_2	y_3
16-QAM 50 MHz	EVM rms (%)		0,67	2,16	0,4
	ACPR (dB)	Lower	47,7	47,7	50,9
		Upper	47,1	42,1	49,2
		Total	44,37	38,17	46,96
64-QAM 50 MHz	EVM rms (%)		0,42	1,93	0,38
	ACPR (dB)	Lower	47,1	47,1	48,6
		Upper	46,0	42,9	46,9
		Total	43,49	40,37	44,66

IV. CONCLUSION

In this paper, a linear compensation model to apply in RF ADCs, commonly used in DPD feedback loops has been extracted. The application of this post-compensation model in the feedback loop enables an improvement of DPD performance. This improvement was quantified in terms of EVM and ACPR, showing significantly gains. Moreover, this compensation system can also be applied in other use case

scenarios in order to improve the signal integrity of any acquired signal.

ACKNOWLEDGEMENT

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013; UID/EEA/50008/2013, the project EXCL/EEI-TEL/0067/2012 (CREaTION), and to the PhD (SFRH/BD/92746/2013, SFRH/BD/85163/2012) and Post-doc (SFRH/BPD/92452/2013) grants given to the first, second and third authors, respectively.

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Paper J1: RF Subsampling Feedback Loop Technique for Concurrent Dual-Band PA Linearization

[J1] - A. Prata, D. C. Ribeiro, P. M. Cruz, A. S. R. Oliveira, and N. B. Carvalho, “RF Subsampling Feedback Loop Technique for Concurrent Dual-Band PA Linearization,” in *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4174–4182, Dec. 2016.

RF Subsampling Feedback Loop Technique for Concurrent Dual-Band PA Linearization

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***Abstract*— This paper investigates feedback loops using radio-frequency (RF) subsampling analog-to-digital converters (ADCs) as a way to improve the concurrent dual-band transmitters linearization. The feedback loop will be characterized and post-compensated in the digital domain, followed by a new technique for a concurrent dual-band digital predistortion (DPD) scenario where aliasing between both carriers is allowed to occur. The proposed technique is based on statistical approximated non-overlapped multi-sines that permit relaxing the feedback loop requirements. Measurement results in a 2D-DPD (two dimensional-digital predistortion) scenario are presented and compared with other state-of-the art techniques. Metrics such as Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM) are evaluated in order to corroborate the correct functioning of the proposed technique.**

***Index Terms*— Mixed-signal, subsampling analog-to-digital converters (ADCs), concurrent dual-band, digital predistortion (DPD).**

I. Introduction

Nowadays, mobile communications are in an endless demand for bandwidth. For instance the current LTE-Advance (LTE-A) standard requires a maximum bandwidth of 100 MHz considering a spectrum aggregation scenario [1]. These requirements pose important efforts to build agile, wideband and efficient radio-frequency (RF) front ends. Regarding flexibility and wider bandwidth there are two fundamental system elements: analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Moreover, to reach adequate amplification power efficiency and meet specific standard spectral masks, digital predistortion (DPD) techniques have a huge importance for telecommunication industry. Within this context, the use of feedback loops or observation paths is mandatory to acquire the PA (Power Amplifier) output signal and then calculate the DPD coefficients to linearize the whole transmission chain. To build these feedback loops, mixer-based architectures followed by low sampling rate ADCs are commonly used. Additionally, when it is required to address a multi-band scenario, multiple receivers tuned at each transmission frequency are usually required (Fig. 1a)). On the other hand, RF subsampling ADCs pose as an alternative to the traditional architectures, by allowing higher bandwidths and concurrent multi-band scenarios using a single receiver (Fig. 1b)).

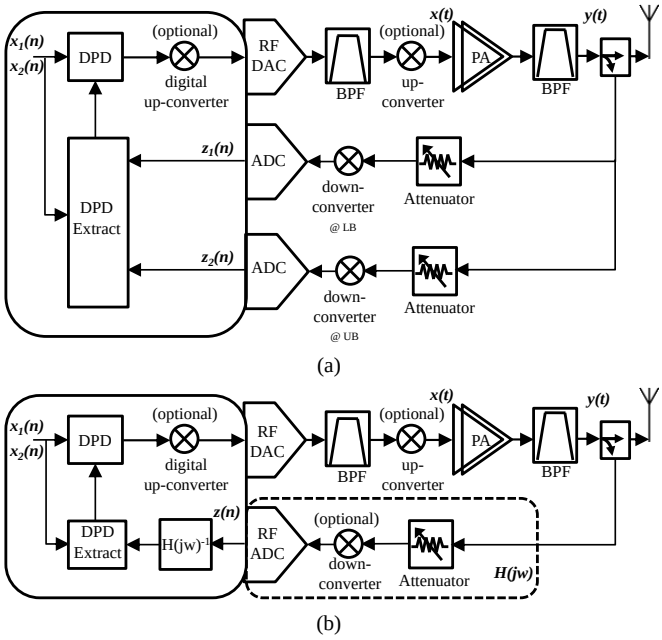

Fig. 1. General block diagrams of a wireless transmitter with a feedback loop for DPD: (a) conventional dual-band DPD feedback loop architecture and (b) architecture of a DPD feedback loop using an RF sampling ADC.

Current commercial RF subsampling ADCs have reached the order of a few GHz both in sampling frequency and in input bandwidth. Although ADCs are inherently non-linear components, due to their limited number of bits (quantization error) and to the aliasing phenomena, their normal behavior (without clipping the ADC and when restricted to a single Nyquist zone (NZ)) is mainly linear. However, this behavior differs from different NZs and degrades as the input frequency increases. Therefore, since ADCs are a key component in modern digital communication transmitters, where they play a fundamental role in the feedback loop of DPD architectures, this signal degradation is an important case study. In fact, this

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was the case study in [2] that we will explore further in this paper.

As previously stated, current wireless communications standards strongly depend on multiple carrier aggregation, in order to increase the communication throughput. In this way, to gather the maximum power efficiency, this has led to the use of a single amplifier for multiple band amplification, instead of using multiple amplifiers tuned at each specific frequency [3], [4]. However in a multiple band scenario the implementation of DPD algorithms and feedback loops is not as straightforward as in a single band case.

Considering a dual-band scenario, first of all the non-linear contributions are now not only from the intermodulation distortion (IMD) products but also from the cross-modulation (CM) mixtures between the two bands that must be considered in the DPD design, so a 2D (two dimensional) model for the PA is mandatory [5]. Several research works have been done in order to look for effective 2D modeling structures, such as [5], [6]. Second, the feedback loop has now to acquire two bands concurrently at the output of the PA, which is at least twice of the required bandwidth in the single band case. A conventional architecture is usually made of two parallel feedback loops acquiring separately the lower band (LB) and upper band (UB) (Fig. 1a)). This matter is also being recently addressed by the scientific community by trying to reduce the needs of two feedback loops. In [7], [8], a single feedback loop strategy is presented by acquiring the multiple bands in different time slots. Another recent contribution in [9] develops a new approach called down-converted carrier co-location (DC^3). However, it requires two external mixers in the feedback path to place both bands at a specific location. Another possibility for the feedback loop is to use RF subsampling ADCs, such as presented in [10], where by changing the sampling frequency of the ADC allows to avoid the aliasing of the different bands, and thus, all the signal components can be recovered.

In this work the proposed architecture is based on RF subsampling ADCs, where the sampling frequency is maintained fixed leading to a simpler digital architecture than [10]. This process can obviously cause aliasing between LB and UB that will be solved by a previous characterization procedure based on statistical approximated non-overlapped multi-sines, as it will be explained later on.

The remainder of this paper is divided as follows. In Section II a compensation model extraction and its application in a single band DPD scenario will be briefly revisited. Section III discusses the aliasing problem when using an RF subsampling ADC in dual-band DPD feedback loops and also the proposed process to overcome this problem based on statistical approximated non-overlapped multi-sines. Then, in order to validate the proposed technique measurement results of Adjacent Channel Power Ratio (ACPR), Error Vector Magnitude (EVM) and NMSE (Normalized Mean Squared Error) will be presented and discussed in Section IV. Finally, some conclusions regarding the proposed technique are drawn in Section V.

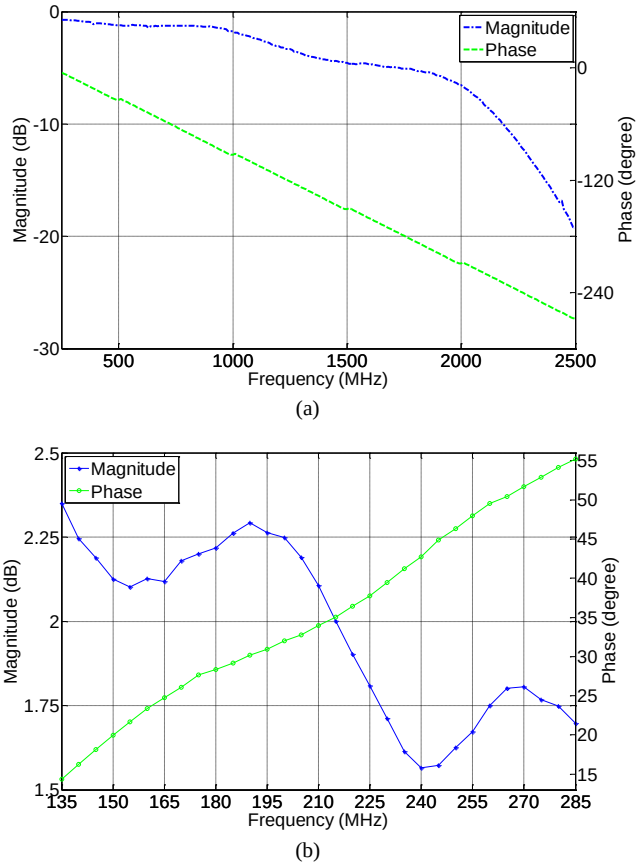

Fig. 2. (a) Measured frequency response of the entire feedback loop, from [12]. (b) Frequency response of the compensation model ($H(jw)^{-1}$), from [2].

II. Revisiting Single Band Feedback Loop Compensation

A feedback loop compensation model extraction focuses in the premise that the signals *z(n)* and a discretized version of *y(t)* are not exactly equal, as they should ideally be (apart from a difference in amplitude due to the coupler) (Fig. 1b)). In order to support the previous statement, the feedback loop, which is made by a single RF subsampling ADC was characterized ($H(jw)$) and its inverse model ($H(jw)^{-1}$) was used to compensate for the impairments [2].

Briefly revisiting the results obtained in [2], which used a Texas Instruments ADC (ADS5400) with 12 bits, 1 GHz of maximum sampling frequency and 2.1 GHz of input bandwidth. The ADC characterization was done following the procedures presented and validated in [2], [11], [12]. Fig. 2a) presents the measured feedback loop frequency response, in both amplitude and phase, from 250 MHz up to 2.5 GHz. Fig. 2b) presents the compensation model response in a bandwidth of 150 MHz centered at 1.79 GHz (located in the 4th NZ), which corresponds to a center frequency of 210 MHz in the folded version at the first NZ.

Using the compensation model presented in Fig. 2b) the mixed-signal feedback loop was de-embedded from the

received signal and applied to a single band DPD scenario considering 16-QAM and 64-QAM 50 MHz wide signals.

TABLE I
MEASUREMENT RESULTS OF ACPR AND EVM WITH AND WITHOUT LINEAR FEEDBACK LOOP COMPENSATION [2].

			PA Output	
Signal Modulation	Measurements		without compensation	with compensation
16-QAM	EVM rms (%)		2.16	0.4
	ACPR (dBc)	Lower	47.7	50.9
		Higher	42.1	49.2
		Total	38.17	46.96
64-QAM	EVM rms (%)		1.93	0.38
	ACPR (dBc)	Lower	47.1	48.6
		Higher	42.9	46.9
		Total	40.37	44.66

Lower, higher and total ACPR [13] results of the scenario with and without post-compensation are presented in Table I [2]. It can be verified an improvement of about 9 dB in the total ACPR and 1.76% in the EVM, by applying compensation in the 16-QAM signal and 4.3 dB and 1.55 % in the 64-QAM signal case. These results show that a mixed-signal characterization for identifying the impairment of the feedback loop, including the ADC is fundamental for an improvement of the DPD technique.

III. FEEDBACK LOOP CHARACTERIZATION IN A DUAL-BAND SCENARIO

After revisiting the feedback loop compensation procedure and its advantages when applied in a single-band DPD scenario, it is now time to focus on the dual-band scenario, since it is a more important case for current wireless communications applications.

In this paper the proposed feedback loop for a dual-band DPD scenario lies on a simple RF subsampling ADC (the same of the previous section) with fixed sampling frequency as presented in Fig. 1b). Moreover, the feedback loop compensation process explained in the previous section is considered mandatory in order to obtain more accurate results and as previously stated it can be extracted and implemented in any type of feedback loop architecture, and despite not directly refereed it will always be considered in the remainder of this paper.

A. *The folding problem in RF sampling approach*

Considering a dual-band scenario presenting a LB and UB that are respectively represented by $x_1(t)$, signal centered at f_{c1}, and $x_2(t)$ centered at f_{c2}. This will originate the signal $x(t)$ given by the summation of $x_1(t)$ and $x_2(t)$, Fig. 3a). If this signal passes through the PA, it will cause non-linear

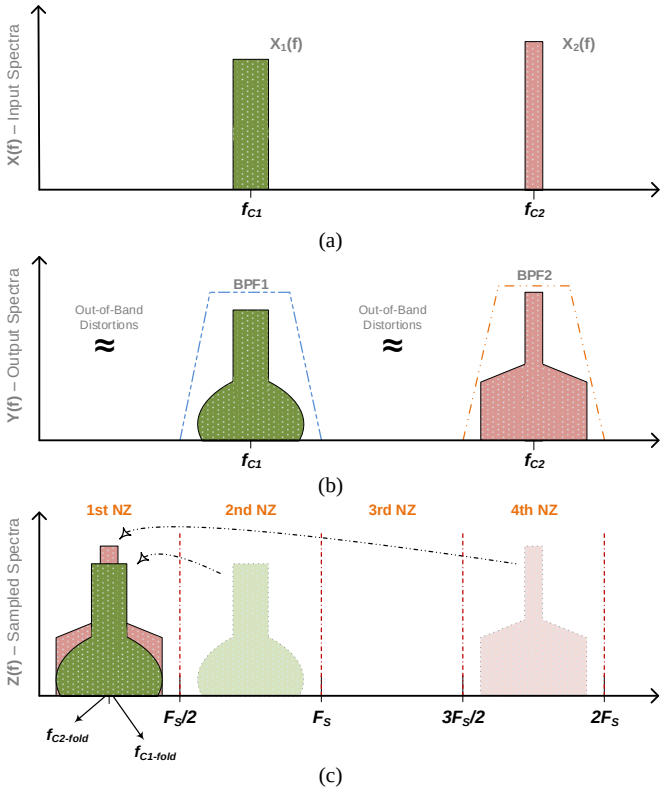

Fig. 3. (a) Spectrum of the signal $x(t)$ at the input of the PA. (b) Spectrum of the signal $y(t)$ at the output of the PA. (c) Spectrum of the signal $z(n)$ acquired by the feedback loop.

distortion (IMD and CM), which will appear in-band and out-of-band (OOB). The OOB distortion can be removed by an analog band-pass filter (BPF), but the in-band cannot be eliminated by the same approach, Fig. 3b).

Therefore, in an RF subsampling feedback loop case with a given sampling frequency (F_s) such that $F_s < min(2f_{c1}, 2f_{c2})$, it is immediate to recognize that overlapping of both the LB and UB may occur in the first NZ. To verify the overlapping occurrence, the first NZ folding frequencies must be computed using (1):

$$f_{fold} = |f_c - \left\lfloor \frac{f_c}{F_s} \right\rceil F_s \,|, \tag{1}$$

where f_{fold} is the folding frequency in the first NZ, f_c is the carrier frequency, F_s is the sampling frequency, $\lfloor ... \rceil$ is the rounding operation towards nearest integer and $|...|$ is the absolute value.

After computing (1) the folding frequencies of the LB and UB will be obtained as $f_{c1\text{-}fold}$ and $f_{c2\text{-}fold}$, respectively. If there is no overlapping between the LB and UB, the problem is reduced to the one presented in Section II. On the other hand, when overlapping occurs the recovery of $z_1(n)$ and $z_2(n)$, which are the sampled versions of $y_1(t)$ and $y_2(t)$, is totally compromised because both signals will fall on top of each other, as shown in Fig. 3c).

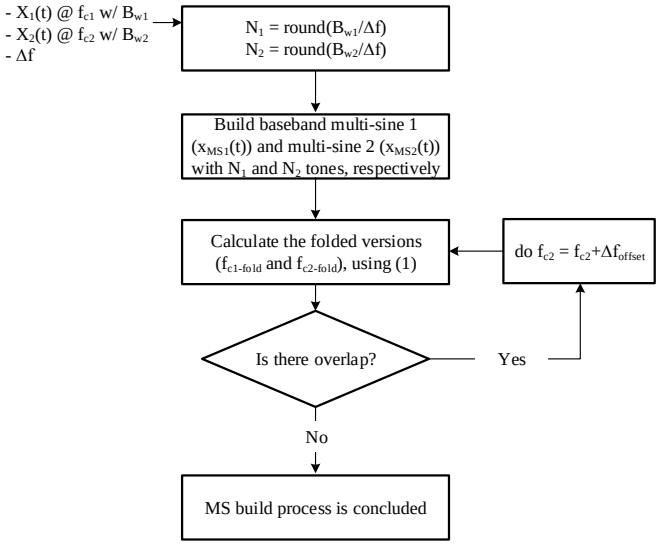

Fig. 4. Procedure flowchart for the construction of the non-overlapping multi-sines.

To avoid this problem the obvious solutions would be to use two independent feedback loops or modify the ADC sampling rate in a way that the acquired signals would not be overlapped [10]. However, these solutions represent an increase in the overall system cost and complexity. Another solution is to acquire LB and UB in different time slots to extract the signals for the DPD [7], [8], but this technique loses the real time functionality of the feedback loop. More recently, an alternative solution based in the carrier co-location technique (DC^3) has been proposed in [9], which allows the extraction of the DPD parameters from the overlapped signals. In any case, such an approach will increase the processing capacity needed for the extraction procedure and imposes the use of different local oscillators (LOs) between the transmitter and feedback loop chain.

Therefore, to address this issue an innovative solution based on statistically approximated non-overlapped multi-sines using a single RF subsampling feedback loop will be proposed.

B. Use of non-overlapped multi-sines for folded model characterization

In order to overcome the previously mentioned aliasing problem, this work will focus in a characterization strategy that replaces the original $x_1(t)$ and $x_2(t)$ modulated signals by statistically approximated non-overlapped multi-sines. The underlying idea of this approach is to choose a suitable placement of the multi-sine frequency bins, avoiding overlapping of LB and UB signals in the extraction procedure.

For this purpose, each multi-sine should present N_1 and N_2 tones with the same fixed separation between tones (Δf) covering a bandwidth BW_1 and BW_2 equal to the channel bandwidth of $x_1(t)$ and $x_2(t)$ signals. Then, it is necessary to verify the overlapping condition assuming multi-sines to be centered at f_{c1} and f_{c2}, originating folded versions at $f_{c1\text{-}fold}$ and $f_{c2\text{-}fold}$ calculated using (1). If there is any multi-sine tone overlap in this process, it is necessary to shift one of the carriers by a certain offset in frequency given by $\Delta f_{offset} = \Delta f/2$ (leading to the minimum sample acquisition requirement). Fig. 4 presents the described procedure.

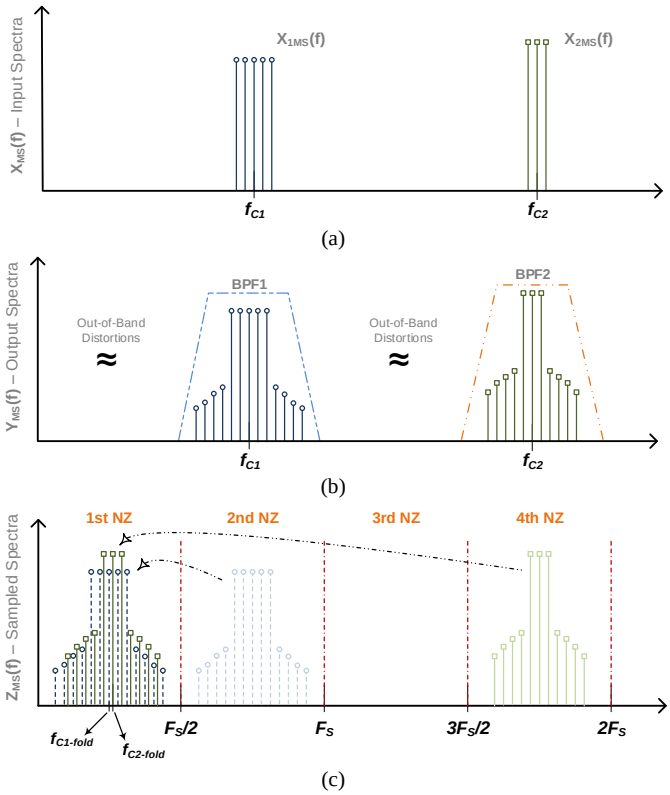

Fig. 5. (a) Spectrum of the signal $x_{MS}(t)$ at the input of the PA. (b) Spectrum of the signal $y_{MS}(t)$ at the output of the PA. (c) Spectrum of the signal $z_{MS}(t)$ acquired by the RF subsampling feedback loop.

In order to conceptually validate the described procedure, the $x_1(t)$ and $x_2(t)$ modulated signals will be replaced by two multi-sine signals $x_{1MS}(t)$ and $x_{2MS}(t)$ built as previously explained together with a specific statistical shaping (see Section II.C). Thus, the signal $x_{MS}(t)$ is the summation of the $x_{1MS}(t)$ with $x_{2MS}(t)$ placed in the desired carrier frequencies, as depicted in Fig. 5a). Consequently, $y_{MS}(t)$ will be the signal at the output of the PA with the non-linear distortion appearing at the same frequencies as in the previous case (Fig. 5b)), and $z_{MS}(n)$ will be the signal acquired by the RF subsampling feedback loop (Fig. 5c)).

Focusing on Fig. 5c), it is possible to verify that the multi-sine tones do not overlap, being possible to recover them in the frequency domain by calculating the folded frequencies of each multi-sine tone using (1). This strategy allows obtaining both $z_{1MS}(t)$ and $z_{2MS}(t)$ after the folding mechanism, and thus, to calculate the respective low-pass equivalent (LPE) signals to model the full system (PA, feedback loop and so on). Moreover, the kernels determination using the statistical-shaped non-overlapping multi-sines will allow to build a 2D-DPD extraction process to be applied in the overlapped modulated signal case.

C. Statistical non-overlapped multi-sine design

In several publications [13]–[15], it was showed that the use of multi-sines is a viable solution for behavioral modelling approach. Nevertheless the correct characterization of the

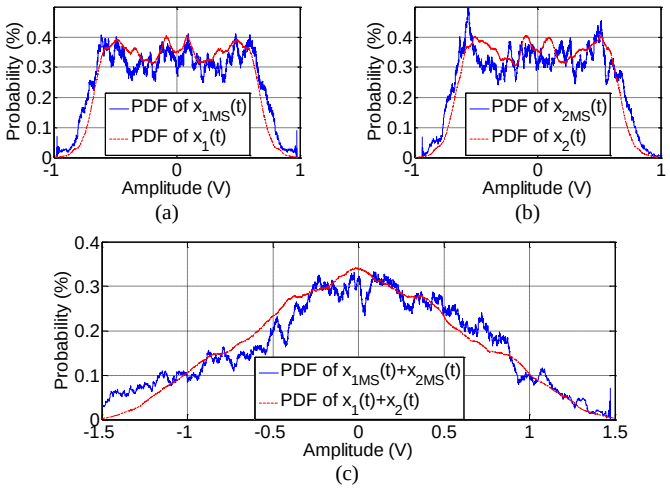

Fig. 6. (a) PDF plot of $x_1(t)$ and $x_{1MS}(t)$ signals. (b) PDF plot of $x_2(t)$ and $x_{2MS}(t)$ signals. (c) PDF plot of $(x_1(t) + x_2(t))$ and $(x_{1MS}(t) + x_{2MS}(t))$ signals.

nonlinear device under test (DUT) under modulated signals is only viable if the multi-sine signals used to extract the model has the same characteristics of the modulated signals, mainly respecting the modulation bandwidth, the carrier frequency and more important from a nonlinear point of view, the amplitude statistical pattern, that will impose similar peak-to-average power ratio (PAPR). It is also proved that, if the DUT behaves memoryless or presents mildly memory effects, the multi-sine approach using the same statistical pattern can be used as the model extraction signal with the corresponding advantages of the periodicity of the multi-sine signals.

In this paper the signals $x_1(t)$ and $x_2(t)$ are real modulated signals, which will impose the model extraction to be performed using multi-sine signals with equivalent statistical shaping.

Considering $x_1(t)$ and $x_2(t)$ as QPSK modulated signals with symbol rates of 5 MHz and 10 MHz respectively and that a baseband filter such as a root raised cosine (RRC) with a factor of 0.25 is used, this implies that the signals will occupy a total channel bandwidth of 6.25 MHz and 12.5 MHz respectively. The latter values are the ones that should be used for the multi-sine design. Considering a tone frequency separation of $\Delta f = 250$ kHz, $x_{MS1}(t)$ will have 25 tones and $x_{MS2}(t)$ will have 51 tones to guarantee similar modulated bandwidths.

Following the algorithm presented in [14], the amplitude and phases of each of the multi-sine signals were calculated in order to achieve a similar statistical pattern between the multi-sine and the modulated signal approach, but keeping the same average power level. The probability density function (PDF) statistical behavior for both modulated and multi-sine signals are presented in Fig. 6.

D. Concurrent dual-band modeling strategy

The proposed modelling strategy starts by performing a model extraction using non-overlapped statistical approximated multi-sines. Thus considering $z_{MS}(n)$ to be the measured signal by the feedback loop using the multi-sines, which after digital filtering of spurs and non-desirable out of band distortion is represented by:

$$z_{MS}(n) = z_{1MS}(n) + z_{2MS}(n) \quad (2).$$

Due to the imposed non-overlapping condition both multi-sines can be recovered by applying a Fast Fourier Transform (FFT). Then, in the frequency domain a selection over the interest bins followed by an Inverse Fourier Transform (IFFT) allows to recover the LPE of $z_{1MS}(n)$ and $z_{2MS}(n)$, which are represented by $z_{1MSBB}(n)$ and $z_{2MSBB}(n)$, respectively [16]. After time alignment of the measured multi-sines and the original versions using a simple cross correlation algorithm, the recovered multi-sine LPE signals will then feed a 2D behavioral modeling structure [5], as follows:

$$z_{1MSBB}(n) = \sum_{m=0}^{M-1}\sum_{k=0}^{K-1}\sum_{l=0}^{k} c_{m,k,l}^{(1)} x_{1MSBB}(n-m) \times |x_{1MSBB}(n-m)|^{k-l} |x_{2MSBB}(n-m)|^{l}, \quad (3)$$

$$z_{2MSBB}(n) = \sum_{m=0}^{M-1}\sum_{k=0}^{K-1}\sum_{l=0}^{k} c_{m,k,l}^{(2)} x_{2MSBB}(n-m) \times |x_{2MSBB}(n-m)|^{k-l} |x_{1MSBB}(n-m)|^{l}, \quad (4)$$

where $c_{m,k,l}^{(1)}$ and $c_{m,k,l}^{(2)}$ are the LB and UB model kernels, $x_{1MSBB}(n)$ and $x_{2MSBB}(n)$ are the multi-sine LPE input PA signals, $z_{1MSBB}(n)$ and $z_{2MSBB}(n)$ are the multi-sine LPE output PA signals. Additionally, K is the non-linear model order, M is the model's memory length and $|...|$ is the absolute value of the complex signal. To extract the model kernels a traditional least square (LS) estimation technique is used. This gives a forward PA model estimation, which allows to estimate the LPE modulated signals at the PA output $\hat{y}_{1BB}(n)$ and $\hat{y}_{2BB}(n)$ in the following way:

$$\hat{y}_{1BB}(n) = \sum_{m=0}^{M-1}\sum_{k=0}^{K-1}\sum_{l=0}^{k} c_{m,k,l}^{(1)} x_{1BB}(n-m) \times |x_{1BB}(n-m)|^{k-l} |x_{2BB}(n-m)|^{l}, \quad (5)$$

$$\hat{y}_{2BB}(n) = \sum_{m=0}^{M-1}\sum_{k=0}^{K-1}\sum_{l=0}^{k} c_{m,k,l}^{(2)} x_{2BB}(n-m) \times |x_{2BB}(n-m)|^{k-l} |x_{1BB}(n-m)|^{l}, \quad (6)$$

where $x_{1BB}(n)$ and $x_{2BB}(n)$ are the LPE modulated signals that are presented to the input of the PA. In this way after the previous step all the information to build a common indirect learning 2D-DPD algorithm [5] is gathered.

The entire proposed procedure can now be briefly summarized as follows:

1. Characterization of the feedback loop, and obtaining its compensation model (Section II).
2. Design of non-overlapped statistical approximated multi-sines (Section III.B and III.C).
3. Apply the modeling strategy introduced in Section III.D.

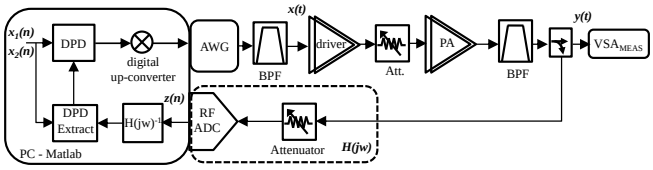

Fig. 7. Block diagram of the measurement setup.

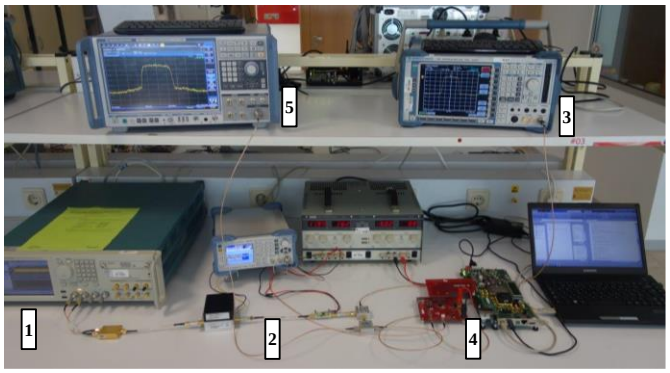

Fig. 8. Photograph of the laboratorial setup (1- AWG; 2- PA; 3- SA_{MEAS}; 4-ADC; 5-VSA_{FL}), from [2].

IV. Measurement Results

In order to experimentally validate the proposed technique the laboratorial setup presented in the block diagram of Fig. 7 was assembled, to mimic the scenario depicted in Fig. 1b). The RF DAC was replaced by a commercial arbitrary waveform generator (AWG), Tektronix AWG70002A, the PA is composed by a Mini-Circuits ZHL-1042J followed by an ERA-4+ and using a variable attenuator between both in order to control the input power level. The used subsampling ADC is the ADS5400 clocked at 1 GHz. At the output of the PA, a vector signal analyzer (VSA), Rohde & Schwarz FSW8, was used in order to measure the PA performance before and after DPD. The laboratorial equipment control and the digital signal processing is performed using *Matlab* software. Fig. 8 presents a photo of the laboratorial setup. In order to perform a comparison with a similar state-of the art method, the same setup was also used to apply the method proposed in [9].

The signals considered for the experimental validation are the referred in Section III.C. The carriers for both LB and UB are respectively 910 MHz and 1090 MHz. Since the ADC sampling frequency was set to be 1 GHz and according to (1), this makes the folded frequencies of the modulated signal to overlap in the 1st NZ at 90 MHz.

A. Proposed modeling technique using non-overlapped multi-sines

Having in mind the proposed technique we will start by performing a measurement using the non-overlapped multi-sines. Therefore we have $x_{MS1}(t)$ with 25 tones, spaced of 250 kHz (Δf) making a total bandwidth of 6.25 MHz and centered at 910 MHz. On the other hand we have the $x_{MS2}(t)$ with 50 tones spaced of 250 kHz leading to a total bandwidth of 12.5MHz and centered at 1090.125 MHz, i.e., using a

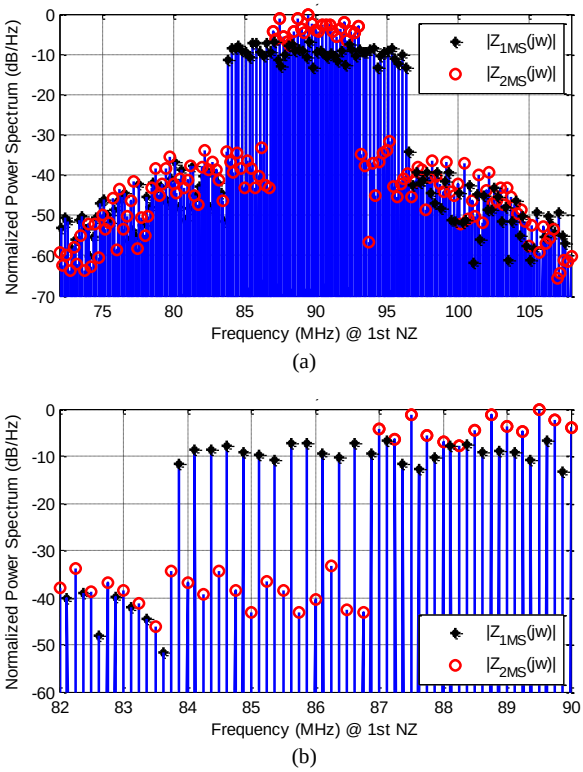

Fig. 9. Frequency domain representation of the measured non-overlapped multi-sines ($z_{MS}(t)$) (a) Spectrum over entire bandwidth of the $z_{MS}(t)$ signal. (b) Zoom-in version of the spectrum focusing both fundamental and IMD distortion components.

$\Delta f_{offset} = \Delta f/2 = 125$ kHz in order to guarantee the non-overlapping condition at the first NZ. Then, due to the non-overlapping condition of the multi-sine signals the LB multi-sine folding frequency is 90 MHz (the same as the modulated signal) and the UB multi-sine folding frequency is 90.125 MHz.

The frequency domain representation of the measured $z_{MS}(t)$ is presented in Fig. 9a). In Fig. 9b) it is clear to observe that the tones from $z_{MS1}(t)$ and $z_{MS2}(t)$ fall in different frequency bins (validation of non-overlapping condition).

Then, the isolated multi-sine frequency bins were separated in the frequency domain, originating $z_{1MSBB}(n)$ and $z_{2MSBB}(n)$ allowing to apply the formulation in (3) and (4). During the extraction process, several K and M pairs were tested and a reasonable compromise was verified for K=7 and M=3. When comparing the acquired distorted multi-sines ($z_{MS1}(t)$ and $z_{MS2}(t)$) with the original ones ($x_{MS1}(t)$ and $x_{MS2}(t)$) it leads to NMSE values of -27.26 dB (LB) and -24.61 dB (UB). The procedure to apply it on modulated signals will be explained in the next section.

B. Validation of proposed modeling technique using real modulated signal

After the multi-sine modeling extraction the focus is now on the application into modulated signal. Thus, by applying the proposed modelling strategy it is possible to estimate the LPE PA output signals $\hat{y}_{1BB}(n)$ and $\hat{y}_{2BB}(n)$, using (5) and (6), which should be properly validated with measurements.

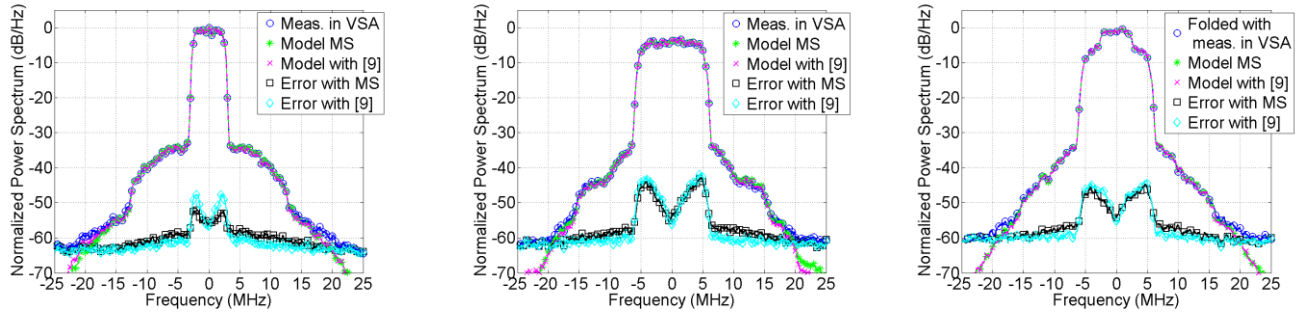

Fig. 10. Spectrum of the PA output measured by the VSA, model using proposed modelling approach and modelling approach of [9], and respective modeling error: (a) LB (b) UB.(c) Folded version (The folded version of the VSA was digitally forced obtaining the LB and UB separately. [MS – non-overlapped statistical approximated multi-sine method].

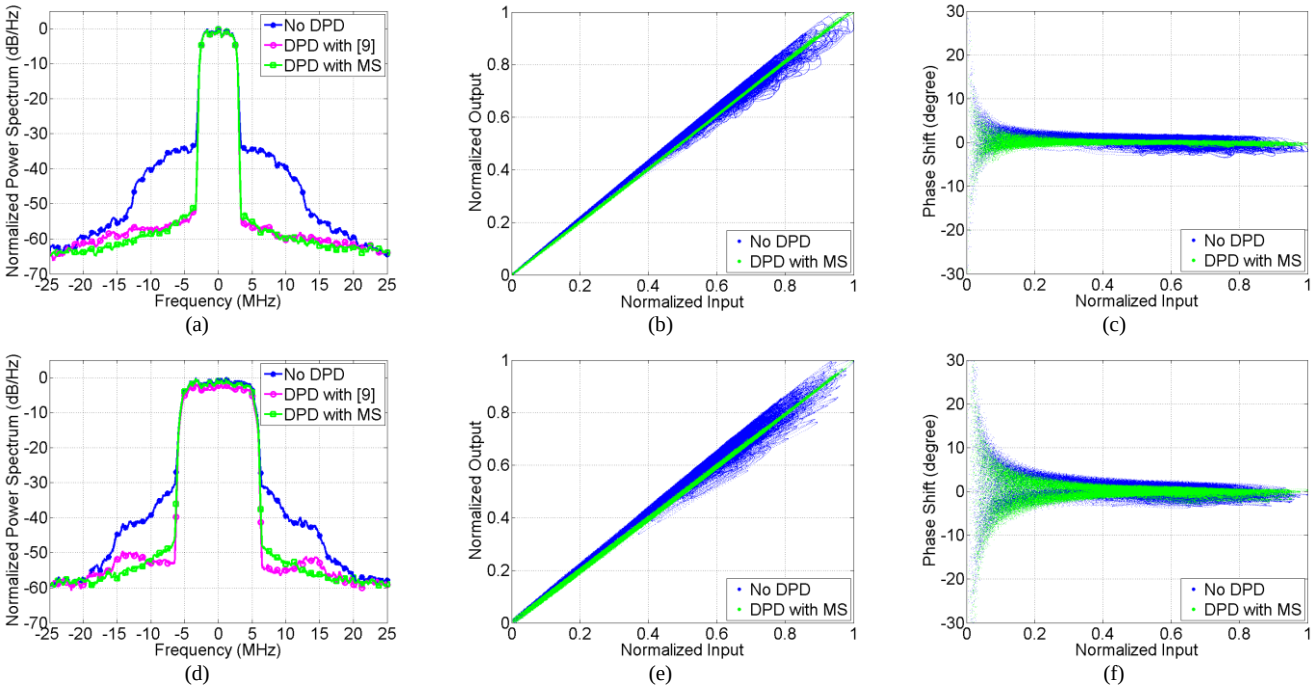

Fig. 11. Dual band DPD results. (a).-(c) Spectrum of the LB signal before and after applying DPD with proposed method and the method of [9], AM-AM and AM-PM plots. (d).-(f) Spectrum of the UB signal before and after applying DPD with proposed method and the method of [9], AM-AM and AM-PM plots. (MS – non-overlapped statistical approximated multi-sine method).

Fig. 10a) and Fig. 10b) present the PA output signal measured directly by the VSA, the modeled signal using the proposed method with multi-sines and the method proposed in [9], and also showing the respective modeling error. Both models were designed with K=7 and M=3. When comparing the estimated modulated signals with the VSA measurement, the proposed method is able to reach a NMSE of -45.99 dB and -40.61 dB for the LB and UB, respectively. Whereas the method of [9] is able to reach a NMSE of -45.26 dB and -39.91 dB in the LB and UB, respectively. Additionally, Fig. 10c) represents the frequency domain of the folded modulated signal acquired by the subsampling feedback loop together with the modeled version and the respective error, reaching an NMSE of -42.09 dB with the proposed method and an NMSE of -41.51 dB with [9]. Therefore, this validates to some extent the complete procedure proposed in the previous sections.

C. Application to a concurrent dual-band DPD scenario

After applying the entire modeling technique to modulated signal the 2D-DPD results are now presented applying an inverse model of K=7 and M=3. Fig. 11 presents the measured results with the VSA at the output of the PA in terms of output spectra, amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM). Moreover, the spectrum results at the output of the PA show the comparison of applying 2D-DPD with the proposed method and with the method of [9]. In fact, by analyzing the total ACPR improvement, one can verify that the prosed method reaches a reduction of 19.98 dBc in the LB and 14.59 dBc in the UB.

TABLE II
MEASUREMENTS RESULTS OF EVM AND ACPR BEFORE AND AFTER DUAL BAND DPD.

			PA Output		
			before DPD	after DPD with MS	after DPD with [9]
Lower Band	EVM rms (%)		1.59	0.48	0.52
	ACPR (dBc)	Lower	33.29	52.73	53.23
		Higher	33.47	54.09	54.86
		Total	30.37	50.35	50.96
Upper Band	EVM rms (%)		3.52	0.82	0.86
	ACPR (dBc)	Lower	35.85	49.99	48.72
		Higher	35.62	50.68	50.49
		Total	32.72	47.31	46.85

Whereas the method of [9], is able to reach a reduction of 20.59 dBc in the LB and 13.78 dBc in the UB. More details of lower band ACPR and upper band ACPR, as also EVM can be found in Table II, for both the proposed method and the method of [9]. A brief comparison in terms of ACPR and EVM performance shows that the method proposed in this paper matches the remaining state-of-the art.

D. Overall Performance Evaluation

The obtained results are considered very promising and similar to other results obtained in other state-of-the art works such as [9], [10], where similar test conditions signals have been performed.

Nonetheless, there are more metrics that should also be evaluated. The main idea of this work was to propose a solution when overlapping of different bands occur using RF subsampling ADCs. If overlapping does not occur both bands are directly available in the digital domain and a traditional 2D-DPD methodology can be applied. However, there may be a given pair of LB and UB carrier frequencies, which cause overlapping between both bands. It is important to refer that this overlapping between LB and UB, may produce equal folding carrier frequencies or not. If the folding frequencies are equal (similar situation to the method of [9]), both our method and the proposed in [9] can be used. The method presented in [9] needs to be modified for a situation where the folding carrier frequencies are not equal, however our method still works in such situation without any additional modification. The only mandatory aspect is to guarantee the multi-sine non-overlapping condition. Other particular aspect of the comparison with [9], is regarding the requirement of a 2-D cross correlation, whereas the proposed method just needs a simple cross correlation, after recovering the LPE of each multi-sine.

When comparing our work with [10], we realize that the proposed method does not need to recalculate and change the sampling frequency, which may be a complicated procedure to do in a real-time application.

Finally, scalability is another important advantage of the proposed multi-sine method, allowing its use with more than two bands. Again, it would be mandatory to guarantee the non-overlapping multi-sine condition, which in an N band case would need to be reformulated to $\Delta f_{offset} = \Delta f/N$.

V. CONCLUSION

In this paper a new technique for concurrent dual-band PA linearization using an RF subsampling-based feedback loop was presented. The presented strategy is based on non-overlapped statistical approximated multi-sine design and allows having any pair of LB and UB modulated signals, even when aliasing occurs between these bands in the feedback loop.

The proposed technique has been validated for a concurrent dual-band DPD scenario, in which the obtained measurement results have shown acceptable ACPR values (> 45dBc) and EVM metrics in the same level as other state-of-the-art approaches recently published. These findings make the proposed technique attractive for realistic commercial implementations, when using wideband carrier aggregated transmitter architectures.

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Paper C2: An agile and wideband all-digital SDR receiver for 5G wireless communications

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An Agile and Wideband All-Digital SDR Receiver for 5G Wireless Communications

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Abstract — In this paper an original agile and wideband all-digital Software Defined Radio (SDR) receiver is presented. The analog-to-digital conversion is based on Pulse Width Modulation (PWM) and it is performed directly at the Radio Frequency (RF) stage. The system is implemented using the high speed differential input buffers of a medium range Field Programmable Gate Array (FPGA) as comparators to quantize the analog signal and generate the PWM representation. Simulation and measured results will be presented and evaluated in terms of Signal-to-Noise Ratio (SNR), Error Vector Magnitude (EVM), bandwidth and power efficiency. Briefly, this architecture allows an input bandwidth of almost 3GHz maintaining an EVM below 2,5% for a 4MHz signal.

Index Terms — Software Defined Radio (SDR), Field Programmable Gate Array (FPGA), Radio Frequency (RF) Analog-to-Digital Conversion (ADC), 5G.

I. INTRODUCTION

Mobile communications are in a constant demand for both bandwidth and Quality of Service (QoS) within a high mobility scenario. Additionally, in the next decade it is expected an high growth of devices, not just due to personal mobile devices but mainly due to the Internet of Things (IoT), which will spread Machine-to-Machine (M2M) communications. According to current trends, in addition to the required high data rates, 5G networks will be characterized by cooperative operation between different technologies and heterogeneous networks, denser base station deployments, improved power efficiency and higher levels of connectivity among devices to support the IoT. Therefore, the telecommunications academia and industry are searching for solutions to deploy 5G networks in an efficient way capable to answer the previous requirements without significant additional Capital Expenditures (CAPEX) and Operational Expenditures (OPEX) costs for the operators [1]. Several enabling technologies, such as C-RAN (Cloud-Radio Access Network) and small/pico-cell deployment, Massive-MIMO, Software Defined Radio (SDR) and mm-Wave are being pointed as 5G networks enablers [1-3], covering a wide range of research topics. Within this context, a central issue is the need of high bandwidth, flexibility and power efficiency in the physical Radio Frequency (RF) chain, which is a challenge that must be addressed by suitable SDR architectures in both RF transmitters and receivers.

The bandwidth and agility of RF receivers are the focus of this paper, where a suitable and innovative architecture to improve them will be proposed. Traditional RF receivers are commonly based on: analog I/Q (phase and quadrature components) direct down-conversion architectures with baseband sampling (1); down-conversion from RF to IF and IF sampling with digital I/Q down-conversion (DDC) (2); or direct RF sampling also with I/Q DDC (3). The first architecture comprises problems regarding the imbalance of the analog I/Q demodulator and other impairments caused by the analog components, which may be solved with post-compensation in digital domain after a proper calibration. The second does not suffer from I/Q imbalance, since I/Q demodulation is performed in digital domain the imbalance is almost inexistent. However, the analog component will present other impairments. Additionally, both first and second architectures have limited flexibility, depending on the frequency range of the mixers and the other analog components. The final one is closer to the ideal SDR concept [3], with reduced number of analog components and posing high flexibility. Nevertheless it requires high-speed ADCs which may be expensive and may present high power consumption. In respect to flexibility and to cope with high bandwidth, this is the preferable architecture, taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches [4]. Therefore, it is easy to understand that to achieve flexibility and wider bandwidth in the RF receiver chain there is a fundamental system element: the analog-to-digital converter (ADC). Additionally, an SDR topology could be an enabler of digital RAN architectures, such as C-RAN which is a strong proposal architecture for 5G networks. Due to the high potential of RF sampling architectures, this will be the focus of this paper as will be described in the further Sections.

In this work, an innovative all-digital FPGA-based SDR receiver founded on Pulse Width Modulation (PWM) is presented. The proposed architecture is highly flexible, power efficient and presents a high analog input bandwidth which is extremely attractive for 5G communications. Validation is performed via simulation and measurement results, considering the evaluation of important RF Figures of Merit (FoMs) such as Signal-to-Noise Ratio (SNR) and Error Vector Magnitude (EVM) for several carrier frequencies and signal

bandwidths. The remainder of this paper is divided as follows. In Section II state of art of RF sampling ADCs and digital RF receivers is presented. In Section III the PWM ADC architecture and work principle is explained. In Section IV an innovative FPGA-based all-digital architecture for wideband and agile RF sampling receivers is presented. In Section V simulation and measurement results of the proposed architecture implemented using a medium-range FPGA are presented and discussed. Finally, some conclusions are drawn in Section VI.

II. Overview of RF Sampling Architectures

Current commercial RF ADCs have reached the order of a few GHz both in sampling frequency as also in input bandwidth. As an example, one can refer the Texas Instruments (TI) ADC ADS5400 that is S/H (Sample and Hold) based with several pipeline stages [5]. However, they are expensive and responsible for a considerable energy consumption reducing the overall system's efficiency. Furthermore, when it is necessary to reach frequencies higher than approximately 2 GHz mixer-based architectures are required increasing the overall system's cost [4].

Recently there are arising new possibilities to build RF ADCs: based on delta-sigma modulation (DSM) [6], voltage-controlled oscillators (VCO) [7, 8] or PWM [9]. All these types of ADCs share the common basis of being single-bit ADCs, i.e., all they deal with a digital pulsed representation of the analog signal. The DSM ADCs are well known in audio applications, where they provide high resolution [4]. Some research is being done in order to apply these ADCs in the RF world, as presented in [6]. Even though the good figures of merit that have been obtained in [6], the needs for a low latency feedback path can impose several limitations in terms of increasing the effective sampling frequency. A VCO-based ADC can be seen as pulse frequency modulation (PFM) achieved using the VCO as input for the analog signal [7]. These types of ADCs present high undesirable nonlinearities related with the VCO behavior, which have been addressed by the scientific community through the use of feedback loops or digital calibration techniques [8]. The PWM ADCs comprise a single comparator, whose inputs are the analog signal and a known reference (usually a triangular wave), generating a PWM representation of the signal [10]. They are commonly used in low-frequency applications [10, 11]. Nevertheless, recently they are also being brought to the RF world, as presented in [9]. However, the results obtained in [9] reveal a weak SNR and EVM. Additionally, in [9] are used high speed comparators to generate the PWM representation, which are expensive components. These last two aspects make the system unfeasible for a real application scenario. The authors of this paper believe that the PWM ADCs have more potential than the obtained in [9], by performing a correct choice of the reference signal and without using expensive high speed comparators. Therefore, this work will present an architecture that will improve both performance and cost of the work presented in [9].

III. PWM ADC Architecture and Working Principle

An ADC comprises two processes: sampling and quantization, which corresponds to discretization in both time and amplitude respectively. In this section the PWM ADC working principle will be briefly addressed focusing both these aspects.

A PWM ADC is mainly based in a comparison between two signals: the desired analog signal (x(t)) and the reference (r(t)), generating a PWM representation of the desired signal (y(t)) (Fig. 1). In this way the PWM signal y(t), can be expressed as:

$$y(t) = sign\big(x(t) - r(t)\big),$$

where x(t) is the input signal, r(t) is the reference signal and considering the sign function defined as:

$$sign\big(z(t)\big) = \begin{cases} -1\,, if\ z(t) < 0 \\ +1\ \,, if\ z(t) > 0. \end{cases}$$

Fig. 1 presents a block diagram of the architecture using a comparator. The comparator has the same behavior as the sign function acting as a single-bit quantizer.

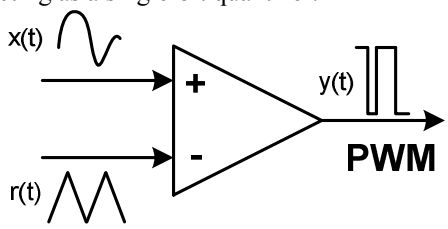


Fig. 1 - Block diagram of a PWM converter.

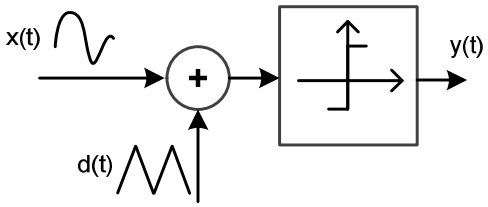


Fig. 2 - Block diagram of the stochastic-ergodic converter [12].

The working principle of this type of converters is similar to the stochastic-ergodic converter (Fig. 2) presented in [12], which was a popular idea in the nineteen-sixties to build low cost ADCs. In that time the stochastic-ergodic converter idea was abandoned due the high variance that these type of converters produce and due to the lack of technology to enable a successful use of this architectures [12]. The idea of this converter is to add some form of dither (d(t)) to an analog signal (x(t)) and fed it in a single-bit quantizer (Fig. 2). The theoretical proof of these converters can be developed based on statistical theory of quantization [13], which show that if the dither signal has an uniform distribution, the mean of the input signal (x(t)) is contained in the output PWM signal

((y(t)), allowing to recover the original signal [12]. An example of a signal with uniform distribution is a triangular wave, which is commonly used in this type of converters due to the previous explanation. In addition to the reference signal's amplitude distribution, another important aspect is its frequency that defines the maximum bandwidth of the signal to sample [12].

After the quantization process it is necessary to sample the signal, that despite of already being represented in two well defined levels, it is not a discrete-time representation. There are at least two ways to discretize this signal by doing it uniformly or not uniformly. The latter leads to a non-uniform sampling process, which is the method used in level-crossing ADCs [14]. However, this requires challenging interpolation methods in order to restore a uniform sampling rate, which is not in the scope of this work. The uniform sampling is simpler and can be easily implemented by directly sampling the bi-level signal at a constant clock frequency, that should be high enough to register all possible PWM transitions.

Finally, it is important to state that the PWM signal generation implies high non-linear phenomena, generating an high level of quantization noise and harmonic distortion that will tend to decrease the signal integrity. This fact will demand to choose a proper reference signal, depending on the signal to acquire, as it will be discussed further in this paper.

IV. FPGA Implementation Architecture

The majority of the RF sampling receiver architectures use FPGAs in order to accommodate the high data rate from a RF ADC. For example in [9] an FPGA is used to accommodate the data rate from the high speed comparators.

An innovative possibility is to use directly the FPGA high speed differential input pins to build the comparator quantizer. This allows a substantial reduction of both system's cost and power consumption, when compared to common RF sampling receivers that already use these types of inputs. The referred inputs are available in the Multi-Gigabit Transceivers (MGTs), which are based on high speed Serializer/Deserializer (SerDes). These are commonly used to implement high speed serial communication links such as SATA, PCIe and recently they are already used to implement all digital SDR transmitters as presented in [15]. In this paper, as the best of the author's knowledge this is the first time that the MGTs are used to implement an SDR receiver.

The proposed FPGA-based SDR receiver architecture is presented in the block diagram of Fig. 3. In this architecture after the antenna there is a bandpass filter in order to select the specific band to receive, which is followed by a Low Noise Amplifier (LNA) with variable gain amplification (VGA) in order to adjust the amplitude of the x(t) signal to be less than the r(t) signal. Alternatively, the amplitude of r(t) can also be changed. After the LNA/VGA there is the FPGA MGT input. The MGT is a quite complex element, however for this purpose it can be simplified as presented in Fig. 3, i.e., a input differential buffer followed by a Serial In- Parallel Out (SIPO) block. The latter is responsible for the sampling rate reduction from a high sampling rate (F_s) up to a low sampling rate capable to be dealt in the standard FPGA logic (F_s/N). At the SIPO's output there is a N-bit parallel word which represents the PWM signal. This parallel word contains a PWM representation of the x(t) signal centered in f_c and sampled at F_s.

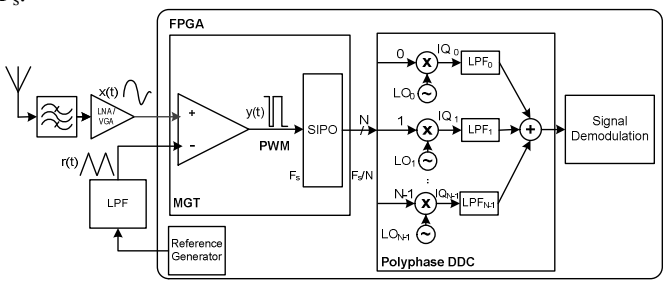


Fig. 3 - Block diagram representation of the proposed architecture.

Therefore, the signal must be digitally down-converted, filtered and decimated up to a low sampling rate to consequently be possible to demodulate and acquire the signal's information. Since the MGTs operate at GHz frequencies (F_s), a suitable polyphase architecture for the DDC must be designed to become possible to operate a F_s sampling inside the FPGA. The DDC is made of a I/Q Direct Digital Synthesizer (DDS), a mixer and Low Pass Filter (LPF). The DDS is in fact formed by N DDS's working with different input phase increments in order to generate a proper sine wave at f_c, in an aggregate sampling frequency of F_s. The mixer is in fact a multiplexer selecting between the DDS output and zero, using the corresponding bit of the MGT parallel word as selector. The last component is the LPF decimation filter, which is a component that should be optimized to the minimum possible order while maintaining an appropriate performance. An adequate filter topology is a CIC filter that produces efficient decimation structures or common FIR filters using specific windows such as Kaiser, Chebyshev or Hamming, which also produce efficient structures. This DDC presents high degree of flexibility being capable to down-convert any sampled signal. Finally, after the DDC the signal is in the base-band and it is represented in a low sampling rate, allowing recovering its information by proper demodulation techniques.

Regarding the reference signal generation (r(t)), this can be performed inside the FPGA using the well-known FPGA-based all-digital transmitter's architectures as presented in [15].

V. Experimental Setup And Results

To validate the proposed architecture in the previous section it was assembled the experimental setup presented in Fig. 4. To generate the reference and the RF signal it was used an Arbitrary Waveform Generator (AWG) – AWG70006 from

Tektronix with high sampling rate (F_s = 16GSample). It was chosen to generate the reference signal in the AWG in order to focus the experimental part in the receiver component, assuming that the reference can be generated with techniques similar to the presented in [15]. Regarding the FPGA, it was used a KC705 development board from Xilinx with a Kintex 7 FPGA. This FPGA is equipped with GTX transceivers capable of a maximum bitrate of 12 Gbps. The GTX transceiver was configured to a rate of 10 Gbps and to generate a parallel word of 64 bits at the deserializer output. This implies that the polyphase DDC will run in 64 parallel paths at a frequency of 10GHz/64 = 156,25 MHz. The LPF was designed using the Matlab Filter Design & Analysis Tool considering a FIR structure with a Chebyshev window generating a filter with order 63 to decimate by a factor of 16, followed by another with order 15 to decimate by 4. The combination of these filters allow a sample rate reduction from 10 GHz up to 156,25 MHz. Fig. 5 presents a photo of the laboratorial setup.

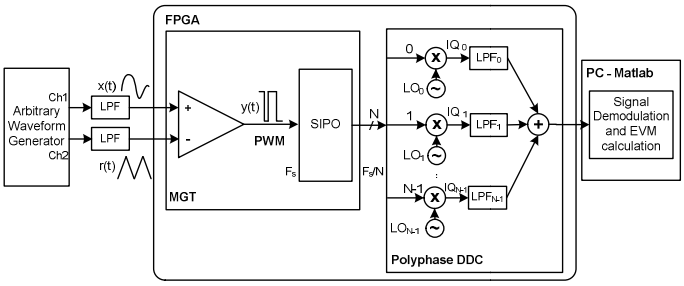


Fig. 4 - Block diagram representation of the laboratorial setup assembled to validade the proposed architecture.

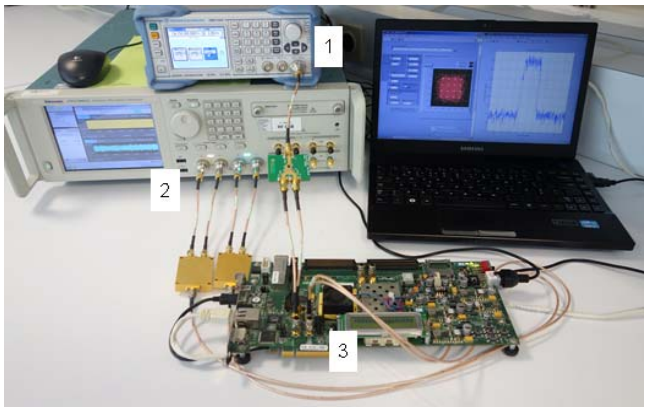


Fig. 5 - Photo of the laboratorial setup. 1 - Clock generator; 2- AWG; 3 - KC705 development kit.

In order to validate the proposed architecture it was performed a sweep on the carrier frequency of the input signal (x(t)), while mantaining a constant signal bandwidth. For each carrier frequency different reference signal frequencies were tested. Therefore the signal was acquired and processed using a Matlab routine. This routine is responsible to calculate the Error Vector Magnitude (EVM) of the signal. The first sweep was performed for a 16-QAM 2MHZ signal, and the simulation and measured results are presented in Fig. 6. It is important to state that the simulation consider an ideal comparator, which is far from reality. Observing the Fig. 6 it is possible to observe that the simulation results produce an almost constant EVM near 0.5 %. Regaring the measurment results the EVM is lower than 2%, i.e., SNR lower than 34 dB, for carrier frequencies above 2,5 GHz. Figs. 7, 8 and 9 present the baseband spectrum and the constelattion diagram of an acquisition with a 16-QAM 2MHz signal centered at 950MHz, 1800 MHz and 2400 MHz, respectively.

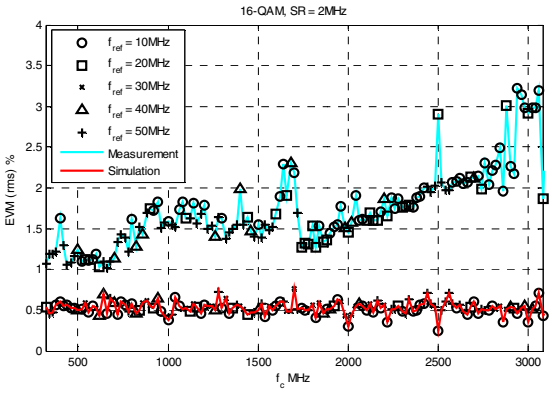
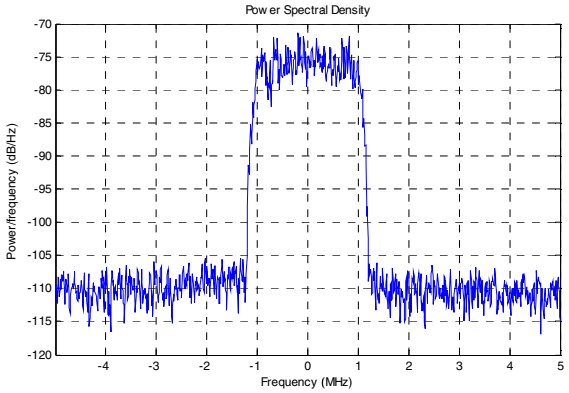


Fig. 6 - Measured and simulated results of a sweep over the carrier frequency using a 2MHz 16-QAM modulated signal.

a)



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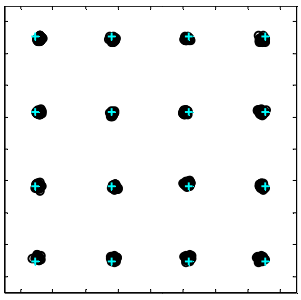
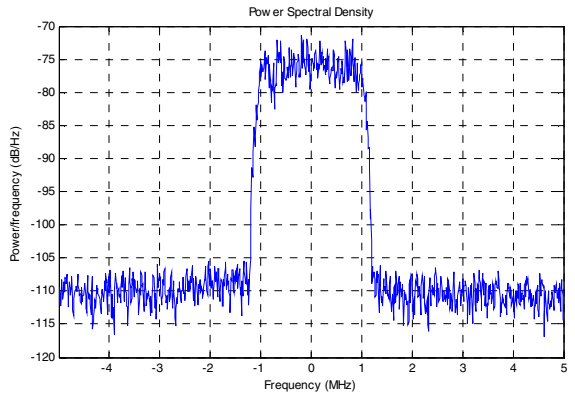


Fig. 7 – a) Baseband frequency domain representation of an acquired 2MHz 16 QAM signal centered at 950 MHz. b) Constellation diagram representation of the same acquisition (EVM_{rms} = 1.51 %).

a)



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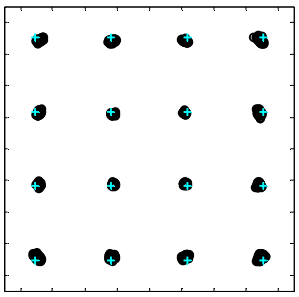
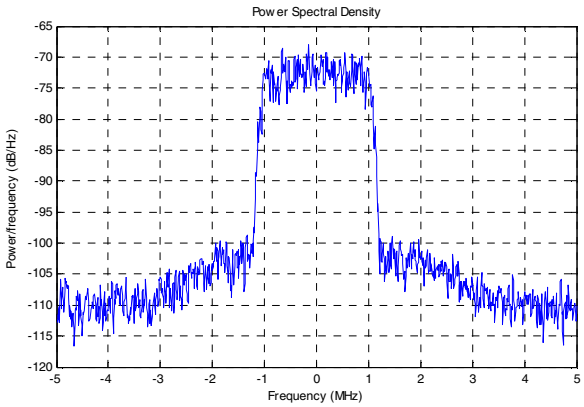


Fig. 8 – a) Baseband frequency domain representation of an acquired 2MHz 16 QAM signal centered at 1800 MHz. b) Constellation diagram representation of the same acquisition (EVM_{rms} = 1.54 %).

a)



b)

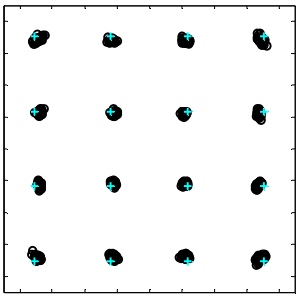


Fig. 9 – a) Baseband frequency domain representation of an acquired 2MHz 16 QAM signal centered at 2400 MHz. b) Constellation diagram representation of the same acquisition (EVM_{rms} = 1.89 %).

A second sweep was also performed with a 4MHz 16-QAM signal and the results are presented in Fig. 10. It is possible to verify a increase in the obtained EVM, altough it stills lower than 2,5 %, which corresponds to 32 dB of SNR. Both the previous presented sweeps (Fig. 6 and Fig. 10) present a slightly increase of EVM above 2,5GHz, that can be explained due to mismatch impairments at the FPGA input, and to non-linearities of the input comparator. Nevertheless, the previous results proof the high flexibility of these architecture, while mantaining a reasonable performance in almost 3 GHz of bandwidth. Both sweeps were performed using a voltage of $500mV_{pp}$ (-2.04 dBm) at the output of the AWG, for both the RF and reference signals.

The amount of FPGA resources used to implement the proposed design is presented in Table 1. It is possible to verify that despite a high quantity of DSP Slices are used there still are enough resources to other digital signal processing requirements such as the signal demodulation. However, the filtering structure could be improved using CIC filters, which are very efficient structures for decimation operations.

Finally, the Vivado tool estimates a total on chip power consumption about 4.4 W, considering the entire FPGA project developed for this work. This power analysis tool also indicates the amount of power on specific elements such as BRAMs, MMCMs, PLLs, GTX, DSP slices, between others. In this way considering the GTXs, the MMCMs and the DSP slices, which are the most important elements within the context of this work, the value of power consumption is about 1.22 W.

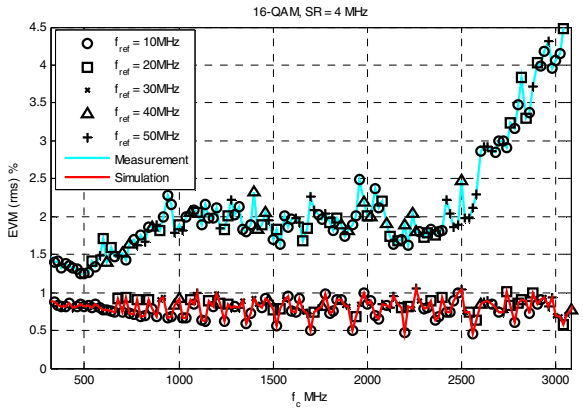


Fig. 10 - Measured and simulated results of a sweep over the carrier frequency using a 4MHz 16-QAM modulated signal.

TABLE 1 – FPGA RESOURCES UTILIZATION.

Resource	# Utilization	# Available	% Utilization
Flip-Flops	51575	407600	13
LUTs	31375	203800	15
DSP48	352	840	42
GTX	1	20	5

VI. Conclusion

In this paper it was presented an innovative FPGA-based all-digital and highly flexible architecture of a wideband RF receivers. It was shown that a 16-QAM modulated signal with up to 4MHz of bandwidth can be successfully recovered with a reasonable SNR, in about 3 GHz of spectra. In addition to the flexibility it was shown that the system can be implemented using a medium-range FPGA and without using analog mixers or high cost ADCs, which represents an improvement in manufacturing cost and energy consumption. This system is suitable to be implemented in several applications scenarios, such as 5G, Digital Pre-distortion (DPD) applications and low-power RF applications that will be extremely important in future IoT scenarios.

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Paper C3: FPGA-based all-digital Software Defined Radio receiver

[C3] - A. Prata, A. S. R. Oliveira, and N. B. Carvalho, “FPGA-based all-digital Software Defined Radio receiver,” in 2015 25th International Conference on Field Programmable Logic and Applications (FPL), 2015, pp. 1–2.

FPGA-based All-digital Software Defined Radio Receiver

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Abstract — In this Ph.D. work it is intended to explore innovative agile and wideband FPGA-based Software Defined Radio (SDR) receiver architectures for future 5G wireless communications. This short paper presents some preliminary work in this area, including interesting results of an innovative SDR receiver. This new architecture implements the analog-to-digital conversion directly at RF stage based on Pulse Width Modulation (PWM). The system is implemented using the high speed differential input buffers of a medium range FPGA as a comparator. Simulation and measured results will be presented and evaluated in terms of Signal-to-Noise Ratio (SNR) and Error Vector Magnitude (EVM). Briefly, this architecture allows an input bandwidth of almost 3GHz maintaining an EVM below 2% for a 2MHz wide signal.

I. Introduction

The traffic and the number of mobile network users is increasing, leading to successive generations of standards with higher throughput and mobility support. According to current trends, in addition to the required high data rates, 5G networks will be characterized by cooperative operation between different technologies and heterogeneous networks, denser base station deployments, improved power efficiency and higher levels of connectivity among devices to support the so-called IoT (Internet of Things). Therefore, telecommunications academia and industry are searching for solutions to deploy 5G networks in an efficient way capable to answer the previous requirements. Within this context, a central issue is regarding the needs of high bandwidth, flexibility and power efficiency in the physical Radio Frequency (RF) chain, which is a challenge that must be addressed by suitable Software Defined Radio (SDR) architectures in both RF transmitters and receivers [1].

This Ph.D. addresses the agility and extensibility of the RF front end in order to efficiently support newer generations of mobile networks. The work will focus on the RF front end architecture and its implementation on reconfigurable digital devices (FPGAs), leading to its virtualization, i.e. the runtime transceiver reconfiguration allowing its adaptation to particular communication scenarios, in order to meet the throughput and multi-standard requirements of newer mobile network generations. The bandwidth and agility problems of RF receivers are the focus of this paper, where a suitable and innovative architecture to solve them will be proposed. Traditional RF receivers are commonly based on analog down-conversion, with base-band or IF (Intermediate Frequency) sampling, which presents some impairments and limited flexibility. Alternatively, the RF receivers can built in direct RF sampling architectures, similar to the ideal SDR concept, with reduced number of analog components and posing high flexibility. In respect to flexibility and to cope with high bandwidth, this is the preferable architecture, taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches.

Current commercial RF ADCs have reached the order of a few GHz in sampling frequency and input bandwidth. However, they are expensive and responsible for a considerable energy consumption reducing the system's efficiency. Recently there are arising new possibilities to build RF ADCs: based on delta-sigma modulation (DSM) [2] and PWM [3]. These types of ADCs share the common basis of being mono-bit ADCs, i.e., all they deal with a digital pulsed representation of the analog signal. The DSM ADCs are well known in audio applications, where they provide high resolution. Some research is being done in order to apply these ADCs in the RF world, as presented in [2]. Even though the good figures of merit that have been obtained in [2], the needs for a low latency feedback path can impose several limitations in terms of increasing the effective sampling frequency. The PWM ADCs comprise a single comparator, whose inputs are the analog signal and a known reference (usually a triangular wave), generating a PWM representation of the signal [4]. They are commonly used in low-frequency applications [4, 5]. Nevertheless, recently they are also being brought to the RF world, as presented in [3]. However the results obtained in [3] reveal a weak SNR and EVM. Additionally, in [3] are used high speed comparators to generate the PWM representation, which are high cost components. These last two aspects make the system unfeasible for a real application scenario. The authors of this paper believe that the PWM ADCs have more potential than the obtained in [3], by performing a correct choice of the reference signal and without using expensive high speed comparators. Therefore, this work will present an FPGA-based architecture that will improve both performance and cost of the work presented in [3].

II. Proposed Architecture

An innovative possibility to build a PWM ADC is to use directly the FPGA high speed differential input buffers to build the comparator quantizer. This allows a substantial reduction of both system's cost and power consumption, when compared to common RF sampling receivers that already use

FPGAs to gather data. The referred inputs are available in the Multi-Gigabit Transceivers (MGTs), which are based on high speed Serializer/Deserializer (SerDes). These are commonly used to implement high speed serial communication links, nevertheless recently they are already been used to implement all digital SDR transceivers as presented in [6].

The proposed FPGA-based SDR receiver architecture is presented in the block diagram of Fig. 1. In this architecture after the antenna there is a bandpass filter in order to select the specific band to receive, which is followed by a Low Noise Amplifier (LNA) with variable gain amplification (VGA) in order to adjust the amplitude of the *x(t)* signal to be less than the *r(t)* signal. After the LNA/VGA there is the FPGA input in which the MGT is used. The MGT is a quite complex element, however for this purpose it can be simplified as presented in Fig. 1, i.e., a input differential buffer followed by a Serial In-Parallel Out (SIPO) block. The latter is responsible for the sampling rate reduction from a high sampling rate (F_s) up to a low sampling rate capable to be dealt in the standard FPGA logic (F_s/N). At the SIPO's output there is a N-bit parallel word which represents the PWM signal. The signal is at this point a PWM signal sampled at F_s, containing the information of the *x(t)* signal at its carrier frequency.

Therefore, to recover the signal this must be digitally down-converted, filtered and decimated up to a low sampling rate to consequently be possible to demodulate and acquire the signal's information. In order to become possible to operate a Fs sampling in the FPGA, a suitable polyphase architecture for the digital down conversion (DDC) must be designed. This DDC presents high degree of flexibility being capable to down-convert any sampled signal. Regarding the reference signal generation (*r(t)*), this can be performed inside the FPGA using the well-known FPGA-based all-digital transmitter's architectures as presented in [6].

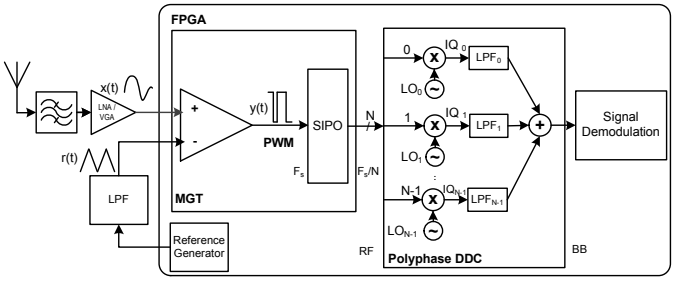

Fig. 1 - Block diagram representation of the proposed architecture.

III. Preliminary Results

In order to validate the proposed architecture it was performed a sweep on the carrier frequency of the input signal (*x(t)*) mantaining a constant signal bandwidth. For each carrier frequency different reference signal frequencies were tested. Therefore the signal was acquired and processed in order to calculate its Error Vector Magnitude (EVM). Fig. 2 presents a sweep performed with a 16-QAM 2MHZ signal, including simulation (considering an ideal comparator) and measured results. These results prove the high flexibility of this architecture, while mantaining a reasonable performance in almost 3 GHz of bandwidth, which represent an important figure of merit of the new proposed architecture.

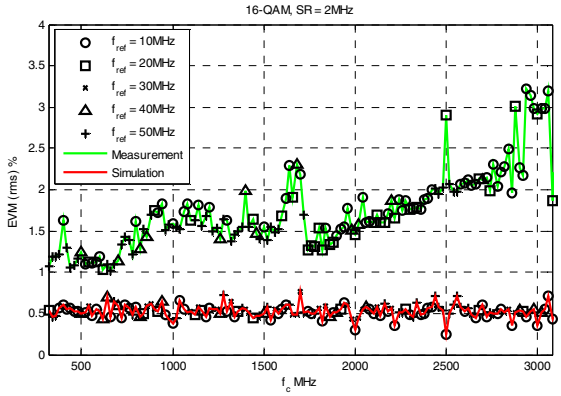

Fig. 2 - Measured and simulated results of EVM in a sweep over the carrier frequency using a 2MHz 16-QAM modulated signal.

IV. Conclusion

In this paper it was presented an innovative FPGA-based all-digital and highly flexible architecture suitable for next generation SDR receivers. Future work is planned in order to improve the bandwidth and the SNR of the proposed receiver, by compensating the impairments introduced by the input differential buffer used as comparator.

Acknowledgement

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Paper C4: FPGA-based all-digital software defined radio system demonstration

[C4] - R. F. Cordeiro, A. Prata, A. S. R. Oliveira, N. B. Carvalho, and J. N. Vieira, “FPGA-based all-digital software defined radio system demonstration,” in 2015 25th International Conference on Field Programmable Logic and Applications (FPL), 2015, pp. 1–1.

FPGA-based All-digital Software Defined Radio System Demonstration

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III. Demo Description

All-digital radios allow the full digitalization of the radio system which poses an important step towards the complete software description of RF signals proposed in SDR. Using digital signal processing techniques and the integration of the radio into a single digital chip, it is expected that high flexibility in these systems will be fundamental for the next generation of wireless networks. In addition, FPGA-based architectures take advantage of the high and heterogeneous processing power of modern FPGAs as well as their dynamic configurability capabilities needed for highly flexible radio transceivers.

This demonstration presents a highly flexible FPGA-based all-digital SDR end-to-end communication system with both transmitter and receiver implemented using medium-range FPGAs.

The transmitter component is based on the complete generation of RF signals using a digital datapath up to the RF upconversion. Delta-Sigma Modulation (DSM) or Pulse Width Modulation (PWM) is used to convert the baseband samples to a single bit resolution baseband signal. The signal up-conversion is done combining in-phase and quadrature 1-bit samples in time-multiplexing. The high-speed conversion occurs using a parallel in serial out FPGA embedded dedicated hardware that works at four times the desired carrier frequency. Fig. 1 presents the transmitter block diagram with the baseband processing, signal shaping and up-conversion stages implemented in an FPGA. The output signal of the FPGA is already at RF frequencies.

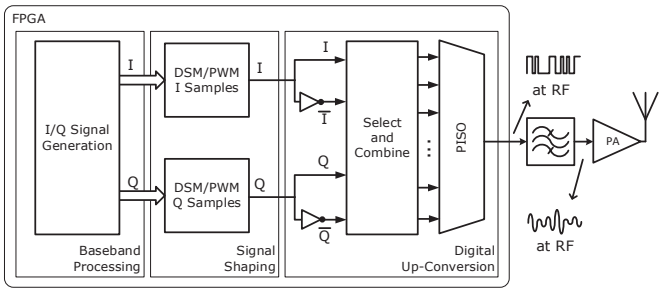

Fig. 1 – Block diagram of the RF transmitter component.

The receiver implements analog-to-digital conversion based on PWM, by using the FPGA input differential buffers as a high speed comparator between the signal to sample and a given reference. Fig. 2 presents a block diagram of the receiver component. After the antenna, there is a bandpass filter to select the band to receive and amplification, followed by the PWM sampling, which is performed using the FPGA input buffers. The reference waveform is also generated inside the FPGA. All the necessary digital signal processing, such as digital down-conversion and filtering is done inside the FPGA. Afterwards the signal is transferred to a computer where signal analysis will be performed presenting fundamental results such as the signal's spectrum, Error Vector Magnitude (EVM), Signal-to-Noise Ratio (SNR) and the constellation diagram.

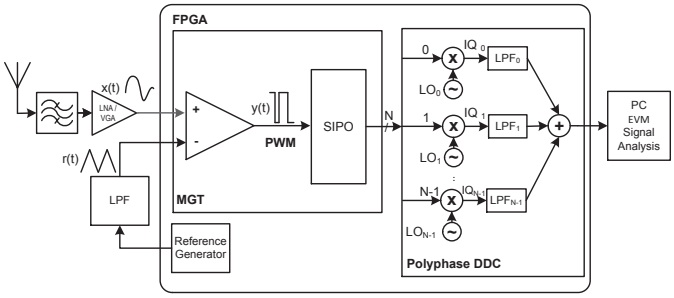

Fig. 2 – Block diagram of the RF receiver component.

Paper C5: All-digital transceivers — Recent advances and trends

[C5] - • A. Prata, R. F. Cordeiro, D. C. Dinis, A. S. R. Oliveira, J. Vieira, and N. B. Carvalho, “All-digital transceivers — Recent advances and trends,” in 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2016, pp. 233–236.

All-Digital Transceivers - Recent Advances and Trends

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***Abstract*—This paper provides an overview on recent advances on all-digital transceivers, as a promising approach to the ideal Software-Defined Radio concept. Several techniques and architectural optimizations are discussed to improve the coding efficiency, spectral purity, signal to noise ratio, bandwidth and flexibility.**

I. Introduction

After four generations of mobile communications with considerable improvements in the user data rates, quality of service and proliferation of cellular infrastructures, the fifth generation (5G) is being prepared and should be deployed by 2020. Peak data rates of 10 Gbps (everywhere and everytime), latencies lower than 10 msec (to support hard realtime applications) and huge device densities (in IoT scenarios), are some of the expected disruptive capabilities [1]. Therefore, 5G radios must efficiently answer to the new communication challenges as well as incorporate previous standards. This implies features such as agility, flexibility, real-time reconfigurability, multi-mode and multi-standard support, which are receiving more and more attention. On the other hand, the trend is to move most of the radio design to the digital domain [2] using Software-Defined Radio (SDR) techniques and, more recently, all-digital approaches. The integrated RF frontends and mixed signal integrated circuits currently available, with ADCs, DACs, filters (either digital or analog), mixers and amplification stages provide many advantages over the traditional discrete-level analog circuitry, in terms of flexibility, size and reduction of analog circuit impairments and mismatches [3]. However, the option for this mixed-signal approach is slowing down, since the analog integration design does not follow the Moore's Law as it happens with the digital integrated circuits [2]. Thus, the natural solution for this problem, is the transition from the mixed-signal methodology to fully digital approaches, with digital logic mimicking the traditional functions undertaken by the analog components.

The concept of All-Digital Transceivers (ADTxRx) has been pointed out as a promising path towards this goal [2]. In their essence, they consist on the design and development of flexible architectures with a fully radio datapath completely defined in the digital domain. By doing this, RF signal generation and analysis move closer to the antenna, removing most of the conventional analog hardware from the transmission and reception chains and its associated problems. This concept allows to take advantage of many benefits that are directly related with digital circuitry such as the miniaturization, the high computation power and predictable behavior. Furthermore, most all-digital transceiver architectures rely on FPGAs for their implementation, exploring the huge computational power and parallelism, I/O bandwidth and flexible integration capacity of modern FPGA devices in order to build custom processing and digital conversion architectures as well as the required dynamic reconfiguration methodologies that fulfill the next generation transceivers requirements.

Usually, all-digital radio architectures rely on the use of Digital Upconversion (DUC) and Digital Downconversion (DDC) schemes together with high speed digital logic data converters. Low resolution and high speed ADCs and DACs, together with pulse shaping techniques allow for these systems to have a good performance on most of commonly used wireless standards, fostering a high level of integration. Fig. 1 shows the typical structure of an all-digital transceiver and its interface with the antenna and baseband processing. On the transmitter side, by reducing the amplitude resolution of the signals with pulse shaping techniques, 1-bit RF DACs and highly-efficient Switched-Mode Power Amplifiers (SMPAs) can be used rather than the traditional and non-efficient topologies. The output filter provides a sufficient filtering for the quantization noise to avoid interference between channels. The receiver uses a high-frequency 1-bit sampler, working as an RF ADC, capable of sampling a large amount of bandwidth. By performing all the operations in the digital domain, the system features a high level of real-time reconfigurability required for multi-standard support and a increased potential for massive integration.

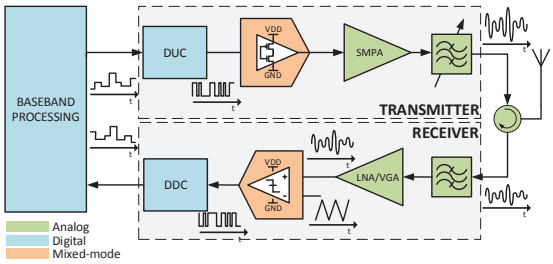

Fig. 1: All-digital transceiver basic architecture.

This paper presents the latest advances in the field of FPGA-based all-digital transceivers with emphasis on the fundamental concepts, relevant challenges and design methodologies.

II. All-Digital Transmitters

All-Digital Transmitter (ADTx) architectures all share the same principle where the input signal is processed in the digital domain for both the baseband and the RF stages in a Digital Signal Processing (DSP) unit. As shown in Fig. 1, the pulsed digital RF is converted to the analog domain using a high speed digital buffer and being afterwards amplified using a 2-level SMPA. An output reconstruction filter is used to remove the quantization noise from the pulsed signal.

Pulse-based modulators using Pulse Width Modulation (PWM) or Delta-Sigma Modulation (DSM) convert the multi-level signal into a two level signal. State-of-the-art pulsed

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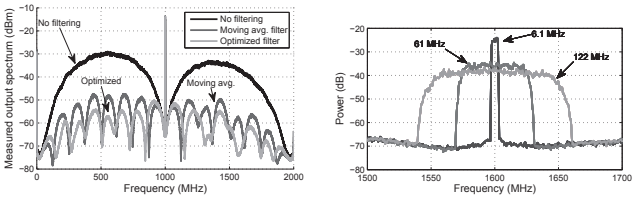

(a) (b)

Fig. 2: (a) ADTx's output spectrum using a CE improvement method by combining multiple pulsed signals [8], and (b) ADTx's spectra of the proposed modulator in [10], capable of 122 MHz of bandwidth.

transmitters presented in the literature fall within this principle, with amplitude and phase modulation of the RF carrier using band-pass DSM [4], PWM [5], low-pass DSM with DUC [6] or hybrid DSM-PWM architectures [7].

The use of DSP techniques and the integration of the radio into a single digital chip enable highly flexible telecommunication systems which will be fundamental for the next generation of wireless communications. There are however some challenges in the use of all-digital radios that must be addressed for these systems to be considered as a viable alternative for RF transmission.

A. Coding Efficiency (CE) and Spectral Purity

Although digital pulse transmitters allow for the use of very efficient amplification techniques, usually most of the power is unwanted quantization noise. The use of low amplitude resolution RF signals introduces a substantial amount of noise that should be filtered to avoid interference with other frequency bands. This quantization noise is transversal to all the pulse shaping techniques such as DSM or PWM. Furthermore, the transmitter total power efficiency should consider the CE together with Power Amplifier (PA) efficiency which will considerably lower the power efficiency gains. Most of the state-of-the-art systems have less than 30% CE, however this value usually depends on both the modulator used and also on the properties of the transmitted signal. In [8] it is shown the dependency of the CE with the baseband signal Peak-to-Average Power Ratio (PAPR). As the PAPR value increases the CE starts to decrease even further.

Noise cancelation techniques have been used to partially remove the quantization noise and improve the transmitter efficiency. These techniques combine multiple signals to generate RF outputs that have higher coding efficiency at the trade of lower drain efficiency [9]. Although with lower drain efficiency, these systems establish an optimal point between CE and PA drain efficiency which improves the overall system efficiency.

In [8], it is shown a new reconfigurable filtering technique for all-digital transmitters using signal interference and cancellation between multiple outputs. This technique is used to reduce the quantization noise from the all-digital transmitters output, as seen on Fig. 2(a), reducing the analog output filter requirements and improving the transmitters coding efficiency. The presented results show the quantization noise reduction without an output analog filter, contributing to an increase of the transmitters CE up to more than 95%.

B. Signal to Noise Ratio and Bandwidth

PWM and DSM allow for the conversion of high amplitude resolution signals into their pulsed representation while minimizing the quantization noise in the signals bandwidth. Oversampling improves the Signal-to-Noise Ratio (SNR) for these modulators which enables the use of pulsed transmitters conforming to the necessary signal quality transmission for modern wireless standards. The relationship between Oversampling Ratio (OSR) and SNR can be defined for DSM and PWM according to equations (1) and (2) respectively.

$$\begin{aligned} SNR_{DSM} &= 2.01(2L+1)log_2(OSR) - 9.36L - 2.76 \\ SNR_{PWM} &= 20log(M) + 1.76 + 10log(OSR) \end{aligned} \quad (1)$$

where *M* is the number of uniform sampling PWM levels and *L* is the DSM filter order.

In both PWM and DSM, the sampling frequency, f_s, is generally enforced by the maximum hardware frequency, meaning that signals with higher bandwidth have lower OSR, and therefore, lower SNR $\left(OSR = \frac{f_s}{2BW}\right)$. On the other hand, improving OSR, while keeping f_s, increases the SNR but decreases the transmitter bandwidth. Thus, improving both the SNR and bandwidth relies on the increase of the f_s of the modulator. Considering this, the use of parallel approaches has been used to process multiple samples in parallel. Parallel architectures make possible the design of considerable higher bandwidth transmitters working at reduced logic frequencies for most of the design and the competitive integration with lower-cost technologies, but, nonetheless, they rely on the use of dedicated high speed logic at the output to guarantee the data throughput. One of the possible approaches is the use of time-interleaved DSM as proposed in [11]. However, as discussed in the same work, this approach still has some scalability problems that limit the sampling frequency increase, being 1 Gsps the maximum frequency achieved in [11] (for a 1st and 2nd order modulator).

In a different approach [10], using multiple parallel DSM cores and combining their outputs in time, it was presented a modulator with a f_s of 3.2 Gsps while maintaining a logic clock of 200 MHz. Using this approach, it was possible to transmit a signal with over 120 MHz bandwidth, as presented in Fig. 2(b), highly improving the state-of-the-art in terms of bandwidth for these systems.

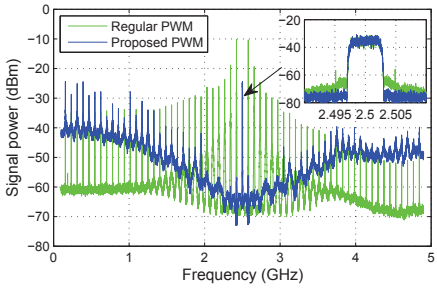

Fig. 3: Comparison between the spectrum obtained with the regular PWM and with the proposed method in [12].

C. Flexibility

A key ADTx limitation is the quantization noise introduced by most of ADTxs, due to the modulation techniques used

to encode the signal into pulsed representations. While DSM applies noise shaping to reduce the quantization noise near the carrier, the filter complexity limits its sampling frequency [13]. On the other hand, PWM logic is fairly easier to design and implement at higher rates, but introduces high power harmonic noise peaks close to the carrier frequency. In both cases, analog narrow band filters must be used to attenuate the out-of-band quantization noise. The introduction of an analog filter reduces the flexibility of the ADTx by binding the transmitter output to the filter central frequency and bandwidth. A fixed analog output filter removes the possibility for multi-band and multi-carrier transmission without hardware replication. In this sense, improving noise shaping techniques to allow simultaneous multiple carriers and shape the quantization noise to other frequency ranges becomes highly important.

Improving noise shaping techniques have already been presented to improve the flexibility of the transmitter. Concurrent multi-band DSM was used in [14] to achieve a compact and flexible multi-band transmitter implementation. A similar approach in [15] uses a bandpass DSM to design a dual-band transmitter. The re-distribution of the harmonic distortion near the transmitted carrier for PWM was also presented in [16]. The used technique shapes the ADTx's quantization noise by changing the PWM waveform patterns, avoiding the need for a high quality factor analog output filter (presented in Fig. 3), and reducing the power of the first PWM harmonic, by more than 50 dB.

III. All-Digital Receivers

At the receiver side, to achieve flexibility and wider bandwidth in the RF chain, the ADC is of paramount importance, by allowing the use of digital signal processing techniques and avoiding analog impairments. Therefore, the main idea of an All-Digital Receiver (ADRx) is to put the analog-to-digital conversion stage as close as possible to the antenna, to provide not only flexibility but also high levels of circuit integration and scalability.

Currently commercial available RF ADCs are capable to reach a few GHz of both bandwidth and sampling rate, however they are quite expensive and present a high level of energy consumption. Recently, new alternatives are arising based on pulse shaping modulations such as DSM [17] or PWM [18], [19]. The DSM ADCs are widely used in low-frequency applications by providing high resolution. Nevertheless, some recent work is bringing these ADCs to the RF domain, as presented in [17]. Even though the good resolution that has been obtained in [17], the bandwidth is low and the need for a low latency feedback path impose limitations in terms of increasing the sampling frequency. The latter aspect makes these architectures more suitable to IC design rather than FPGA-based implementation, however this is still an open research topic in this field. On the other hand, the PWM ADCs are basically made of a comparator, whose inputs are an analog signal and a reference, generating a PWM representation of the analog signal. Despite being commonly used in low-frequency applications [20], recently they are also being implemented in RF domain [18], [19], mainly either using IC-based or FPGA-based implementations as proofs of concept. The latter will be the focus of the next sub-section.

A. Initial Work on All-Digital Receivers

Following the diagram of Fig. 1, and focusing on RF receiver section, one can verify that after the antenna, there is a circulator to isolate the transmitter from the receiver path, a filter to select the interest band, and then, a low noise variable gain amplifier (LNA/VGA). Afterwards, there is a comparator, in which one of the inputs is used for the RF signal and the other one for a reference signal ($r(t)$), which is usually a triangular or a sawtooth waveform, due to its uniform amplitude distribution. At this point both signals should present similar peak-to-peak amplitude, which is guaranteed by the LNA/VGA stage. Additionally, the $r(t)$ signal frequency is related with the maximum acquisition bandwidth, and this should be at least two times higher than the analog signals bandwidth. At the comparator's output, a natural sampling PWM waveform is generated, which is then sampled at a rate of f_s creating a uniform sampling PWM signal, containing the RF signals information. Although the simplicity of this architecture, its detailed analysis is not trivial, since the PWM generation creates out-of-band harmonic content that may fold in the interest band after sampling, if an incorrect dimensioning of the $r(t)$ waveform is performed. Thus, the $r(t)$ waveform must be carefully designed depending on the f_s, bandwidth and carrier frequency to be sampled. An alternative way to address the sampling circuit can be explained by means of statistical quantization theory in [21], which falls out the scope of this paper. Therefore, and focusing on the RF scenario, in [18] the idea of PWM-based RF receivers was presented for the first time. In the same work, high speed comparators were used to generate the PWM signal and then, the high speed inputs of an FPGA were used to acquire the PWM signal. However, the authors do not provided much details about the working principle of the RF PWM ADC process, being simply presented as a modulator. Additionally, the use of external comparators may increase the systems cost and compromise the integration as also the scalability.

B. FPGA Integration of All-Digital Receivers

In [19], a step towards the integration was achieved by being capable to use the FPGA high speed differential inputs as comparators, showing that external ones are not required. Additionally, the system proposed in [19] presents an analog input bandwidth of almost 3 GHz and reasonable EVM for 2 MHz and 4 MHz signals. Moreover, this immediately allows to design a highly scalable solution with a high degree of integration.

IV. On-going Work and Trends

Regarding current challenges, the bandwidth increase can be considered as one of the most important ones, by studying how such a system can support higher bandwidths while maintaining reasonable Figures of Merits (FoMs). At the same time, the carrier frequency increase to mmWave bands, also represents a major challenge for these architectures.

The potential of the ADTxRx has also been widespread for other scenarios, such as the Radio-over-Fiber (RoF) architectures. The current trend in RAN architectures is to move the baseband processing to the cloud to achieve centralized signal processing and management. Centralized Radio Access Network (C-RAN) paradigm is an example of these new cellular network architectures, where several distributed

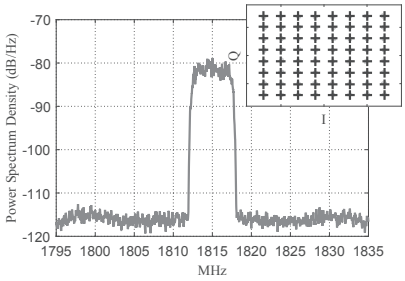

Fig. 4: RF spectrum and constellation of a 5 MHz 64-QAM modulated signal centered at 1815 MHz (adapted from [22]).

Remote Radio Heads (RRHs) are connected to a central or Baseband Unit (BBU). The connection between the RRHs and the BBU is typically supported by an optical infrastructure. Digitized RoF techniques have been proposed to surpass the common RoF limitations by using digital optical links. Instead of analog modulation, digital samples are sent over the fiber and converted with a DAC at the RRH. However, this type of solution may increase substantially the complexity at the RRH side, resulting in a relatively costly radio head. In [12], an all-digital architecture for RoF downlink scenarios was proposed and experimentally validated, resulting in very simple RRHs comprised only by amplification, filtering and air interface. Additionally, the uplink scenario was addressed in [22], where a low-cost and scalable RRH architecture was proposed. Fig. 4 depicts the spectrum and a constellation of a 5 MHz 64-QAM signal acquired at 1815 MHz (with an EVM of 1.43%), using the latter system.

A block diagram illustrating the integration of both the downlink and uplink architectures with the concept of ADTxRx is depicted in Fig. 5. In the same figure, the modules "E-O" and "O-E" refer to the conversion between the electrical and optical domains.

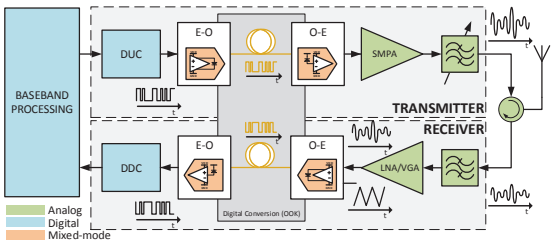

Fig. 5: Application of the ADTxRx concept to RoF scenarios.

V. Conclusion

This paper presented the state-of-the art on ADTxRx, including the proposed techniques and architectures to improve key FoMs. The FPGA capabilities, in terms of parallel processing, I/O speeds and development tools, allow designing and fast prototyping of flexible RF transceivers for next generation wireless communication systems.

Acknowledgment

This work is funded by National Funds through FCT - Fundação para a Ciência e a Tecnologia under the project PEst-OE/EEI/LA0008/2013, UID/EEA/50008/2013, the PhD (SFRH/BD/92746/2013) grant given to the first author, the PhD (SFRH/BD/91533/2012) grant given to the second author and the PhD (PD/BD/105857/2014) grant given to the third author.

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Paper C6: All-digital Flexible Uplink Remote Radio Head for C-RAN

[C6] - A. Prata, A. S. R. Oliveira, and N. B. Carvalho, “All-digital Flexible Uplink Remote Radio Head for C-RAN,” in 2016 IEEE MTT-S International Microwave Symposium, IMS 2016, 2016, pp. 1–4.

All-digital Flexible Uplink Remote Radio Head for C-RAN

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Abstract — The Centralized-Radio Access Networks (C-RAN) are one of the current trends for the next generation mobile standards. The main concept of C-RAN is the separation of the baseband processing and management tasks from the radio access units. This paper presents an all-digital, simple and flexible RF uplink section for a C-RAN Remote Radio Head (RRH). The implemented system presents an analog input bandwidth of about 3GHz, being capable to receive any signal up to 5MHz symbol rate while maintaining the current LTE Error Vector Magnitude (EVM) requirements.

Index Terms — Remote Radio Head (RRH), Centralized-Radio Access Network (C-RAN), Software Defined Radio (SDR), Pulse-Width Modulation (PWM).

I. INTRODUCTION

The number of mobile network users and the traffic is growing, leading to successive generations of standards with higher throughput and mobility support. This increasing is imposing high requirements to the radio access network (RAN), such as, energy efficiency, bandwidth, flexibility, Quality of Service (QoS), manageability, upgradability and cost. Next generation mobile communication standard, the so-called 5G, must efficiently answer to these requirements. Therefore many new ideas are being discussed and some are already in early-development stage by the academia and industry, such as Massive MIMO, mm-Wave exploitation, small/pico-cell deployment, SDR/CR circuit design and Centralized/Cloud/Cooperative/Clean-Radio Access Network (C-RAN) [1, 2]. The two latter topics are the main focus of this paper.

The main concept of C-RAN is the centralization of the signal processing and management tasks, removing them from the radio access units [2] (Fig. 1). Briefly, this new architecture is based on the following three components: a) a pool of central units (CUs) that are responsible for the management and signal processing; b) a set of distributed Remote Radio Heads (RRHs); c) a high-bandwidth and low-latency optical or microwave transport layer (fronthaul) between the CU and the RRHs. This centralized architecture would bring efficient interference management between RRHs, spectral efficiency, flexibility and support of high data rates [2]. In order, to take the highest profit of the C-RAN paradigm, the RRH should ideally present a simple, low power and low cost architecture.

Actually, this topic related with the RRH is already being addressed by the scientific community. In [3] an all-digital transmitter architecture using delta-sigma modulation (DSM) or Pulse Width Modulation (PWM) based on digital-radio over fiber (D-RoF) with a simple RRH was presented, answering the previous requirements for the RRH downlink section.

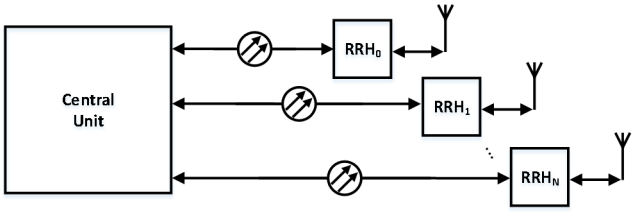

Fig. 1. C-RAN block diagram scheme composed by a CU connected to several RRHs through an optical transport layer (fronthaul).

Additionally, in [4] an entire base station system was presented with a transmitter section similar to [3], and with a receiver chain also based on PWM but without taking full profit of the PWM representation of the analog signal, due to the unnecessary use of conventional analog down-conversion architecture in the CU. In fact, following a topology as presented in [4] there are several serious issues regarding the system performance and cost that will be properly addressed and improved in this work.

In this paper, a simple, low-power, low-cost RRH with high analog input bandwidth, which is suitable and highly scalable to a scenario of a CU connected to multiple spread RRHs is presented and evaluated. This RRH is made by an antenna, filters, low noise amplifier (LNA) with variable gain amplification (VGA) and an electro/optical (E/O) converter based on a small form-factor pluggable (SFP) device. The analog-to-digital conversion (ADC) is implemented directly at the Radio Frequency (RF) stage based on PWM, taking profit of the close interaction between an SFP and a Field Programmable Gate Array (FPGA) at the CU. In comparison to [4], the approach proposed in this work has several advantages, namely:

- Simpler and lower cost RRH implementation;
- Scalability, since a single FPGA can handle multiple RRHs;
- Improved performance and flexibility due to FPGA-based all-digital processing.

The remainder of this paper is divided as follows. In Section II the state of the art of RF PWM-based ADCs is briefly addressed. Sections III and IV present the proposed system

and experimental results for the receiver part of a C-RAN scheme. Finally, Section V draws the conclusion of this work.

II. RF PWM ADCs State Of The Art

An RF-PWM ADC is made of a single comparator as presented in Fig. 2, where one of its inputs is used for the RF signal (x(t)) and the other for a reference signal (r(t)), which is usually a triangular or sawtooth wave. At the output of the comparator a PWM representation of the x(t) signal will appear (p(t)).

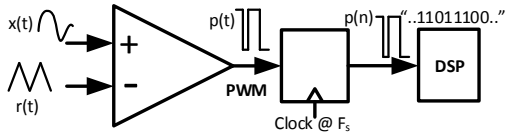

Fig. 2. PWM ADC block diagram.

Following the comparator there is a one bit register that will sample the p(t) signal at a rate of Fs, generating a discrete time representation of x(t), p(n). Despite its architecture being simple, its analysis is not trivial, since the PWM generation creates out-of-band non-linear distortion that may fold in the interest band after sampling, if an incorrect dimensioning of the r(t) waveform is performed. Therefore, the r(t) waveform must be carefully designed depending on the sampling frequency (Fs), bandwidth and carrier frequency to sample.

This type of converters had its origin in the 1960's [5]. The circuit sampling behavior can be explained by means of statistical quantization theory. Following this theory it can be demonstrated that the r(t) signal frequency is related to the maximum acquisition bandwidth and the amplitude of the r(t) must be equal to the signal to sample (x(t)) [5, 6]. Additionally, to equally sample the x(t) signal, the r(t) must present an uniform amplitude distribution, which is the reason for the use of a triangular or sawtooth waveform [5, 6]. However, in that time due to the lack of technology the idea was left and sigma-delta ADCs were preferred.

Even though these type of converts are commonly used in low-frequency applications, recently they are also being used in RF receiver's design [7, 8]. In [7] high speed comparators to generate the PWM representation were used followed by an FPGA to gather the signal. In [8] the high speed inputs of a single FPGA-chip are used to build the ADC and the remaining receiver, presenting a flexible and integrated architecture.

III. Proposed Receiver Chain for C-RAN

The proposed receiver architecture for a C-RAN scenario is presented in Fig. 3 a), and is divided into three main blocks: an RRH, an optical transport layer and the CU.

Following the diagram of Fig. 3 a), it is possible to observe that after the antenna, the RRH begins with a bandpass filter responsible to select the bands to receive, followed by an LNA/VGA that performs low noise adaptive gain in order to put the signal level accordingly with the reference waveform (r(t)). Since the SFP laser driver presents a high bandwidth differential input, these inputs are used as a comparator. Therefore, both the RF signal x(t) and the reference signal (r(t)) feed the SFP inputs, which will generate a PWM representation of x(t) that will drive the optical laser. Then, the optical fiber will carry a two-level optical signal containing the RF signal information. The transport layer is connected to the CU that will receive the optical signal with other SFP receiver made of a photo diode, which is responsible to convert the optical signal back to the electrical domain (p(t)).

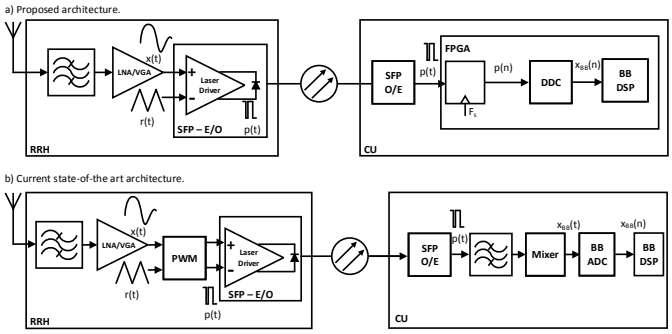

Fig. 3. Comparison between the proposed receiver architecture (a) and the current state-of-the-art architecture (b) from [4].

The p(t) signal is acquired by the high speed inputs of an FPGA-chip, which will sample the signal at a given sampling rate (Fs). After sampling, the signal must now be processed by a digital down conversion (DDC) in order to recover the signal's complex envelope. The receiver chain ends with the signal's demodulation stage.

Considering such a system, it is important to address its scalability. In fact, by using a single FPGA-chip for the CU it enables the possibility to have several simultaneous RRHs, being possible to take profit of its powerful parallel digital signal processing capabilities to implement all the signal processing from RF to the baseband protocol stage. Additionally, by using simultaneous different wavelengths at the fiber path (Wavelength Division Multiplexing) the scalability could also be improved or it could enable a multi RF carrier scenario.

Finally, the proposed system (Fig. 3a)) can now be compared to the system presented in [4] (Fig. 3 b)), where it is obvious the gains in terms of the system cost, scalability, simplicity and agility due to the all-digital approach.

IV. Implemented System and Measurement Results

In order to evaluate the proposed system a laboratorial measurement setup was assembled as shown in Fig. 4. An Arbitrary Waveform Generator (AWG) (AWG7002A from Tektronix) was used to generate both the RF and reference signals. These signals are directly connected to the RRH SFP (AFBR-709SMZ from Avago). Since this is a laboratorial prototype the antenna and LNA/VGA were not included in the

RRH. Then an optical fiber connects the RRH to the CU. The CU, which contains an SFP equal to the RRH, was built using a KC705 Xilinx FPGA development board.

The evaluation measurement focus on the system's response to a real RF modulated signal x(t). Thus, a signal with a given fixed power, modulation and bandwidth was generated, and its carrier frequency was swept. The signal was acquired at the CU and sent to a local PC running a Matlab routine, which is responsible to evaluate the signal's EVM. The EVM is the metric selected to evaluate the system performance, since it is related with the Signal-to-Noise Ratio (SNR). Fig. 5 presents the first measured carrier frequency sweep from 315MHz up to 3.065GHz with a step of 25MHz, for a 2MHz symbol rate signal with 16-QAM and 64-QAM modulation schemes. It is possible to observe that the system is able to maintain an EVM_{rms} between 0.79% and 3.45%. Fig. 6 presents the second measured carrier frequency sweep with the same characteristics than the previous but using a 5MHz symbol rate signal. For a 5MHz signal the EVM_{rms} is always above 1.15% and below 4.05%. Considering the EVM minimum requirements for the LTE standard presented in [9], it can be verified that the system is able to meet the required specifications.

Fig. 7 presents the RF signal spectrum of an acquired 64-QAM 5MHz signal centered at 1815MHz and also the signal's constellation diagram.

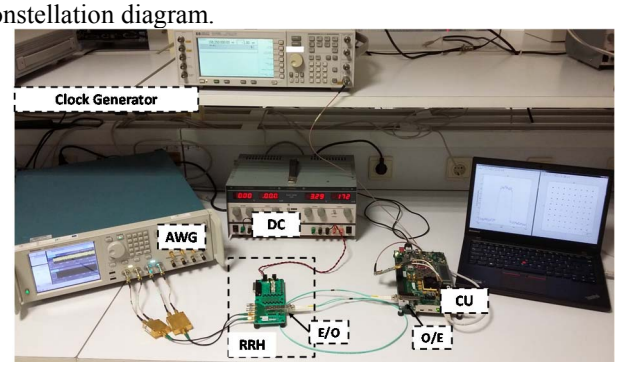

Fig. 4. Photo of the implemented and measurement setup.

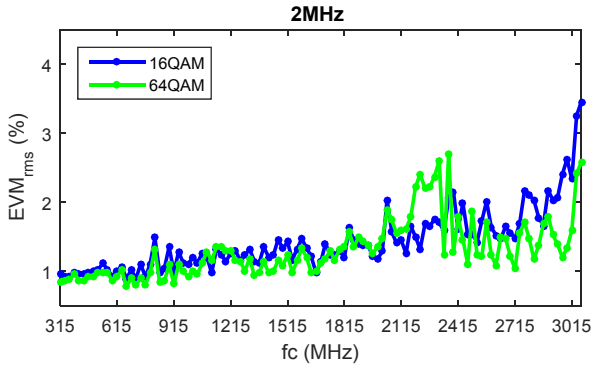

Fig. 5. Carrier frequency sweep for a 2MHz symbol rate signal.

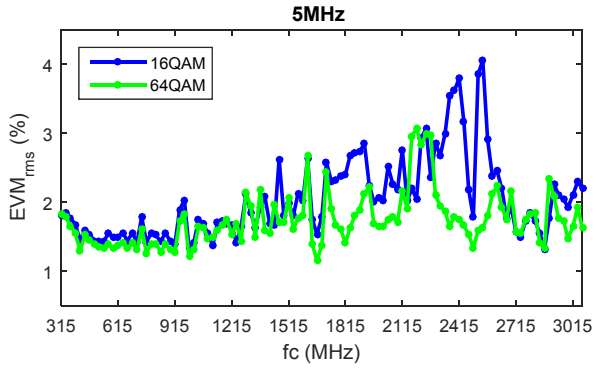

Fig. 6. Carrier frequency sweep for a 5MHz symbol rate signal.

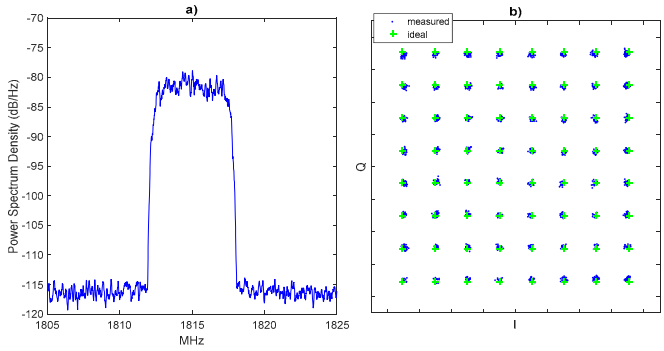

Fig. 7. Acquisition of a 5MHz 64-QAM modulated signal at centered at 1815MHz. a) Frequency domain representation; b) Constellation diagram with EVM_{rms} = 1.43%, which corresponds to an SNR of 36.9 dB.

V. Conclusion

In this paper a simple and flexible RRH suitable for C-RAN architectures was presented and evaluated. Using such an architecture the processing task is completely integrated at the CU, leaving the RRH completely agnostic to the type of signal to receive, which is important for system upgradeability and durability among the evolution towards future protocol standards. The measurement results shown that the proposed RRH is able to operate in almost 3GHz of bandwidth being capable to receive signals up to 5MHz of symbol rate maintaining a reasonable EVM, i.e., obeying the requirements of the current LTE standard [9].

Acknowledgement

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Paper J2: Agile All-Digital RF Transceiver Implemented in FPGA

[J2] - R. F. Cordeiro, A. Prata, A. S. R. Oliveira, J. M. N. Vieira, N. B. Carvalho, “Agile All-Digital RF Transceiver Implemented in FPGA,” in IEEE Trans. Microw. Theory Techn., vol. x, no. x, pp. 1–12, 2017.

Agile All-Digital RF Transceiver Implemented in FPGA

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***Abstract*— This paper presents a new all-digital transceiver architecture fully integrated into a single field-programmable gate array chip. Both the radio frequency (RF) receiver and the transmitter were entirely implemented using a digital datapath from the baseband up to the RF stage without the use of conventional analog-to-digital converter, digital-to-analog converter, or analog mixer. The transmitter chain uses delta–sigma modulation and digital upconversion to produce a two-level RF output signal. The receiver uses a high-speed comparator and pulsewidth modulation to convert the RF signal into a single-bit data stream, which is digitally filtered and then downconverted. Both the transmitter and the receiver are agile with flexible carrier frequency, bandwidth, and modulation capabilities. The transceiver error vector magnitude and the signal-to-noise ratio figures of merit were analyzed in a point-to-point transmission to evaluate the transmitter's performance. The results show the feasibility of this approach as a more flexible alternative to common radio architectures.**

***Index Terms*— All-digital transceivers, delta–sigma modulation (DSM), pulsewidth modulation (PWM), software-defined radio (SDR).**

I. Introduction

IN THE last two decades, mobile wireless communications have witnessed a phenomenal growth in terms of users, mobile terminals, and throughput requirements to drive multimedia and video services. This has led to successive generations of mobile cellular standards from the highly successful 2G networks (GSM), going through the 3G (HSPA), and up the current 4G (LTE). During the next decade, this trend will continue, due to the proliferation of personal communication devices and the Internet of Things phenomena. This will spread machine-to-machine communications by embracing billions of constantly connected devices and seeking the integration of different standards to provide ubiquitous high-rate and low-latency experience [1].

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Therefore, 5G must be capable to efficiently answer the new communication challenges and, at the same time, act as an integrator over the previous standards. A number of new ideas and concepts are being suggested and evaluated by the industry and academia for 5G support technologies, such as massive MIMO, exploitation of higher radio frequency (RF) bands, such as millimeter wave range, and centralized radio access networks for highly digital radio access networks [1], [2]. Nonetheless, the increasing use of new wireless standards using different frequencies, diverse coding and modulation schemes, and targeting various applications is already taking place. The need for cooperation between access points and devices in the network using different heterogeneous technologies will be essential to support the required flexibility and spectral efficiency for 5G networks.

Ultimately, 5G and all networks beyond will be extremely dense, flexible, and heterogeneous, which introduces many new challenges for network modeling, analysis, design, and optimization. The core network will also have to reach unprecedented levels of flexibility. Spectrum regulation will need to be rethought, and energy and cost efficiencies will become even more critical [2]. Furthermore, there will be an increasing trend to digitalization motivated by the flexibility and high performance allowed by the cognitive radio and software-defined radio (SDR) approaches, where mixed-signal and all digital systems will have a rising importance in the design of radio and telecommunication systems. The all-digital transceivers will be the focus of this paper due to their improved flexibility permitted by the completely digital signal processing up to the RF stage.

In this paper, a new all-digital RF transceiver architecture, fully integrated into a single field-programmable gate array (FPGA) chip, will be presented and evaluated. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. In this sense, the proposed system does not use conventional analog-to-digital (ADC) and digital-to-analog converters neither any kind of analog mixing device, enabling the creation of a much more compact and integrated radio. To the best of our knowledge, this is the first time a fully integrated all-digital RF transceiver architecture is presented.

This paper is organized as follows. In Section II, the state of the art of SDR transceiver architectures is presented. Section III presents the proposed transmitter and receiver architectures and their hardware implementation. To validate

the proposed system, the measurement results of error vector magnitude (EVM) and signal-to-noise ratio (SNR) will be presented and discussed in Section IV. Finally, some conclusions are drawn in Section V.

II. State of the Art

SDR transceiver architectures will be fundamental in the future radio communication systems in order to endow the physical layer with high flexibility, spectral, and energy efficiency [3]. Therefore, this section addresses the state of the art on SDR transceivers focusing on all-digital platforms, due to the enormous advantages that such architectures can provide.

A. Transmitters

All-digital transmitter architectures typically use pulsed-modulation approaches to allow the full digitalization of the radio system, which poses an important step toward the complete software description of RF signals proposed in SDR.

Recent advances involving pulsed-RF transmitters include the development of novel all-digital transmitter architectures, where the radio datapath is digital from the baseband up to the RF stage. These transmitters perform a conversion from an m-bit digital representation to a two-level signal, usually done by means of the delta–sigma modulation (DSM) or pulsewidth modulation (PWM) schemes. The state-of-the-art pulsed transmitters can use amplitude and phase modulation of the RF carrier using PWM [4]–[7], bandpass DSM [8], [9], or low-pass DSM with digital upconversion (DUC) [10]–[14]. To improve signal quality, many works have focused into the increase of the signal oversampling ratio (OSR). Most of pulsed-RF transmitters achieve higher OSR by optimizing the digital design for a higher frequency [15]. However, digital switching logic has frequency limits that bound the achievable OSR to a maximum value depending on the used technology. An alternative approach for higher OSR is to use parallelized processing followed by dedicated high-speed logic, such as a multiplexer or a serializer [16]–[18]. This eases the design of higher bandwidth transmitters working at reduced logic frequencies and the competitive integration with lower cost technologies.

The functionality and the flexibility of the transmitter are also of great importance, since the purpose of a digitally controlled transmitter is to easily adapt the radio to its environment and user needs. Carrier frequency flexibility means that a single digital chip can be a wideband radio with multiple channels and standards. In this paper, we present a transmitter capable of covering signal bands from 400 MHz to 2.4 GHz.

B. Receivers

Traditional RF receivers are commonly based on homodyne or heterodyne architectures, usually performing analog down-conversion up to the baseband or up to an IF stage, where the signal is sampled by an I/Q (ADC) or by an IF ADC. These architectures present a high dependence on analog components imposing problems, such as limited bandwidth, due to the analog components frequency response. Alternatively, the IF ADC can be replaced by an RF ADC, allowing sampling the spectrum directly at the RF stage and, therefore, performing the entire signal processing in the digital domain, as it was envisioned as the ideal SDR receiver [3] (Fig. 1). These architectures present high flexibility and high bandwidth and allow taking profit of the high efficient and accurate digital signal processing techniques, avoiding the analog impairments and mismatches [19].

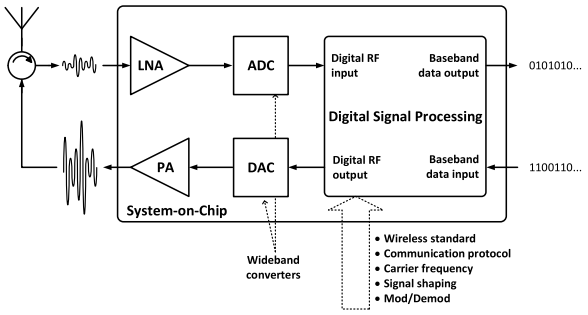


Fig. 1. Ideal SDR transceiver architecture.

Modern SDR receiver performance and flexibility is susceptible to the ADC's bandwidth as well as its linearity. Current commercial RF ADCs have reached a few gigahertz of sampling frequency and analog input bandwidth. However, they are expensive and have a significant energy consumption, which may reduce the overall systems efficiency.

Recently, new possibilities to build RF ADCs based on pulsed-modulation converters were proposed, such as, DSM [20], pulse frequency modulation (PFM) [21], [22], or PWM [23], [24]. All these types of ADCs are single-bit ADCs, i.e., all deal with a digital pulsed representation of the analog signal. The DSM ADCs are often used in audio applications, due to their high resolution that they provide [19]. Several research works presented RF DSM ADCs, such as [20] where a high resolution ADC was built, however with low analog input bandwidth. A PFM ADC is based on a voltage-controlled oscillator (VCO) to create a PFM representation of the input analog signal [21]. These types of ADCs present high undesirable nonlinear behavior related to the VCO that may be improved using techniques as the ones presented in [22]. A PWM ADC is made of a single comparator, whose inputs are the analog signal and a given reference wave (usually a triangular wave), generating a PWM representation of the analog signal [25]. They are commonly used in low-frequency applications [25]; nevertheless, they are also being applied in the RF world, as presented in [23] and [24]. In [23], high-speed comparators to generate the PWM representation are used, and in [24], a single FPGA-chip is used to build the ADC and the remaining receiver, presenting a flexible and promising architecture. However, none of these works present an exact way to obtain the best reference waveform to optimize the receiver figures of merit. In this paper, we present an algorithm that optimizes the frequency of a reference triangular wave in order improve the receiver performance.

III. Proposed Architecture

This section presents and explains the proposed architecture for the all-digital transceiver. For the sake of clarity,

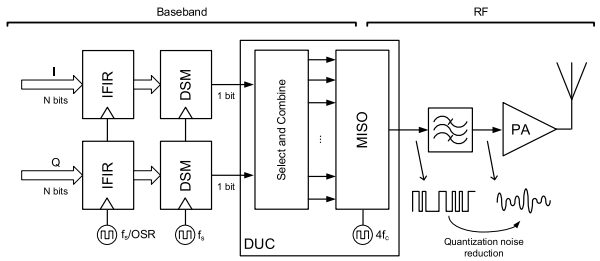


Fig. 2. DSM-based ADT architecture. Baseband delta–sigma clock frequency is f_s, while the DUC works at a four times the carrier frequency f_c.

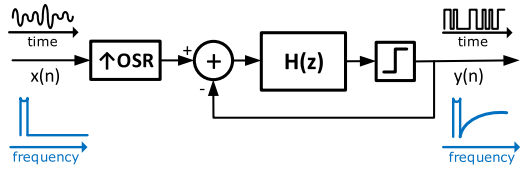


Fig. 3. DSM loop with loop filter $H(z)$.

the transmitter and receiver architectures will be presented separately, but implemented and tested together.

A. Proposed Transmitter Architecture

This section presents and explains the proposed architecture for the all-digital transmitter. The digital transmitter architecture used is shown in Fig. 2. The baseband complex signal is divided into two components, the in-phase (I) and quadrature (Q) signals. It should be noted that for the purpose of this paper, no particular protocol or standard is considered, i.e., the digital baseband processing can be performed as in conventional transmitter architectures, for any particular standard use.

The proposed architecture uses DSM with a two-level output. The delta–sigma modulator, as shown in Fig. 3, is a signal shaping stage of the modulator, which converts the I and Q signals with N bits resolution, into single-bit representation signals, at the tradeoff a higher resolution in time. The signal is initially upsampled to improve the OSR using a digital interpolation filter. The filter inside the delta–sigma loop shapes the quantization noise inserted by the 1-b quantizer at the output by feeding back the error signal. The output of the modulator is a binary signal with added out-of-band quantization noise.

The DSM loop filter will define the transmitted signal resolution and consequent signal quality in terms of SNR. Higher order DSM allows higher noise rejection for the signals band at the same OSR. However, the higher in-band noise rejection increases the noise in the adjacent bands. In [26], an extensive study was made on the influence of the DSM's order on the signal to quantization noise ratio (SQNR). An approximation of the SQNR value given by (1) and equivalent signal resolution in number of bits is shown in Fig. 4 for a first-, second-, and third-order DSMs. In the presented equation, OSR is the oversampling ratio and L is the DSM order. Higher DSM orders require lower values of OSR to achieve the same performance when compared with lower DSM orders, and

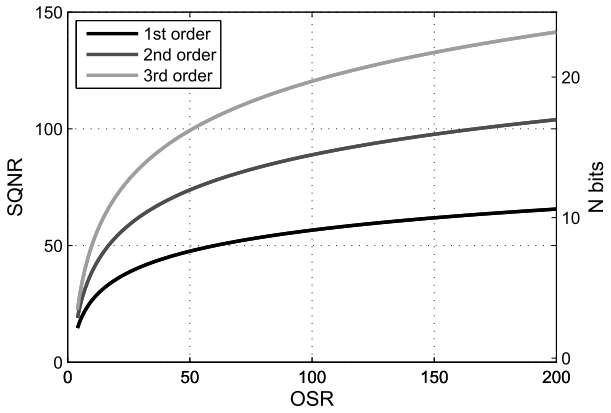


Fig. 4. SQNR and effective number of bits for two-level DSM with different orders of modulation.

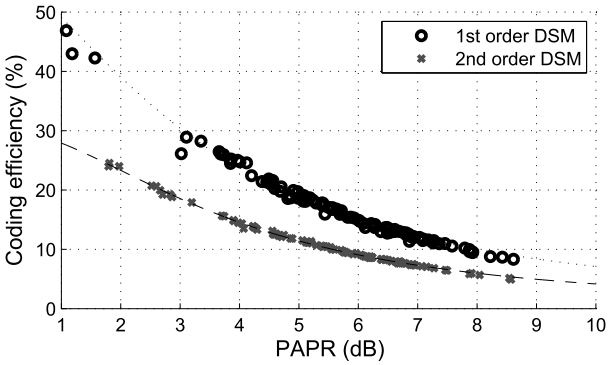


Fig. 5. CE variation with input signal for the first- and second-order DSM. The measured PAPR and CE values are from random phase and amplitude multisine signals.

therefore, lower sampling frequencies could be used. Hence, it should be desirable to use a higher order modulator to improve the transmitter SNR

$$\mathrm{SQNR_{dB}} = 3.01 \times \log_2(\mathrm{OSR}) \times (2L+1) - 9.36L - 2.76. \tag{1}$$

In RF applications, this becomes a problem, since additional out-of-band noise reduces the transmitter efficiency. The relationship between in-band power and total transmitted power is the modulator coding efficiency (CE). It can be defined as the signal channels power P_s over the total transmitted power P_t [27], as it is shown in

$$\mathrm{CE} = \frac{P_s}{P_t}. \tag{2}$$

The CE of DSM varies subject to the nature of the input signal, particularly its peak-to-average power ratio (PAPR), and is typically lower than 30%. However, higher orders of modulation will decrease even further the CE of the transmitter. Fig. 5 shows a representative graph of CE measurements for an all-digital transmitter with both the first-order and the second-order modulators for different PAPR signals. It is perceptible that for common wireless communication standards with PAPR varying from 3 dB up to 12 dB, the CE is considerably low, especially for higher order modulators.

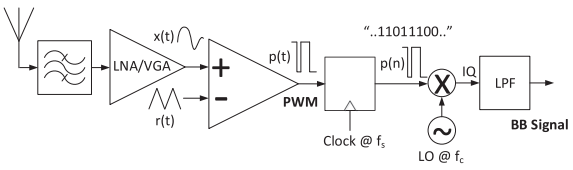


Fig. 6. PWM-based all-digital receiver architecture.

Since higher order DSM limits the transmitters CE, increasing the modulators order is not a satisfactory solution to improve the signal SNR. A possible alternative is to increase the OSR of the modulator by increasing its operation speed. However, a key limitation in digital DSM is the typically low bandwidth of the signal modulator due to frequency restrictions for the digital logic clock because of the loop-filter propagation delays. To overcome this, it was used a time-interleaved DSM to improve the maximum modulator sampling frequency. This parallel DSM architecture used was initially presented in [18] to improve the modulator OSR by allowing the processing of multiple parallel delta–sigma samples in a single clock period.

The DSM used is a first-order modulator, because it has a higher CE for the transmitted signal. In addition, a simpler loop filter can be implemented with fewer logic elements. Less logic gates allow for a smaller logic delay path and, therefore, a higher sampling rate and signal bandwidth.

The DUC is achieved by time interleaving the delta–sigma modulated two-level samples (I and Q) in time with their inverted versions. The resulting wave, w in (3), is equivalent to the multiplication of I and Q baseband components with two square waves with a 90° phase shift between them. To do this, a parallel to series block with a switching frequency four times superior to the desired carrier frequency f_c can be used

$$w = [I;\, Q;\, \overline{I};\, \overline{Q}]. \tag{3}$$

The resulting output signal has the baseband complex signal upconverted to f_c with added quantization noise in the sidebands added by the DSM. This noise can be filtered and the RF signal recovered.

B. Proposed Receiver Architecture

In this section, the receiver architecture will be presented and explained, considering a PWM-based topology, which was chosen mainly due to the high analog input bandwidth and flexibility that such topology can provide.

The generic block diagram architecture for the proposed receiver is shown in Fig. 6, where the signal $x(t)$ represents the RF signal, centered at f_c with bandwidth BW, received at the antenna after filtering and low noise variable gain amplification (LNA/VGA). The $x(t)$ signal is one of the inputs of a comparator, while the other is a reference signal $[r(t)]$, of frequency f_r, which is usually a triangular wave. At the output of this comparator, there is a continuous time PWM signal $p(t)$ that contains the information of the $x(t)$ signal. The $p(t)$ signal is a natural sampling PWM representation of $x(t)$ [28], which implies that no quantization noise is added into the signal's band. Following the comparator, there is a single-bit register responsible to sample and discretize the continuous time PWM signal $p(t)$, at a sampling rate of f_s, with ($f_s > 2f_c$ and $f_s \gg$ BW). Thereafter, the signal is available for further processing regarding digital downconversion and filtering in order to recover the baseband signals information.

The analog-to-digital conversion stage, which is the key element of this receiver, as any other converter can be separated in two processes; sampling and quantization, which are related to discretization in both time and amplitude, respectively. The proposed way to implement the conversion (PWM) is similar to the stochastic ergodic converter presented in [29], which was a popular idea in the 1960s to build low-cost and low-frequency ADCs. However, at the time, due to the lack of enabling technology, the idea was abandoned and sigma–delta converters were preferred [29]. This converter is mainly based on adding a dithering wave to an analog signal and then feeding it to a single-bit quantizer. The theoretical demonstration of this converter can be developed based on the statistical quantization theory, which shows that if the dithering signal presents uniform distribution, the input signal will be equally quantized, i.e., the mean of the input signal will be contained in the output quantized signal, allowing its recovering. A common selection for the dithering wave is a triangular or sawtooth wave, since both present uniform amplitude distributions [29], [30]. This dithering wave can be directly transposed for the PWM RF ADC, playing the same role as the reference signal $r(t)$, which should also present uniform amplitude distribution.

In addition to the reference signal amplitude distribution, two other important characteristics are the reference frequency and the sampling frequency of the sampler after the comparator, which define the maximum bandwidth of the signal to acquire. The latter two variables will also impose the converters resolution, since the ratio between the effective sampling frequency (f_s) and the reference signal frequency (f_r) indicates the number of PWM levels and, therefore, the number of bits of the converter (4) and its SNR (5), as follows:

$$N_{\text{bits}} = \log_2(N_{\text{levels}}) = \log_2 \frac{f_s}{f_r} \tag{4}$$

$$\text{SNR} = 6.02N_{\text{bits}} + 1.76. \tag{5}$$

The previous relationships indicate that the higher the ratio between the sampling frequency and the reference signal, the higher will be the converter effective resolution. Therefore, we may consider that the limit for f_s will be imposed by the maximum frequency allowed by a given technological process or by a set of requirements, such as resolution or power consumptions of a certain application. Nonetheless and without loss of generality, in order to simplify the digital architecture and to provide the maximum resolution, f_s should be fixed to the maximum achievable value and maintaining the previous assumptions $f_s > 2f_c$ and $f_s \gg$ BW. Thereafter, considering an analog signal occupying a given bandwidth (BW), it is important to select the minimum reference signal frequency to provide the higher resolution, while a selection of a minimum

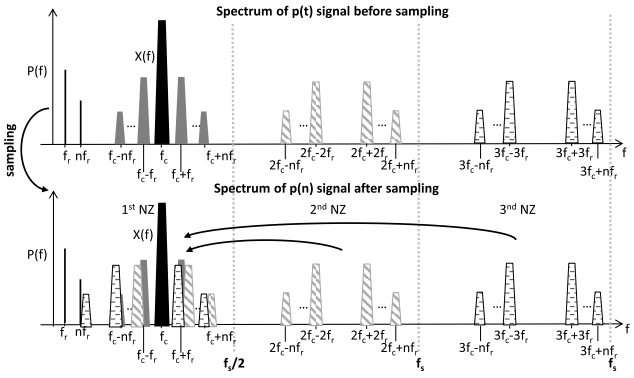


Fig. 7. Conceptual representation of the PWM signal spectrum, in the first three NZs, before and after sampling.

reference frequency, f_r, of 2 BW for a sawtooth waveform or of BW for a triangular waveform allows achieving the same resolution, and it creates a different harmonic content in the PWM spectrum. The sawtooth wave puts the first distortion band closer to the interest band, making the triangular wave a preferable way to acquire the signal and to provide a relaxation of the filtering requirements in the digital downconvert (DDC) chain.

At the register's input, ideally, there is a perfect square wave with varying duty cycle of infinitesimal resolution, which presents an infinite power spectrum, as shown in spectrum before sampling in Fig. 7. Then, the single-bit register running at f_s samples the continuous time $p(t)$ waveform, generating a discrete-time $p(n)$ PWM waveform. As already mentioned, the relation $f_s > 2f_c$ imposes the signal of interest $x(t)$ to be in the first Nyquist zone (NZ). However, the sampling process causes a frequency overlap at the first NZ due to the aliasing of PWM harmonics coming from higher NZs, as shown in Fig. 7 after sampling. This aliasing is unavoidable, since an antialiasing filter cannot be included between the comparator and the register, in order to maintain a two-level signal. The use of a binary signal allows to simplify the sampling hardware to a single-bit register. Therefore, an analysis of the $p(t)$ PWM spectrum signal should be considered, in order to understand how this overlapping can be avoided in the signal's band.

The PWM modulation process (6), which is the comparison between the RF signal, $x(t)$, and the reference signal, $r(t)$, can be described by the sign function (7)

$$p(t) = \text{sign}(x(t) - r(t)) \tag{6}$$

$$\text{sign}(x(t)) = \begin{cases} -1, & \text{if } x(t) < 0 \\ +1, & \text{if } x(t) > 0. \end{cases} \tag{7}$$

In [31], a general mathematical model to approximate (6) is presented in (8), and is valid for every $x(t)$ signals

$$p(t) = x(t) + \frac{2}{\pi} \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{1}{n} e^{jn\omega_r t} \sin\left(\frac{n\pi}{2}(1 + x(t))\right) \tag{8}$$

where ω_r is the angular reference signal frequency and $x(t)$ is the RF signal that can be described as $x(t) = x_{BB}(t) \sin'¡(\omega_c t)$, where $x_{BB}(t)$ is the baseband signal's envelope modulated by a carrier centered at ω_c. Then, replacing $x(t)$ by the previous description and applying some well-known trigonometric identities (8) can be simplified into

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} \cos(n\omega_r t) \times \sin\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t) + \frac{n\pi}{2}\right). \tag{9}$$

Consequently, applying the sum-to-product trigonometric identity, (9) becomes

$$p(t) = x(t) + \sum_{n=1}^{+\infty} \frac{4}{n\pi} \cos(n\omega_r t) \sin\left[A(t)_{n\,\text{even}} + A(t)_{n\,\text{odd}}\right] \tag{10}$$

where $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ are, respectively, given by

$$A(t)_{n\,\text{even}} = \cos\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t)\right) \tag{11}$$

$$A(t)_{n\,\text{odd}} = \sin\left(\frac{n\pi}{2}\right) \cos\left(\frac{n\pi}{2} x_{BB}(t) \sin(\omega_c t)\right). \tag{12}$$

To know the spectrum of the PWM signal $p(t)$, a Fourier transform must be applied on (10). However, the Fourier transform of all the elements is not trivial, since it implies to calculate the transform of a function in the format $\sin(\beta \sin(\theta))$ and $\cos(\beta \sin(\theta))$. It can be further simplified using the Jacobi–Anger expansion, which uses the first-order kind Bessel function [32]

$$\sin(\beta \sin(\theta)) = 2 \sum_{k=1}^{+\infty} J_{2k-1}(\beta) \sin((2k-1)\theta) \tag{13}$$

$$\cos(\beta \sin(\theta)) = J_0(\beta) + 2 \sum_{k=1}^{+\infty} J_{2k}(\beta) \cos(2k\theta) \tag{14}$$

where $J_k, k \geq 0$ represents the first-order kind Bessel function. Therefore, by applying (13) and (14) on (11) and (12) a new approximation for $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ can be achieved in the form of (15) and (16)

$$A(t)_{n\,\text{even}} = \cos\left(\frac{n\pi}{2}\right) 2 \sum_{k=1}^{\infty} J_{2k-1}\left(\frac{n\pi}{2} x_{BB}(t)\right) \times \sin((2k-1)\omega_c t) \tag{15}$$

$$A(t)_{n\,\text{odd}} = \sin\left(\frac{n\pi}{2}\right) \left[J_0\left(\frac{n\pi}{2} x_{BB}(t)\right) + 2 \sum_{k=1}^{\infty} J_{2k} \times \left(\frac{n\pi}{2} x_{BB}(t)\right) \cos(2k\omega_c t) \right]. \tag{16}$$

Considering now (10) with the new expressions for $A(t)_{n\,\text{even}}$ and $A(t)_{n\,\text{odd}}$ it is possible to reach an approximation of the central frequency bins, where the PWM distortion will fall. In fact it is not relevant to solve the entire Fourier transform of (10), since the idea is just to choose a reference frequency $r(t)$ to avoid the distortion overlap in the first NZ and, consequently, optimize the receiver SNR.

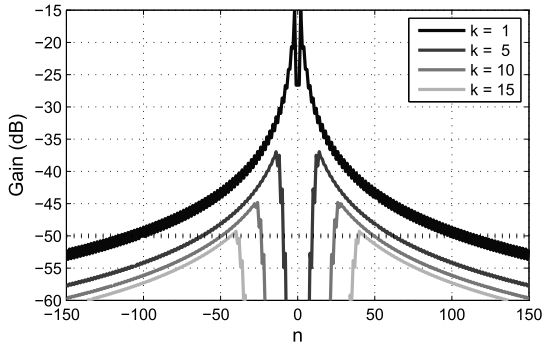


Fig. 8. Magnitude of the amplitude response of $P^*(f)$.

Thus, (17) and (18) present the center frequencies of the PWM distortion bands

$$P^*_{n\,\text{even}}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) * \left[\sum_{k=1}^{\infty} |J_{2k-1}(B(t))|_{\max}\delta(f - (2k-1)f_c)\right]$$

$$P^*_{n\,\text{odd}}(f) = \sum_{n=1}^{\infty} \frac{2}{n\pi}\delta(f - nf_r) \quad (17)$$

$$* \left[|J_0(B(t))|_{\max} + \sum_{k=1}^{\infty} |J_{2k}(B(t))|_{\max}\delta(f - 2kf_c)\right] \quad (18)$$

where $P^*_n(f)$ are the central bins of the positive part of the $p(t)$ spectrum, $\delta(f)$ is the Dirac delta function, $|J_k\ (B(t))|_{\max}$ with, $B(t) = (n\pi/2)x_{BB}(t)$, is the maximum absolute value of the amplitude response for a given distortion bin.

At this point, it is important to note that (17) and (18) give the information of the central frequencies of each PWM harmonic, as shown in spectrum before sampling in Fig. 7. Thus, considering a certain level of required or imposed SNR, it should be guaranteed that the PWM harmonics do not fall over the interest band in the first NZ. Therefore, the folding frequency bins placement in the first NZ should be calculated using (19)

$$f_{\text{fold}} = \left| f_c - \left\lfloor \frac{f_c}{f_s} \right\rceil f_s \right| \quad (19)$$

where f_{fold} is the folding frequency in the first NZ, f_c is the carrier frequency, f_s is the sampling frequency, $\lfloor \ldots \rceil$ is the rounding operation toward nearest integer, and $|\ldots|$ is the absolute value. In addition, the amplitude response of $|J_k\ (B(t))|_{\max}$ must be analyzed, up to an n and k value that guarantee the calculation of all distortion bands above the SNR limit.

The maximum k and n values from (17) and (18) can be extrapolated from an imposed limit of the amplitude response of $P^*_n(f)$. In Fig. 8, a limit of -50 dB is considered for the amplitude gain which immediately imposes a maximum value of 15 for the maximum carrier frequency harmonic k. Then,

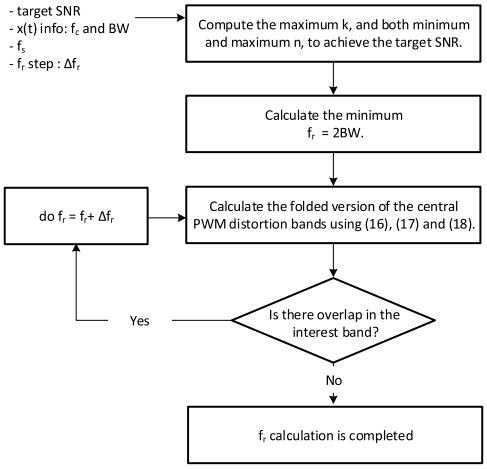


Fig. 9. Flowchart diagram of the proposed algorithm to find the best reference frequency to improve the SNR.

after obtaining n, k that will be considered, for the calculation of the folding spectrum version using (19), this information must be used in an algorithm to obtain the best reference frequency (Fig. 9).

The proposed algorithm starts with a set of inputs, which are the target SNR, the carrier frequency, f_c and the bandwidth, BW, of the signal $x(t)$, the sampling frequency, f_s, and a step for the reference frequency (Δf_r). It should be noted that BW here considered is the channel bandwidth instead of the signal bandwidth in order to allow for a small frequency margin for filtering, usually a small percentage of the signal bandwidth, for example, 30% is considered reasonable.

Regarding the algorithm, it starts by computing k and both minimum and maximum n to guarantee the target SNR, as previously described. Then, it calculates the minimum reference frequency, which is given by 2BW. Following, there is the calculation of the folded version of the spectrum and the verification of the presence of any overlap that may jeopardize the SNR. If there are no overlaps, the reference frequency calculation finishes, otherwise a new reference frequency is tested, given by the previous frequency plus a given step (Δf_r). This step should be small enough to allow a small loss of resolution and should have an irrational relation to f_s in order to avoid successive occurrences of overlaps from various NZs. Therefore, this step was fixed to be a submultiple of π. An alternative should also be to vary f_s, however that would increase the complexity of the DDC chain due to the need of irrational decimation filters. This procedure will allow to obtain a f_r that will generate a sampled signal, which obeys to the target SNR limit.

In order to exemplify the proposed algorithm, Fig. 10 presents the simulation results of the proposed receiver considering an ideal comparator. The simulation was performed considering a carrier frequency of 1650 MHz and a 16-QAM signal with 5 MHz of symbol rate. The minimum reference is 14 MHz and the optimized reference after computing the proposed algorithm is 30.9 MHz. As it is possible to verify in Fig. 10, the signal's spectrum using the minimum reference frequency presents a degraded SNR when compared with the spectrum with the best reference. In fact, after computing the

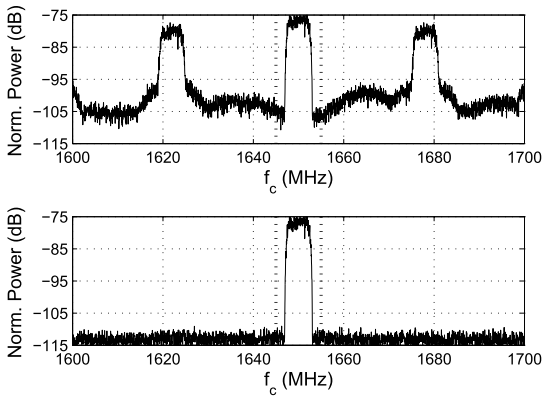


Fig. 10. Receiver simulation results with and without best reference calculation, top and bottom plot, respectively.

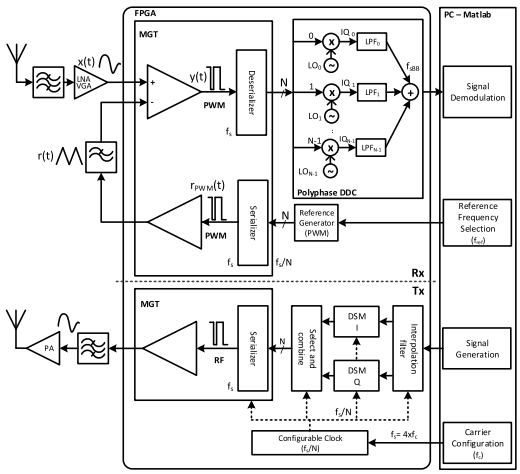


Fig. 11. Block diagram representation of the proposed FPGA-based all-digital transceiver architecture.

EVM of both situations, it was verified an SNR improvement of 9 dB, which validates the proposed technique.

Finally, during laboratorial measurements new spectral bins, different from the ones predicted by (17) and (18) were detected. In fact, these new distortion bins are associated with a dc offset error α at the input of the comparator, which can be modeled by (8) considering that $x(t)$ is now given by $x(t)+\alpha$. Therefore, applying the mathematical steps presented previously, a new expressions for $P_n^*(f)$ considering the mismatch Î±, can be reached (20) and (21), as shown at the bottom of this page.

C. FPGA Implementation

A proof of concept prototype was developed using the proposed transmitter and receiver architectures presented in the previous sections. The hardware design was implemented in a KC705 board from Xilinx with a Kintex-7 XC7K325T FPGA. An FPGA design allows for a completely integrated approach of both the all-digital transmitter and receiver due to the high logic capacity of modern FPGAs. Also, their inherent reconfigurability allows for a fast adjustment of the radio hardware to different purpose scenarios, which strongly falls within the concept of SDR. The FPGA-based transceiver architecture, shown in Fig. 11, can be separated into its two main functional blocks, the transmitter (ADT) and the receiver (ADR). The implemented system has an Ethernet connection to a local PC running a MATLAB routine responsible for the baseband signal generation and demodulation, transceiver carrier control, and reference signal frequency calculation. The transmitter interpolation filter defines the datapath sampling rate. Higher sampling frequencies will improve the signal OSR in the DSM and, therefore, the transmitted signal quality. However, the sampling rate must be adjusted depending on the carrier frequency. For carriers between 400 MHz and 1 GHz, the sampling frequency is equal to f_c, and the RF waveform is the following parallel word w_{low} on (22). The use of repeated samples in (22) reduces the carrier frequency to half while maintaining the transceiver clock within the FPGA PLL frequency lock range. This allows to use this ADTx architecture for carrier frequencies between 400 MHz and 2.4 GHz

$$w_{\text{low}} = [I_0;\, I_0;\, Q_0;\, Q_0;\, \overline{I_1};\, \overline{I_1};\, \overline{Q_1};\, \overline{Q_1};\, I_2;\, I_2;\, Q_2;\, Q_2;\, \overline{I_3};\, \overline{I_3};\, \overline{Q_3};\, \overline{Q_3}] \quad (22)$$

The input IQ signal is upsampled to an equivalent sampling frequency of $f_s = f_c$ using a polyphase interpolation filter with four parallel paths. This enforces a digital hardware clock frequency of $f_c/4$ (between 100 and 250 MHz depending on f_c) for the interpolation filter, DSM and select and combine logic. For carriers above 1 GHz and up to 2.4 GHz, the sampling frequency is half of f_c and the RF waveform is given

$$P^*_{n\,\text{even}}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f-nf_r) * \left[\left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \left|J_0(B(t))\right|_{\max} + \left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k-1}(B(t))\right|_{\max} \delta(f-(2k-1)f_c) + \left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k}(B(t))\right|_{\max} \delta(f-(2k)f_c) \right] \quad (20)$$

$$P^*_{n\,\text{odd}}(f) = \sum_{n=1}^{\infty} \frac{n\pi}{2}\delta(f-nf_r) * \left[\left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \left|J_0(B(t))\right|_{\max} + \left|\cos\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k}(B(t))\right|_{\max} \delta(f-2kf_c) - \left|\sin\left(\frac{n\pi}{2}\alpha\right)\right| \sum_{k=1}^{\infty} \left|J_{2k-1}(B(t))\right|_{\max} \delta(f-(2k-1)f_c) \right] \quad (21)$$

by the word w_{high} as in

$$w_{\text{high}} = [I_0;\, Q_0;\, \overline{I_0};\, \overline{Q_0};\, I_1;\, Q_1;\, \overline{I_1};\, \overline{Q_1};\, I_2;\, Q_2;\, \overline{I_2};\, \overline{Q_2};\, I_3;\, Q_3;\, \overline{I_3};\, \overline{Q_3}] \quad (23)$$

In this case, the equivalent sampling rate varies between 500 and 1200 MHz (four parallel paths), and the logic clock will be between 150 and 300 MHz depending on f_c. The DSM stage is built with two parallel modulators, one for each of I and Q datapath, with polyphase implementation of a first-order modulator with four parallel paths. The DSM hardware runs with the same clock as the interpolation filter, being able to process up to 1200 Ms/s. The output will be a parallel word of 4 b for each modulator correspondent to four consecutive time samples. The upconversion to the carrier frequency is done by combining the DSM outputs accordingly to a specific order, as stated in (20) or (21) subject to the carrier frequency. The word w is then serialized accordingly to the specified order. The serialization of the word is using an integrated high-speed transceiver capable of data rates up to 10 Gb/s. The transceiver's clock frequency will be either $4f_c$ or $8f_c$ depending on whether the word at the input is w_{low} or w_{high}. At the output of the serializer, the two-level signal will be centered in f_c surround by quantization noise from the DSM in the sidebands. To remove the quantization noise, an output filter at the target frequency band can be used.

Similar to the RF output signal, the proposed transceiver also uses a binary output to produce the reference waveform for the receiver. In this case, a baseband PWM is used to generate a triangular wave at the specified reference frequency, varying between 4 and 30 MHz. The signal is filtered with a low-pass filter to recover the required waveform by removing the PWM quantization noise. The reference signal is compared with the input RF signal using the FPGA high-speed differential input buffers as a comparator. This comparator is followed by a register working at 10 GHz of sampling frequency, generating a digital bitstream that will be deserialized by a factor of N, as shown in Fig. 11. Therefore, the sampled PWM waveform arrives at the remaining FPGA logic at f_s/N, with $N = 64$. Then, the RF data have to be downconverted to baseband, filtered, and decimated. The downconversion and the filtering are performed using a polyphase digital direct synthesizer and a polyphase filter, in this case with $N = 64$ parallel branches. After the DDC, the signal is transferred to the local PC via an Ethernet connection, where the baseband data are demodulated and analyzed for its EVM.

IV. Measurement Results

The transceiver performance was measured in terms of signal quality for both the transmitted and received signals. The figure of merit used to evaluate the signal quality is the EVM using two different signals 16-QAM and 64-QAM, with 2 and 5 MHz of symbol rate, both generated using a root raised cosine filter with a roll-off of 0.22, which implies a channel bandwidth of 2.44 and 6.1 MHz. The following sections show the performance results for the isolated transmitter (Figs. 12 and 13), isolated receiver (Fig. 14), and transceiver point-to-point configuration.

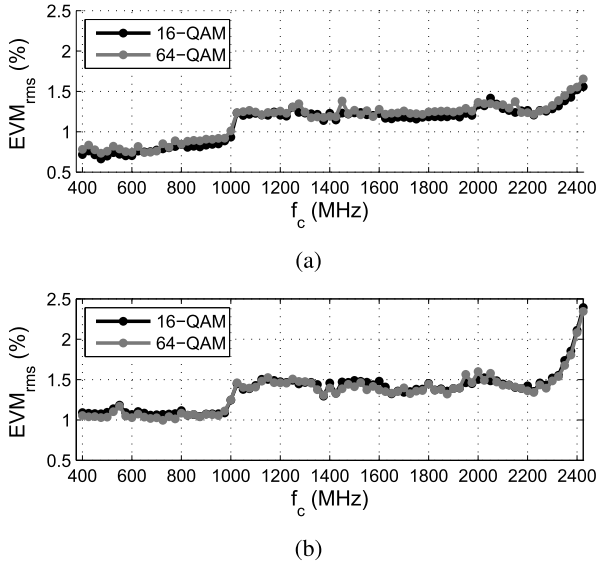


Fig. 12. Transmitter EVM using 16-QAM and 64-QAM signals. (a) 2-MHz bandwidth signal. (b) 5-MHz bandwidth signal.

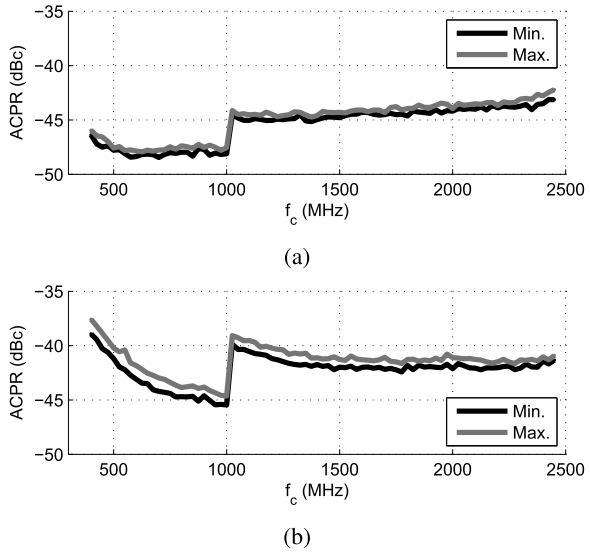
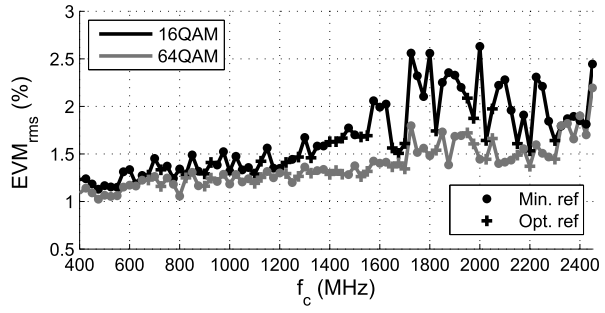


Fig. 13. Transmitter ACPR measurement. (a) 2-MHz bandwidth channels. (b) 5-MHz bandwidth channels.

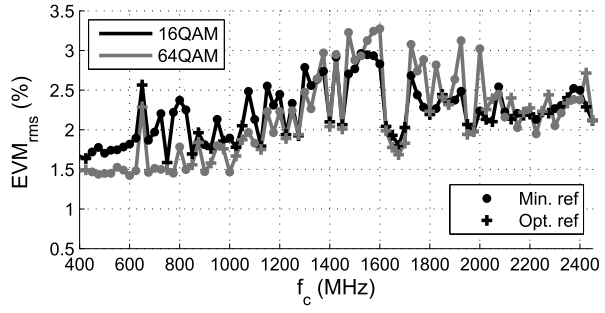
A. Transmitter

The transmitter performance was measured in terms of SNR performing a sweep over the carrier frequencies between 400 MHz and 2.425 GHz with a step of 25 MHz. The measurement setup was assembled, as shown in Fig. 15. In Fig. 12(a) and (b), the EVM results are shown for a 2- and 5-MHz symbol rate. The results show that for the tested modulations and symbol rates, the EVM along the measured carrier frequencies is always inferior to 2.5%.

The adjacent channel power ratio (ACPR) was measured for both the 2- and 5-MHz channels along the tested carrier frequencies. The measured ACPR values are shown in Fig. 13, and the maximum and minimum values correspond to the best and worst ACPR scenarios considering the tested modulation of 16-QAM and 64-QAM. Both the lower and upper channels were measured for every frequency and the worst case was considered as the ACPR value for that carrier frequency.



(a)



(b)

Fig. 14. Receiver EVM measurement. (a) 2-MHz symbol rate signal. (b) 5-MHz symbol rate signal.

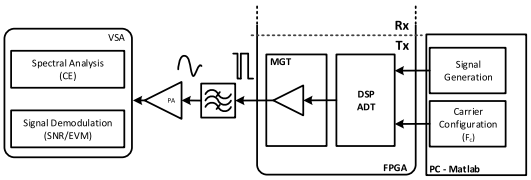


Fig. 15. Block diagram of the transmitter measurement setup.

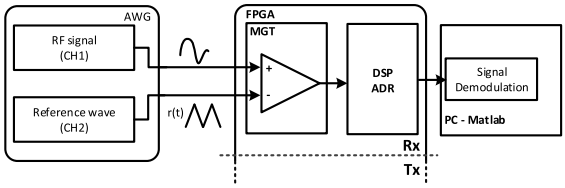


Fig. 16. Block diagram of the receiver measurement setup.

The CE for the transmitted signal of 16-QAM and 64-QAM was also measured and was found to vary between 15% and 22% depending on the PAPR of the signal. The EVM variation around 1 GHz occurs due to the change from w_{low} to w_{high}, which presents worst jitter behavior. The EVM change around 2.4 GHz, however, appears because the DSM reaches its maximum clock operation and starts to present errors. Nonetheless, these results demonstrate the viability for this transmitter to be used over the measured frequencies.

B. Receiver

The receiver performance was measured performing a sweep over the carrier frequency from 400 up to 2400 MHz with a step of 25 MHz considering the setup shown in the block diagram of Fig. 16. A two channel arbitrary waveform generator (AWG7000A from Tektronix) is directly connected to the receiver and is responsible to generate both the reference and RF signals. For each carrier frequency, the reference signal frequency was previously optimized, considering the algorithm described in Section III.

The EVM sweep results for 2- and 5-MHz symbol rate signals are shown in Fig. 14(a) and (b). In both these sweeps, it is possible to see the points that were measured using the minimum reference and optimized reference. The use of the optimized reference allows for the EVM to maintain relatively constant value for the swept carrier frequencies, despite of the PWM folded harmonics. Regarding the 2-MHz signal, it was possible to reach an EVM below 2.7% for the entire bandwidth.

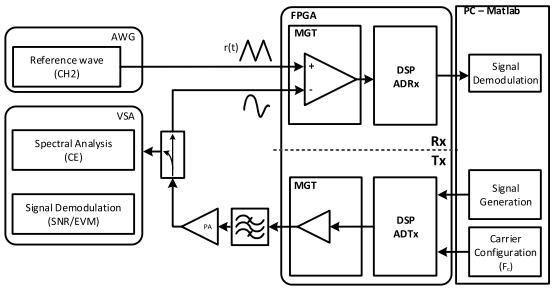


Fig. 17. Block diagram of the transceiver loop-back measurement setup.

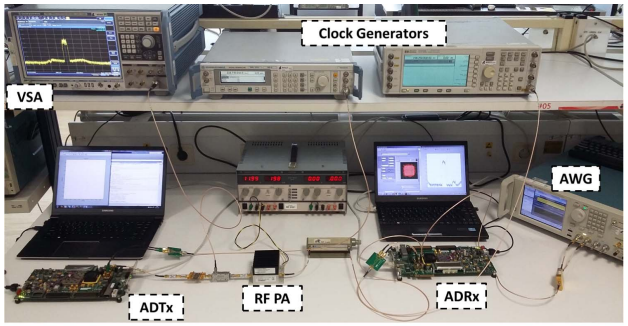


Fig. 18. Measurement setup photograph.

C. Full System Transceiver

The implemented all-digital transceiver was tested in a Tx/Rx point-to-point configuration for some frequency bands of interest and feasible with the proposed architecture. For this measurement, the transmitted signal is filtered by a bandpass filter, and is sent directly to the receiver that acquires the signal. Then, after the DDC, the signal quality is analyzed in terms of EVM. Simultaneously, the signal is also analyzed and demodulated in a VSA, in order to have a reference EVM measurement for the transmission. The measurement setup is shown in Fig. 17. Fig. 18 presents a photograph of measurement setup. In addition, Fig. 19 shows the spectrum of the transmitted and the received signals at 1850 MHz. In the latter, it is possible to observe the PWM distortion around the carrier frequency.

The test signals are 64-QAM with a 2- and 5-MHz sampling rate varying the carrier frequency over the selected bands with

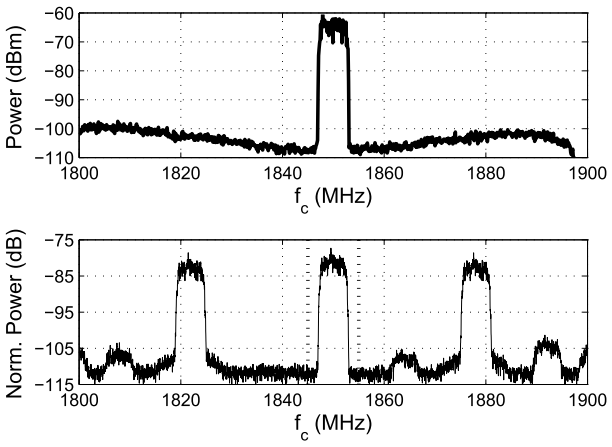


Fig. 19. Top: spectral capture of the transmitted signal with a VSA. Bottom: RF received signal at the all-digital receiver.

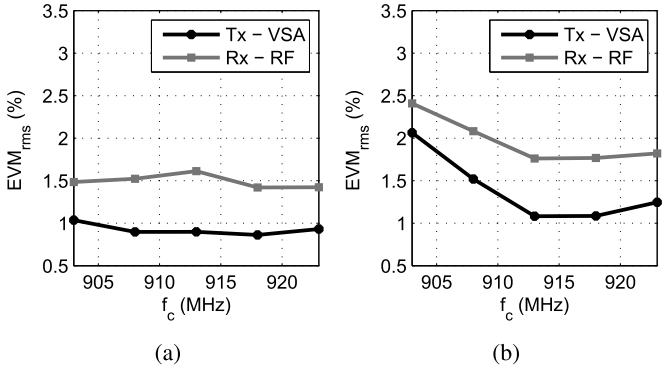


Fig. 20. Measurement over the 900-MHz ISM band. (a) Using a 2-MHz 64-QAM signal. (b) Using a 5-MHz 64-QAM.

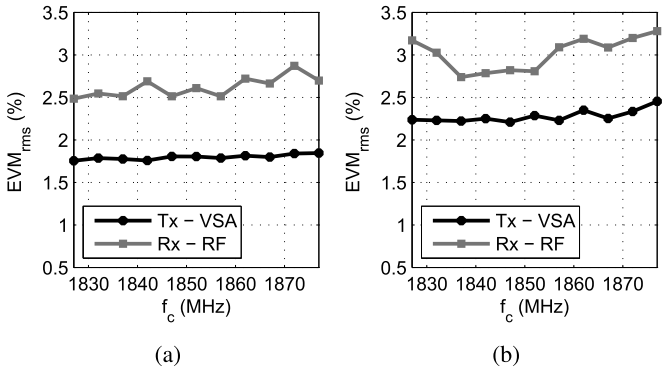


Fig. 21. Measurement over the 1800-MHz LTE band. (a) Using a 2-MHz 64-QAM signal. (b) Using a 5-MHz 64-QAM.

a step of 5 MHz. Fig. 20 shows a sweep over f_c in the 900-MHz ISM band starting on 903 and up to 923 MHz. Fig. 21 shows a sweep over f_c in the 1800-MHz LTE band starting on 1827 and up to 1881 MHz. The presented measurements show the feasibility of the proposed transceiver architecture for some of common frequency bands.

Finally, an overall comparison between the proposed architecture and other similar state-of-the-art transceivers must be considered. However, since this is the first time, such an architecture is presented, and this comparison can only be done to the transmitter and receiver independently with the respective state-of-the-art architectures.

The proposed transmitter uses polyphase architecture as presented in [18], which is in line with the state-of-the-art figures of merit in terms of bandwidth, SNR, and CE. However, the transmitter architecture was designed to allow for fast carrier frequency flexibility, and in fact, this is the first time that such a large set of carrier frequencies were tested showing the feasibility and functionality of this transmitter for those frequencies.

On the receiver side, the same carrier frequencies were also tested presenting reasonable results. When comparing this system with [23], focusing on the 5-MHz signals, there were improvements in terms of SNR/EVM. Despite the fact that in [23], the PWM sampling is two times superior to 10 GHz used in this paper, the proposed technique allowed to obtain an EVM lower than 3.5%, whereas in [23], the presented EVM is about 6%. Moreover, when comparing this paper with [24], an improvement was also obtained. Both the previous improvements are due to the new technique for selecting the reference frequency.

In order to consider a receiver evaluation in terms of sensitivity and dynamic range, the LNA/VGA should be mandatorily included, which is out of the scope of this paper. However, it is possible to get an estimation of the instantaneous dynamic range transposing the EVM values into SNR by applying the formulation presented in [33]. Therefore, considering that the best and the worse obtained EVM values are, respectively, 1% and 3.5%, by applying the previous formulation it is possible to get an SNR of 40 and 30 dB. Hence, this leads to an indicative value of the receiver instantaneous dynamic range.

V. Conclusion

In this paper, it was presented for the first time a fully integrated single FPGA-based all-digital RF transceiver, which marks a breakthrough in digital RF system design. The entire signal processing from the baseband up to the RF stage for the transmitter, and the opposite for the receiver, is completely performed in the digital domain. The transmitter chain of the radio is implemented recurring to DSM modulation and the receiver based on PWM modulation, which was optimized with a nonlinear analysis of its behavior.

The proposed system presents high flexibility in a bandwidth of almost 2.5 GHz while maintaining reasonable EVM results for 2- and 5-MHz symbol rate signals. The obtained results make this system highly suitable for the future radio transceivers, specifically focusing on the integration of previous standards that operated in sub-2.5-GHz bands. An FPGA was used as an implementation proof of concept, due to its faster verification and deployment capability. Nevertheless, an application specific integrated circuit could be built following the proposed architecture. However, due to the FPGA's reconfigurability capabilities, it adds an increase degree of flexibility required by SDR applications.

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Paper J3: Agile All-Digital DPD Feedback Loop

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Agile All-Digital DPD Feedback Loop

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***Abstract*— This paper presents an original agile all-digital feedback loop receiver system for power amplifier (PA) linearization using digital pre-distortion (DPD). The proposed feedback loop is based on a radio-frequency (RF) pulse-width modulation (PWM) analog-to-digital converter (ADC). For proof of concept the system was implemented using a single Field Programmable Gate Array (FPGA) chip. Additionally, the system is also presented in a remote version, suitable for future Centralized Radio Access Network (C-RAN), in which the DPD can be performed in a central unit (CU), far from the PA.**

Measurement results of important DPD metrics such as Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM) are presented and evaluated to verify the correct functioning of the proposed feedback loop. The obtained results demonstrate the system's agility and high analog input bandwidth from a few MHz up to almost 4 GHz, while maintaining the LTE ACPR and EVM requirements.

***Index Terms*—Analog-to-Digital Converters (ADCs), Pulse-Width Modulation (PWM), Field Programmable Gate Array (FPGA), Digital Pre-Distortion (DPD), PA linearization.**

I. INTRODUCTION

Current wireless communications systems present stringent requirements in terms of bandwidth, flexibility and power efficiency. Certainly, future (5G) systems will maintain the trend to fulfill these requirements [1]. In order to successfully achieve these needs, wideband and efficient devices are required, such as radio-frequency (RF) sampling analog-to-digital (ADC) and digital-to-analog (DAC) converters, mixers and power amplifiers (PA). Nowadays already exist a few GHz capable converters and mixers, however the PA is usually the more difficult device to get both high efficiency, high power and high bandwidth. Additionally, to increase the PA efficiency, to eliminate the PA in-band non-linear distortion effects and to meet important spectral masks imposed by the standards, linearization techniques based on digital pre-distortion (DPD) are widely used [2], [3].

In order to implement DPD algorithms, the presence of a feedback loop, or observation path, is mandatory to acquire a replica of the signal at the output of the non-linear device, i.e., the PA. This receiver will allow to estimate a behavioral model for the PA, and extract an inverse digital model that will compensate its non-linear effects. The ideal result would be a linear system with improved efficiency, without non-linear distortion and obeying the spectral masks requirements. Fig. 1a), presents a traditional architecture of an RF transmitter with a feedback loop receiver for DPD. The homodyne receiver topology using analog mixers for the signal down-conversion, in which the same local oscillator (LO) is shared with the transmitter, followed by a dual-channel based-band ADCs, represent the most commonly used architecture for the feedback loop path. On the other hand, as presented in Fig. 1b) RF sampling ADCs can provide an alternative way to design the feedback-loop receiver offering high bandwidth and improved flexibility to the system. However, the commercially available RF ADCs are usually quite expensive and present a high power consumption, which makes its use sometimes prohibitive [4].

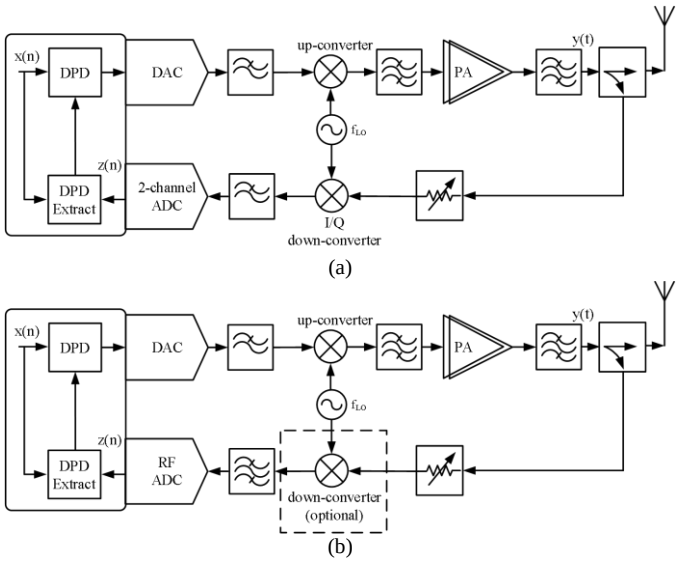

Fig. 1. Block diagram representation of an RF transmitter with a feedback loop receiver for DPD: a) traditional feedback loop architecture using homodyne receiver b) feedback loop using an RF sampling ADC.

Within this context, there are two main research fields that have been intensely addressed by academia and industry. Firstly, there is an effort to look for efficient behavioral modeling structures, which allow to get more accurate PA models and consequently improved DPD performance. The most common used behavioral models are usually based on Volterra series simplifications, such as Memory Polynomial (MPs) models [3], [5]–[7], due to their improved performance, whereas maintaining a reduced number of coefficients. The

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second important topic is regarding the feedback requirements relaxation, as it is referred in [2] as one of the future challenges in DPD. In this topic there are some recent works, focusing on under-sampling ADCs such as presented in [4], [8], [9]. In [4] a technique using ADCs that operate at sampling rates much lower than required by Nyquist limits is proposed, achieving a 3 to 5 times sampling rate reduction. In [8] low-speed ADCs in the feedback loop path are used together with spectral extrapolation, which is introduced to the acquired band-limited signal. In [9] a method to improve the linearization in under-sampling scenarios is presented.

The latter topic is the main focus of this paper, in which a novel agile all-digital feedback loop receiver for PA linearization is presented. This work presents for the first time a feedback loop architecture based on a single bit RF pulse-width modulation (PWM) ADC using a single-bit comparator, implemented using a medium-range Field-Programmable Gate Array (FPGA). The proposed system is presented in two simple and highly flexible topologies. In the first topology the receiver is implemented by using FPGA inputs directly as a comparator. While the second topology is suitable for Centralized Radio Access Network (C-RAN) architectures, in which the receiver is presented in a simple remote version, as in [10]. In [10], an uplink section of a C-RAN architecture was proposed and evaluated in terms of received signal's Error Vector Magnitude (EVM), whereas in this work the focus is on the DPD observation path. The key idea of C-RAN architectures, as presented in Fig. 2, is to centralize the management and signal processing jobs at a central unit (CU). At the same time these jobs are removed from the radio access units [11], leading to simple and low cost Remote Radio Heads (RRHs). To connect the CU to the RRH a low-latency and high-bandwidth microwave or optical transport layer (fronthaul) is required. Such an architecture brings directly advantages in terms of spectral efficiency, interference management between radio heads and agility [10], [11].

This paper is organized as follows. Section II addresses the working principle of RF PWM ADCs. In Section III the proposed feedback loop architecture is presented. Then, in order to validate the proposed technique measurement results of Adjacent Channel Power Ratio (ACPR), EVM and NMSE (Normalized Mean Squared Error) will be presented and discussed in Section IV. Additionally, to fairly compare the obtained results with the proposed receiver, a Vector Signal Analyzer (VSA) is also used as feedback loop, in order to mimic a traditional configuration. Finally, Section V presents the conclusion of this work, addressing some of the advantages and drawbacks of the proposed technique.

II. RF PWM ADCs

Fig. 3 presents the block diagram representation of an RF PWM ADC, which is composed by a single comparator. Following this diagram, it is possible to verify that one of the comparator inputs is used for the incoming RF signal (*s(t)*),

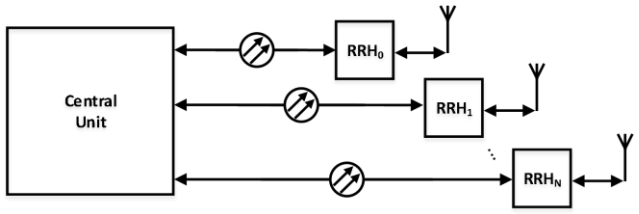

Fig. 2. Block diagram representation of a C-RAN architecture made by one central unit (CU) connected to a set of RRHs through an optical fiber used as transport layer (fronthaul), from [10].

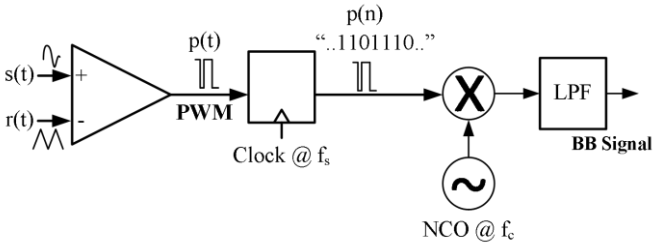

Fig. 3. RF PWM receiver block diagram (NCO – Numerical controlled oscillator, LPF – low pass filter).

which is centered at f_c and presents a bandwidth of *BW*. The other input is used for a reference signal (*r(t)*) that is typically a sawtooth or triangular wave with a frequency of f_r. At the comparator's output it will appear a natural sampling PWM representation of the RF signal (*s(t)*), which is represented as *p(t)*. In theory, if *r(t)* is correctly dimensioned the *p(t)* signal should preserve the same Signal-to-Noise Ratio (SNR) with respect to the *s(t)* signal [12]. After the comparator, a single-bit register is responsible to uniformly sample and discretize the *p(t)* signal at a rate of f_s (with $f_s >> BW$ and $f_s > f_c$), producing a discrete time version *p(n)*, which is a uniform-sampling PWM signal containing the s*(t)* signal's information. Afterwards in the digital domain the remaining processing tasks such as down-conversion and filtering can be performed to recover the *s(t)* envelope [10], [13].

Despite the simplicity of this architecture, its analysis is not trivial. The natural sampling PWM signal (*p(t)*) generation generates out-of-band PWM harmonic content, that may fold and overlap in the band of interest after sampling, if the *r(t)* waveform is not correctly dimensioned. Thus, the *r(t)* signal must be carefully designed depending on the *s(t)* carrier frequency (f_c), bandwidth (*BW*) and the sampling frequency (f_s), which was the main focus of [13].

This type of converters were firstly suggested in 1960's [14]. The behavior of the sampling circuit can be explained recurring to statistical quantization theory. According to this theory it can be proved that the *r(t)* signal frequency is related to the maximum bandwidth to acquire and its amplitude must be equal or greater to the amplitude of the signal to sample (*s(t)*) [14], [15]. Moreover, to equally sample the *s(t)* signal, *r(t)* must present an uniform amplitude distribution, which is the motive for the use of a triangular or sawtooth waveforms [10], [14], [15].

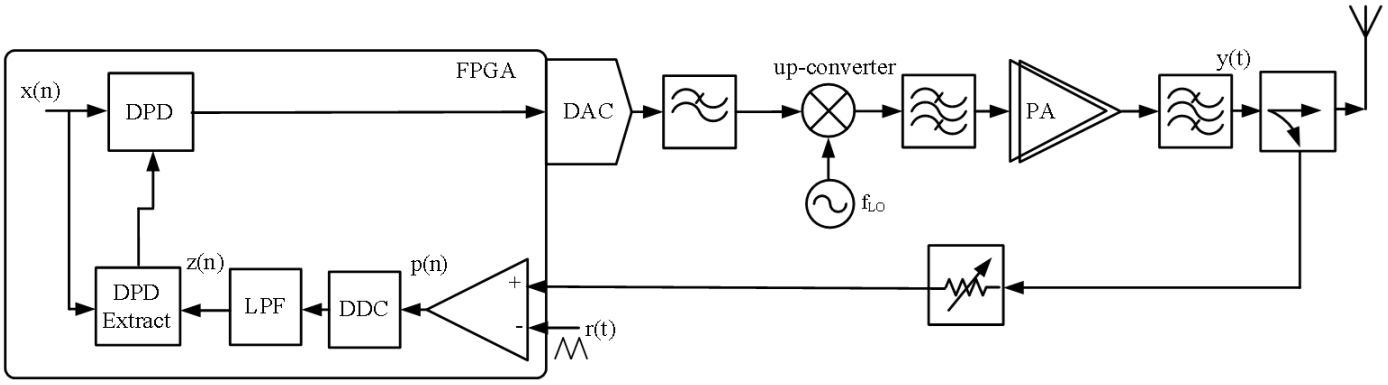

Fig. 4. Block diagram representation of an RF transmitter with an FPGA-based all-digital feedback loop receiver for DPD. (DDC - digital down-conversion).

Although these ADCs are frequently conceived for low-frequency applications, lately there was some research effort to use them for the design of RF receivers [16]–[19]. The usage of high speed comparators to produce an RF PWM signal is explored in [16], where an FPGA is used to collect the signal created by the comparators. In [17]–[19] a step towards higher integration is achieved allowing to build an entire RF receiver using a single FPGA chip by using its high speed inputs directly as comparators. In [10] the possibility to adapt this architecture to a C-RAN is proposed where the RF front-end is presented in a simple remote version. Finally, this type of converters present a high analog input bandwidth being suitable for a DPD feedback loop receiver as it will be demonstrated in this paper.

III. Proposed Feedback Loop

In a common feedback loop architecture for DPD as presented in Fig. 1, the *y(t)* signal is the PA's output, which is transmitted through the antenna and acquired by the feedback loop in order to be possible to pre-compensate for the PA non-linear behavior by applying a suitable DPD algorithm. The signal acquired by the feedback loop is represented as *z(n)*, and its low-pass equivalent (LPE) envelope should be the closest possible representation to the one of *y(t)*. Therefore, the receiver should present minimal impairments in order to get the most accurate model for DPD, as it was already studied in [20].

After addressing the main concept of an RF PWM ADC, this Section presents the two topologies of the proposed new all-digital feedback loop for DPD. Both topologies are presented considering an FPGA implementation, due to the importance that such devices have nowadays in digital signal processing (DSP) tasks, which are fundamental in the existing wireless communication systems. Current state-of-the-art FPGA devices present high logic capacity that can be used for intensive DSP tasks, such as for DPD models implementation and extraction. However, model extraction is more commonly implemented in high speed processors. In this context current System-on-Chip (SoC) devices, which present a high speed processor and an FPGA in the same chip are quite important for DPD application scenarios. Additionally, the FPGAs reconfiguration capability, which allows in run-time to change the digital circuitry, provides tremendous versatility to operate different tasks in different time frames. Due to this, FPGAs are also commonly used to implement several communication DSP tasks and to interface with high-speed mixed-signal converters (ADCs and DACs). Moreover, these devices present several very high speed single-bit inputs and outputs (currently operating at speeds up to 28 Gbps), which can be used to implement single-bit RF mixed-signal converters as presented in [10], [17]–[19], [21]–[23] and explored for the first time in this work as a base component of an all-digital feedback loop.

A. All-digital feedback loop receiver for PA linearization via DPD

Fig. 4 presents the proposed block diagram representation of an RF transmitter with an all-digital feedback loop for DPD, in which it is used an FPGA-based RF PWM ADC. By analyzing Fig. 4 diagram, it is possible to verify that the transmitter section has not been changed, being the same as presented in Fig. 1. However, the observation path is now quite simpler than the one in Fig. 1. In fact, after the coupler the only required analog component is a variable attenuator in order to avoid the ADC clipping, which is also required in traditional architectures. Thereafter, there is immediately one of the comparator's inputs, while the other is used for the reference waveform *r(t)*. Despite not shown in the diagram the *r(t)* signal can be generated using the FPGA high speed output following similar techniques as presented in [13], [21]–[23].

Consequently, after the comparator, in which the signal is sampled at a frequency f_s , an uniform sampling PWM signal containing the signal *y(t)* information is available to be processed digitally. Therefore, by using digital donwn-conversion (DDC) at f_c and a low-pass filter (LPF) it its possible to recover a replica of the *y(t)* LPE, represented in the diagram as *z(n)*. Regarding the DDC, this must be designed in a polyphase topology to be able to cope the high sampling rate. One might consider its dimension to be difficult, considering the high decimation ratio, however in [13], [17] it was already shown feasible implementation with the FPGA available resources.

Afterwards every piece of data is gathered to apply a DPD algorithm suitable for the type of PA being used. In the

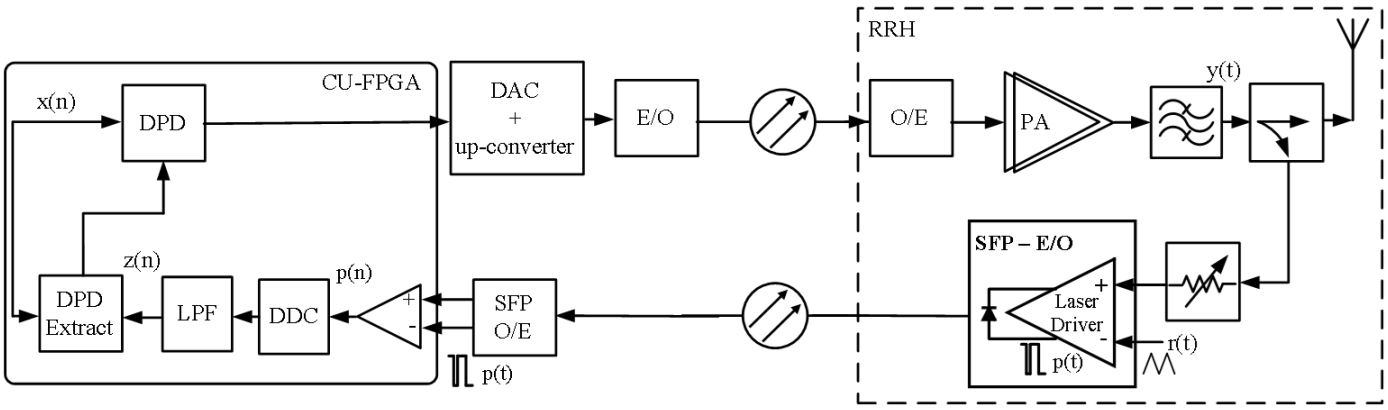

Fig. 5. Block diagram representation of a C-RAN architecture with RRH and an all-digital feedback loop receiver for DPD.

context of this work, a Memory-Polynomial (MP) model is used, as presented in [24]:

$$\hat{z}(n) = \sum_{k=0}^{K-1} \sum_{m=0}^{M} h_{k,m} \hat{x}(n-m) |\hat{x}(n-m)|^k, \quad (1)$$

where $\hat{x}(n)$ and $\hat{z}(n)$ represent the LPE signal at the input and output of the PA, respectively, $h_{k,m}$ the PA model coefficients, K the non-linearity order and M the memory depth. Then by applying an indirect learning technique by using an inverse model for the PA, the DPD model coefficients can be extracted by using a least-squares estimation technique. Finally, the following procedure would be to apply the model kernels to the input signal *x(n)*, in order to generate the pre-distorted version.

B. Remote All-digital feedback loop receiver for PA linearization via DPD

As previously stated, one of the strongest candidates for next generation wireless networks architectures is C-RAN, which consists in a different scenario than the one described in the previous sub-Section. In such scenario, simple RRHs are required, while the complexity is moved to the CU (Fig. 2) [10], [25].

As presented in Fig. 5, the transmitter chain contains significant changes. The processing of the baseband signal and its up-conversion to the RF domain is performed in the CU, then an electro-optical converter (E/O) transmits the RF signal over an optical fiber link in a well-known Radio-over-Fiber (RoF) scenario. At the RRH an optical-electrical converter (O/E) translates the signal back to electrical domain and feeds a PA followed by an antenna. There are several alternatives to this type of architectures for the transmitter chain, such as Digital-RoF [25], [26] and baseband signal transportation using specific protocols [27], however this topic falls out of the scope of this paper.

Focusing on the proposed feedback loop for PA linearization, this can also be implemented by using a single bit comparator built with a Small-Form Factor (SFP) optical transceiver. An SFP is a device that presents a high bandwidth differential input to excite an optical laser driver, which can be directly used as an RF comparator. Hence, the reference signal *r(t)* and the *y(t)* attenuated signal feed the SFP inputs, consequently producing a PWM representation of *y(t)*, that will drive the optical laser. Afterwards, an optical fiber path transports a two-level optical signal containing the RF signal's information. At the Central Unit, the fiber path is connected to another SFP transceiver, which is used as a photo diode to receive the optical signal and convert it again to the electrical domain *p(t)*.

At that point, the high speed inputs of an FPGA-chip will sample and discretize the *p(t)* signal at a sampling rate of f_s, creating an uniform sampling PWM signal containing the signal *y(t)* information. After sampling, the signal has to be digitally filtered and down-converted to get the *y(t)* signal LPE. Afterwards all data is gathered in order to apply a DPD algorithm as explained in the previous sub-Section. This architecture enables a new concept of Centralized-DPD, in which several PAs can be remotely linearized by applying DPD at the CU.

Finally, the scalability of such a system is an important feature to be addressed. Considering that a single FPGA chip has powerful DSP capabilities and that presents several high speed inputs it is possible to use it to allow several concurrent feedback loops serving different RRHs at the same time. Additionally, has referred in [10], the use of different wavelengths in the fiber (Wavelength Division Multiplexing) may also be used to improve the scalability or to allow a scenario with multiple simultaneous RF carriers. Therefore, such an architecture answers the C-RAN requirements by allowing the processing of a high number of simple and low-cost RRHs using just a single FPGA at the CU.

IV. Measurement Results

To experimentally corroborate the proposed feedback loop architecture and to mimic the scenario of Fig. 5, a laboratorial setup was assembled accordingly to the block diagram representation of Fig. 6a). The DAC and the up-conversion section of the transmitter was replaced by a commercial arbitrary waveform generator (AWG), namely a Tektronix AWG70002A. In order to simplify the measurement setup no

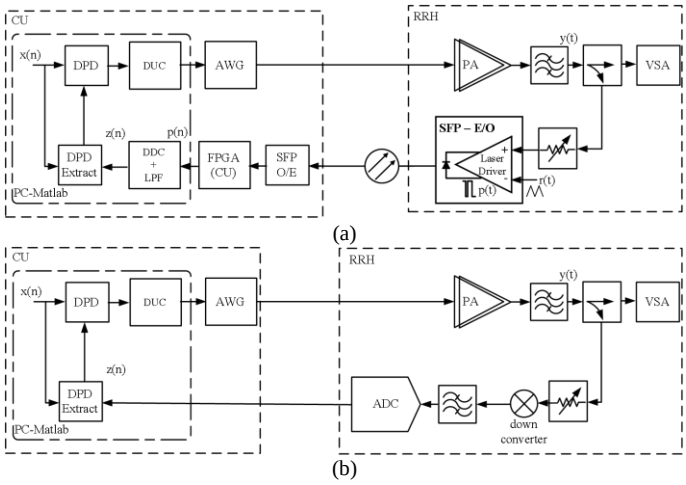

Fig. 6. Block diagram of the measurement setup: a) All-digital feedback loop measurement setup. b) Traditional feedback loop measurement setup.

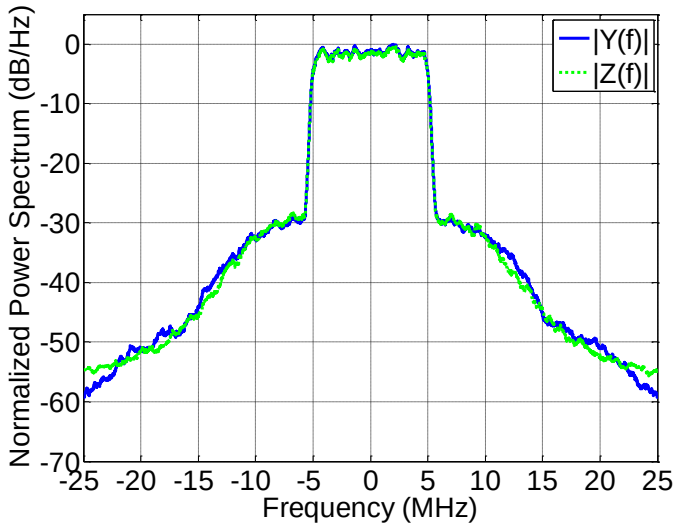

Fig. 8. Spectrum of the signals acquired by the VSA and by the feedback loop. The captured signal has 10 MHz bandwidth and is centered 915 MHz.

fiber path was used in the transmitter chain, therefore the AWG is directly connected to the PA. The PA block is made by a Mini-Circuits ZHL-1042J followed by an ERA-4+. Despite not shown in the block diagram the AWG is also responsible to generate the *r(t)* signal. The feedback loop receiver is made with an SFP optical transceiver AFBR-709SMZ from Avago, working at a wavelength of 850 nm. The same SFP is used in the CU. The latter is connected to a medium-range FPGA development board KCU105. The FPGA differential inputs were set to work at a sampling rate of 16 Gbps. At the output of the PA, a vector signal analyzer (VSA), a FSW8 from Rohde & Schwarz, was used in order to measure the PA performance before and after DPD. Additionally, in order to fairly compare the proposed system, the same VSA was also used to mimic a traditional feedback loop (Fig. 6b)). The laboratorial equipment control and the digital signal processing is performed using *Matlab* software.

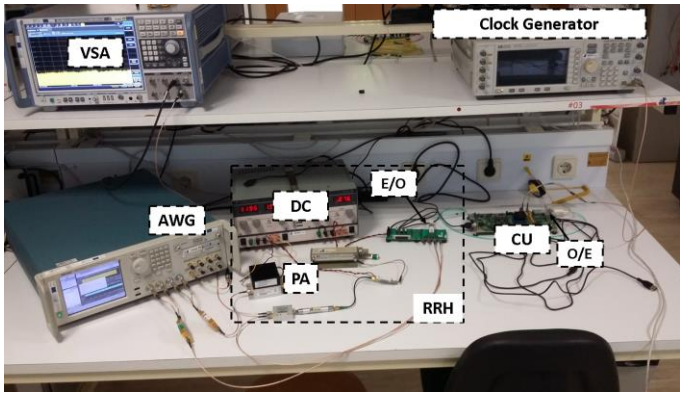

Fig. 7. Photograph of the laboratorial setup.

TABLE I

MEASUREMENTS RESULTS OF NMSE BETWEEN THE SIGNALS CAPTURED BY THE TRADITIONAL FEEDBACK LOOP (VSA) AND THE PROPOSED FEEDBACK LOOP.

f_c (MHz)	BW (MHz)	NMSE (dB)
700	5	-29.23
	10	-25.92
	20	-25.27
915	5	-27.64
	10	-27.65
	20	-25.30
1800	5	-21.23
	10	-23.10
	20	-22.41
2400	5	-25.52
	10	-23.70
	20	-21.26
3450	5	-25.27
	10	-24.07
	20	-22.16

Fig. 7 presents a photograph of the assembled laboratorial setup.

The measurements were performed with 16-QAM modulated signals considering different bandwidths such as 5 MHz, 10 MHz and 20 MHz, which are the most commonly used in nowadays wireless cellular communication systems. Each of these signals has 6.1 dB, 6.2 dB and 7 dB of peak-to-average power ratio (PAPR), respectively. Additionally, in order to show the system's flexibility the following carrier frequencies were tested: 700 MHz, 915 MHz, 1800 MHz, 2400 MHz and 3450 MHz.

A. Evaluation of the signal acquired by the feedback loop

The first step towards the validation of the proposed system is to evaluate the quality of the signal acquired by the feedback loop. In order to perform this evaluation the same

TABLE II

MEASUREMENTS RESULTS OF ACPR AND EVM BEFORE AND AFTER DPD WITH BOTH TRADITIONAL FEEDBACK LOOP (VSA) AND THE PROPOSED ALL-DIGITAL FEEDBACK LOOP.

f_c (MHz)	BW (MHz)	No DPD			DPD with all-digital feedback loop					DPD with traditional feedback loop		
		ACPR (dBc)		EVM_{rms} (%)	K	M	ACPR (dBc)		EVM_{rms} (%)	ACPR (dBc)		EVM_{rms} (%)
		Lower	Higher				Lower	Higher		Lower	Higher	
700	5	30.36	30.34	5.10	7	2	48.37	48.15	0.57	50.01	49.39	0.46
	10	30.18	30.00	4.91	7	2	50.89	50.7	0.42	49.74	49.80	0.44
	20	32.48	32.37	3.83	7	3	49.87	51.91	0.38	51.91	51.81	0.36
915	5	31.15	31.36	4.57	7	2	50.25	50.04	0.48	49.41	49.18	0.48
	10	31.07	31.27	4.30	7	2	50.61	51.20	0.43	49.33	49.85	0.45
	20	33.34	33.84	3.32	7	3	47.23	47.77	0.50	51.38	51.50	0.38
1800	5	32.44	32.56	3.89	7	2	46.2	45.88	0.78	45.56	45.23	0.75
	10	32.57	32.48	3.67	7	2	46.41	46.69	0.71	45.62	45.67	0.70
	20	35.21	35.63	2.68	7	4	48.23	49.34	0.58	48.79	49.12	0.54
2400	5	29.96	30.00	5.36	7	2	45.67	46.07	0.85	44.73	44.73	0.83
	10	30.02	29.97	4.98	7	2	47.06	47.22	0.73	45.15	45.50	0.74
	20	32.48	32.74	3.73	7	4	45.23	46.12	0.84	47.49	47.66	0.64
3450	5	30.34	30.41	5.06	7	2	46.01	45.92	0.89	46.29	46.20	0.76
	10	31.18	31.16	4.85	7	2	45.7	45.25	0.93	45.58	46.01	0.77
	20	32.30	32.58	3.80	7	3	45.10	45.03	0.97	47.37	47.77	0.68

signal captured by both the traditional feedback loop (VSA) and the all-digital feedback loop was compared in terms of NMSE:

$$NMSE = 10\log_{10}\left(\frac{\sum(z(n)-y(n))^2}{\sum y(n)^2}\right)(dB), \qquad (2)$$

where, *y(n)* represents the signal captured by the traditional feedback loop, and *z(n)* the signal captured by the all-digital feedback loop.

Table I presents the results of such comparison for all the combination of carriers and bandwidths that have been measured. It is always possible to verify an NMSE better than -20dB, validating a reasonable accuracy for the feedback loop receiver. One might consider that these NMSE values are low to get an accurate model in a DPD scenario. However, it is important to state that the signal acquired by the feedback loop, due to its one-bit quantization process may contain a high value of quantization noise. However, despite of the impact that this quantization noise has in the computed NMSE it will not directly represent such a strong effect in the modelling stage, since the presented system was able to present quite reasonable results in terms of important DPD metrics, as it will be show in the next sub-Section.

Additionally, Fig. 8 presents the spectrum of a 10 MHz signal centered at 915 MHz at the PA's output, captured with both the VSA and the proposed feedback loop.

B. Application to a DPD scenario

Focusing now on a DPD scenario, all the different signals referred previously, with three different bandwidths and five different carriers were applied at the input of the PA. Then, the output of the PA was measured both by the remote all-digital feedback loop and by a traditional feedback loop. Consequently, in order to compare the proposed method, a DPD MP model (1) with the same parameters (K and M) was applied using the signals acquired by the two different receivers. Additionally, the DPD measurements were done using a single iteration for both receivers.

Fig. 9 presents the obtained results in terms of spectrum of the signal before and after DPD, amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM). All the acquisitions presented in Fig. 9 were performed using the VSA. Table II summarizes the results of ACPR and EVM for the measurements presented in Fig. 9, and also for the all the remaining evaluated carriers and bandwidths.

Considering the obtained results presented in Fig. 9 and Table II, it is possible to conclude that the proposed all-digital feedback receiver presents reasonable results when compared with a traditional one, both in terms of EVM and ACPR. Regarding the ACPR, it is important to state that the obtained results are always greater than 45 dBc, which fits the current LTE standard requirements. Additionally, the same is also

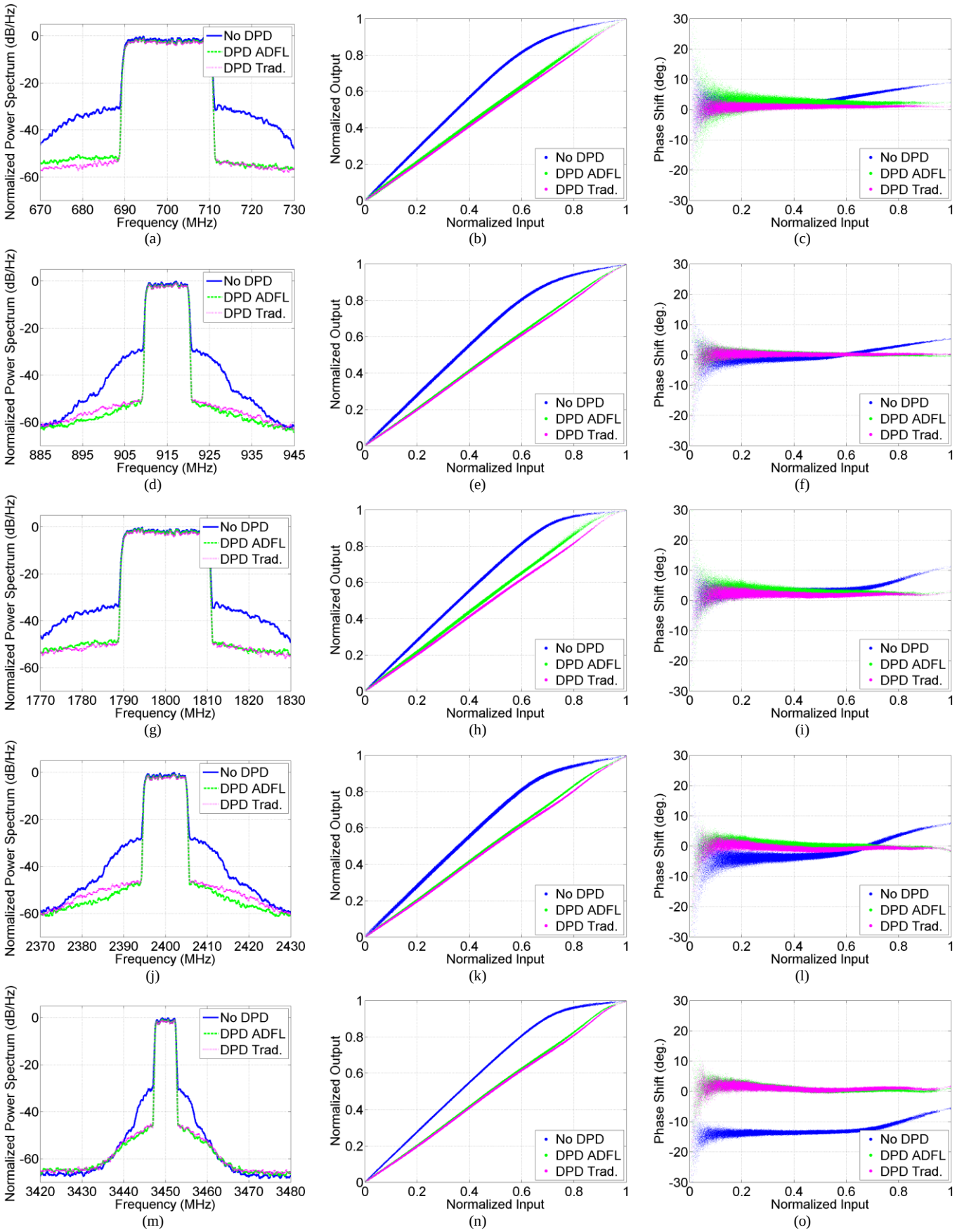

Fig. 9. DPD results: Spectrum before and after applying DPD with ADFL and with traditional one, AM-AM and AM-PM plots. (a)-(c) Results with f_c at 700 MHz and BW of 20 MHz. (d)-(f) Results with f_c at 915 MHz and BW of 10 MHz. (g)-(i) Results with f_c at 1800 MHz and BW of 20 MHz. (j).-(l) Results with f_c at 2400 MHz and BW of 10 MHz. (m)-(o) Results with f_c at 3450 MHz and BW of 5 MHz. [ADFL – all-digital feedback loop; Trad. – Traditional feedback loop].

valid for the EVM. Another important factor to note is the agility of the feedback loop, since the results show its feasibility from 700 MHz up to 3450 MHz Moreover, in a practical implementation, from the point of view of the feedback loop the change of carrier frequency only requires a different configuration of the NCO, which can be achieved in a few microseconds.

C. Scalability Evaluation

In the previous sub-Section the system was evaluated, showing its agility and feasibility to reach reasonable DPD metrics. Considering a C-RAN scenario where multiple RRHs share the same CU, the evaluation of the system's scalability is a very important metric.

In order to perform this evaluation, we will consider an implementation, with the same FPGA used in this work, the XCKU040-2FFVA1156E, which is the FPGA chip used in the KCU105 development board. The FPGA I/Os that allow to implement receivers such as the one presented in this work, are commonly known as Multi-Gigabit Transceiver (MGT). Each MGT allows to build a different receiver, i.e., a different dedicated feedback loop. The referred FPGA chip contains 20 MGTs, which would allow to implement 20 different feedback loops. Additionally, one may not forget the remaining powerful DSP capabilities that such a device could also bring. Therefore, the high scalability of such a system is another important advantage.

V. Conclusion

In this paper a new agile all-digital feedback loop receiver for PA linearization using DPD was presented and evaluated. The presented architecture is suitable for traditional RF transmitters and for future C-RAN scenarios, in which, the RRH is far from the baseband processing unit, i.e., the Central Unit (CU).

The proposed feedback loop, was evaluated in terms of ACPR and EVM, showing results capable to cope with the current LTE standard requirements. Several carrier frequencies and bandwidths were tested, showing the high versatility and agility of the system. Additionally, the system characteristics when used in a C-RAN scenario, present a very high scalability factor, while maintaining the same cost. All these features make the proposed system, attractive and suitable to be applied in the next-generation RAN architectures. However, it is important to refer that the distance between the RRH and the CU, may affect the DPD performance due to the optical link latency, which is a study that should be considered in future work.

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Paper C7: Towards Circulator-Free Multi Antenna Transmitters for 5G

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Towards Circulator-Free Multi Antenna Transmitters for 5G

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***Abstract*—Multi-antenna transmitters based on Massive MIMO and beamforming will be one of the 5G enabler technologies. To have suitable commercial architectures for these transmitters, they must be scalable, cost-effective, energy efficient and present a high-level of integration. This paper presents a technique where the circulator (bulky and expensive) is no longer required in the architecture. This paper also addresses the mutual coupling between antennas as one of the main problems associated with the circulator removal and identifies the PA load impedance variation, efficiency degradation, distortion generation and EVM degradation as severe consequences. To mitigate these problems, a digital compensation technique is proposed and verified with measurements in a laboratorial setup using 6W ultra-compact 2-stages MMIC PAs. The obtained results show that it is possible to remove the circulator and keep almost similar performance as in the single antenna operation mode.**

***Index Terms*—5G mobile communication, power amplifiers, digital pre-distortion, massive MIMO.**

I. Introduction

Multi-antenna transmitter architectures such as beamforming and Massive MIMO pose as strong candidates for both 5G and pre-5G (sub 6 GHz bands) systems. The use of these techniques allows the communication data throughput increase (parallel data streams and interference reduction) [1]. Both these techniques require a large number of concurrent transmitters, which immediately impose several challenges in terms of integration, scalability and cost.

Fig.1 depicts an example of a multi-antenna transmitter architecture based on the current Time Division Duplexing (TDD) LTE MIMO systems. Additionally, two receivers for data and another to perform linearization via digital predistortion (DPD) are also included. Since the power amplifier (PA) requires a stable load to operate properly, a circulator is used to isolate the PA output from the antenna and to reduce the input power level requirements of the switch. However, the future multi-antenna transmitters will not process individual high power but medium power signals. Therefore, an RF switch-based solution becomes feasible (blue part in Fig.1), being possible to remove the circulator and allowing for higher integration, scalability, reduced bill of materials and cost effectiveness.

Although, in the scope of a multi-antenna array transmitters, the circulator removal brings a new problem, which is the PA becomes affected by the mutual coupling between antennas [2]. This phenomenon will produce a variation in the antenna input impedance (i.e., PA load variation), which will cause the PA to decrease its performance (efficiency and linearity), and

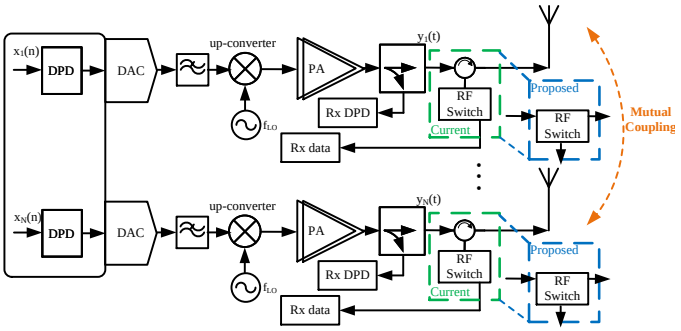


Fig. 1. Multi-antenna transmitter architecture based on conventional approach using circulators together with RF-switches, and proposed architecture using a single RF-switch (blue).

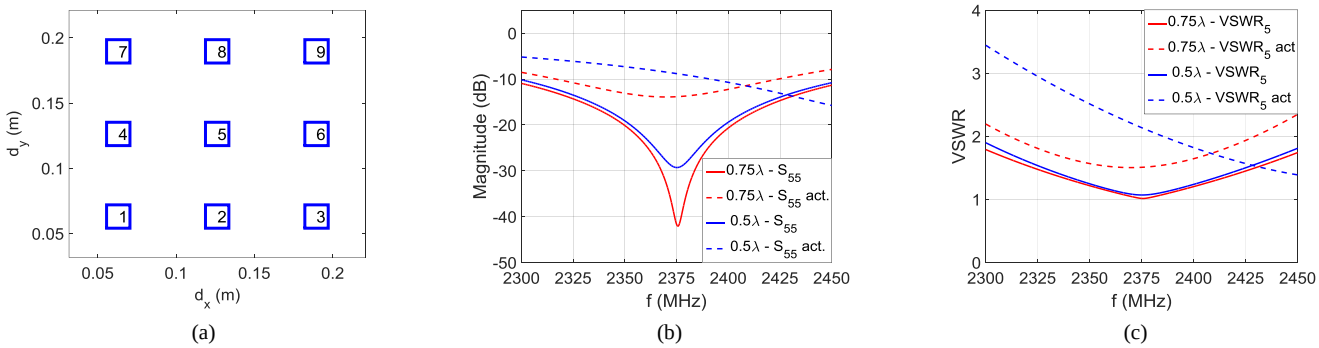
degrade the Error Vector Magnitude (EVM) of the transmitted signal. In [3] this problem was already verified in terms of non-linear effects depending on the distance between antennas. In [4] the mutual coupling effects were emulated by directly connecting two PAs using a variable attenuator, and metrics such as Adjacent Channel Power Ratio (ACPR) and EVM have been analyzed depending on attenuation.

In this paper, a generic DPD model that allows to linearize and to mitigate the mutual coupling effect will be presented and evaluated in a multi-antenna transmitter scenario where the mutual coupling is introduced by patch antennas. The remainder of this paper is divided as follows. Section II presents an example of the mutual coupling problem and its consequences in a 3x3 patch antenna array. Section III presents the digital compensation solution to solve the previous issues. Section IV presents the measurement results in a dual antenna configuration that corroborate the well-functioning of the proposed solution. Finally, some conclusions are drawn in Section V.

II. Mutual Coupling Problem

To exemplify the mutual coupling problem in an antenna array we will focus on a 3x3 patch antenna array simulated and designed in CST for fc = 2.375 GHz with equal horizontal (d_x) and vertical (d_y) distance between patches as depicted in Fig.2a).

It is important to define the single element input impedance, which is the one of a patch when individually excited. On the other hand, there is the active element input impedance (or scan impedance), which corresponds to the one of a given element when two or more elements are simultaneously excited [2]. This impedance variation depends on several factors



(a) (b) (c)

Fig. 2. a) 3x3 patch antenna. (b)-(c) Single element and active element (dashed line) input impedance in patch 5 in terms of S_{55} (magnitude) and VSWR.

such as, array configuration, spacing between elements and the phase difference applied at each element. In [2] it is shown that by knowing the S-parameter matrix of the array obtained with single individual excitations it is possible to find the active input impedance for a given simultaneously excitation.

Therefore, considering the array configuration of Fig.2a) and by applying the formulation presented in [2], the active input impedance can be computed. Fig.2b)-c) present both the single and active element input reflection coefficient in terms of magnitude and VSWR for the central patch antenna, which is the one more prone to this issue. Additionally, two cases are presented with dx=dy=0.75λ and dx=dy=0.5λ. Focusing on the VSWR, it is possible to verify that at fc it has suffered a variation from 1 to 1.5 in the 0.75λ case and from 1 to 2 in the 0.5λ case. This will obviously impose a new load to the PA and act as non-desirable load modulation that will degrade the overall transmitter performance when no isolator is present.

III. Digitally Compensation-Based Solution

Before presenting the proposed technique it's important to realize that there are also circuit-based techniques to design antennas in order to minimize the mutual coupling effect [5]. However, as also referred in [5], these solutions are usually complex and may result in narrowband matching performance. Additionally, increasing the space between antenna elements could be considered as the simplest solution. However, this immediately produces a negative impact in both radiation pattern as also in the array physical size, which is even more significant for the sub 6 GHz frequency bands.

The proposed solution to mitigate the previous referred problem is based on digital compensation performing both linearization via DPD and also compensation of the mutual coupling effect. From now on let us consider the fundamental signal as the signal that is intended to be transmitted in each patch and as interference signals to the signals that are coupled from the other patches. Considering that a feedback loop for DPD is available it is possible at the same time to extract a behavioral model for the PA and also to characterize the coupling response between each patch. After knowing this, it is possible to inject the summation of the opposite phase signal's that will appear at the load of the PA and cancel the mutual coupling effect and improve the Figures of Merit (FoM), such as efficiency, ACPR and EVM.

In fact, the currently existent DPD models for 2 transmitters MIMO scenarios, already allow to compensate for both non-linear and linear cross-talk [6], [7], therefore they can easily be used to implement this process. However, so far, these models are only conceived for two-transmitter scenarios, which brings the need to expand these models to a generic number of transmitters. Considering the Generalized Memory Polynomial for Linear Crosstalk (GMPLC) presented in [7], this can easily be adapted to a generic number of transmitters N, as follows:

$$y_1(n) = \sum_{l=1}^{N}\left[\sum_{m_1=0}^{M_1}\sum_{m_2=0}^{M_2}\sum_{k=0}^{\frac{K+1}{2}} h_{1l(m_1,m_2,k)}\, x_l(n-m_1)|x_l(n-m_1-m_2)|^{2k}\right] \quad (1)$$

where, N is the number of parallel transmitters, K is the non-linearity order defined for the polynomial, M_1 and M_2 are memory depths, $x_l(n)$ are the original signals at the input of each patch and $y_1(n)$ is the signal measured at the output of the PA of transmitter 1. The same process must be applied to the remaining N-1 transmitters. The presented model includes linear combinations between all the N transmitters.

IV. Measurement Results

To experimentally validate the proposed technique, a measurement setup with two concurrent transmitters was assembled (similar to Fig.1 architecture). This is composed by a dual-channel transmitter from TI (TSW38J84) and an RF ADC also from TI (ADC12J4000). Despite only two antennas were used several VSWR tests were performed. The PA used in each lane is a 6W ultra-compact 2-stages LDMOS MMIC Class-AB PA and the patch antennas were designed for fc at 2.375 GHz. The coupler was also designed to allow that the transfer function between the input to the coupled port and from the output to the coupled port present the same response. This is mandatory because the feedback loop must acquire a replica of the overall signal presented at the output of the PA (not possible with a standard coupler due to the isolation between the output and the coupled port). The signals used

TABLE I
SUMMARY OF RESULTS IN TX1.

	no DPD		SISO DPD		MIMO DPD		BO (7dB)		Cfg
Pout (dBm)	29.6		25.9		**26.0**		22.0		a
Eff. (%)	35.0		23.0		**23.0**		12.9		
ACPR (L/H) (dBc)	30/32		57/57		**57/58**		54/55		
EVM rms (%)	*		1.00		**1.07**		*		
PAPR (dB)	7.6	4.1	10	7.5	**10**	**7.5**	7.6	7.5	
Pout (dBm)	29.6		25.9		**26.1**		22		b
Eff. (%)	35.5		22.4		**23.0**		12.9		
ACPR (L/H) (dBc)	30/32		52/53		**55/55**		53/55		
EVM rms(%)	*		5.28		**0.92**		*		
PAPR (dB)	7.6	4.3	10	7.6	**11**	**7.5**	7.6	7.3	
Pout (dBm)	29.9		25.1		**25.9**		22.3		c
Eff. (%)	37.9		20.7		**22.0**		14		
ACPR (L/H) (dBc)	29/32		44/45		**52/51**		50/53		
EVM rms(%)	*		*		**1.38**		*		
PAPR (dB)	7.6	4.4	8.9	7.3	**11**	**7.6**	7.6	7.0	

*-not possible to demodulate and measure an EVM value.

during the measurements were 16-QAM modulated signals with 12 MHz bandwidth and approximately 8 dB of peak-to-average power ratio (PAPR).

Several different measurement scenarios were considered. Firstly, a measurement without the presence of any mutual coupling effect in which the PAs are individually (and one at a time) connected to each antenna. These measurements will give the best reference FoMs (configuration (config.) (a)), and are similar to the ones obtained if a circulator would be used. Secondly, it is necessary to test in a mutual coupling scenario, in which the antennas are placed side-by-side spaced of 0.5λ (config. (b)). This scenario corresponds to a VSWR about 1.2. The last scenario is solely aimed to test a higher VSWR condition in which the antennas are placed face-to-face (config. (c)). This is not a real practical scenario, however allows to mimic the same VSWR existent in the central patch of a 3x3 array antenna. Additionally, several measurements were taken considering no DPD applied, SISO GMP DPD algorithm, MIMO DPD algorithm (1) and back-off (BO) scenario (corresponding to the same linearity (ACPR) achieved with DPD).

Table I summarizes the obtained measurements results of the most important FoMs, considering the previously described scenarios, for the transmitter 1 (transmitter 2 has similar results).

As expected, in the config. (a), without any mutual-coupling, both algorithms present similar results. In the config. (b), light coupling, the MIMO algorithm is able to achieve better FoMs than with a common SISO algorithm. Comparing the MIMO algorithm with the BO operation, it is possible to conclude that despite similar linearity is achieved, the average efficiency using the proposed technique is about 44% higher (12.9% to 23%) and the EVM is lower than 1%. Moreover, the average efficiency value was restored to the same value as in single antenna excitation (config. (a)), which means that the interference waveform was completed eliminated. Focusing

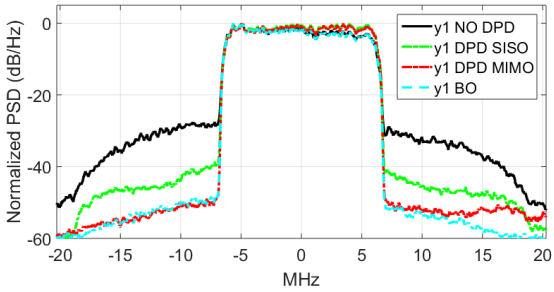


Fig. 4. Spectrum of the signals for each different test at the coupled port.

now on the config. (c), heavy coupling, one may realize that the SISO model is not even able to reach 45 dBc of ACPR. On the other hand, the proposed method is able to keep reasonable performance in all the FoMs, while keeping the leverage over the BO operation in terms of average efficiency and EVM. Additionally, Fig.4 presents the spectrum of the measured signals at the coupled port of the PA 1 for the config. (c).

Finally, it is also important to assess how this solution behaves in terms of digital signal processing complexity, which in this case will be evaluated regarding the number of coefficients. By inspecting (1), it is possible to realize that comparing with the SISO GMP the number of coefficients increase by a factor of N. Considering both configs. (a) and (b) of Table I (in which, K=9, M_1=3 and M_2 =1) the number of coefficients in the MIMO DPD (80) is twice of the number in SISO algorithm (40). However, with the increase of the mutual coupling in the config. (c) and to keep the same level of performance it was necessary to add an additional non-linear cross-term $(x_i(n)|x_j(n)|^2, i \neq j)$ to the MIMO model reaching to 88 coefficients.

V. CONCLUSION

In this paper a solution to remove the circulator on multi-antenna transmitters was proposed. The solution is based on pre-compensation in the digital domain allowing at the same time to linearize and to mitigate the mutual coupling effect.

The proposed technique was validated in a setup with two antennas where different VSWRs were emulated and evaluating important FoMs before and after applying digital compensation.

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