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Configurable Operational Amplifier Architectures based on Oxide Resistive RAMs

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This paper introduces memristor-based operational amplifiers in which semiconductor resistors are suppressed and replaced by memristors. The ability of the memristive elements to hold several resistance states is exploited to design programmable closed-loop operational amplifiers. An inverting operational amplifier, an integrator and a differentiator are studied. Such designs are developed based on a calibrated memristor model, and offer dynamic configurability to realize different gains and corner frequencies at reduced chip area.

Keywords: Memristor; Opamps; RRAM, Analog calibration.

[*] Typeset names in 8 pt Times Roman. Use the footnote to indicate the present or permanent address of the author.
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1. Introduction

Emerging technologies such as Resistive RAMs (RRAMs) are attracting significant attention, due to their interesting characteristics such as high integration density, CMOS compatibility and non-volatility to replace the current conventional memories [1] [2] [3]. A typical RRAM device consists of two metallic electrodes that sandwich a thin dielectric layer used for permanent storage. Oxide-based Resistive Random Access Memory (so-called OxRAM) uses transition metal oxides as a dielectric layer. Metal oxides such as HfO_2, NiO, TiO_2 and TaO_2 are promising candidates due to their compatibility with CMOS processes. In this study, an HfO_2 oxide-based RAM stack is considered.

A recent advance in the field of OxRAM memories is related to Multi Level Cell operation (MLC) [4] [5]. According to this approach, more than two data states are made possible for each memory cell, simply by finely controlling the programming of the cell. Proposed memristor-based operational amplifier (OpAmp) topologies use OxRAM cells as analog programmable devices by exploiting all the resistance states of the memory cell (i.e. extension of the MLC approach). High voltages are used to program the OxRAM states during the OpAmp calibration and low voltages are applied across the OxRAM cell during the OpAmp operation. Thus, the state of the OxRAM does not change during the OpAmp operation. It is worth noting that a series of short pulses are applied across the OxRAM cell during the calibration process. Pulse switching in 10 ns is reported in the literature [6]. Narrow programming pulses are possible due to the excellent high speed switching characteristic of the OxRAM cell. This programming strategy allows an optimal control of the programmed resistance despite the intrinsic cell variability [7] [8].

The approach to use memristors in programmable analog circuits was suggested in [9]. However, the memristor emulator used for simulations was far from actual memristive devices and the memristor programming interface within the analog circuits was not discussed. In [10], an introductory idea of using memristive devices in an open-loop OpAmp for neuromorphic applications is presented. Simulations were performed based on a SPICE memristor model. Also in this case, the approach was too conceptual and far from actual memristive device implementations. In [11], an ultra-low power open-loop OpAmp was designed in a 0.18µm technology using a memristor-based compensation technique and the VTEAM model introduced in [12]. But no references to actual memristive devices was provided. In [13], the adoption of memristive elements to customize a sensor interface is proposed. However, the technical implementation of the memristive element as a trimming device is absent and the trimming methodology is not developed. Alternatively, in [14] Floating Gate (FG) non volatile devices are used as analog trim elements by controlling the amount of charges transferred onto the FG. However, this technique needs a specific fabrication process to implement FG devices.

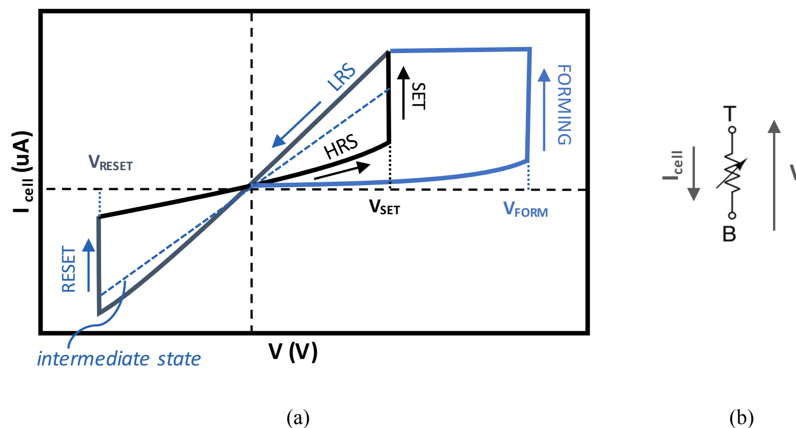
In this work, configurable closed-loop operational amplifiers are proposed based on a 130nm technology from ST-Microelectronics and an OxRAM model calibrated on

silicon. The analog storage feature of the OxRAM cell is evaluated based on actual data before its integration in operational amplifiers. A full design scheme targeting the implementation of OxRAMs as programmable analog devices within OpAmps is presented, including the OxRAM programming interface. This work is motivated by the greatest advantage of OxRAMs to be fabricated with low thermal budget, allowing their implementation into the Back-End-Of-the-Line (i.e. on top of CMOS transistors) with high integration density [15]. Moreover, as OxRAMs resistance can be programmed, closed-loop OpAmp parameters can be set dynamically.
The paper is organized as follows: section 2 presents the OxRAM technology, section 3 focuses on three configurable OpAmp architectures (inverting amplifier, integrator and differentiator) and provides simulation results and analysis. Finally, section 4 gives some concluding remarks.

2. Resistive RAM technology

2.1. *OxRAM memories*

In memory devices relying on a resistance change, complex physical mechanisms are responsible for reversible switching of the electrical conductivity between high and low resistance states. This resistivity change is generally attributed to the formation/dissolution of conductive paths between metallic electrodes [16].
OxRAM cell operation is depicted in Figure 1a. The resistance change is triggered when the voltage difference across the TOP and BOTTOM electrodes of the cell (labeled respectively “T” et “B” in Figure 1b) reaches specific voltages (namely $V_{SET,}$ V_{RESET} and V_{FORM}). SET operation is achieved by applying a voltage difference across the cell greater than the threshold V_{SET}. RESET operation is achieved by applying a voltage difference across the cell lower than the threshold V_{RESET}. To obtain intermediate ON and OFF states, programming can be done gradually by applying an increasing number of identical voltage pulses across the cell [17].



(a) (b)

Figure 1. (a) OxRAM I-V hysteresis and (b) OxRAM cell symbol

Before any SET/RESET operation, a FORMING operation is needed. The FORMING operation, achieved one time in the device life is a voltage-induced resistance switching from an initial virgin state with a very high resistance to a conductive state [18].
After FORMING, the OxRAM element can be reversibly switched between a High Resistance State (HRS or OFF state) and Low Resistance State (LRS or ON state). It is important to note that the FORMING stage is the first and most critical step as it determines the switching characteristics during the future operation of the memory cell. Also, a FORMING operation needs more important voltage values.

2.2. *OxRAM Model*

The proposed OxRAM modeling approach relies on electric field-induced creation/destruction of oxygen vacancies within the switching layer. The model enables continuously accounting for both SET and RESET operations into a single master equation in which the resistance is controlled by the radius of the conduction pathways (r_{CF}) [19]:

$$\frac{dr_{CF}}{dt} = \left(r_{CF\max} - r_{CF}\right)\cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea - q\cdot\alpha_{red}\cdot V_{cell}}{k_b\cdot T}} - r_{CF}\cdot 10^{\beta_{RedOx}} \cdot e^{-\frac{Ea + q\cdot\alpha_{ox}\cdot V_{cell}}{k_b\cdot T}} \quad (1)$$

where β_{RedOx} is the nominal oxide reduction rate, E_a is the activation energy, α_{red} and α_{ox} are the transfer coefficients (ranging between 0 and 1), k_b is the Boltzmann constant, r_{CFmax} is the maximal size of the conductive filament radius, T is the temperature and V_{cell} the voltage across the cell.
Moreover, the model makes assumptions of a uniform radius of the conduction pathways, a uniform electric field in the cell and temperature triggered acceleration of the oxide reduction reactions ("redox"). Finally, the total current in the OxRAM includes two components, i.e. one is related to the conductive species (I_{CF}) and the other to the conduction through the oxide (I_{OX}).

$$I_{CF} = \frac{V_{Cell}}{L_x}\cdot\left(\pi\cdot r_{CF}^2\cdot\left(\sigma_{CF} - \sigma_{OX}\right) + \pi\cdot r_{CF\max}^2\cdot\sigma_{OX}\right) \quad (2)$$

$$I_{OX} = A_{HRS}\cdot S_{Cell}\left(\frac{V_{Cell}}{L_x}\right)^{\beta_{HRS}} \quad (3)$$

where L_x is the oxide thickness, S_{Cell} is the total area of the device, σ_{Ox} the oxidation rate and σ_{CF} the reduction rate. To take into account I_{OX} trap assisted current (Poole-Frenkel, Schottky emission, Space Charge Limited Current (SCLC)), a power law between the cell current and the applied bias is considered with two parameters A_{HRS} and β_{HRS}. Finally, the total current flowing through the cell is given is by:

$$I_{Cell} = I_{CF} + I_{OX} \tag{4}$$

I_{CF} is the main contributor to LRS current (I_{LRS}) and I_{OX} is the main contributor to HRS current (I_{HRS}). The memory cell compact model is calibrated on silicon. The model was confronted to quasi-static and dynamic experimental data before its implementation in electrical circuit simulators. As presented in Figure 2a, after calibration, the model satisfactorily matches quasi-static and dynamic experimental data measured on actual HfO_2-based memory elements (TiN/Ti/HfO_x/TiN stack [20]). In Figure 2b, the evolution of SET voltages (V_{app}) as a function of the programming ramp speed is presented. The model implementation focused on this dependence which is crucial for the model to be confidently implemented in circuit simulators.

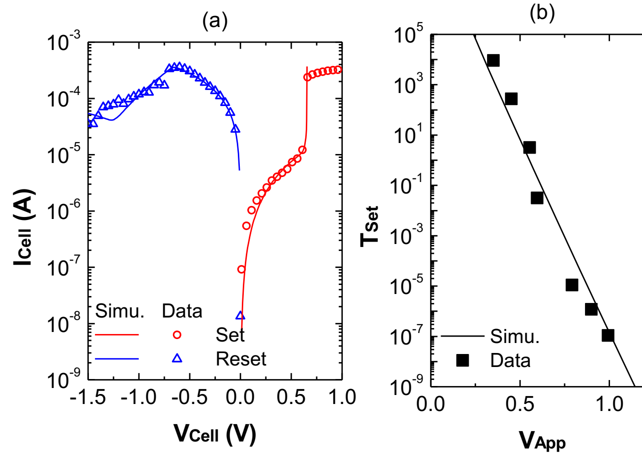
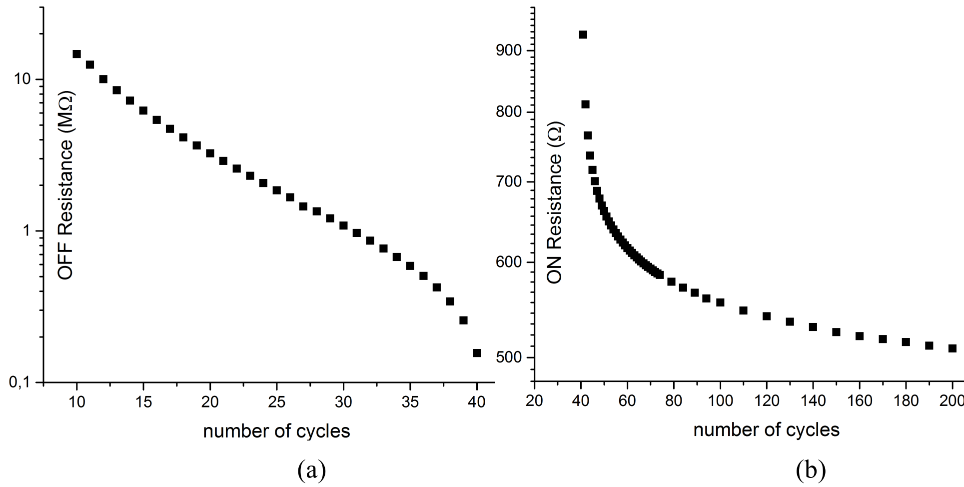


Figure 2. (a) I-V characteristic measured on HfO_2-based devices [20] and corresponding simulation using a bipolar OxRAM physical model. (b) SET voltage as a function of the programming ramp

2.3. *OxRAM operation as a programmable resistance*

To monitor the variation of the analog resistance, an analysis of the cell resistance variation after FORMING is performed. The memory cell is formed gradually by applying a series of short programming pulses across the OxRAM cell. The number of pulses is controlled by a programmable pulse generator. The pulse width is set to 50 ns within a period of 100 ns and the pulse level is set to 3 V. As a result, the resistance of cell decreases. Figure 3a presents the evolution of the HRS resistance versus the number of pulses. Figure 3b presents the LRS resistance versus the number of pulses. The resistive switching from HRS to LRS occurs at cycle number 40. HRS resistance variations are in the MΩ range [15MΩ - 156kΩ] and LRS resistance variations are in the 100 Ω range [955Ω - 500Ω]. This ability of the OxRAM memory cell to hold several resistance values is evaluated based on an OxRAM compact model calibrated on silicon [20] [21].



(a) (b)

Figure 3. (a) HRS resistance variation and (b) LRS resistance variation versus the number of pulse cycles

Several observations can be made. First, the abrupt change of the resistance (at cycle number 40) is a rapid phenomenon preventing the use of this area for resistance calibration purposes. In contrast, HRS and LRS resistance variations exhibit two interesting areas suitable for analog calibration: between programming cycles 14 and 40 for the HRS resistance and between cycles 45 and 200 for the LRS resistance. The second observation is related to the capacity of the cell to be reset after a FORMING/SET operation (i.e. change of the resistance value from a low impedance state to a high impedance state) allowing a restart of the calibration process. A third observation is related to the resistance step variation which can be decreased or increased by modulating the programming pulse width and level, allowing a fine tune of the cell resistance. Moreover, as the OxRAM memory state is comparable to a simple resistance, no refresh of the cell is needed (i.e. the cell resistance maintains its value).

3. Configurable Operational Amplifier Topologies

3.1. *Open-loop amplifier*

Figure 4 shows the circuit diagram of a two-stage CMOS amplifier [22]. The first stage consists of a n-channel differential pair M1-M2 associated with a p-channel current mirror load M3-M4 and a n-channel tail current source M5. The second stage consists of a p-channel amplifier M6 associated with a n-channel current-source load M7. The high output resistances of these two transistors provide a relatively large gain for this stage and an overall moderate gain for the complete amplifier. Since multi-stage amplifiers have more poles and zeroes than single-stage amplifiers, all multi-stage amplifiers suffer closed-loop stability problems. One common compensation technique requires placing a

compensation capacitor C_C between the input and the output nodes of the second stage and a low value resistor represented by M_C placed in series with the capacitor. The main amplifier parameters obtained after simulations are presented in Table 1.

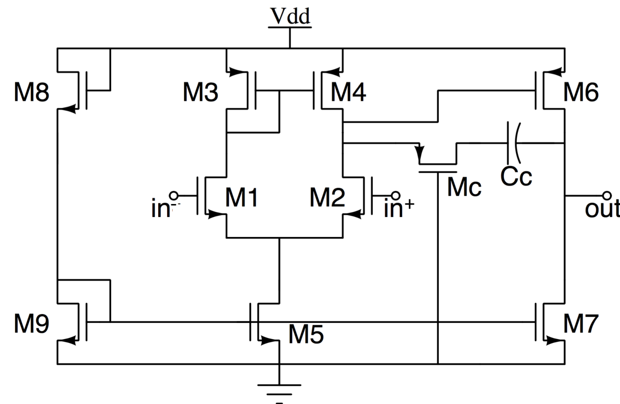


Figure 4. Two-stage CMOS amplifier

Table 1. CMOS operational amplifier parameters

Parameter	Value[a]
DC supply (V)	1.8
Technology (nm)	130
Open loop gain (dB)	72
Output swing (V)	1.2
Slew-rate (V/µs)	10
Phase margin (Degree)	75
CMRR (dB)	80
Power consumption (µ*W*)	150

[a] Evaluated with a 5pF load

3.2. *Configurable closed-loop inverting amplifier*

Based on the amplifier presented in Figure 4, a closed-loop inverting OpAmp configuration is built and presented in Figure 5a. In Figure 5a the feedback resistance R2 and the input resistance R1 of the classical inverting OpAmp are replaced by OxRAM cells.

The OpAmp including its programming interface is presented in Figure 5b. In OpAmp calibration mode, the programming interface is activated when the EN signal is set High. In the same time transmission gates S1 and S2 disconnect the OpAmp output and isolate the OpAmp input from the rest of the circuit. Then, SET and RESET pulses are applied across the cell through the 3-state buffers in order to program dynamically and independently each OxRAM cell. Table 2 presents the different voltage levels to apply across R1 and R2 to perform "soft" SET/RESET operations. Note that the OxRAM bottom electrode B is shared between R1 and R2 allowing the use of only one RESET

signal. Regarding the calibration speed, the calibration process is not time consuming as a series of short pulses are applied across the cell.
In OpAmp normal operation mode, OxRAM cells behave as conventional resistances, and voltages across the cells are always below OxRAM programming voltages. Indeed, the input voltage is meant to be low and the OpAmp output swing voltage is limited to 1.2V as presented in Table 1.

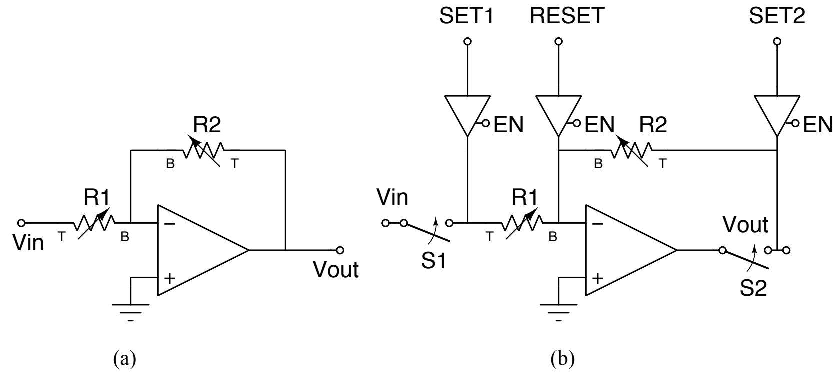


Figure 5. (a) OxRAM-based inverting OpAmp (b) OxRAM-based inverting OpAmp with programming interface

Table 2. SET/RESET voltage levels

OxRAM input signals				
SET1	RESET	SET2	OxRAM States	# Configuration
L	L	L	*no effect*	1
L	L	H	R2 SET	2
L	H	L	R1 & R2 RESET	3
L	H	H	R1 RESET	4
H	L	L	R1 SET	5
H	L	H	R1 & R2 SET	6
H	H	L	R2 RESET	7
H	H	H	*no effect*	8

According to Figure 3 and as mentioned in section 2.3, HRS resistance variation is in the MΩ range [15MΩ - 156kΩ] and LRS resistance variation is in the range [955Ω - 500Ω]. The gain of the open-loop OpAmp presented in Figure 5 is equal to -R2/R1. Thereby, the gain of the OpAmp can be adjusted dynamically after changing R1 and R2 resistance states.
As an application example, let's consider configuration 3 of Table 2. In this configuration, R1 and R2 are reset to 250kΩ after applying a series of 39 programming pulses across both OxRAM cells (HRS resistance variation versus the number of pulses is given in Figure 3a). As expected, a unity gain is provided by the OpAmp. Then, only R1 is set to

662Ω after 50 programming cycles according to configuration 2 of Table 2 (LRS resistance variation versus the number of pulses is given in Figure 3b). A new gain equals to 377 is now provided by the OpAmp. This gain can be increased dynamically by increasing the number of pulses applied across R1. Figure 6 presents the evolution of the OpAmp gain versus the number of programming pulses. The gain variation is in the range [377 – 490].

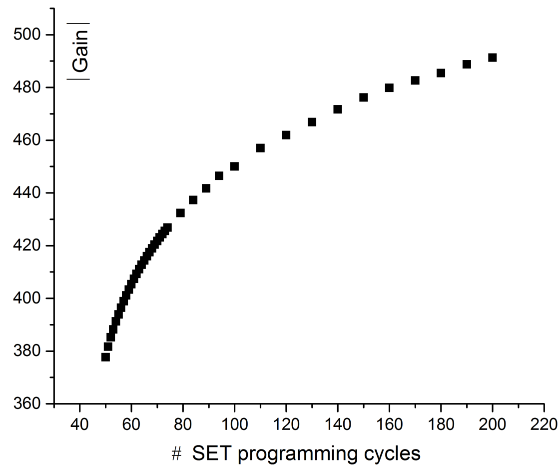
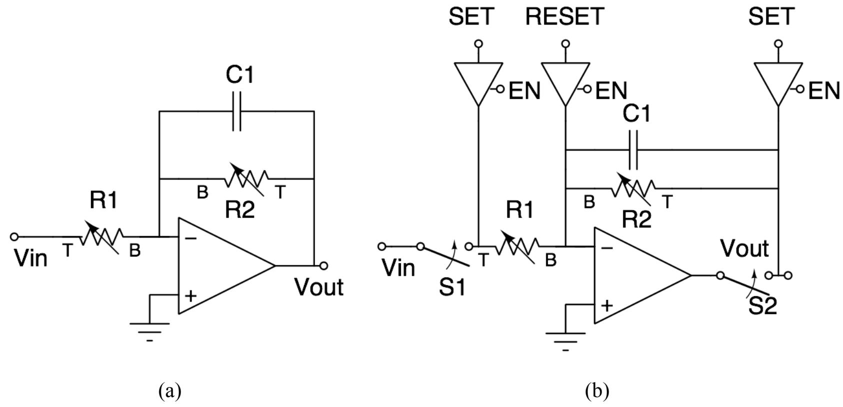


Figure 6. Absolute value of the OpAmp gain (|-R2/R1|) versus the number of pulses applied across R1

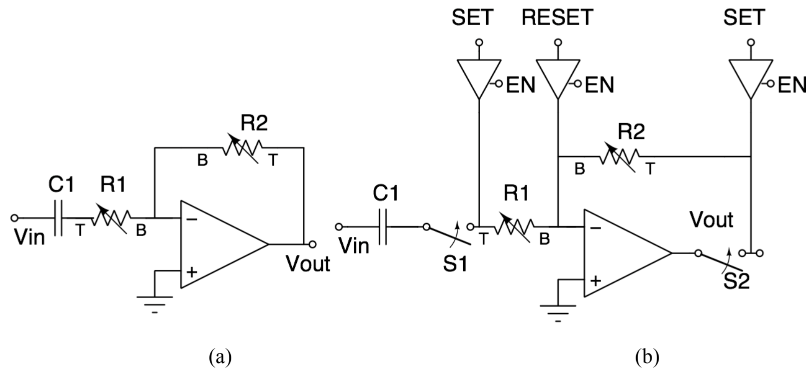
3.3. *Configurable integrator and differentiator*

Figure 7a presents the classical OpAmp integrator circuit where resistances are replaced by OxRAM cells. The input resistance of the integrator is replaced by the OxRAM cell R1 and the feedback resistance, connected in parallel with capacitor C1, is replaced by the OxRAM cell R2. The feedback resistor R2 gives the circuit the characteristics of an inverting amplifier with a finite closed-loop gain of R2/R1. At very low frequencies the circuit acts as a standard integrator, while at higher frequencies the capacitor shorts out R2 due to the effects of capacitive reactance, reducing the amplifier gain and making the circuit to behave as a Low Pass Filter (LPF). The OpAmp including its programming interface is presented in Figure 7b.



(a) (b)

Figure 7. (a) OxRAM-based integrator (b) OxRAM-based integrator with the programming interface



(a) (b)

Figure 8. (a) OxRAM-based differentiator (b) OxRAM-based differentiator with the programming interface

Figure 8a presents the classical OpAmp differentiator circuit where resistances are replaced by OxRAM cells R1 and R2. In order to reduce the overall closed-loop gain at high frequencies, the extra input resistor R1 was added to the input, limiting the differentiator increase in gain at a ratio of R2/R1. At low frequencies, the circuit acts as a differentiator amplifier making the circuit to behave as a High Pass Filter (HPF). The OpAmp including its programming interface is presented in Figure 8b.

For both integrator and differentiator, capacitor C1 value is set to 159nF and R1 and R2 are programmed in parallel (i.e. R1 and R2 are programmed to the same value). Figure 9 presents the frequency response (Bode plot) of the integrator and differentiator after a RESET operation for an HRS resistance variation in the range [0.5MΩ – 5MΩ]. The evolution of the corner frequency versus the resistance variation is extracted from Figure 9 and presented in Figure 10 for the integrator and differentiator. The theoretical corner frequency is also added for comparison purposes, demonstrating the proper operation of

the configurable OpAmps. It is worth noting that the corner frequency variation is in the range [0.24kHz - 2.4kHz] with respect to R1 and R2 variations.

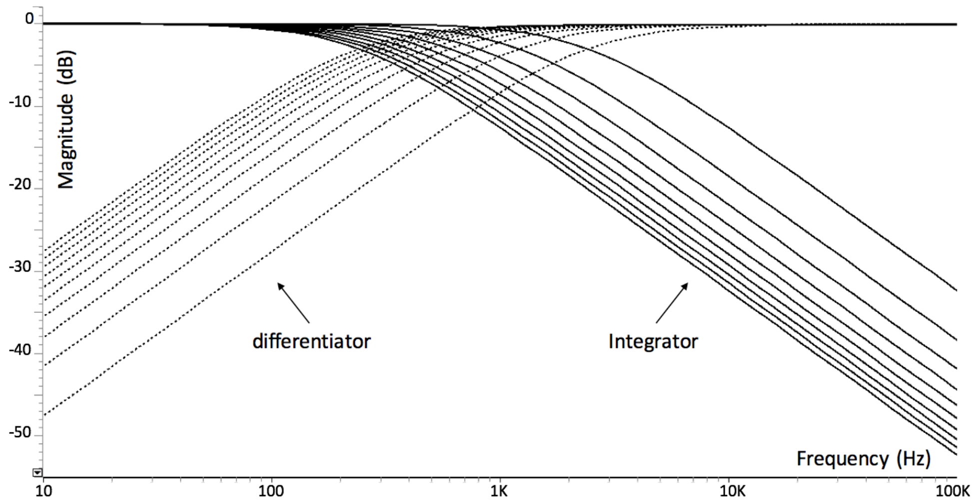


Figure 9. Frequency response of the integrator and differentiator versus R1 and R2 resistance variation in the range [0.5MΩ – 5MΩ].

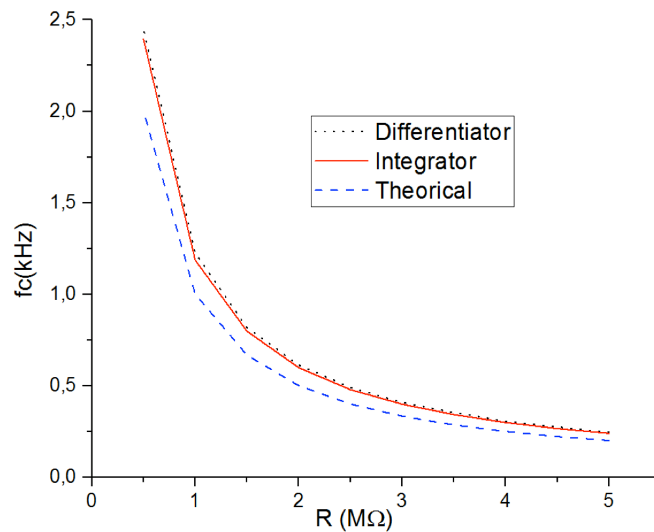


Figure 10. Differentiator, integrator and theorical corner frequency fc versus resistance variation (R1 and R2)

Finally, to check the integrator and differentiator functionality, transient simulations are performed. Figure 11 presents the integrator transient responses. If we apply a constantly changing signal such as a sine-wave (Figure 11a) or a triangular wave (Figure 11b), the

resultant output signals are integrated (i.e. the resultant output signals change according to the RC time constant of the Resistor/Capacitor combination).
Figure 12 presents the differentiator transient responses. When applying a constantly changing signal such as a sine-wave (Figure 12a) or a triangular wave (Figure 12b) to the input of the differentiator circuit, the resultant output signals are respectively a cosine wave and a rectangular wave, demonstrating the differentiation capability of the circuit.

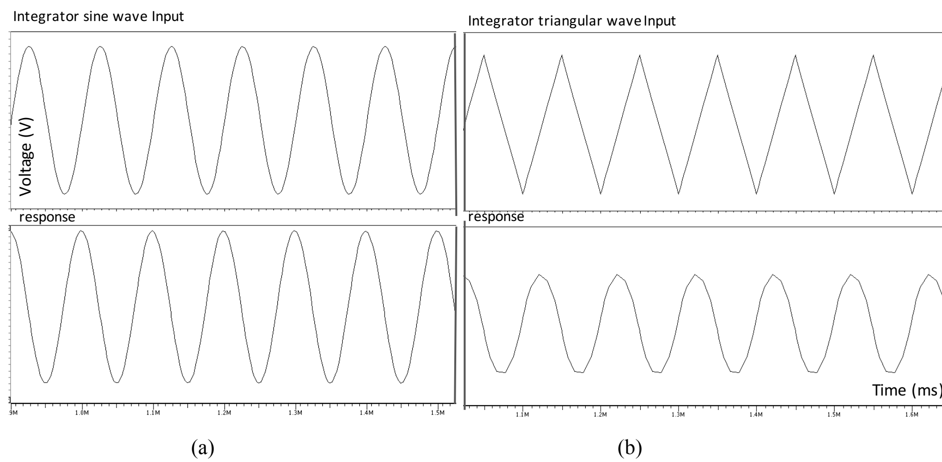


Figure 11. Transient simulation results of the integrator for (a) sine wave and (b) triangular wave inputs

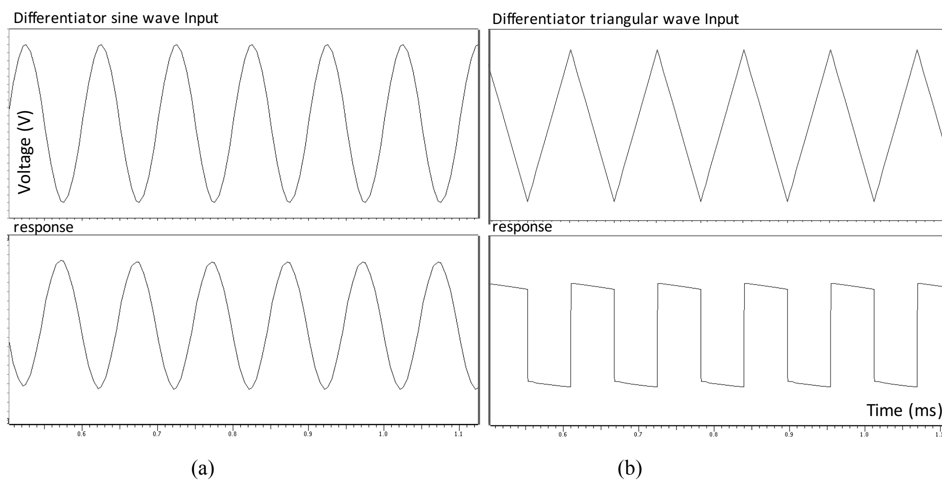


Figure 12. Transient simulation results of the differentiator for (a) sine wave and (b) triangular wave inputs

3.4. *Discussion*

In the presented OpAmp calibration methodology, the memristive device is programmed to a desired resistance prior to the operation of the amplifier. To achieve a proper programming of the OxRAM cells, 3 additional three-state buffers and 2 pass-gates are added to the conventional closed-loop OpAmp designs. These additional components impact performances of the closed-loop OpAmps by introducing a slight voltage drop (< 0.1mV) at the OpAmp inputs. This voltage drop can be reduced by oversizing the pass gates or by modulating R1/R2 resistance ratio.
Benefits of the presented methodology are related to the suppression of semiconductor resistances usually implemented in closed-loop OpAmp topologies. Moreover, an in-circuit resistance calibration feature is provided. Another important aspect of the presented work is the use of actual memristive devices (HfO_2 OxRAM stack model calibrated on silicon) combined with a programming interface designed in a 130 nm High Voltage (HV) CMOS technology. The HV technology is chosen to allow the use of thick-gate-oxide transistors able to sustain OxRAM programming voltages.

4. Conclusion

Memristive devices provide an inspiring variety of opportunities for circuit designers. In the presented approach, OxRAM based memristive devices are programmed to a desired resistance value prior to their operation within closed-loop OpAmps (i.e. inverting amplifiers, integrators and differentiators). The OxRAM cells operate in such a way that in the analog mode of operation (when the OxRAM performs a useful function as an analog circuit element) only voltages of small magnitude (0-1.2V) are applied to the device, while higher-amplitude voltages are used only for programming (~3V). The final closed-loop OpAmps feature a programmable gain and corner frequency while suppressing the use of semiconductor resistances.

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