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A Single Chip Computational Sensor System for Neutron Detection Applications

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Nathan Schemm, Sina Balkır, Michael W. Hoffman, Mark Bauer, David Schultz, James C. Petrosky, John W. McClory, Marcus Natta, Jennifer I. Brand, Jinke Tang, and Wendong Wang

***Abstract*—This paper presents the design and test results of a standalone computational radiation sensor system based on a single chip solution. A low-power sensor front end with a charge sensitive amplifier and an event driven analog-to-digital converter is integrated on the same chip as a dedicated microcontroller to process and bin the data from the neutron detector diode heterojunction according to pulse height. This combination effectively implements a single chip multichannel analyzer with the capability to do further processing of the data in software. The design was fabricated in a 0.18 μm CMOS technology with field tests demonstrating the validity of the approaches taken. The total system power consumption is 24 μW.**

***Index Terms*—Computational sensor, gadolinium, hafnium oxide, multichannel analyzer, neutron detection, radiation detector.**

I. Introduction

THE detection of radioactive materials is an important sensor application that requires a data acquisition and processing system for reliable and low-power operation. In such an application, low-power operation becomes a key issue in order to achieve maximum battery life. While low-power circuit design techniques can provide a degree of battery life extension, the transmission of a single information bit still requires power that is equivalent to thousands of digital computations. Hence, a key challenge is the mitigation of energy usage for data transmission through on-sensor computation. Integrating sensing with computation and shifting critical computations to an on-board processor can minimize the amount of raw data to be transmitted from the sensor output. This paradigm can lead to significant reduction in sensor system power requirements.

To that end, the design, fabrication and test of a complete computational radiation sensor system with on board processing is presented in this paper. The design integrates a custom low-power microcontroller core, I/O hardware, timers, SRAM, and a bank of quad low-power front ends on a single chip using a 0.18 μm CMOS technology. The front end design is based on a novel charge sensitive amplifier (CSA) which has a significant reduction in power consumption. As compared to earlier work in the open literature [1]–[5], this new design allows the peak current available to the CSA to be more than 20 times the dc bias level by dynamically scaling the bias current during a neutron detection event. This allows the amplifier to remain in the linear region for more accurate detection.

The electronic circuit design migrates the following critical computation tasks of detection into the sensor head: Counting the neutron events, energy bin classification of captured neutrons and pulse height spectra computation, and the dissemination of the results with minimal redundancy. Hence, the presented computational radiation sensor effectively acts as a low bit-rate information source. The single chip solution leads to a fully functional miniaturized radiation sensor, which is a significant improvement over past work on handheld detectors [1] or more cumbersome industry standard NIM or CAMAC bench or rack instrumentation. Furthermore, integrating everything on a single chip, including the processor and power supply, allows for very tight integration of the system components leading to a lower power consumption and smaller size than an alternate solution using some off-the-shelf components.

In Section II, the architecture of the system is described. Section III presents the fabrication of the complete system and the associated test bed development. Various lab and field test results are presented Section IV. Finally, Section V concludes this paper.

II. Computational Radiation Sensor Architecture

The design choices have been mainly driven by low power of operation, small area, reliable communication, and robustness constraints. The overall sensor architecture is displayed in Fig. 1. In particular, the sensor analog front end, event driven analog-to-digital converter (ADC), microcontroller core and its

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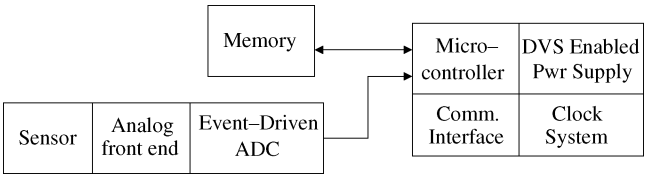

Fig. 1. Computational radiation sensor architecture. The blocks shown comprise the computational radiation sensor and have been included in a test chip using a 0.18 μm CMOS technology.

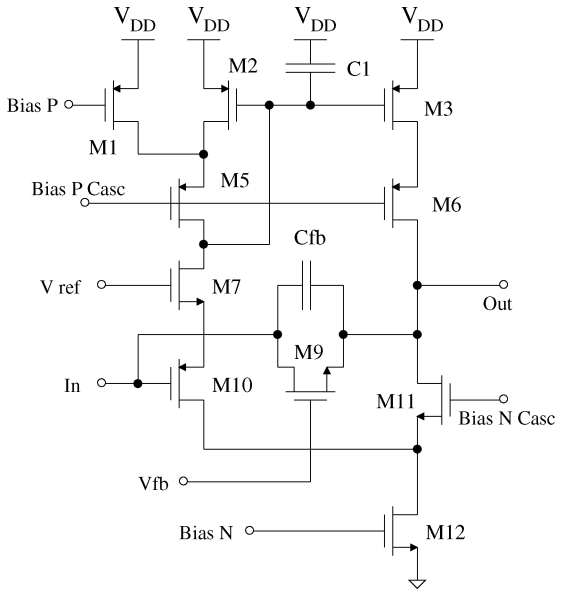

Fig. 2. CSA topology dynamically scales the dc bias current [6].

associated peripherals have been designed and included in a test chip.

A customized and dedicated low-power microcontroller core, memory, I/O hardware, timers, a low-power analog front end with quad charge sense amplifiers and ADC are housed in this test chip.

- *Sensor analog front end:* A circuit using an adaptive biasing scheme that results in significantly reduced power consumption has been developed. The front end is based on a CSA, and its power consumption is critical due to the always-on nature of the neutron sensor. The schematic of the low-power CSA is shown in Fig. 2 [6]. The core of the amplifier is based on a folded cascode circuit configuration. The dc operating currents are set at 1.5 μA through M12 and 0.75 μA through both M10 and M11. The mirroring gain from transistor M2 to M3 is 30. Hence, in the dc case, most of the current through M5 is diverted away from the mirror M2 and instead flows through M1. M1 is present exclusively to increase the dc current through the input transistor M10 and therefore decreases noise. C1 is required for stability. By carefully selecting the bias voltages, a wide swing can be obtained. During a particle detection event, the small signal current through M10 increases. As in a conventional folded cascode configuration, the current through M11 then decreases. The current through M2 also increases, which is amplified by the mirroring gain from transistor M2 to M3, before being applied to the output. Thus, the bias current is dynamically scaled during a particle detection event and the peak current is allowed to be more than 20 times the dc bias level by utilizing this adaptive bias scheme. This mechanism permits the amplifier to stay in the linear region allowing more accurate characterization of detection events.
  The output swing can be as large as $\mathrm{V_{DD}} - 4\mathrm{V_{ov}}$, where $\mathrm{V_{ov}}$ is the overdrive voltage of the transistors. The dc output level is controlled by Vref. The closed loop charge-to-voltage conversion gain can be approximated as $1/\mathrm{Cfb}$, where Cfb is adjustable in this design to range from 0.2 pF to 15.2 pF in 1 pF increments. The time constant of the circuit can be tuned by adjusting the voltage Vfb.
- *Integration of sensor front end with an event driven ADC:* A block diagram of the completely developed sensor front end is shown in Fig. 3. The programmability of the front end is implemented via DACs to control the detection threshold and the feedback resistor value. The adjustable feedback capacitor is also shown. Following the CSA, a peak detector circuit captures the peak value of each detection event which is then converted to a digital value via an 8 bit charge-redistribution successive approximation ADC. The comparator Cmp 1 detects when the CSA output goes above its normal quiescent point. When this happens, the ADC trigger line goes low. This also turns M1 and Cp into a peak detector. Internally, the ADC begins to power up and track the input. After the particle event, the ADC begins its conversion on the peak value, and the peak detector returns to tracking the input again. Cc is used to eliminate the dc bias present on the CSA output. The ADC is shut off in between detection events to further reduce power consumption. Fig. 3 shows the architecture of the ADC. It is a standard successive approximation architecture with a buffer on the front and an input signal range from 0 to Ref. It uses a clocked comparator which minimizes power consumption, and the input buffer is shut off after the sampling stage to further conserve power. Not shown, a digital section for the ADC controls the switches to sequence the conversion.
  Initial work on the development of the complete low-power front end section for particle detection applications was presented by the authors in [7]. While the earlier work was based on a prototype development using a 0.35 μm CMOS technology, the current design is based on a 0.18 μm CMOS technology with significant reduction in power consumption and overall performance improvement in the circuit specifications. In the current design, the entire circuit consumes between 4 μW and 20 μW of power depending on the particle detection rate. The peak ADC conversion rate, and therefore particle detection rate, is 400 K samples per second. The conversion energy is 75 pJ per conversion. This low-power operation enables the development of compact, long-life, battery powered, remote particle sensors.
  The digital interface for the ADC consists of a 16 byte FIFO buffer. This is present to decrease the frequency at which the processor must be interrupted to process the neutron detection events. This is important when using dy-

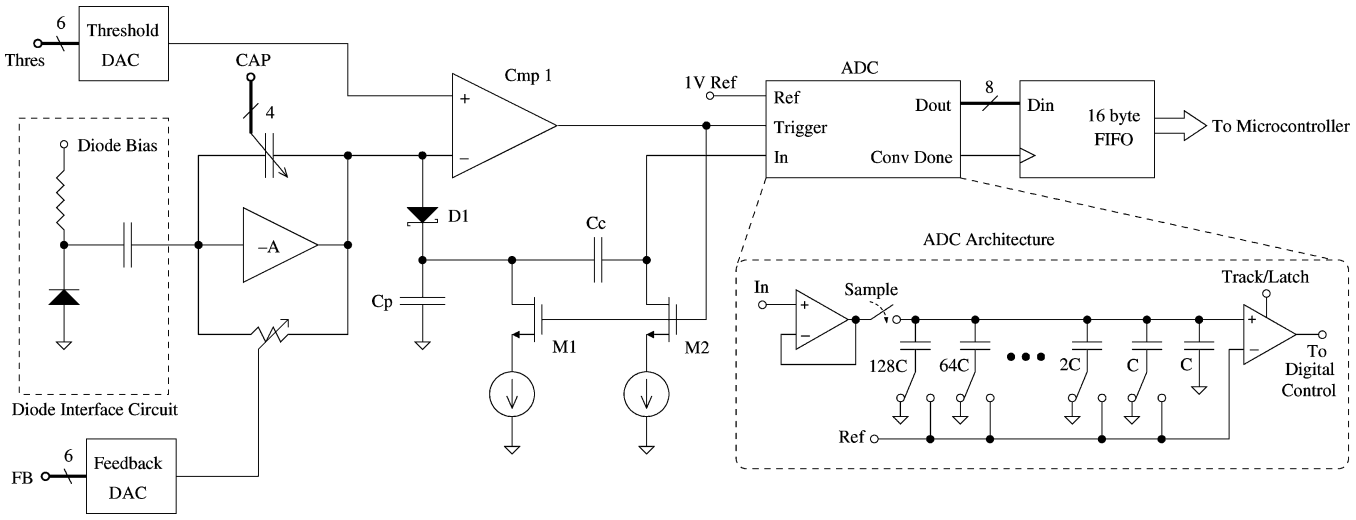

Fig. 3. Overall sensor front end.

namic voltage scaling (DVS), as energy is consumed each time the processor supply voltage must be increased from its sleep voltage to its operating voltage. The FIFO is also more tolerant of the interrupt processing delay introduced by the DVS. This delay stems from the fact that the processor must wait for the supply voltage to reach its proper value before commencing interrupt routine execution.

- *Custom low-power microcontroller core:* The core is responsible for processing the particle events and storing and transmitting the data to a host system. The main design constraints for the processor are power consumption and silicon area. To this end, a simple 16 bit RISC processor has been modeled in RTL-level VHDL. To simplify the design, only a small instruction set consisting of 28 instructions has been implemented. The design uses a Von Neumann architecture without any instruction pipeline. The processor executes almost all instructions in the same number of clock cycles as the number of memory accesses which are required by the instruction with a peak clock speed of 60 MHz when operating at the maximum voltage of 1.8 V. The dynamic voltage scaling capability can be utilized to trade off peak processor speed for power consumption. The processor will operate down to a supply voltage of 900 mV. The processor supports a two priority interrupt structure with interrupts generated either externally or by internal modules. The processor contains 9000 gates with the silicon area dedicated to the processor core of 0.08 mm^2. Also included are resources for various serial communication protocols, timers for timekeeping functions, I/O resources, and system control.
- *Power supply and support circuitry:* Two buck power supplies are integrated on the chip to supply power efficiently to the digital and analog circuitry. One buck regulator has a 1.8 V fixed output to supply the analog circuits, and the other supplies the core voltage and supports dynamic voltage scaling. Buck regulators were chosen over linear regulators because they can supply the required voltages efficiently from a 3 V battery. Using a buck regulator allows the one to fully realize the power savings gained from DVS. Ideally, using DVS, the power consumption should scale quadratically as the supply voltage. If using a linear regulator, the power only scales linearly with the supply voltage. The difference is due to the efficiency of the linear regulator decreasing linearly as the supply voltage is scaled. However, the efficiency of buck regulator remains approximately constant. Therefore the buck regulator can reap twice the benefits from DVS (in dB) over a linear regulator. Each buck regulator requires an off-chip inductor and capacitor.

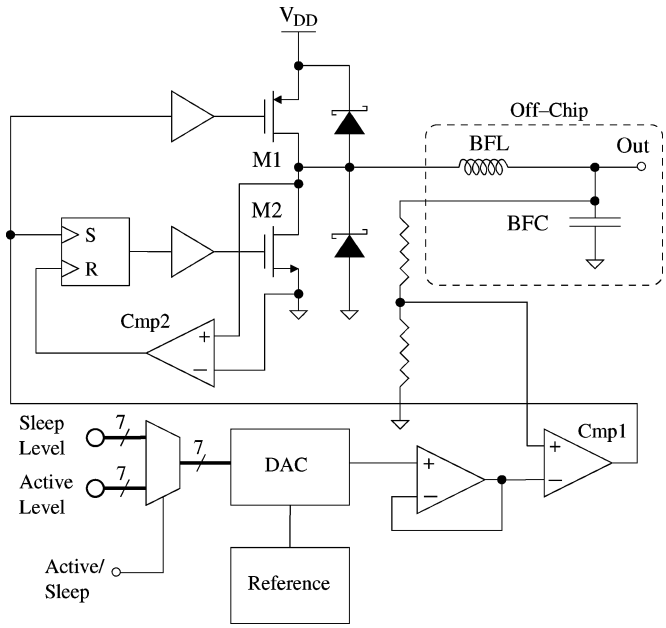

Fig. 4. Low-power buck regulator with DVS [8].

The buck regulators must be designed to efficiently supply a very small output current. The regulators utilize a very simple pulse frequency modulation scheme which allows very high efficiency even at very low loads. Fig. 4 shows the regulator architecture. The comparator Cmp1 is responsible for keeping the output in regulation, while Cmp2

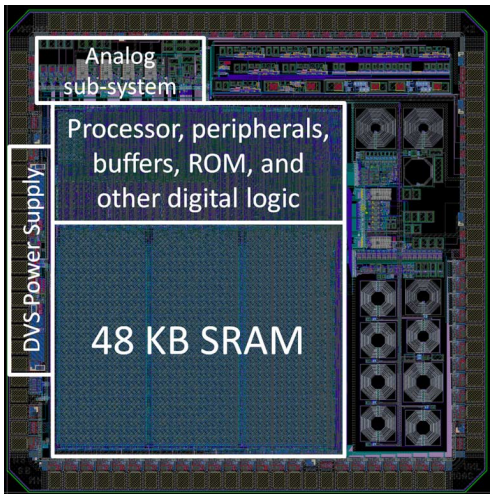

Fig. 5. Overall computational sensor chip layout.

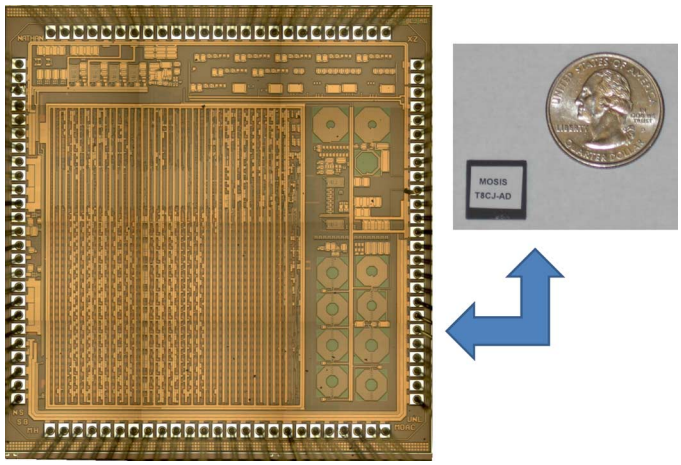

Fig. 6. Fabricated computational sensor chip.

shuts off M2 when the current through it drops to zero. The DAC allows the output voltage to be changed, and the following buffer has a slow slew rate to implement soft-start. The complete design is presented in [8].

A clock system is also required. A low-power 32 kHz crystal oscillator similar to that presented in [9] is used as the time base. This is the only active clock for the majority of the time. This is used to schedule processor wakeup intervals and timekeeping functions. The ADC generates its own internal clock when needed, so it does not require a system clock. When the processor is active, a digitally controlled oscillator is used as the system clock. This low-power oscillator starts up very quickly, and is internally stabilized by the 32 kHz crystal oscillator.

These blocks comprise the computational radiation sensor. Fig. 5 displays the layout of the main functional sections of the chip.

III. Fabrication of Computational Radiation Sensor Section and Test Bed Development

A 3 mm $\times$ 3 mm chip based on a 0.18 μm CMOS technology, containing the blocks indicated in the previous section has been fabricated. Fig. 6 displays the die photo of the fabricated chip. The test bed architecture for the chip is shown in Fig. 7. This includes an interface to the external semiconductor diode neutron sensors as well as an interface to the computer via a USB to serial communications device. The serial flash stores the program for the internal RISC microcontroller, as the fabrication process used does not support integrated flash memory. At boot, the 2 kB boot ROM contains a program to copy the user program from the external serial flash to the internal SRAM and execute that program. The timers are used for timekeeping functions, and can operate on the always-active crystal oscillator clock. The system and power control module also includes a watchdog timer if required for system reliability. In the analog front end, the analog signals can be extracted or inserted at various places along the signal chain for maximum flexibility in testing.

The fabricated test bed PCB is shown in Fig. 8, where the computational radiation sensor chip is clearly visible in

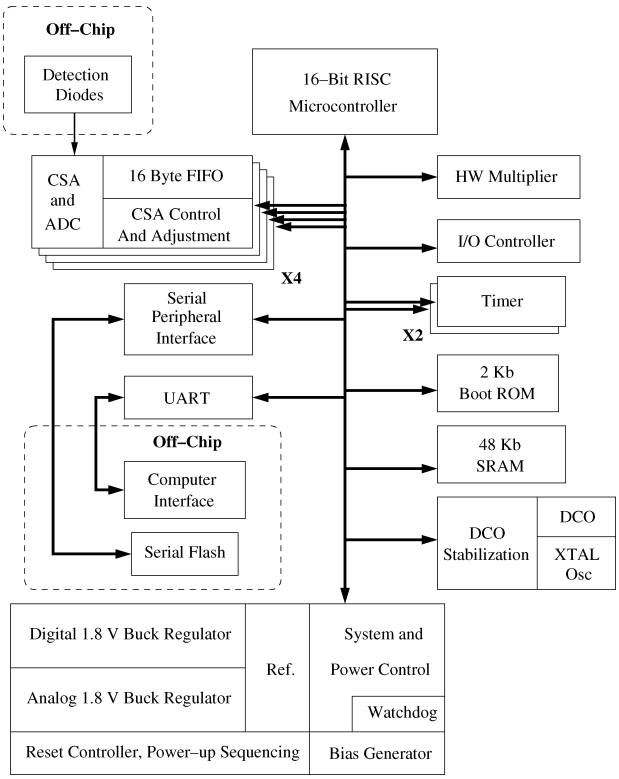

Fig. 7. Computational sensor architecture.

the center of the PCB. A coin-type lithium battery can be mounted on the back of the PCB. The overall dimensions are 3.5 cm $\times$ 6 cm $\times$ 1.6 cm including the battery.

A self-contained computational radiation sensor operation is required as part of this detection scheme. To that end, a software development environment has been devised using the test bed developed for this purpose. While the developed software does not lead to a full operating system, it is more of a shell to provide an environment that enables the individual developing the system full access to all I/O and memory locations without needing to recompile and reprogram the chip. In addition, the software allows additional features and functions to be added by using simple commands. Communications with the processor is done with a 3 V USB to serial communications device. The use

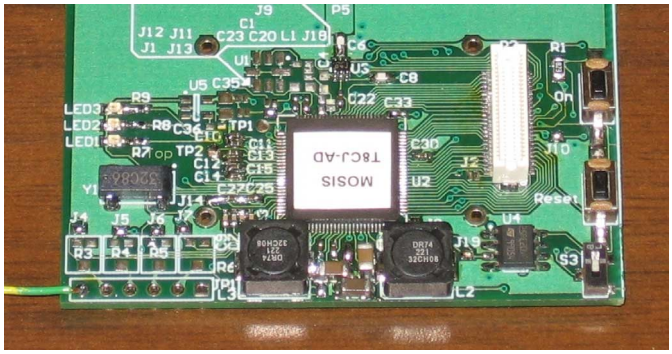

Fig. 8. Test bed PCB.

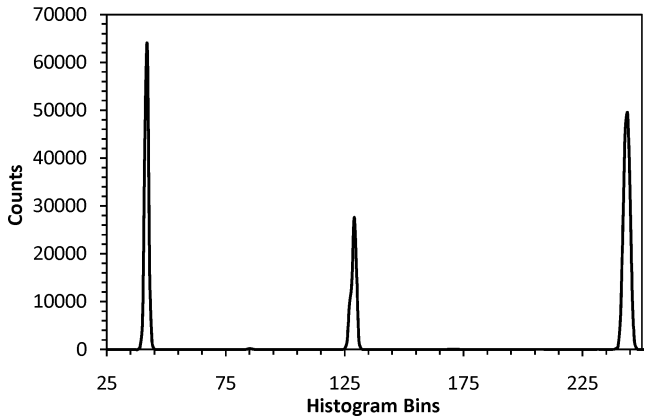

Fig. 9. Sample histogram acquired.

of USB allows almost any computer systems to be used for development. The software written for this system is a subset of the Forth programming language. This was chosen because of its ability to operate in a very restricted memory footprint. The entire Forth system requires only 8 kbytes of memory.

In the Forth system, actions are done with two different types of codes, native and interpreted. The native codes are in the binary language of the microprocessor and generated with a *gcc* compiler. A basic set of codes, some native and some interpreted, exist immediately after booting. These basic codes include math, simple I/O, memory management, time keeping, looping, and a compiler. The compiler is used to add additional functionality.

IV. Lab and Field Tests

A. Lab Tests

The pulse height spectra gathering application has been developed and implemented on the single chip computational radiation sensor to demonstrate the functionality of the software environment during lab tests. With an 8-bit ADC resolution, the application uses 256 separate counters to keep track of how many neutron events occurred with each pulse height. A plot of those counters produces a histogram of the neutron counts. Using an arbitrary waveform generator, a sequence of pulses with three distinct amplitudes with different arrival rates were applied to the analog front end of the computational sensor chip. Fig. 9 displays a sample pulse height spectra with 256 bins generated by the Forth system running on the chip.

TABLE I
Design Specifications

Process:	0.18 μm
Area:	9 mm^2
Front End Power Consumption:	$4 + 0.075 \times R$ μW[a]
CSA Feedback Capacitance:	0.2 - 15.2 pF in 1 pF increments
Max Particle Detection Rate:	4×10^5 sec^{-1}
Equivalent noise charge, detector disconnected, C_{fb}=0.2 pF:	525 e$^-$
ADC Type:	Charge Redistribution SAR
ADC Bits:	8
ADC Conversion Energy Consumption:	75 pJ
Max Processor Frequency:	60 MHz
Processor Voltage Active:	0.9-1.8 V
Processor Voltage Sleep:	0.65-1.8 V
Processor Active Power:	100-300 μW/MHz[b]
Processor Sleep Power:	2.5-9 μW[b]
Crystal Oscillator, Biases and References Total Power Consumption:	3 μW
Battery Voltage:	3 V
Battery Capacity:	3 WHr
Total Computational Sensor Average Power Consumption:	24 μW[c]
Battery Life:	$>$ 10 Years

[a] R is particle rate in thousands particles/sec.
[b] Power varies depending on DVS voltage setting.
[c] With single channel active, 4 μW for each additional channel.

To minimize the power consumption, the processor is in sleep mode over 99.9% of the time. The main digitally controlled oscillator is disabled during this time, except for when a character transmission to or reception from the computer is occurring. With the clock disabled, the digital circuitry only consumes between 2.5 and 9 μW of power depending on the supply voltage. The 32 kHz crystal oscillator operates continually. The main digital supply is operated at 900 mV to further reduce power consumption. The analog front end only wakes the processor when 12 or more unprocessed neutron events are in one of the FIFOs. When the processor wakes, it processes all the events in all four FIFOs, and then returns to the sleep state.

Table I gives some relevant specifications obtained from measurements of the chip.

B. Field Tests and Discussion of Results

Neutron field tests were conducted with a paraffin moderated 5.2 curie plutonium-beryllium neutron source which provided 2.2×10^4 thermal to epithermal $\mathrm{neutrons/cm^2\text{-}second}$, as calibrated by foil activation methods. Fig. 10 displays the actual test setup used in the testing of the computational sensor. As the front end CSA design is well suited for semiconductor neutron detectors [10], heterojunction diodes composed of mixed gadolinium and hafnium oxide ($\mathrm{GdHfO_2}$) on silicon have been utilized as the neutron sensing devices in this work [11]. In particular, the diodes that were utilized in the field tests are constructed with slightly less than 100 nm oxides of 15% gadolinium and 75% hafnium oxide films that were deposited on n-type single crystal Si(100) substrates using pulsed laser deposition [11], [12].

The absorption of the neutron leaves the ^{158}Gd in an excited state that releases energy through emission of high energy

Fig. 10. Field test setup.

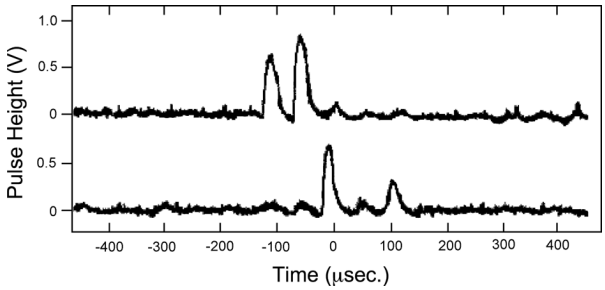

Fig. 11. Charge sensitive amplifier output waveforms.

gamma rays, low-energy gamma rays, X-rays, internal conversion (IC), and Auger Coster-Kronig (ACK) conversion electrons as

$$^{157}\mathrm{Gd}(\mathrm{n},\gamma) \rightarrow {}^{158}\mathrm{Gd} + \gamma + \mathrm{X{-}rays} + \mathrm{IC\ e^{-}} + \mathrm{ACK\ e^{-}}.$$

During a neutron capture event, the conversion electrons generate charge pulses in the heterojunction diodes which are converted to voltage by the front end section of the computational sensor.

Typical charge sensitive amplifier output waveforms captured over a period of 1 ms by the sensor system are shown in Fig. 11. The waveforms show several large spikes resulting from neutron detection at a charge-to-voltage gain setting of 833 $\mu\mathrm{V/fC}$, corresponding to 1.2 pF of integration capacitance with an amplifier time constant setting of 20 $\mu\mathrm{S}$. A diode reverse bias level of 2 V has been used with a bias resistor value of 20 $\mathrm{k}\Omega$ during the experiments.

For the pulse height spectra gathering, 256 histogram bins were created using an incremental bin resolution of 5.64 fC/bin, which corresponds to 4.7 mV after charge-to-voltage conversion. The experimental pulse height spectrum is shown in Fig. 12. Following electronic suppression of pulses below 170 mV, which dominate the pulse height collection without electronic suppression, the main contributions to the detection signal come from the conversion electron and the Gd k-shell Auger electron resonances. For $^{158}\mathrm{Gd}$, the current pulses generated by 79.5 keV (and other) conversion electrons can be efficiently measured and reliably identified. The K-shell binding energy is 50.2 keV resulting in a variety of Auger electron resonances of decreasing kinetic energy, ending in the 29.3 keV conversion electron centered pulse [13]. The K-shell electron excitation is accompanied by a 44 keV X-ray [13]–[15] which is not identified in the spectra in Fig. 12. The M shell

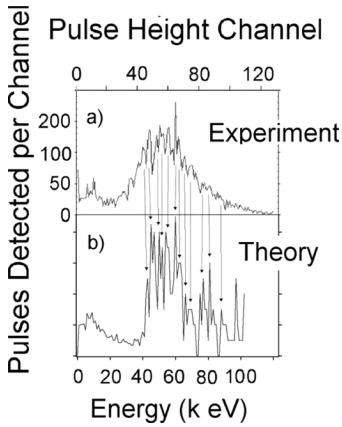

Fig. 12. Pulse height spectra of 15% Gd doped $\mathrm{HfO_2}$ on n-type Si(100) with thermalized neutrons from a PuBE source.

binding energy is 1.8 keV, resulting in only a small reduction of the 79.5 conversion electron energy to about 77 keV. Overall the pulse height spectra results in the creation of 40 to 80 keV pulses largely for $^{157}\mathrm{Gd}(\mathrm{n},\gamma)$ that are in good agreement with the model calculations. The features in the experimental spectra can be assigned to specific expected K-shell Auger resonances, but with a nonuniform distribution over this range [13].

To provide a comparison with theory, the devices have been simulated using the Monte Carlo N-Particle Transport Code (MCNP5.0) [16], where a planar source of 10^{11} neutrons was assumed and a model neutron spectrum was calculated from 30 eV to 14 MeV. To better compare experiment with the model simulations, there are corrections at the low energy end of the model pulse height spectra to account for the large number of counts rejected by electronic noise and signal suppression below a 170 mV pulse height in the experiment. By incorporating these corrections to the model, there is considerable agreement between experimental and theoretical pulse height spectra displayed in the bottom portion of Fig. 12. The deviations observed between simulation and experiment at larger pulse heights can be attributed to incomplete charge collection due the fact that the 15% Gd doped $\mathrm{HfO_2}$ film is rather thin.

It should be noted that the presented prototype system is not radiation hardened, thus it will be affected by radiation striking the electronics. Fast neutrons may cause crystal defects which accumulate slowly over time to eventually cause permanent circuit failure and thermal neutrons may cause single-event upset errors. The software includes a watchdog timer to facilitate recovery from such software errors.

Other neutron detection technologies exist [17], most of which could be directly interfaced to the electronics with minimal hardware modifications. Table II shows a comparison of selected technologies.

All of the detection technologies except the solid-state one require a high voltage supply to bias either the detector itself or the photomultiplier tube (PMT). These supplies range from 500 V to 3 kV which dramatically increases system power consumption. Furthermore, the detector or PMT are fragile elements which are not suitable for harsh environments. The solid-state neutron detectors such as the presented $\mathrm{GdHfO_2}$ detector do not require the high voltage supply and are therefore particularly suited to low-power applications [18].

TABLE II
DETECTION TECHNOLOGIES

Technology	Detection Probability			Power
	Thermal Neutron	Fast Neutron	γ-ray	
BF_3 Tubes	high	low	moderate	moderate
^3He Tubes	very high	low	low	moderate
^4He or CH_4	low	high	moderate	moderate
Fission Chamber	low	low	very low	moderate
Plastic Scintillator	high	very high	very high	high
Solid-State	high	low	moderate	low

V. CONCLUSION

A miniaturized computational radiation sensor that effectively acts as a low bit-rate information source has been developed based on a 0.18 μm CMOS technology. The electronic circuit design migrates the following critical computation tasks of detection into the sensor head: counting the neutron events, energy bin classification of captured neutrons and pulse height spectra computation, and the efficient dissemination of the results via existing communication interfaces. Hence, the presented standalone integrated sensor paradigm relaxes the data transmission requirements and opens up possibilities for achieving low-power wireless sensor network operation. Fully integrating all the components of the design allows for a lower overall power consumption than a solution using some off-the-shelf components, allowing a battery life of over ten years. Lab measurements and field tests have confirmed the operation of the chip and the validity of the approaches taken.

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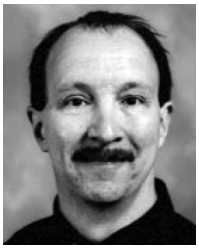

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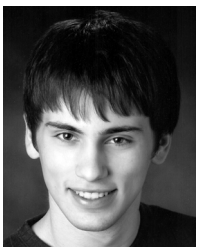

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