Materials, Device, and System Integration of Amorphous Oxide Semiconductor TFTs

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Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. This dissertation contains fewer than 65,000 words including appendices, bibliography, footnotes, tables and equations and has fewer than 150 figures.

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Abstract

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) have great potential for use in the next-generation of electronics. AOS TFTs can be used to fabricate circuits and sensors on various substrates, due to unique properties, including high mobility, excellent uniformity, and it requiring a low-temperature process. Currently, indium gallium zinc oxide (IGZO) is the predominant AOS used in the display industry as a TFT semiconductor. Although the IGZO technology is very mature, the development of AOS continues. Additional AOSs are being investigated to reduce cost and improve stability. Considering availability and the potential of materials, indium silicon oxide (ISO) was selected for this project. ISO uses silicon to suppress the instability originating from the oxygen vacancy. The silicon-oxygen bond has a higher dissociation energy, which improves retention of oxygen atoms in the film, and thus, increases the transistor's stability.

This detailed study follows a bottom-up approach. It starts with the fabrication and characterisation of materials. Basic material properties of the ISO film are discussed within, including amorphicity, bandgap, stoichiometry, and Hall-effect parameters. Based on the characterisation results, different deposition recipes for the TFT were developed and tested. The interface quality and etching selectivity were investigated. Uniformity and stability data were extracted from a TFT array using the developed photo-lithography process, which was used to verify and quantitate the capability of the process in system integration and circuit design. A Monte-Carlo simulation environment was established based on the extracted data. The two urgent challenges in all-TFT analogue circuit design, the lack of proper active load and the large parasitic capacitance, were investigated. In-depth analysis on these two issues and applicable solutions were presented. Investigation on system integration of TFT circuits and sensors were conducted, since the device demonstrated the required performance and uniformity. An all-TFT differential-input amplifier was designed and verified, as the first mixed signal all-TFT circuit.

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Nomenclature

Symbols

λ	Wave length
Ω	Ohm
σ	Standard deviation
εr	Relative permittivity
ε0	Vacuum permittivity
q	Elementary charge
h	Planck constant

Acronyms/Abbreviations

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
HUD	Head-up Display
PCB	Printed Circuit Board
TFT	Thin Film Transistor
AOS	Amorphous Oxide Semiconductor
ISO	Indium-Silicon-Oxide
RF	Radio Frequency
XRD	X-ray diffraction
JCPDS	Joint Committee on Powder Diffraction Standards
SEM	Scanning electron microscope
UV-Vis	Ultraviolet–visible spectroscopy
DFT	Density Functional Theory
UPS	Ultraviolet photoelectron spectroscopy
IP	Ionization potential
EDX	Energy-dispersive X-ray spectroscopy
SD	Standard deviation

MIS	Metal-Insulator-Semiconductor
GUI	Graphical User Interface
CMOS	Complementary Metal Oxide Semiconductor
ADC	Analog-to-Digital Converter
RHP	Right half-plane
GBW	Gain-bandwidth product
HF	Hydrofluoric
TLC	Tap-limited conduction
FFT	Fast Fourier Transform
THD	Total Harmonic Distortion
Op-amp	Operational amplifier
SNR	Signal-to-noise ratio
DAC	Digital-to-Analog Converter

Chapter 1

Introduction

This chapter provides the background for amorphous oxide semiconductor (AOS) thin-film transistors (TFT), and discusses the motivation to develop the In-Si-O TFT photo-lithography process and all-TFT circuit. In Section 1.1, the promising future of TFT is revealed. The developing trends for TFT applications, mainly sensors and the unique properties of all-TFT integrated circuits, along with potential applications, are provided. Section 1.2 reviews the background of AOS TFTs and all-TFT circuits. Overall objectives of this dissertation are given in Section 1.3.

1.1. Motivation

AOS TFTs have already become the sole choice for large area-based applications, including screens and large-area imaging [1]–[3]. Unlike Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), the development of TFTs largely relies on new application scenarios, as opposed to more advanced fabrication processes for a smaller device [4]. Therefore, it is imperative to explore new avenues for TFT applications.

With the recent popularization of smart phones, wearables, and portable sensing platforms, flexible electronics and sensors have attracted worldwide attention [5]–[7]. A large number of gadgets, accessories, and wearable electronics emerged for mobile devices; this phenomenon expanded the flexible electronics and sensor market dramatically. According to the Wearable Robotics Association, from 2016 to 2025, the global market forecast for wearable technologies is expected to have a 21.1% compounded annual growth rate. The visual/Head-up Display (HUD) and smart textiles market will contribute most of the growth and will continue to lead other sectors in terms of sales and growth. These two technologies provide more interactive response

and feedback to users than the current technologies. TFTs are likely to be widely used in display-related and textile-related electronics [8]–[10].

At the same time, concepts such as the Internet-of-things (IoT) and wireless sensor networks (WSN) continue to heat up the sensor market [11]–[14]. It is predicted that sensors will become one of the biggest businesses in the history of wearable electronics. With a growing demand for health and environmental monitoring, a sensor platform that can measure the physical response of the wearer and status of his/her surrounding environment becomes essential for portable electronics. Consequently, building such a platform has aroused intense interest in both academia and industry [15], [16].

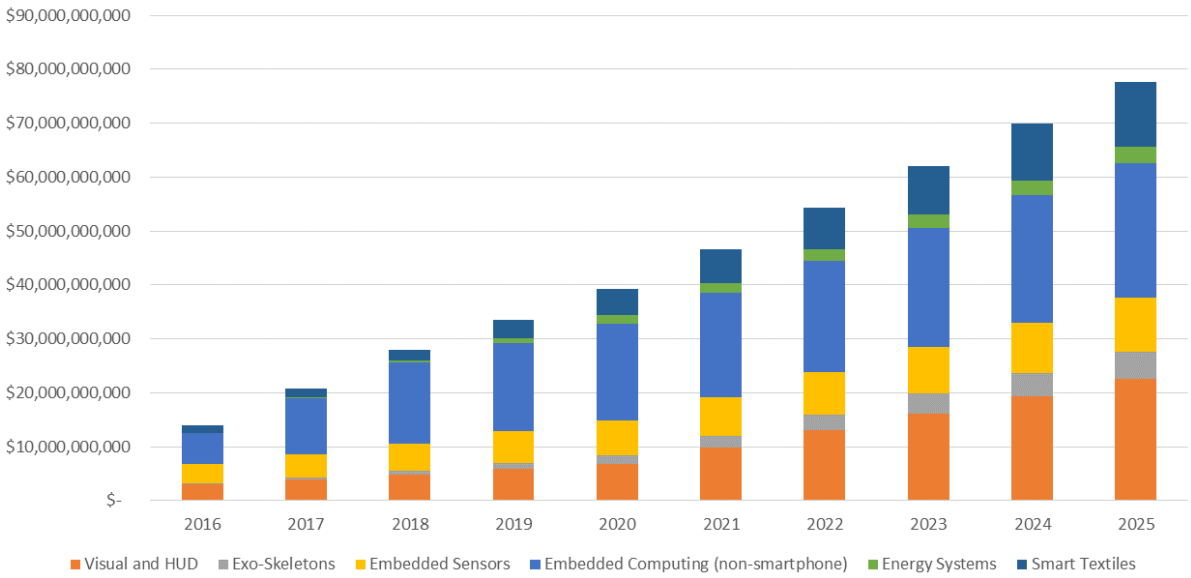

Fig. 1.1. Wearable technology growth worldwide, 2016-2025.

Source: Wearable Robotics Association

In order to meet the future demand in a variety of fields, the next generation of electronics requires significant improvements in sensitivity, specificity, and comfortability [17]–[20]. Conventional electronic modules are typically based on printed circuit board (PCB) and silicon chips, which are inflexible and bulky. For instance, the set-up procedures of a conventional sensor require conductive gel, tape, or wires to ensure proper contact between the hardware and the objective surface, which is not only time-consuming, but it also constrains the movement of the wearer. An ideal sensor platform for wearable electronics should be skin-like; more specifically, the sensor platform should be ultrathin, flexible, stretchable, and even self-healing [21][22]. Several concepts of future sensor platforms are shown in Fig. 1.2, including the smart bandage [23], a skin-like/tattoo-like sensor [24], and artificial skin [25]. These

platforms were designed to continuously monitor uterine contractions, heart rate, oxygen levels, and body temperature [26], [27]. The platforms must also integrate different types of sensors, wireless communication modules, and related circuits [28].

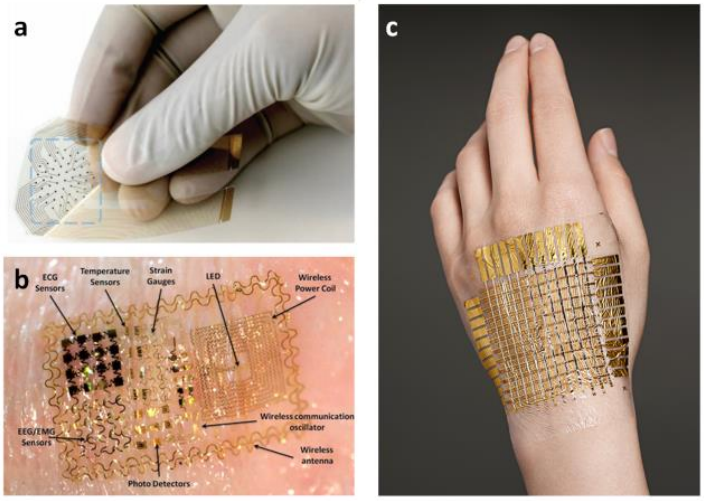

Fig. 1.2. Sensor platform proof of concepts: (a) smart bandage [23], (b) skin-like/tattoo-like sensor [24], (c) artificial skin [25].

Many advances have already been made to improve sensing techniques, including new transduction mechanisms, different structural designs, and innovative materials [29]–[31]. Unfortunately, signal processing circuits for sensors have not received as much attention, even though a carefully designed configuration can greatly boost the performance of sensors. The signal conditioning circuits alone can dramatically compromise performance under certain conditions [32]. As shown in Fig.1.3, the signal conditioning circuit, usually an amplifier, is not fabricated on the same substrate as the sensor. In most cases, the sensor and the amplifier are two separate components connected by wires. The major disadvantage of this configuration is that the thermal noise generated on the connection wire is also amplified [33].

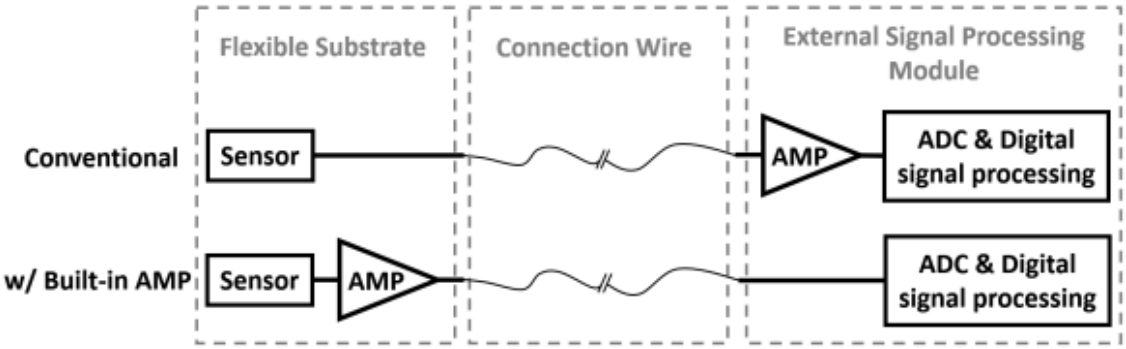

Fig. 1.3. Built-in pre-amplifier for sensors.

To avoid thermal noise amplification, the most straightforward solution is to move the amplifier to the front-end, which can dramatically increase the signal-to-noise ratio. Maximum performance of such configuration can be obtained when the amplifier is fabricated on the same substrate as the sensors. In addition to thermal noise, common-mode noise generated from an external source may compromise the performance of the amplifier. For long-distance connection wires, screened or twisted-pair cabling is used to cancel out the external electromagnetic interference [34]. However, for wearable electronics based on thin film techniques, the realisation of screened/twisted pair cabling is not practical and the wire length is relatively short [35]. Therefore, a differential input pair is used to suppress the common-mode noise generated on a medium-distance connection wire [36].

However, building circuit components based on a flexible substrate is not an easy task [37]. The electrical properties and fabrication techniques of elastic materials, mostly thin-film materials, are very poor compared to conventional III-V semiconductors [38]. Traditionally, much of the preliminary work in thin-film electronics centred around area-intensive applications, such as flat panel displays and photovoltaics [39], [40]. These applications are less sensitive to component performance, but require the capability to cover a large area. In recent years, rapid development of thin-film materials has led to a great improvement in thin film electronics. The involvement of new materials, including metal-oxide, organic, one-dimension, and two-dimension materials has boosted the performance of thin-film electronic components, which are now used in conventional applications with uniquely advantageous performance benefits [41]–[44].

The scope of applications envisioned for thin-film electronics is expanding substantially, especially in novel concepts, such as an integrated sensor, printed radio frequency identification, and electroluminescent phosphor [45]–[48]. Thin-film electronics offer low cost, large area compatibility, high scalability, and extreme potential for flexibility. Most notably, field-effect transistors based on TFTs can be fabricated at low temperatures on a variety of substrates [49], [50]. In addition, the intrinsic mobility of the semiconductor materials used in TFTs has increased exponentially over the past few decades [51]. Today's commercially available thin-film semiconductors have mobility performance in the range of 1 cm^2/Vs to 20 cm^2/Vs. Fig 1.4 summarizes data collected by Plastic Logic. It shows the mobility and process temperature of different types of TFTs. Although the mobility remains low, especially

at low fabrication temperatures, some TFTs can be used to design simple circuits. As performance increases, TFTs will become a more attractive option for the design and fabrication of flexible electronic external circuits [52], [53].

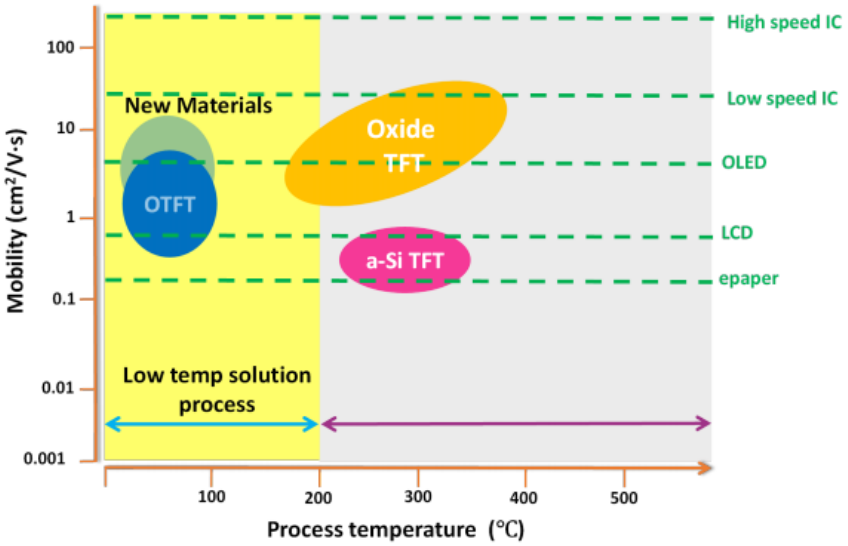

Fig. 1.4. Mobility and process temperature of different types of TFTs.

Source: Plastic Logic

1.2. Background

AOSs have been investigated extensively as a promising semiconductor for next-generation electronics TFTs. The AOS has many appealing properties, including low processing temperature, large-area uniformity, wide bandgap, high transparency, and high mobility [54]. Amorphous indium oxide (a-InO_x)-based semiconductors are believed to be the most promising semiconductors for TFT [55]. Previous reports on a-InO_x detailed the following types: InGaZnO, InSnZnO, InZnO, InWO, InYO and InSiO TFTs [56]–[58].

Among all the a-InO_x TFTs, IGZO is the most widely used semiconductor in both industry and academia. The IGZO TFT was first proposed in 2004. Its high mobility is attributed to the direct overlap of the isotropic s orbitals of its indium atoms [59]. Its crystallization and hall mobility can be controlled by changing the composition of the film. Gallium, which has different ionic charges and sizes, is mixed into the film to form amorphous phases and suppress the formation of oxygen vacancy, thus reducing instability. Increasing the indium content can boost the intrinsic mobility. The best stoichiometry of In:Ga:Zn:O occurs at ratios of 1:1:1:4 or 2:2:1:7. The electrical properties of the film can be moderately changed near the best recipe, allowing

engineers to adjust the material to meet different requirements [60]–[62]. However, IGZO is not perfect, and suffers from instability. The IGZO TFT is sensitive to bias/current stress, temperature, light illumination, and water vapour exposure [63]–[66]. It is widely accepted that oxygen vacancy acts as a hole trap, and is a major contributor to the instability issue. To suppress the impact of oxygen vacancy on the transistor's performance, one or more cations in IGZO must be replaced with other materials [67].

Recently, Shinya *et al.* reported a new material, the In-Si-O (ISO) [68]. ISO uses silicon to suppress the instability originating from the oxygen vacancy. The silicon-oxygen bond has higher dissociation energy, which improves the retention of oxygen atoms in the film, and thus increases stability. The ISO TFTs were fabricated with stencil shadow masks on a silicon substrate, and the deposition of ISO was by DC sputtering. By varying the silicon oxide content, field-effect mobility was regulated from 5 cm^2/Vs to 30 cm^2/Vs. Changing the argon-to-oxygen ratio during sputtering adjusted mobility, threshold voltage, and subthreshold swing over a certain range [69]–[71]. These features show great potential for TFT-based circuits and systems.

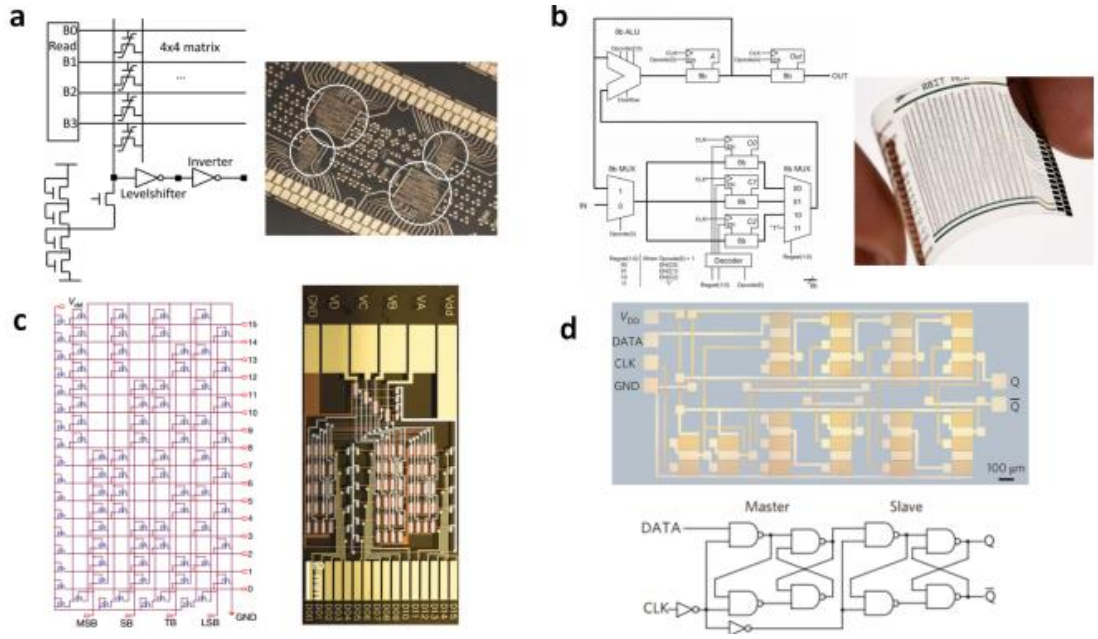

Fig. 1.5. State-of-art digital circuits: (a) non-volatile re-addressable memory [72], (b) 8-bit 40-instructions-per-second microprocessor [73], (c) a 4-bit decoder [74], and (d) a master-slave delay flip-flop [75].

In terms of all-TFT circuits, Fig. 1.5 shows the state-of-art, which includes non-volatile re-addressable memory [72], an 8-bit 40-instructions-per-second microprocessor [73], a 4-bit decoder [74], and a master-slave delay flip-flop [75]. The

performance of these circuits (i.e. the clock rate) is on par with MOSFET technology from fifty years ago.

For analogue TFT circuits, the state-of-art is demonstrated in Fig. 1.6 [76]–[78]. Although some specifications of the amplifiers are acceptable, specifications including bandwidth, input and output impedance usually cannot meet practical needs. Drawbacks of TFT circuits can be traced back to the properties and fabrication processes of thin film transistors. Low intrinsic mobility and high threshold voltage lead to low transconductance, which is usually on the order of 10^{-6} Siemens, while an MOS transistor can reach 10^{-3} Siemens. Therefore, to obtain an equivalent gain, the load in a TFT amplifier will need to be at least a thousand times larger than that in a MOSFET amplifier.

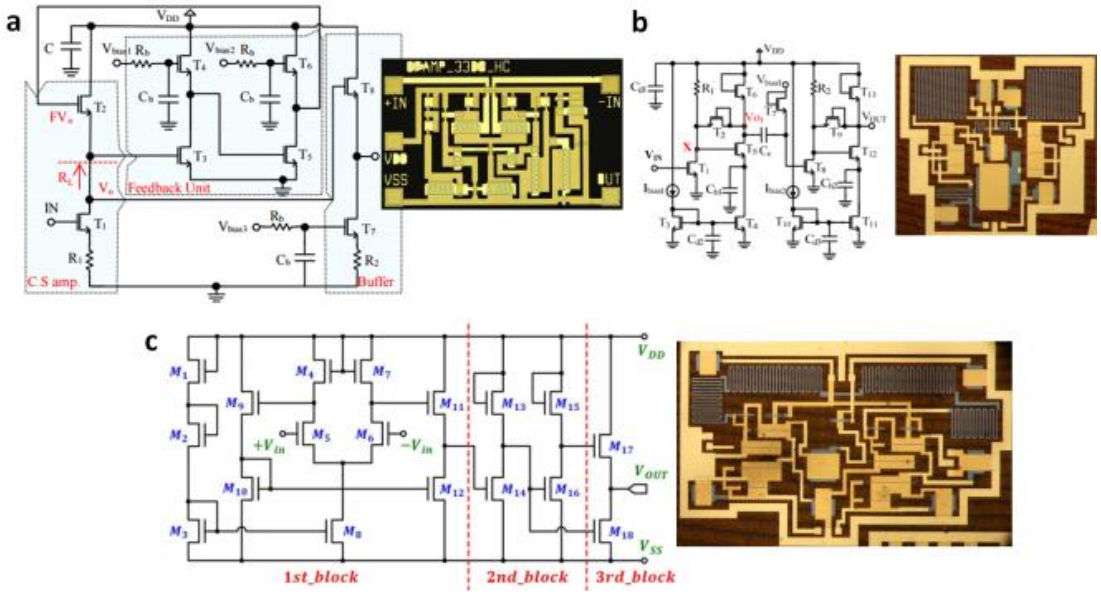

Fig. 1.6. State-of-art analogue circuits: (a) a high gain amplifier [76], (b) a Cherry-Hooper amplifier [77], and (c) a three-stage operational amplifier [78].

1.3. Dissertation Outline

The objective of this dissertation is to investigate the remaining challenges associated with the ISO material, device, and system integration. The outline of this dissertation is as follows. **Chapter 2** details ISO TFT development and characterisation. Basic material properties of the ISO film are discussed, including amorphicity, bandgap, stoichiometry, and Hall-effect parameters. **Chapter 3** presents the uniformity and stability data from a TFT array using the photo-lithography process. Origins of the threshold voltage shift in bias-stress measurement are carefully evaluated using C-V

and field-effect measurements. The spatial and temporal variations of ISO TFT are used to verify and quantitate the capability of the process in system integration and circuit design. A Monte-Carlo simulation environment was established based on the extracted data. **Chapter 4** addresses two of the most urgent challenges in all-TFT analogue circuit design, which are the lack of proper active load and the large parasitic capacitance. In-depth analysis of these two issues and applicable solutions are given. **Chapter 5** presents the process of designing, simulating, and fabricating an all-TFT amplifier. A 4-bit capacitor array was successfully integrated into the amplifier. Design strategy, simulation results, layout design, and measurement results are given in this chapter. **Chapter 6** summarizes the results obtained in this dissertation and discusses the novelty of this research. The outlook for future extension of this study is provided as well.

Chapter 2

Indium-Silicon-Oxide TFT

This chapter describes how the Indium-Silicon-Oxide (ISO) TFT was developed. Section 2.1 provides material characterisation results of the ISO using different techniques. Section 2.2 introduces the four-mask/six-mask process as well as the plastic process. Methods adopted to improve robustness are also given in this section. Section 2.3 provides characterisation results of the ISO TFTs.

2.1. Semiconductor Characterisation

Semiconductors, the vehicle and valve of electron flow, are the most important component of the TFT device. The characteristics of the materials are essential and prerequisite to building an outstanding TFT. In this section, the characteristics of deposited ISO film are examined.

2.1.1. X-Ray Diffraction Spectroscopy

X-ray diffraction (XRD) measurements are widely used to validate whether a deposited film is amorphous [79]. Using this technique, the correlations between the semiconductor's microstructure, the deposition conditions, and the annealing conditions were investigated.

The ISO thin films were grown on an Si substrate using radio frequency (RF) sputtering employing a 90% In_2O_3, 10% SiO_2 ceramic target. The RF power of the electron guns was 150 W, and the ISO films were sputtered in a 4 mTorr atmosphere. The O_2:(O_2+Ar) flow rate ratio varied from 0% to 17%. During the sputtering, the ISO target was constantly moving/rotating to obtain uniformly coated films. By varying the

deposition time, the film thickness was fixed to 100nm. Prior to the deposition, the Si substrates were cleaned in an ultrasonic cleaner with de-ionized water, acetone, and isopropyl alcohol. Three different deposition conditions, namely three oxygen flow rate ratios were used to fabricate samples for the XRD measurements: 0%, 3%, and 17%. The samples were diced into 12 smaller pieces so that the impact of annealing conditions could be investigated as well. Four annealing conditions were tested: without annealing, one-hour of annealing at 150°C, 12 hours of annealing at 150°C, and 24 hours of annealing at 150°C.

The XRD measurements were conducted with the assistance of Joana Cerdeira at the Faculty of Sciences and Technology, Campus of Caparica. The equipment used was a PANalytical X'Pert PRO with Cu Kα radiation (λ=1.540598 Å). Fig. 2.1 (a) compares the XRD data of the as-deposited ISO films with different recipes. Peaks at 31.3° were found in all films. According to the Joint Committee on Powder Diffraction Standards (JCPDS), 21.5° (211), 30.6° (222), and 35.5° (400) were assigned to the XRD 2θ peaks of the cubic phase, c-In_2O_3. 31.3° is classified as a (222)-like peak. The (222) peak is asymmetric and broad, due to an overlap of two adjacent peaks or inhomogeneous strain. Compared with the 0% oxygen as-deposited sample, the 3% and 17% oxygen as-deposited samples had much weaker (222)-like peaks.

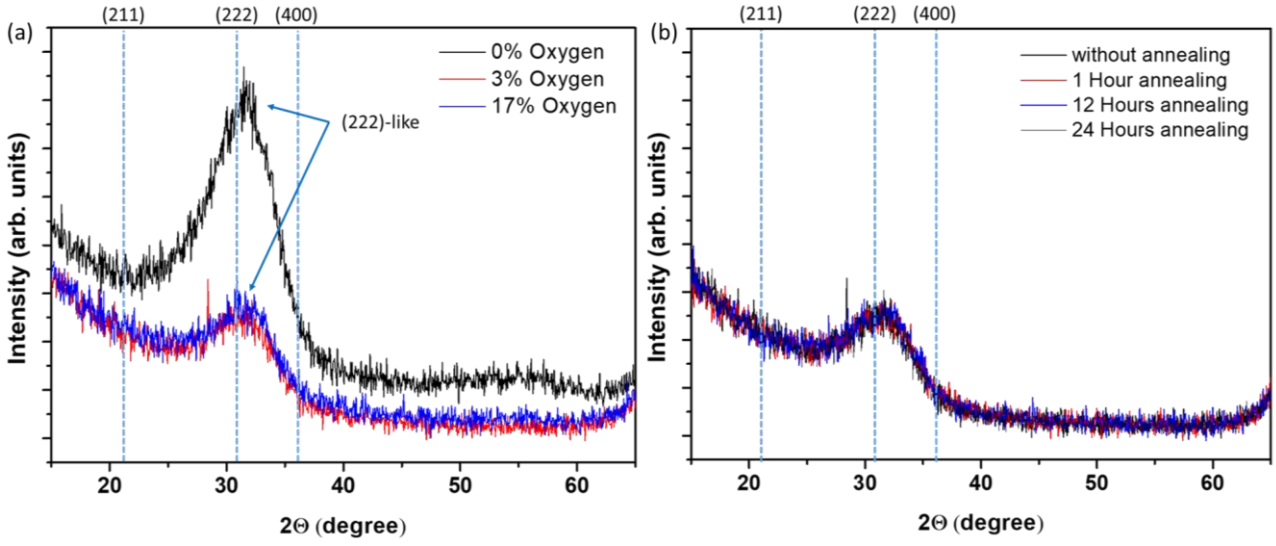

Fig. 2.1. XRD data of (a) the as-deposited ISO films with different oxygen flow rate ratios and (b) the 3% oxygen films under different annealing conditions.

Fig. 2.1 (b) shows the XRD data of the 3% oxygen ISO films under different annealing conditions. The annealing used an IKA hot plate (metal plate) in atmosphere. The temperature uniformity and stability of the hot plate were verified with a thermometer.

Similar trends were also found in the 0% and 15% annealing experiments. Thus, the 150°C annealing did not cause any crystallization changes in the ISO film.

Based on the XRD data, when there was no oxygen in the chamber during deposition, a very small amount of the polycrystalline ISO was found in the deposited film. Thus, feeding oxygen into the chamber can effectively reduce the polycrystalline. The 3% and 17% oxygen ratio deposited ISO was amorphous with and without 150°C annealing.

2.1.2. Scanning Electron Microscope

A scanning electron microscope (SEM) was used to verify the conclusion in the previous section. The monocrystalline ISO grain was 20nm in size, which is detectable by SEM [80], [81]. The SEM photos were taken at Cambridge using a ZEISS SEM. As shown in Fig. 2.2, no visible crystalline grains or boundaries were found in the SEM pictures. Thus, all the deposited films were amorphous.

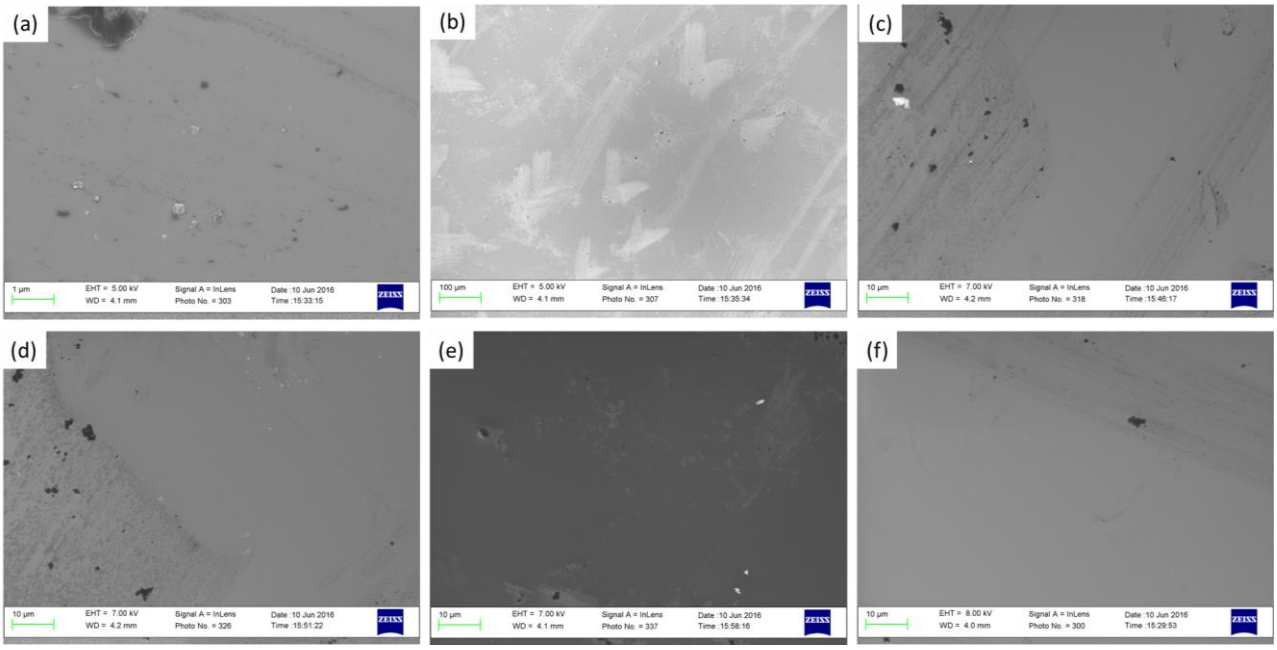

Fig. 2.2. SEM pictures of the as-deposited ISO films with varying oxygen ratios: (a) 0%, (b) 3%, and (c) 17%; SEM pictures of the 3% oxygen ratio ISO film annealing for (c) one hour, (d) 12 hours, and (e) 24 hours.

2.1.3. Ultraviolet–Visible Spectroscopy

Ultraviolet–visible spectroscopy (UV-Vis) can be used to characterise the optical bandgap properties of amorphous materials. For inorganic semiconductors, there is very little interaction between electrons and holes; i.e. the exciton binding energy is very

small. Therefore, the optical bandgap and electronic bandgap are essentially identical [82].

The samples used in the measurement were annealed at 150°C for one hour. The measurement equipment was the Unicam UV4 UV/Vis Spectrophotometer. Fig. 2.3 shows the optical absorption spectrum of the ISO film with varying oxygen ratios. The 0% oxygen sample had a slightly higher absorbance than the 3% and 17% samples. The absorbance peaks became insignificant when the wavelength was longer than 500nm. Applying the Tauc method gives the relationship between optical bandgap and photon energy:

$$(h\nu\alpha)^{1/n} = A(h\nu - E_g) \tag{2.1}$$

where $h\nu$ is the photon energy, α is the absorption coefficient, A is the transition constant, and n is the power factor.

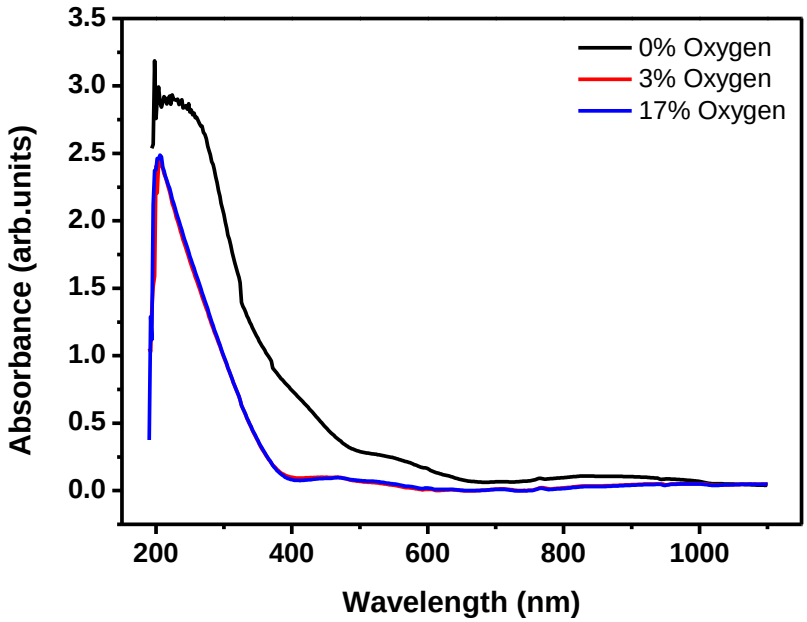

Fig. 2.3. Optical absorption spectrum of the ISO film with varying oxygen ratios.

With the band structure unknown, both allowed indirect and allowed direct transitions of the electrons were considered. Fig. 2.4 (a) shows the allowed indirect transition Tauc plot. The optical bandgap of the 0%, 3%, and 17% oxygen samples were 1.23eV, 1.97eV, and 1.97eV, respectively. In terms of the allowed direct transition scenario, the Tauc plot is shown in Fig. 2.4 (b). The optical bandgap of the 0%, 3%, and 17% oxygen samples were 2.83eV, 3.55eV, and 3.55eV, respectively.

Taking the 3% oxygen sample as an example, its electronic bandgap would likely fall between the allowed direct and indirect transition scenarios, which is [1.97eV,

3.55eV]. Previous reports suggested that the conventional energy band dispersion model for metal oxides was applicable to the ISO. Thus, allowed direct was assumed to be the transition type of the ISO film in this dissertation. Density functional theory (DFT) simulations will be used to obtain a more accurate band structure in the future.

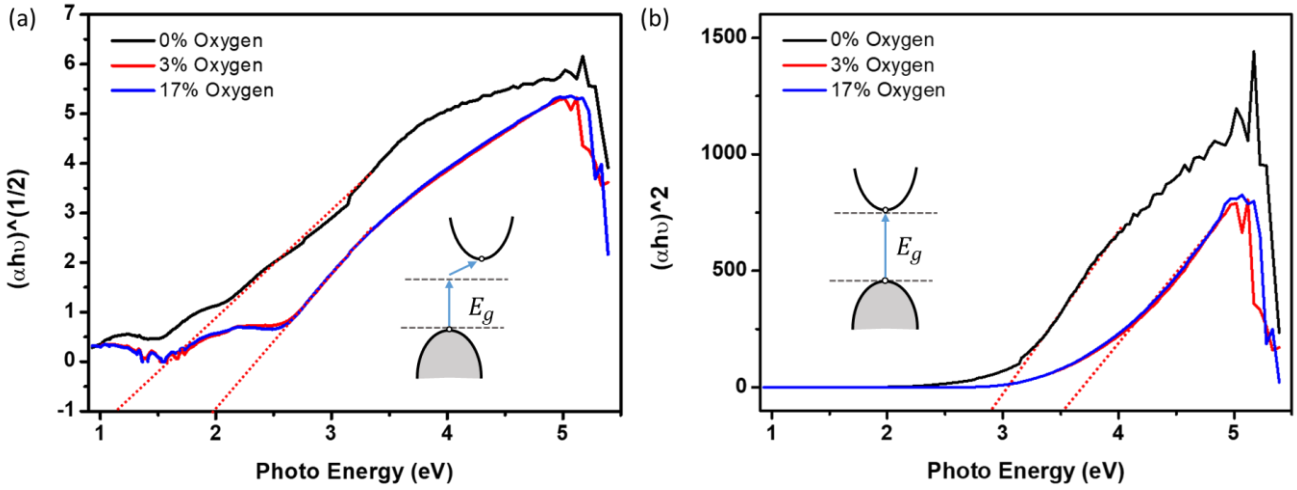

Fig. 2.4. Tauc plot of the ISO film assuming that the transitions type is: (a) allowed indirect and (b) allowed direct.

2.1.4. Ultraviolet Photoemission Spectroscopy

Ultraviolet photoelectron spectroscopy (UPS) measures the kinetic energy spectra of photoelectrons emitted by molecules that have absorbed ultraviolet photons [83]. It is used to determine the relative position of the ISO's valence band. The equipment used for UPS measurements was an Escalab 250Xi along with the near ambient pressure (NAP) X-ray photoemission spectroscopy (XPS) system. The sample prepared for the UPS measurement was a 3% oxygen ISO film deposited on a silicon substrate. The sample was annealed at 150°C for one hour. A thin layer of Ag was sputtered on the sample as the reference electrode.

Fig. 2.5 shows the UPS measurement results. The ionization potential (IP) of the ISO film is the energy separation between the vacuum level and the valence band's maximum. The IP value can be extracted from the intercept between the x-axis and the red fitting line of the first peak, which was 6.67 eV. From the previous section, the bandgap for allowed direct transition was 3.55 eV. Adding this value to the valence band minimum obtained the conduction minimum, which was 3.12 eV. The schematic band diagram of the ISO film is shown in the inset figure below.

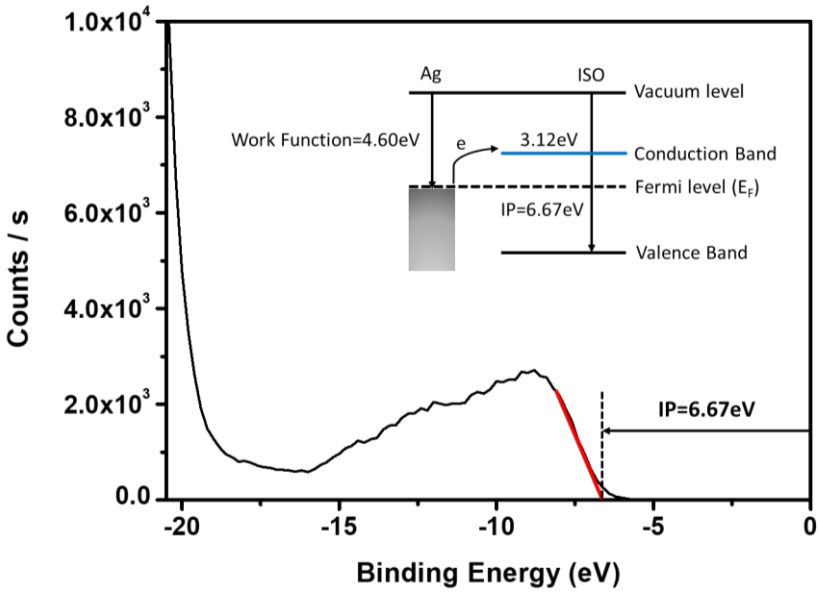

Fig. 2.5. UPS low binding energy edge of the ISO thin film on a silicon substrate, inset figure is the schematic band diagram for the ISO/Ag

2.1.5. Energy-dispersive X-ray spectroscopy

Energy-dispersive X-ray spectroscopy (EDX) provides elemental analysis and chemical characterisation of the ISO sample [84]. The measurement equipment was an INCA EDX, and the sample was a 3% oxygen ISO film deposited on a silicon substrate that had been annealed for one hour. Fig. 2.6 shows the EDS elemental mapping, where oxygen, indium, and silicon were uniformly distributed throughout the material.

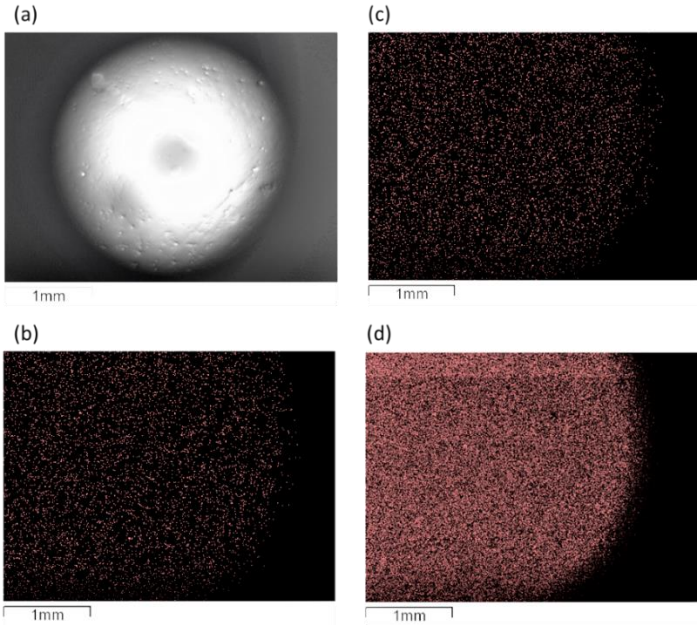

Fig. 2.6. EDS elemental mapping: (a) selected area on the sample, (b) O mapping, (c) In mapping, and (d) Si mapping. ***Gamma adjusted for better image quality***

EDX spectra of the ISO film is shown in Fig. 2.7. Since no other elements were found, the sample was not contaminated during the fabrication process. Removing the background interference, the stoichiometric expression of the material was $In_9SiO_{14.02}$.

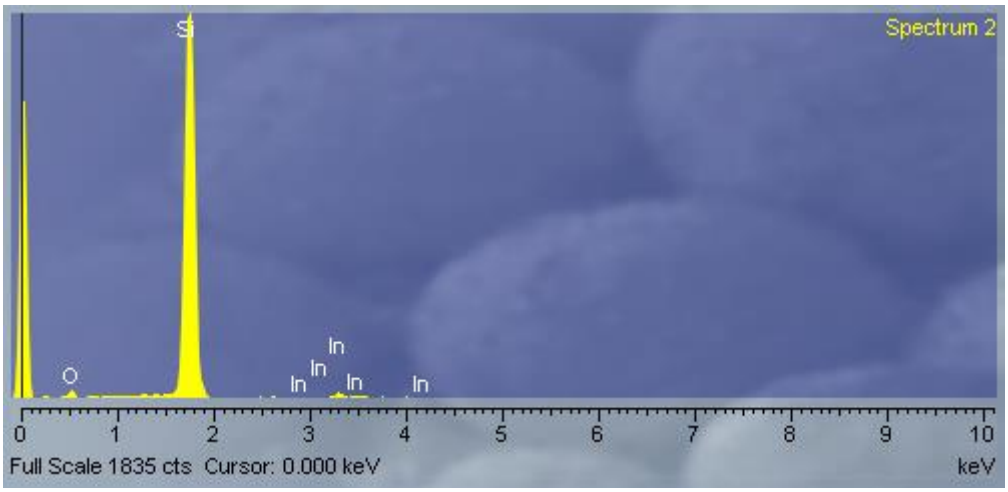

Fig. 2.7. Energy dispersed electron spectra of the ISO film.

2.1.6. Hall Effect Measurements

The electrical properties of the ISO film were investigated by Hall effect measurements. The equipment used was an MMR Hall and Van der Pauw Measurement System. The measurement temperature was 26℃. All films exhibited n-type conduction. The as-deposited 3% film possessed a carrier concentration of 2.80×10^{19} cm^{-3}, a Hall mobility of 2.16 $cm^2/(V\cdot s)$, a resistivity of 0.1031 Ω·cm, and a Hall coefficient of 0.22 cm^3/Coul. The measurement error, or the observation error of the machine, was 20%. The other recipes used in the previous sections with different annealing conditions were also tested, but the variations were in the range of the observation error. Thus, the effect of different recipes and annealing conditions on Hall Effect measurements will not be discussed, since the variation was too small.

Generally speaking, carrier density was very sensitive to defect structure. If the films remained amorphous after annealing, increasing the annealing temperature and time could possibly reduce defects, thus increasing the carrier density. For amorphous metal oxide semiconductors, the Hall mobility, carrier concentration, and resistivity of the IGZO thin films are believed to be dependent on deposition power. The lower the deposition power, the better the film quality (less defects).

2.2. Fabrication Process

The ISO TFTs used in this work were developed at The Centre for Advanced Photonics and Electronics (CAPE) and The Nanoscience Centre. In this section, the limitations of the equipment are discussed, along with the design and development of the TFT process.

2.2.1. Selective Etching

Most of the equipment used in this work was designed for research or prototype verification, and had very little control of uniformity. It was essential to determine the limits of the machines and to design suitable processes to improve robustness. First, the uniformity of the deposited films was tested. Different films were deposited on single-side polished 4-inch glass/silicon substrates. Nine different positions (a 3×3 array, one in the centre, and the rest at intervals of 2.5 cm) were used to collect thickness data. A Dektak XT Profilometer was used to measure the film thickness.

As shown in Table 2.1, 10 films were measured. Cr and Mo were deposited by a Precision Atomics DC sputter. The other films were deposited by the MVSystems Cluster tools. Compared to the other films, the semiconductor (ISO, ZnON) and the AlO_x films had much smaller standard deviations. This was because the RF sputter chamber had a rotating stage to ensure the deposited semiconductor film was uniform. In addition, the working mechanism of the ALD ensured that the AlO_x thickness across the substrate was controlled precisely by varying the number of cycles.

Table 2.1. Thickness (nm) of the deposited films on 4-inch substrates

Deposited films	1	2	3	4	5	6	7	8	9	**Mean**	**SD**
Cr (DC Sputter)	212	215	245	230	221	238	239	231	244	**231**	**12.22**
Mo (DC Sputter)	318	344	350	364	363	331	337	319	374	**344**	**20.04**
SiN_x (SiH_4:H_2:NH_3=1:40:10)	245	249	271	254	281	258	235	259	253	**256**	**13.63**
SiN_x (SiH_4:H_2:NH_3=1:40:20)	285	315	309	309	335	319	287	313	317	**310**	**15.59**
SiO_x (SiH_4: N_2O=1:5, 20W)	271	289	287	266	321	282	250	299	287	**284**	**20.27**
SiO_x (SiH_4: N_2O=1:5, 15W)	295	334	332	309	352	320	292	327	337	**322**	**19.99**
ISO	296	317	302	307	321	301	304	321	316	**309**	**9.42**
ZnON	318	329	333	321	339	322	344	328	337	**330**	**8.87**
AlO_x (150°C, 1.0s purge)	271	278	289	276	282	286	282	282	280	**281**	**5.32**
AlO_x (150°C, 1.2s purge)	286	287	298	310	295	294	298	291	307	**296**	**8.18**

Among all the layers of TFT, the semiconductor and insulator are the most important. Variations in thickness can have direct impact on device performance. Fortunately, the semiconductor layer and the dielectric layer (AlO_x) had already been verified as uniform across the 4-inch substrate. Other films had slightly larger standard deviations. SiN_x and SiO_x were used as passivation layers in this work, which were much less sensitive to uniformity. As long as the metals were still conducting and the work function remained unchanged, the change in thickness at the source/drain did not have any physical impact on the performance of the TFTs.

Secondly, the etching techniques were characterised. Table 2.2 shows the details of the wet/dry etching used in this work. Etch rates were calculated using the average thickness divided by the time it took to completely remove the film from the substrate. Large variations were observed among the different films using the same etching technique. For example, the ISO and AlO_x could not easily be dry etched, but the SiO_x and SiN_x were easily removed using the same technique.

Table 2.2. Etching techniques details.

Method	Material	Chemicals/Process conditions	Etch rate (nm/s)
Wet etching	**AlO_x**	**Buffered oxide etchant (HF)**	**0.17**
	SiO_x	**Buffered oxide etchant (HF)**	**0.63**
	SiN_x	**Buffered oxide etchant (HF)**	**1.67**
	Mo/Cr	Buffered oxide etchant (HF)	0.00
	ISO	Buffered oxide etchant (HF)	99.99
	ISO	**HCl (1.2%)**	**0.17**
	AlO_x/ SiO_x/ SiN_x/Cr/Mo	HCl (1.2%)	0.00
	Cr	**Cr etchant (Sigma-Aldrich)**	**0.11**
	ISO	Cr etchant (Sigma-Aldrich)	99.99
	SiN_x /SiO_x /AlO_x	Cr etchant (Sigma-Aldrich)	0.00
Dry etching	**Mo**	**CF_4:50 sccm; 150 mTorr; 100 W**	**0.06**
	Cr	CF_4:50 sccm; 150 mTorr; 100 W	0.00
	ISO/ZnON	CF_4:50 sccm; 150 mTorr; 100 W	0.00
	AlO_x	CF_4:50 sccm; 150 mTorr; 100 W	0.00
	SiO_x	**CF_4:40 sccm O_2:10 sccm; 150 mTorr; 100 W**	**0.83**
	SiN_x	**CF_4:45 sccm O_2:5 sccm; 150 mTorr; 100 W**	**1.00**

It should be noted that the semiconductor films used in this work were very sensitive to acid. The semiconductor films were etched off as soon as the substrate was soaked into the acid. In most cases, if the acid was strong (e.g. undiluted), the semiconductor dissolved into the acid even if it was covered by a photoresist. Wet

etching became a lift-off process in such circumstances. The residual photoresist did not dissolve in the acid, and the remaining photoresist after wet etching caused great difficulty in the following steps. Through multiple experiments, it was found that 1.2% HCl was the most suitable wet etching solution (i.e. no lift-off observed, acceptable etch rate) for the ISO film.

The selectivity of etching provided an opportunity to compensate for the non-uniformity originating from the equipment. If properly used, selectivity could not only keep the previous layers undamaged, but could also increase the tolerance for mistakes in fabrication. The combination of two layers using selective etching to pattern the top layer is given in Table 2.3. The chemicals/process conditions in the table ensured that the bottom layer was not damaged during the etching. These combinations were heavily relied upon to improve the robustness and yield of the TFT process.

Table 2.3. Selective etching that protects the bottom layer.

Materials		Etching techniques	Chemicals/Process conditions
Top (The layer to be patterned)	Bottom		
Cr	Glass substrate	Wet	Cr etchant (Sigma-Aldrich)
Mo	Glass substrate	Dry	CF_4:50 sccm 150 mTorr 100 W
AlO_x	Mo/Cr	Wet	Buffered oxide etchant (HF)
SiO_x/SiN_x	Mo	Wet	Buffered oxide etchant (HF)
SiO_x/SiN_x	Cr	Dry/Wet	CF_4:40 sccm O_2:10 sccm; 150 mTorr; 100 W / Buffered oxide etchant (HF)
ISO	AlO_x	Wet	HCl (1.2%)
ISO	SiO_x/SiN_x	Wet	HCl (1.2%)
ISO	Mo/Cr	Wet	HCl (1.2%)
Cr	ISO	-	-
Mo	ISO	Dry	CF_4:50 sccm; 150 mTorr; 100 W

2.2.2. TFT Structure and Fabrication Process

The TFT structure has large impact on its electrical performance. A well-designed structure can increase the efficiency of both TFT fabrication and device development [85]. There are two major considerations for device structure: the impact on device performance (performance optimisation) and the simplicity of the manufacturing process. For field effect transistors, there are four types of device structures: top-gate bottom-contact (staggered), bottom-gate top-contact (inverted staggered), top-gate top-contact (coplanar), and bottom-gate top-contact (inverted coplanar). Compared with other structures, the bottom-gate top-contact structure deposits the gate dielectric and semiconductor without breaking the vacuum between the two processes. A clean

interface, which determines the subthreshold swing, can be easily obtained using this method. Based on prior TFT development experience, the subthreshold swing was the most difficult specification to improve. Therefore, bottom-gate top-contact was selected as the structure used to develop the ISO TFT.

As shown in Fig. 2.8, a four-mask/six-mask process was used for bottom-gate top-contact TFT fabrication. First, a 100 nm Cr film was deposited by DC sputtering, which was defined by photolithography with chromium etchant as gate electrodes. A 120 nm AlO_x layer was then deposited by ALD at 150°C. Without breaking the vacuum, a 10 nm In-Si-O layer was deposited by RF-sputtering at room temperature. The sample was patterned with buffered hydrogen fluoride and hydrogen chloride to form via holes and semiconductor regions, respectively. Finally, a 100 nm Mo layer was deposited and defined by reactive-ion etching (RIE) for source and drain electrodes. The region without semiconductor and etch stopper layers was used as a capacitor in the TFT circuit.

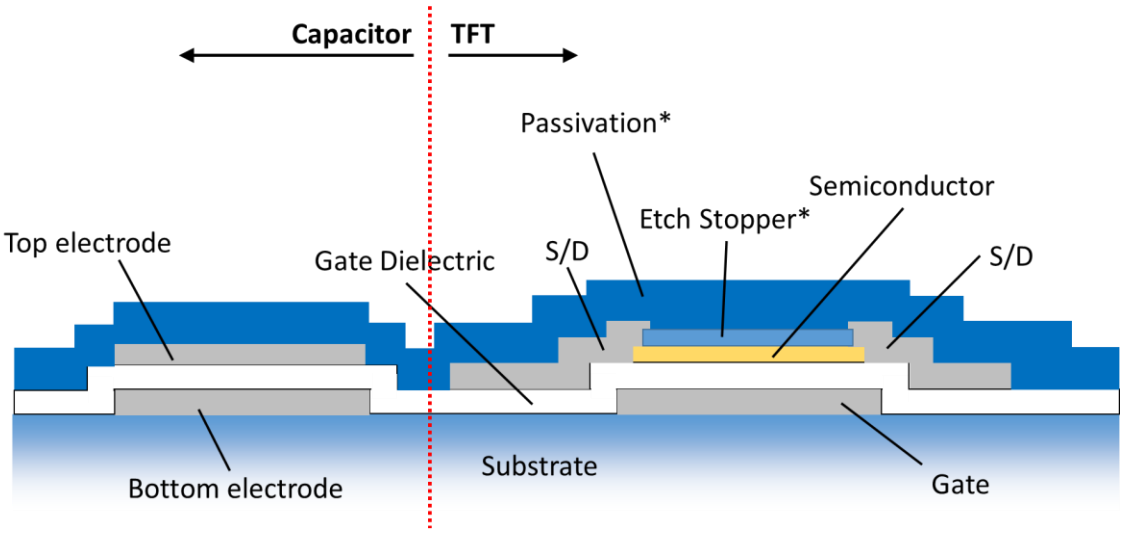

Fig. 2.8. Fabrication process for the In-Si-O TFT (* marks the optional layers in the six-mask process).

The etch stopper and passivation layers (marked with *) were also available in the six-mask process. Theoretically, fabrication with the etch stopper could have better process control at the sacrifice of throughput. The etch stopper could also protect the back interface of the channel from plasma damage, thus reducing the trap density. The optimised active layer thickness could be different for the devices with and without etch stopper layers.

A set of rules (mainly the safe margins) were defined that summarised empirical experience with the TFT fabrication process, providing guidance on layout and circuit design. Based on these rules, high yield of TFT circuits/arrays over a 3-inch glass substrate was guaranteed. This set of design rules was initially generated for simultaneous fabrication of a series of TFT circuits. In general, it is much more conservative than the most advanced process. Fig. 2.9 shows the design rules in the fifth mask. The critical dimensions shown in the graph were generated after obtaining experience with TFT fabrication and the limitations of the photolithography machine (MJB4 Suss Microtec). To summarize, the channel length was fixed to 20 μm for all TFTs, the minimum overlap among layers (alignment safe margin) was 2 μm, and the minimum distance between track centres was 50 μm.

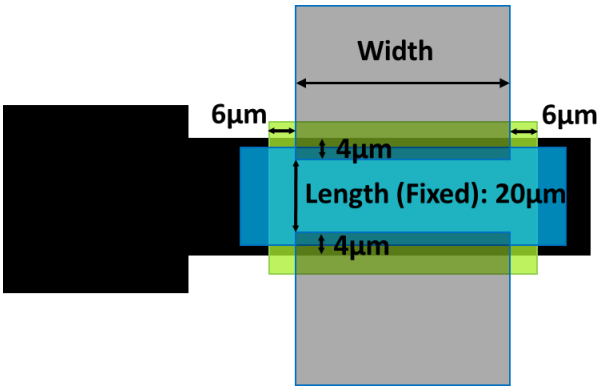

Fig. 2.9. An example of the design rules (the fifth mask).

2.2.3. TFT on Plastic

The demand for flexible electronics has driven the development of TFT on flexible substrates. The proposed TFT process features low fabrication temperature, which is ideal for a flexible substrate. The possibility of applying the full-photolithography TFT process to plastic substrates was explored. The substrate used was the DuPont™ Kapton HN thermal insulating film, which can withstand temperatures up to 400°C (much higher than the proposed process temperature). For a low-temperature process, fabricating a single TFT device on plastic is not challenging as long as the process temperature is controlled below the melting point of the substrate. The photolithography alignment and the yield of TFTs become obstacles, due to the shrinkage of the plastic, especially for a large plastic sheet.

The pressure built up inside the plastic during fabrication was released when it was heated [86]. According to the DuPont™ Kapton HN general specifications, the

shrinkage along the machine direction and transverse direction was less than 0.35% when the film was conditioned by freely suspending it for two hours in an oven controlled to 200°C. Repeating the same experiments, the Kapton HN sheet was annealed as shown in Fig. 2.10 (a). The shrinkage was not uniform, but randomly distributed on the surface of the plastic sheet.

First, alignment marks were added to the plastic sheet, but the misalignments were too small to be observed. To further investigate the shrinkage, the standard four-mask process was used to fabricate a TFT array on the Kapton HN sheet. As shown in Fig. 2.10 (b), 12 yield test regions were used to evaluate the impact of the shrinkage. Large variations in the alignment were found. Pictures of four typical scenarios were taken: Fig. 2.10 (c), (e), and (f) had relatively small misalignments, while the gate and source/drain were completely misaligned in 2.10 (d). Misalignment data (the distance between centres of the TFT on two masks) are summarized in Table 2.4.

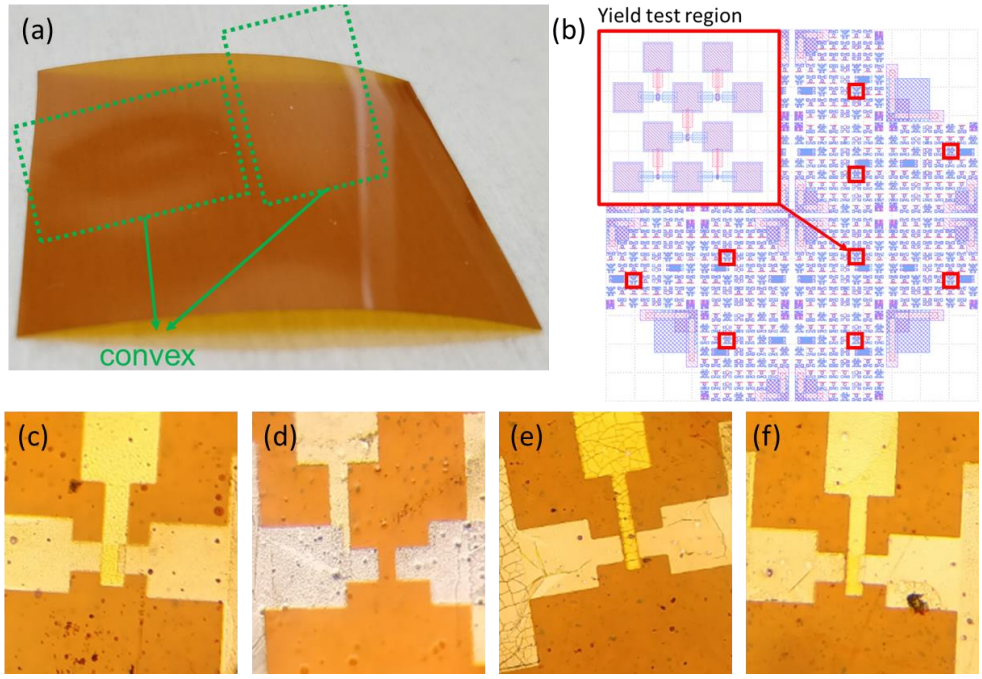

Fig. 2.10. (a) The Kapton HN sheet was heated for two hours at 200°C. (b) The yield test regions on the 3-inch TFT array masks. (c), (d), (e), and (f) are photos of the selected transistors in the yield test regions.

Table 2.4. Misalignment in the yield test regions on the sample.

Position	1	2	3	4	5	6	7	8	9	10	11	12
Misalignment (µm)	7.3	2.6	2.2	3.6	2.6	0.8	1.3	1.4	8.9	18.9	45.1	20.7

The large variations in misalignment proved that the shrinkage problem could not be solved by using a set of scaled-down masks. Possible solutions were most likely in the process before fabrication. If the shrinkage from fabrication could be decreased to that seen before alignment (photolithography), the misalignment would be greatly reduced.

The most fitting solution started by annealing the Kapton film for two hours at 200°C to release the built-in pressure. A rigid substrate, usually a silicon wafer, was used as the backplane to keep the film from deforming. Finally, wafer dicing tapes were used to keep the rigid substrate firmly attached to the Kapton film. The top-view and cross-sectional view of this method are shown in Fig. 2.11 (a) and (b). Wafer dicing tapes have weak adhesion, which will not alter the pressure along the Kapton film when the temperature changes, such that it can be easily peeled off after fabrication. With this method, the masks were aligned. Fig. 2.11 (c), (d), (e), and (f) show four selected TFTs in the yield test region. The misalignment for all TFTs on the substrate was within 4 μm, which is comparable with the process on glass.

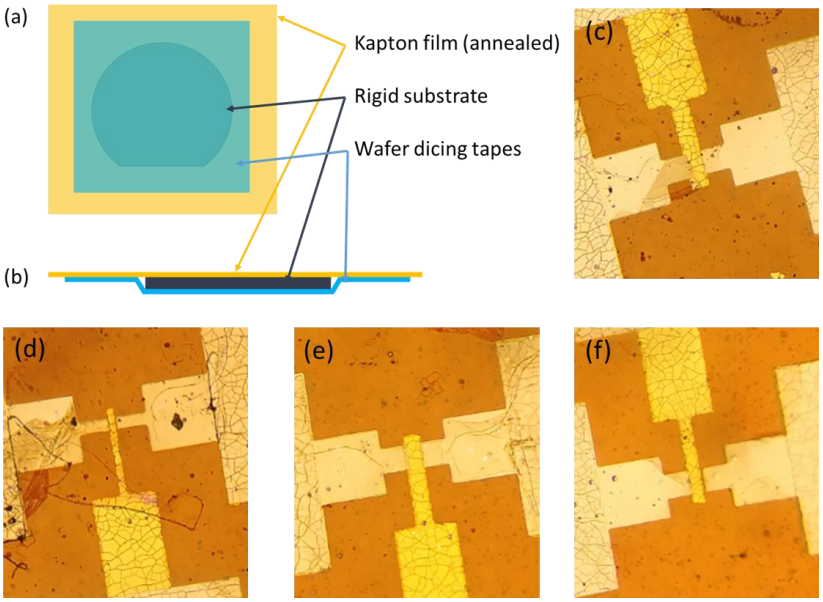

Fig. 2.11. (a) Top-view and (b) cross-sectional view of the proposed solution to plastic shrinkage. (c), (d), (e), and (f) are photos of the selected transistors in the yield test regions on the substrate (improved method).

Fig. 2.12 (a) shows the TFT array that was fabricated on plastic at CAPE. The TFTs on the sample were still functional after bending 100 times to a 1 cm bending radius. The typical performance of TFT on plastic is shown in Fig. 2.10 (b). Hysteresis (<0.5V) was observed in the transfer characteristics. The potential causes of the

hysteresis include annealing temperature too low to remove the defects and the large surface roughness of the plastic increasing traps at interfaces. The potential causes of hysteresis will be analysed and discussed in the third chapter.

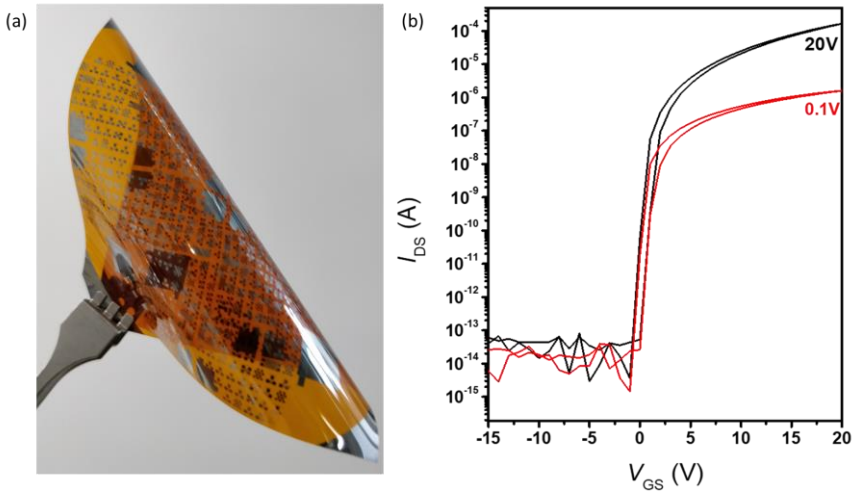

Fig. 2.12. (a) The ISO TFT array on a Kapton HN sheet. (b) Typical performance of the TFT on plastic.

Although the TFT array was successfully fabricated on plastic, it should be noted that circuits cannot be fabricated on plastic, due to the lack of technique to pattern via holes. Wet etching with Hydrofluoric (HF) was used to pattern the AlO_x in the standard process on glass. Unfortunately, this method did not work on plastic. When the plastic was soaked in HF, the entire layer of AlO_x dissolved into the solution. Residual HF on the plastic also made this process too dangerous to be used. New etching methods and materials will continue to be sought for the TFT process on plastic.

2.3. TFT Characterisation

This section discusses the results of a group of experiments used to characterise the TFT. Trial and error experiments are not presented, and repeated measurements have also been removed. Thus, this section presents a simplified device development process.

2.3.1. Dielectric Layer

TFT performance is mainly governed by speed and power. Speed depends upon the drive current or the drain current. Ideally, it should be increased, while decreasing the transistor's static power consumption. The total TFT leakage, of which the gate leakage is a major component, dictates the static power consumption. The leve1-1

model, or the quadratic model, reveals that the drain current of the field-effect transistor is proportional to $\frac{\varepsilon_r}{t_{ox}}$, where ε_r is the relative permittivity and t_{ox} is the dielectric thickness. Theoretically, thin dielectric layers with high relative permittivity can boost the drain current. This is equivalent to an increase in the field-effect mobility. A thinner dielectric layer has a less effective potential barrier to the exchange of charge carriers between the TFT channel and the gate electrode. This results in a higher gate leakage current, because of the direct tunnelling mechanism. The dielectric strength that determines the breakdown voltage is also essential to determining the maximum operating voltage of the TFT.

Fig. 2.13 (a) and (b) show the capacitor array that was fabricated for the dielectric layer testbench. ITO-coated glasses were used as the substrates. First, the edges of the substrates were covered with shadow mask so that the bottom electrode could be easily accessed. The dielectric layer was then deposited. The top electrodes were Mo or Cr, which were patterned during sputtering with a shadow mask. Experiments showed that the thickness of the dielectric layers had to be greater than 50 nm, otherwise the majority of the capacitors were short-circuited, likely caused by dust on the sample or defects in the deposited dielectric layers.

C-V measurements determined the capacitance of the samples that functioned properly. Multiple frequencies were used so that frequency-related characteristics were obtained. Fig. 2.13 (c) shows a typical C-V measurement result in the array. The low-frequency C-V curve had greater noise and slightly higher capacitance. The average capacitance at different frequencies was used to analyse the dielectric layer.

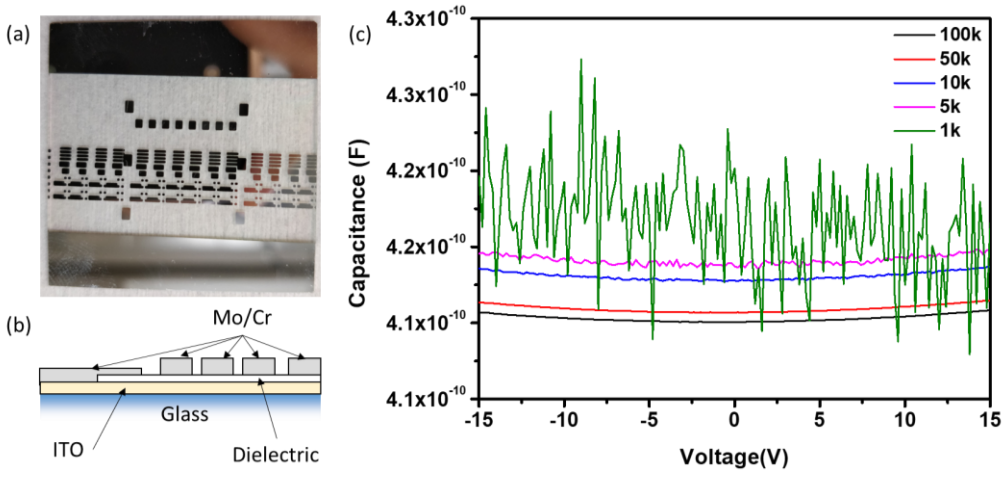

Fig. 2.13. (a) Picture and (b) cross-sectional view of the capacitor array. (c) C-V measurement of a capacitor in the array at different frequencies.

Dielectric strength and leakage current density were measured with the breakdown testbench. Two terminals of the capacitor were connected to a Keithley 4200s SMU. The voltage applied to the capacitor was increased until a large leakage current was observed (breakdown of the dielectric layer). The leakage current density was calculated by dividing the leakage current before breakdown by the total area of the capacitor. Fig. 2.14 shows the measurement results for several frequencies using the following recipes for TFT fabrication: 100nm AlO_x, 310nm SiN_x and 500nm SiO_x. Measurement results on the dielectric layers are summarized in the Table 2.5.

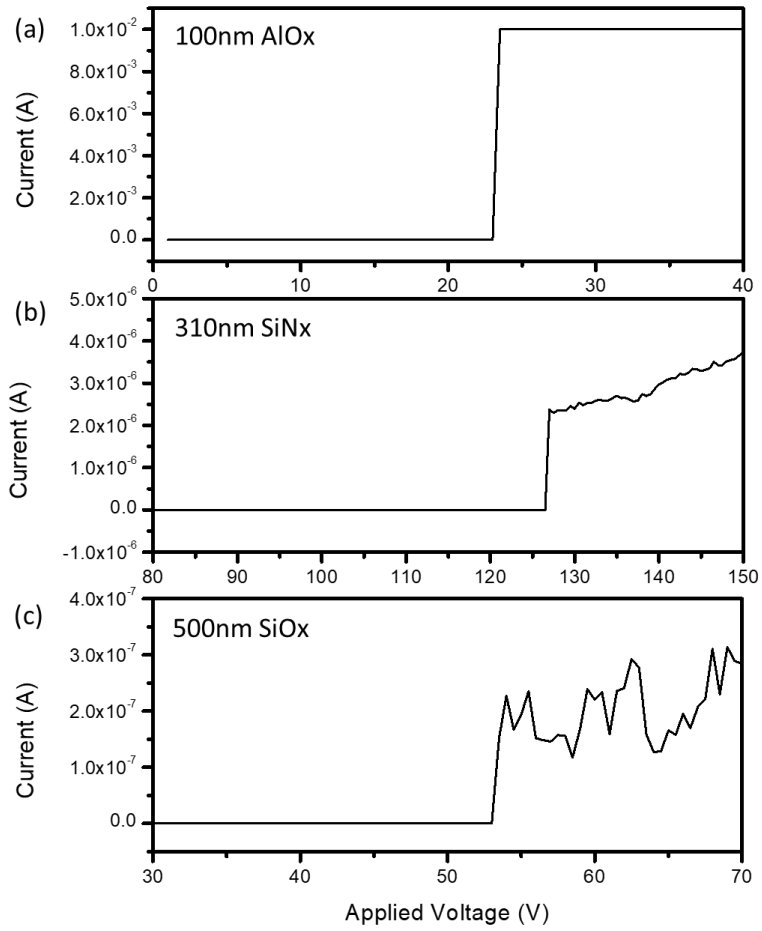

Fig. 2.14. Results from dielectric breakdown testbench for (a) 100nm AlO_x, (b) 310nm SiN_x, and (c) 500nm SiO_x.

The data in Table 2.5 are from the selected films with the highest quality; however, the calculated dielectric constants of the deposited films were smaller than the theoretical values. This could be due to measurement errors in the film thickness, or further improvements to the deposition machine may be needed, which was not realistic for the cluster tools used. In this work, other methods to improve device performance are investigated.

Table 2.5. Measurement results of the deposited dielectric layers.

Dielectric	Cap (pF)	Relative Error (%)	Thickness (nm)	Area (μm^2)	Dielectric Constant	Breakdown Voltage (V)	Dielectric strength (V/m)	Leakage current density (A/ μm^2)
SiNx SiH_4: NH_3=1:10	104	1.15	256	880,838	3.42	155	6.04E5	1.56E-16
SiNx SiH_4: NH_3=1:20	114	1.75	310	880,838	4.53	127	4.09E5	1.84E-16
AlO_x @ 150°C	418	1.43	120	880,838	6.43	23	2.3E5	6.53E-17
SiO_2	66	3.03	500	880,838	4.23	53.5	1.7E5	1.44E-17

2.3.2. Metal-Semiconductor Contact

Interface properties of the metal-semiconductor have a strong influence on TFT performance. Contact resistance at the interface between the source/drain electrode and the semiconductor can affect carrier movement [87]. Assuming other conditions are the same, the transistor with Schottky contacts required more source-drain voltage to attain the same current level as the transistor with ohmic contacts [88], [89]. Previous reports showed that a Schottky-contact transistor had a bend at the beginning of its output characteristics [90], which was caused by the diode behaviour of the two barriers at the metal-semiconductor interfaces. From the perspective of a circuit designer, this bend reduces the linearity of conventional analogue circuits and increases power consumption of conventional digital circuits. Hence, the barrier height and the width between the source/drain electrode and the semiconductor should be minimised.

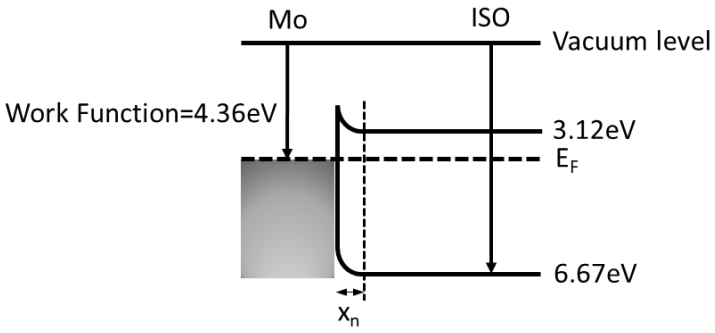

Fig. 2.15. Conduction mechanism for the Mo/ISO contacts.

Based on the characterisation results of the ISO film in section 2.1.4, the conduction mechanism for the Mo/ISO contact is shown in Fig. 2.15. Generally speaking, there are two types of conduction mechanisms for metal/semiconductor

contact: thermionic emission and field emission. Thermionic emission occurs in a wide space charge region, where electrons must jump the potential barrier by emission over the maximum. Conversely, electrons can tunnel through the thin potential barrier in field emission. The equation for the width of the space charge region follows equation 2.1:

$$X_n = \sqrt{\frac{2\varepsilon_s\varepsilon_0\Phi_i}{qN}} \tag{2.1}$$

where ε_s is the relative permittivity of the ISO, Φ_i is the built-in voltage, and N is the carrier concentration. When the space charge region, x_n, is smaller than 2.5 nm, electrons can tunnel through the barrier. Using the data obtained from the Hall effect measurement, the relative permittivity of ISO is given by:

$$\varepsilon_s \leq \frac{{X_n}^2 qN}{2\Phi_i} = 24.91 \tag{2.2}$$

The permittivity of alloy materials $A_{1-x}B_x$ were interpolated from the values of the basic materials as a quadratic function of x:

$${\varepsilon_s}^{AB} = (1-x){\varepsilon_s}^{A} + x{\varepsilon_s}^{B} + (1-x)xC_\sigma \tag{2.3}$$

where C_σ is referred to as a nonlinear or bowing parameter. It is very unlikely that the relative permittivity of ISO would exceed 24.91, since the relative permittivity of SiO_2 and In_2O_3 are 3.9 and 9.0, respectively.

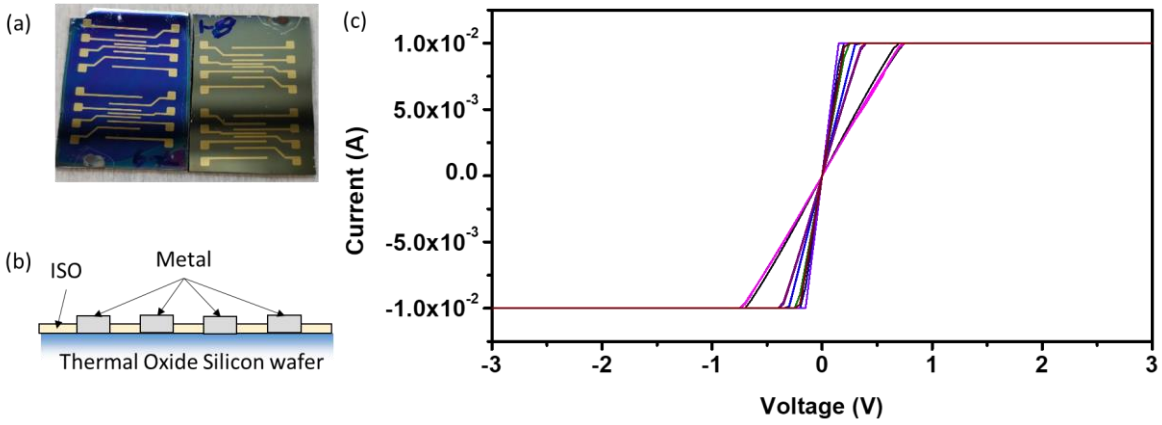

Fig. 2.16. (a) Two samples for the contact resistance measurement. (b) Cross-sectional view of the samples. (c) I-V characteristics of the Mo/ISO contacts with various semiconductor deposition recipes.

To verify this hypothesis, metal-semiconductor-metal devices were built on thermal oxide silicon wafers. First, a thick layer of metal, usually more than 300 nm, was deposited and patterned by a shadow mask. A thinner layer of ISO (50 nm) then followed. The picture and cross-sectional view of the sample are shown in Fig. 2.16 (a)

and (b), respectively. Fig. 2.16 (c) shows the I-V characteristics of the Mo/ISO contacts, where no diode behaviour was found. A wide range of ISO recipes were tested, all of which showed ohmic-contact behaviour.

Apart from the Mo/ISO contact, other available metals were tested at CAPE. All were ohmic-contact. The information is summarised in Table 2.6.

Table 2.6. Verified ohmic metal-semiconductor contacts.

Metal	Work function of the metal	ISO deposition condition			Annealing condition
		RF power	O_2:Ar flow rate	Chamber pressure	
Mo	4.36	150	50:3	4 mTorr	-
		150	50:3	4 mTorr	2 Hr, 150℃
		150	50:3	4 mTorr	2 Hr, 200℃
		150	50:10	4 mTorr	2 Hr, 200℃
		200	50:3	4 mTorr	-
		200	50:3	4 mTorr	2 Hr, 200℃
Cr	4.5	150	50:3	4 mTorr	-
		150	50:3	4 mTorr	2 Hr, 200℃
Au	5.10	150	50:3	4 mTorr	-
		150	50:3	4 mTorr	2 Hr, 200℃
Ni	5.04	150	50:3	4 mTorr	-
		150	50:3	4 mTorr	2 Hr, 200℃

2.3.3. Semiconductor Optimisation

Optimisation of the semiconductor is the key process in TFT development. This is also the most time-consuming process, due to the numerous possible combinations of process parameters. The most influential parameters include deposition power, chamber pressure, reaction gas flow rate ratio, layer thickness, annealing time, and annealing temperature. Using the four-mask process, many sets of deposition and annealing conditions were tested.

Generally, the lower deposition power/pressure (or deposition rate), the better the film quality, and thus, the higher the performance [18], [91]. The controllable range of deposition rate is highly dependent on the equipment. Taking the chamber pressure as an example, the minimum pressure that can strike a plasma in the utilised cluster tool chamber was 4mTorr, which limited the potential to design more aggressive and comprehensive experiments. In this section, the optimisation of the annealing conditions and the semiconductor layer thickness are discussed.

Annealing conditions are crucial to device optimisation [92], [93]. For amorphous metal oxide semiconductors, the as-deposited films might not possess uniform carrier concentration and a stable structure. Possible interface state and deep state locations are shown in Fig. 2.17. There are three major types of defects: front channel interface states, deep states, and back channel interface states. Front channel interface states are induced from the by-product of the ALD process, which is a layer of hydroxy at the interface between the gate dielectric and the semiconductor. Deep states are due to atom dislocations during deposition. During source/drain patterning, high power plasma creates back channel interface states. Annealing helps to improve uniformity and remove the loosely bounded species [94]. Devices with inadequate or incorrect annealing conditions could mislead the investigation.

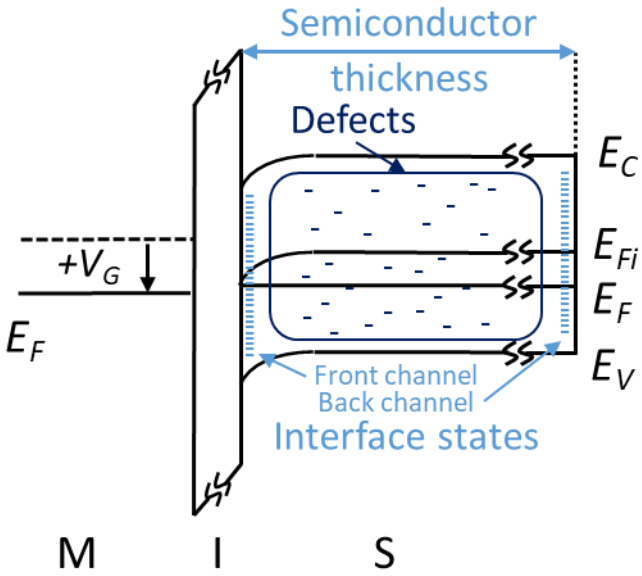

Fig. 2.17. Possible interface state and defect locations in the In-Si-O bandgap diagram.

Three representative annealing conditions were selected to illustrate the impact on device performance. Fig. 2.18 (a) shows the transfer characteristics of the ISO TFT annealed in a glove box filled with nitrogen. The device was always conducting no matter how long it was annealed. For indium-oxide-based semiconductors, the carrier concentration was strongly dependent on the oxygen vacancies. Annealing in a nitrogen environment could possibly remove the defects in the film, but would not compensate for the oxygen vacancies. Thus, no significant improvement was observed. Fig. 2.18 (b) and (c) show the transfer curves of two samples that were annealed in the atmosphere at 150°C and 200°C. The shapes of the transfer curves changed after thermal annealing,

where the subthreshold swing and hysteresis were greatly reduced. The trend was more pronounced for the TFT annealed at 200°C.

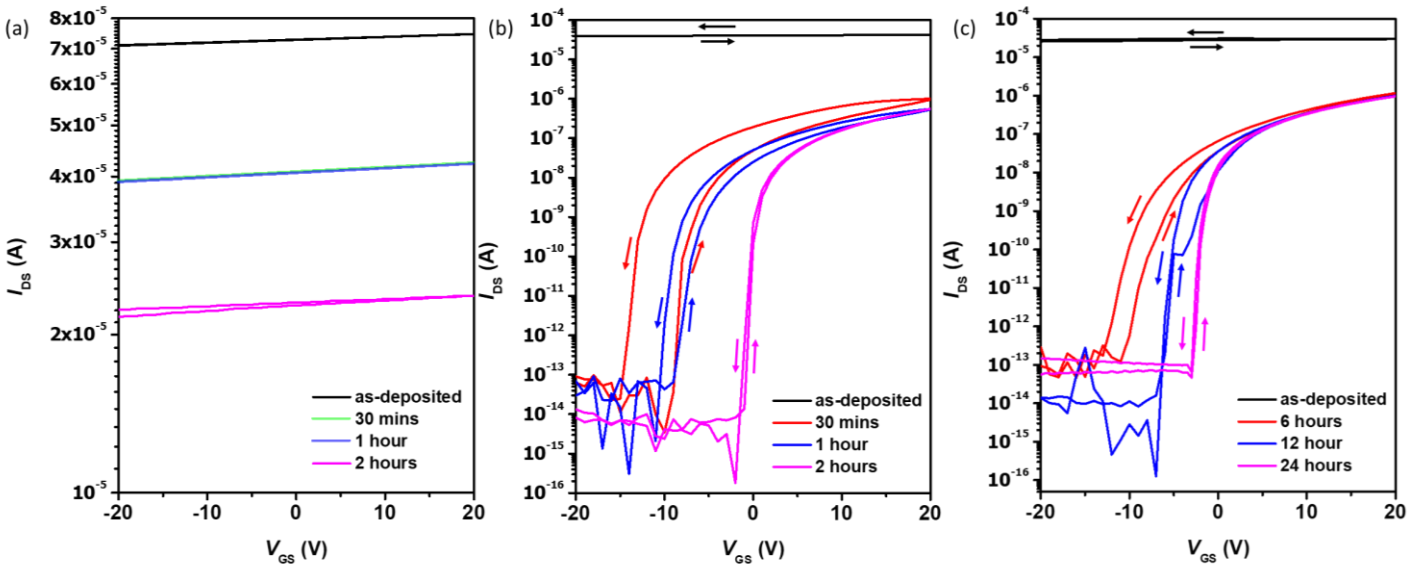

Fig. 2.18. The transfer characteristics at V_{DS}=10V for (a) the ISO TFT annealed in nitrogen (glove box) at 200°C, (b) the ISO TFT annealed in atmosphere at 200°C, and (c) the ISO TFT annealed in atmosphere at 150°C.

The extracted hysteresis and mobility are shown in Fig. 2.19. To the detriment of mobility, increasing the annealing temperature can reduce the time required for the transfer characteristics to converge to where hysteresis is zero.

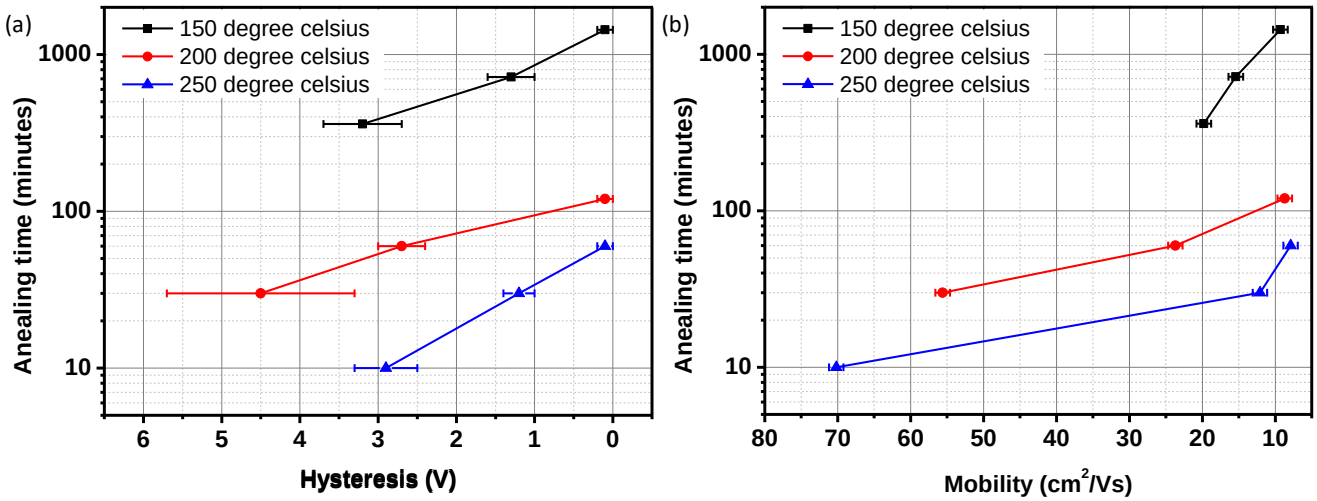

Fig. 2.19. Transistor properties of ISO TFT over various annealing temperatures, showing changes in (a) hysteresis and (b) mobility.

There are three commonly accepted mechanisms that cause hysteresis: electron/hole trapping at the interface of the gate insulator, the creation of ionized

oxygen vacancies, and donor-like defect creation in the channel [95]. Thermal treatment promotes the migration and oxidation of atoms, which reduces the density of both defects and carriers. It is reflected in the decrease of mobility and hysteresis as the annealing time increases. Annealing in atmosphere reduces oxygen vacancies. The presence of an oxidizing agent is essential for controlling the oxygen vacancies in amorphous oxide semiconductors. Annealing in a vacuum or in nitrogen could increase the defect concentration in amorphous oxide semiconductors, due to the loss of oxygen leading to oxygen vacancies, which act as dopants. The annealed ISO film can remain stable for a long period of time in the atmosphere, due to the high dissociation energy of the silicon-oxygen bond, which suppresses the formation of oxygen vacancies, and thus, improves the stability of this indium-based semiconductor.

Based on the two hours at 200℃ annealing condition, the electrical performance of the ISO TFT was investigated by varying the channel thickness. Limited by the equipment, the semiconductor could only be deposited with a thickness that was an integral multiple of 5 nm. The 5nm channel did not conduct, and when the channel was thicker than 20 nm, the selected annealing condition could not completely remove hysteresis. Subsequently, three comparable scenarios remained: 10, 15, and 20 nm.

Fig. 2.20 (a) shows the transfer characteristics of the ISO TFTs with different channel thicknesses. A parallel shift was observed when the thickness increased. The extracted mobility and threshold voltage are shown in Fig. 2.20 (b) and (c). When the thickness increased, the field-effect mobility remained nearly the same, while the threshold voltage decreased.

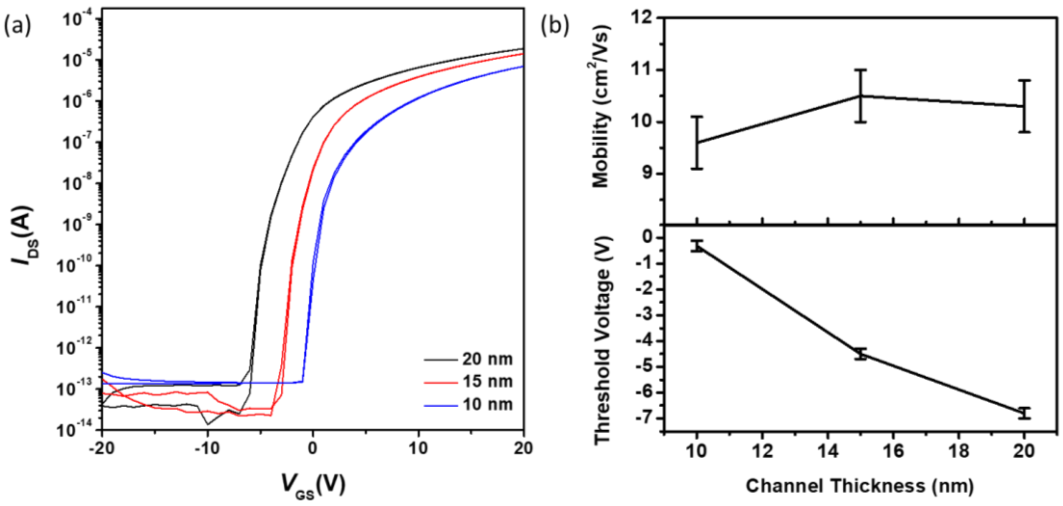

Fig. 2.20. (a) The transfer characteristics of the ISO TFTs with different channel thicknesses at V_{DS}=10V. (b) The corresponding extracted mobility and threshold voltage.

For TFTs, the threshold voltage extracted using the level-1 model did not have a clear physical meaning like that of a MOSFET. However, it did reflect the relative voltage required to switch on the transistor. In the TFT, the balancing of the gate charge was performed by the charge strapped in the defect states within the band gap of the ISO. As the gate voltage increased further, the Fermi level moved toward the conduction band edge. If sufficient carriers were provided, the ISO TFT was switched on. Assuming the extracted threshold voltage is a function of the turn-on voltage, the relationship between threshold voltage and thickness can be obtained as:

$$\Delta V_{th} = \Delta V_{on} = \left(\Phi_{ms} + \frac{qN_{trap}t_{s1}}{C_{ox}}\right) - \left(\Phi_{ms} + \frac{qN_{trap}t_{s2}}{C_{ox}}\right) = \frac{qN_{trap}\Delta t_s}{C_{ox}} \qquad (2.4)$$

where Φ_{ms} is the work function difference between the semiconductor and the metal, N_{trap} is the effective concentration of trap states, and t_s is the effective channel thickness. A thicker semiconductor layer could have a larger effective channel thickness, which would eventually lead to a decrease in the threshold voltage.

In conclusion, to increase the yield while maintaining a reasonable efficiency, the following were chosen as the optimised semiconductor recipes:

- Thickness: 10nm
- Annealing conditions for TFTs on glass: two hours, 200℃
- Annealing conditions for TFTs on plastic: 24 hours, 150℃

Chapter 3

Uniformity and Stability of TFTs

For TFT processes, it is crucial to collect uniformity and stability data. These data verifies and quantitates the capability of the process in system integration and circuit design. In this chapter, the standard four-mask ISO TFT process is investigated. Section 3.1 introduces the parameter extraction toolkit, section 3.2 delivers uniformity data and statistical analysis, and section 3.3 discusses the TFT stability issues and recovery methods.

3.1. Parameter Extraction Toolkit

Collecting uniformity data involves a great deal of parameter extractions. To better control the accuracy of extractions and reduce the repetitive workload, a parameter extraction toolkit was developed using MATLAB. Fig 3.1 shows the GUI of the parameter extraction toolkit. Users must select or change the TFT model for data fitting first. The extraction process was designed for each model, and the values of the parameters then extracted. If the errors between the measurement data and the fitting model are acceptable, the toolkit can be used to generate a Verilog-AMS written TFT model. The model can be implemented in any SPICE-based simulation environment; for example, Cadence and HSpice.

The accuracy of the extraction is also influenced by the selected TFT model. Unique properties of TFTs with different semiconductors must be captured in matching TFT models. With the help of Dr. Xiang Cheng, the TFT model for the ISO TFT was

established based on a model that was originally developed by Dr. Sungsik Lee at the Hetero-Genesys Laboratory [96].

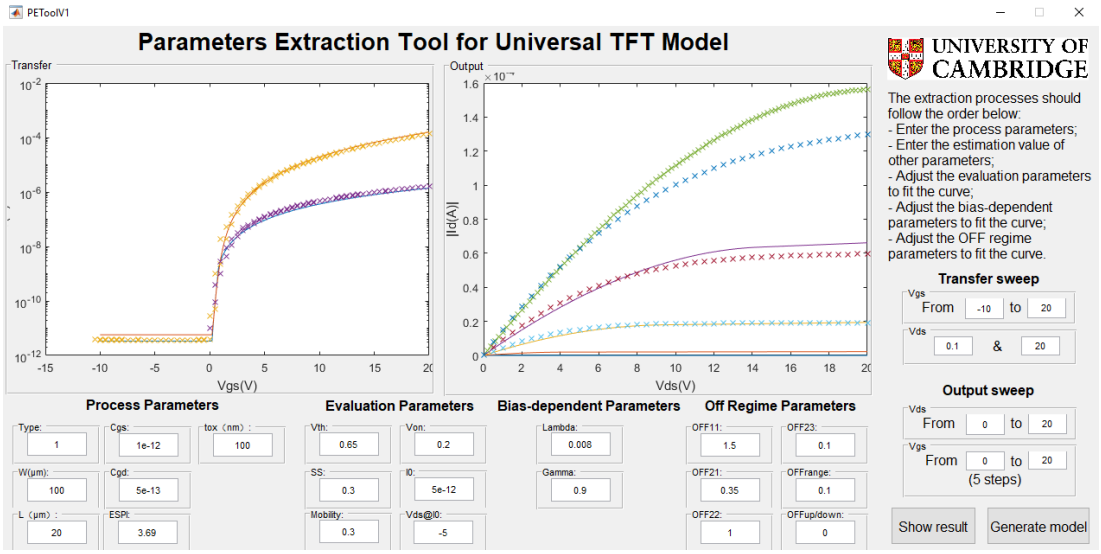

Fig. 3.1. GUI of the parameter extraction toolkit for a universal TFT model

The ISO TFT model combined trap-limited conduction with percolation conduction. The effect of trap-limited conduction was considered to be the ratio of free carrier density (n_{free}) and trapped carrier density (n_{tail}), yielding the trap-limited conduction (TLC) constant:

$$\gamma_{TLC} = \frac{n_{free}}{n_{free}+n_{tail}} \tag{3.1}$$

Percolation conduction associated with the potential barriers above the conduction band minimum were considered to be intrinsic mobility, assuming a Gaussian distribution of potential barriers (mean value of φ_{B0}). These conditions yield the combined mobility model:

$$\mu_{FE} = \mu_0 \left(\frac{n_{free}}{n_{free}+n_{tail}}\right)\left(\frac{C_{ox}}{Q_{ref}}\right)^{\alpha_p}(V_{GS}-V_T)^{\alpha_p} \tag{3.2}$$

where μ_0 is the intrinsic mobility and Q_{ref} is a parameter generated when solving Poisson's equation for the total volume charge density at the gate dielectric. α_p is a parameter derived from the percolation mechanism.

Using equation 3.2, the current-voltage relation with a V_{GS} above the threshold voltage was derived based on the drift of current principle:

$$I_{\text{Drift}} = \mu_0 \left(\frac{n_{free}}{n_{free}+n_{tail}}\right)\frac{W}{L}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS}-V_T)^{\alpha_p+1}V_{DS} \tag{3.3}$$

The sub-threshold current was a result of diffusion current, such that:

$$I_{\text{Diff}} = \mu_0 \frac{W}{L} \frac{C_{ox}^{\alpha_d+1}}{Q_d^{\alpha_d}} (V_{GS} - V_{FB})^{(\alpha_d+1)} V_{DS} \tag{3.4}$$

These equations were combined into a total drain current using a harmonic average:

$$I_{DS} = (I_{\text{Diff}}^{-m} + I_{\text{Drift}}^{-m})^{-1/m} \tag{3.5}$$

This model featured high speed circuit simulation since only a few parameters were used, which is essential for large-scale circuit design and simulation. The parameter extraction toolkit also provided users with choices depending on model preferences. The users could choose a more physical model (complicated parameter extraction steps and slower simulations), or the compact model, which was simpler in terms of the number of parameters used.

3.2. Uniformity

During the development of the TFT process, great progress was made in improving and sustaining wafer uniformity for the deposition of different films on the 4-inch glass substrate. Use of selective etching has proven effective in the patterning steps. As the process moves into circuit fabrication and system integration, extracting the uniformity data to verify circuit design is critical to the yield realised. In this section, the intra-wafer uniformity and batch-to-batch uniformity were investigated using a TFT array.

3.1.1. Intra-Wafer Uniformity

Intra-wafer variations, including inter-die and intra-die variations, are caused by the manufacturing tolerances that affect the mean value of parameters inside a wafer [97]. Without proper design and consideration, variations among parameters within a wafer can result in performance degradation or failing circuits. In most cases, the variations are uncontrollable and impossible to completely eliminate [98]. For example, the thickness variations caused by the random diffusion flux of precursors in the ALD reactor were related to the equipment and could not easily be prevented when designing the equipment. While uncontrollable, these variations were not completely random, but were represented as stochastic processes with dependence on the spatial wafer coordinates. Typically, the impact of variations was coupled. This made it more difficult to identify an individual contribution, such that its variation could be isolated and extracted. Therefore, the impact of the variations was parameterised using the TFT

performance parameters, namely the threshold voltage, field-effect mobility, subthreshold swing, and the off current. The gate capacitance per area (C_{ox}/t_{ox}) was assumed to be a constant across the entire substrate, thus, the variation of gate capacitance was reflected in the field-effect mobility.

The test regions in the TFT array used during the uniformity measurements are illustrated in Fig 3.2. For a 4-inch substrate with a 3 mm exclusion edge, there were 16 dies in total. Each die had 12 identical test regions. Five TFTs with critical dimensions ranging from 1 μm to 8 μm were fitted into the test region.

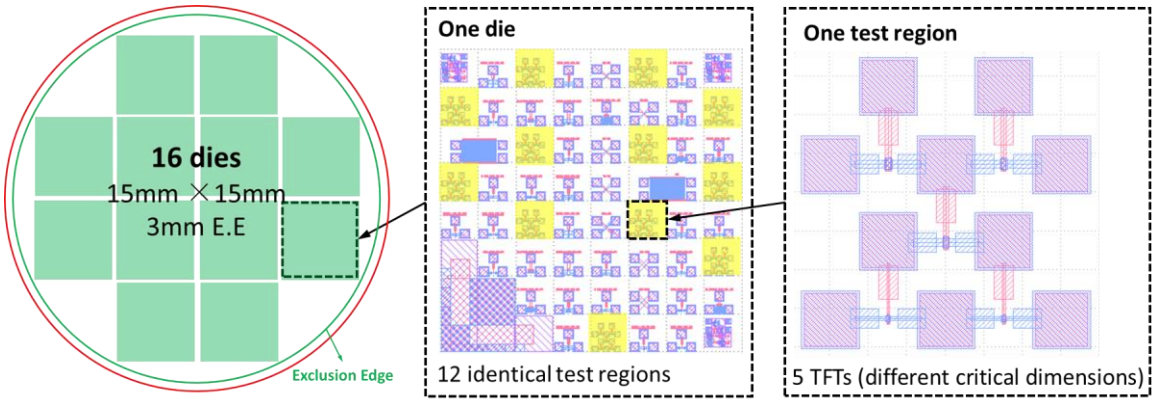

Fig. 3.2. Test regions and stamp design of the TFT array on a 4-inch substrate.

Fig. 3.3 (a) and (b) show the transfer characteristics of the 2 μm ISO TFT in each die and the mappings of extracted TFT parameters, respectively. Clear intra-wafer variations were found in the transfer characteristics. The mappings of extracted TFT parameters offered more insight into the intra-wafer variations. Gradual transitions were observed in the threshold voltage and field-effect mobility mappings, while the mappings for subthreshold swing and off-current were more random.

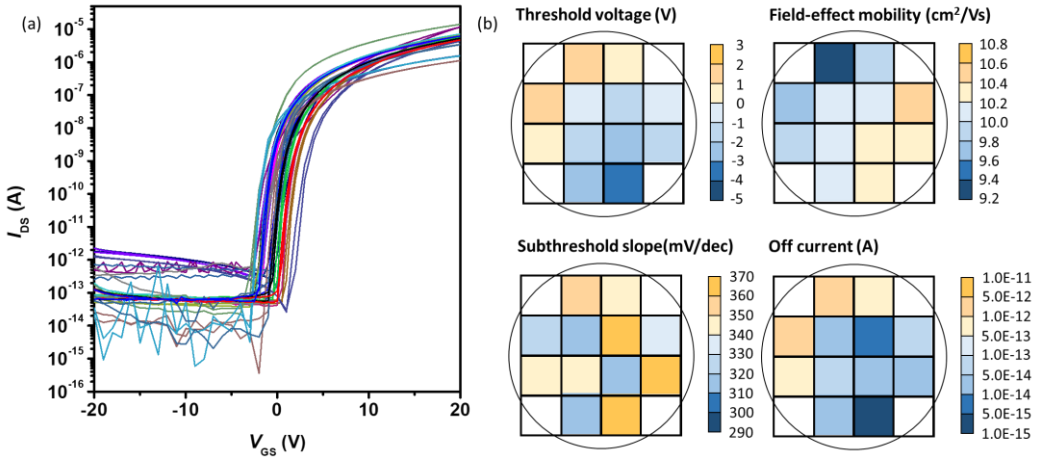

Fig. 3.3. (a) The transfer characteristics of 16 ISO TFTs distributed across a 4-inch glass substrate at V_{DS}=10V. (b) Extracted ISO TFT parameters, in the form of wafer spatial distribution maps.

The random variation could have been triggered by a wide range of actions, including imperfection in photolithography, etching, annealing, or contaminations in the substrate. In contrast, the gradual transition reflected the impact of one major disturbance or the combined impacts of several disturbances in the fabrication process. For example, assuming that a concentric ring pattern was found in the dielectric, the thickness variation of the dielectric layer was large enough to be considered the most influential factor in TFT performance. This variation was reflected in the ring pattern field-effect mobility mapping when using the parameter extraction toolkit.

Generally, the intra-die variations were much smaller than the inter-die variations. Taking the threshold voltage variation as an example, the intra-die mapping is shown in Fig. 3.4 (a). The magnitude of the intra-die threshold variation was less than 2V, which was much smaller than the inter-die variation. As shown in Fig. 3.4 (b), assuming both variations followed the normal distribution, the intra-die sample had a variance that was only one-fifth the inter-die variance. The shift in mean threshold voltage was a result of the systematic variations.

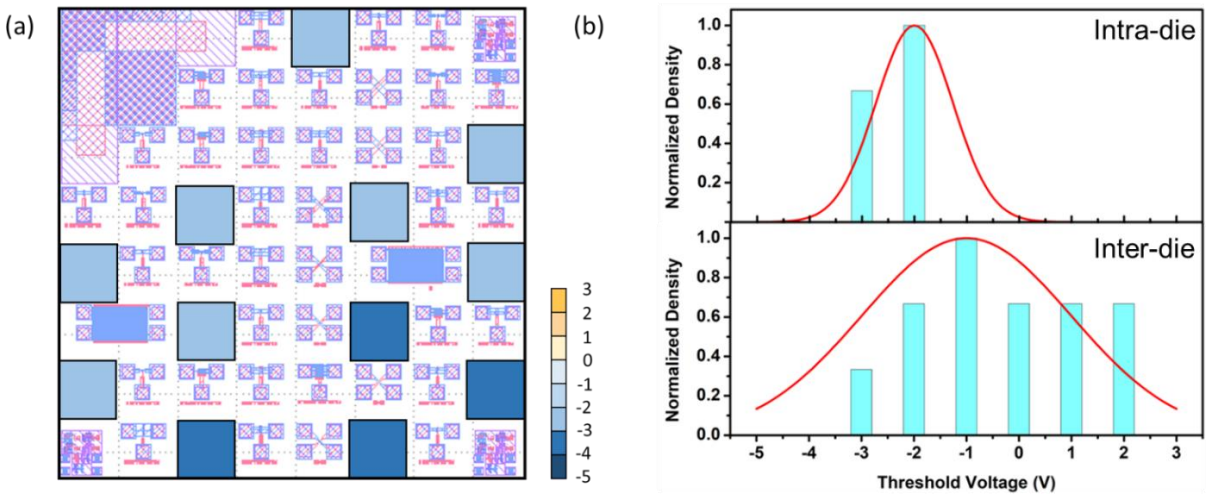

Fig. 3.4. (a) Intra-die threshold voltage mapping. (b) Comparison of the intra-die and inter-die variations.

3.1.2. Batch-to-Batch Uniformity

More than 10 batches of the TFT using the same fabrication process were measured. The selected TFTs were located in the die at the same position on the substrate, and all had identical aspect ratios and critical dimensions. During the measurements, batch-to-batch threshold voltage variation was insignificant if intra-wafer variations were

considered. Meanwhile, the batch-to-batch mobility and subthreshold swing variations were larger than/comparable to the intra-wafer variations.

Fig. 3.5 (a) shows two sets of transfer characteristics; each set contains data from five TFTs. A clear difference was found between these two sets of data. The average value of the extracted parameters from the five TFTs in one batch formed one data point in the statistical analysis. The distribution of mobility and subthreshold swing from the 10 batches of TFTs are shown in Fig. 3.5 (b) and Fig. 3.5 (c), respectively. Variance of batch-to-batch mobility was twice the intra-wafer variance, while the variance of subthreshold swing was similar to intra-wafer variance.

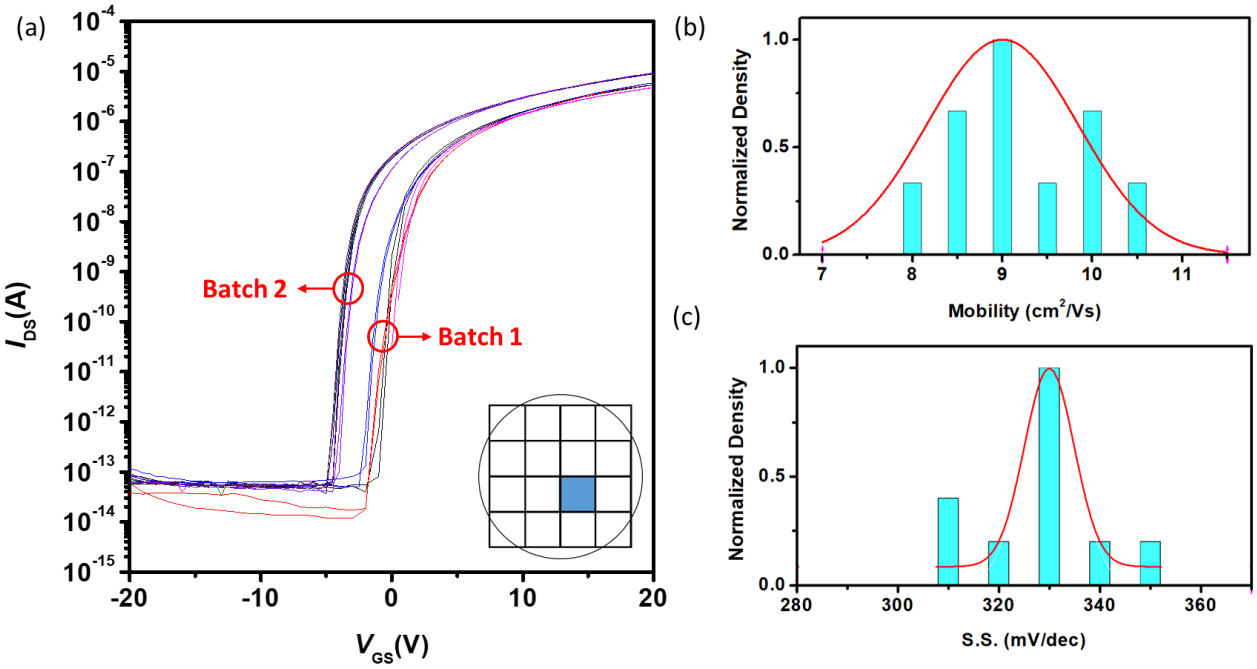

Fig. 3.5. (a) Comparison of 10 selected transfer characteristics from two batches of the TFT array, insert is the position of the selected die. The batch-to-batch (b) mobility and (c) subthreshold swing variations.

3.1.3. Monte Carlo Simulation Environment

Monte Carlo analysis is a statistical analysis that essentially calculates the response of a circuit when the device model parameters are randomly varied between specified tolerance limits according to a statistical distribution. As shown in Table 3.1, parameters inside the variation model consisted of two parts: the mean and the standard deviation (**σ**). The values used were determined based on the uniformity data in previous sections and experience in fabrication. Taking threshold voltage as an example, the function of those two values can be expressed in the following equation:

$$V_{th} = V_{th0} + \Delta V_{th\_mean} + \sigma_{th} \tag{3.6}$$

For a Monte Carlo simulation, the statistical data was selected according to different situations. It is highly recommended that stricter conditions are used in circuit design verification.

Table 3.1. Statistical data for the Monte Carlo analysis.

Uniformity	Parameter variation	Standard deviation	Notes
Global	Channel width	3% of the width	Estimate
	Channel length	3% of the width	
Batch-to-batch	Field-effect mobility	1.12 cm^2/Vs	
	Subthreshold swing	11.82 mV/dec	
	Off current	5e-14 A	
Intra-wafer (4-inch)	Threshold voltage	1.33 V	
	Field-effect mobility	0.10 cm^2/Vs	
	Subthreshold swing	12.20 mV/dec	
	Off current	5e-14 A	
Intra-die (15mm×15mm)	Threshold voltage	0.42 V	
	Field-effect mobility	0.05 cm^2/Vs	
	Subthreshold swing	10.40 mV/dec	
	Off current	5e-14 A	

3.3. Stability

This section presents the analysis of the ISO TFT stability via bias stress and light illumination. The ISO TFT was biased for up to four hours at three different temperatures. The shift of threshold voltage with stress temperature at different times fit the empirical equation well. The empirical equation was modified from the stretched exponential model. It further improved the consistency by separating the temperature dependence of β. Transfer characteristics of the ISO TFTs were measured under light illumination at different wavelength. A wavelength shorter than 660 nm impacted the transfer characteristics. Persistent photoconductivity measurements matched the results of typical amorphous oxide semiconductors, which indicated that the distortion of transfer characteristics was caused by light-induced shallow doubly-ionised donor states.

3.2.1. Bias-Stability

The bias stress measurements were conducted with a Lake Shore Model PS-100 table top cryogenic probe station and a Keithley 4200. Stress temperature was controlled by a model 336 controller. All measurements were taken in a dark environment. Fig. 3.6 shows the effect of bias stress on typical transfer characteristics

at 20°C. A constant V_{DS} of 20V and V_{GS} of 0.5V were applied for up to four hours. The bias was interrupted at certain times to record the evolution of the transfer characteristics. Dual sweeps were used to obtain the transfer characteristics. V_{GS} was a sweep in the range of -20V to +20V and V_{DS} was biased at 0.5V. All the transfer curves had similar shapes, negligible hysteresis, and shifted toward the positive direction along the gate voltage axis. This behaviour was also observed in the measurements at 50°C and 100°C.

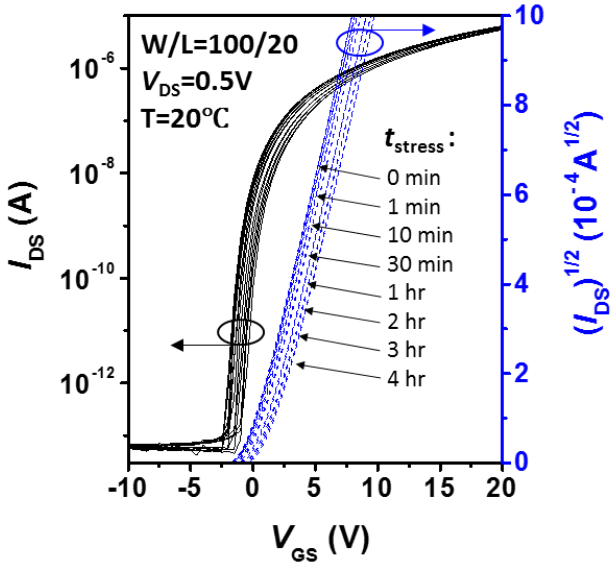

Fig. 3.6. Evolution of bias stress (V_{GS} = 20V, V_{DS} = 0.5V) on the transfer characteristics of the ISO TFT at 20°C.

To quantitatively analyse the shifts of transfer curves, three parameters were extracted: mobility, threshold voltage, and subthreshold swing. The extracted results are summarized in Fig. 3.7. Taking the error from the extraction procedures into account, the shifts in mobility and subthreshold swing were insignificant. The shift of threshold voltage followed a stretched-exponential behaviour. Consistent with previous reports [99]–[101], the conventional stretched-exponential equation fit the data with a temperature-dependent β. However, the equation already used temperature as one of its parameters, such that the temperature dependence of β was redundant and broke the equation's consistency. Obtaining a unified equation will help identify the temperature-dependent phenomenon of bias-induced threshold shift.

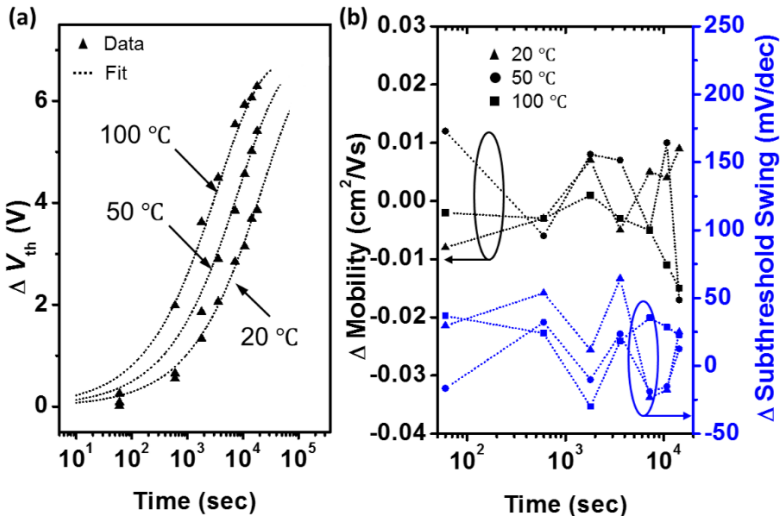

Fig. 3.7. Parameters extracted from bias stress measurements at three different temperatures: (a) threshold voltage shift versus stress time, and (b) mobility and subthreshold swing shift versus stress time.

By moving the temperature dependence of β into another parameter α, a new empirical equation was formed that fit all the data at different temperatures with constant parameters:

$$|\Delta V_{th}| = |\Delta V_0| \left\{ 1 - \exp\left[-\left(\frac{t_{stress}}{\alpha + \tau_0 \exp(\frac{E_r}{kT})} \right)^{\beta} \right] \right\} \tag{3.7}$$

As shown in Fig. 3.7 (a), using V_0 = 8.2 V, α = 2.836 × 10^3 s, τ_0 = 8.209 × 10^{-4} s, Er = 0.44 eV, and β = 0.58, the threshold voltage shift data was well fitted by equation 3.5. However, for the first two data points, namely those at one and 10 minutes, deviations were found between the measured data and the model. This was because bias-induced negative threshold shift during the measurements generated non-negligible errors. A single transfer measurement takes three minutes, which was on the same level as the bias time of the first two data points. The current at negative V_{GS} bias was much smaller than the on-current and it took more time to measure the low current region, where the gate was biased with negative voltage. Since negative gate voltage bias can generate negative threshold voltage shift, the inevitable negative bias had a large impact on the threshold voltage shift when the bias time was short.

C-V characteristics were collected during the bias stress measurement. As shown in Fig. 3.8 (a), when the gate voltage was smaller than -2V, the ISO film was depleted of free carriers. As gate voltage increased, the channel gradually formed from electrons and the semiconductor eventually entered accumulation mode. The capacitance in MOS theory follows:

$$C = \frac{d\,Q_g}{d\,V_g} = 1/[\frac{1}{C_{ox}} + \frac{1}{C_{accu}}] \tag{3.8}$$

where C_{accu} is the channel capacitor in accumulation mode. In response to the AC signal, the electrons in the accumulation layers increased and decreased at the AC frequency. This accumulation layer, or the conducting channel, acted as the bottom electrode of the capacitor. It was proportional to the carrier density and inversely proportional to (V_g-V_{fb}). Assuming the carrier density was irrelevant to bias stress, the change in MOSCAP indicated that the flat-band voltage of the ISO TFT changed during the bias stress. In the presence of charges in the oxide or at the oxide-semiconductor interface, the flat-band voltage was given by:

$$V_{fb} = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x)\, x dx \tag{3.9}$$

where the second term is the voltage across the oxide due to the charge at the oxide-semiconductor interface and the third term is due to the charge density in the oxide. The decreasing flat-band voltage in Fig. 3.8 (b) reflects the fact that defects increased when the TFT was biased with voltage stress.

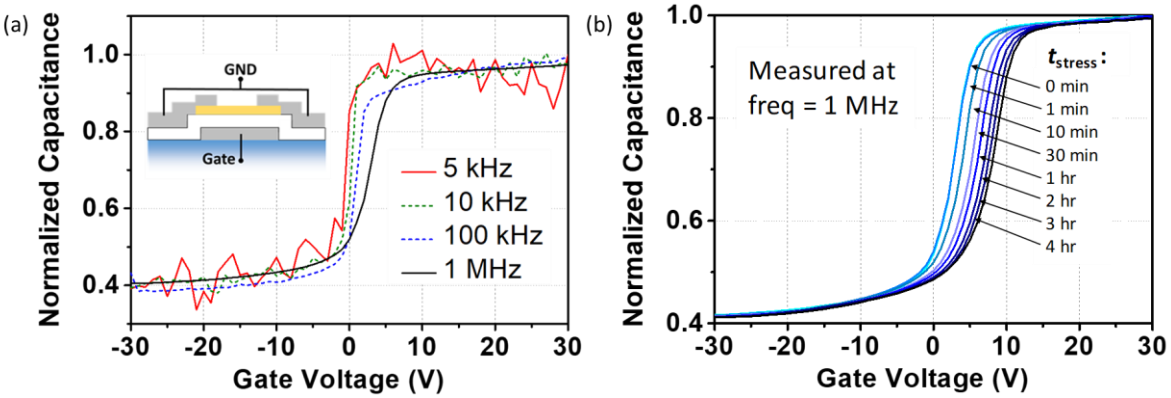

Fig. 3.8. (a) C-V characteristics as a function of frequency for the ISO TFTs, insert is the TFT configuration. (b) Evolution of bias stress (V_{GS} = 20V, V_{DS} = 0.5V) on the C-V characteristics at 20°C.

Based on the previous analysis, the threshold voltage shift reflected the change of interface states and defects inside the dielectric. Assuming the metal semiconductor work function difference applied, φ_{ms}, was constant. Threshold voltage was a function of oxide trapped charge in the dielectric and the interface states. It is widely accepted that subthreshold slope/swing is directly related to the density of semiconductor-dielectric interface states. In the stress measurements, subthreshold swing remained nearly the same, which indicated that interface states did not change significantly. Therefore, the primary cause of the threshold voltage shift in the bias stress

measurement was hot carrier injection and trapping in the dielectric layer. This trap could be removed using low temperature annealing. The bias stress performance could thus be improved by improving the dielectric layer quality, for example, by using higher quality precursors in the ALD.

3.2.2. Photo-Stability

In the light illumination measurements, mounted LEDs and a T-Cube LED Driver from Thorlabs were used to generate light at different wavelengths. The LEDs were controlled by an Agilent 33500B signal generator. The experiments were conducted in a dark environment, where the impact of ambient light was reduced to the bare minimum. Fig. 3.9 shows the transfer characteristics of ISO TFTs under exposure to light at different wavelengths. When the wavelength, λ, was smaller than 660 nm, the shape of the transfer characteristics was altered by the illumination. The subthreshold swing, off-current, and on-current increases were inversely proportional to λ. The figure insert shows the UV-Vis absorbance and the LED spectroscopy. The ISO film strongly absorbed at wavelengths shorter than 400 nm. With an increase in wavelength, the absorbance became weaker, and nearly zeroed at 500 nm. A small absorbance peak reappeared between 520 nm and 900 nm. Although the ISO film could absorb light from 660 nm and 850 nm LEDs, photons at these wavelengths did not possess enough energy to generate photoconductivity. Thus, no obvious change in the transfer characteristics was observed.

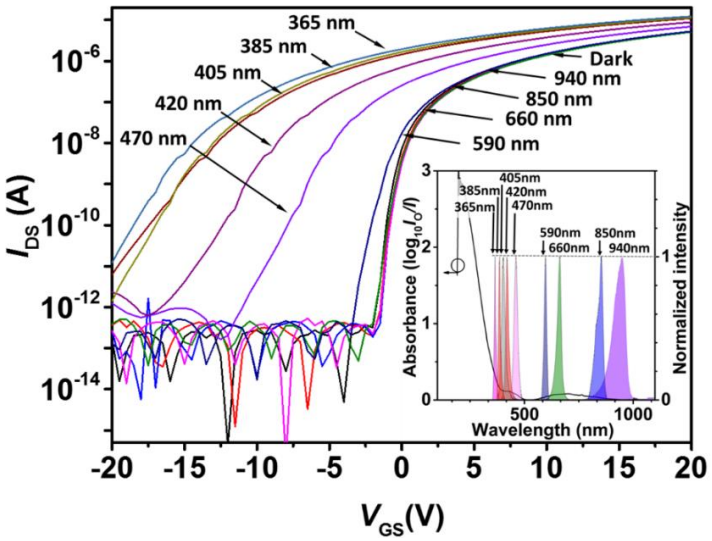

Fig. 3.9. Transfer characteristics of ISO TFTs under exposure to light at different wavelengths (V_{DS} = 0.5 V), insert is the UV-Vis absorbance of the ISO film and normalized spectroscopy of the LED intensities, the spectral data of LEDs were adapted from Thorlabs datasheets.

For amorphous oxide semiconductors, the illumination ionises oxygen vacancy sites, and thus generates shallow doubly-ionised donor states and an un-depleted channel. Confined photo-generated electrons caused persistent photoconductivity. The persistent photoconductivity in an amorphous oxide semiconductor can be eliminated by a positive gate bias [3], [102], [103].

As shown in Fig. 3.10, the generation, recovery, and elimination of photoconductivity were investigated with illumination pulses. A 470 nm LED was selected as the light source. The transistor was biased at a V_{DS} of 20 V and a V_{GS} of -10 V. A 10 second illumination pulse generated photocurrent at the level of 10^{-8}. A 40 second rest in the dark followed, but the TFT did not fully recover from the impact of illumination. To eliminate persistent photoconductivity, an experiment was designed. Using the signal generator, synchronized signals that controlled the light illumination and gate voltage were produced. The interval between the falling edge of the light illumination signal and the rising edge of the gate bias signal was three seconds. With a gate pulse, the drain current went back to the previous value in the dark environment, which indicated that positive gate bias could accelerate recovery, thus, effectively suppressing the persistent photoconductivity in the ISO film.

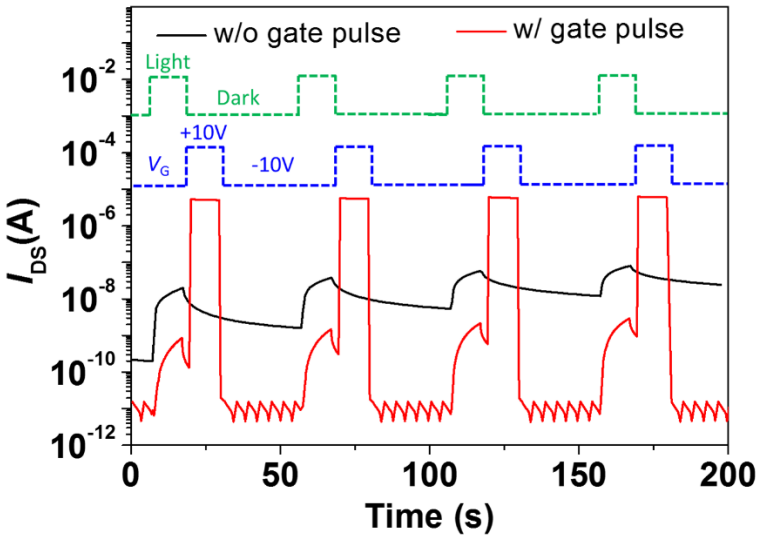

Fig. 3.10. Generation, recovery, and elimination of persistent photoconductivity at 20V V_{DS} under exposure to pulse illumination (470 nm).

Chapter 4

Overcoming the TFT Nonidealities in Analogue Circuits

This chapter investigates two of the most urgent challenges via TFT nonidealities in analogue circuit design, namely the lack of proper active load and the large parasitic capacitance (narrow bandwidth). In-depth analysis of the challenges and applicable solutions are given.

4.1. Lack of Proper Active Load

Active loads are extremely important blocks for analogue circuits, especially for amplifiers [104]. Conventional active load configurations might not function properly or are not feasible in all-TFT integrated circuits. Here, the feasibility of conventional active load structures in all-TFT integrated circuits are carefully investigated. Structures designed for ISO TFTs have also been developed and tested.

4.1.1. Limitations of Conventional Structures

Taking the single-stage common-source amplifier as an example, the common-source transistor converts variations in its gate-source voltage into a small-signal drain current. The drain current passes through the load, usually an active load, to generate an output voltage. Assuming the output resistance of the common-source transistor is r_o, the equivalent resistance value of the active load is R_L, and the magnitude of gain (the common-source stage amplifier) is $g_m(r_o//R_L)$. Therefore, if $r_o \gg R_L$, then increasing the value of R_L can directly improve the gain. The best circumstance for an

amplifier is using an ideal current source as an active load. If R_L is infinite, the magnitude of gain will reach the maximum value, $g_m r_o$.

Two structures can mimic the behaviour of an ideal current source: a current mirror and a class AB configuration. The schematics of those two structures are shown in Fig. 4.1. As an active load, a current mirror provides the driving transistor with a voltage-controlled current source and a fixed gate-source voltage. Owing to the channel-length modulation, this voltage-controlled current source is not entirely ideal, as its output current is influenced by the voltage across it. To model this behaviour, an equivalent resistance (the output resistance), r_0, is placed between the source and drain of M_1 and M_2. The gain of the amplifier in Fig. 4.1 (a) is $-g_m(r_{o1}//r_{o2})$. If the P-type transistor is an identical match to the N-type transistor, the gain will be $-g_m r_o/2$. The active load of the class AB amplifier is a P-type transistor with its gate connected to the input signal. Both transistors are controlled by the input signal. The P-type transistor mimics the small signal behaviour of the N-type transistor; thus two identical voltage-controlled current sources are paralleled, and the gain is boosted to $-g_m r_o$. However, complementary transistors are prerequisite to build a current mirror amplifier or a class AB amplifier, which is not feasible for ISO TFTs.

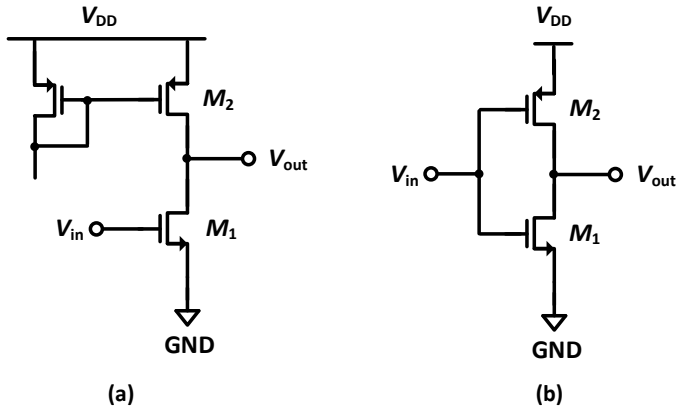

Fig. 4.1. Active load for an amplifier. (a) Amplifier with current mirror as active load. (b) Class AB amplifier.

4.1.2. Monotype Active Load Structures

Diode load and zero-V_{GS} configurations can be used as an active load in monotype ISO-TFT circuit design. The diode load uses a transistor with its gate connected to its drain. It has a small-signal resistance of $1/g_{m2}$ in parallel with the output resistance of r_{o2}. Since r_{o2} is usually several orders or magnitude larger than $1/g_{m2}$, the equivalent

resistance can be simplified to $1/g_{m2}$. The small-signal model of the diode connected active load will be a resistance of $1/g_m$ in parallel with a capacitor. Compared with previous techniques, the gain is very low, and is calculated as the square root of the aspect ratio of the load transistor divided by the aspect ratio of the driving transistor. Zero-V_{GS} configurations connect the gate and the source of the transistor, providing larger resistance for the driving transistor. Under such circumstances, the equivalent resistance of the zero-V_{GS} load can be several orders higher than the diode load.

Another widely used monotype TFT amplifier structure is the Pseudo-CMOS amplifier. Schematics of two typical Pseudo amplifier is shown in Fig. 4.2 [105], [106]. Taking the Pseudo-E configuration as an example, M_1 and M_2 invert the polarity of the input signal and send it to the gate of M_3. Thus, M_3, together with M_1 and M_2, can imitate the behaviour of a P-type transistor. M_4 remains the common-source transistor, and the drain current through M_3 is now inversely proportional to the input signal.

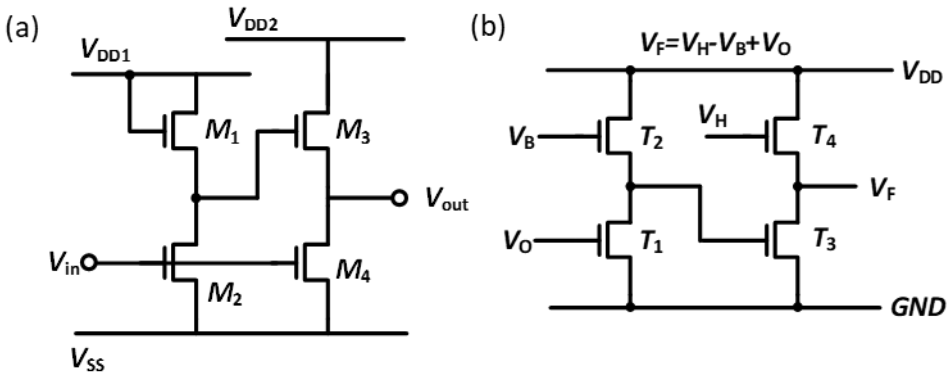

Fig. 4.2 Two different types of the Pseudo-CMOS amplifier: (a) Pseudo-E and (b) Pseudo-CMOS

Fig. 4.3 shows the small signal equivalent circuit of the pseudo-CMOS. The transfer function of the pseudo-CMOS amplifier is given by:

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m3}g_{m2}(r_{o2}//R_2) + g_{m4}}{g_{m3+}\dfrac{1}{r_{o3}//r_{o4}}} \tag{4.1}$$

From equation 4.1, the transconductance of M_3 is amplified by a factor of $g_{m2}(r_{o2}//R_2)$, and is added to the transconductance of M_4. Adding the transconductance of a common-source transistor and a load transistor is very similar to the typical

behaviour of a complementary amplifier. Theoretically speaking, the gain of a pseudo-CMOS amplifier is increased compared with the diode-connected load amplifier.

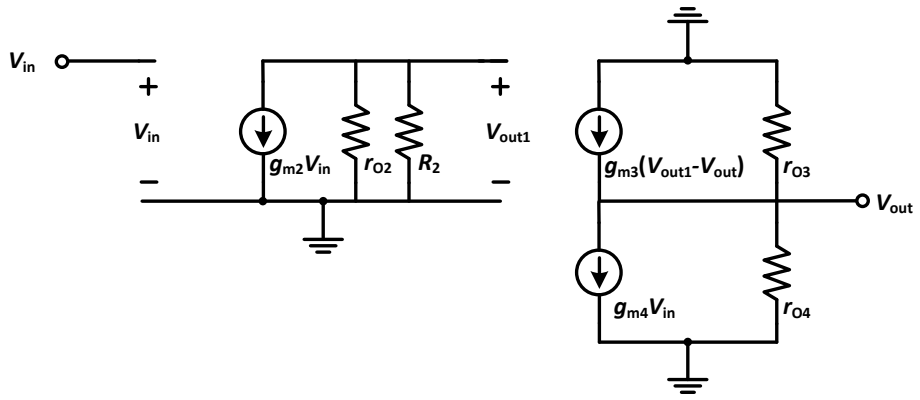

Fig. 4.3 Small signal equivalent circuit of the pseudo-CMOS.

4.1.3. Gain Boosting Techniques

The lack of proper active load can be compensated for by deploying extra gain boosting techniques. Commonly used gain boosting techniques include the cascode configuration, current starving, current cancellation, and bootstrapping. The cascode topology is widely used in CMOS circuit design. It consists of a common-source stage and a common-gate stage. The common-source stage generates a small-signal drain current proportional to the input voltage signal, and the common-gate stage routes the drain current to the load. The DC current in the common-gate stage and the common-source stage are the same. This configuration can provide a high output impedance of $g_{m2}r_{o1}r_{o2}$. Here, g_{m1}, r_{o1}, g_{m2}, and r_{o2} are the transconductance and output resistance of the common-gate stage and the common-source stage. If the load in the cascode amplifier is an ideal current source, then it can reach a gain of $-(g_m r_o)^2$.

Current starving and current cancellation can also be used to increase the gain. Current starving uses an extra DC current source in parallel with the load, which is shown in Fig. 4.4 (a). Since most DC current is supplied by an external current source, the output resistance and voltage gain are higher. If the value of the DC current source is KI_D, the gain of the amplifier can be increased to $A_0/(1-K)$. Here, A_0 is the DC gain of the amplifier without current starving. Typically, K is 0.8, such that the gain is increased by a factor of five. Current cancellation is an approach that can build a load with quasi-infinite resistance. A typical current cancellation load is shown in Fig. 4.4 (b). Cross coupling M_2 and M_3 creates positive feedback, such that the differential resistance of M_2 and M_3 is negative, at $-2/g_{m2}$. When M_1 is parallel-connected with M_2,

and M_3 with M_4, a load with an equivalent resistance value of $2/(g_{m2} - g_{m1})$ can be created. If all the devices have the same dimensions, this technique can create an infinite resistance, which is the ideal load for a differential amplifier.

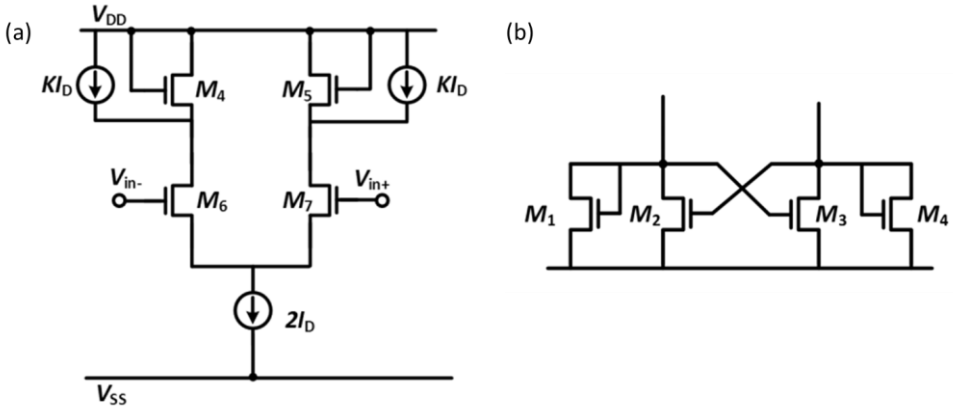

Fig. 4.4. Structures of (a) the current starving and (b) current cancellation techniques.

Using bootstrapping techniques to increase the impedance of diode-connected load not only increases the gain, but it also maintains the bandwidth. Fig. 4.5 shows the bootstrapping diode-connected active load, which consists of two transistors and a coupling capacitor. M1 is a diode connected load, which has an equivalent resistance value of r_o// $(1/g_m)$. Since $1/g_m$ is usually much smaller than r_o, $1/g_m$ is bootstrapped out for this purpose. In this configuration, the capacitor C_1 couples the gate and source of M_1, while the diode-connected M_2 connects the gate and drain of M_1. For a DC voltage signal, C_1 consumes nearly all the voltage drop between V_+ and V_- and diode-connected M_2 consumes negligible voltage. For an AC signal, the gate and source of M_1 are short circuited via C_1 when frequency is high enough to take effect. From the small-signal equivalent circuits, the equivalent impedance of the bootstrapping diode-connected active load can be given by:

$$\frac{V_+ - V_-}{I_{total}}(s) = \frac{r_o R_{eq} C_1 s + r_0}{R_{eq} C_1 s + r_o g_m + 1} \tag{4.2}$$

where I_{total} is the total current through this circuit and R_{eq} is the equivalent resistance of the diode-connection M_2. From this equation, the equivalent resistance of the bootstrapping active load is $r_o/(g_m r_o + 1)$ at low frequency and r_o when the frequency is higher than that of the zero. The frequency of the zero is given by:

$$f_z = \frac{1}{2\pi R_{eq} C_1} \tag{4.3}$$

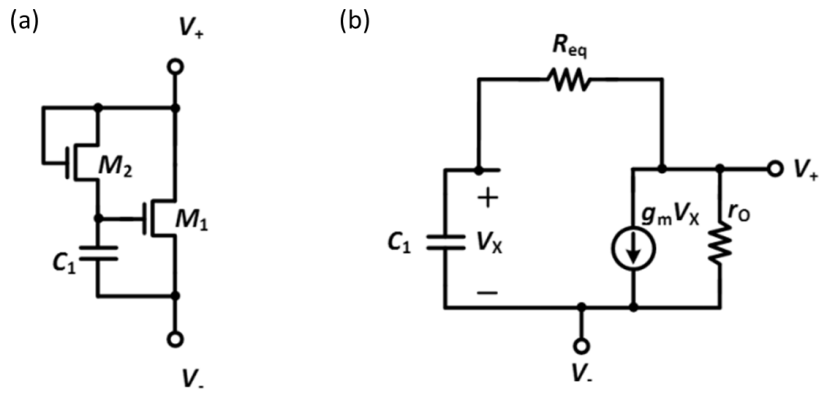

Fig. 4.5. Bootstrapping diode-connected active load: (a) schematic, and (b) small-signal equivalent circuit.

4.1.4. Active Loads for the ISO TFT

Based on the previous discussion, several configurations applicable to the ISO TFT were implemented and tested, including the diode-connected load, the depletion load, the bootstrapping load, and the pseudo-CMOS.

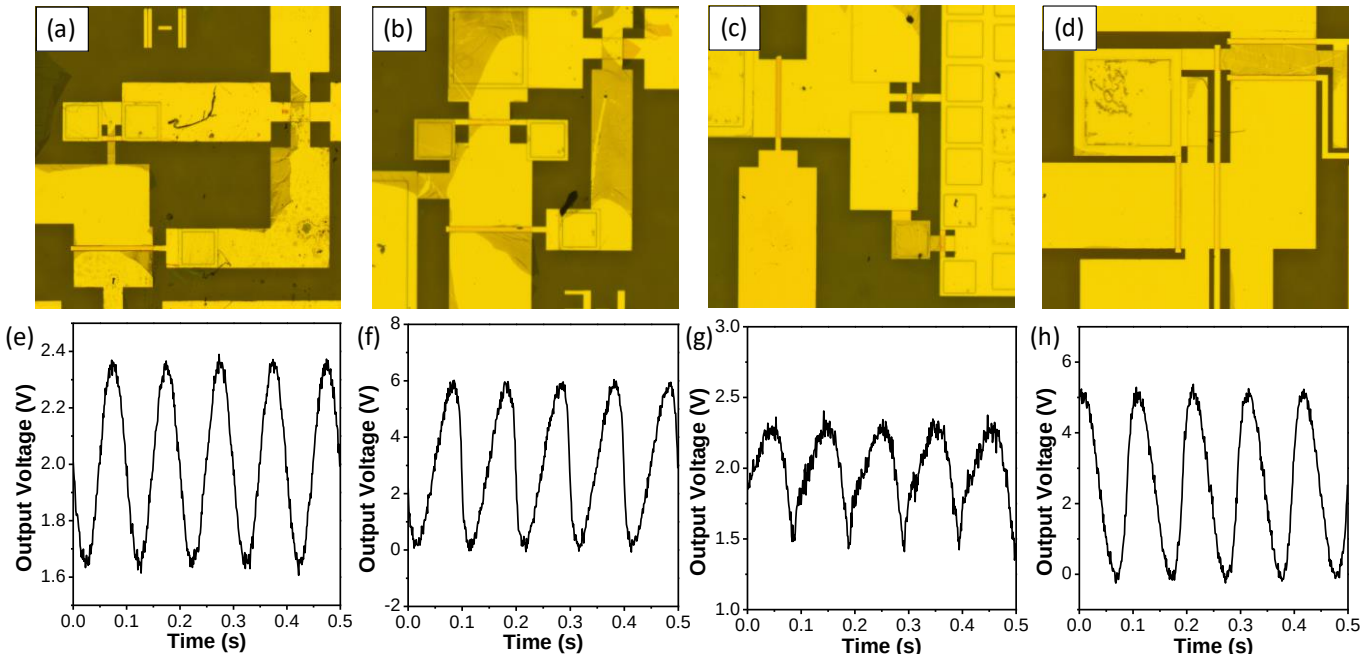

Fig. 4.6. Pictures of (a) diode-connected load amplifier, (b) depletion load amplifier, (c) bootstrapping load amplifier, and (d) pseudo-CMOS amplifier. (e), (f), (g), and (h) are the corresponding output signals of the amplifiers with sine wave input signals.

Fig. 4.6 shows four amplifiers with associated output signals when the input was a sine wave. The diode-load and pseudo-CMOS amplifier had relatively small distortions, and the depletion load amplifier had a sharper falling edge, while the bootstrapping load amplifier suffered from severe distortion. Further simulations and analyses showed that

the drain-gate capacitor and the source-gate capacitor of the extra bootstrapping transistor created a small signal path for positive feedback, which damaged the stability of the amplifier. Reducing the width of the bootstrapping transistor could effectively suppress this positive feedback at the cost of a potentially lower operating speed.

Fig 4.7 compares the AC performance of different active loads. From the simulation results, the diode-connect load amplifier only had a gain of 10.11 dB. In contrast, the current source load, or the ideal load, reached 39.27 dB ($g_m r_o$). The gain of the pseudo-CMOS amplifier was 2.83 dB higher than the diode-load gain, while the bootstrapping amplifier was 17.08 dB higher than the pseudo-CMOS gain. Theoretically, the gain of the depletion load (zero-VGS) amplifier should fall between 10.11 dB and 39.27 dB, which is entirely dependent on the equivalent impedance determined by the drain current at zero gate-source voltage. The measurement result revealed that the actual DC gain of the amplifier was 33.80 dB. Both diode load and pseudo CMOS measurement results matched the simulation curves. The AC performance measurement data of the bootstrapping load amplifier were not given, due to instability.

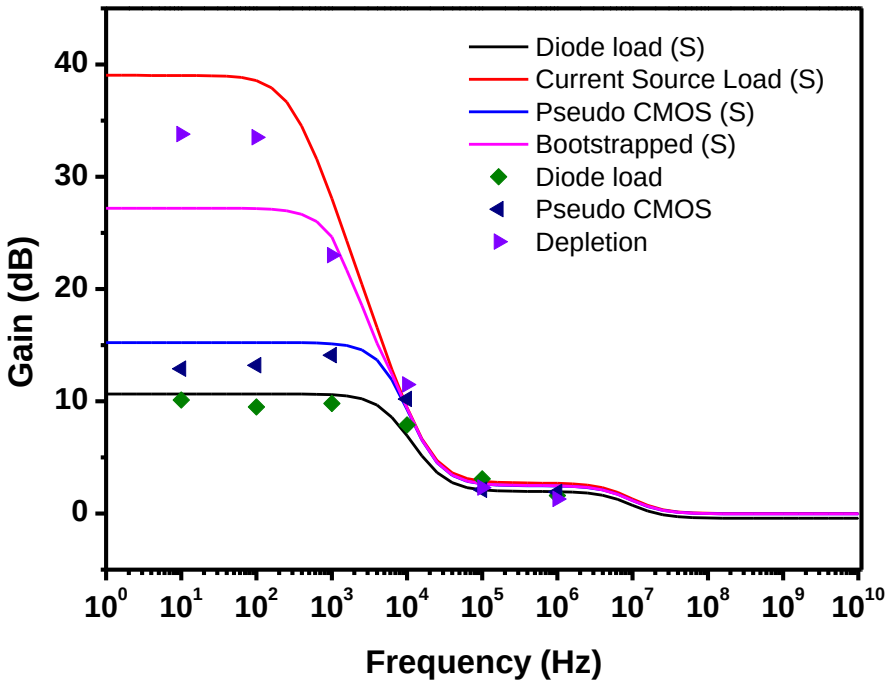

Fig. 4.7. Performance comparison of the active loads, lines represent simulation results and the scattered points are measured data.

Performance data are summarized in Table 4.1. Among the stable configurations, the depletion load amplifier had the highest gain, while maintaining an acceptable THD.

The bootstrapping load did not function properly, due to instability. However, the bootstrapping load appeared more promising than the depletion load, and its instability issue could be solved by using smaller aspect ratios. For the time being, depletion load was used as the active load for the ISO TFT analogue circuits.

Table 4.1. Performance of common-source amplifiers with different active loads.

Parameters		Types of active load			
		Diode-connected	**Depletion**	**Pseudo-CMOS**	**Bootstrapping**
Simulation	DC gain	10.11	[10.65, 39.03]	12.94	27.19
	Cut-off frequency	1.0E+4	[5.0E+3, 1.0E+4]	5.0E+3	1.0E+3
	Distortion (THD)	2.91%	3.39%	1.12%	8.44%
	Stable	Yes	Yes	Yes	Yes
Measurement	DC gain	10.65	33.80	15.23	-
	Cut-off frequency	1.0E+4	3.0E+2	4.0E+3	-
	Distortion (THD)	2.92%	4.18%	5.78%	-
	Stable	Yes	Yes	Yes	No

4.2. Large Parasitic Capacitances

Parasitic capacitances in the TFTs originated from the layout margin of mask misalignment. Based on the data collected from the TFT array, the minimum critical dimension that the current equipment could achieve was 2 μm. As shown in Fig. 4.8 there were two layers sandwiched between the gate and the source/drain: a dielectric layer and a semiconductor layer. On the top of all the layers, there was an optional etch stopper layer. Considering the overlap between the two layers was fixed at 2 μm, the total overlap between the source/drain and the semiconductor was:

$$L_{overlap} = L_1 + L_2 + L_3 \tag{4.4}$$

where L_1 is the length that the semiconductor exceeded the gate region, L_2 is the length difference between the gate and the ESL region, and L_3 is the overlap between the source/drain and the ESL. L_2+L_3, which was 4 μm in this case, contributed to the parasitic capacitance in the ISO TFT.

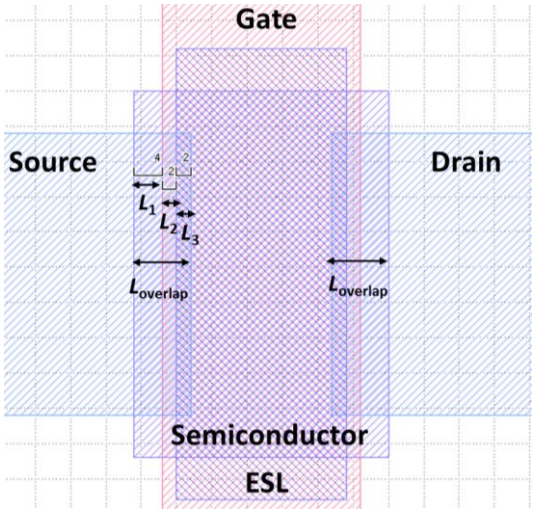

Fig. 4.8. Top view of the ISO TFT layout, showing the overlap between layers.

To evaluate the impact of the parasitic capacitance, a common-source amplifier was used in the analysis as an application scenario. Its small-signal equivalent circuit is shown in Fig. 4.9 and by applying KCL, the transfer function is given by:

$$\frac{V_{out}}{V_{in}} = \frac{(C_{GD}s - g_m)R_D}{R_D R_S \zeta s^2 + [R_S C_{GD}(1+R_D g_m) + R_S C_{GS} + R_D(C_{GD}+C_L)]s + 1} \tag{4.5}$$

where $\zeta = C_{GS}C_{GD} + C_{GS}C_L + C_{GD}C_L$. From equation 4.5, there were two poles and one zero, as follows:

$$f_{dp} = \frac{1}{(1+R_D g_m)R_S C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_L)} \tag{4.6}$$

$$f_{np} = \frac{(1+R_D g_m)R_S C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_L)}{R_D R_S(C_{GS}C_{GD} + C_{GS}C_L + C_{GD}C_L)} \tag{4.7}$$

$$f_z = \frac{g_m}{C_{GD}} \tag{4.8}$$

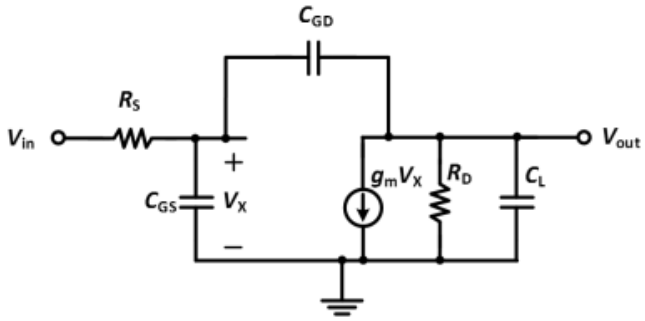

Fig. 4.9 Small-signal equivalent circuit of common-source TFT amplifier.

Typically, the gate-drain capacitor is much smaller than the gate-source capacitor when the transistor operates in the saturation region. Owing to the fact that overlap capacitance becomes dominant, the gate-drain capacitor was comparable with the gate-source capacitor. When the gate-drain capacitor is small, there are two poles. As the capacitor increases, the dominant pole moves to a lower frequency, while the non-dominant pole moves to a higher frequency. Considering the large gate-drain capacitance of the all-TFT integrated common source amplifier, the poles in the transfer function were split, and thus, bandwidth was reduced. The split of poles caused difficulties in multi-stage amplifier design, because poles of each stage overlapped in the low frequency region, as in TFT circuits. Methods such as Miller compensation could no longer be applied to the amplifier, since very little bandwidth trade off remained. As a result, new methods to increase the bandwidth were required in the all-TFT circuit design.

4.1.5. TFT Layout

At the device level, the new TFT layout was designed and verified. As shown in Fig. 4.10, an island structure was used to reduce the influence of the gate-drain capacitor, which was much larger than the gate-source capacitor. Using the drain current level as the specification, the effective channel width of the island-structure TFT was:

$$\frac{W_{effective}}{L} \approx \frac{2}{5}\frac{(W_1+W_2+W_3)+(W_4+W_5+W_6)}{L} \tag{4.9}$$

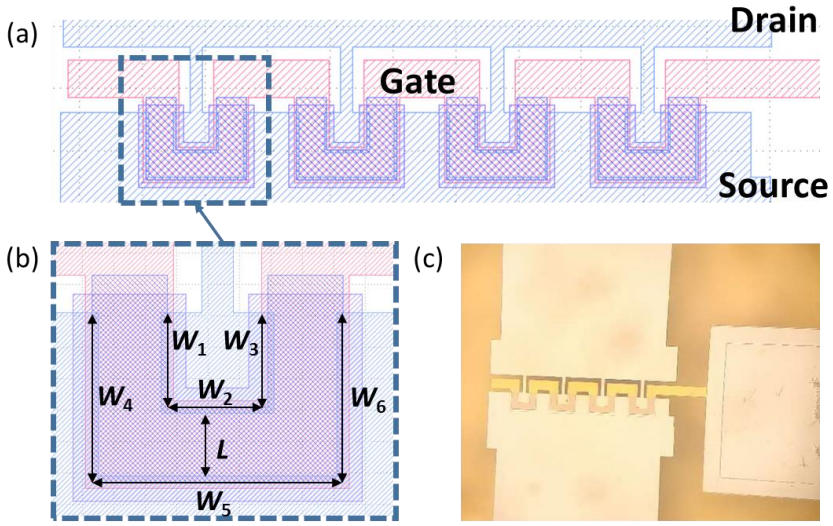

Fig. 4.10. (a) Top view of the island-structure TFT. (b) Top view of the single cell in the TFT. (c) Picture of the island-structure TFT.

In the new layout, the gate-drain capacitor and gate-source capacitor were given by:

$$C_{gd} \approx C_{ox}(W_1 + W_2 + W_3)(4\mu m) \tag{4.10}$$

$$C_{gs} \approx C_{ox}(W_4 + W_5 + W_6)(4\mu m) \approx \frac{7}{3}C_{gd} \tag{4.11}$$

The gate-drain capacitor was half the size of the gate-source capacitor, which was the same size as the parasitic capacitors in a normal layout. Theoretically, if C_{gd} was reduced to 3/7 of its original value, the corresponding pole in the amplifier would move to a frequency that was 7/3 the original frequency.

Using this new layout that impacts the dominant pole greatly increased the bandwidth of the circuits. Fig. 4.11 (a) compares the AC performance of the normal layout with the island-structure layout. The gain bandwidth product of the new layout was two times higher than that of the normal layout. This proves that reducing the miller capacitor, in this case the C_{gd} of the common-source TFT and the C_{gs} of the diode-connected load, effectively increased the bandwidth.

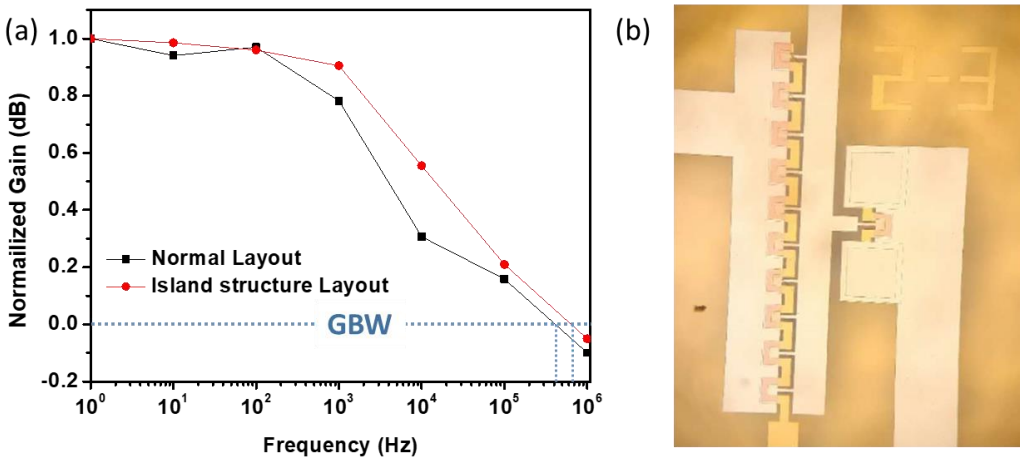

Fig. 4.11. (a) Bode plot comparison of the normal layout and the island structure diode-connected amplifier layout. (b) Top view of the island-structure diode-connected amplifier layout.

4.1.6. Capacitive and Inductive Peaking

Inductive peaking places inductors in strategic locations in order to generate a resonance with parasitic capacitance [107]. Consequently, the bandwidth will expand. Compared with conventional high-speed circuits for broadband communications, inductive peaking can increase the bandwidth without decreasing the gain or adding too many components. For inductive peaking, the size and location of the peaking inductor

should be carefully selected through theoretical analysis and simulation. For a single stage amplifier, there are three major types of inductive peaking techniques: drain peaking, gate peaking, and feedback peaking.

An analysis based on gate inductor peaking is given below as an example. As shown in Fig 4.12, an inductor is involved in the input path of the trans-impedance amplifier. The transimpedance of the amplifier follows:

$$A_R = \frac{(1-g_m R_f + R_1 R_f C_f s) R_1}{1+g_m R_l + A_s + (B+CL_g)s^2 + DL_g s^3 + EL_g s^4} \tag{4.12}$$

where L_g is the gate peaking inductor, and A-E are constants defined below:

$$\mathrm{A} = R_l(C_{in} + C_L + C_1 + C_{ds}) + R_f(C_f + C_{in}) + g_m R_l R_f C_f \tag{4.13}$$

$$\mathrm{B} = R_l R_f[(C_f + C_L + C_1 + C_{ds})C_{in} + C_f(C_L + C_1 + C_{ds})] \tag{4.14}$$

$$\mathrm{C} = C_{in}(1 + g_m R_l) \tag{4.15}$$

$$\mathrm{D} = R_l C_{in}(C_{in} + C_{out}) + R_f R_{in}(C_f + C_{in}) + g_m R_l R_f C_f C_{in} \tag{4.16}$$

According to the equation above, the 3 dB bandwidth of the amplifier can increase up to a certain point, in contrast with the condition that $L_g = 0$. However, increasing the inductance past the optimum point will result in a bandwidth decrease. The peaking technique must be controlled to avoid amplifier instability, otherwise overshoot may occur.

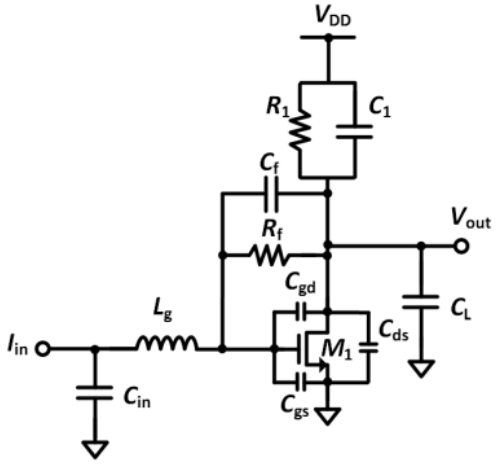

Fig. 4.12. TIA with gate peaking inductor.

Another peaking technique for bandwidth enhancement is termed capacitive peaking. It was developed to compensate for the impact of stray inductor capacitance.

Since the parasitic capacitor is not a fixed value, due to fabrication variation, the peaking inductor cannot perfectly match the capacitor. In some cases, a peaking inductor can cause bandwidth degradation rather than improvement. Capacitive peaking can be utilised to design a broadband Butterworth-type trans-impedance amplifier by adding an extra pole to the transfer function. In addition, the area consumption of a capacitor is much smaller than that of an inductor.

Fig. 4.13 shows a circuit schematic of a capacitive peaking TIA. The simplified transfer function is:

$$A_R = \frac{A\omega_1\omega_2}{s^2+s(\omega_1+\omega_2)+\omega_1\omega_2} \tag{4.12}$$

Here, ω_1 and ω_2 are the poles. The poles of this transfer function are the complex conjugate if the quality factor (Q) is larger than 0.5, and the bandwidth can then be broadened, due to the cancellation of the imaginary parts. When Q reaches $\sqrt{1/2}$, the circuit is a Butterworth design and obtains maximum bandwidth. Normalised denominator polynomials in factored form for Butterworth type filter (Q=$\sqrt{1/2}$) reveals the relationships between these poles:

$$\omega_2 = \frac{\omega_1}{\sqrt{2}\omega_1-1} \tag{4.12}$$

Therefore, if a proper peaking capacitor can be selected to satisfy the condition in equation 4.12, bandwidth of the closed-loop amplifier can be pushed to the maximum.

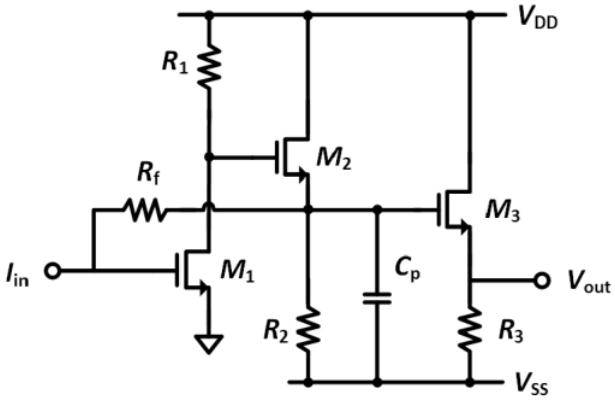

Fig. 4.13. Circuit schematic of capacitive peaking TIA.

Chapter 5

All-TFT Amplifier

In this chapter, the process of designing, simulating, and fabricating an all-TFT amplifier is presented. A 4-bit capacitor array was successfully integrated into the amplifier, as the first mixed-signal all-TFT circuit in the world. Section 5.1 sets the performance targets of the amplifier, and section 5.2 states the design strategy. Section 5.3 discusses the simulation results. Section 5.4 introduces the layout design and fabrication processes, and finally, Section 5.5 provides the measurement results.

5.1. Design Goals

In previous chapters, thorough investigations were conducted on the ISO TFT. The knowledge obtained on this elementary building block provided the insight required of more complicated circuits. Compared with conventional CMOS transistors, the ISO TFT has significant advantages: it is a low-temperature process, has large-area coverage, and is transparent. However, it still suffers from low mobility, instability, and a lack of proper active load. Thus, the most promising circuit application lies in the front-end system for signal sensing. Among all front-end circuits, the operational amplifier, or voltage amplifier, is the most common and versatile circuit block. The standard operational amplifier amplifies the differential input signal and turns it into a single output signal. Normally, feedback loops that serve different functions are applied. To ensure the stability of the feedback loop, enough phase margin must be designed into an amplifier [108]. According to Barkhausen's criteria, the phase margin should not exceed -180° when the feedback loop gain reaches one, otherwise the feedback will become positive and cause oscillation in the circuit.

One of the most common applications of signal-sensing circuits is in picking up biomedical signals. Biomedical signals collected directly from electrodes are relatively weak; i.e. smaller than 10 mV or 1 µA and less than 1 kHz. Ideally, the front-end circuit should be able to amplify the input signal into a voltage signal that can be processed by the following ADC or digital circuits. In this case, the amplifier should drive a reasonable output load. To simulate the scenario, the amplifier was connected to a high input impedance circuit via a metal track, and the output load was set to 5 pF with a 1 MΩ resistor in parallel.

As discussed in Chapter 4, the nonidealities of ISO TFTs created limitations on the all-TFT amplifier design. One of the major problems was the large parasitic capacitor in TFTs, which was influenced by the minimum feature size of the photolithography machine. The photolithography machine used was a SUSS MircoTec MJB4 mask aligner with a printing resolution of 0.5 µm. To maintain adequate fabrication yield, 1 µm was set as the minimum feature and 2 µm was the overlap between the gate and the source/drain electrode. However, the 2 µm overlap created a relatively large parasitic capacitance, thus the frequency performance worsened. This negative impact could have been reduced by optimising layout or using a self-aligned structure. Considering this was not the most important requirement of front-end circuits, bandwidth was sacrificed in exchange for improving other specifications. The target specifications for this amplifier are listed in the Table 5.1.

Table 5.1. Target specifications for the all-TFT amplifier

Specifications	Target
Open loop gain	> 30 dB
Input impedance	> 100 MΩ
Output impedance	< 100 KΩ
Output load capacitor	= 5 pF
Common-mode input/output voltage	0.5(VDD+VSS)
Output dynamic range	[0.2(VDD-VSS), 0.8(VDD-VSS)]
Static power consumption	< 0.1mW
Total harmonic distortion	< 10%
Phase margin	> 60°
Slew rate	> 0.01V/ms
Bandwidth	Maximise

5.2. Amplifier Design

As mentioned in the previous chapter, there are many remaining challenges in the all-TFT circuit design. Though new methods were proposed to solve these problems, not all were used in this amplifier, due to the tape out probability for a functional and successful circuit. The proposed all-TFT amplifier uses a two-stage differential input structure with innovations in the elementary building blocks. More aggressive and advanced design strategies from successful simulations are presented in the appendix and will be taped out in the future.

Fig. 5.1 shows the schematic of the proposed amplifier. It consists of two amplifier stages and a phase compensation stage. It may look like a conventional CMOS two-stage Miller amplifier, but the working mechanism is completely different. Unlike the CMOS design, which uses a PMOS differential input pair and a bias transistor, the proposed all-TFT amplifier uses n-type TFTs. T_2 and T_3 are the differential input pair and T_1 is biased in the subthreshold region to control the DC current. Since the gate-source voltage of T_1 is fixed at zero, the DC bias current of the first stage will be constant at I_1 when the supply voltage is applied. I_1 is determined by the depletion behaviour of transistor that is shown in Fig. 2.18. T_4 and T_5 form the current mirror, with T_4 connected as a diode-load. The voltage at node 2 will be determined by the current flow through T_4, which ideally is $I_1/2$ if the current mirror is perfectly matched. Voltage at node 3 is floating until it is connected to the second stage. In the second stage, the DC current is controlled by the threshold-biased T_6, thus the gate-source voltage of T_7 is determined. As a result, when the first stage is connected to the second stage, the DC operating point will be established automatically.

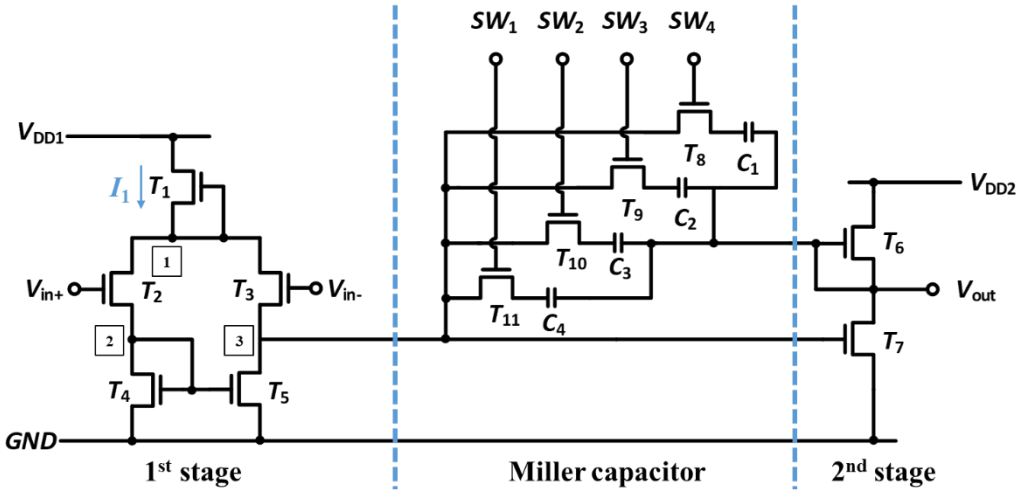

Fig. 5.1. Schematic of the proposed all-TFT amplifier.

Fig. 5.2 show the small-signal equivalent circuits of the amplifier. If both the differential input pair and the current mirror are perfectly matched, the transconductance of T_2 and T_3, as well as T_4 and T_5 will be the same:

$$\begin{cases} g_{in} = g_2 = g_3 \\ g_{mirror} = g_4 = g_5 \end{cases} \tag{5.1}$$

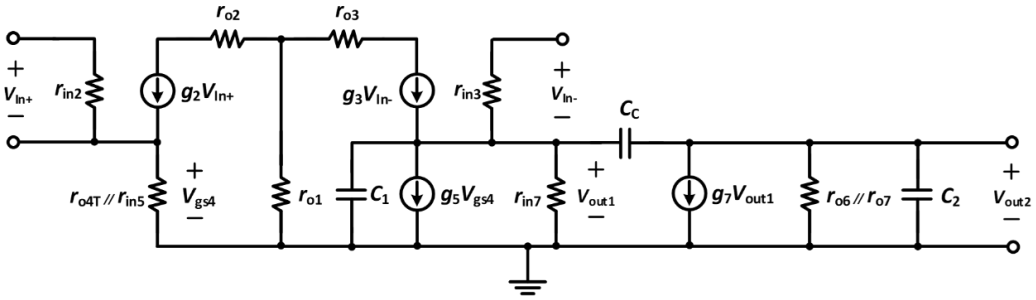

Fig. 5.2. Simplified small-signal equivalent circuits of the all-TFT amplifier

Since T_7 and the differential input pair transistors are biased in the saturation region, using the universal SPICE level-1 model gives:

$$g = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) = \frac{2I_{DS}}{V_{GST}} \tag{5.2}$$

Moreover, T_4 is a diode-connected transistor, such that its output resistance is:

$$r_{o4T} = \frac{1}{g_4} //r_{o4} \tag{5.3}$$

Applying Kirchhoff's Current Law, the following equations were derived:

$$\begin{cases} g_3V_{in-} - g_5V_{gs4} + \frac{V_{in-}}{r_{in3}} - \frac{V_{out1}}{r_{in7}} = 0 \\ \frac{V_{gs4}}{r_{o4T}//r_{in5}} - g_2V_{in+} - \frac{V_{in+}}{r_{in2}} = 0 \end{cases} \tag{5.4}$$

yielding

$$A_1 = \frac{V_{out1}}{V_{in+} - V_{in-}} = \frac{V_{out1}}{V_{in}} = -\left(g_{in} + \frac{1}{r_{oin}}\right) r_{in7} \tag{5.5}$$

The gain of the second stage is:

$$A_2 = -g_7(r_{o6}//r_{o7}) \tag{5.6}$$

Therefore, the open loop gain of the amplifier in Fig. 5.2 is:

$$A = A_1A_2 = r_{in7}g_7(r_{o6}//r_{o7})(g_{in} + \frac{1}{r_{oin}})$$

$$\approx 4r_{in7}(r_{o6}//r_{o7})\frac{I_{DS7}I_{DSin}}{V_{GST7}V_{GSTin}} \tag{5.7}$$

As expected, the gain of the amplifier was a function of the DC bias current, overdrive voltage, and output resistance. With the new current mirror and bias stage, the gain was also proportional to the input resistance of the second stage, which ideally was much higher than the output resistance, thus boosting the gain. In terms of the frequency response, C_1 and C_2 are the total capacitance between the output of the first/second stage and the ground:

$$\begin{cases} C_1 \approx C_{GS5} + C_{GS7} \\ C_2 \approx C_{GS7} + C_{GD6} + C_L \end{cases} \tag{5.8}$$

According to Kirchhoff's Current Law and the previous assumptions, at the output node of the first and second stage:

$$\begin{cases} g_{in}V_{in} + sC_1V_{out1} + \frac{V_{out1}}{r_{in7}} + sC_c(V_{out1} - V_{out2}) = 0 \\ g_7V_{out1} + sC_2V_{out2} + \frac{V_{out2}}{r_{o6}//r_{o7}} - sC_C(V_{out1} - V_{out2}) = 0 \end{cases} \tag{5.9}$$

Thus, the transfer function for the amplifier is:

$$\frac{V_{out2}}{V_{in}} = [g_{in}(g_7 - sC_C)r_{in7}(r_{o6}//r_{o7})]/\{r_{in7}(r_{o6}//r_{o7})(C_CC_1 + C_CC_2 + C_1C_2)s^2 + [r_{in7}C_1 + (r_{o6}//r_{o7})C_2 + C_Cg_7r_{in7}(r_{o6}//r_{o7}) + C_Cr_{in7} + C_C(r_{o6}//r_{o7})]s + 1\} \tag{5.10}$$

From equation 5.9, the zero and poles of the amplifier are:

$$f_z = \frac{g_7}{2\pi C_C} \tag{5.11}$$

$$f_d = \frac{1}{r_{in7}C_1+(r_{o6}//r_{o7})C_2+C_Cg_7r_{in7}(r_{o6}//r_{o7})+C_Cr_{in7}+C_C(r_{o6}//r_{o7})} \tag{5.12}$$

$$f_{nd} = \frac{r_{in7}C_1+(r_{o6}//r_{o7})C_2+C_Cg_7r_{in7}(r_{o6}//r_{o7})+C_Cr_{in7}+C_C(r_{o6}//r_{o7})}{(C_CC_1+C_CC_2+C_1C_2)(r_{o6}//r_{o7})r_{in7}} \tag{5.13}$$

Where f_z, f_d, and f_{nd} are the frequency of the zero, the dominant pole, and the non-dominant pole, respectively.

To keep the amplifier stable, especially when feedback is applied, the phase of output signal should be kept away from -180°. Otherwise, the negative feedback will turn into positive feedback and cause peaking or oscillation. Therefore, the phase of output signal must be verified to ensure it stays away from the critical -180°; i.e. adequate phase margin must be ensured. From the simplified small-signal analysis, the proposed amplifier has two poles and one zero on the right half-plane (RHP). If the

compensation capacitor C_C was increased to split the dominant and non-dominant poles, the zero on the RHP would be reduced, as well as the phase margin.

Using equations 5.11, 5.12, and 5.13, the relationship between C_C and f_z, f_d, and f_{nd} is visualized in Fig. 5.3. When C_C was small (<1 pF) and comparable to the C_{GS}/C_{DS}, its effect on the zero and poles was very limited. When C_C was relatively large (>20 pF), it dominated the f_{nd}. In equation 5.13, a large C_C cancelled itself out and eliminated other smaller factors in both the numerator and denominator. f_{nd} and f_d reduced the gain by +20 dB/dec and shifted the phase by +90°. The zero on the RHP increased the gain by +20 dB/dec and shifted the phase by +90°, which worsened the system's stability. To maintain stability, the poles must be split and kept at a distance that is larger than one decade. The most efficient compensation scheme was adding a 10 pF capacitor, as marked by the blue line in Fig. 5.3. It made the non-dominate pole coincide with the zero, thus maximising the bandwidth. Considering the variation in the TFT process, a capacitor array was used for compensation, which varied from 0 pF to 50 pF.

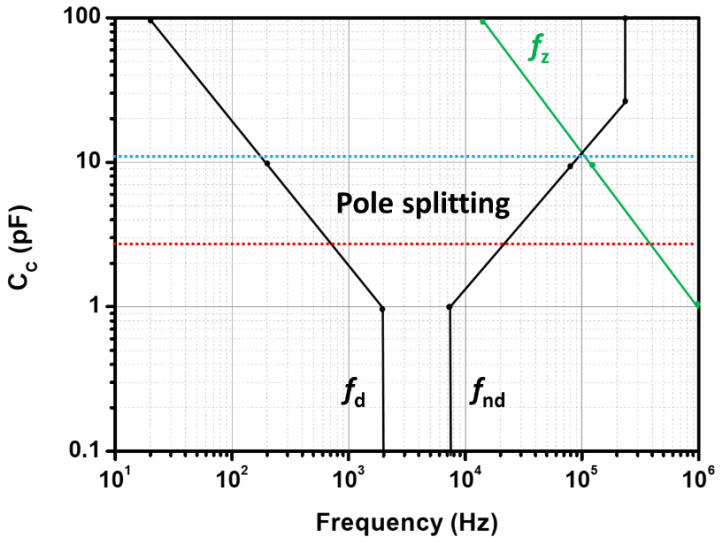

Fig. 5.3. Relationship between compensation capacitor and zero/poles of the proposed amplifier.

5.3. Simulation

The simulations were conducted using Cadence 6.1.5 with a Verilog-AMS written TFT model in a Linux environment. Fig. 5.4 shows the TFT model used in the simulation, with the solid line being generated by the Verilog-A model and the crosses representing the measured data. The extracted parameters are presented in this figure

as well. Due to the restriction of the model, noise performance will not be analysed in the simulation.

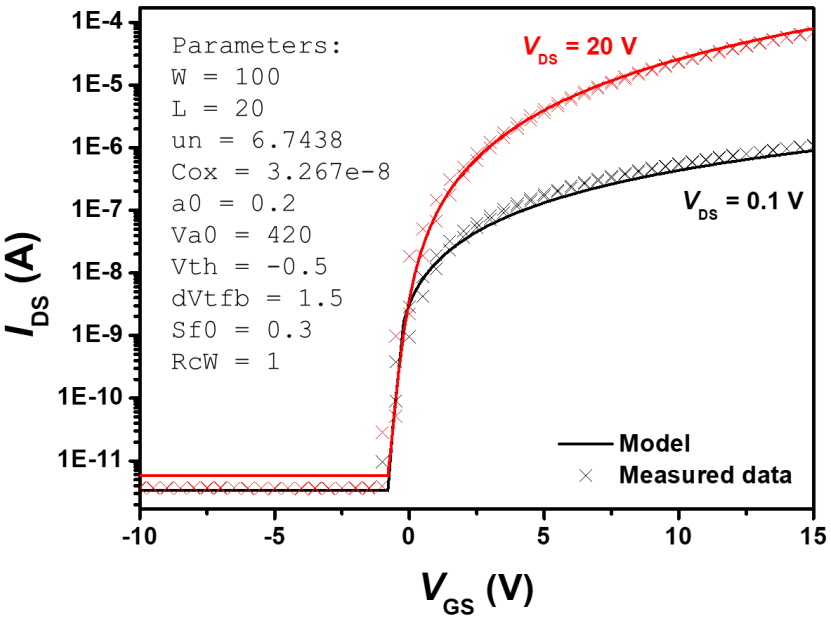

Fig. 5.4. The ISO TFT model used in the simulation.

A schematic of the proposed all-TFT amplifier used in the simulation is shown in Fig. 5.5. In this simulation, the capacitor array was simplified into a single capacitor. Based on the previous analysis, the dimensions of each transistor were determined, which are shown in Table 5.2.

Table 5.2. Dimensions of the TFTs in the proposed amplifier.

TFT	Width/Length (μm/μm)
T_1	40/20
T_2	80/20
T_3	80/20
T_4	40/20
T_5	40/20
T_6	200/20
T_7	200/20

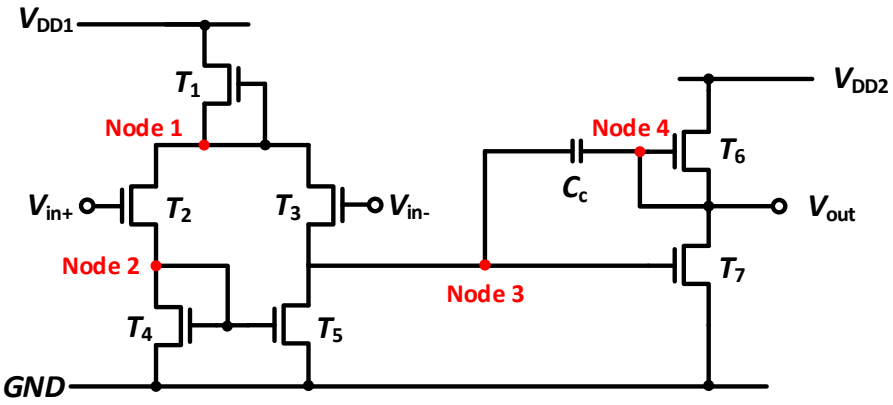

Fig. 5.5. Schematic of the all-TFT amplifier used in the simulation.

5.3.1. DC Operating Point and Static Power Consumption

Among all testbenches, the DC operating point is the most fundamental and important. In this testbench, V_{DD1} was fixed at 5 V, the input common-mode voltage was set to 2.5 V, and the supply voltage of the second stage, V_{DD2}, was varied from 5 V to 20 V to control the output voltage level. Under all conditions, transistors T_1 and T_6 were biased in the subthreshold region, and all the other transistors were biased in the saturation region. Table 5.3 shows the node voltages, static current, and power consumption in the DC simulation.

Table 5.3. Node voltages, static current, and power consumption under different second stage supply voltages.

V_{DD2}	2.5 V	5 V	20 V
Node 1	4.084 V	4.084 V	4.084 V
Node 2	1.383 V	1.383 V	1.383 V
Node 3	1.383 V	1.383 V	1.383 V
Node 4	1.366 V	2.434 V	10.88 V
I_{DS1}	32.09 nA	32.09 nA	32.09 nA
I_{DS2}, I_{DS3}	16.05 nA	16.05 nA	16.05 nA
I_{DS4}, I_{DS5}	16.05 nA	16.05 nA	16.05 nA
I_{DS6}	80.71 nA	81.53 nA	84.31 nA
I_{DS7}	80.71 nA	81.53 nA	84.31 nA
Static power consumption	332.84 nW	538.71 nW	1817.26 nW

To keep all transistors biased in the appropriate region, the supply voltage needed to be at least 2.5V. The output voltage level was controlled by varying the supply voltage of the second stage. The simulation results showed that the DC operating point of the second stage was proportional to V_{DD2}. However, this conclusion might not be

accurate. Since the gate-source voltage of T_7 was pinned, the output voltage of the second stage was determined by how the active load, T_6, and the driving transistor, T_7, reacted to the change in drain-source voltage. T_6 and T_7 were biased in the subthreshold region and the saturation region, respectively. The previous conclusion can only be true if varying the source-drain voltage had an identical impact on the source-drain current in both the subthreshold and saturation regions, which is not realistic. To evaluate the design, apart from simulation, it was divided into several building blocks, which were fabricated for further testing. This process was essential, and was applied throughout the design process of the amplifier.

5.3.2. Gain, Bandwidth, and Phase Margin

The testbench for evaluating the AC performance of the proposed amplifier is shown in Fig. 5.6. V_{DD1} and V_{DD2} were set to 5 V, the input common voltage was 2.5 V, and two 0.1 V AC signals with a 180° degree phase difference were used as the input signals. Compared with the single input signal AC testbench, the differential input testbench provided more accurate results in terms of the zeros and poles.

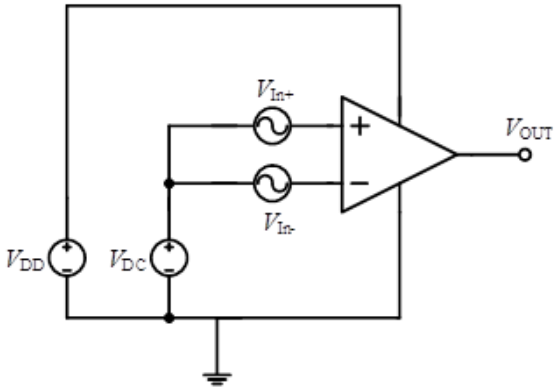

Fig. 5.6. AC testbench.

The AC performance of the proposed amplifier is shown in Fig. 5.7, where a 0.1 pF compensation capacitor was used in the simulation. The DC gain was 40.28 dB, the gain-bandwidth product (GBW) was 65 kHz, the phase margin was 59.2°, and the gain margin was 6.2 dB. Though the amplifier could achieve a larger bandwidth with a smaller compensation capacitor, the phase margin would not meet the requirement in such circumstances.

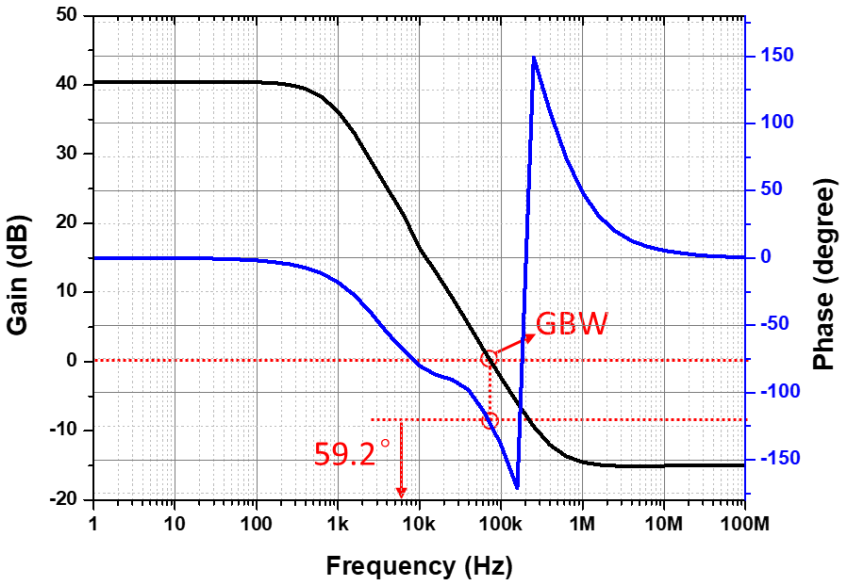

Fig. 5.7. Bode diagram of the proposed amplifier.

The compensation capacitor was increased and the corresponding AC performance was evaluated. From Fig. 5.8, increasing the capacitor effectively split the poles, thus increasing the phase margin. In addition, the impact of the compensation capacitor on the dominant pole was slightly greater than its impact on the non-dominant pole and the RHP zero.

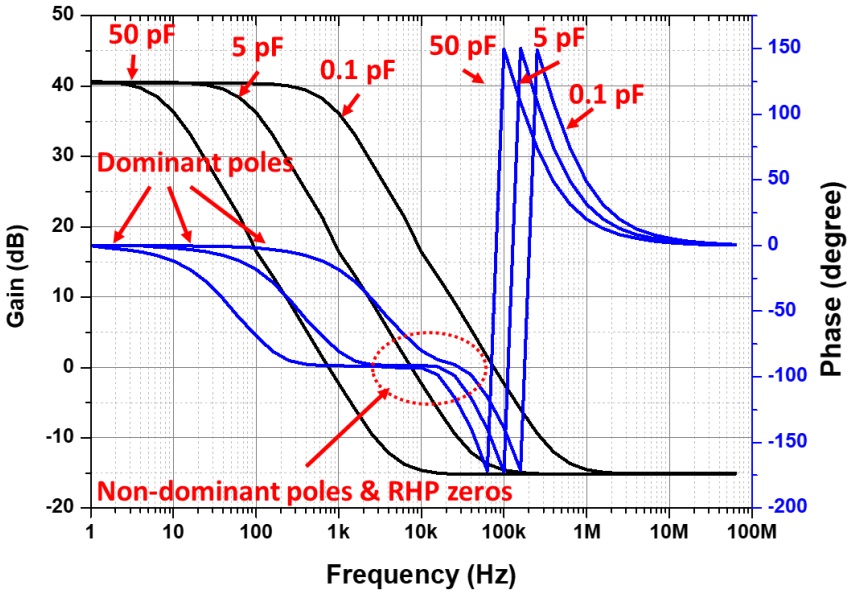

Fig. 5.8. The impact of the compensation capacitor on the Bode diagram.

5.3.3. Output Dynamic Range, Signal Distortion, and Slew Rate

In this section, output dynamic range, signal distortion, and slew rate of the proposed amplifier were tested with a 5 pF compensation capacitor. To determine the

proper output dynamic range, a sine wave on a 2.5 V DC signal was applied to the positive input terminal, while the negative input terminal was fixed at a 2.5 V DC voltage. Fig. 5.9 shows the input and output signals when the peak-to-peak amplitude of the input sine wave was 10 mV. Effective data from this testbench were obtained once the system stabilized, which took one cycle of the input sine wave. From these data, distortions in the output signal were found.

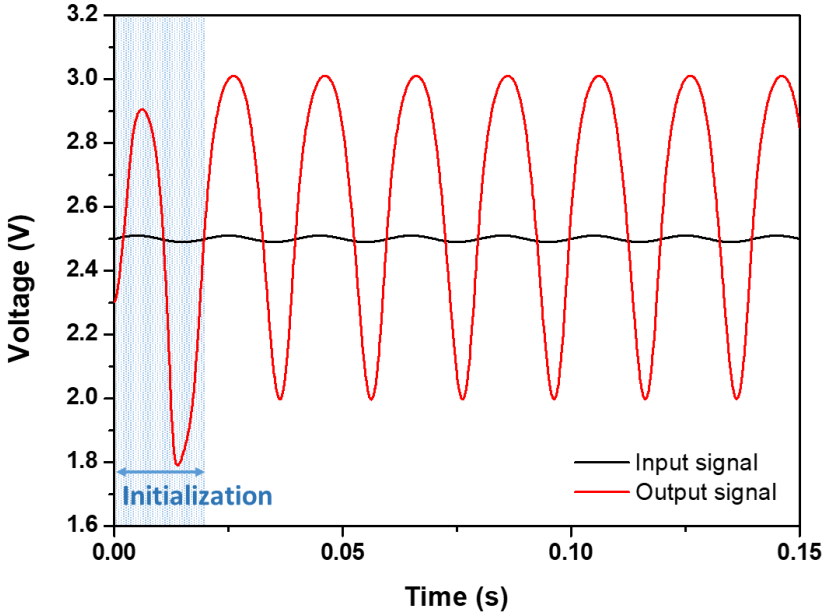

Fig. 5.9. Input and output signals in the simulation (10 mV peak-to-peak amplitude of the input sine wave).

Using a fast Fourier transform (FFT), further analysis of the output signal was conducted to obtain the frequency spectrum, as shown in Fig. 5.10. The highest peak was found at the fundamental frequency, 50 Hz; the amplitude of this peak is marked as H_1. A series of harmonics were found at multiples of this frequency in the original wave. The amplitude of the second and third harmonics were H_2 and H_3, etc. for each of the following harmonics. Total harmonic distortion (THD) was used for assessment:

$$THD = \frac{\sqrt{H_2^2+H_3^2+H_4^2+\cdots}}{\sqrt{H_1^2+H_2^2+H_3^2+H_4^2+\cdots}} \tag{5.14}$$

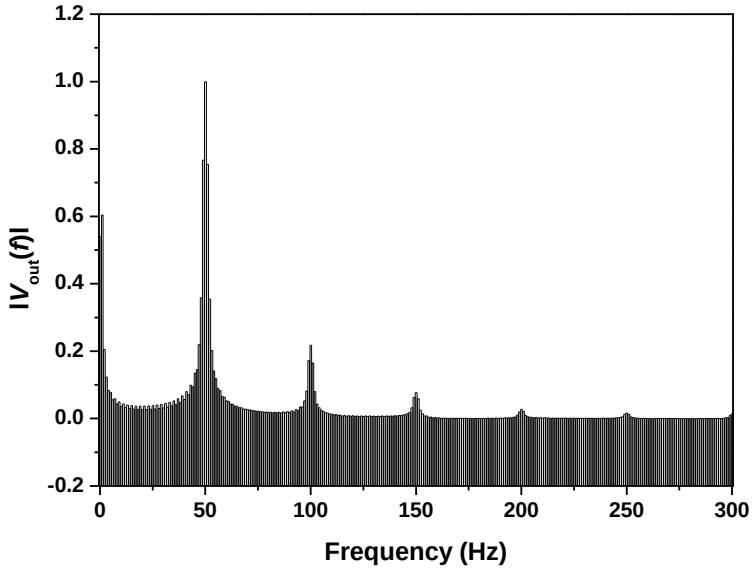

Fig. 5.10. Frequency spectrum of the output signal.

In the previous testbench, the input sine wave had a peak-to-peak amplitude of 10 mV, and the corresponding output range was 1.79V - 2.91V, with a THD of 5.19%. Varying the amplitude of the input sine wave, THD data at different output ranges were collected, as shown in Table 5.4. The THD was less than 10% in most cases, but when the peak-to-peak amplitude of the input signal reached 50 mV, a large distortion (25.46%) was found in the output signal. For the open-loop testbench, the input signal was amplified by 40 dB. To reduce the THD and ensure a proper DC operating point, the input signal (single input scenario) should be less than 27.5 mV and the output signal amplitude should not exceed 3.02 V.

Table 5.4. THD of the output signal at different output ranges.

Input signal amplitude (pk-pk)	Output range	Output signal amplitude (pk-pk)	THD
2.5mV	2.20V~2.48V	0.28V	4. 81%
5.0mV	2.05V~2.60V	0.55V	4. 93%
10.0mV	1.79V~2.91V	1.12V	5.19%
25.0mV	0.98V~3.74V	2.76V	5.35%
27.5mV	0.83V~3.85V	3.02V	7.21%
50.0mV	0.58V~4.11V	3.53V	25.46%

In terms of the slew rate, the testbench was similar to the one used in the output dynamic range. Instead of a sine wave, a square wave with a ±2.5V peak-to-peak amplitude was applied to the positive terminal. The simulation results are shown in Fig.

5.11. The slew rate to charge the output load was 0.05 V/ms, and the slew rate to discharge the output load was 0.1 V/ms.

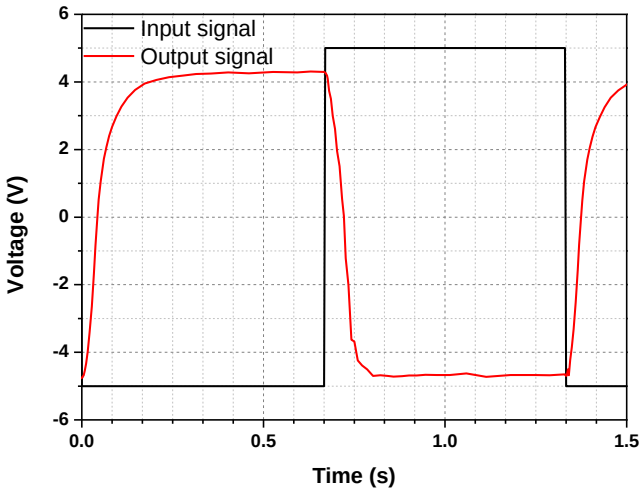

Fig. 5.11. Slew rate of the proposed amplifier.

5.3.4. Monte Carlo Simulation Results

Based on the data collected from the measurements on uniformity in Chapter 3, a Monte Carlo simulation environment was established. Both AC and DC tests were conducted.

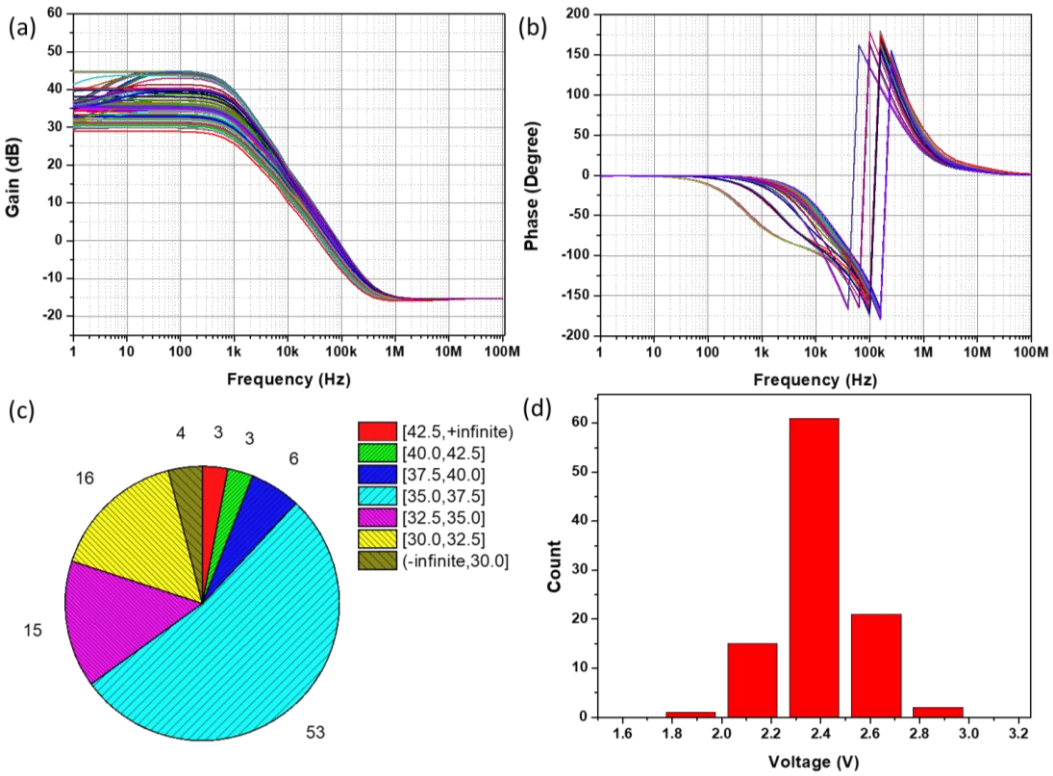

Fig. 5.12. Monte Carlo simulation: (a) gain, (b) phase, (c) DC gain, and (d) output voltage level statistics.

Fig. 5.12 shows a summary of the simulation, including the gain, phase, DC gain, and output voltage level statistics. In this testbench, DC gain was the most important specification. The worst case for DC gain is if it is slightly higher than 30 dB. Most results fell between 37.5 dB and 40 dB. Though this is slightly lower than the simulation result in the previous section, it still met the requirement. More than 80% of the data showed acceptable values. For a TFT tapeout, an 80% success rate indicated that the proposed amplifier was ready to be fabricated and tested.

5.4. Layout and Fabrication

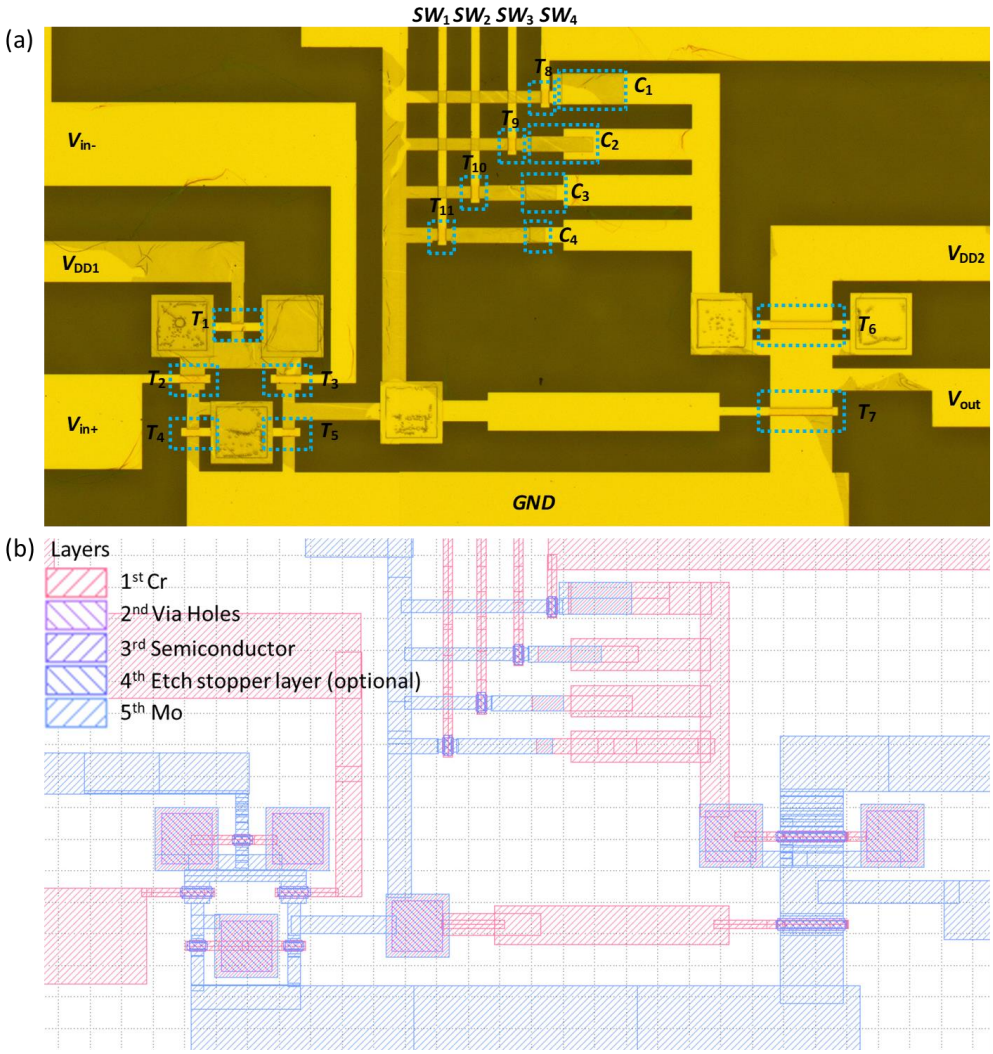

Fig. 5.13. (a) Photo of the glass substrate on which the amplifier was formed, (b) layout design of the amplifier.

Fig. 5.13 (a) shows a photo of the amplifier on a glass substrate. 11 TFTs and four capacitors were fabricated on this die. 10 input/output (I/O) terminals were used and connected to the pins of the die. The total area of the proposed amplifier was 1635 μm

× 2360 μm without the I/O pins, and 9800 μm × 9800 μm with the I/O pins. The corresponding layout design is shown in Fig. 5.13 (b), which shows a part of the second set layout design. Complete mask designs are attached in the Appendix. Regarding the fabrication process, the standard five-mask process was used, as described in Chapter 2. In this process, it is highly likely that the etch stopper could change the annealing conditions and reduce the yield, thus an etch stopper was not used.

5.5. Measurement Results

As mentioned above, the amplifier was divided into several small building blocks for the convenience of trouble-shooting. These building included the current mirror, the differential input pair, the output stage, and the capacitor array. During the measurements, the current mirror and differential input pair could not be measured properly, due to a design flaw in the layout and the measurement kit. As a result, measurements of these two building blocks will not be discussed in the section. This problem will be addressed in the next set of masks. Details about this flaw are stated in the appendix.

5.4.1. Measurement Kit

The measurement kit can be seen as a packaging technique for TFT circuits. The main functions of the kit included connecting the TFT circuits with measurement equipment via pogo pins and buffering the output signals with a source follower array. Fig. 5.14 shows the top view, layout, and cross-sectional view of the measurement kit. To test the TFT circuits, Kapton tape was used to fix the glass substrate onto an identical PCB, but without soldered components. This PCB was used as a backplane, with a metal track to provide useful position data on the pogo pins. The top PCB was aligned with the bottom PCB. Whether pogo pins contacted the circuit I/O pads could be determined through the observing window. Four screws were used at the corners to reduce movement during measurement. The power supply for the active components on the PCB (mainly the operational amplifiers) was provided by an external power source through a coaxial connector on the left side. There were 12 I/O terminals under the small observing window, which were connected to the pogo pins separately.

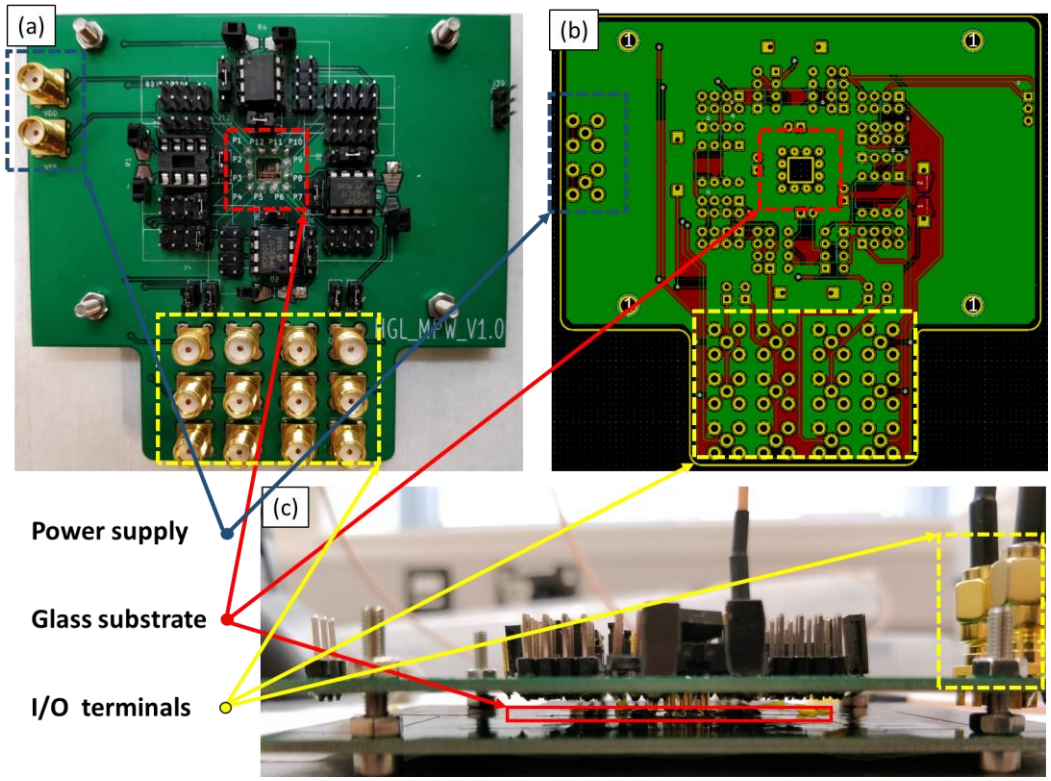

Fig. 5.14. (a) Top view, (b) layout, and (c) cross-sectional view of the measurement kit.

Fig. 5.15 shows a simplified schematic of the measurement kit; the full schematic is given in the appendix. Input signals, including the supply voltage for TFT circuits, were fed directly into the system. Output signals were collected by source followers/voltage buffers, which were realized by connecting the output of the op-amp (MCP601) to its inverting input. This design reduced the load capacitance for the TFT circuits, thus reaching the maximum bandwidth during the measurements. To some degree, flexibility in this design allowed the user to select whether the I/O pad was used for taking in the input signals or buffering the output signals.

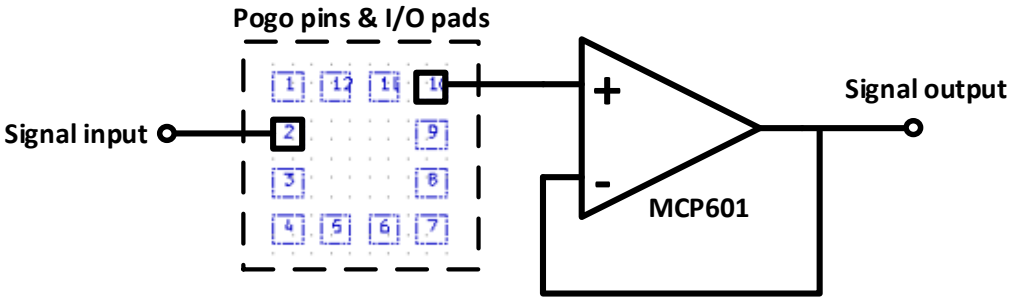

Fig. 5.15. Simplified schematic of the measurement kit.

5.4.2. Capacitor Array

The capacitor array is a non-critical building block in the proposed amplifier. It did not have a direct impact on the yield of the proposed amplifier, and a failed capacitor array (e.g. short circuit) could be disconnected from the amplifier by simply cutting/etching the metal track connection. It was designed to stabilize the amplifier when feedback was used; therefore, the accuracy of the programmed capacitor value was the most important specification. In this section, a discrete capacitor array was tested to verify the design. Fig. 5.16 shows a photo and a schematic of the capacitor array. The circuit was the same as that used in the proposed amplifier, but this capacitor is four times larger. This is to reduce the relative measurement error, especially at low capacitance levels. The capacitor array was measured with a Keithley Model 4200-SCS semiconductor characterisation system. Offset error, or the zero-code error, was ignored in this measurement, because the capacitance value at 0000 input code was deducted (2 pF). This offset was mainly due to the coaxial connection wires, and is a fixed value. Thus, it will not have significant impact on the capacitor array when integrated into the amplifier.

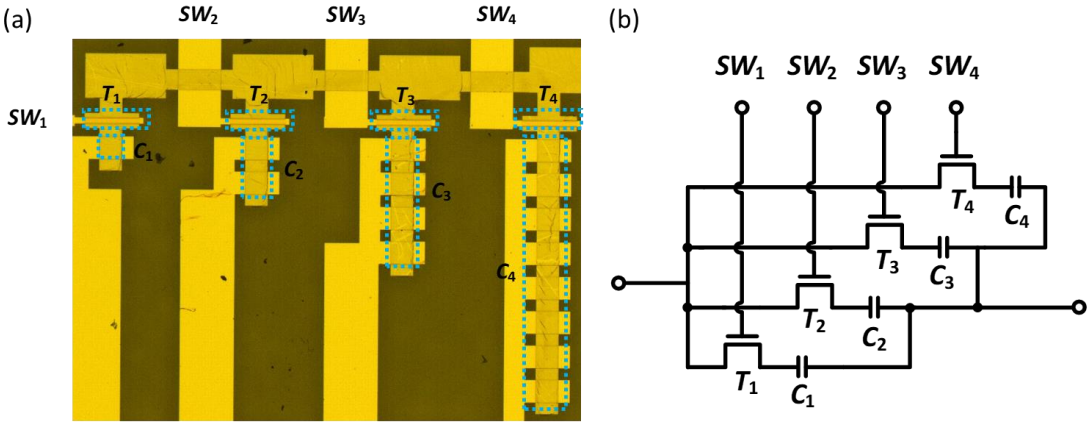

Fig. 5.16. (a) Photo of the capacitor array and its (b) circuit diagram.

Fig. 5.17 (a) shows the capacitance of the capacitor array with different input codes. The difference between the ideal capacitance (solid purple straight line) and the quantised capacitance (at multiple frequencies) is the signal error, which has a saw-tooth shape. The quantisation error is shown in Fig. 5.17 (b). The signal-to-noise ratio follows the standard DAC SNR equation:

$$SNR = \frac{3}{2}2^{2N} = 6N + 1.76dB = 25.76dB \quad (5.15)$$

Here, N is the input bit of the array. Gain error of the array was calculated by comparing the slope of the blue and purple solid lines in Fig. 5.17 (a). The gain error of this array was 1.51 at 1 kHz, 1.42 at 5 kHz, 1.31 at 10 kHz, and 1.21 at 100 kHz.

Shrinking the capacitance by a factor of four gave an array that ranged from 0 pF to 65 pF. The SNR was not influenced by the changes in the sizes of the capacitance, and neither was the gain error. If all four switch TFTs are working properly, the capacitor array can be used to split the poles even if there is a great shift in AC performance from the simulation results.

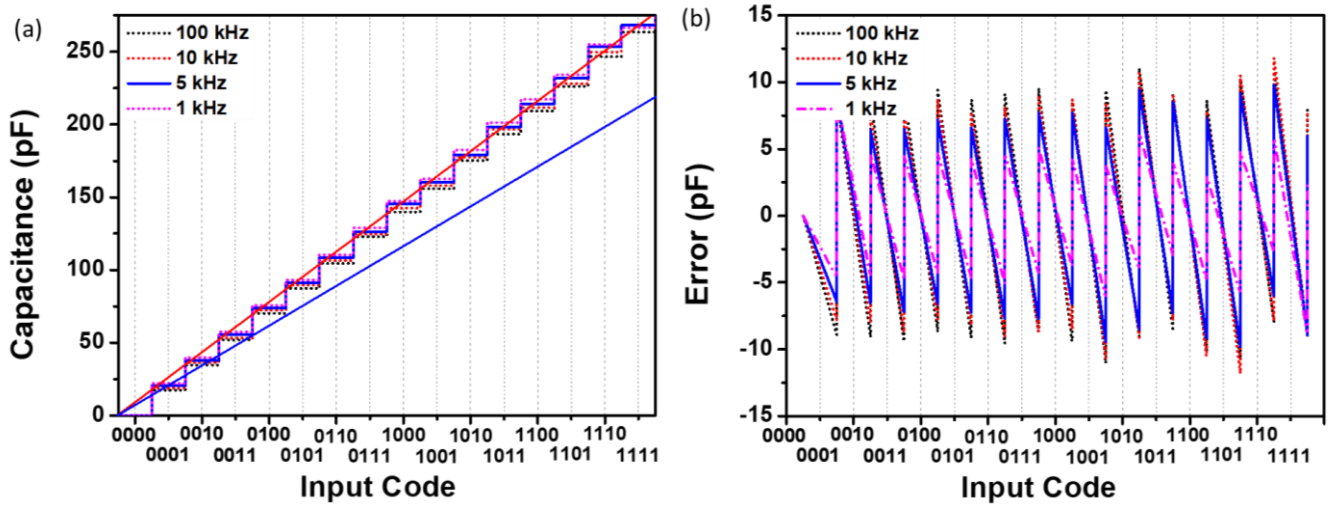

Fig. 5.17. (a) Capacitance and (b) the quantisation error of the capacitor array.

5.4.3. Output Stage

The output stage is the second stage of the amplifier, which further amplifies the output signal and regulates the final output voltage to an appropriate level. In this section, an individual amplifier with the same circuit structure as that used in the output stage was tested. As shown in Fig. 5.18 (a), the output stage had a common-source structure. A depletion-mode transistor, T_2, was used as the active load. The driving transistor, T_1, could be biased in both the saturation region and the sub-threshold region. Due to two design flaws, namely the DC operating point failure (because the width of the load transistor was too small) and the lack of connection pads, the performance of this amplifier in the saturation region could not be verified. Additionally, measurements that required output buffers were not conducted. These problems will be corrected in future experiments.

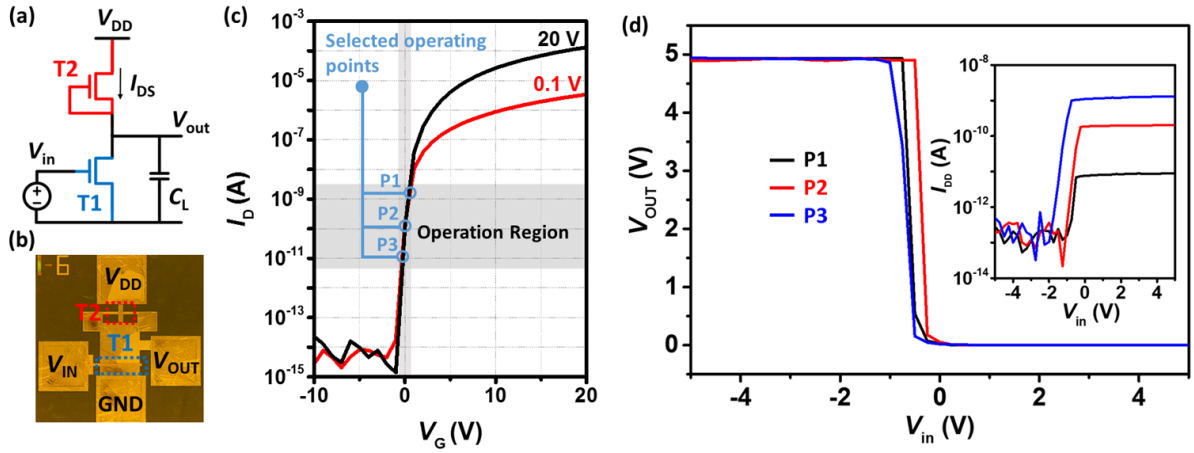

Fig. 5.18. (a) Schematic, (b) photo, (c) sub-threshold operating points, and (d) the corresponding input/output characteristics of the output stage.

During the measurements this structure worked perfectly in the sub-threshold region. Fig. 5.18 (c) showed the transfer curve of the driving TFT and three operating points that ranged from 10^{-11} A to 10^{-9} A. A square wave signal with a 10 V peak-to-peak amplitude sitting at 0 V was used as the input signal. The output signals and the operating currents are shown in Fig. 5.18 (d). In all three operating regions, this structure showed exceptional sensitivity to the input signal.

To investigate the potential of using this structure in ultra-low power electronics, it was first compared with a diode-load common-source amplifier. The comparison results are shown in Fig. 5.19 (a). With the same aspect ratios, supply voltage, and input signal, the sub-threshold depletion load amplifier operated at a working current that was 10^4 times lower than the diode-load amplifier. Using the common-source amplifier as an inverter, the depletion load amplifier could switch off much faster than the diode-load amplifier.

Once this structure's advantages in low-power electronics were confirmed over conventional diode-load amplifiers, the minimum supply voltage without interfering with the performance was sought. The output characteristics of the driving transistor and the depletion-mode transistor are shown in Fig. 5.19 (b). Overlaps between these two sets of curves indicated that this structure could operate even if the supply voltage dropped to 0.25 V. Fig. 5.19 (c) and Fig. 5.19 (d) show the output signals and the corresponding operating currents under different supply voltages. The measurement results proved that this structure could operate under a supply voltage as low as 0.25 V. Moreover, the operating current was less than 10×10^{-11}A in all tested circumstances.

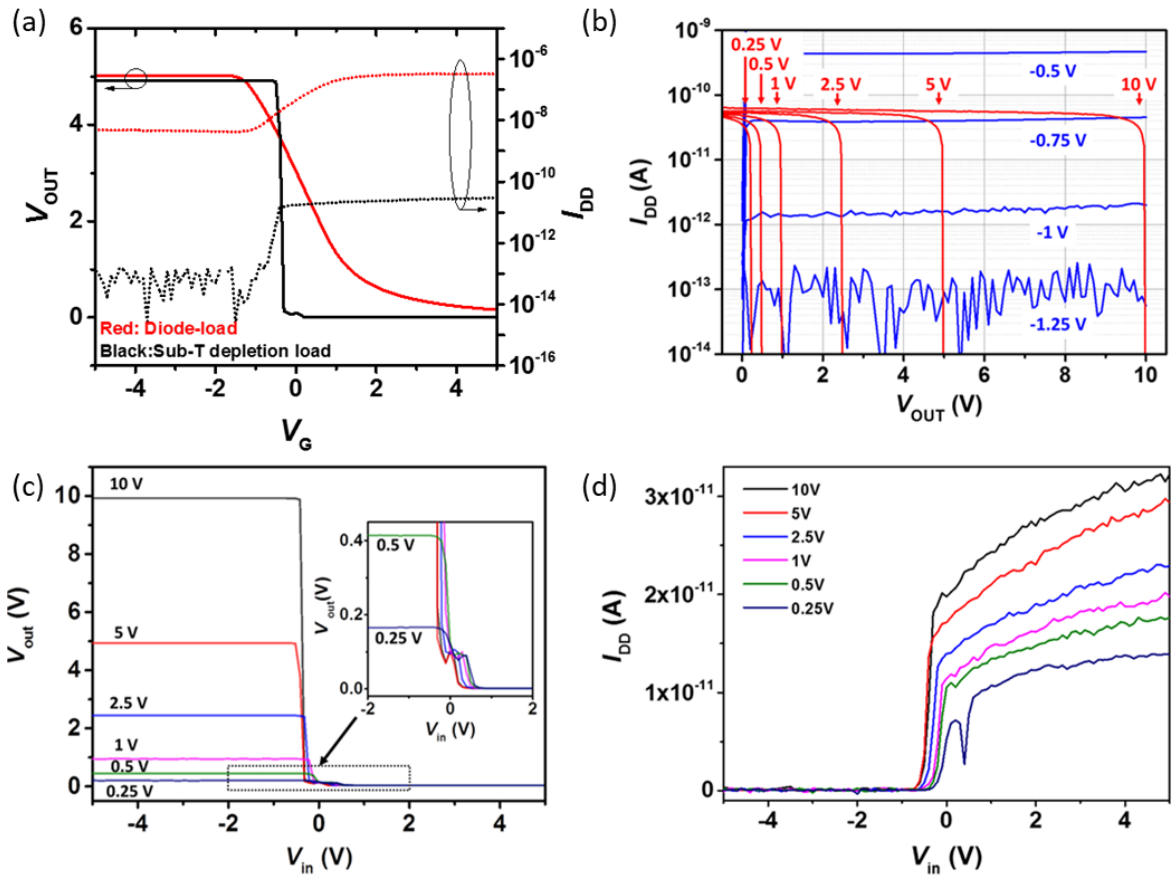

Fig. 5.19. (a) Comparison between diode-load and sub-threshold depletion load. (b) Output characteristics of the load transistor and the driving transistor. (c) Output signals of the amplifier and its (d) corresponding operating currents.

Based on the information above, this structure has great potential for use in ultra-low power electronics. Front-end circuits for bioelectronics, more specifically, the signal amplifying or low-speed digital signal processing circuits, are ideal application scenarios for this structure.

5.4.4. Proposed Amplifier

As shown in Fig. 5.13 (a), the proposed amplifier has 10 I/O terminals in total: two for voltage supply, one for ground, two for input signal, one for output, and four to control the switches. The output terminal was connected to the external source follower so that the load capacitor did not have a significant impact on the performance of the proposed amplifier. To ensure that the measurement results were reliable, the performance of the source follower was verified. Its gain was 1.0013 and its THD was less than 0.1%. The output signals of the proposed amplifier had to be kept in the measurement range of the source follower, which was determined by its core

component, the MCP601. MCP601 is a rail-to-rail op-amp that works with supply voltages up to ±5.5 V. For this measurement, V_{DD1} and V_{DD2} of the proposed amplifier were capped at 5 V. The DC level of the input signal was 2.5 V. The turn-on voltage for the switch was 15 V, and the turn-off voltage was -15 V.

First, all the compensation capacitors were disconnected, and two 50 Hz, 12.5 mV sine waves with a 180° phase difference were used as input signals. Fig. 5.20 shows the output signal. It had a DC level of 2.31 V, an amplitude of 1.21 V, and the THD was 6.34%. The gain of the proposed amplifier was 33.70 dB at 50 Hz.

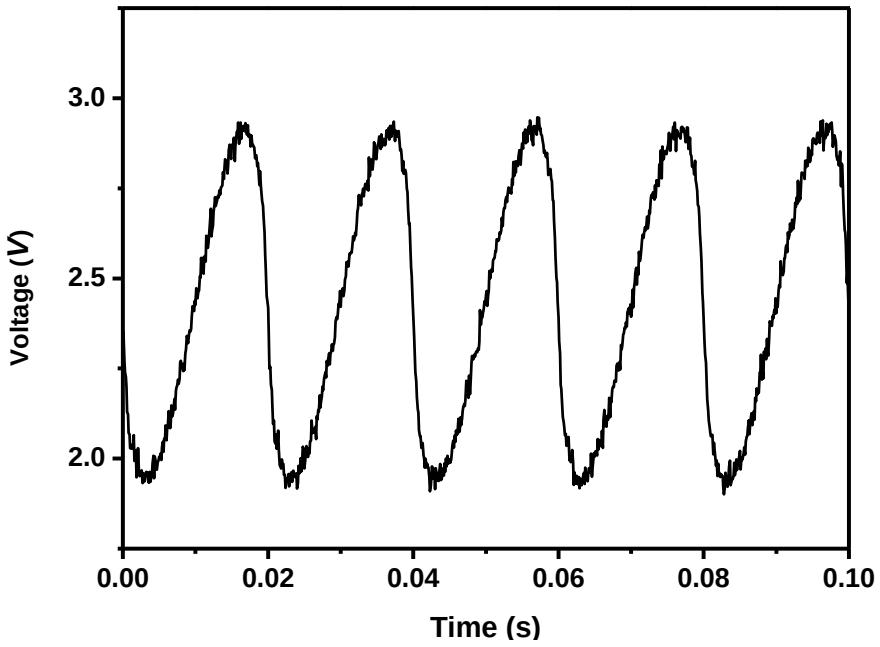

Fig. 5.20. Output signal of the proposed amplifier with a 50 Hz, ±12.5 mV pk-pk input sine wave.

Varying the input signal frequency and the code of the switch control signal obtained the Bode diagram of the proposed amplifier with different compensation capacitors. The measurement results are shown in Fig. 5.21. The blue region in the figure could not be measured with the current equipment, hence, the data in this region were estimated based on the behaviour of this amplifier in previous simulations. From the measured data, the gain of the proposed amplifier reached 33.7 dB at 100 Hz when the compensation capacitor was less than 6 pF. As expected, increasing the compensation capacitor split the poles and reduced the bandwidth. The cut-off frequency for the amplifier without the compensation capacitor was 400 Hz. The frequency with a 30 pF compensation capacitor was 100 Hz and that with 60 pF compensation capacitor was 10 Hz.

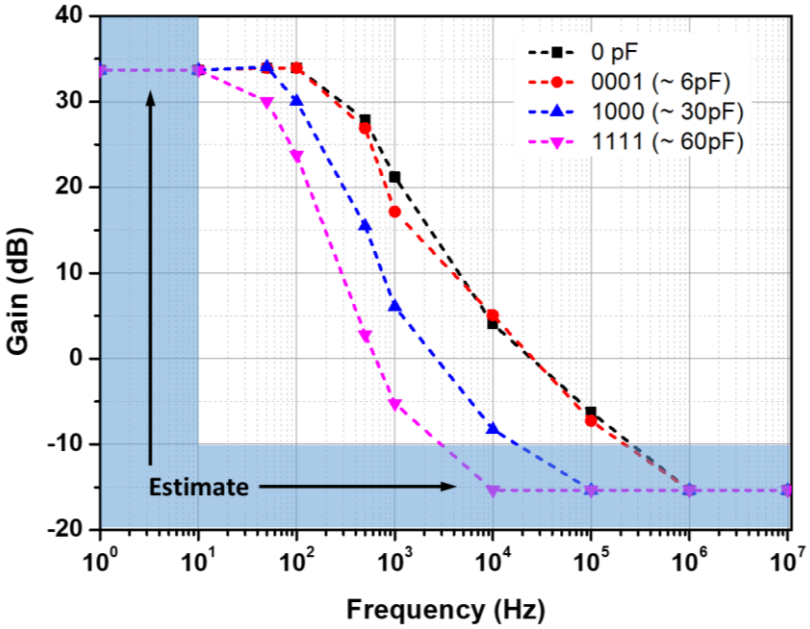

Fig. 5.21. Bode diagram of the proposed amplifier (measured).

The slew-rate was tested with a 1 Hz, 3.30 V peak amplitude square wave. The measurement results are shown in Fig. 5.22. The proposed amplifier charged the output load at 45.61 V/s and discharged at 79.28 V/ms. The difference in charging and discharging speed was due to the driving capacity gap between the driving TFT (saturation region) and the load capacitor (sub-threshold region).

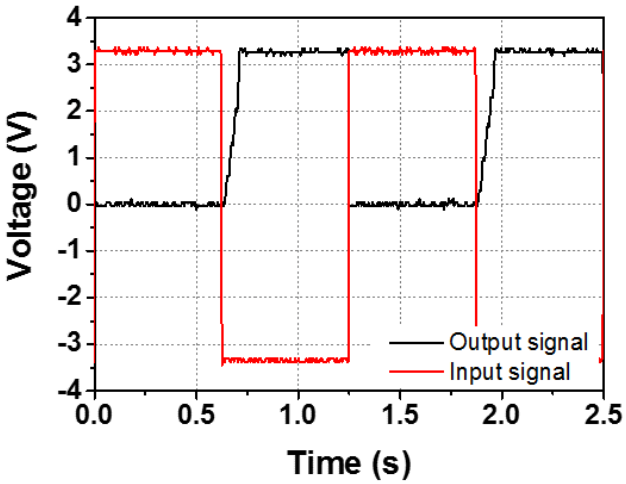

Fig. 5.22. Slew-rate testbench for the proposed amplifier.

To conclude, an all-TFT amplifier was successfully designed, fabricated, and tested. Although more than half the circuits failed in the same set of masks (details can be found in the appendix), this process provided very valuable experience. The

proposed amplifier shows great potential for use in low-frequency signal processing and will be integrated into bio-sensing applications in the future.

Chapter 6
Discussion, Conclusions and Future Work

This research aims to thoroughly investigate the AOS TFTs and find their potential applications. This is achieved using a bottom-up approach: the investigation started with materials, then it came over the TFT fabrication (characterisation) and finally covered the TFT circuitry.

During the material development, two semiconductor materials were fabricated and investigated: ZnON (as shown in the appendix) and ISO. The deposited ZnON showed great potential in building a high-mobility device, as Hall-effect measurements revealed that the deposited film had an intrinsic mobility of 73 cm^2/Vs. However, this material suffered from ion migrations. Nitrogen ions escaped at high temperature, and hydrogen ions in the dielectric layers (from the deposited SiN_x and SiO_x) could diffuse into ZnON, which created deep states and significantly boosted the off current. Ion migrations could occur during fabrication or annealing. For example, in the PECVD, the substrate was heated to 250℃, and thus caused the ion migration. Encapsulation and surface treatment were effective at reducing ion migration. Due to time limitations, the ZnON TFT development could not be completed. ZnON will be investigated in future studies.

ISO was a promising semiconductor, possessing great transparency, outstanding air stability, and better light-stability than most other AOSs. Though mobility of the ISO used (10% SiO_2, 90% In_2O_3) was much lower than ZnON, it was the most suitable semiconductor for TFT device/circuit development under the circumstances. Moreover, compared with ZnON, ISO had better transparency, which made it more suitable for use in developing a transparent TFT. During the investigation of the deposited ISO films, multiple characterising methods were implemented to verify its structural and

electrical properties. From the measurement results, band structure of the deposited ISO films was established for the first time. There was, however, a remaining issue: it was assumed that the ISO had a direct bandgap structure. Though most AOSs are direct bandgaps, a DFT simulation would have been helpful to determine the actual status of the ISO band structure. To further understand the material, studies have been planned with with Prof. John Robertson, who is running DFT simulations on ISO.

With a solid understanding of the ISO material, the full-photolithography TFT process was developed on a glass substrate. All available equipment in the division were studied and characterised. Non-uniformity caused by the random variations in process conditions were taken into consideration, such that robustness was obtained. First, all possible combinations of two adjacent deposition or etching processes were listed and tested. The combinations that could meet the uniformity requirements and would not cause any damage to the prior layers were selected to be used for device development. Based on the previous experiment, a six-mask TFT circuitry process (including two optional masks for an etch stopper layer) were developed. The spatial uniformity of this process was tested to establish a Monte Carlo simulation environment. Intra-wafer, inter-wafer, and batch-to-batch uniformity data were collected and analysed using a parameter extraction toolkit in MATLAB. The AI toolbox in MATLAB will be used for automated extraction in the future.

The temporal stability of the ISO TFT was investigated as well, which reflected the material defects, and thus helped to further understand the device. The fundamental difference between the full-photolithography process that was developed and the shadow-mask process in previous reports [80], [81] was that this process was verified for circuit design. Efforts have also been devoted to transfer this process from a glass substrate to a plastic substrate. The main challenges include alignment issues caused by the shrinkage of the plastic substrate and formation of via holes. The alignment issue was solved using pre-heating combined with fixing the plastic on a rigid substrate using a wafer dicing film. However, the via hole formation issues on plastic remain, and new dry etching methods can be used to solve this problem.

For the development of high-performance all-TFT circuits, two major problems need to be overcome. The first is a lack of active load, as ideal active load for an analogue circuit is a current source that is independent of external signals. A conventional CMOS amplifier uses a P-type transistor to generate this behaviour. However, in this case, only N-type transistors can be used in the all-TFT circuit, which

introduces a huge challenge in active load design. For monotype transistor amplifier design, four configurations that are suitable for the ISO TFTs were fabricated and tested. The depletion-mode load offered the best performance, and the highly-anticipated bootstrapped load was not stable during transient measurements. Further analysis revealed that this was likely caused by an inappropriate aspect ratio of the bootstrapping transistor, which will be corrected and tested in the next set of masks. The second problem is a large parasitic capacitor, which reduces the bandwidth of circuits and may cause instability under certain circumstances. Two approaches were used to reduce the impact of the parasitic capacitor: the layout approach and the circuitry approach. The layout approach used an island-structure to minimise the gate-drain capacitor. The gate-drain capacitor contributed most to the miller capacitor in an amplifier. Reducing this capacitor greatly increased the bandwidth. The circuitry approach used capacitor peaking and inductive peaking techniques to boost the bandwidth. The capacitive peaking configuration provided a new method to analyse the stability of a closed-loop amplifier, as maximised bandwidth could be achieved with a suitable peaking capacitor.

The design flow for an all-TFT amplifier is as follows: general calculations, circuit simulations, layout design, circuit fabrication, and measurement. In the general calculation, depletion-mode TFTs were selected as the active load for the amplifier, because of outstanding gain performance. The depletion-mode transistor fixed the DC operating voltage of both the differential input pair and the current mirror. The same working principle was applied to the second stage of the amplifier. Between the first and second stage of the amplifier, a switch capacitor array was used to compensate for the stability of the amplifier. Simulation results showed that the proposed amplifier had a gain of 40 dB, and the cut-off bandwidth (3dB bandwidth) reached 1 kHz with a relatively small phase margin. The phase margin could be manipulated using the switch capacitor array. Layout design of the amplifier strictly followed the design rules stated in the second chapter. The fabrication process used for this amplifier was the four-mask ISO TFT process on a glass substrate. Prior to the amplifier measurement, individual circuit building blocks were tested. The amplifier stage showed great open-loop performance. SNR of the 4-bit switch capacitor array was 25.67dB, and the controllable range of the switch array used in the amplifier was from 0 pF to 60 pF. Measurement results of the all-TFT amplifier demonstrated that using the capacitor array efficiently increased the stability of the all-TFT amplifier. Due to the large parasitic capacitor (caused by the limitation of alignment, which was dependent on the photolithography

equipment), the overall performance of this amplifier was not optimised, but it was the very first attempt at a mixed signal all-TFT circuit. Further improvement of the performance of the ISO TFT circuits requires a significant reduction in the parasitic capacitor. Therefore, the development of self-aligned TFTs will be pursued, and the first set of self-aligned TFT masks have already been designed. Self-alignment related experiments will be conducted.

In this research, most of the concept verifications were conducted using the ISO TFTs, including the island structures, the amplifier configurations, and the flexible fabrication process. These concepts can also be applied to other transistor techniques, especially for TFTs that share similar behaviours. Furthermore, multiple TFT processes will be integrated in the future to achieve better circuit performance. For example, the P-type CuO_x or the printed organic TFT could be used as the active load. Nevertheless, novel application scenarios have also been found. In the second set of masks, DNA sensor arrays based on an ISO TFT have already been designed. Work will continue with Dr. Hanbin Ma to construct a portable DNA sensing platform using the ISO TFTs.

To conclude, this dissertation encompassed the material, device, and system integration of ISO TFTs. New information was added to the current pool of knowledge on AOS TFTs, as follows:

- The ISO semiconductor was studied in detail to build a useful TFT and to understand the working mechanism behind the device. The schematic band diagram of the ISO film was extracted using UPS and UV-Vis for the first time. It was also the first trial in developing a full-photolithography process with optional etch stopper layers for the ISO TFT. An extra-low-temperature plastic-compatible fabrication process was investigated and verified as well. TFTs using multiple ISO deposition recipes were characterised. The interfaces, especially the metal-semiconductor interfaces, were studied extensively.

- The spatial and temporal uniformity data of ISO TFTs were collected to establish a Monte-Carlo simulation environment. This was the first use of a Monte-Carlo simulation in circuit design. A parameter extraction toolkit was developed to accelerate the process and reduce the repetitive workload. Stress measurement revealed that hot carrier injection and trapping in the dielectric layer were the primary causes of threshold voltage shift. Photo-stability tests confirmed that

shallow doubly-ionised donor states were generated in the ISO film under illumination.

- Two urgent challenges, namely the lack of proper active load and the large parasitic capacitance, in all-TFT analogue circuit design were investigated. In-depth analysis of these issues and verified applicable solutions were given as well.

- A new all-TFT amplifier structure was proposed. It solved the active load, current mirror, and stability compensation issues. Moreover, the proposed amplifier successfully integrated a 4-bit capacitor array to compensate for stability, which made it the world's first mixed signal all-TFT circuit.

There are still many opportunities/challenges that are worth investigating. For the improvement of this work, potential promising areas include:

- The zinc oxynitride (ZnON) semiconductor: 10 months were spent on the development of ZnON TFTs. The project was suspended, due to time and budget limitations. However, a working transistor was nearly developed. Compared with ISO, ZnON offers more freedom in controlling the cations of the semiconductor, thus the deposition conditions can be manipulated to build different semiconductors for different applications.

- Extra-low-temperature TFT circuitry processes on plastic: the current TFT plastic does not support the formation of via holes, which is curial in circuitry fabrication. The full-photolithography process with a new dry etching technique should be investigated to develop a TFT process for circuits on plastic.

- Using AI toolboxes in the parameter extraction toolkit: The parameter extraction process is repetitive work that could be done by the AI toolboxes in MATLAB. Exploring this possibility will require writing a fully automatic parameter extraction toolkit.

- Threshold voltage shift compensation in analogue circuits: a solution to the V_{th} shift in analogue circuits is still being sought. Conventional compensation schemes used in AMOLED did not suit analogue circuits. If this problem was

solved, it would be one step towards the commercialisation of front-end all-TFT circuits for sensing applications.

- New digital/analogue circuits: there were many design flaws in the second set of masks (more than half the circuits failed). Many of the designs should be corrected/improved, including the DC operating point failures, adding output buffers, and using feedback to evaluate how much the compensation capacitor split the poles.

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Appendix A

Zinc Oxynitride TFT

The semiconductor films deposited based on multiple zinc oxynitride deposition recipes have been characterised. The deposition pressure, RF power and gas-flow control measurement results are shown in Fig. A.1 and Fig. A.2.

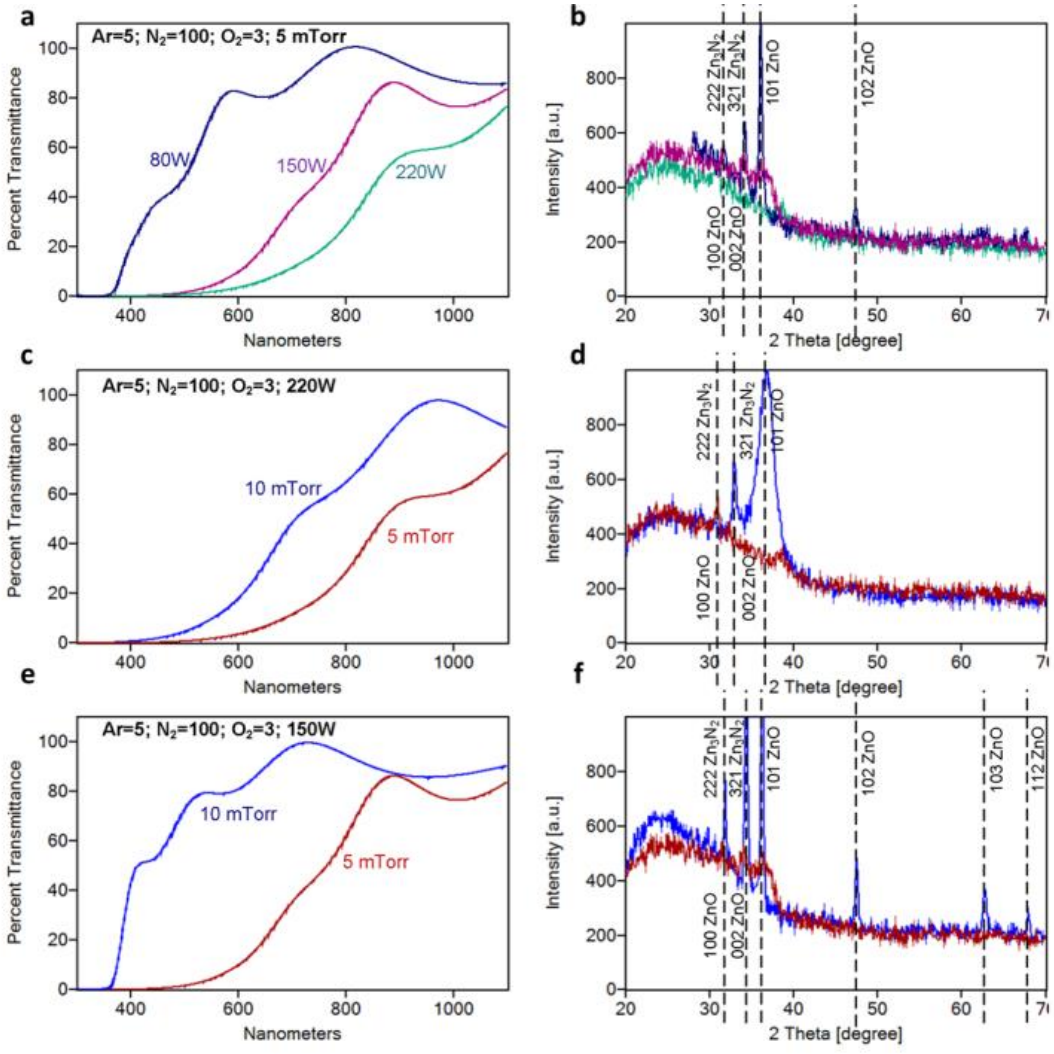

Fig. A.1 UV-VIS (left) and XRD (right) measurement results for RF power and pressure control experiments, (a) and (b) RF power control; (c), (d), (e) and (f) pressure control.

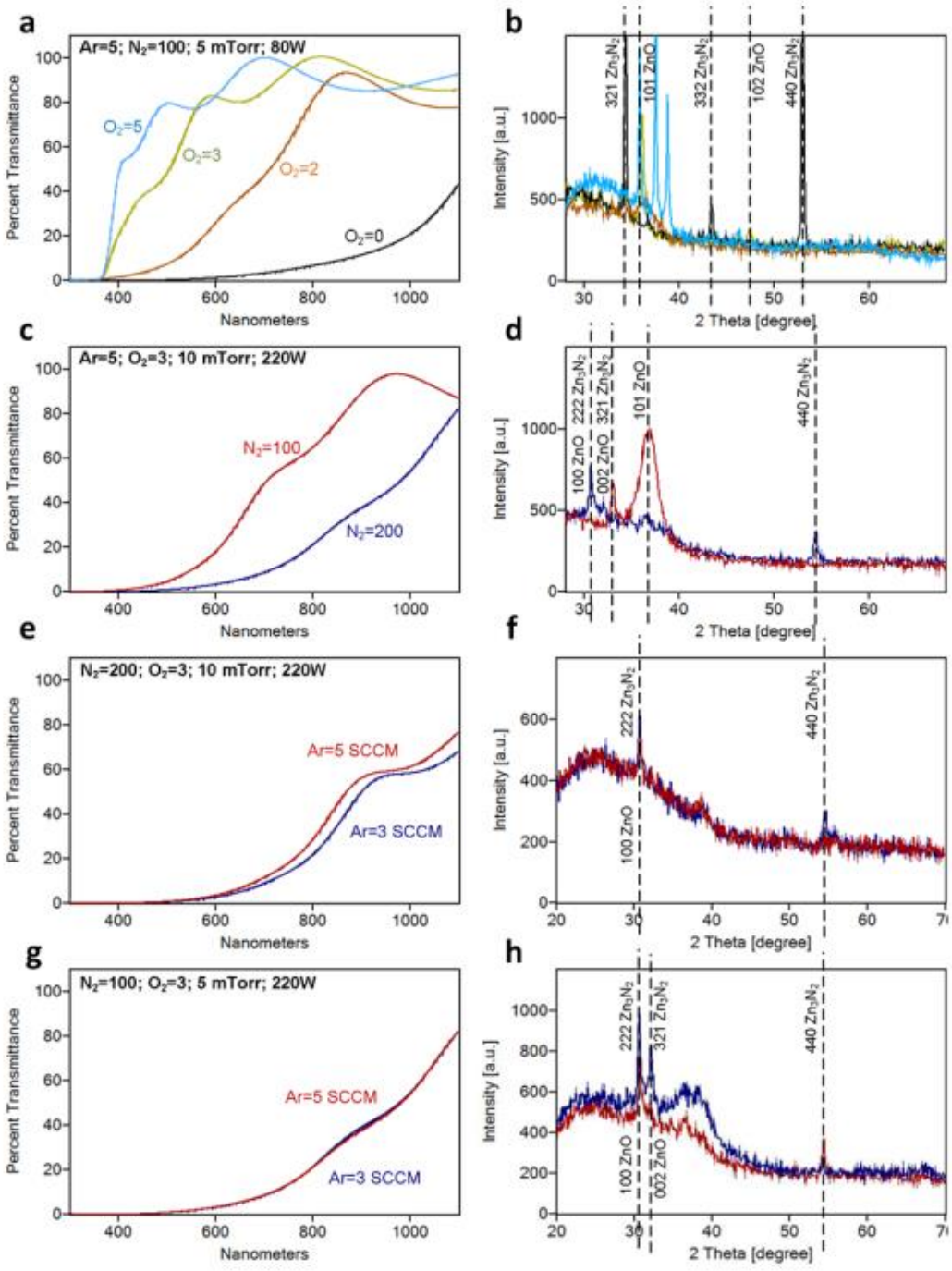

Fig. A.2 UV-VIS (left) and XRD (right) measurement results for gases control experiments, (a) and (b) oxygen control; (c) and (d) nitrogen control; (e), (f), (g) and (h) argon control.

The transfer characterisation results of three selected TFTs are shown in Fig. A.3, where switching behaviours were observed. The chamber pressure was set at 12.5 mTorr and the RF power was 150 Watt. Judging from our experience, it is highly

likely that a decent device can be fabricated by reducing the deposition pressure and RF power.

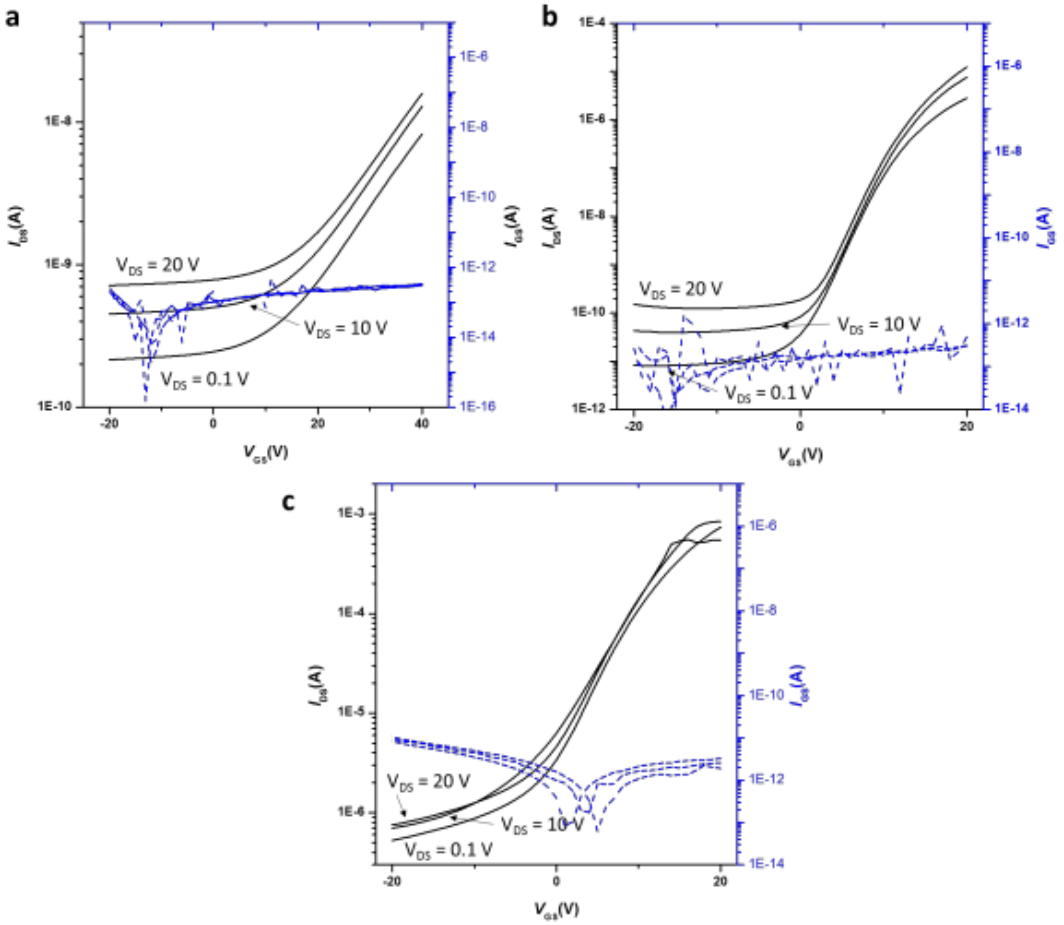

Fig. A.3 Effect of nitrogen reactant on TFT performance (a) N2/(N2 + O2) = 95.2% (b) N2/(N2 + O2) = 97.1% (c) N2/(N2 + O2) = 98.5%.

Appendix B

Masks and Measurement Kit

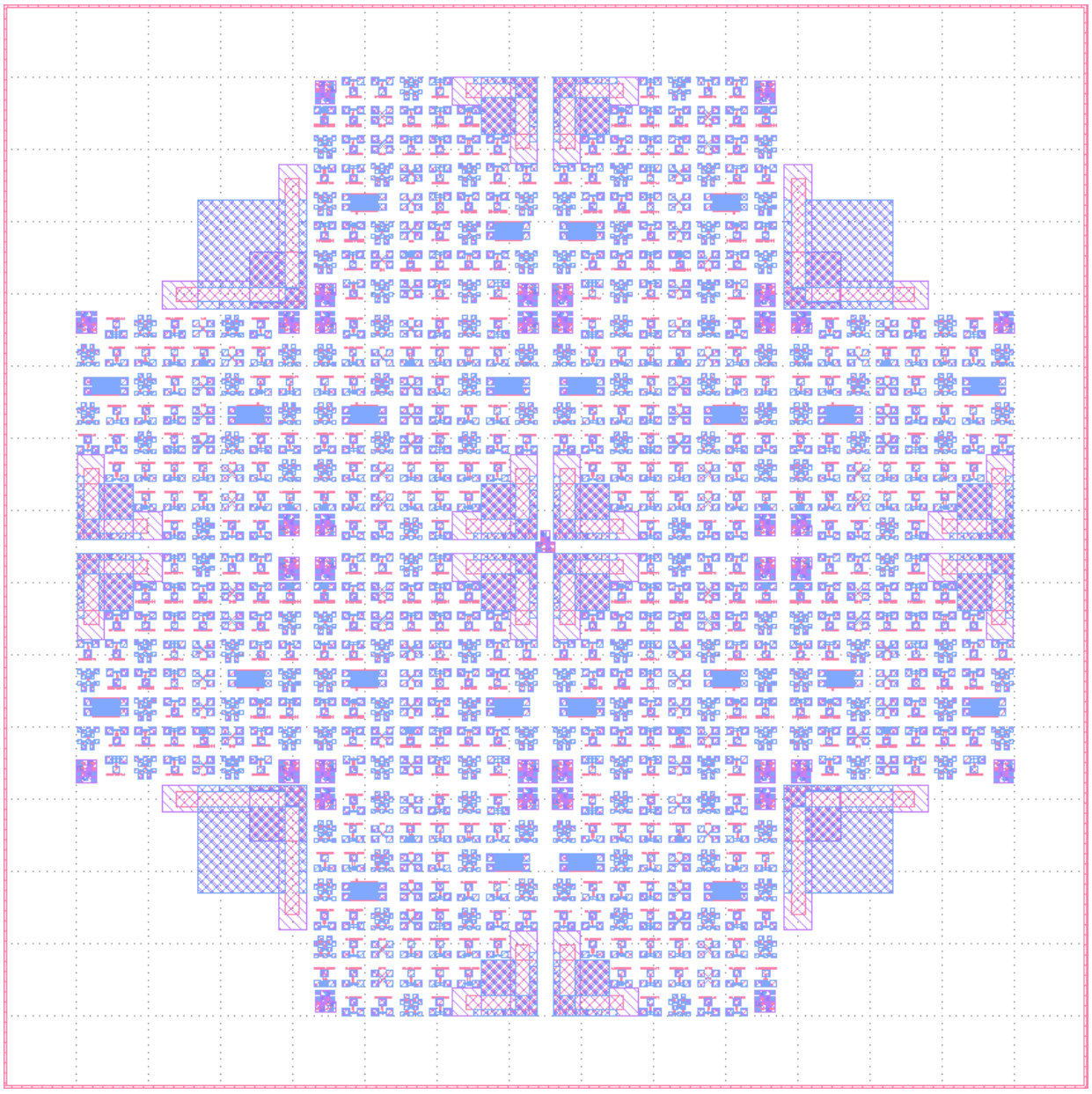

Fig. B.1. First set of Masks.

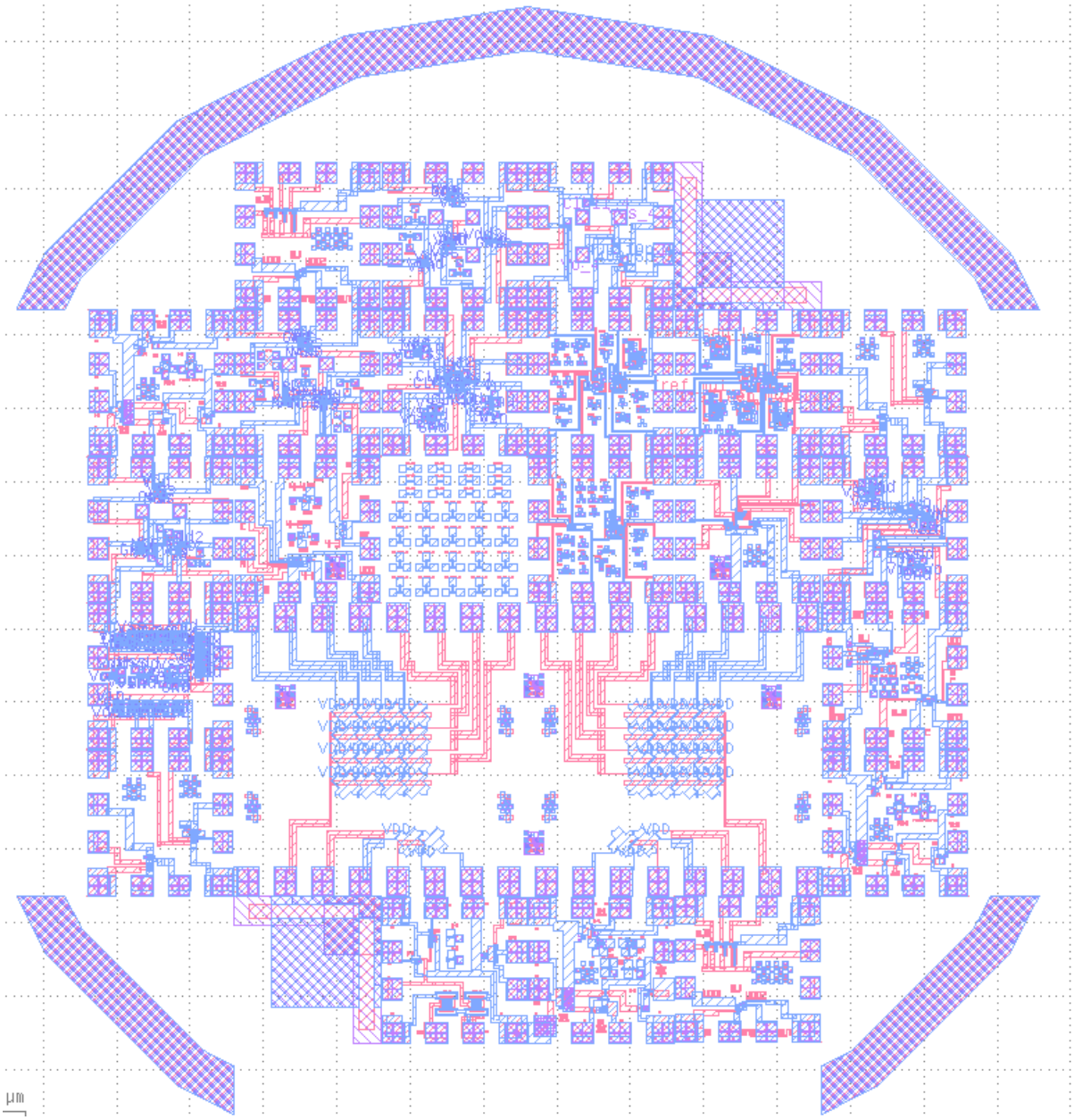

Fig. B.2. Second set of Masks.

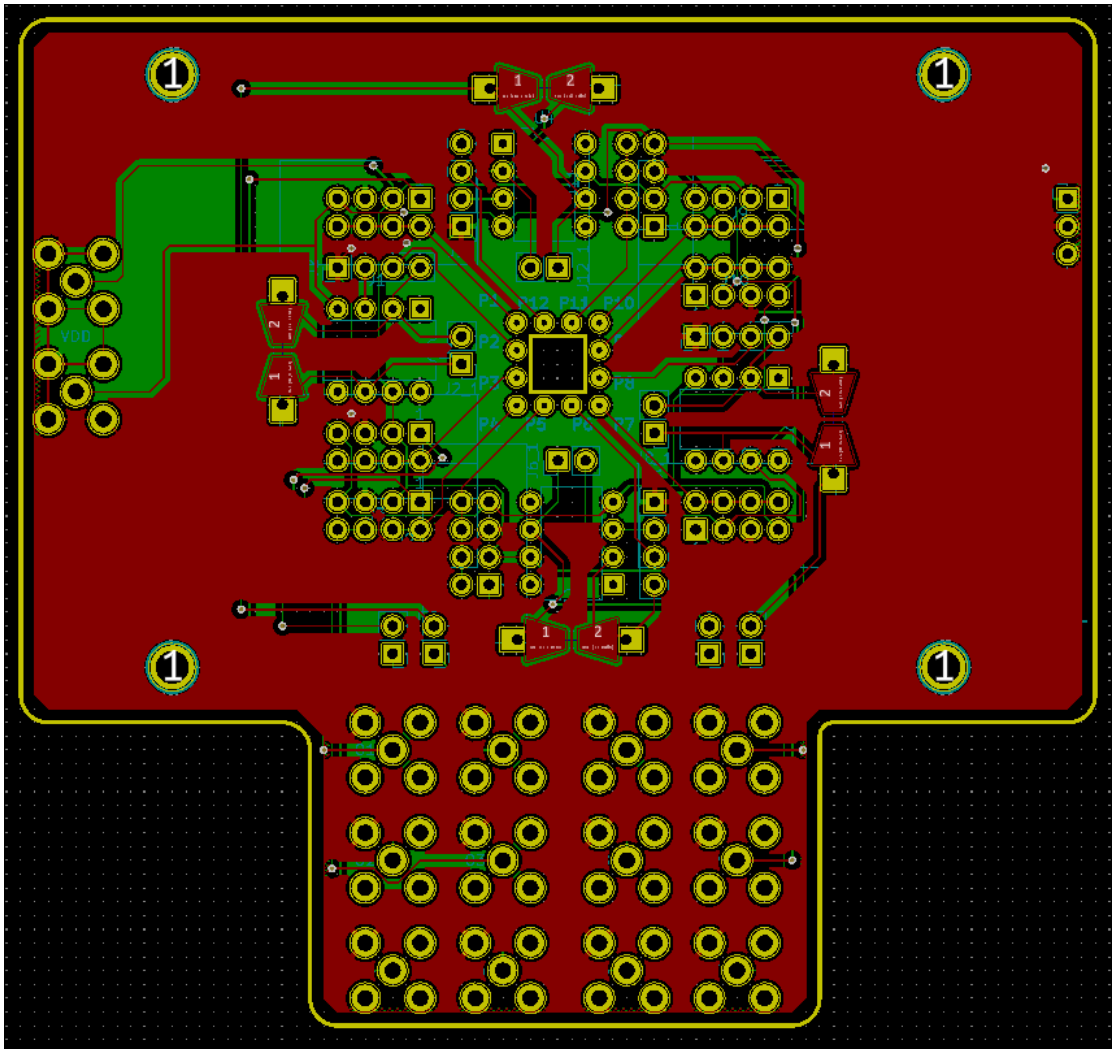

Fig. B.3. PCB layout of the measurement kit.

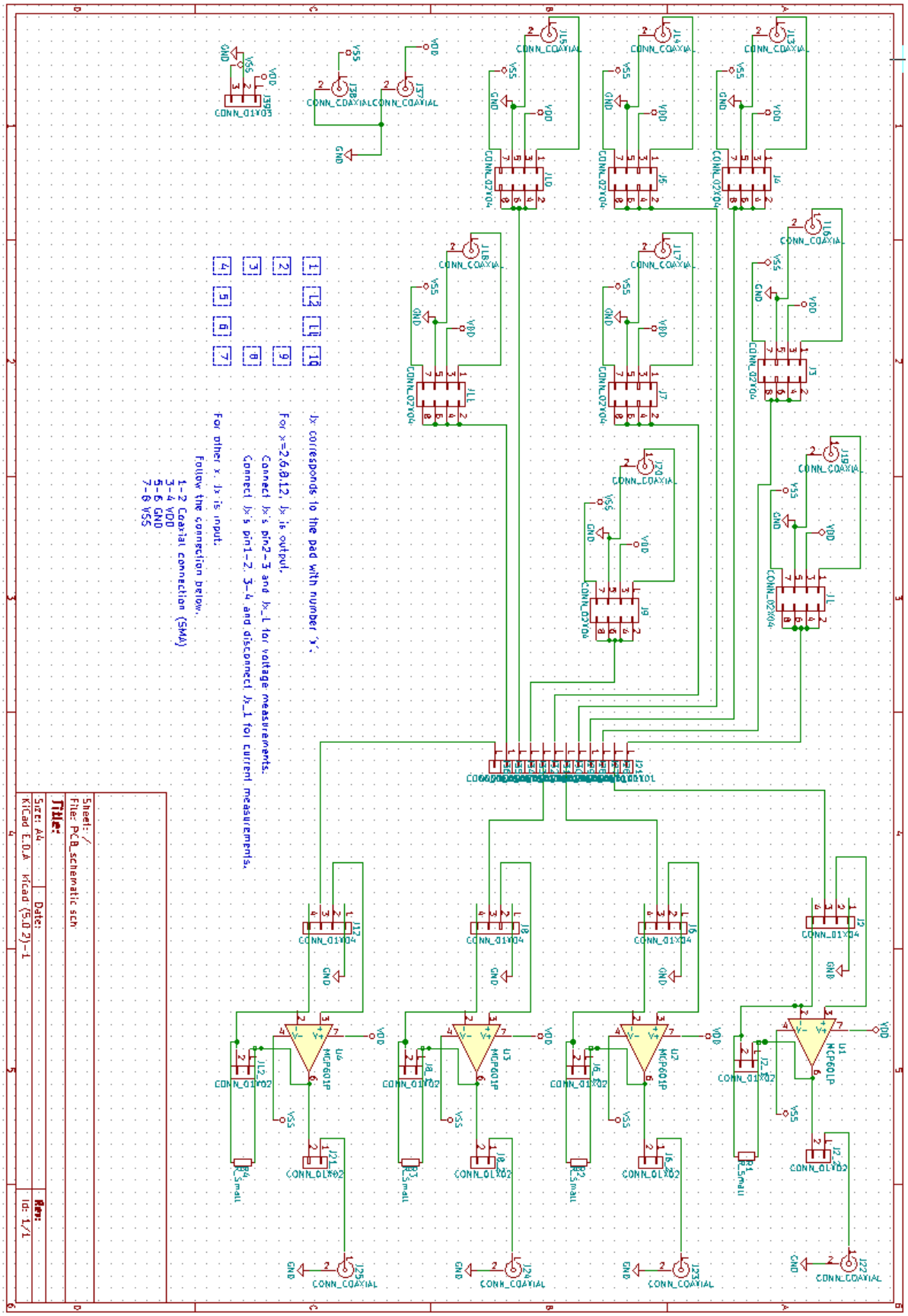

Fig. B.3. PCB schematic of the measurement kit.

Appendix C

Summary for All the Designed Circuits

Table C.1. A summary for all the designed circuits.

Circuits and Label	Status	Notes
Diode-load 1.1	Completed	
Depletion 1.2 (different load)	Completed	
Bootstrap: Different aspect-ratios, diode load: • 80/20 3.3 • 40/20 1.3 • 20/20 1.4 Different Capacitor: • C 500*350 3.4 • C1000*350 1.3 • C1000*700 3.1 Different Load: TFT- depletion 3.2	Suspended	Simulations had passed, but signal distortions (THD) is too large to be integrated into more complex circuits.
Full adder 4.1	Terminated	DC operating point failure
Schmitt trigger 4.2 4.4	Terminated	DC operating point failure
Monostable Multivibrator 4.3	Terminated	DC operating point failure
SR latch 5.1	Terminated	DC operating point failure
Level shifter 6.1	Completed	
Binary capacitor array 6.2	Completed	
Buffer 2.1	Completed	
Layout improvement: • Transistor: • T1* 2.5 • T4* 2.6 • Diode-load 2.3 • Depletion 2.2 • Bootstrap: 2.4	Completed	
Current source 3.5	Completed	
Bias stage • Diode load 3.6_400/20 3.8_800/20 • Depletion 3.7	Completed	
Cascode (depletion & bootstrapped)7	Suspended	Cannot measure due to measurement kit design flaws
Amp 8	Completed	
TIA	Suspended	Simulation passed, to be fabricated in next set of masks.

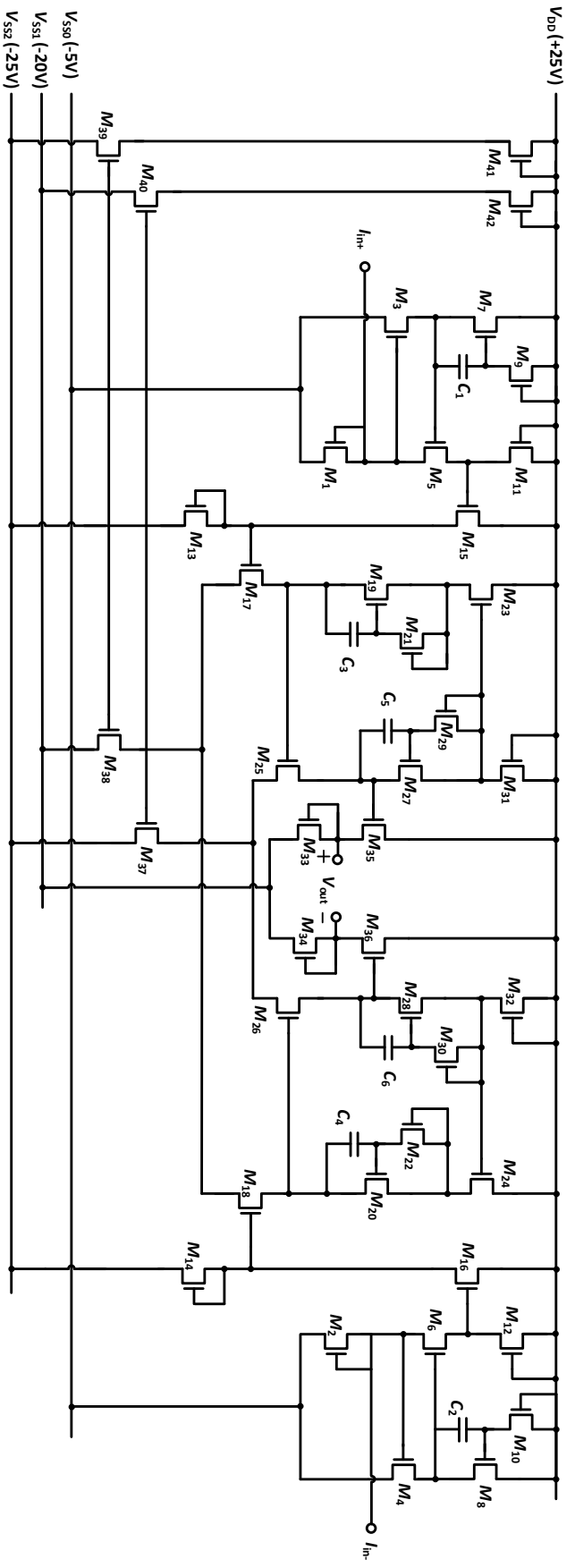

Fig. C.1. The TIA to be verified in the next set of masks.

Table C.2. Simulation results of the TIA.

Specifications	This work
Number of transistors	42
Output dynamic range	$11V$
Input impedance	$2k\Omega$
Output impedance	$18k\Omega$
Static power consumption	$28.4mW$
Transimpedance gain	$130dB$
Bandwidth	$10Hz - 3kHz$
Slew rate	$0.1V/\mu s$