RF POWER AMPLIFIER AND ITS ENVELOPE TRACKING

A Dissertation

by

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ABSTRACT

With unprecedented growth of functional density in portable devices, battery run-time has become a critical factor in the wireless market. Due to significant power consumption in wireless devices, the power amplifier (PA) plays a critical role in determining battery run-time. Usually, the PA operates at power back-off (PBO) levels, but its efficiency suffers at these levels. In order to improve power efficiency at PBO levels, the envelope tracking (ET) technique and digital polar architecture are commonly favored.

This dissertation introduces an agile supply modulator with optimal transient performance for the envelope tracking supply in linear power amplifiers. For this purpose, an on-demand current source module, the bang-bang transient performance enhancer (BBTPE), is proposed. Its objective is to follow fast variations in input signals with reduced overshoot and settling time without deteriorating the steady-state performance of the buck regulator. The proposed approach enables fast system response through the BBTPE and an accurate steady-state output response through a low switching ripple and power efficient dynamic buck regulator. Fast output response with the help of the added module induces a slower rise of inductor current in the buck converter that further assists the proposed system to reduce both overshoot and settling time. To demonstrate the feasibility of the proposed solution, extensive simulations and experimental results from a discrete system are reported. The proposed supply modulator shows 80% improvement in rise time along with 60% reduction in both overshoot and settling time compared to the conventional dynamic buck regulator-based solution. Experimental results for a PA using the LTE 16-QAM 5 MHz standard shows improvement of 7.68 dB and 65.1% in ACPR and EVM, respectively.

In a polar power amplifier, the input signal splits into phase and amplitude components using a non-linear conversion operation. This operation broadens the spectrum of the polar signal components. The information of amplitude and phase contains spectral images due to the sampling operation in non-linear conversion operation. These spectral images can be large and cause out-of-band emission in the output spectrum. In addition, during the recombination process of phase and

amplitude, a delay mismatch between amplitude and phase signals, which can occur due to separate processing paths of amplitude and phase signals, causes out-of-band emissions, also known as spectral regrowth. This dissertation presents solutions to both of the issues of digital polar power amplifier: spectral images and delay mismatch. In order to reduce the problem of spectral images, interpolation of phase and amplitude is proposed in this work. This increases the effective sampling frequency of the amplitude and phase, which helps to improve the linearity by around 10 dB. In addition, a novel calibration scheme is proposed here for the delay mismatch between phase and amplitude path in a digital polar power amplifier. The scheme significantly reduces the spectral regrowth. The scheme uses the same path for phase and amplitude delay calculation after the recombination that allows having a robust calibration. Furthermore, it can be executed during the empty transmission slots. The proposed scheme is designed in a 40 nm CMOS technology and simulated with a 64-QAM IEEE 802.11n wireless standard. The scheme achieved 7.57 dB enhancement in ACLR and 84.35% improvement in EVM for a 3.5 ns mismatch in phase and amplitude path.

DEDICATION

To my mother, my father and my wife

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Contributors

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1. INTRODUCTION

1.1 Background

1.1.1 Wireless Communication Trend

In this era of connected devices, wireless communication becomes a critical node to have a smooth experience in day-to-day life. Fig. 1.1 shows a scenario of connected devices. In this, cellphones plays an important role due to its portability with users. Furthermore, with an increase in number of connected devices and surge in gaming and video streaming, we have seen requirements of more and more data in the wireless communication. The tremendous increase of network data traffic has been seen in the cellular network [1], [2].

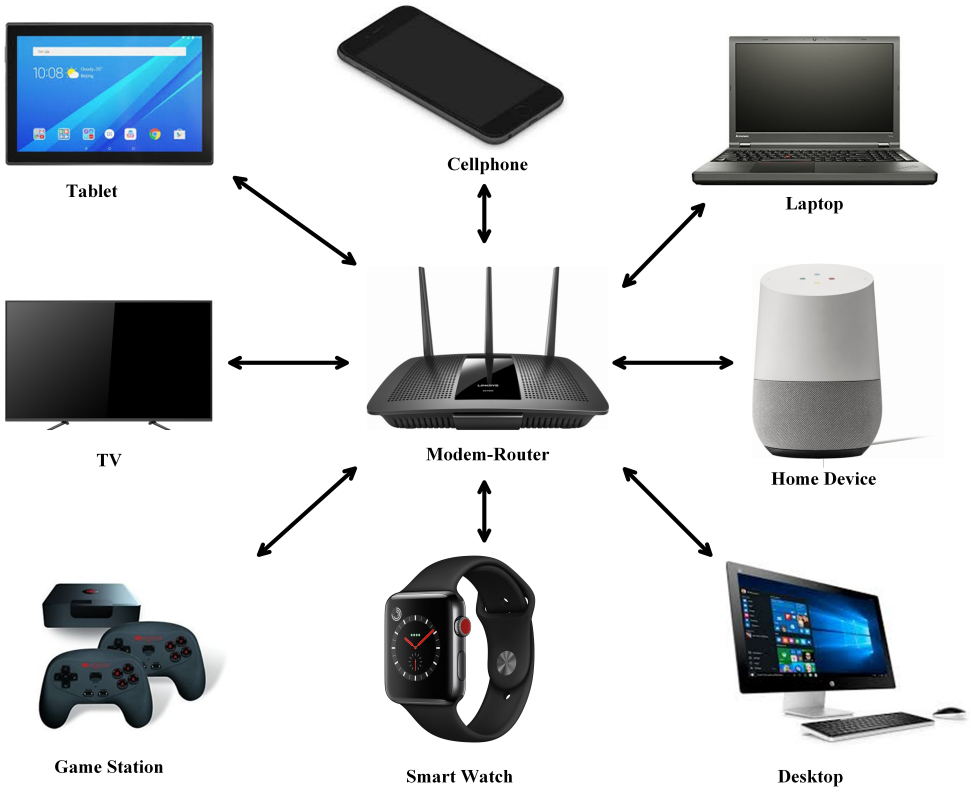


Figure 1.1: Example of Connected Devices.

Besides network data, accessibility, connectivity and cost effectiveness are important parameters for wireless communication. These aspects of wireless communication become more important when having infrastructure of wired communication is costly. Also, the wireless communication systems have shown possibilities of connecting remote parts of the world.

This explosion of network data traffic is only feasible by a demanding wireless standard that comes with large baseband bandwidth at high RF frequency [3]. These standards come together with larger and larger PAPR (peak to average power ratio). From GSM (Global System for Mobile Communication) to IEEE 802.11g wireless standard, the PAPR increases from 0 dB to almost 10 dB. For a wireless standard, the PAPR is given by $10log_{10}(N)dB$, where N is number of sub-carriers used [4]. With upcoming standards, the number of sub-carries is increasing, hence PAPR. The comparison between these two wireless standards is shown in Table 1.1. This increment of PAPR comes with a lower power efficiency of power amplifier in wireless transmitter [5].

Parameters	GSM	IEEE 802.11g
Channel Bandwidth	200 kHz	20 MHz
Carrier Frequency	900, 1800, 1900 MHz	2.4 GHz
PAPR	0 dB	18 dB (theoretical)
Peak Data Rate	22.8 kbps	54 Mbps
Modulation Format	GMSK	QAM-16, QAM-64, QPSK, BPSK

Table 1.1: Wireless Communication Standard Parameters

1.1.2 Wireless Transmitter

Modern demanding wireless standards keep pushing innovation in the transmitter. A traditional transmitter architecture is shown in Fig. 1.2.

In wireless transmitter architecture, the information is first processed in the baseband processor. The processing in the baseband processor can include digital predistortion, timing alignment calibration for polar transmitter, etc. The digital output of the processor is converted to analog via D/A converter. The analog signal is put over RF frequency via mixer, and is transmitted via power

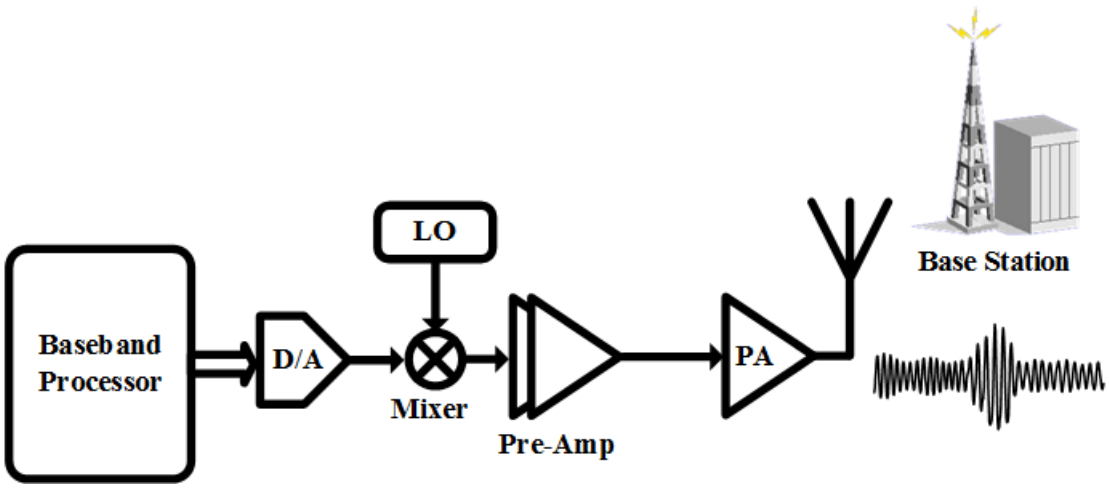


Figure 1.2: Wireless Transmitter Architecture.

amplifier through antenna as shown in the figure [6], [7].

In a wireless transmitter, I/Q mismatch, power amplifier linearity, mixer linearity, carrier leakage, oscillator pulling, spur mixing, etc. are important aspects to consider [8], [9]. The issue of I/Q mismatch leads to an error in the signal constellation [4]. The calibration of I/Q mismatch can be done with the help of a single sinusoidal input in an quadrature up-converter; it reduces the phase and amplitude mismatch between two paths (I and Q) [4]. In addition, DC offset of baseband paths (I and Q) leads to carrier leakage. This will also lead to an error in the constellation. It can also make it difficult to measure signals at receiver for low output power as the power of leakage carrier can dominate in the transmitter output signal. This case is especially true when a cellphone is near the base station then the signal power needs to reduce in order to avoid saturation at the receiver end. The simple way to avoid this issue due to carrier leakage is to have large baseband signal; however, it has an impact on the linearity in the transmitter chain. In order to nullify the carrier leakage, i.e., DC offset at the baseband, a DAC based calibration technique is used in the literatures [10].

Transmitter linearity is a very important performance parameter for a wireless transmitter. Its requirement depends upon the adjacent channel needs and error tolerance of a wireless receiver. ACPR (Adjacent Channel Power Ratio) and EVM (Error Vector Magnitude) are two important

parameters to characterize the transmitter linearity [4]. The specification of these parameters varies from standard to standard. Considering complexities involved in ACPR and EVM measurement, 1-dB compression point input/output is a simplified way to test the linearity of a transmitter. The 1-dB compression point is depicted in Fig 1.3. Due to a smaller input signal, the mixer linearity in the transmitter is less significant compared to the power amplifier. However, if the mixer is very non-linear then it can even dominate the linearity of the transmitter. In general, the power amplifier tends to compress before the mixer in a well designed transmitter [11].

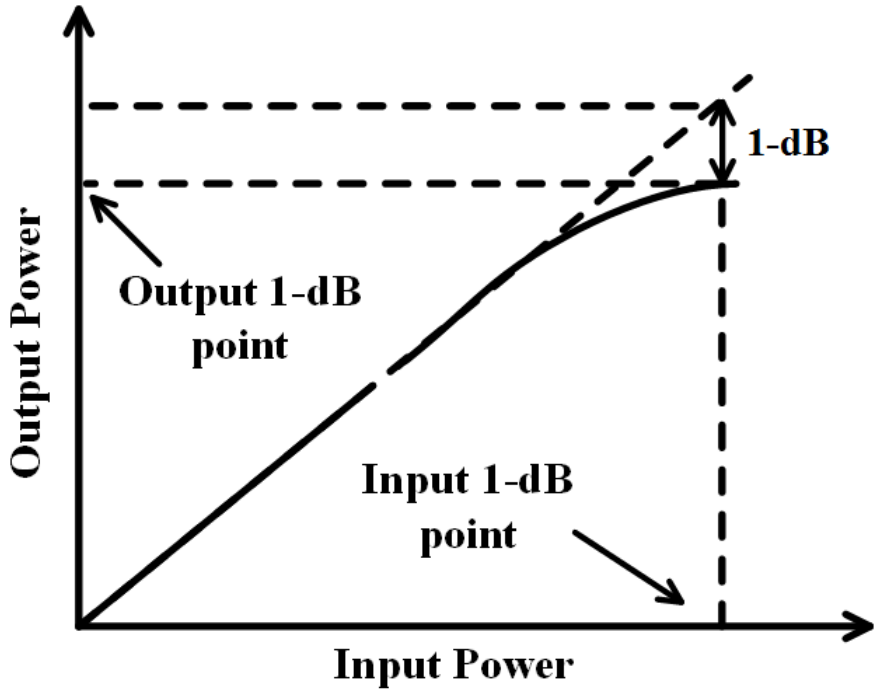


Figure 1.3: 1-dB Compression Point.

One critical issue in a direct-conversion transmitter architecture is oscillator pulling [12]. Due to large output power of the power amplifier, its output couples to various parts of the transmitter. The coupling remains strong even if the power amplifier is not sharing the substrate with the rest of the transmitter blocks. This coupling pulls the oscillator, and it generates more frequency components in its frequency spectrum than intended. The resulting spectrum of the spectrum passes into

the transmitter and generates unwanted spectrum at the transmitter output. The oscillator pulling becomes further stronger when LO signal is weak, or feedback loop of the oscillator is not strong enough to counteract the pulling [13]. The pulling gets smaller in case of a differential power amplifier because here positive and negative coupling cancels each other. This can be be removed in a transmitter architecture itself by having twice oscillator frequency and then divided it by two and use in the transmitter as shown in the Fig 1.4 [4].

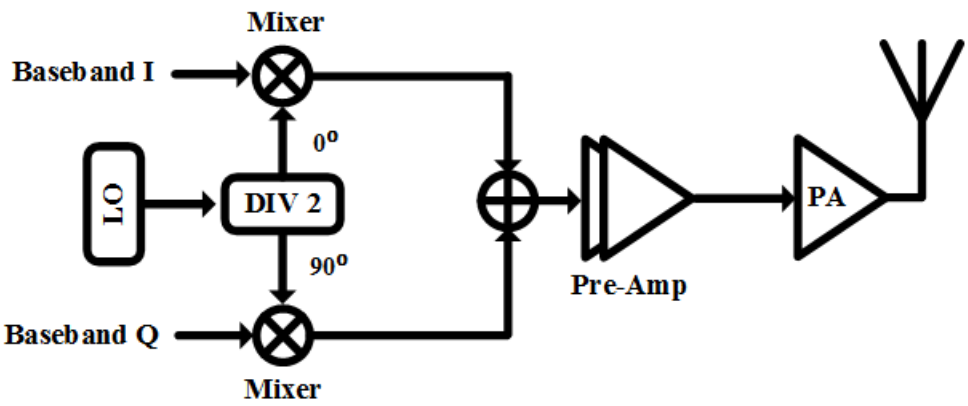


Figure 1.4: A Modified Direct-Conversion Wireless Transmitter Architecture.

Another architectural approach to solve the issue of the oscillator pulling is the heterodyne transmitter [14]. A typical architecture of heterodyne transmitter is shown in Fig. 1.5. In this, the baseband information, first modulated with an intermediate frequency via the first mixer, and then move to the RF frequency via the second mixer. Keeping the LO frequencies (LO1 and LO2 frequencies) away from the transmitter carrier frequency helps to save the transmitter from the issue of oscillator pulling [14]. The downside of the architecture is the complexity compared to the direct down-conversion transmitter. Besides this, mixing spurs and carrier leakage are dominating issues of this architecture [15].

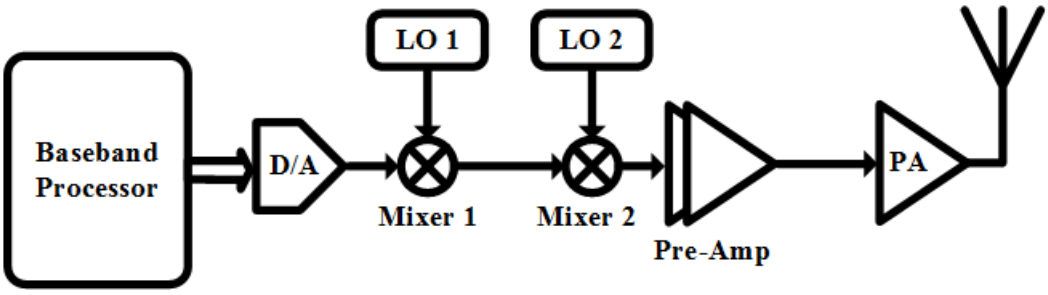


Figure 1.5: A Simplified Heterodyne Wireless Transmitter Architecture.

1.1.3 Power Amplifier Basics

In portable wireless devices, the power amplifier (PA) is a deciding factor for a battery run-time [2], [16]. A basic configuration of class A PA architecture is shown in Fig. 1.6. Here, the inductor choke is used to have a large headroom swing compared to a resistive loaded case. The load of the CMOS power amplifier needs to be a low impedance (in general, around 3-5 Ω) in order to provide the needed output power for a cellular transmission purpose while keeping the drain signal swing within the breakdown limit of the CMOS transistor [4]. However, in general, the load of antenna is 50 Ω. To solve this problem, a matching network is utilized here to provide a 50 Ω to a low impedance conversion as shown in Fig. 1.6. Here, Z_{IN} is the load to the power amplifier provided by the matching network. Various architectures of the matching network are reported in the literature based on the requirement of bandwidth, insertion loss, complexity, etc [17], [18].

Based on the gate bias condition of the common source transistor show in Fig. 1.6, it works as different classes of power amplifier. This is further discussed in the next chapter. In general, the power amplifier deals with the trade-off between linearity and efficiency [19]. In addition, the power amplifier's specifications include peak output power, efficiency, power gain, linearity, stability and power control [20]. For efficiency characterization, PAE (power added efficiency) and drain efficiency are important parameters to be measured. For a power amplifier, PAE is defined as 1.1.

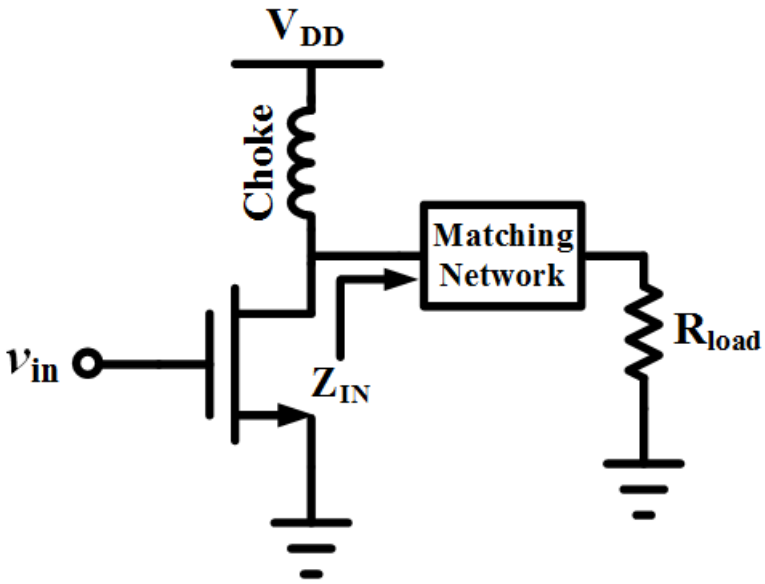


Figure 1.6: Class A Power Amplifier Architecture.

$$\eta_{PAE} = \frac{P_{RF\_OUT} - P_{RF\_IN}}{P_{DC}} \tag{1.1}$$

Here, P_{RF_OUT}, P_{RF_IN} and P_{DC} are the output power, input (gate) power consumption, and the DC power consumption of the power amplifier, respectively. For the drain efficiency, the governing equation is given by 1.2.

$$\eta_{DE} = \frac{P_{RF\_OUT}}{P_{DC}} \tag{1.2}$$

In addition, the peak efficiency of the power amplifier is defined as the efficiency of the power amplifier while transmitting peak power, and the average power efficiency is defined as the ratio of the average RF output power and average input supply power [16]. For PM/FM modulation, the signal's amplitude is constant, so the peak and average power efficiency are the same. However, for power control scenario, the peak power and average power efficiency are different for PM/FM modulation because of different signal amplitudes for both scenarios of peak and average power efficiency calculations [4]. Also, for AM modulation, the peak and average efficiency are different due to the envelope statistics and different output power levels [21]. In modern radios, a transmitter

power control is used in order to reduce the impact of the transmitter on nearby receivers. The power control scenario is described in Fig. 1.7. This shows that for a shorter distance between a transmitter and a base station, the transmitter delivers smaller output power to the base station comapred to that in case of a larger distance. This comes together with the issue of poor power efficiency of power amplifier for a shorter distance because the efficiency of power amplifier drops at back-off power levels [22]. In order to solve this issue, the average power tracking is used in literature [16].

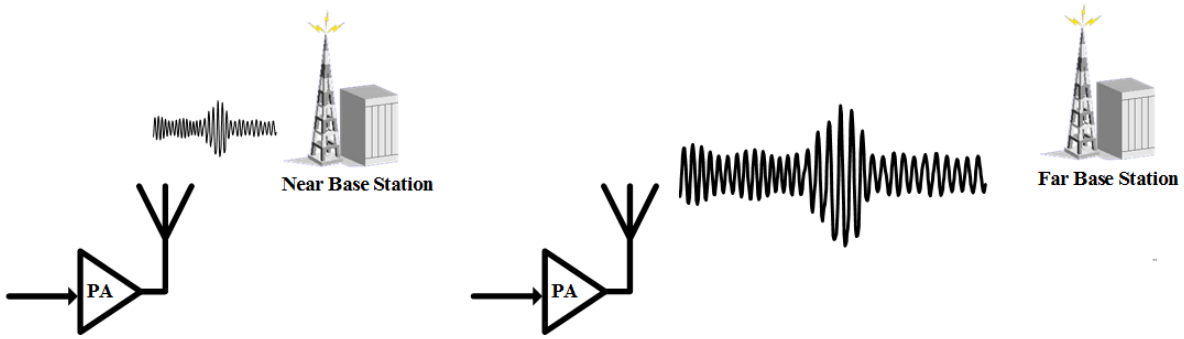


Figure 1.7: Power Control Scenario for a Power Amplifier.

Linearity of the power amplifier is one of the main performance challenges. The dominant sources of non-linearity in the power amplifier are AM-AM and AM-PM conversion [2]. Here, AM-AM non-linearity is dominated by transconductance's non-linearity of the power amplifier, and AM-PM conversion is dominated by non-linear output capacitor at the power amplifier [4]. In order to measure linearity of the power amplifier, ACPR (adjacent channel power ratio) and EVM (error vector magnitude) are used [4]. ACPR is defined as the ratio of the adjacent channel to the main channel power as shown in the Fig. 1.8. The EVM is defined as the ratio of rms (root mean square) magnitude of error voltage to the signal rms voltage as shown in 1.3. Here, V_{RMS} is rms of the signal, e_j is the magnitude of error signal vector as illustrated in Fig. 1.9, and N is the number of the test points.

$$EVM = \frac{1}{V_{RMS}} \sqrt{\frac{1}{N} \sum_{j=1}^{N} e_j^2} \tag{1.3}$$

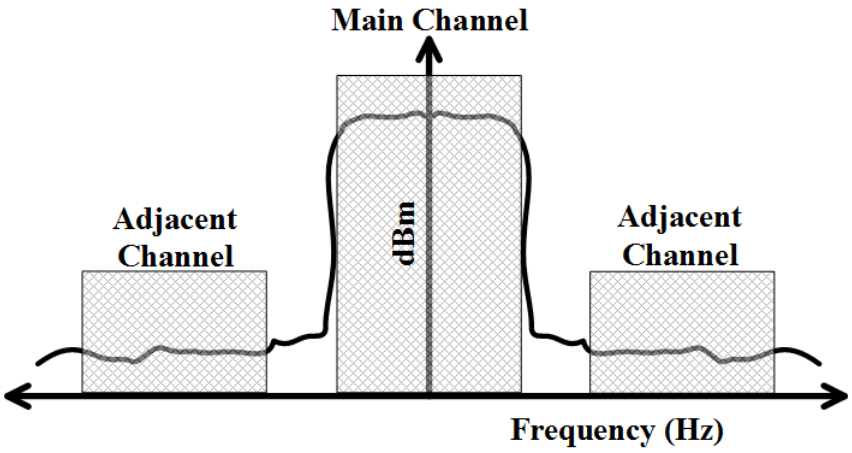


Figure 1.8: Adjacent Channel Power Ratio.

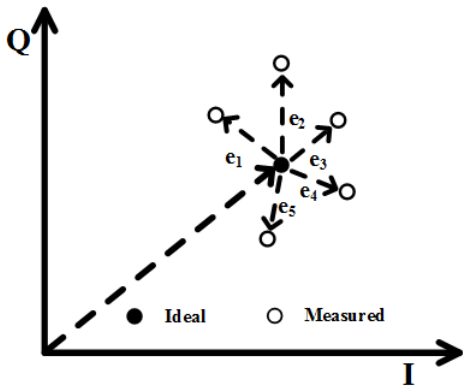


Figure 1.9: Error Vector Magnitude.

1.1.4 Dissertation Motivation and Goal

The motivation behind this work is to increase the power efficiency of the power amplifier. To achieve this goal, an envelope tracking technique is used for the linear power amplifier. However, an efficient envelope tracking is becoming more and more challenging with upcoming wireless standards. In this work, this challenge has worked as a motivation. The goal of this work is to have an efficient envelope tracking for the linear power amplifier that tracks fast moving envelope envelope signals for demanding wireless standards.

Along with this, an efficient variant in the power amplifier's architecture, digital polar power amplifier, was also under research. Besides being efficient, the digital polar power amplifier architecture is dealing with two main issues: spectral images and timing misalignment between amplitude and phase. The goal of this work was to solve these two bottlenecks in order to utilize the power efficient architecture.

With these goals, we hope to contribute towards enhancement in the power efficient wireless transmitter solution.

1.1.5 Dissertation Organization

This chapter provides a background on modern wireless communication trends, wireless transmitters, and power amplifier basics. We also established dissertation motivation and goal. The rest of the dissertation is organized in the following format:

Chapter 2- Overview of RF Power Amplifier

In this chapter, RF power amplifier and its classifications are presented. The chapter provides overview on class A, AB, B, C, D, E, and F power amplifier. Harmonics termination in matching network and voltage stress in linear power amplifier are also briefly discussed in this chapter.

Chapter 3- Linearization Techniques for Power Amplifiers

This chapters deals with the different linearization techniques to improve the linearity of a linear power amplifier. This include pre-distortion, feedforward linearization, envelope correction, and baseband I-Q feedback techniques. The chapter also briefly describes outphasing and envelope

elimination and restoration (EER) power amplifier architecture.

Chapter 4- Digital Polar Power Amplifier

Digital polar power amplifier along with its challenges related to spectral images and time misalignment between amplitude and phase signals are discussed here. An interpolation work for spectral image issue and a calibration scheme for the timing alignment issue are discussed in this chapter.

Chapter 5- An Agile Supply Modulator for Envelope Tracking Purpose

The proposed work for the envelope tracking technique is shown here. It also discusses various existing trade-offs in traditional envelope tracking solutions. Simulation as well as experimental results are discussed here.

Chapter 6- Conclusion

The summary of the dissertation is discussed in this chapter.

2.1 RF Power Amplifier and its Classification

The RF power amplifier is divided into several classes such as A, AB, B, C, D, E, F, etc. Classes A, AB, B, C are defined based on the conduction angle of the power amplifier. For classes D, E and F, the transistor of the power amplifier works as a switch.

2.1.1 Power Amplifier Classification Based on Conduction Angle

The conduction angle (Θ) of the transistor is defined as the fraction of time for which the transistor is ON (i.e., the gate voltage is greater than threshold voltage (V_{TH}) of the transistor) multiplied by $360°$, i.e., $360°\Delta T/T$. Here, ΔT is the time for which the transistor of the power amplifier is ON during signal time period (T). The generic configuration of the conduction angle based power amplifier classification is shown in Fig. 2.1. Here, the transistor works in the common source configuration.

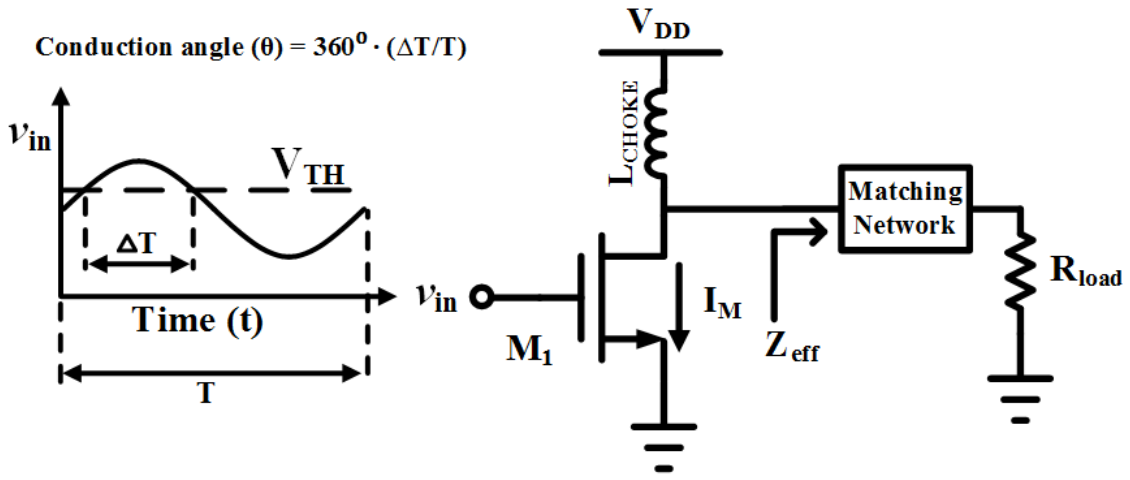


Figure 2.1: Conduction Angle based Power Amplifier Classification.

2.1.1.1 *Class A Power Amplifier*

For class A power amplifier, the conduction angle (Θ) of the transistor of the power amplifier is $360°$. The power amplifier's configuration and its ideal waveform are shown in Fig. 2.2. In this class, the gate voltage always needs to be greater than the threshold voltage V_{TH} of the transistor so that the transistor is always ON. The bias current is chosen such that it is greater than the peak ac current so that the transistor is always conducting. In order to calculate its maximum power efficiency, for simplification, let us assume that the load is resistive, i.e., R_{eff}. For the case of maximum efficiency, the drain voltage v_D reaches $2V_{DD}$ and 0. Thus, the output power to the matching network is given by $V_{DD}^2/2R_{eff}$. The power taken from the source V_{DD} is $V_{DD} \cdot I_B$, which is equal to V_{DD}^2/R_{eff} as $I_B = V_{DD}/R$. Hence, the maximum power efficiency of class A power amplifier is limited to 50% [4].

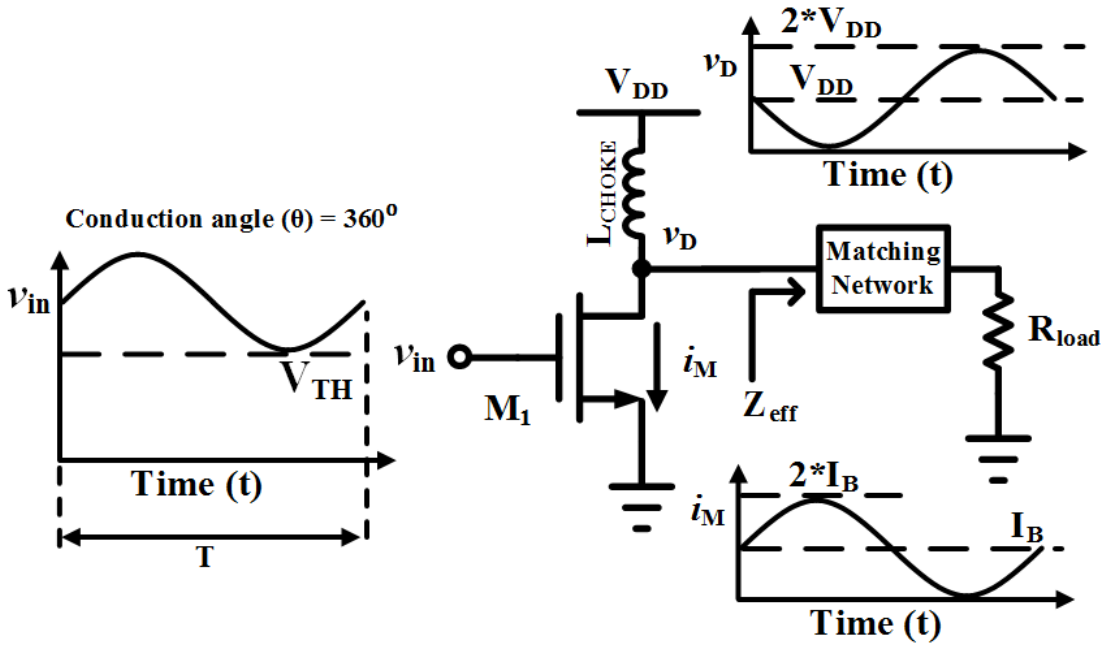


Figure 2.2: Class A Power Amplifier with ideal waveforms for maximum efficiency.

The calculation of the maximum power efficiency is done with the assumption that the tran-

sistor operates in a linear condition even with the drain voltage lesser than the overdrive voltage. However, this drastically impacts the linearity of the transistor [23]. In order to solve this problem, a voltage headroom needs to be provided for the transistor so that minimum drain voltage is greater than the overdrive voltage of the transistor. Depending upon the value of the provided voltage headroom, the power efficiency goes down as per 2.1 [4]. Furthermore, 50% of the maximum power efficiency also assumes that the matching network is lossless; however, practical matching network comes with additional insertion losses (IL). Due to the insertion loss, the power efficiency of the power amplifier decreases by the factor of $10^{(IL(dB)/10)}$. For example, 1 dB of insertion loss in a matching network decreases the power efficiency by the factor of 1.25. In addition, the assumption of $2 * V_{DD}$ voltage signal swing at the drain node of the transistor is not justified without knowing the breakdown voltage of the transistor. This is especially true for CMOS transistors where the advance technologies nodes come with lower and lower breakdown voltage.

$$\eta = \frac{1}{2}(1 - (V_{DSAT}/2V_{DD}))^2 \tag{2.1}$$

Considering, modern wireless standards where amplitude (envelope) of the signal is non-constant, especially for OFDM signal, the efficiency of the class-A amplifier suffers based on the statistical distribution of the envelope [16]. An example of varying envelope for RF modulated signal is shown in Fig. 2.3. Here, the power efficiency of the power amplifier is lower when the envelope signal is smaller compared to that in case of a larger envelope signal. Hence, the average power efficiency of the power amplifier suffers when the envelope signal is non-constant. For a non-constant envelope signal, four possible scenarios of the supply voltage and the bias current of the transistor can be evaluated. In first scenario, the supply voltage and bias current are kept constant. This is the classic class-A power amplifier. The output power for this case is ${V_{ENV}}^2/2R_{eff}$, where V_{ENV} is the enveloep of the drain voltage of the transistor. The input DC power is ${V_{DD}}^2/R_{eff}$. Hence, the power efficiency is given by 2.2.

$$\eta = \frac{V_{ENV}^2}{2V_{DD}^2} \tag{2.2}$$

In the second scenario, the supply voltage of the transistor changes as the envelope of the drain node voltage of the power amplifier; this approach is termed as an envelope tracking technique. Here, the output power remains the same like previous scenraio; however, the input DC power is $V_{ENV} * V_{DD}/R_{eff}$. The power efficiency of this scenario is given by 2.3 [4]. This technique is discussed in details in the chapter 5.

$$\eta = \frac{V_{ENV}^2/2R_{eff}}{V_{ENV} * V_{DD}/R_{eff}} = \frac{V_{ENV}}{2V_{DD}} \tag{2.3}$$

In the third scenario, the bias current of the transistor in the power amplifier changes as per the output envelope signal. For low output envelope signal, the bias current is reduced; for high output envelope signal, the bias current is increased. It can be shown that the power efficiency for this case is also given by 2.3 [19]. This is the fundamental concept behind digital polar power amplifier, which is discussed in the chapter 4. The fourth scenario is the combination of the second and third scenarios. In this, the supply voltage as well as the bias current are adapted as per the output envelope signal. The power efficiency for this scenrio is 50% [4]. These techniques help to improve the power efficiency of class-A amplifier for varying envelope signal. However, all these approach comes with higher complexities [20].

The Power capacity (PC) metric for the power amplifier is used for the quantification of the relative stress on the device in a power amplifier[24]. This is the ratio of maximum output power to the product of peak voltage and peak current applied on the device in the power amplifier. A higher PC metric shows a lower stress on the device compared to the power amplifier with the lower metric for the given output power. The power capacity is given by 2.6.

$$PC = \frac{P_{OUT,max}}{V_{max} \cdot I_{max}} \tag{2.4}$$

For class-A power amplifier's configuration shown in Fig. 2.2.,

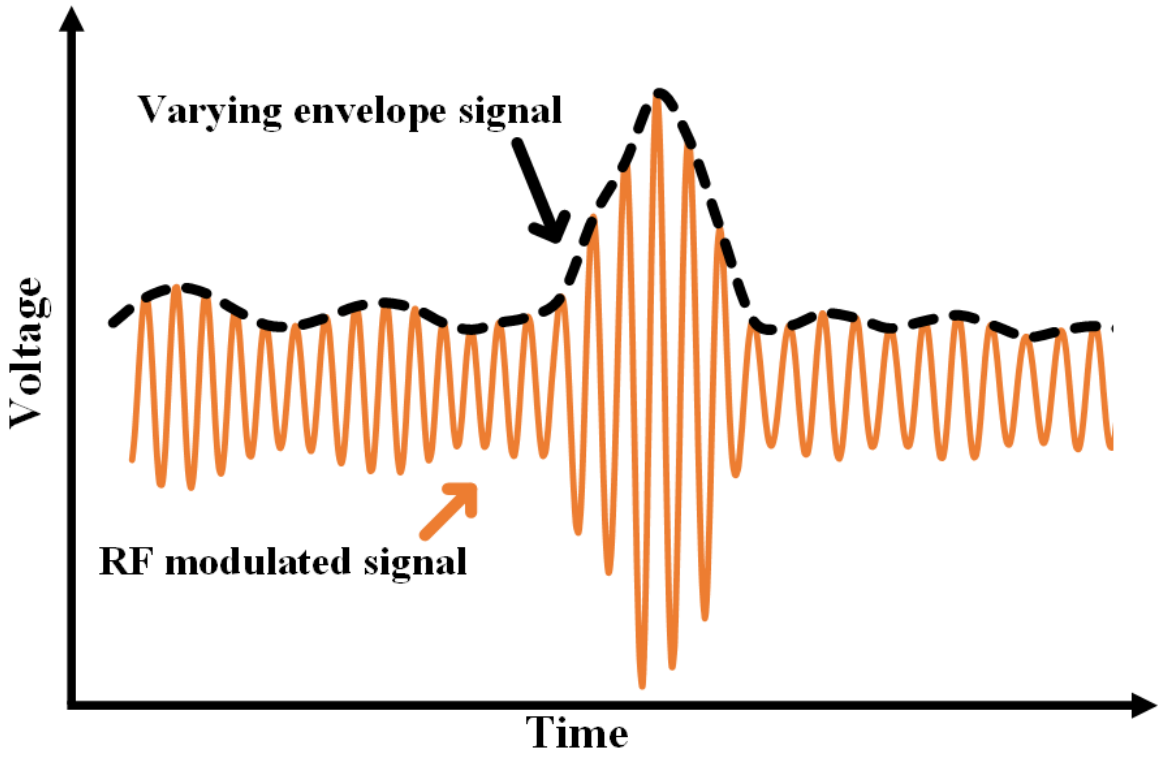


Figure 2.3: Varying Envelope Signal.

$$P_{OUT,max} = \frac{1}{2} V_{DD} \cdot I_B$$

$$V_{max} = 2 \cdot V_{DD}$$

$$I_{max} = 2 \cdot I_B$$

Hence, the power capacity for the class-A power amplifier is given by 2.5.

$$PC = \frac{\frac{1}{2} V_{DD} \cdot I_B}{2 \cdot V_{DD} \cdot 2 \cdot I_B} \tag{2.5}$$

This is equal to 1/8=0.125. Hence, the power capacity of the class A power amplifier is limited to 0.125.

2.1.1.2 Class AB, B and C Power Amplifier

The Table 2.1 shows the correlation between conduction angle and the classes of power amplifier.

Conduction Angle (Θ)	Power Amplifier Class
$\Theta = 360°$	A
$360° > \Theta > 180°$	AB
$\Theta = 180°$	B
$\Theta < 180°$	C

Table 2.1: Conduction Angle and Classes of Power Amplifier.

For these classes, it is important to see the trend of the power efficiency versus the conduction angle. For this, the circuit shown in the Fig. 2.4 is considered. Here, V_B biases the transistor of the power amplifier. In this, the voltage applied at the gate of the transistor is $v_{in} + V_B$. Assuming current through the choke is I_{DC}, and the current to the matching network is i_{sig}, then voltage at the drain of the transistor is $V_{DD} + i_{sig}Z_{eff}$. Similarly, the current through the transistor is $I_{DC} - i_{sig}$. Here, the conduction angle (θ) is governed by v_{in} and V_B. For the given amplitude of input signal v_{in}, V_B controls the classification of the power amplifier.

As shown in the Fig. 2.5, the gate voltage above the threshold voltage of the transistor decides the conduction angle (θ). As the conduction angle decreases, the drain current also decreases. Hence, the output power of the power amplifier decreases with the decrement in the conduction angle. This can be shown that the output power is proportional to $(\Theta - \sin(\Theta))/\sin^2\Theta/4$ [4]. The output power versus conduction angle is tabulated in Table 2.2. It can be also shown that the efficiency (η) is given by 2.6 [4].

$$\eta = \frac{1}{4}\frac{\Theta - \sin(\Theta)}{\sin(\frac{\Theta}{2}) - (\frac{\Theta}{2})\cos(\frac{\Theta}{2})} \tag{2.6}$$

The maximum power efficiency (η) increases with the decrement in the conduction angle as

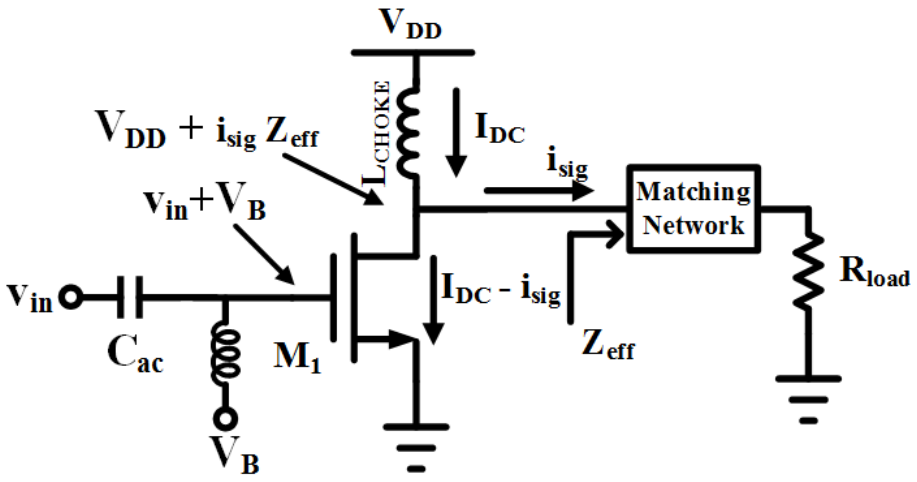


Figure 2.4: Circuit for the Generic Analysis of Power Amplifier Classification with Conduction Angle.

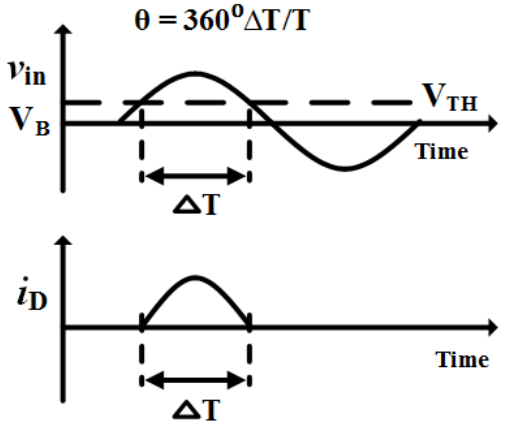


Figure 2.5: Input Gate Voltage and Drain Current.

Conduction Angle (Θ)	Maximum Output Power
$\Theta = 360°$	100%
$\Theta = 180°$	68.15%
$\Theta = 90°$	62%

Table 2.2: Conduction Angle and Output Power of Power Amplifier.

shown in Table 2.3.

Conduction Angle (Θ)	Maximum Power Efficiency (η)
$\Theta = 360^\circ$	50%
$\Theta = 180^\circ$	78.5%
$\Theta = 90^\circ$	93.71%

Table 2.3: Conduction Angle and Maximum Efficiency of Power Amplifier.

However, increment in the power efficiency comes with the decrement in the maximum output power of the power amplifier. To have the same maximum output power of the class A power amplifier, i.e., conduction angle $= 360^\circ$, the transistor in the low conduction angle configuration of the power amplifier, e.g., class C, needs to be far wider in size. Hence, high efficiency configuration of the power amplifier at the same output power comes with the cost of wider transistor size.

2.1.1.3 Voltage Stress Solution for Linear Power Amplifier

In case of class-A power amplifier, the output voltage at the drain node of the transistor reaches $2 \cdot V_{DD}$ in order to maximize its power efficiency. However, it creates a voltage stress on the transistor of the power amplifier. One way to solve this problem is to use the supply voltage at half of the breakdown limit of the transistor. However, it reduces the output voltage swing at the drain of the the transistor, hence the output power.

A cascode configuration can be used in order to reduce the voltage stress on the RF transistor of the power amplifier. The configuration of the stage is shown in Fig. 2.6. In this case, a thick device is shown at the top transistor in the cascode stage.

In order to protect the bottom transistor (M1) from voltage stress, the top transistor (M2) needs to work in the saturation region. Considering the saturation condition for both of the transistors, it can be shown that the output voltage swing improves slightly but at the cost of linearity and power efficiency [4]. In addition, the cascode stage comes with the benefit of reverse isolation, which provides more stability to the power amplifier [25].

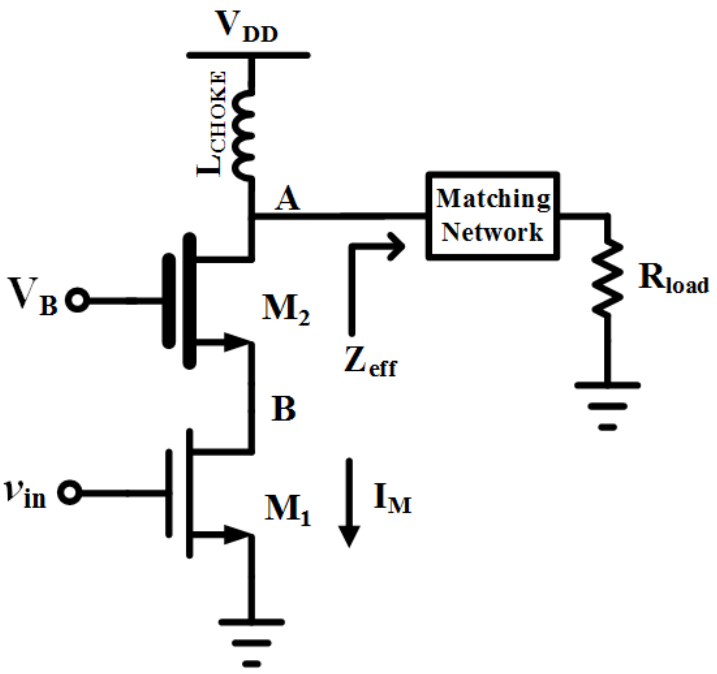


Figure 2.6: Cascode Stage in Power Amplifier to Reduce the Voltage Stress.

2.1.1.4 Harmonics In Power Amplifiers

In order to improve the power efficiency of a power amplifier, harmonics exploitation can be done [26]. The basic idea is to reduce the overlapping of drain voltage and its current, which leads to lesser power consumption in the transistor of the power amplifier, hence higher power efficiency. For this, the output matching network can be used to proivde harmonics termination [27]. For practical purposes, a load-pull simulation is one of the ways to decide which harmonics configuration provides power efficiency enhancement.

However, such a technique comes with a larger order output matching network, which eventually comes together with a higher insertion loss. In practice, such harmonics enhancement is done for one harmonics only (either second or third order harmonics) as the matching network becomes complicated and impractical with multi-harmonics enhancement.

2.1.2 Switching Class of Power Amplifier

In this category of the power amplifier, the transistor of the power amplfieir works as a switch [28]. In this subsection, we will overview D, E and F power amplifier classes, which are switching power amplifier.

2.1.2.1 Class D Power Amplifier

The configuration of class-D power amplifier is shown in Fig. 2.7. In this configuration of

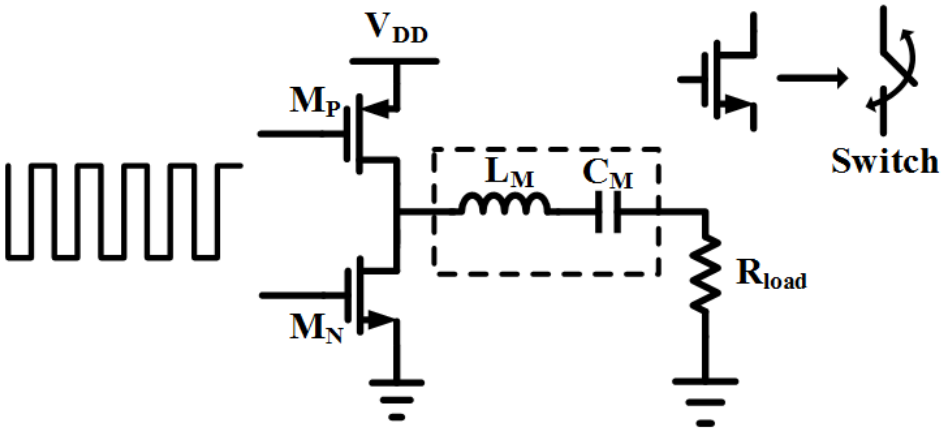


Figure 2.7: class-D Power Amplifier.

the power amplifier, both NMOS and PMOS transistors work as a switch [29]. Here, the input to the switches contains phase information. Based on the phase information, the duty cycle of the switches is decided [30]. In order to only pass fundamental components from the rectangular pulses, a series LC filter is used here. It passes first harmonic and suppresses higher harmonics. A higher order filter can also be implemented here to suppress higher order harmonics more than the shown second order filter. However, it comes together with additional insertion losses. Considering ideal switches in the class-D power amplifier, there is no overlap between voltage and current in the switches as shown in the Fig. 2.8. It means when the current is flowing through the switch, the voltage across it is zero. Also, when the voltage exists across the switch, it carries no current.

Hence, The multiplication of current and voltage across the switch is zero, i.e., there is no losses in the switches [31].

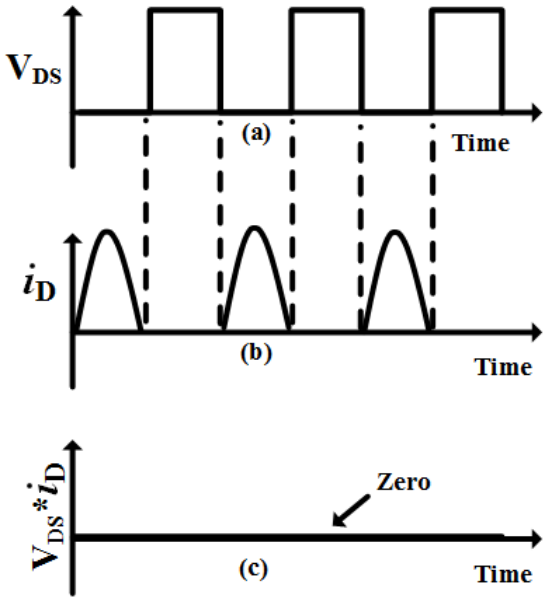


Figure 2.8: Voltage and Current Waveform and its Multiplication Across the Switch in Class-D Power Amplifier.

However, due to non-idealities of the switches, there is overlap between voltage across the switch and the current through the switch [24]. This leads to a decrease in the power efficiency of the class-D power amplifier. The waveforms of the voltage across the switch and current through the switch in the case of switch with constant resistance is shown in Fig. 2.9. As shown in Fig. 2.9c, the product of voltage across the switch and the switch current is non-zero, which represents the power loss in the switch. Also, it is important to note that for this case, when the switch is off the V_{DS} will not be fixed; however, for simplicity, it is shown as a fixed value in Fig. 2.9. In addition, there is a loss of the power efficiency due to power at other harmonics after filtering in the class-D power amplifier as only fundamental harmonic component at the output needs to be considered for the output power in the power efficiency calculation.

The resistance of the switch can be decreased by increasing the size of the switch, but it comes

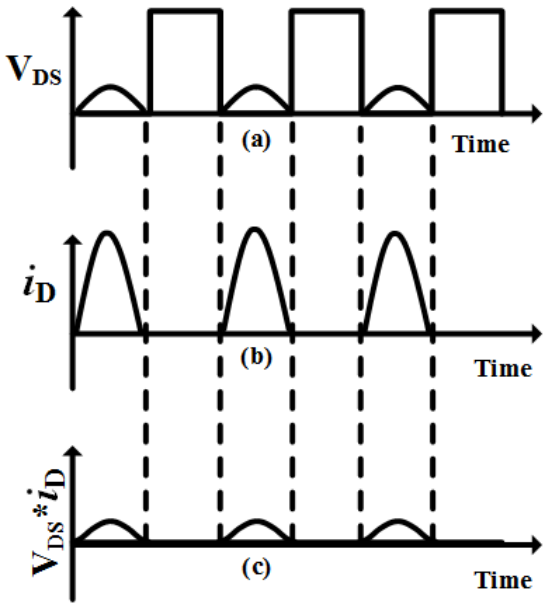


Figure 2.9: Voltage and Current Waveform and its Multiplication Across the Switch with Switch Resistance in Class-D Power Amplifier.

with a larger gate capacitance, which increases the driver loss hence lower the power efficiency of the power amplifier. It also comes with a larger parasitic substrate losses.

Besides shown architecture of class-D power amplifier in Fig. 2.7, there is a differential architecture for the same [24]. It removes the need of PMOS switch, which improves the driver efficiency [4]. Also, it comes with better common-mode rejection and lesser impact of bond-wire inductor on the power amplifier's performance. The drawback of this architecture is the addition of balun, which causes insertion loss. The power capacity of class-D architecture is much better than the class A [24].

2.1.2.2 Class E Power Amplifier

The class E power amplifier is also a switching power amplifier [32]. A generic architecture of the class E switching amplifier is shown in Fig. 2.10 [33]. In order to have high efficiency, the class E transistor should have small voltage across the switch when it passes current. The switch should also carry a small current when it has voltage across it. In addition, the transition time between switch on and off needs to be minimized [4].

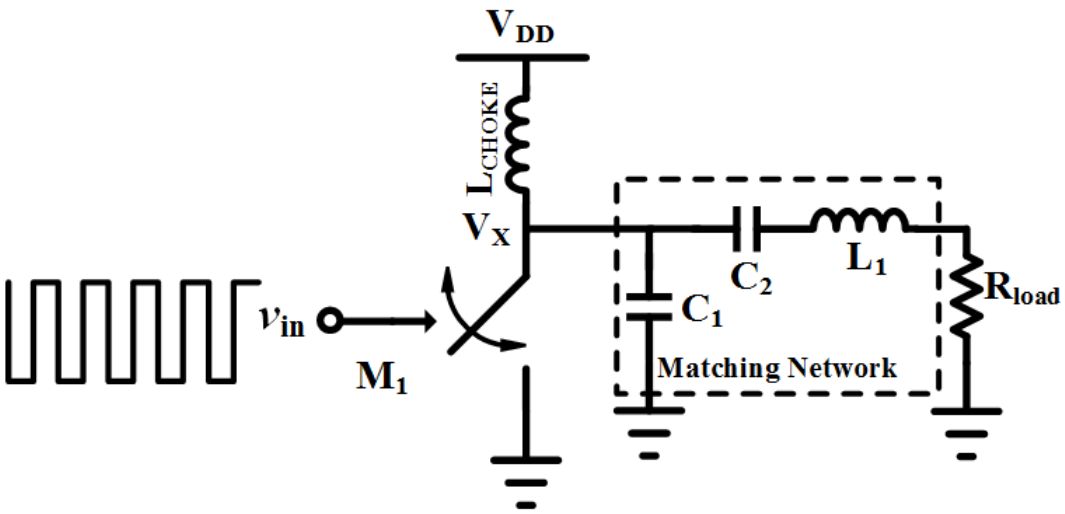


Figure 2.10: Class-E Power Amplifier.

Here, the matching network provides the needed wave shaping for high power efficiency [2]. Compared to the linear power amplifier, where the requirement for the transistor is to work as a current source, the class-E transistor drain voltage and gate voltage need to be controlled accordingly. In this case of class-E power amplifier, these constrains are not present,so the drain voltage (also the gate voltage) can even reach ground. Here, the components of the matching network (C_1, C_2 and L_1) need to be chosen such that Vx satisfy condition for high power efficiency [34]. This is basically the condition for a robust zero-voltage switching such that there is no loss in the switch while switching [32].

Considering the switch resistance R_S and its parasitic capacitance C_S, the drain efficiency of the class E can be shown as 2.7 [35].

$$\eta = \frac{(\pi/2 + w_C C_S R_S)^2 + 1}{(1 + \pi^2/4)(1 + \pi w_C C_S R_S)^2} \tag{2.7}$$

Where, w_C, R_S, and C_S are frequency of switching, switch resistance, and switch capacitance, respectively. As shown in the table 2.4, the efficiency decreases drastically with the increment in $w_C R_S C_S$. Hence, this combination needs to be minimized for a highly efficient class-E amplifier.

$w_C R_S C_S$	Power Efficiency
0.01	94.7%
0.05	78%
0.1	63%
0.2	45%

Table 2.4: Class E Power Efficiency Vs. $w_C R_S C_S$.

The issue with this architecture of the switching amplifier is the large voltage across the switch during turn-off time [32]. It is around 3.5 times V_{DD}, which makes a serious case for reliability. For example, with supply of 1.5 V, the peak voltage across the switch is around 5.25 V. The non-linearity of the switch capacitance is another issue with class-E power amplifeir as the non-linear capacitance distorts the voltage waveform at V_X, which has a direct impact on its performance [2].

2.1.2.3 Class F Power Amplifier

Class F power amplifier is switching amplifier along with harmonic terminations [36]. The requirement of non-overlap condition for switch current and voltage remains the same as other discussed switching amplifiers for high power efficiency. In this work, the non-overlapping is achieved by harmonic terminations. The harmonics termination provides here high impedance to odd harmonics signal in order to make it close to square wave signal from sinusoidal signal [4]. As shown in Fig. 2.11, L_1 and C_1 are used here to provide high impedance at third harmonics, and L_2 and C_2 are used to provide high impedance at fifth harmonics. In practice, due to insertion losses of matching network, only one harmonic termination is used in a class-F power amplifier.

The waveform at V_X is shown here in Fig. 2.12 with multi-harmonics termination. As depicted in the figure, multi-harmonics helps to turn sinusoidal wave to nearly square wave. However, it comes with the needs of a fast-hard-switching of the class-F transistor at RF frequency. This is a difficult task to achieve at RF frequency. This has direct impact on the waveform at V_X, hence power efficiency [37].

As all discussed switching amplifiers only process phase information, these architecture of power amplifier cannot be used with wireless standard with amplitude modulation. This restricts

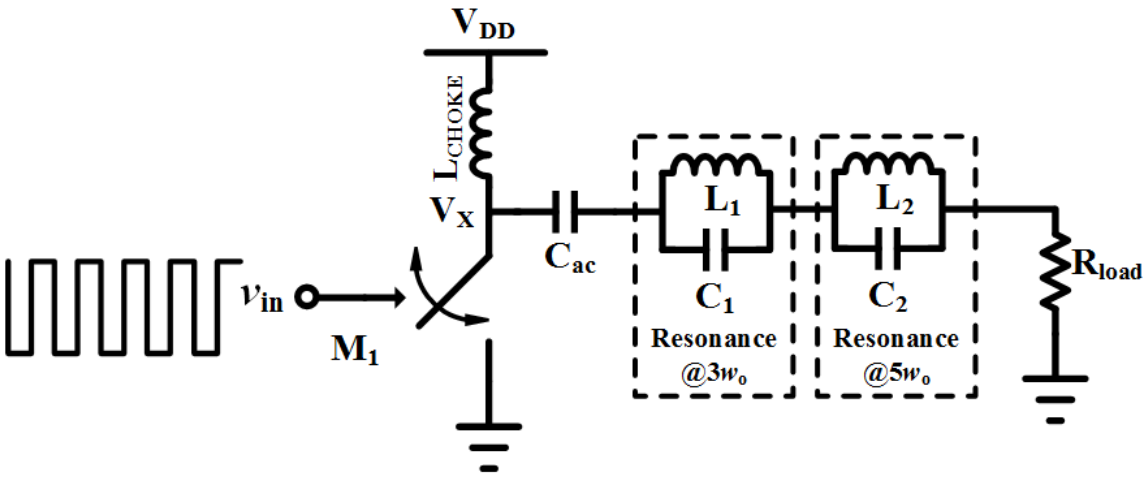


Figure 2.11: Class-F Power Amplifier.

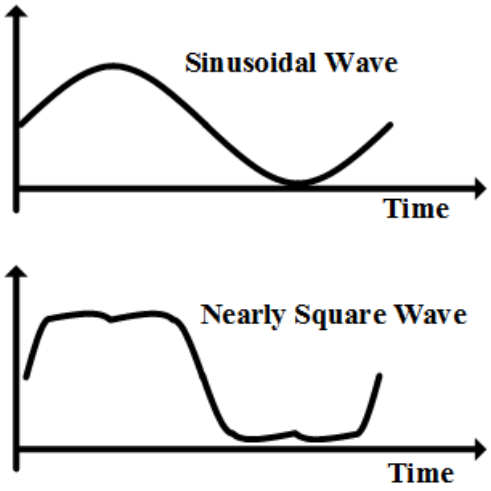


Figure 2.12: Waveform at V_X with Multi-Harmonics Termination.

its usage in all upcoming wireless standards with amplitude and phase modulations.

3. LINEARIZATION TECHNIQUES FOR POWER AMPLIFIERS

First, this chapter deals with basic linearization techniques for power amplifier. These techniques aimed for a linear power amplifier. These linearization techniques include pre-distortion, feedforward, envelope correction and baseband I-Q feedback. Second, the chapter describes power amplifier architectures that linearizes switching power amplifier in order to use with ongoing wireless standards. This includes outphasing and envelope elimination and restoration (EER) power amplifier architecture.

3.1 Basic Linearization Techniques for Linear Power Amplifier

3.1.1 Pre-Distortion

This is the most famous linearization technique used in industry [38]. The basic idea of this linearization technique is to first find the input-output function of the system under test, and then use its inverse function to linearize it [39]. The basic flow of the pre-distortion is shown in Fig. 3.1. Here, f(x) is the function that is subjected to linearize. For the purpose of linearization, the inverse function of f(x), $f^{-1}(x)$, is added in front of the f(x).

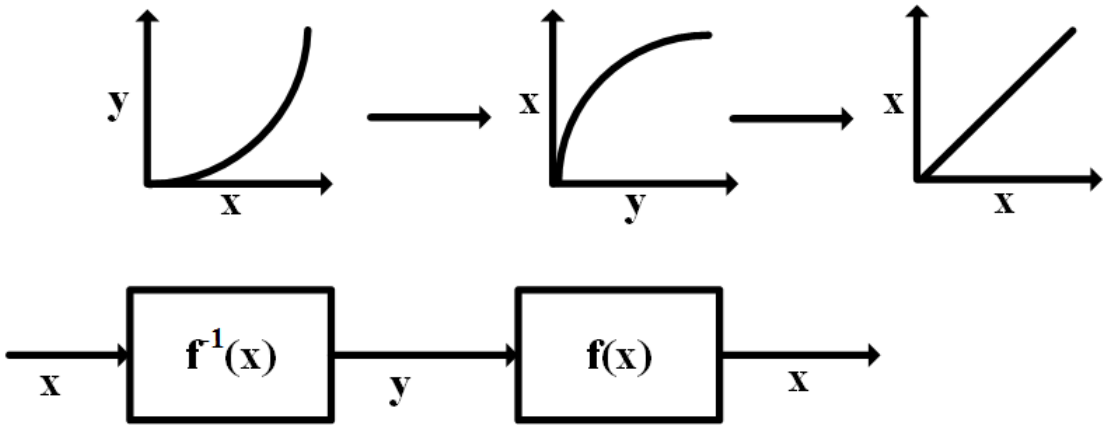


Figure 3.1: Predistortion Linearization Technique.

The same flow is used for the linearization of the power amplifier. In this technique, first the power amplifier needs to be characterized, and then its inverse function is applied at its input as shown in Fig. 3.2. Several approaches are reported in literature to find the inverse function of the power amplifier [40], [41]. The predistortion can be done digitally on baseband information in the bandband processor itself. There are two main approaches for the digital pre-distortion: look-up table and polynomial based predistortion [42], [43]. Besides a better performance than the latter, the former technique suffers from large memory need and slow convergence speed [44]. In order to track changes in the characterization of the power amplifier over PVT, a feedback loop can be added here to modify coefficient of predistortion polynomial [38].

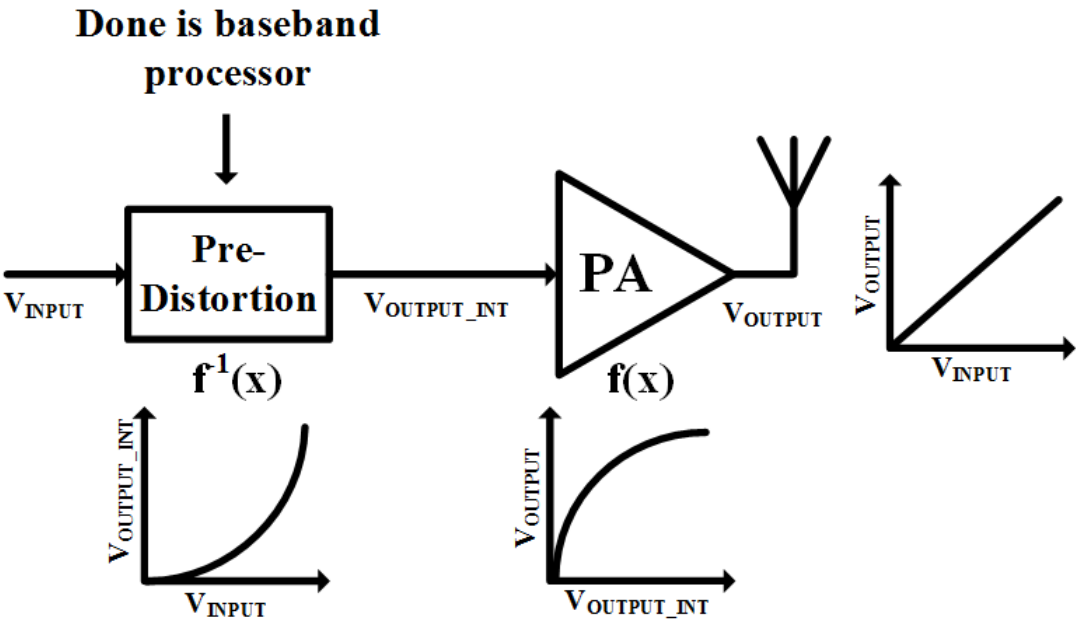


Figure 3.2: Predistortion Technique for Power Amplifier.

Mostly, the characterization of the power amplifier is done for static non-linearities, a simple look-up table based pre-distortion technique is not enabled to handle dynamic non-linearities such as memory effect [42]. A memory based polynomial model is proposed in [44] to handle memory effect in the polynomial based pre-distortion scheme. The cost of correcting PA's strong non-

linearities could be high as it demands higher order polynomial in the predistotion scheme [4].

3.1.2 Feedforward Linearization Technique

In this linearization technique, a feedforward path is used in order to linearize the power amplifier [45], [46]. Here, we subtract the non-linear component of the power amplifier response at the output in order to linearize the power amplifier. A basic approach of this linearization technique is shown in Fig. 3.3 [4]. Here, NL is the non-linear component in the output response of the power amplifier, which is also generated in the feedforward path.

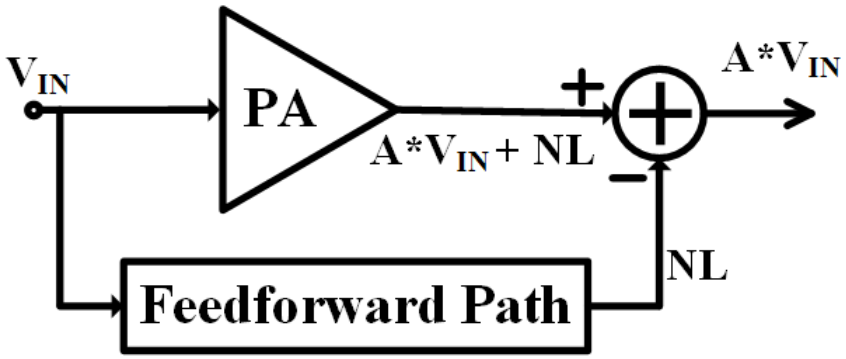


Figure 3.3: Feedforward Technique for Power Amplifier.

The generation of the non-linear component of the power amplifier's response can be done in several ways [47], [48]. For example, the output of the power amplifier can be subtracted from the ideal output, $(A * V_{IN})$, in order to generate the non-linear component. However, the generation of ideal output can be difficult considering that it is a large signal. Another way to generate the non-linear component is to reduce the output of the power amplifier by its ideal gain, then subtract it from the input signal, V_{IN}, followed by the amplification with gain "A" [49], [50]. In compared to previous approach, the latter approach is easier because it processes (NL/A), which is small signal. For a small input signal, getting an ideal gain is easier than than in case of a large input signal. The generation of NL is shown in Fig. 3.4 [24].

However, the latter approach of generation of NL comes with the overhead of generating gain

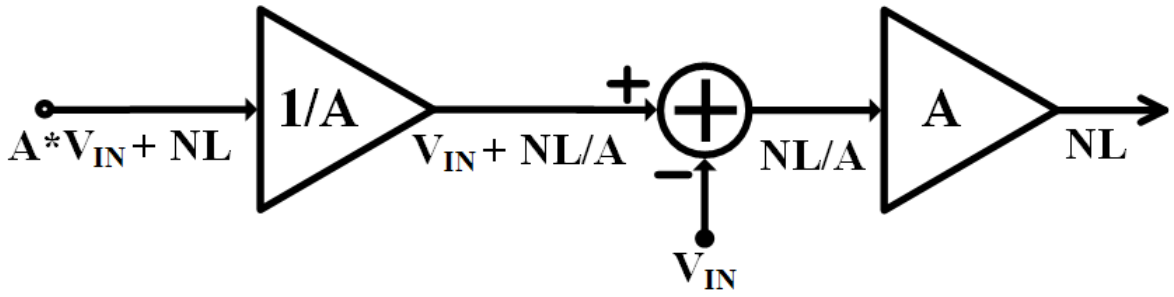


Figure 3.4: Generation of NL for Feedforward Technique.

of (1/A), a subtractor, and another gain block (A). The frequency dependency of these elements puts a serious challenge to this linearization technique [51]. Besides this, the timing mismatch between the two paths (main path and feedforward path) can nullify the benefit of this technique. In addition, the mismatch can add further distortion at the output [51]. In order to solve this problem a timing characterization is needed, which puts additional delay in the main path in order to equate the delays for both of the paths. Considering frequency dependency of these delays, this problem becomes difficult to solve. Furthermore, adding any delay element in the main paths comes with additional losses and distortions [52]. Besides the delay mismatch, the gain mismatch between the two paths is also a bottleneck of this technique. In order to correct this, the gain characterization is needed for both of the paths [53]. Also, having a subtractor at the output as shown in Fig. 3.3 degrades efficiency and increases the complexity of the linearization technique.

To further improve the benefits of the feedforward linearization technique, multi-loops are also used [4]; however, it adds further complexities to the solution. Overall, the feedforward technique is an easy mathematical solution; however, its implementation comes with several issues like delay mismatch, additional complexity of addenda, which make this technique less attractive.

3.1.3 Envelope Correction Technique

This linearization technique is used to only correct AM/AM nonlinearity [54]. In this technique, the envelope of the power amplifier's input and the scaled envelope of the power amplifier's output are compared and provide feedback to the power amplifier in order to equate the output

envelope signal to the input envelope signal [55]. The block diagram of the linearization technique is shown in Fig. 3.5. As shown, there is a feedback path from the output of the power amplifier followed by an attenuator. The gain of the attenuator needs to be equal to the inverse of the desired gain of the power amplifier. Based on the inputs from two envelope detectors, the bias control changes the bias setting of power amplifier in order to meet the required envelop gain [56]. The stability analysis of this feedback system is described in [57].

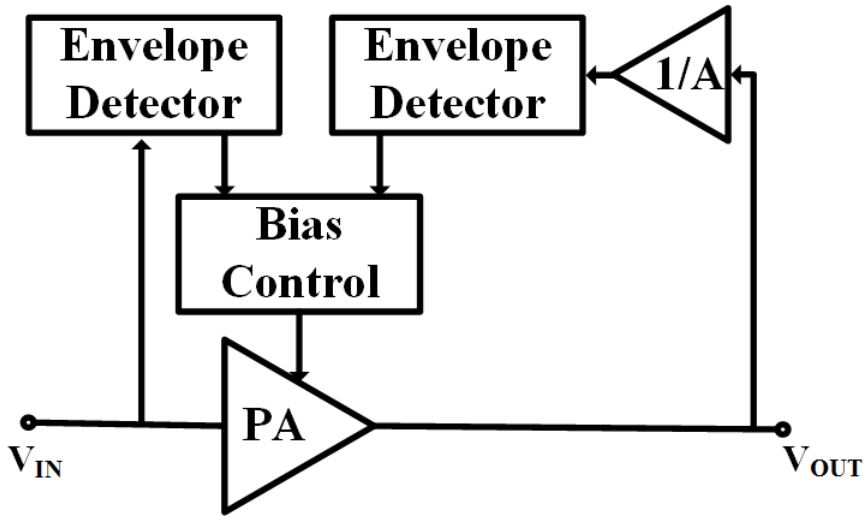


Figure 3.5: Envelope Correction Technique.

Here, the envelope detector can be implemented with the system shown in Fig. 3.6 [4]. In this, a mixer is used to do multiplication of amplitude and phase modulated RF signal with constant amplitude-phase modulated RF signal. The output of the mixer is shown in 3.1. Here, k is the conversion gain of the mixer.

$$k \cdot V_{ENV} sin(\omega t + \Theta(t)) \cdot V_{LIM} sin(\omega t + \Theta(t)) \tag{3.1}$$

$$\frac{1}{2} \cdot k \cdot V_{ENV} \cdot V_{LIM}[1 - cos(2 \cdot (\omega t + \Theta(t))] \tag{3.2}$$

The equation 3.1 can also be written as 3.2. The output of the mixer is processed with a low

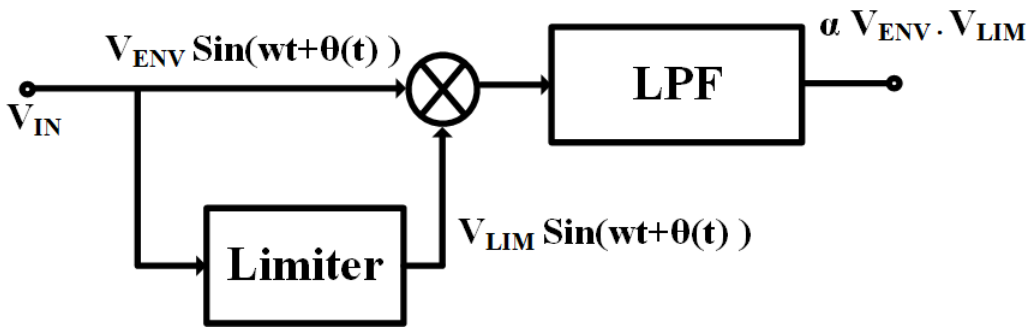


Figure 3.6: Envelope Detector.

pass filter to remove high frequency component, $cos(2 \cdot (\omega t + \Theta(t))$. The output of the low pass filter is $\frac{1}{2} \cdot k \cdot V_{ENV} \cdot V_{LIM}$, which is proportional to V_{ENV}. The main issue of this linearization technique is its inability to linearize AM-PM non-linearities.

3.1.4 Baseband I-Q Feedback Technique

In this baseband I-Q feedback linearization technique (also know as Cartesian feedback), feedback loops are used for baseband signals, I and Q, in order to linearize the power amplifier [58], [59], [60]. Here, the non-linearity of the power amplifier is reduced based upon loop gain [23]. The I-Q feedback loops are shown in the Fig. 3.7 [4]. In this, the baseband signals (I' and Q') are retrieved from the output of the power amplifier and feed to the loop in order to equate to the input baseband signal (I and Q) [61]. For this, the output of the power amplifier is passed to an attenuator, which has inverse of the expected PA gain, followed by a down-converter mixer. After this, the baseband information is extracted from a low pass filter as shown in the Fig. 3.7. Here, the linearity of addenda (attenuator, down-converter, low pass filter) needs to be sufficiently higher compared to the linearity of the power amplifier [62]. In this linearization technique, the envelope information needs to be preserved at the output of the power amplifier for the feedback loop to work. Hence, this technique is only utilized for a linear power amplifier. It is important to note that this linearization technique can linearize of whole transmitter chain [63], [64].

The stability of the feedback loop is a concern of this technique [58]. A phase shift $\Delta\Theta$ is generally used here in order to provide stability to the loop [65], [66]. However, PVT variations

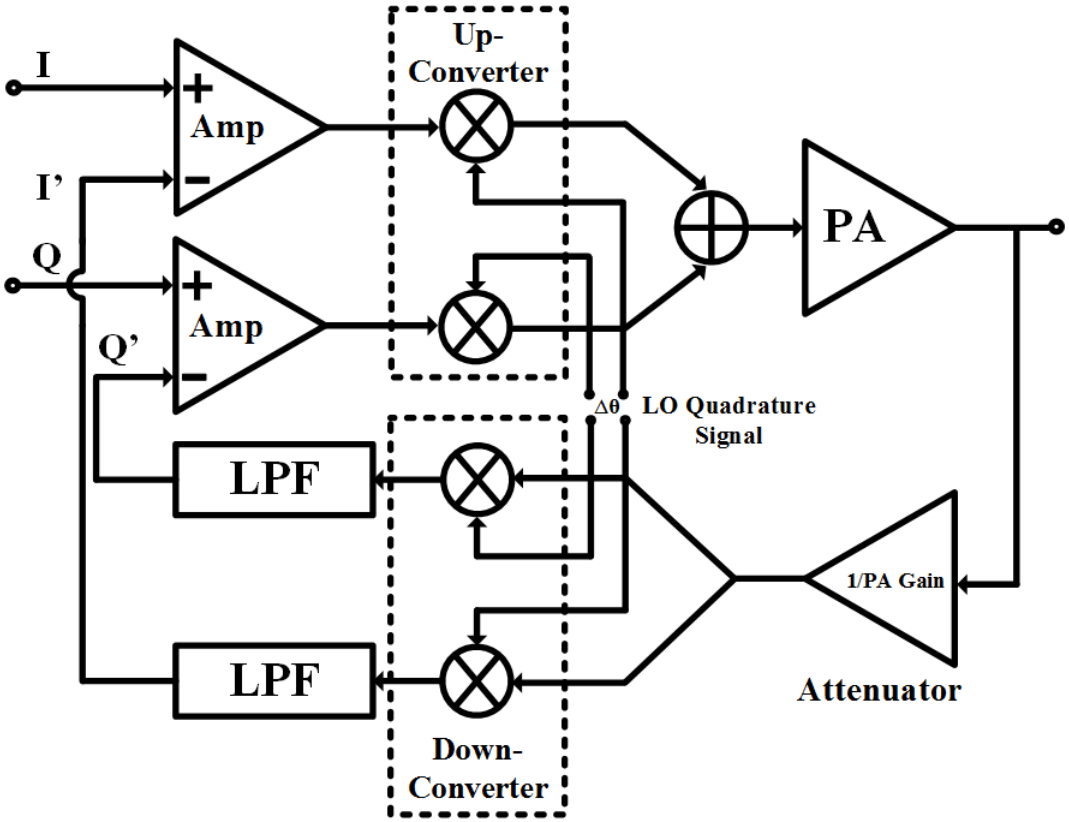


Figure 3.7: Baseband I-Q Linearization Technique.

become problematic in the selection of the phase shift [67]. Also, the loop needs to be fast enough, which is challenging for high bandwidth wireless standards [68].

3.2 Linearization of Switching Power Amplifier

As the switching power amplifier cannot be used for amplitude modulated signal, this reduces its importance for ongoing and upcoming wireless standards which are amplitude as well as phase modulated [69]. Outphasing or LINC (linear amplification using non-linear components) power amplifier and EER (envelope elimination and restoration) power amplifier are two architectures of power amplifier that linearizes the switching power amplifiers so that it can be used with amplitude and phase modulated signals [70], [71].

3.2.1 Outphasing Power Amplifier

The outphasing power amplifier (also called LINC, linear amplification with non-linear components) based on the idea of splitting the amplitude and phase modulated signal into phase modulated signals that can be directly processed in highly efficient switching power amplifiers [72]-[75]. The outputs of switching power amplifiers are combined in order to get amplitude and phase modulated signal. The architecture of the outphasing power amplifier is also shown in Fig. 3.8 [76], [77].

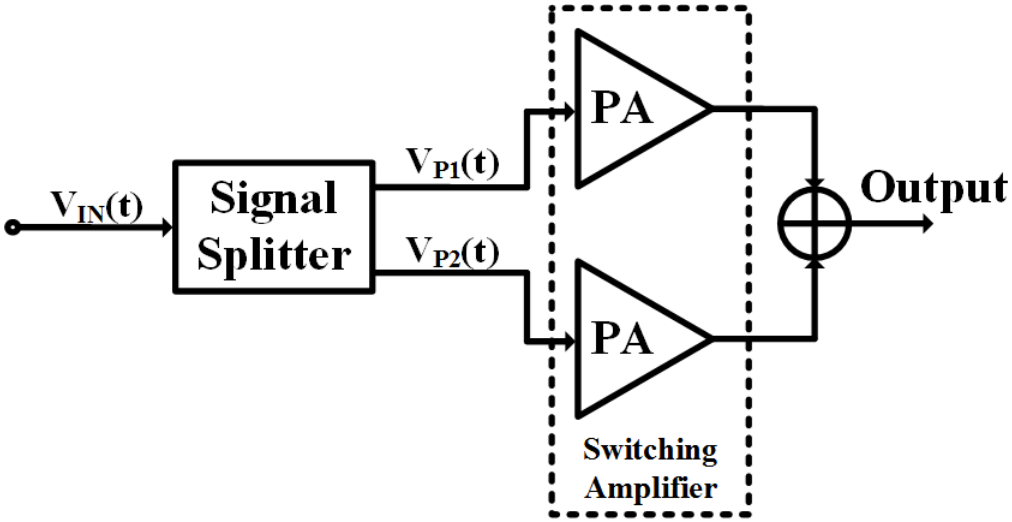


Figure 3.8: Outphasing Power Amplifier.

The process of this splitting is shown in 3.3. As shown, the amplitude and phase modulated signal, $V_{IN}(t)$, splits into $V_{P1}(t)$ and $V_{P2}(t)$, which are phase modulated signals with constant amplitude ($V_A/2$). Here, V_{ENV} and $\Theta(t)$ represent amplitude modulation and phase modulation in the signal $V_{IN}(t)$, respectively.

$$
\begin{aligned}
V_{IN}(t) = V_{ENV}(t)sin(\omega t + \Theta(t)) = V_{P1}(t) + V_{P2}(t) \\
V_{P1}(t) = \frac{V_A}{2}cos[\omega t + \Theta(t) - \phi(t)] \\
V_{P2}(t) = -\frac{V_A}{2}cos[\omega t + \Theta(t) + \phi(t)] \\
\phi(t) = sin^{-1}(\frac{V_{ENV}}{V_A})
\end{aligned}
\tag{3.3}
$$

In the outphasing power amplifier, the summation of the outputs of the switching power amplifiers is done with a power combiner; however, it comes with additional power losses [78], [79]. Besides this, the outphasing power amplifier suffers from three main disadvantages. First, interaction of two switching power amplifiers at the output is one of the major disadvantages of this power amplifier, which leads to spectral regrowth and output signal corruption [4]. To solve this problem, an isolation is needed so that impact of the switching power amplifiers on each other can be minimized [76]. For this purpose, Chireix technique is favored in the literature [80], [81], [82]. The second disadvantage is phase and gain mismatches between two parallel paths, which results in spectral regrowth at the output [83]-[85]. A pre-distortion based calibration technique is used in literature in order to calibrate these mismatches [86]. Third is larger bandwidth of $V_{P1}(t)$ and $V_{P2}(t)$ compared to the composite signal, $V_{IN}(t)$, which increases the processing bandwidth needs in the two parallel paths, hence higher power consumption [4], [87].

In all, the implementation of signal splitter (conditioning) at input, the power loss in the power combiner at the output, and discussed three disadvantages are major bottlenecks in the outphasing power amplifier's implementation [4].

3.2.2 Envelope Elimination and Restoration Power Amplifier

The EER (envelope elimination and restoration) or analog polar power amplifier is one of the most famous architectures in power amplifier [71], [88], [69]. The architecture allows to use switching power amplifier for OFDM signal, i.e. amplitude as well as phase modulated signal. A simple flow of this architecture is shown in Fig. 3.9 [4]. In this, first baseband signal splits

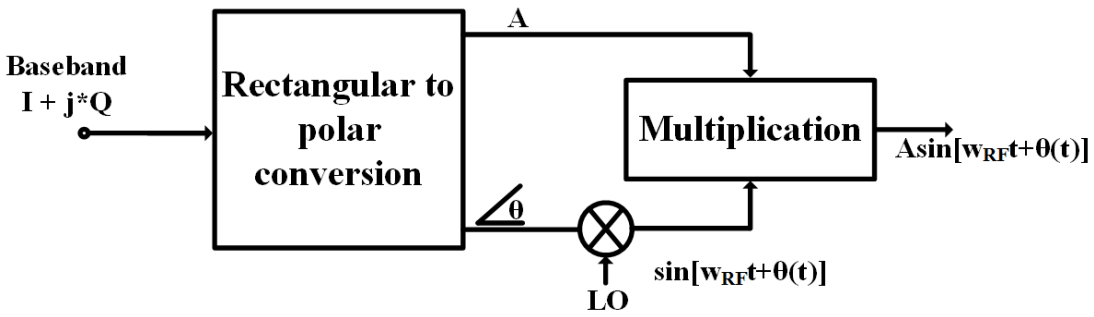


Figure 3.9: Basic Flow of Envelope Elimination and Restoration Power Amplifier.

into amplitude (envelope) and phase signals. The split operation is basically rectangular to polar conversion as shown in 3.4. Here, $(I + j * Q)$ is the rectangular representation of baseband signal. A and Θ are amplitude and phase of rectangular signal $(I + j * Q)$, respectively. Further, the phase information is modulated over RF signal followed by multiplication with amplitude signal. The splitting step allows here to use a switching power amplifier in the phase path (not shown in the figure).

$$\begin{aligned} \Theta &= tan^{-1}(\frac{Q}{I}) \\ A &= \sqrt{I^2 + Q^2} \end{aligned} \tag{3.4}$$

An elaborated block diagram of this architecture is shown in Fig. 3.10. Besides the previous discussion on the flow of envelope elimination and restoration, this diagram also contains envelope modulator, limiter, switching power amplifier along with matching network and load. In the amplitude path, an envelope modulator is used to amplify the amplitude signal. The envelope modulator provides supply to the switching power amplifier, which is responsible for the multiplication of the amplitude and phase signals [88]. The limiter is employed to convert the output of mixer to rail-to-rail signal, which is needed for the input of switching power amplifier [69].

Due to non-linear operation for rectangular to polar conversion shown in 3.4, the bandwidth of the phase is around five to seven times the composite baseband information [89]. Also, the bandwidth of the amplitude information is around two to three times than the composite baseband

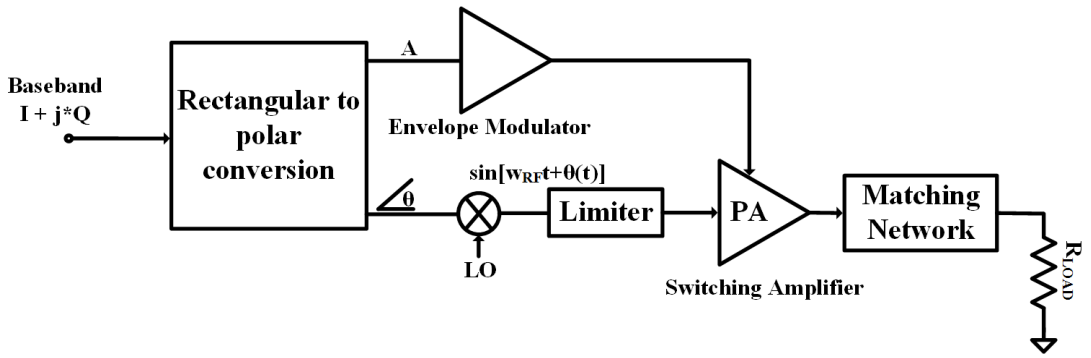


Figure 3.10: Block Diagram of Envelope Elimination and Restoration Power Amplifier.

information. This enlarged bandwidth put a huge challenges for the power efficient design of this architecture [90]. Besides this, there are two major issues of EER power amplifier: operation of limiter at RF frequency and delay mismatch between two parallel paths (amplitude and phase paths). Here, limiter is used to have a sharp rail-to-rail signal to turn-on and off the transistor of the switching power amplifier. Considering the input loading of the power amplifier along with high RF frequency, the limiter suffers from the limited rise and fall time. This limits the operating frequency of the switching amplifier i.e. RF frequency. The finite bandwidth of the limiter introduces AM/PM conversion, i.e., non-linearity [4]. The issue related to the delay mismatch between envelope and phase path is one of the most important issues in the polar power amplifier [91]. This mismatch corrupts the output signal; the corruption is proportional to the delay mismatch and derivative of the envelope signal [92]. The issue is more pronounced for the wide bandwidth wireless standards.

4. DIGITAL POLAR POWER AMPLIFIER

4.1 Introduction

Evergrowing multifunctionalities in cellphones come with a huge rise of network-data consumption. This huge consumption of network-data makes the battery run-time as an instrumental performance criterion in cellphones. In a cellphone, the power amplifier (PA) is the most power-hungry block, which controls the battery run-time [4]. This makes an imperative need for a highly power efficient power amplifier [88]-[99].

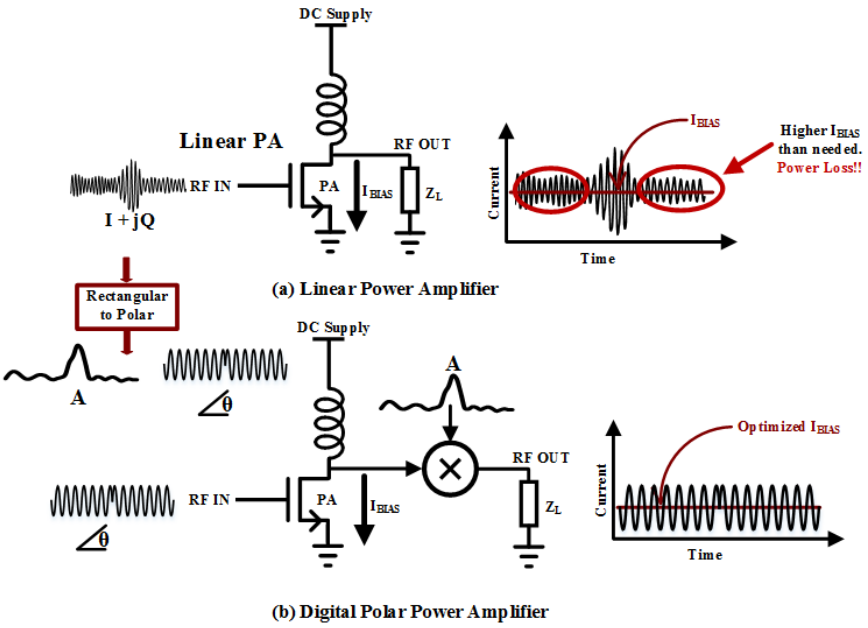


Figure 4.1: Power amplifier comparison (a) linear power amplifier (b) digital polar power amplifier.

For an efficient power amplifier, the envelope-elimination and restoration (EER) technique is commonly known in literature [100]-[101]. The technique has been briefly described in the previous chapter. In EER flow, the constant-envelope phase-modulated signal is processed efficiently using a switching amplifier and the amplitude information is restored using amplitude modulator at

the output [71]. Due to the limited frequency response of the amplitude modulator, this approach gets limited to low bandwidth wireless standard [19]. In order to solve this drawback, the digital polar power amplifier (DPA) is proposed [102], [19], [92]. The open loop structure helps here to meet the bandwidth requirement for demanding wireless standards [103]-[109]. The conceptual diagram of digital polar power amplifier is shown in Fig. 4.1. This shows a basic conceptual difference between the linear power amplifier and the digital polar power amplifier. Here, the amplifiers are of class-A category. As shown, in case of the linear amplifier, the bias current needs to be high enough in order to take care of a large PAPR (peak-to-average-power-ratio). This makes the amplifier less current efficient especially for upcoming wireless standards where PAPR is even larger than 6 dB. In order to have efficient current biasing, the baseband information is converted to polar representation (from rectangular representation). After this, the phase information is modulated over RF signal, and then the modulated RF signal, which is having constant amplitude, is processed through the power amplifier transistor. As the RF modulated input is having constant amplitude, the current biasing of the transistor can be optimized as shown in the Fig. 4.1. The output of the transistor needs to be multiplied by amplitude signal as shown in the figure. Hence, current bias optimization is achieved here with the help of coordinate transformation (from rectangular to polar). In an implementation of digital polar power amplifier, the multiplication is replaced by an amplitude controlled thermometric coded addition as shown in Fig. 4.2.

For this, the power amplifier is divided into several sub-PAs. The RF modulated phase information, which is having constant amplitude, is provided as the input to the gate of all sub-PAs. As the gate input amplitude is constant, so the previous argument regarding optimized current biasing remains valid for this configuration. As shown in the figure, instead of multiplication with amplitude, addition of each sub-PAs' current is used for the amplitude modulation. Based on the value of amplitude, the sub-PAs get enabled or disabled, and its current gets added at the output in order to provide amplitude modulation.

As discussed previously, the current bias optimization, hence enhancement in current efficiency is achieved in digital polar power amplifier compared to the linear power amplifier; this leads to

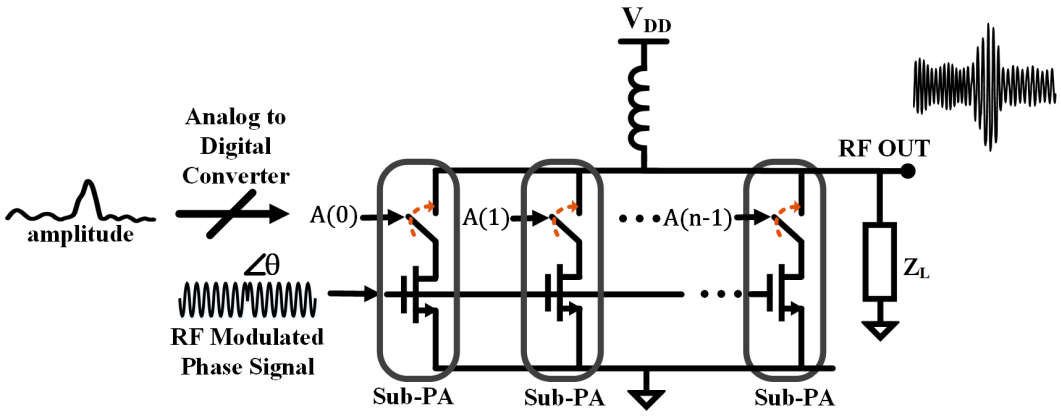


Figure 4.2: Conceptual implementation of digital polar power amplifier.

the improvement in the power efficiency. The voltage efficiency remains the same for both (linear power amplifier and digital polar power amplifier) as the supply voltage is constant for both of the cases. The related equations of power efficiency (η) is shown in 4.1.

$$\begin{aligned} \eta &= \frac{P_{OUT}}{P_{DC}} \\ P_{DC}(linearPA) &= V_{DD} * I_{BIAS} \\ P_{DC}(DPA) &= V_{DD} * \frac{1}{T}\int_0^T i_{BIAS}(t)dt \end{aligned} \tag{4.1}$$

Here, P_{OUT} is the power delivered to the load by the power amplifier, which is the same for both configuration (linear PA and DPA). Also, P_{DC} is power provided by the power supply (V_{DD}) to the power amplifier. For linear power amplifier, the power provided by the supply is $V_{DD}*I_{BIAS}$. Here, V_{DD} and I_{BIAS} are the supply voltage and bias current. For linear power amplifier, I_{BIAS} is constant and decided by the peak load current, which is shown in Fig. 4.1a. In case of DPA, the power provided by the supply is $V_{DD} * \frac{1}{T}\int_0^T i_{BIAS}(t)dt$. Here, $\frac{1}{T}\int_0^T i_{BIAS}(t)dt$ is the average current provided by the power supply during whole operation of the digital polar power amplifier. This average bias current depends upon amplitude statistics, which further depends upon wireless standards. Here, a test case of ideal power amplifier with IEEE 802.11n with 20 MHz wireless

standard and PAPR of 10.4 dB is used to show difference in bias current as well as the power efficiency for linear power amplifier and digital polar power amplifier. For this an ideal power amplifier with the load (Z_L) of 1.5 Ω is used that delivers output power of 22.48 dBm. For this test case, the transistor drain current is shown in Fig. 4.3.

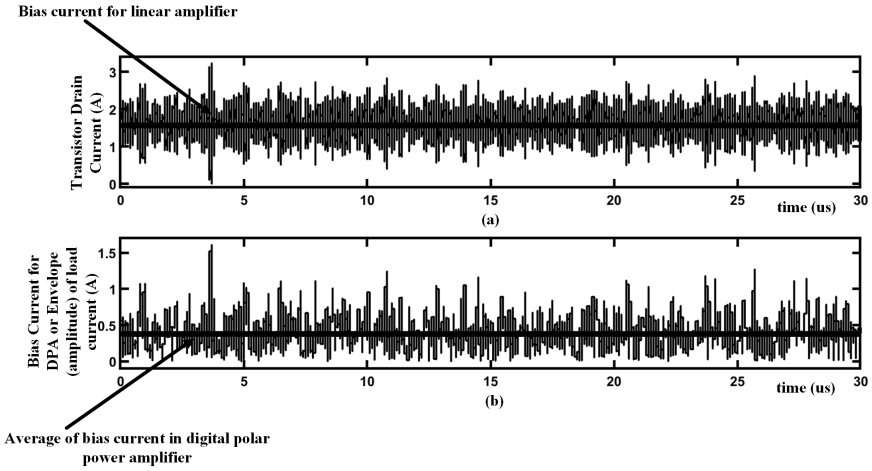


Figure 4.3: Test Case for IEEE 802.11n 20 MHz Wireless Standard (a) linear power amplifier Drain Current and bias current (b) digital polar power amplifier bias current.

In case of linear PA, the bias current needs to be 1.61 A, which is equal to the peak value of load current. In case of DPA, the bias current varies with amplitude (or envelope) of the load current as shown in Fig. 4.3b. The average of the bias current for the digital polar power amplifier is 0.431 A. Hence, the power efficiency improved in case of DPA compared to linear power amplifier by 3.74 times for wireless standard 802.11n with 20 MHz bandwidth, which is having PAPR of 10.40 dB. For the presented test case, the drain efficiency of the ideal linear power amplifier and ideal DPA is 4.6% and 17.15%, respectively. It is important to note that this test case is having a very high PAPR for an implementation of a transmitter [11].

For a realistic system implementation of a wireless transmitter, the PAPR is clipped down [5]. The power efficiency of the linear power amplifier and digital polar power amplifier with PAPR for IEEE 802.11n wireless standard is shown in Table 4.1. As shown in the table, the decrement

PAPR (dB)	Linear Power Amplifier Ideal Power Efficiency	Digital Polar Power Amplifier (DPA) Ideal Power Efficiency
10.4	4.6%	17.15%
9.25	6.02%	19.6%
7.92	8.15%	22.86%
6.4	11.72%	27.25%
4.65	17.84%	33.66%

Table 4.1: PAPR Vs. Ideal Power Efficiency.

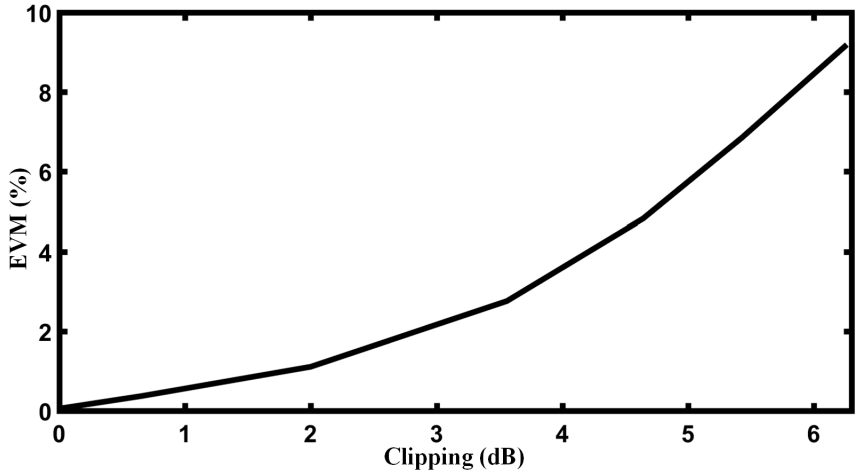


Figure 4.4: Error vector magnitude (EVM) vs PAPR for an ideal simulation setup for IEEE 802.11n 20 MHz Wireless Standard.

of PAPR increases the efficiency of both power amplifiers. It decreases the power supply for both configurations of power amplifier [20]. In addition, it decreases the bias current for the linear power amplifier because the peak load is reduced with decrease in PAPR [4]. However, the average bias of the digital polar power amplifier does not reduce significantly compared to the linear power amplifier. This is due to the statistics of the amplitude (envelope) signal in the wireless standard [39]. This helps to improve the linear power amplifier from 4.6% to 17.84%, which is 3.87 times for the clipping of PAPR by 5.75 dB. On the other hand, the power efficiency of the digital polar power amplifier improves from 17.15% to 33.66%, which is 1.92 times for the same clipping of PAPR. This is important that the class-A power amplifier operation is assumed for this ideal

power amplifier efficiency calculation. The power efficiency of the power amplifier can easily be increased with Class-AB or Class-B implementation. Besides the benefit of power efficiency enhancement with PAPR clipping, the clipping of PAPR degrades linearity as shown in Fig. 4.4 [92]. In this figure, an ideal simulation setup is used to measure the impact of PAPR clipping on modulation source's linearity in terms of error vector magnitude (EVM). As shown, when there is no clipping the EVM is as close as 0% and as the clipping of the PAPR increases the linearity degrades. For having 5% of EVM, a maximum clipping of 4.8 dB can be applied. However, this demonstration does not include non-linearity of power amplifier, hence a margin is needed to be included while considering clipping of PAPR.

The architecture of the digital polar transmitter is shown in Fig. 4.5. In this, first digital baseband processor generates baseband signal (I and Q), which is in digital rectangular format. This rectangular baseband information is converted to digital polar information (A and $\angle\theta$), which is mostly done with the help of CORDIC (Coordinate Rotation Digital Computer). This is a non-linear transformation as shown in 4.2. Due to non-linear operation, the bandwidth of amplitude (A) and phase is larger than the composite baseband signal (I and Q). For the amplitude and the phase signals, the bandwidth is 2-4 times and 5-7 times larger than composite baseband signal, respectively. For IEEE 802.11n 20 MHz, the amplitude and phase signal bandwidth are around 50 MHz and 110 MHz, respectively. This demands larger bandwidth for sub-PAs, which is one of the major drawbacks of the digital polar power amplifier.

$$\begin{aligned} A(t) &= \sqrt{I^2(t) + Q^2(t)} \\ \theta(t) &= tan^{-1}(Q(t)/I(t)) \end{aligned} \tag{4.2}$$

After this conversion, the digital phase information ($\angle\theta$) is converted to analog signal with the help DAC (digital-to-analog converter) as shown in the Fig. 4.5. As the phase signal bandwidth is quite larger compared to the composite baseband signal, this increases the bandwidth requirement for DAC. For the phase information in 802.11n wireless standards, the bandwidth of DAC needs

to be more than 250 MHz. This is an overhead in the digital polar transmitter compared to the linear transmitter. The output of DAC is modulated over RF with help of mixer, and the output of the mixer goes to the input of the power amplifier. As previously described in Fig. 4.2, the whole power amplifier is divided into small sub-PAs. All these sub-PAs receive the RF modulated phase information at their transistor gate input. These sub-PAs switch on-off to provide amplitude modulation depending upon amplitude information. The number of sub-PAs is depending upon the linearity specification of employed wireless standards. For example, there is a need of around 64 thermometric coded sub-PAs for QAM-64 IEEE 802.11g [19]. For wireless standard 64-QAM IEEE 802.11n with 20 MHz bandwidth, EVM versus amplitude bits is shown in Table 4.2. For this, an ideal setup of digital polar power amplifier is used. As shown in the table, minimum 5 amplitude bits are needed to satisfy the standard requirement of 802.11n; However, it does not include the power amplifier non-linearity. Therefore, most reported work uses 6 or higher amplitude bits [92].

Amplitude bits	Error Vector Magnitude (EVM) (%)
4	6.54%
5	3.60%
6	1.95%
7	1.42%
8	1.21%

Table 4.2: EVM Vs. Amplitude Bits.

Besides the benefit of improving the power efficiency, the digital polar power amplifier has the same flow of signal processing like EER technique, i.e., splitting and recombination of the input signal. This power amplifier suffers from two main issues: delay mismatch and spectral images. The flow of splitting and recombination makes it sensitive to the delay mismatch between phase and amplitude path as both are going through different circuits and path before recombining in sub-PAs as shown in Fig. 4.5. This delay mismatch leads to linearity degradation [110]-[4]. A delay mismatch calibration scheme based on nulled signal energy is reported in[114]. However,

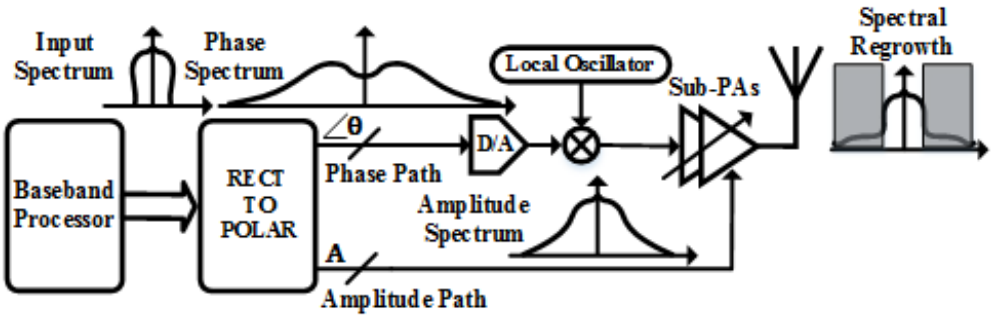


Figure 4.5: Digital polar transmitter architecture

this has complexity related to the nulled signal energy detection. For the linearity improvement, different pre-distortions schemes have been proposed [113]. A time aligner based delay-locked loop with variable high-pass filter is discussed for the EER architecture in [101]; however, it is not suitable for the digital polar architecture. Overall, there is limited attention shown so far for the delay mismatch issue in the digital polar power amplifier. Besides the issue of delay mismatch, the issue of spectral images is prominent in digital polar power amplifier which is present due to sampling of baseband information. These spectral images can violate the spectral mask of wireless standards. In addition, these image components are close to the RF frequency so it is not feasible to filter it out easily. A linear interpolation and digital filter are discussed in literature in order to reduce these spectral image components in the output spectrum [19], [5].

The comparison between linear power amplifier and digital polar power amplifier is shown in Table 4.3. Besides the benefit of higher power efficiency, the implementation complexity increases in case of digital polar power amplifier due to additional blocks (DAD, CORDIC and demanding mixer). As explained before, the mixer in case of digital polar transmitter is more bandwidth demanding due to the larger bandwidth of the phase information compared to the case of linear transmitter. Hence, this is an additional overhead for the digital polar transmitter. In additional, layout complexity is also higher for digital polar power amplifier due to numerous sub-PAs that are needed to be placed along with amplitude routing. It is also important to note that CORDIC, DAC and mixer also contribute to the power consumption. For CORDIC, the power consumption for

16 bits at 120 MHz is around 0.47 mW [115]. This does not include drivers' power consumption that is needed to drive the digital polar power amplifier's amplitude control bits and DAC inputs. For DAC, the power consumption for 10 bits at 250 MHz is around 100 mW [116]-[119]. For the mixer that can be used for IEEE 802.11 wireless standard, the power consumption is around 50 mW [120]. The power consumption of DAC and mixer is quite significant in the calculation of whole system power efficiency. It limits the digital polar power amplifier to a high power application, where the power consumption of additional blocks like DAC and mixer can be neglected. Similar to digital polar power amplifier, outphasing power amplifier also takes advantage of baseband signal transformation in order to use either current bias optimized linear power amplifier or switching amplifier (as discussed in the previous chapter) [72]. The baseband processing is different in case of the outphasing power amplifier compared to the digital polar power amplifier (rectangular to polar coordinate transformation) [73]. In case of outphasing power amplifier, the amplitude information is also embedded along with the baseband phase information as discussed in [76], [77]; this makes the larger bandwidth requirement for the sub-PAs in the outphasing power amplifier. Compared to the multiple sub-PAs in digital polar power amplifier, the outphasing power amplifier has only two sub-PAs. This makes its layout lesser complex in case of the outphasing power amplifier. These both amplifier suffers from the issue of mismatches between two paths. It is the phase and amplitude path delay mismatch for digital polar power amplifier; however, for outphasing power amplifier, it is gain and delay mismatch between two paths to the input of sub-PAs after signal-splitting [77]. The usage of power combiner at the output of two sub-PAs is another drawback of outphasing power combiner due to additional complexities and power losses [78], [79].

In this chapter, a calibration scheme for delay mismatch between phase and amplitude paths is presented for the digital polar power amplifier. This is an offline calibration which can be executed during any empty transmission slot. Besides this, an approach with linear interpolation filtering is presented here in order to improve out-of-band spectrum by reducing spectral images in the output spectrum. For this, the interpolation of amplitude and phase is used for the filtering purpose. This work is simulated in a 40 nm CMOS technology, and tested with 64-QAM IEEE 802.11n wireless

Parameters	Digital Polar Power Amplifier (DPA) wrt. Linear Power Amplifier
Power Efficiency	Higher (without additional modules power consumption)
Area	Larger due to layout routing, and additional modules
Additional Modules	DAC, CORDIC and demanding mixer
Additional Issues	Spectral images and timing alignment of amplitude and phase
Complexity	Higher in design and implementation

Table 4.3: Comparison of Linear Power amplifier and Digital Polar Power Amplifier.

standard. The organization of the chapter is as follows. In Section 4.2, the issues regarding delay mismatch between amplitude and phase, and spectral images are described. Section 4.3 presents a calibration scheme for delay mismatch between phase and amplitude in the digital polar power amplifier. Section 4.4 presents a linear interpolation approach for the spectral images reduction at the output of digital polar power amplifier. In Section 4.5, schematic design and layout of the digital polar power amplifier is discussed followed by simulation setup and results in Section 4.6. Finally, conclusions are drawn in Section 4.7.

4.2 Issues in Digital Polar Power Amplifier

4.2.1 Delay Mismatch between Amplitude and Phase Signal

In the digital polar power amplifier, the phase and amplitude are generated from the same source (composite baseband information). Therefore, any variation in the baseband signal should impact phase and amplitude at the same time instance. However, considering the fact that phase and amplitude follow different paths and circuits, there can be a delay mismatch between phase and amplitude before they are recombined at the sub-PA. This effect is illustrated in Fig. 4.6. In this figure, different scenarios of the delay mismatch is shown. Due to non-linear behavior of splitting and recombining of the baseband input signal, the linear non-idealities like delay-mismatch between phase and amplitude signal causes spectral regrowth [92]. For the sake of understanding of impact of the delay mismatch, assuming the delay mismatch of Δt between phase and amplitude, the output of the power amplifier ($V_{out}(t)$) can be written as 4.3 [4]; for simplicity, the delay mismatch is only assigned to the amplitude path.

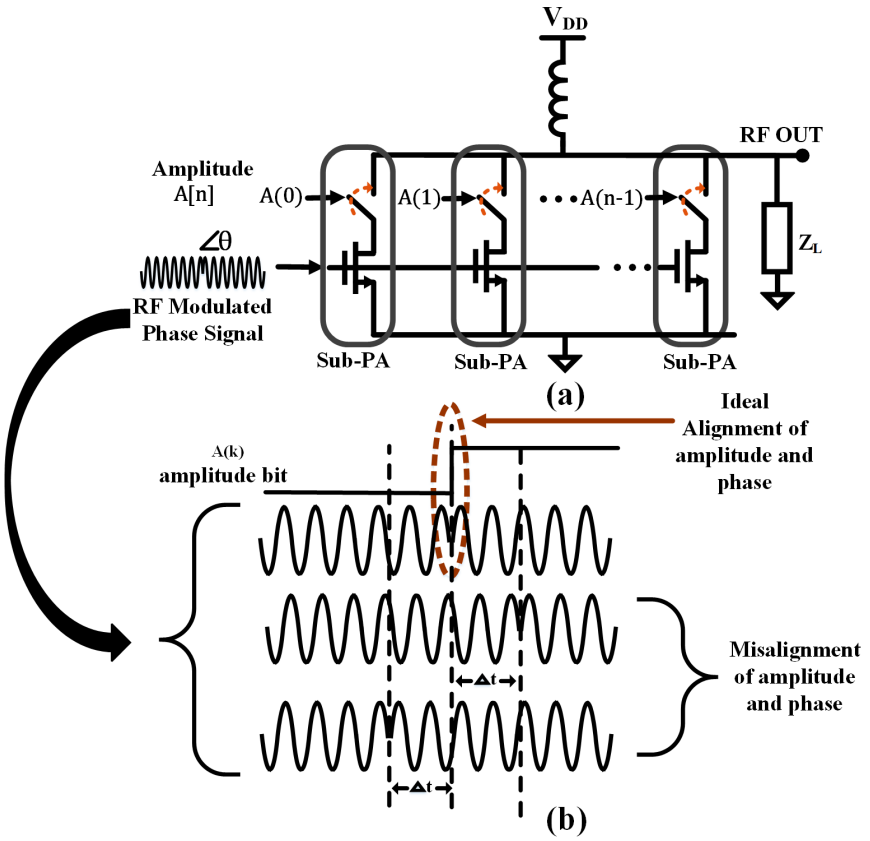


Figure 4.6: Delay mismatch illustration (a) digital polar power amplifier (b) timing alignment scenarios between amplitude and phase

$$V_{out}(t) = A(t + \Delta t)cos(\omega_{RF}t + \theta(t)) \tag{4.3}$$

$$V_{out}(t) \approx A(t)cos(\omega_{RF}t + \theta(t)) + \Delta t \left(\frac{dA(t)}{dt}\right) cos(\omega_{RF}t + \theta(t)) \tag{4.4}$$

$$V_{out}(j\omega) \approx A(jw) * \mathcal{F}\left(cos(\omega_{RF}t + \theta(t))\right) + \Delta t \left(jwA(jw)\right) * \mathcal{F}\left(cos(\omega_{RF}t + \theta(t))\right) \tag{4.5}$$

where ω_{RF} is the carrier frequency. With the help of Taylor series, $A(t + \Delta t)$ can be approximated as $[A(t) + \Delta t\frac{dA(t)}{dt}]$ as shown in 4.4. The first term of 4.4 is an ideal output of digital polar power amplifier. However, the second term of 4.4 is an addendum in the $V_{out}(t)$. This addendum is proportional to the delay mismatch, and the time derivative of the amplitude signal. To understand, the impact of the delay mismatch in the frequency spectrum, the Fourier transform of the $V_{out}(t)$ is

shown in 4.5. Here, $\mathcal{F}$ and $*$ are Fourier transform operator and convolution symbol, respectively. For the sake of simplicity, the cosine function has been kept within the Fourier operator. In 4.5, there is an extra multiplication of Δt and jw with $A(jw)$ in its second terms of RHS (right hand side). Here, jw multiplication with $A(jw)$ changes its magnitude and phase, and its further convolution with $\mathcal{F}\left(cos(\omega_{RF}t + \theta(t))\right)$ generates output which is different in magnitude and phase compared to the first term of RHS in 4.5, and this is unwanted component in the output. Also, the contribution of the multiplication of Δt is to increase the magnitude of the unwanted component in the output spectrum. This unwanted component in the output spectrum corrupts the ideal output spectrum(in-band as well as out-of-band).

In order to quantify the impact of delay mismatch, adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) are plotted versus delay mismatch between phase and amplitude for an ideal digital polar power amplifier simulation setup shown in Fig. 4.7. It is for wireless standard 64-QAM IEEE 802.11n with 20 MHz bandwidth. As expected, ACLR and EVM both degrade with the increment in delay mismatch. The maximum allowed delay mismatch depends upon the requirement of the wireless standard specifications for ACPR and EVM. For the considered case here, the maximum allowed value for the delay mismatch should not exceed 2 ns. However, it does not include any margin for power amplifier non-linearity, which further constraints this delay mismatch to around 1 ns.

4.2.2 Issue of Spectral Images

In a digital polar power amplifier, the operating sampling frequency in rectangular to polar conversion (in CORDIC) causes spectral images at the output spectrum [5]. These spectral images can violate the spectral mask of a wireless standard. A scenario of such violation is shown in the Fig. 4.8. For this, an ideal digital polar power amplifier is simulated for IEEE 802.11n 20 MHz wireless standard, which has the sampling frequency of 120 MHz. The issue becomes more serious for the power amplifier with low sampling frequency, e.g. 80-100 MHz in CORDIC because in such cases the spectral images are closer to the carrier frequency. However, even with a high sampling frequency of around 300-400 MHz, the issue of spectral violation due to spectral images

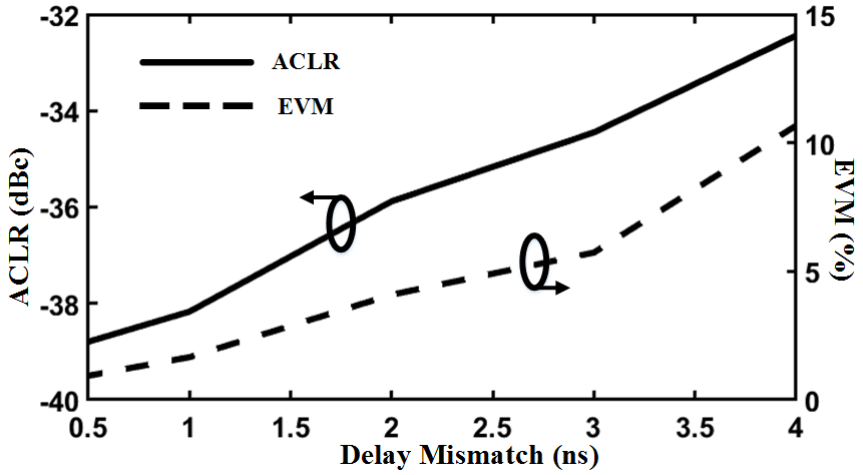


Figure 4.7: ACLR and EVM Vs. delay mismatch between phase and amplitude for IEEE 802.11n 20 MHz wireless standard

is not completely removed [19].

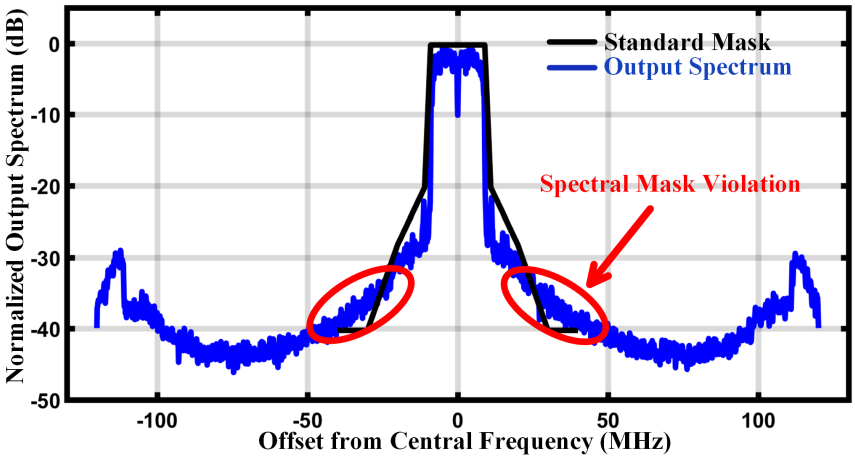


Figure 4.8: An Illustration of violation of the spectral mask due to spectral images for IEEE 802.11n 20 MHz wireless standard in an ideal digital polar power amplifier

4.3 Proposed Calibration Scheme for Delay Mismatch Between Phase and Amplitude

In order to have a delay mismatch between phase and amplitude path within the allowed limit, a calibration scheme is presented here. In the proposed approach, the delay between a phase-to-

phase transition is matched with that in phase-to-amplitude transition (or vice-versa) in order to have synchronization between phase and amplitude. For this purpose, a special calibration input pattern is used. The input pattern is selected to easily detect phase and amplitude transitions that eventually helps to synchronize them.

4.3.1 Proposed Calibration Scheme

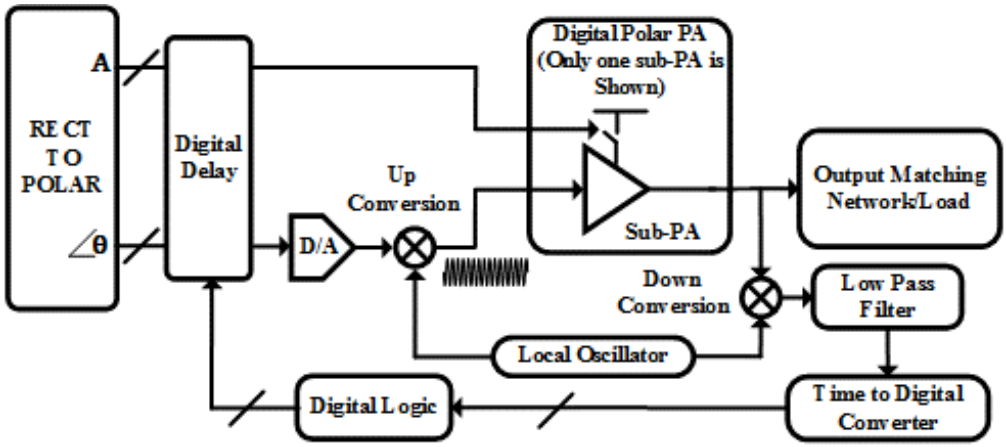


Figure 4.9: Proposed calibration scheme for the delay mismatch between phase and amplitude

In order to obtain delay of phase-to-phase and phase-to-amplitude transitions at the output of the digital polar power amplifier, the baseband information needs to be retrieved from the output of the power amplifier. After this, delays between mentioned transitions are needed to be equated. A block diagram of the proposed calibration scheme is shown in Fig. 4.9. Here, downconverter, low pass filter, time to digital converter, digital logic and digital delay are additional blocks compared to conventional digial polar transmitter. In Fig. 4.9, the purpose of the down converter and the low pass filter is to obtain the baseband information and to remove high frequency spectral components. Additionally, an amplifier (not shown in the figure) is employed to amplify the output of the filter to rail-to-rail voltage. A time-to-digital converter is used to measure phase-to-phase and phase-to-amplitude transitions. Furthermore, the digital logic block contains logic that compares the delay of phase-to-phase transition and phase-to-amplitude transition obtained from the time-to-digital

converter and it generates the control signal for the digital delay block to equate these two delays. The digital delay block is having a programmable delay which is achieved through a multiplexer and a chain of inverters. The flow for the calibration is also shown in Fig. 4.10. The down converter is connected via a switch (not shown in the figure), so it does not load the power amplifier during its normal operation.

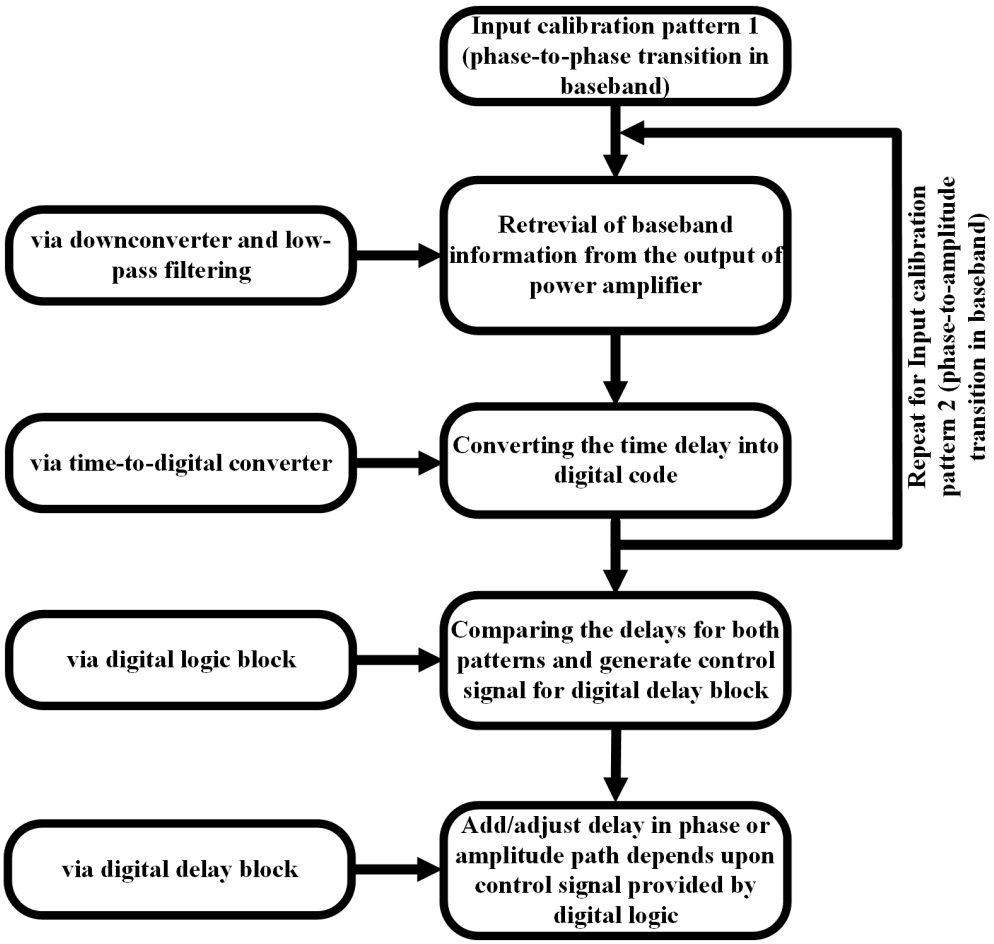


Figure 4.10: Proposed flow of the calibration scheme for delay mismatch between phase and amplitude

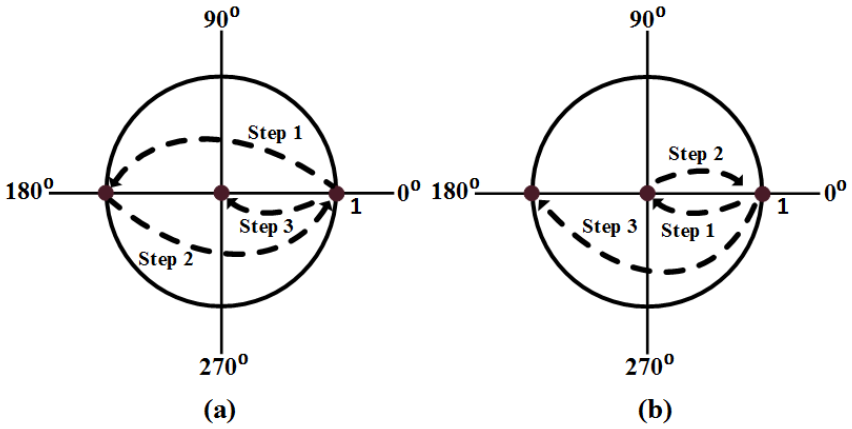


Figure 4.11: Calibration input pattern sequences (a) phase-to-phase and phase-to-amplitude transitions (b) amplitude-to-amplitude and amplitude-to-phase transitions

4.3.2 Input Pattern Sequence for Calibration Purpose

In order to detect the transitions of phase or amplitude at the output of power amplifier (after down-conversion and low-pass filtering), the phase and amplitude variations need to be selected in such a way that it creates an optimum case for detection on the time-to-digital converter. During phase-to-phase transition, the phase is chosen either $0°$ or $180°$ so that it gives maximum variation, i.e., 1 to -1. Additionally, the amplitude is either 1 or 0 to enable or disable the sub-PA. The input sequence is shown in Fig. 4.11a. First, phase and amplitude are kept at $0°$ and 1 (ON), respectively. After this the phase changes by $180°$ followed by $0°$ keeping amplitude at 1. This transition helps to determine phase-to-phase transition time. In the next step, the amplitude is 0 (OFF), which enables to determine phase-to-amplitude transition time. An alternate input pattern sequence is also shown in Fig. 4.11b. The simulation result of this calibration scheme is discussed in Section 4.6.

4.4 Interpolation based filtering for Spectral Images Issue

In order to solve the issue of spectral images, which is discussed in Section 4.2, a linear interpolation technique is used in this work. The linear interpolation helps here to achieve filtering operation, which reduces the spectral images component in the output spectrum of the digital polar

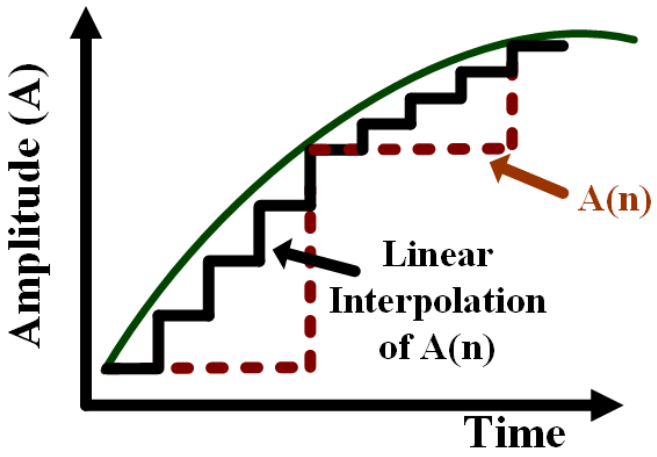


Figure 4.12: An example of interpolation.

power amplifier. The basics of interpolation are shown in Fig. 4.12 for the amplitude signal (A). Here, A(n) is linearly interpolated by delay (T/4); assuming 1/T(= fs) is the sampling frequency of A(n). The expression of the interpolated A(n), $A_{IP}(n)$, is shown in 4.6. In order to understand filtering operation provided by the interpolation operation, z-domain transformation of 4.6 needs to be done as shown in 4.7. Here, $H_{IP}(z)$ is the filter transfer function, which is provided with the help of interpolation operation. The transfer function is plotted in Fig. 4.13, and it shows nulls at 1/T (=fs), 2/T(=2fs), and 3/T(=3fs); hence, the spectral images will be suppressed at these frequencies by the linear interpolation. This can be also understood from 4.8, which is obtained by substituting $z = e^{sT}$ and $s = jw$ in $H_{IP}(z)$ [121]. In 4.8, by equating cosine terms to zero, the location of nulls can be obtained as discussed.

$$A_{IP}(n) = \frac{1}{4}\left(A(n) + A(n-1/4) + A(n-1/2) + A(n-3/4)\right) \tag{4.6}$$

$$\begin{aligned} A_{IP}(z) &= \frac{A(z)}{4}\left(1 + z^{-1/4} + z^{-1/2} + z^{-3/4}\right) \\ A_{IP}(z) &= A(z) \cdot H_{IP}(z) \\ Where, H_{IP}(z) &= \frac{1}{4}\left(1 + z^{-1/4} + z^{-1/2} + z^{-3/4}\right) \end{aligned} \tag{4.7}$$

$$H_{IP}\left(exp(jwT)\right) = exp(-j3wT/8) \cdot cos(jwT/8) \cdot cos(jwT/4) \tag{4.8}$$

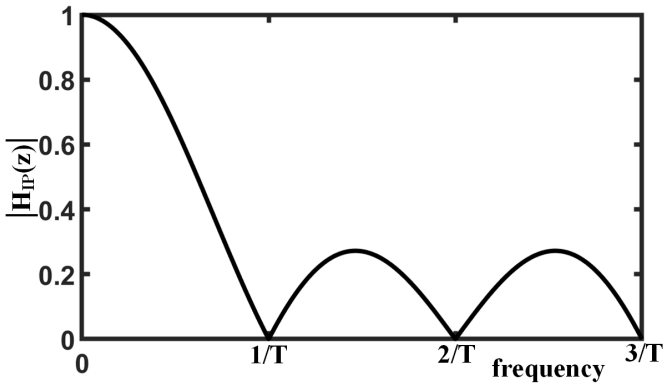


Figure 4.13: Magnitude response of the interpolation filter (H_{IP}(z)).

In the case of digital polar power amplifier, the phase ($\theta(n)$) and the amplitude ($A(n)$) both have spectral images [19]. In order to reduce spectral images through linear interpolation operation, the amplitude and phase are interpolated and processed through the digital polar power amplifier. The concept is shown in Fig. 4.14. Here, the interpolation is done over amplitude ($A(n)$) and phase ($\theta(n)$) and then each respective interpolated components of phase and amplitude are multiplied followed by summation at the output (OUT(n)). The operation is shown in 4.9, and its z-transform is shown in 4.10. Here, $H_{IP}(z)$ represents the implemented filtering with the help of the linear interpolation. As discussed earlier, this filter puts null at the sampling frequency and its multiples [19].

$$
\begin{aligned}
OUT(n) = \frac{1}{4}[&A(n)\cdot\theta(n) + A(n-1/4)\cdot\theta(n-/4) + A(n-2/4)\cdot\theta(n-2/4)+ \\
&+ A(n-3/4)\cdot\theta(n-3/4)] \\
&= \frac{1}{4}\sum_{k=0}^{3} A(n-k/4)\cdot\theta(n-k/4) \\
&= \frac{1}{4}\sum_{k=0}^{3} P(n-k/4) \\
&Where, P(n) = A(n)\cdot\theta(n)
\end{aligned}
\tag{4.9}
$$

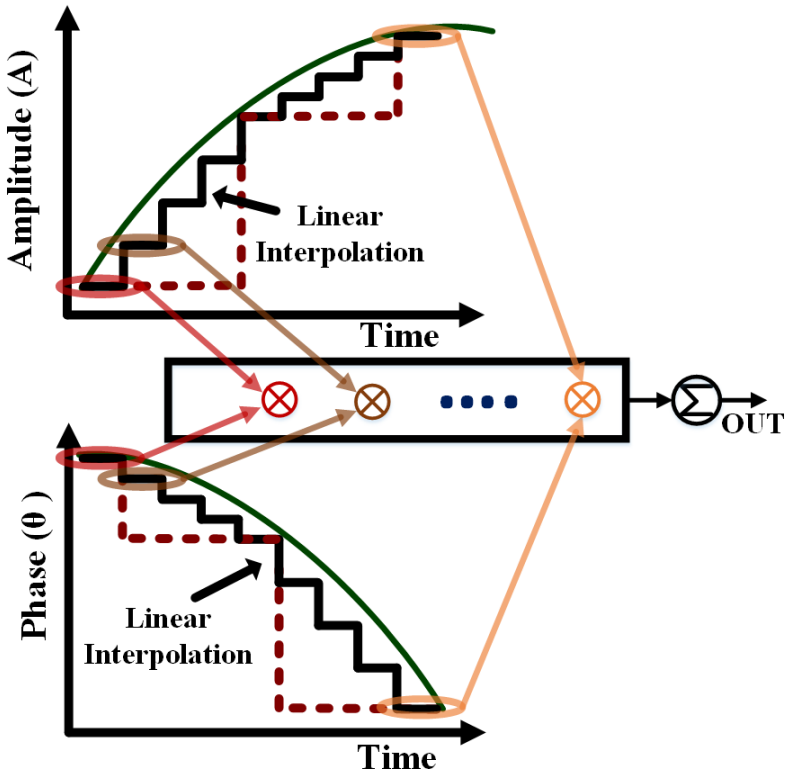


Figure 4.14: Conceptual diagram of amplitude and phase interpolation.

$$
\begin{aligned}
&OUT(z) = P(z)(1 + z^{-1/4} + z^{-1/2} + z^{-3/4}) = P(z) \cdot H_{IP}(z) \\
&Where, H_{IP}(z) = \frac{1}{4}\left(1 + z^{-1/4} + z^{-1/2} + z^{-3/4}\right)
\end{aligned}
\tag{4.10}
$$

The architecture of the proposed digital polar transmitter is shown in Fig. 4.15. Here, a subsequent delay of T/4 is added in amplitude and phase in order to have a linear interpolation. The respective phase and amplitude is multiplied at each sub-PAs as discussed in Section 4.1. The output of all the sub-PAs are added at the output to achieve the expression shown in 4.9. Here, the purpose of digital controller is to switch on/off sub-PAs based on the amplitude information, which is further disused in the next section. The delay (T/4) can be changed in order to implement a different filter function, $H_{IP}(z)$. Here, each sub-PA are furthers divided, which depends upon the number of the implemented amplitude bits as discussed in Section 4.1. The implementation of the system and its results are discussed in Sections 4.5 and 4.6.

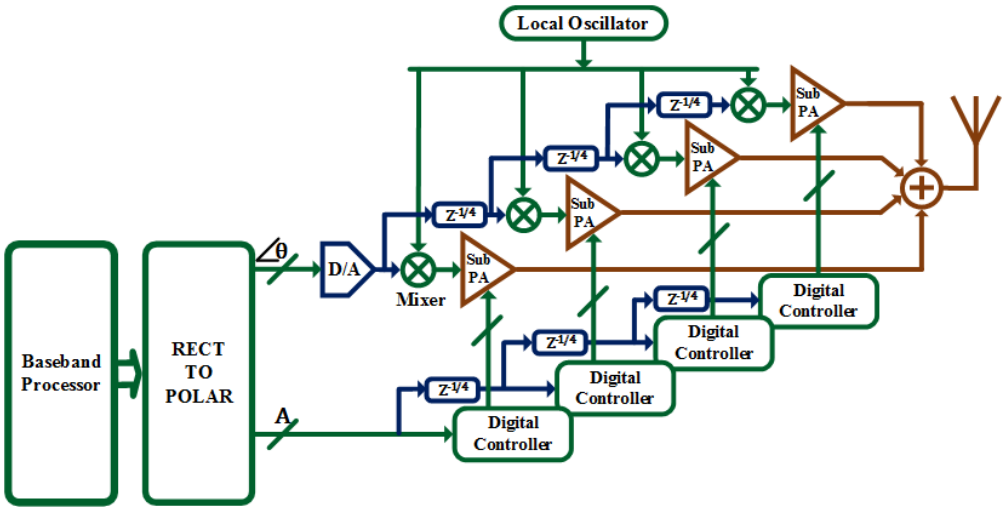


Figure 4.15: Architecture of amplitude and phase interpolation based digital polar transmitter.

4.5 Schematic Design, Layout and Silicon

For this work, the digital polar power amplifier was designed in CMOS 40 nm technology node. The block diagram of the power amplifier and its matching network is shown in Fig. 4.16. The power amplifier consists of three stages, pre-driver, driver and PA last stage. The driver stage is switchable so that it can be turned off when not in used; hence, providing higher power efficiency. There is a direct connection between driver stage and the PA last stage, so a common mode feedback (not shown in the figure) is needed to control the DC operating voltage at the output node of the driver stage. AC-coupling capacitors are used at the output of the pre-driver stage in order to provide control of the input bias voltage of the driver stage via R_{BIAS}. Here, the digital logic block, which mainly consists of D-flip flop and inverter and logic gates, is used to control the logic to turn on-off the drivers and sub-PAs of the digital polar power amplifier. The input of the digital logic block are the amplitude bits, which is coming from a FPGA in this work. Also, here the RF input is phase modulated RF signal. The matching network is off-chip. Due to the switching nature of the digital polar power amplifier, a common mode current switching is expected, which can create a large common mode voltage swing [5]. To nullify the impact of this common mode voltage swing in the power amplifier operation, a common mode feedback circuit (CMFB) is added (off-chip) as shown in Fig. 4.16.

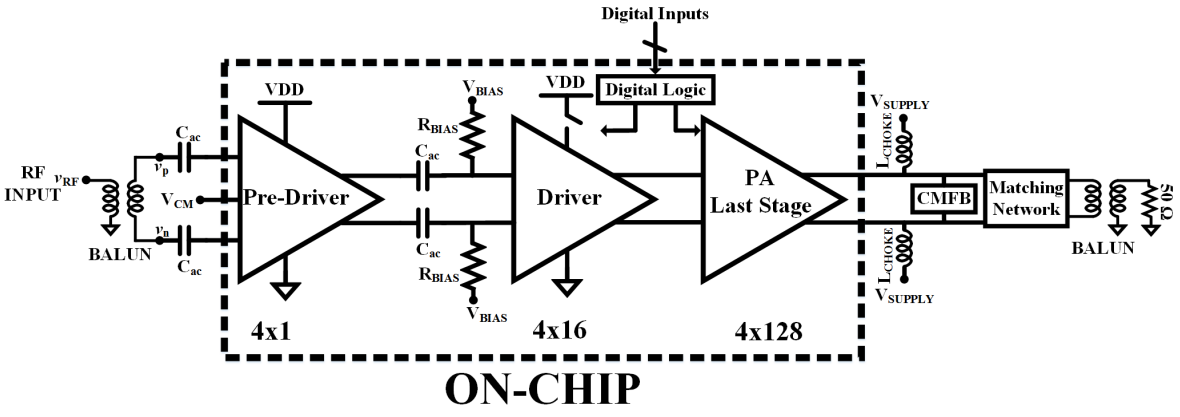


Figure 4.16: The block diagram of digital polar power amplifier.

Due to expected high temperature of operation of power amplifier, $100°C$ is used as a temperature parameter in the design setup. The performance is simulated at 2.4 GHz considering IEEE 802.11 n wireless standard with 20 MHz bandwidth for the system simulation. The schematic of the pre-driver stage is shown in the Fig. 4.17. This is a single stage amplifier. The input of the transistor is connected to 50 Ω for the termination purpose. The triple-well RF transistor is used here. The size for input transistor is W/F (width per finger) =1um, L = 120 nm and 128 fingers. The tail transistor's size is W/F (width per finger) =3um, L = 120 nm and 320 fingers. The supply voltage for the pre-driver stage is 1.8 V. The value of resistor, R, is 32.89Ω. The tail current, I_{TAIL} is 24.42 mA. The applied I_{BIAS} is 7.68 mA. The DC power consumption of this stage is 43.96 mW without including external I_{BIAS} current consumption. The V_{OV} (overdrive voltage) of the input RF and tail transistors is 265.4 mV and 176.4 mV, respectively, at input gate bias of 1 V. The input gate capacitance is 168.96 fF (single sided). The S_{21} (gain) is 1.97 V/V at 2.4 GHz. Considering small input voltage swing for being first stage of the power amplifier, the linearity performance of this stage does not show any concern here.

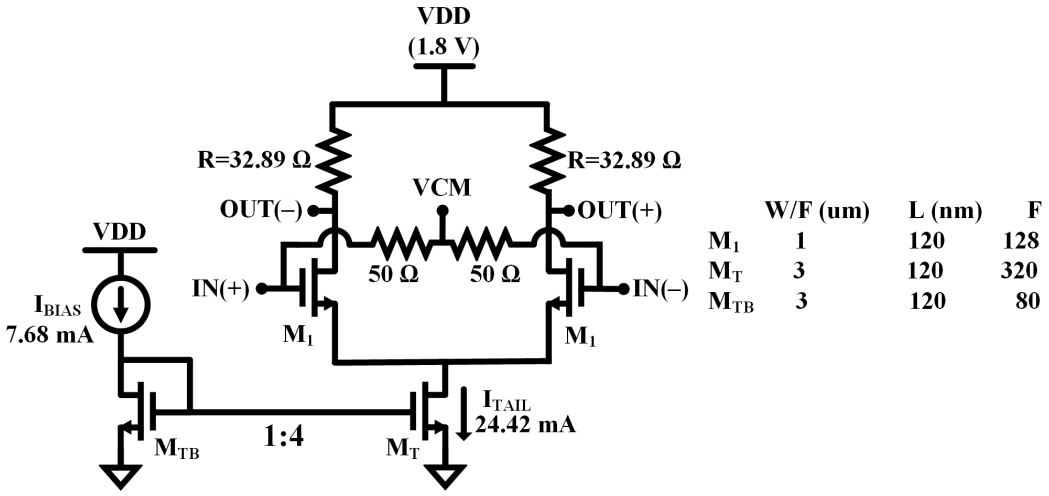


Figure 4.17: Pre-driver stage schematic.

The schematic of the driver stage is shown in the Fig. 4.18. Here the top transistor is working

as a switch and it is controlled by amplitude logic through an inverter. If the driver is not in use then it can be turned off with the help of this switch, which decreases the DC power consumption of this stage, hence a better power efficiency. In order to control the DC operating voltage of the driver stage output node, the gate voltage of the M_T is used, which is discussed in the next paragraph. Here, the transistor size for input transistor is W/F (width per finger) = 1 um, L = 120 nm with 24 fingers, and its gate capacitance is 31.58 fF. The tail transistor size is W/F=3um, L = 120 nm with 72 fingers. The top switch size is W/F = 2.9um, L = 270 nm with 36 fingers. Here, the resistor R is 220 Ω. The input gate DC voltage bias is 950 mV, which is provided through R_{DBIAS} of value $9.8k\Omega$. The value of ac coupling capacitor is 470 fF. The applied supply for this stage is 1.45 V. The overdrive voltage (V_{OV}) of the input transistor and tail transistor is 245.9 mV and 147.1 mV, respectively. The I_{TAIL} (tail current) is 3.47 mA. This stage is having gain of 2.21 V/V at 2.4 GHz. This also provide IM_3 of 36.25 dB for differential output voltage of 750 mVpp. In this work, one pre-driver controls 16 driver stages, and one driver stage drives eight last stage PA cell.

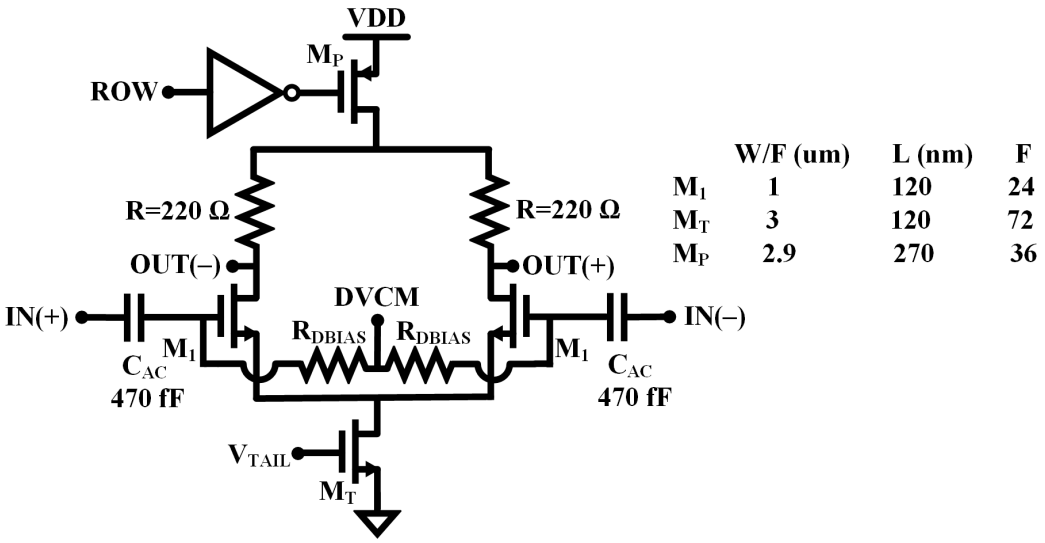


Figure 4.18: Driver stage schematic.

The schematic of the V_{TAIL} voltage generator is shown in the Fig. 4.19. This stage is used to

generate the needed voltage for V_{TAIL} node in the driver circuit in order to have pre-defined DC operating voltage for the output node of the driver circuit. For this purpose, a common mode circuit of the driver stage is designed as shown in Fig. 4.19 [23]. To reduce the DC power consumption, the finger of the common mode circuit is reduced to $1/6th$ for this replica stage. A feedback control loop is used here to generate V_{TAIL} as shown in Fig. 4.19. Here, a simple single-stage single-ended amplifier is used to provide enough loop gain. For the loop stability, the capacitor, C_{TAIL} of value 1 pF is added at V_{TAIL} node. The DC gain, phase margin and unity gain frequency of the feedback loop are 41.7 dB, 75° and 360 MHz, respectively. The reference voltage, V_{REF}, for the control loop is generated from PA's last stage replica cell, which is having a current bias, I_B, of value 654.2 uA in order to generate the needed voltage for the bottom transistor in PA last stage replica cell as shown in Fig. 4.19. The purpose of C_{BYPASS} (150 fF) is here to decrease the impact of the external noise through I_B. The size of transistors of the blocks are also shown in Fig. 4.19.

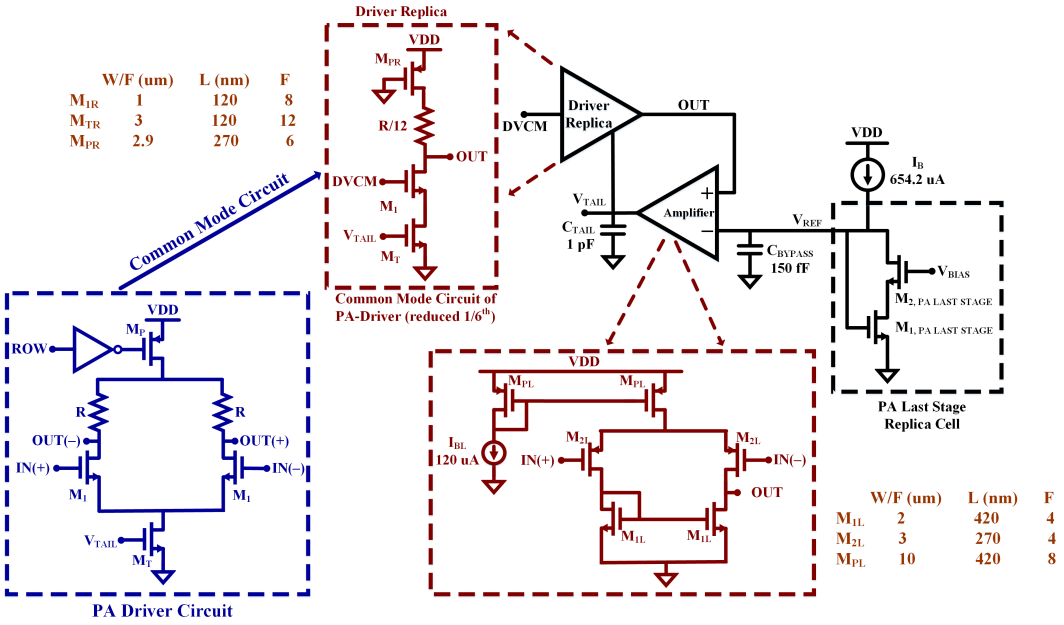
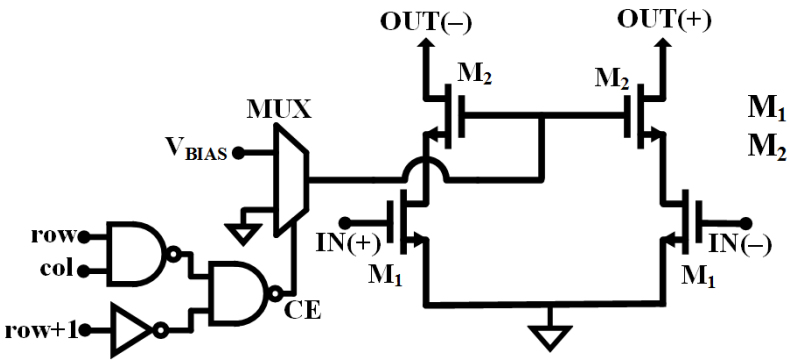


Figure 4.19: V_{TAIL} voltage generator.

The schematic of the last stage of the power amplifier is shown in the Fig. 4.20. Eight of these last stage cells are driven by a single driver in this work. The transistor size of the bottom transistor (M_1) is W/F (width per finger) = 1 um, L = 120 nm with 6 fingers. The top transistor size (M_2) is W/F=2.9 um, L = 270 nm with 6 fingers. The single ended quiescent current is 654.2 uA. The gate bias voltage of the bottom transistor and the top transistor is 800 mV and 1.38 V (V_{BIAS}), respectively. The input gate capacitor of the bottom transistor is 8.05 fF. Also, the transconductance of the bottom transistor is 2.96 mA/V. In this work, 512 of PA last stage cells provides 27 dBm of saturated output power. The PA last stage cell is switchable depending upon information of amplitude provided at the system input. The digital logic including inverter, NAND, MUX are used here to switch the top transistor of the PA cell. The truth table of the digital logic is shown in Table 4.4. Here, CE logic (cascode enable) is high when either row and column both are enabled or when next row is enabled.



	W/F (um)	L (nm)	F
M_1	1	120	6
M_2	2.9	270	6

Figure 4.20: PA last stage schematic.

The floor plan of the power amplifier is shown in the Fig. 4.21. In order to have discussed linear interpolation of Section 4.4, the whole power amplifier is divided into four corners. Here, each corner is a replica of the other. Considering the need of having 7 amplitude bits including margin for the linearity as shown in Table 4.2, each corner is having 128 (2^7) power amplifier last stage cells. For the ease in layout and given die area, these 128 power amplifiers cells are divided

row+1	row	col	CE
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	X	X	1

Table 4.4: Truth table of digital logic in PA last stag cell.

into 16 rows and 8 columns ($16 \times 8 = 128$). Hence, 7 bits of amplitude is divided into 4 bits of row and 3 bits of columns. Here, each row, which is having 8 power amplifier last stage cells, is driven by a driver as shown in Fig. 4.21. A driver is responsible for a whole row; hence, it can be turned off during disabled row logic, which is driven by amplitude bits. For this purpose, a switchable supply is provided in the power amplifier driver as shown in Fig. 4.18. There are 16 power amplifier drivers in a corner and these drivers are driven by a pre-driver as shown in Fig. 4.21. In this work, thermometric coding is used for row and column logic as all PA last stage unit cells are identical. For this purpose, binary to thermometric converter is presented in the digital logic. The layout and silicon die is shown in Fig. 4.22. RF output is taken from the vertical side of the PA chip. RF input (phase modulated RF signal) is provided to the each corner through top and bottom as shown in Fig. 4.22. The size of the layout or die is 3mmx2mm; considering its large size, it is having complexities in routing for row, column, clock, RF output. Here, the RF signal needs to be routed to 128 PA last stage cells in each corner along with rows and columns. The digital logic (row, column and clock) needs to be routed such that it does not interact with RF signal as it can contaminate it. Therefore, a safe distance (based upon layout extracted simulation) has been used where coupling of the digital routing signal and RF signal is small. In addition, digital logic like thermometer converter has been placed in the center of the die (shown in red box in Fig. 4.22), which is far from the four corners. In this work, the routing of amplitude and phase signal puts delay mismatch of around 100-150 ps in post-layout simulation on critical path. This delay mismatch is within the limit as shown in Fig. 4.7. However, the delay mismatch remains critical for the digital polar power amplifier performance due to separate path of amplitude and

phase outside the chip through DAC and mixer as shown in Fig. 4.5. The discussed complexities of the layout is another drawback of the digital polar power amplifier compared to the linear power amplifier.

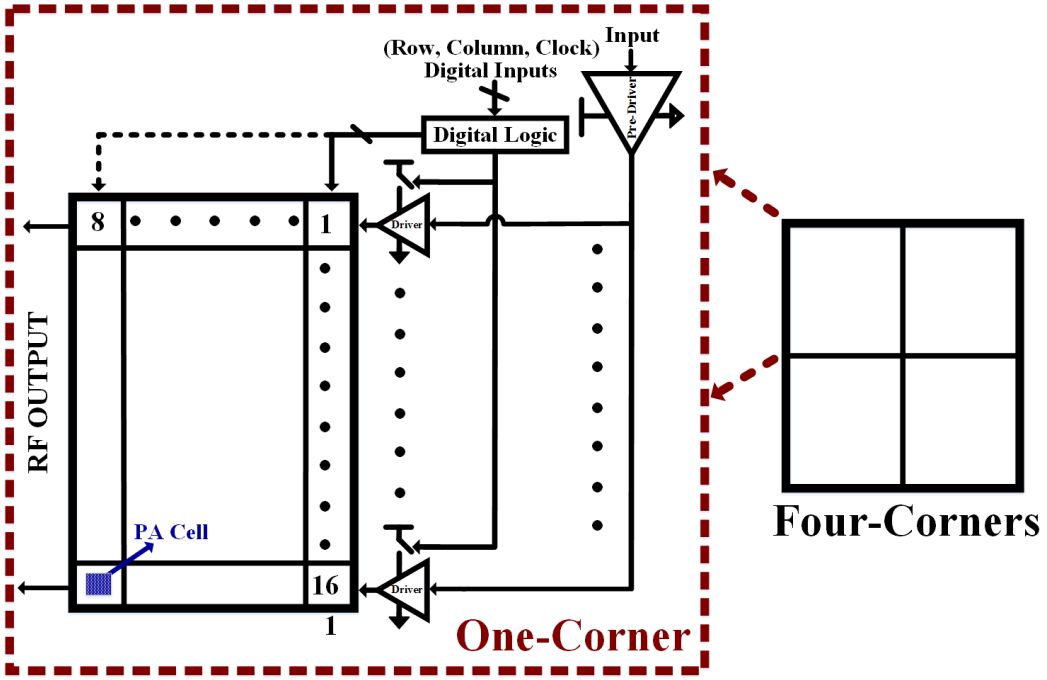


Figure 4.21: Power amplifier floor plan.

4.6 Simulation Setup and Results

4.6.1 Simulation Setup

For the discussed calibration scheme for the delay mismatch between phase and amplitude, a system shown in Fig. 4.9 is implemented in Cadence. As discussed earlier, the used digital polar power amplifier, a three-stage power amplifier, was designed for the saturated output power of 27 dBm. The employed matching network at the output of the power amplifier is cascade L-matching network (0.37 nH, 11.25 pF, 1.64 nH and 1.33 pF). For the purpose of prototype demonstration of this work, the most blocks except the power amplifier are either kept at the behavioral level, which include digital logic, digital delay, DAC, low pass filter and mixers. For the low pass filter, a

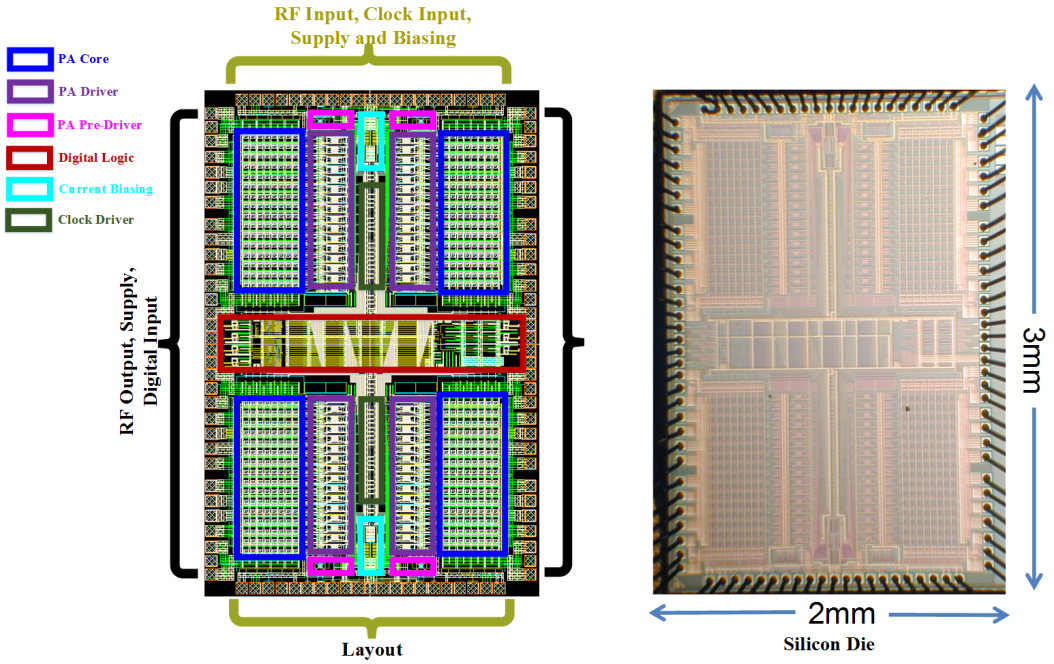


Figure 4.22: Power amplifier layout and silicon die.

2nd order Butterworth filter with cut-off frequency at 250 MHz was employed in VerilogA [122]. Regarding time-to-digital converter, a textbook digital delay-line based architecture was designed with 42 digital buffers [123]. The delay of each buffer is kept at 0.30-0.35 ns. With this, a wide range of delay mismatch was able to calibrate in the presented scheme.

For the purpose of Cadence-based simulation of the linear interpolation based filtering in digital polar power amplifier, the test input of wireless standard 64-QAM IEEE 802.11n with 20 MHz bandwidth is directly used from Cadence built-in RF source. The simulation setup is shown in Fig. 4.23. For the simplification, the single ended version is shown here. The sampling frequency in the coordinate transformation was kept at 120 MHz. Due to complexity of implementation, the interpolation of the phase is done outside the implemented digital polar power amplifier. For this, the digital baseband phase information is passed through four series DFF (D flip-flop) with the clock with four phases (0°, 90°, 180° and 270°). These digital baseband phase information after converting to analog via DAC is modulated over RF carrier (2.4 GHz) with the help of up-converter. The up-converter for the simulation purpose is behaviorally implemented here. The output of each

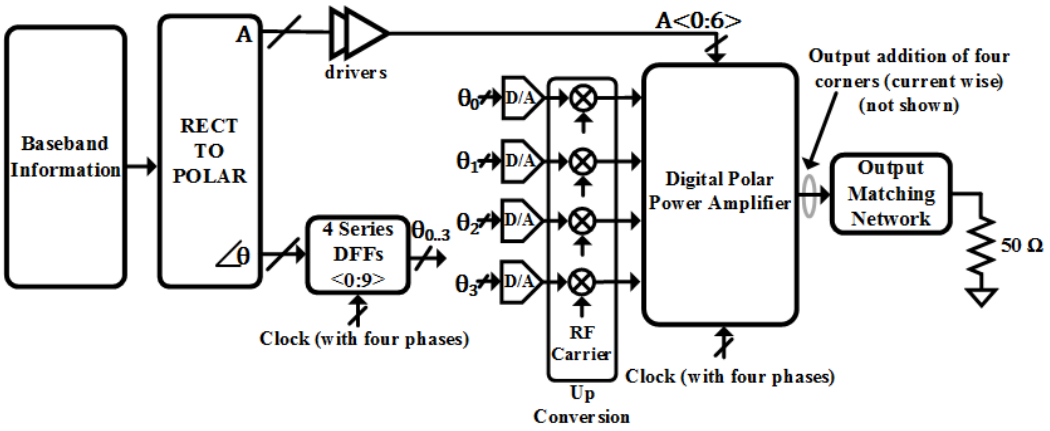


Figure 4.23: Simulation setup for linearly interpolated digital polar power amplifier (single ended version is shown).

corner of the digital polar power amplifier is added current wise (not shown in Fig. 4.23).

4.6.2 Simulation Results

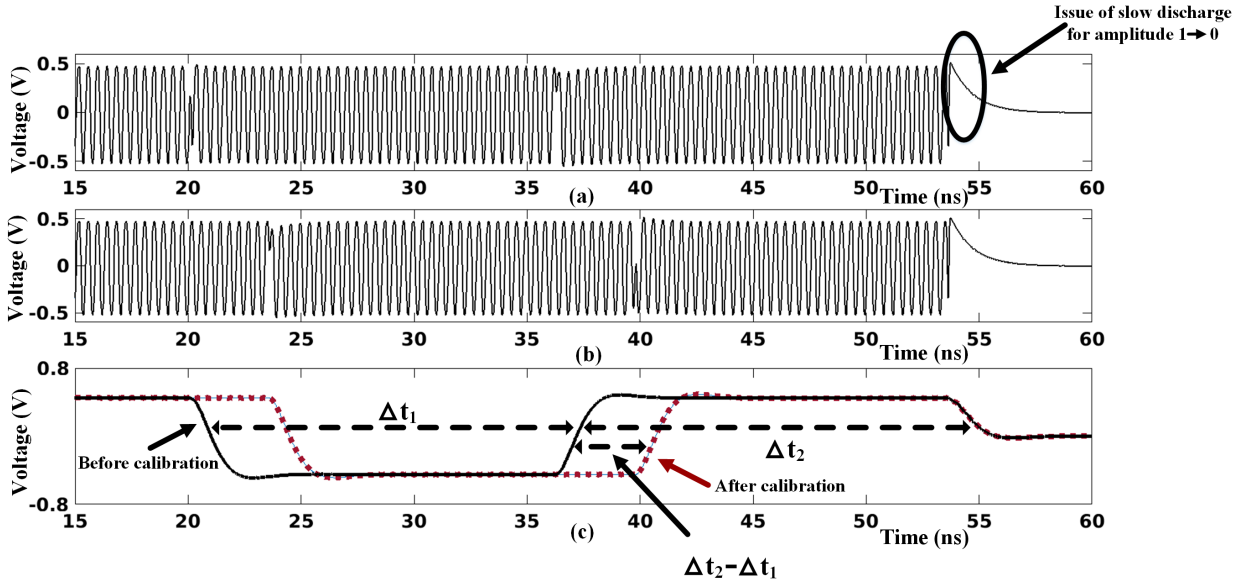


Figure 4.24: Delay mismatch calibration waveform (a) power amplifier output before calibration (b) power amplifier output after calibration (c) low-pass filter output

For the calibration of delay mismatch between amplitude and phase paths, the system is tested with 64-QAM IEEE 802.11n wireless standard with 20 MHz bandwidth at carrier frequency of 2.4 GHz. Here, the input pattern sequence shown in Fig. 4.11a was used. For the purpose of demonstration of calibration scheme, a delay mismatch of 3.5 ns was used for the test case; in practice, this value depends upon the delay added due to DAC, mixer and mismatch in PCB traces between amplitude and phase paths. The RF output of the sub-PA with the delay mismatch is shown in Fig. 4.24a for the input calibration pattern. The output of the low pass filter is shown in Fig. 4.24c. Here, the mismatch between the paths ($\Delta t_2 - \Delta t_1$) is 3.5 ns. With the help of the calibration scheme discussed in Section 4.3, the digital logic enabled a delay in the phase path through digital delay block to match the delay in the amplitude path. After calibration, the RF output of the sub-PA is shown in Fig. 4.24b. In this, phase-to-phase and phase-to-amplitude transitions are equal to Δt_1 as shown in the low pass filter output in Fig. 4.24c. The calibration scheme showed residual error of around 0.5 ns in delay mismatch due to the slow discharge of the sub-PA's RF output for the amplitude movement from 1 to 0.

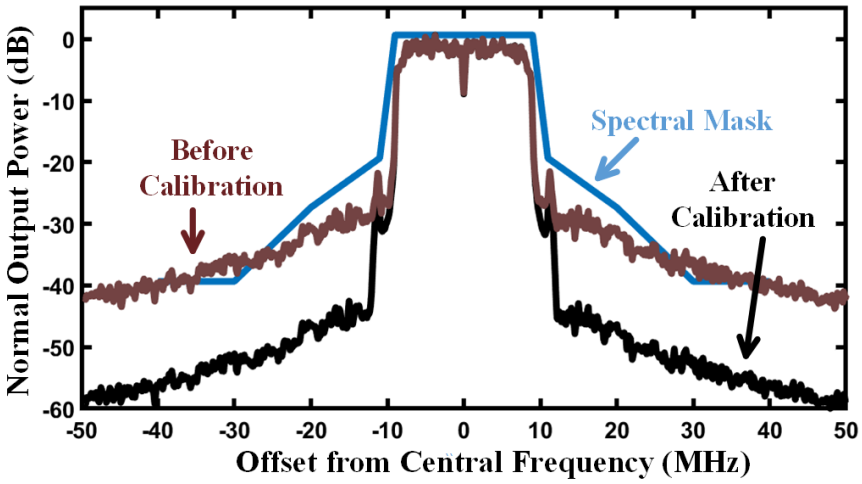


Figure 4.25: Output spectrum for 802.11n 64-QAM OFDM data before and after delay mismatch calibration

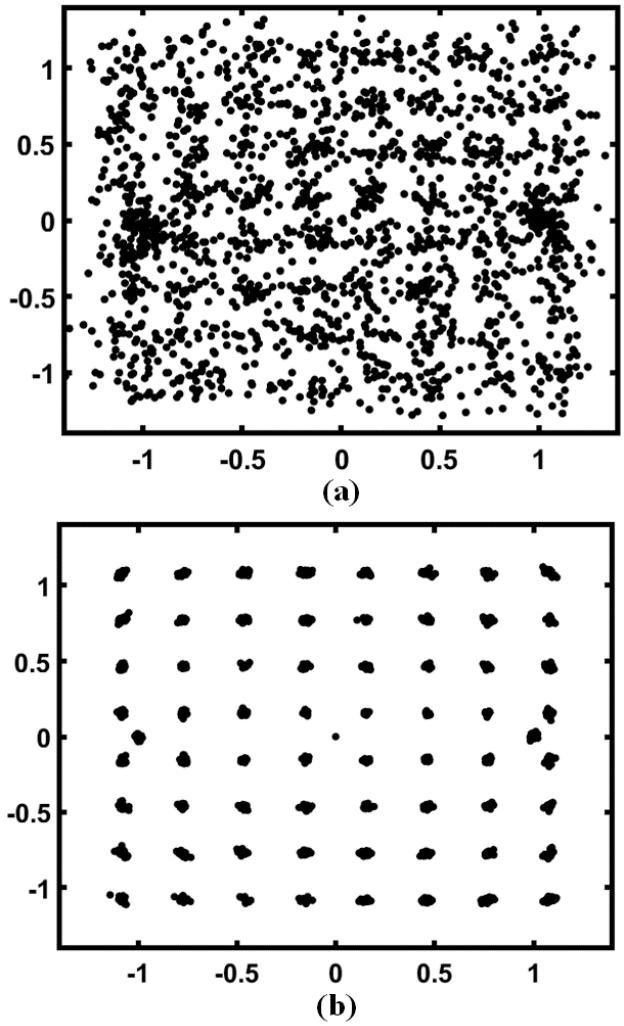


Figure 4.26: EVM for 802.11n 64-QAM OFDM data (a) before delay mismatch calibration (10.67%) (b) after delay mismatch calibration (1.67%)

The performance of the calibration scheme is demonstrated with the help of ACLR and EVM improvement. Before calibration, the ACLR and EVM of the digital polar power amplifier were -28.44 dBc and 10.67%, respectively. After calibration, the ACLR and EVM were improved to -36.01 dBc and 1.67%, respectively. The ACLR and EVM with and without calibration scheme are shown in Fig. 4.25 and 4.26. This calibration can be executed during idle transmission slots. There is no power penalty due to calibration scheme since the calibration addenda are switched off during the normal operation of the transmitter. The usage of the common path (after recombination

of phase and amplitude) for the calibration enabled here to have a robust calibration regarding PVT variations in the calibration addenda.

For the linear interpolation based filtering for spectral images related issue, the output spectrum is shown with and without linear interpolation in Fig. 4.27 and Fig 4.28. The simulated work showed the improvement in the ACPR is around 10 dB. Compared to [19], which is having only amplitude interpolation, the presented work showed far better output spectrum as shown in Fig. 4.28. The table of comparison with state-of-art is shown in Table 4.5. The current simulated result showed better simulated EVM of 2.1% compared to other works. In addition, the average efficiency is 25% which provided a competitive scenario for the state-of-art. The benefits in the power efficiency is due to the switching of driver stage depending upon input amplitude information, which helped to decrease power consumption of the power amplifier.

Ref.	Modulation	Signal BW (MHz)	Frequency (GHz)	P_{SAT} (dBm)	PAE (%)	Avg. Efficiency (%)	ACPR (dBc)	EVM (%)
[124]	802.11g	20	1.5	-	-	14	-	3.5
[92]	WiMax	5	0.8-2	23.5-25.2	40-47	22	-	3.16
[102]	802.11g	20	2.0	24.8	51	24	-	2.82
[19]	802.11g	20	1.56	-	-	6.7	-	4.62
[5]	802.11g	20	2.25	22	44	18	-	3.98
This work	802.11n	20	2.4	27	45	25	-35	2.1

Table 4.5: Performance comparison with state-of-the-art results

Besides the discussed benefits of the linear interpolation of amplitude and phase, the power amplifier have several drawbacks including complexities in layout and PCB design, gain and phase mismatch of interpolated phase paths, three additional requirement of DACs and upconverters for phase interpolation. In addition, the provided power efficiency of the power amplifier did not include the power consumption in CORDIC logic, 40-DFF (used in phase interpolation), four DACs, four mixer, and additional driver (needed in PCB implementation). Among these, only four DACs and four mixers consume around 600 mW (as discussed in Section 4.1) and this degrades the power efficiency from 45% to 29.23%. These drawbacks limit the benefits of the linearly

interpolated digital polar power amplifier. Further research is needed in this work in order to reduce the requirement of additional DACs and upconverters by doing phase interpolation in RF domain.

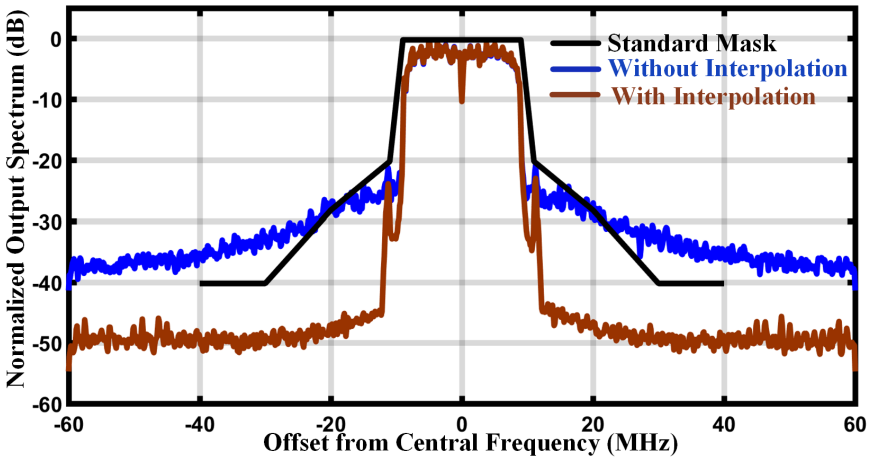


Figure 4.27: Output spectrum with and without interpolation for 802.11n 64-QAM OFDM data

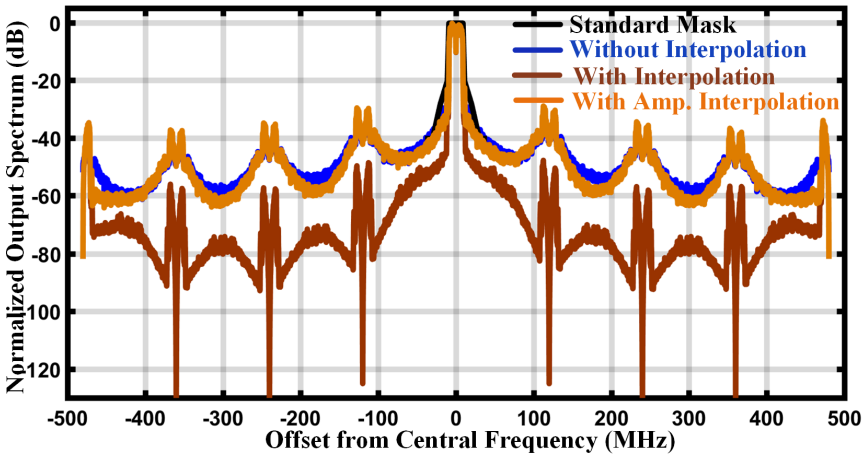


Figure 4.28: Extended output spectrum for 802.11n 64-QAM OFDM data

4.7 Summary

In this chapter, we have proposed a novel calibration scheme for phase and amplitude delay mismatch for the digital polar power amplifier. The chapter also discussed an effective input sequence for the calibration scheme. The presented scheme able to achieve a time alignment between phase and amplitude that satisfied the standard specification for IEEE 802.11n with 20 MHz bandwidth. The calibration is developed to execute during empty transmission slots. For the considered test scenario of the delay mismatch, the proposed scheme showed improvement in ACPR and EVM by 7.57 dB and 84.35%, respectively. In addition, the linear interpolation technique for amplitude and phase was also discussed in this chapter, which showed improvement by 10 dB in ACPR compared to the conventional solution. The power amplifier showed 45% power efficiency at 27 dBm of saturated output power.

5. AN AGILE SUPPLY MODULATOR FOR ENVELOPE TRACKING PURPOSE

5.1 Introduction

With exponential growth in high-level integration and functional density in portable devices, battery run-time has become an instrumental deciding factor for the consumer electronics market. Due to its significant portion in power consumption, the power amplifier (PA) has become a critical component that determines battery run-time in portable devices. Usually, the PA operates at power back-off (PBO) levels, but its efficiency is low at these frequent power levels [16]. To improve power efficiency at PBO levels, the envelope tracking (ET) technique is favored in literature; the main concept is shown in Fig. 5.1 [100]-[125] . An ideal envelope tracking method generates a drain voltage which follows the RF output envelope signal with an operational margin to guarantee PA functionality and to optimize PA efficiency. The power efficiency of the entire PA system is the product of PA efficiency and envelope tracking supply modulator efficiency (5.1) [16], [90], [128]

$$\eta_{PA\_ET} = \eta_{PA} \cdot \eta_{ET\_SM} \tag{5.1}$$

where η_{PA_ET} is the overall system efficiency (including PA and envelope tracking supply modulator) and η_{PA} is the drain efficiency of the power amplifier, and η_{ET_SM} is the efficiency of the envelope tracking supply modulator.

According to (5.1), there is an imperative need for a highly efficient envelope tracking supply modulator for overall system efficiency [90], [129], [21]. Due to high power efficiency, the switching regulator as a supply modulator is preferred in applications where power efficiency is instrumental, e.g., PA systems [16].

For using the regulator with time variant input signals for applications such as envelope tracking systems, the transient response of the regulator determines the envelope's tracking speed. Tracking becomes challenging for high peak-to-average power ratio (PAPR) standards as shown in Fig. 5.1. Here, a safety margin (V_{SM}) on top of the operational margin is needed to provide room

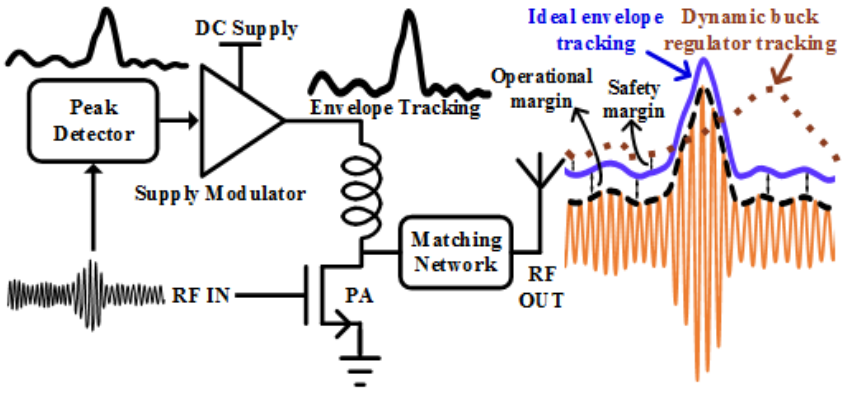


Figure 5.1: Envelope tracking technique for RF PAs

for the voltage ripple and settling error of the switching regulator. The dynamic buck regulator may not be able to follow the RF output envelope signal with needed margins (operational and safety) for a high PAPR system with acceptable power efficiency and switching ripple for wide-band applications [16], [131]. An agile supply modulator is required to accommodate wide band standards. As shown in Table 5.1, the bandwidth of envelope tracking increases with modulation bandwidth, which becomes challenging for a power efficient implementation [16].

Ref.	Modulation	ET Bandwidth
[16]	CDMA IS-95 1.25 MHz	5 MHz
[90]	LTE 16-QAM 5 MHz 7.5 dB PAPR	50 MHz
[89]	LTE 16-QAM 10 MHz 6.44 dB PAPR	72.9 MHz/53.8 MHz

Table 5.1: ET BANDWIDTH FOR DIFFERENT MODULATION SCHEMES

Several techniques have been proposed for high-speed supply modulators including buck, buck-boost, and several combinations of linear with switching amplifiers [100]-[136] as shown in Fig. 5.2. However, considering the high bandwidth of modern wireless standards, the needed high switching frequency penalizes the efficiency of the converter. Compared to a two-phase buck converter, the three-level buck converter solution provides higher bandwidth and smaller current

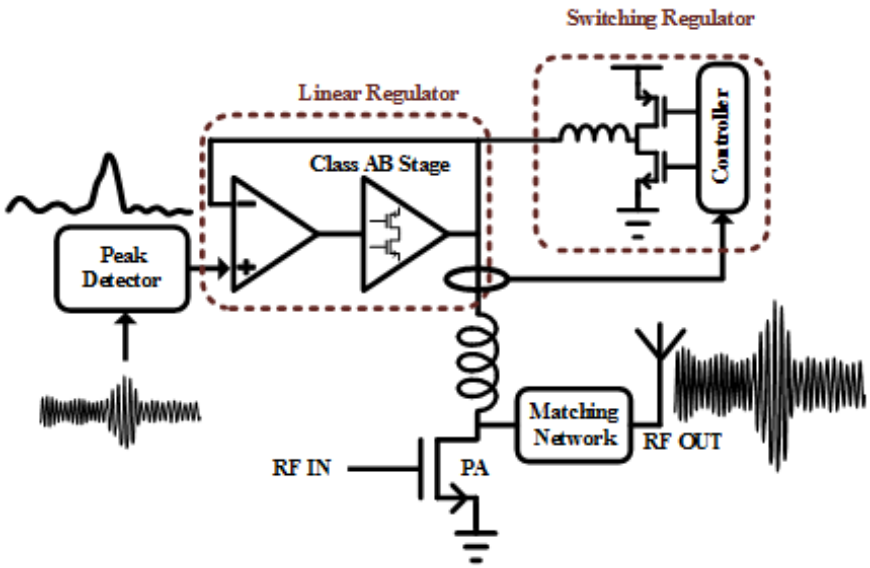


Figure 5.2: Linear Amplifier and switching amplifier combination for envelope tracking.

ripple but with higher conduction loss [137]. To provide highly efficient envelope tracking along with high bandwidth, a switching amplifier with a linear regulator is proposed in [100]-[21], [138]-[143]. The combination has shown good results but comes with increased complexities of control and synchronization [144]. The power efficiency of the combined system might be limited due to poor power efficiency of the linear regulator. Improvement in supply modulator transient response has also been achieved with the help of different compensation networks and switching control solutions [145]-[148]. Some off-chip solutions for improving transient responses of the switching regulator include the use of an auxiliary transformer, inductor, capacitor, diode and higher order filters [137], [149] -[22].

However, it is not practical to have excessive off-chip components in a system where area and cost effectiveness are essential. Hence, in existing work regarding envelope tracking techniques, the tradeoffs are present to provide higher efficiency, wider bandwidth and less complexity. In addition, overshoot has also become an issue due to the downside trend of breakdown voltage in the CMOS technology nodes. The modulator settling time is also an important parameter for proper management of data in highly demanding wireless standards [146].

In this chapter, an agile supply modulator, the bang-bang transient performance enhancer (BBTPE) with a dynamic buck regulator are proposed for envelope tracking purpose in linear PA systems [156]. Here, the approach is to manage slow varying components of an input envelope signal with a power-efficient dynamic buck regulator, and thereby enable BBTPE for fast varying envelope components. The approach alleviates the problem of the transient response of a dynamic buck regulator in terms of rise time, overshoot and settling time. Moreover, to facilitate efficient envelope tracking, the solution presents selective tracking of the envelope signal, wherein the BBTPE helps only in tracking the rising edge of the envelope signal with enough safety margin. With respect to linear amplifier-based approaches, the proposed solution differs in terms of accuracy of tracking and selective tracking, and provides a solution with around 80% power efficiency. This work contributes towards

- Study on the tradeoffs among switching ripple, switching frequency and rise time.
- Study the correlation between overshoot and settling time with rise time improvement.
- Detailed analysis of regions of operation for dynamic buck regulator.
- Demonstration of feasibility of proposed solution via simulation and measurement from low-frequency and RF-frequency prototypes.

The organization of this chapter is as follows. first, envelope tracking with dynamic buck regulator is described along with its regions of operation and design tradeoffs. After this, theoretical aspects of the proposed agile supply modulator architecture is discussed. It is followed by system architecture, implementation, simulation and experimental results.

5.2 Conventional Envelope Tracking

5.2.1 Dynamic Buck Regulator

A simplified architecture of the dynamic buck regulator as an envelope tracker in a wireless transmitter is shown in Fig. 5.3. The regulator is comprised of switches (S_P and S_N), an LC network along with compensation network to ensure loop stability and steady-state precision, and

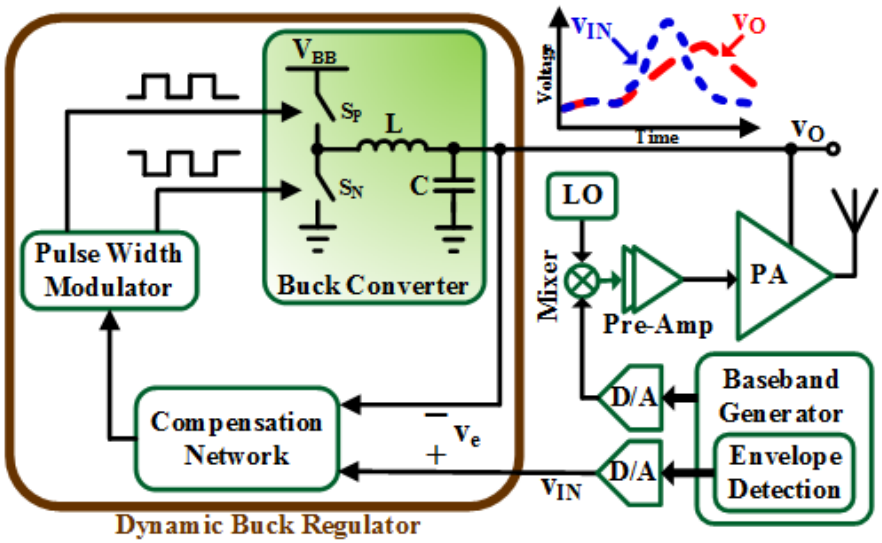


Figure 5.3: Dynamic buck regulator as a supply modulator for envelope tracking in the simplified architecture of a wireless transmitter

a pulse width modulator (PWM) [157]. The PA can be modeled as a load impedance Z_L, which is application dependent [158]. In this work, the input/reference signal v_{IN} stands for the predicted RF output envelope signal added with operational and safety margins. The dynamic buck regulator is also referred to as a conventional solution for envelope tracking.

5.2.2 Regions of Operation

Realization of the regulator intended to serve as an envelope tracking supply modulator comes with the design goals of minimizing switching ripple, overshoot, rise time and settling time, as well as maximizing system power efficiency. The optimization procedure of transient and quasi-steady state performance is not evident since, on one hand, the loop must be agile to track fast and large input signals, but on the other hand, switching ripple and regulator losses must be maintained within specifications. To highlight the design tradeoffs, let us consider the step response of the dynamic buck regulator. For this, the following constraint about compensation network (shown in Fig. 5.3) will be considered.

The compensation network is used to stabilize the loop, and it presents large low-frequency gain with at least one pole at low-frequency, compensating zeros properly located to stabilize the

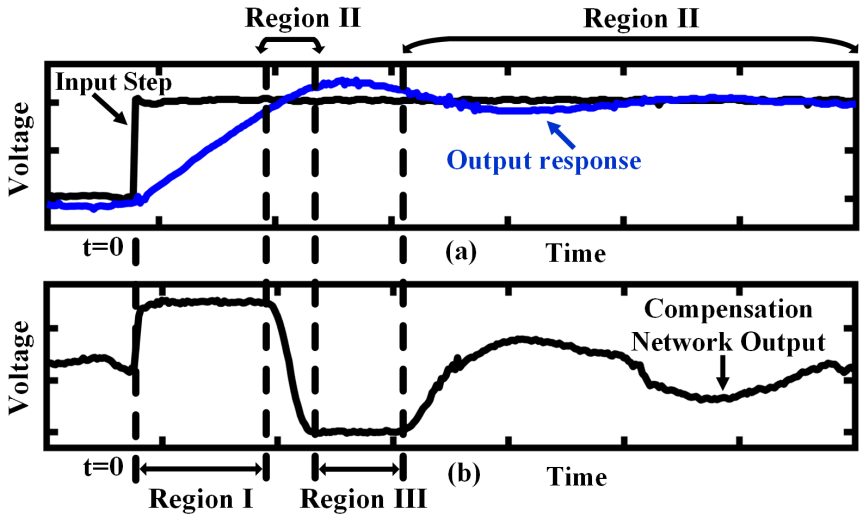


Figure 5.4: Typical measured step response (three regions of operation) of dynamic buck regulator with underdamped loop (a) input voltage and output voltage vs. time, and (b) compensation network output voltage vs. time

regulator loop, and high frequency poles to attenuate high frequency noise. The compensation network usually has a large bandwidth with three main poles and two zeros. Due to the loop's high low-frequency gain and the low bandwidth of the LC filter, the compensation network output saturates if the error signal is large. If that happens, the feedback loop of the regulator is broken, and the LC network operates in an open loop. To facilitate the analysis, let us assume that initially the buck regulator is in a quasi-steady state. Fig. 5.4 shows an example of the input step response of the dynamic buck regulator with an underdamped loop, which corresponds to light load conditions and high loop gain. The different regions of operation during the step response are described as follows.

5.2.2.1 Region I

A large positive input step generates an instantaneous large error signal, i.e., $|v_e| >> 0$. This further moves the active compensation network out of the linear region to the saturation region due to its large gain and wide bandwidth and keeps raising the output voltage v_O towards the input signal as shown in Fig. 5.4. The output of the compensation network through PWM causes the

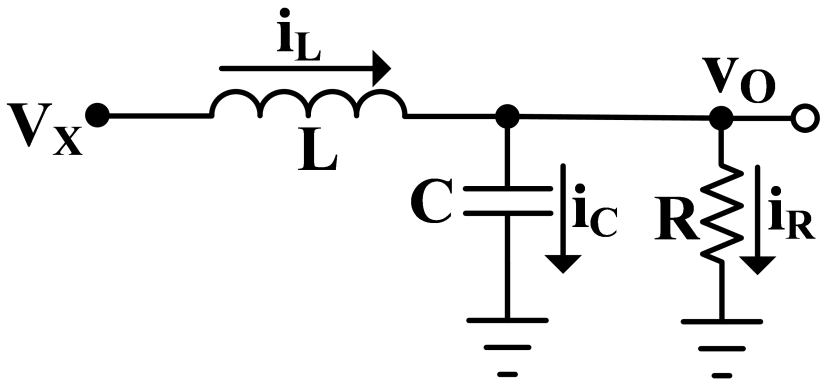


Figure 5.5: Configuration of dynamic buck regulator for Region I ($V_X = V_{BB}$) and Region III ($V_X = GND$)

top switch (S_P) to close and the bottom switch (S_N) to open (Fig. 5.3). The equivalent circuit driving the output is depicted in Fig. 5.5 with $V_x = V_{BB}$, where V_{BB} is the battery voltage. To simplify the analysis, the PA is modeled as a resistive load (R). On average, the current in the inductor is set by the current demanded by load R. Since loop gain is large in a quasi-steady state operation and assuming the voltage ripple is small, the output voltage v_O is set to input voltage v_{IN} before occurrence of the input step (from $v_{IN}(0)$ to $v_{IN,F}$). Therefore, the initial conditions in the inductor and capacitor are: $i_L(0) = v_O(0)/R$, and $v_O(0) = v_{IN}(0)$. After the input step is applied and if the compensation network is saturated, then the output voltage $v_O(t)$ is expressed by (5.2) for $v_O(0) \leq v_O(t) \leq v_{O,F}$ and $R \neq (L/4C)^{0.5}$ [121]. Its derivation in shown in appendix A.

$$v_O(t) = V_{BB}\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + 1\right) - v_O(0)\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + \frac{e^{s_1 t} - e^{s_2 t}}{RC(s_1 - s_2)}\right) + \\ + \frac{i_L(0)}{C(s_1 - s_2)}(e^{s_1 t} - e^{s_2 t}). \tag{5.2}$$

In (5.2), $s_{1,2}$ are the roots of the characteristic equation. Here, $v_{O,F}$ is the final steady-state output voltage. With the help of (5.2), the response of the regulator to fast transitions in the input envelope signal from the back-off level to the peak power level is characterized by the rise time

(t_{rise}). Due to the complexity of the solution for output voltage $v_O(t)$ in (5.2), the explicit solution for the rise time is even more complex, which makes it difficult to get any insight. Therefore, a numeric solver is used to find the value of t_{rise} from (5.2) for given parameters. Before discussing the results, let us replace L and C in (5.2) by voltage ripple (Δv_O), inductor current ripple (Δi_L) and switching frequency (f_{sw}) with the help of (5.3) and (5.4) so that tradeoffs among different performances and design parameters can be discussed [157].

$$\Delta v_O = \frac{(1-D)V_O}{(16LCf_{sw}^2)} \tag{5.3}$$

$$\Delta i_L = \frac{R(1-D)I_L}{(2Lf_{sw})} \tag{5.4}$$

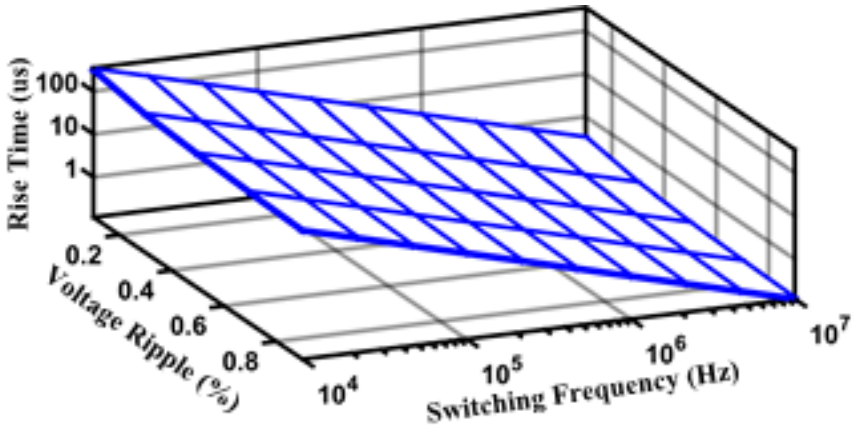


Figure 5.6: Rise time versus voltage ripple and switching frequency at 15% current ripple

In (5.3) and (5.4), $D(= V_O/V_{BB})$ represents the duty cycle, V_O is the average output voltage in quasi steady state, and I_L is the average inductor current. Here, rise time (t_{rise}) is assessed by measuring the 10% to 90% rise of the regulator output voltage. For an input step of 0.5 V-1.5 V and battery voltage V_{BB} of 4.4 V, the rise time versus voltage ripple, and switching frequency is plotted in Fig. 5.6 for 15% inductor current ripple, and the load impedance of 1 Ω. The analysis does not include switch S_P resistance or its turn-on time, which further worsens output voltage

rise time.

As shown in Fig. 5.6, increment of voltage ripple, keeping fixed switching frequency and current ripple, slightly decreases the regulator's rise time. This can also be analyzed as the increment in voltage ripple allows a decrease in capacitance of the LC tank, thereby moving the roots of characteristic equation away from imaginary axis on left hand-side (LHS) side of s-plane i.e. increasing the speed of response. However, voltage ripple is constrained by the safety margin hence efficiency of the system. The rise time also decreases with increment in switching frequency at fixed voltage and current ripple. These conditions from using (5.3) and (5.4) require a decrease in both L and C, which are inversely proportional to the switching frequency increment thereby increasing the bandwidth. However, increment in switching frequency causes higher switching losses; therefore, this approach is limited by the power efficiency of the buck converter. A similar trade-off of rise time versus voltage ripple and switching frequency is shown in Table 5.2 and 5.3. These are derived from an LTspice based non-ideal simulation environment. Table 5.2 is evaluated at 15% current ripple and $100\ kHz$ switching frequency, and Table 5.3 is assessed at 0.4% voltage ripple and 15% current ripple.

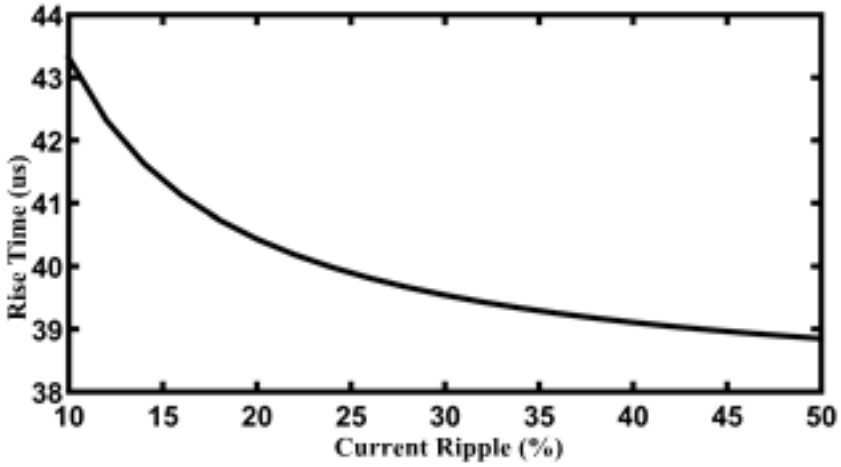


Figure 5.7: Output voltage rise time versus current ripple for 0.25% voltage ripple, 50 kHz switching frequency

As shown in Fig. 5.7, rise time decreases with increment in current ripple for given voltage ripple and switching frequency. Equations (5.3) and (5.4) suggest that this can be achieved by decreasing the inductance, which increases the modulator's bandwidth. However, current ripple is constrained by the current limit of the inductor and semiconductor devices. Therefore, maximum allowed values of voltage ripple, current ripple and switching frequency-all serve to constrain output voltage rise time.

Voltage ripple (%)	Rise time (μs)
0.26	24.95
0.38	17.44
0.51	14.92
0.77	12.73
0.94	11.59

Table 5.2: RISE TIME (t_{rise}) VARIATION WITH VOLTAGE RIPPLE

Switching frequency (Hz)	Rise time (μs)
10k	172.4
100k	17.44
1M	1.73
10M	0.17

Table 5.3: RISE TIME (t_{rise}) VARIATION WITH SWITCHING FREQUENCY

5.2.2.2 Region II

When the regulator's output voltage approaches the input voltage, the error voltage decreases, $|v_e| \approx 0$ and forces the compensation network to enter into its linear region (Region II) as shown in Fig. 5.4, which again enables the linear operation of the regulator loop. The system configuration for this region is shown as a dynamic buck regulator in Fig. 5.3. In this stage, if the inductor current is close to the current demanded by the load, and the loop damping factor is not quite small

enough, the regulator's output voltage smoothly settles down depending upon linearized response of the loop, i.e., transfer function as shown in (5.5)

$$H(s) = \frac{V_O(s)}{V_{IN}(s)} = \frac{H_{comp}(s)H_{PWM}(s)H_P(s)}{1 + H_{comp}(s)H_{PWM}(s)H_P(s)} \tag{5.5}$$

where $H_{comp}(s)$ is the transfer function of the compensation network. $H_{PWM}(s)$ is the equivalent transfer function of the pulse width modulator ($= 1/V_M$), where V_M is the peak-to-peak amplitude of the sawtooth waveform [157]. $H_P(s)$ is the transfer function of the power stage that contains the LC filter along with load (R), which is equal to $V_{BB}/(s^2LC + sL/R + 1)$ [121].

If the inductor current in this region is excessive (i.e., underdamped RLC network), the output voltage moves further away from the input voltage; then, the regulator enters into Region III as shown in Fig. 5.4.

5.2.2.3 Region III

In this region, at the starting point, the output voltage increases due to excessive inductor current, and this again saturates the compensation network as shown in Fig. 5.4. Through PWM, it closes switch S_N and opens switch S_P as depicted in Fig. 5.5 with $V_x = GND$. The governing equation of the output voltage, the inductor current and load current for this region can be derived from (5.2) by substituting $V_{BB} = 0$ and corresponding initial conditions. In this region, the inductor current starts decreasing until it reaches the value of the load current, which creates a maxima condition for output voltage $v_O(t)$. Hence, the overshoot of the output voltage occurs in this region. The value of the overshoot depends upon the dynamics of the region and its initial conditions. The damping factor (ξ) of the LCR network shown in Fig. 5.5 increases with increments in inductance value, which decreases the overshoot [157]. However, (5.4) indicates that it also decreases current ripple, which worsens rise time during Region I as shown in Fig. 5.7. The damping factor can also be increased by decreasing capacitance; however, (5.3) suggests that it also increases voltage ripple.

Therefore, Region I is mainly responsible for rise time. The existing tradeoffs makes it infeasi-

ble for a dynamic buck regulator to manage specifications of instrumental performance parameters like switching ripple and power efficiency, along with needed rise time. Furthermore, Region III is responsible for overshoot, while final settling depends on loop dynamics in Region II. In the current work, without loss of generality, it is assumed that the input step puts the regulator system into region transitions I$\rightarrow$ II $\rightarrow$ III $\rightarrow$ II before it settles down. For large overshoot cases, Region II operation between Region I and III can be ignored; hence, overall movement of the regions is simplified to I$\rightarrow$III$\rightarrow$II.

5.3 Agile Supply Modulator for Efficient Envelope Tracking

Most modern wireless standards require PAPR over $12\ dB$; this sometimes can be clipped within linearity specifications up to a PAPR of $7 \sim 8\ dB$ depending upon the standard. Furthermore, the peak of probability density function of transmitter power is around the PBO region, which means that most of the time, the signal is around 25% of the peak value [16], [158]. Due to PDF distribution, a sharp transition in the envelope signal from PBO to the peak power region is not frequent. However, these conditions have to be properly managed by both the PA and supply modulator to avoid distortion. Furthermore, increasing the switching frequency of the dynamic buck regulator (as suggested in Fig. 5.6) for managing fast signal transition, which has a low probability of occurrence, is not a power-efficient approach. The proposed solution takes advantage of this property.

5.3.1 Core Concept

According to (5.2), with the exception of the passive elements, output voltage, and hence, the subsequent rise time, is a function of battery voltage V_{BB}, initial output voltage $v_O(0)$, and initial inductor current $i_L(0)$.

An intuition about the impact of these parameters on the average speed of an output signal can be realized using a circuit configuration as shown in Fig. 5.5; in which an increment of V_{BB} increases the voltage difference across inductor L; hence the inductor provides more current during rise time, which increases output voltage speed. On the other hand, the increment of $v_O(0)$

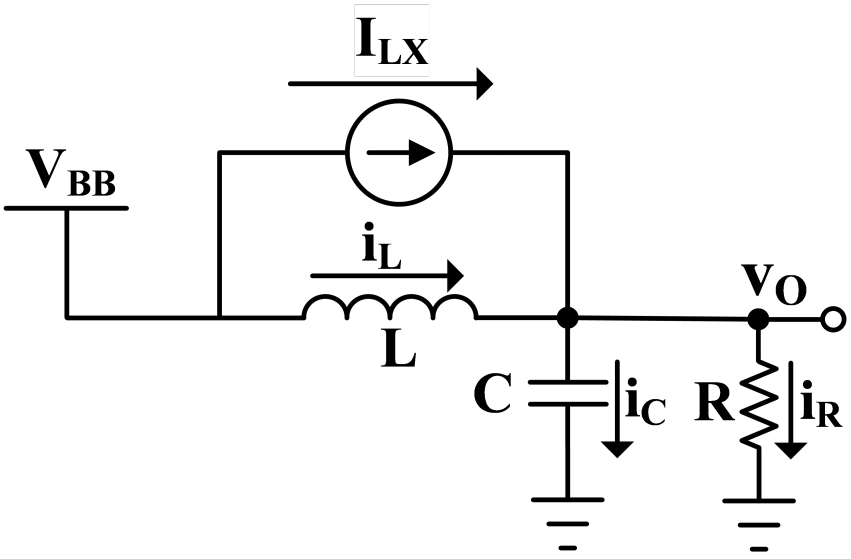


Figure 5.8: Conceptual schematic for manipulation of initial inductor current during Region I in proposed solution

decreases the voltage drop across inductor ($V_X - v_O$), thereby decreasing the inductor current. The increment of $i_L(0)$ also enhances rise time by providing more current to capacitor C and load R. In these parameters, $v_O(0)$ is determined by the initial condition of the input signal. Additionally, V_{BB} is a technology-constrained parameter, so it cannot be manipulated. Similarly, the initial inductance current $i_L(0)$ is determined by the average current demanded by the load before the transient. One of the main reasons for the limited rise time of output voltage is the slow change in inductor current, which is dictated by the integral of the voltage difference across its terminals and its inductance value. The proposed technique is based on the manipulation of the current injection to the load that emulates the effect of the higher initial inductor current when needed as shown in the conceptual diagram of Fig. 5.8. The auxiliary current source (I_{LX}) is placed parallel to the inductor, and represents the manipulation in the initial inductor current while the system operates in Region I. The output voltage for this region is expressed as (5.2) by adding the I_{LX} term with $i_L(0)$ in the last term. Fig. 5.9 shows the modulator output voltage versus time for I_{LX} variation by 0, 100%, 300% and 500% of the initial inductor current $i_L(0)$ for Region I. The figure shows that

output voltage is raising faster due to the contribution of I_{LX}. As shown in Fig. 5.9, $I_{LX} = 5 \cdot i_L(0)$ reduces rise time by a factor of 1.5 for the considered test configuration. The figure of improvement in rise time becomes more pronounced for an overdamped system, and mostly driven by I_{LX}/C when the current of the auxiliary current source exceeds the inductor current.

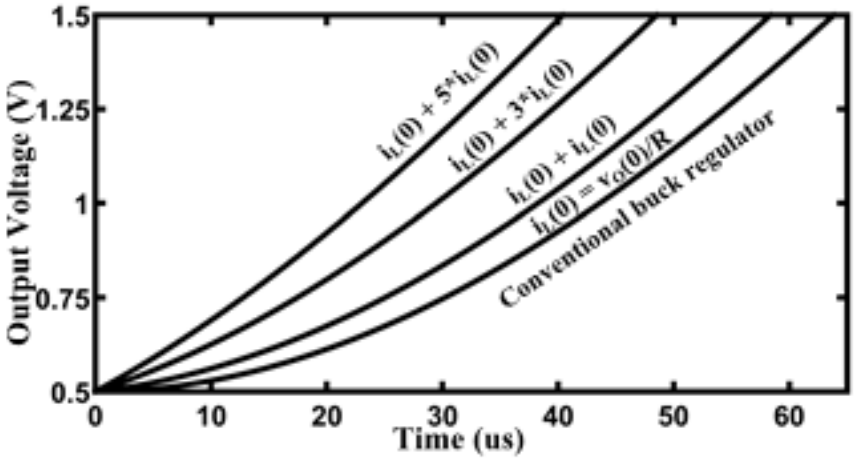


Figure 5.9: Output voltage during rise time (Region I) vs. time for different initial inductor current with input step of 0.5 V to 1.5 V

5.3.2 Analysis of Transient Performance, Stability and Power Efficiency

During Region I, the auxiliary current source I_{LX} helps to increase output voltage v_O faster than that with the conventional dynamic buck regulator-solution. This decreases the voltage difference across inductor Δv_L more quickly and reduces the time spent in Region I ($t_{regionI}$) in comparison to the conventional solution. It leads to a decrease in the excessive rising current in the inductor during Region I.

After Region I, the system enters into Region III, ignoring interim Region II since it is a reasonable assumption for high overshoot cases. Thus, the initial inductor current for Region III is smaller for the regulator having an auxiliary current source (I_{LX} during Region I) than that for the conventional dynamic buck regulator. Since I_{LX} is only used in Region I, system configuration for

Region III is the same as that of the dynamic buck regulator shown in Fig. 5.5 with $V_X = GND$. Considering the worst case for overshoot and settling time, which occurs in underdamped configurations of the LCR network, i.e., $R > (L/4C)^{0.5}$, the governing equation of the output voltage for Region III, i.e., $v_O(t) > v_{O,F}$, which starts at $t = t_3$ is shown in (5.6), which is derived from (5.2) by removing the V_{BB} terms as for this region $V_x = GND$.

$$v_O(t) = \frac{e^{\frac{t-t_3}{2RC}}}{\omega_d}\left(v_O(t_3)\Big\{-\frac{1}{2RC}sin(\omega_d(t-t_3)) + \omega_d cos(\omega_d(t-t_3))\Big\} + \frac{i_L(t_3)}{C}sin(\omega_d(t-t_3))\right) \tag{5.6}$$

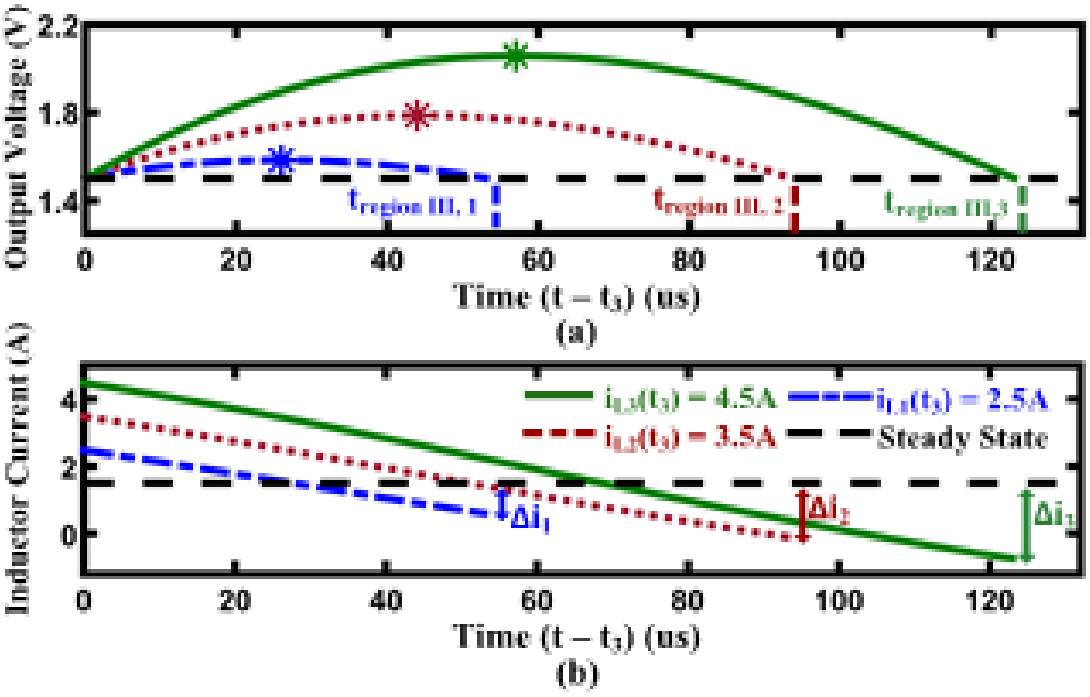


Figure 5.10: Region III waveform for different initial inductor currents (4.5 A, 3.5 A, and 2.5 A) (a) output voltage vs. time and (b) inductor current vs. time

where the ringing frequency ω_d is $\sqrt{(1/LC) - (1/2RC)^2}$. The equation is plotted for different values of the initial inductor current $i_L(t_3)$ in Fig. 5.10a. The figure shows that overshoot increases

with increment in the initial inductor current $i_L(t_3)$. Intuition for this comes from its last term, which is $(i_L(t_3)/C)sin(\omega_d(t-t_3))$, as its amplitude is increasing with i_L (t_3), i.e., increasing overshoot. Therefore, in accordance with these results, it is evident that the dynamic buck regulator with an auxiliary current source during Region I has a smaller overshoot than that in case of the conventional dynamic buck regulator due to the smaller inductor current at the end of the Region I.

Comparison of settling time can be done region wise; i.e., input step transition to output steady state that includes region transition from $I \rightarrow III \rightarrow II$, assuming only these transitions are needed to settle down the system. Due to the use of I_{LX} in Region I, time spent and inductor current in Region I by the proposed system is less than that in the dynamic buck regulator system. As shown in Fig. 5.10a, time spent in Region III ($t_{regionIII}$) is higher for the higher value of the initial inductor current; i.e., $t_{regionIII,3} > t_{regionIII,2} > t_{regionIII,1}$ for i_{L3} $(t_3) > i_{L2}(t_3) > i_{L1}(t_3)$. This shows that time spent in Region III is smaller for the proposed system than that spent in the dynamic buck regulator system.

The inductor current during Region III for $R > (L/4C)^{0.5}$ can be obtained from adding a capacitor current and load current of the circuit shown in Fig. 5.5 [121]. Its derivation in shown in appendix B. It is plotted for different values of initial inductor current $i_L(t_3)$ in Fig. 5.10b. At the end of Region III, the figure shows that initial deviation of inductor current from steady state for Region II increases with increment in the initial inductor current in Region III, i.e., $\Delta i_3 > \Delta i_2 > \Delta i_1$ for $i_{L3}(t_3) > i_{L2}(t_3) > i_{L1}(t_3)$. Therefore, settling time in Region II is smaller for the proposed solution than that for the dynamic buck regulator because the conventional regulator starts with a higher deviation in the inductor current. Consequently, settling time in the case of a proposed agile supply modulator is smaller than that in the conventional solution.

Even though settling time is improved in the proposed solution, the key issue is that the linear PA drain voltage must be greater than the minimum required voltage to stay in its linear operation. The time needed to make a linear PA operational is estimated by the time after which the modulator output voltage is greater than the minimum needed PA drain voltage, i.e., $v_{IN} - v_O \leq V_{SM}$, which

is the effective settling time for linear PAs ($t_{s,eff}$). Table 5.4 shows that both effective settling time $t_{s,eff}$ and overshoot voltage (V_{ov}) decrease with increment in I_{LX} for V_{SM} 50 mV. As soon as the voltage undershoot becomes smaller than V_{SM}, the $t_{s,eff}$ moves to Region I and decreases drastically as shown in the table.

$\frac{I_{LX}}{i_L(0)}$	$\frac{t_{s,eff}}{t_{s,eff,conventional}}$	$\frac{V_{ov}}{V_{ov,conventional}}$
0 (conventional system)	1	1
1	0.94	0.83
3	0.17	0.54
5	0.14	0.16

Table 5.4: $t_{s,eff}$ AND V_{vo} VARIATION WITH AUXILIARY CURRENT

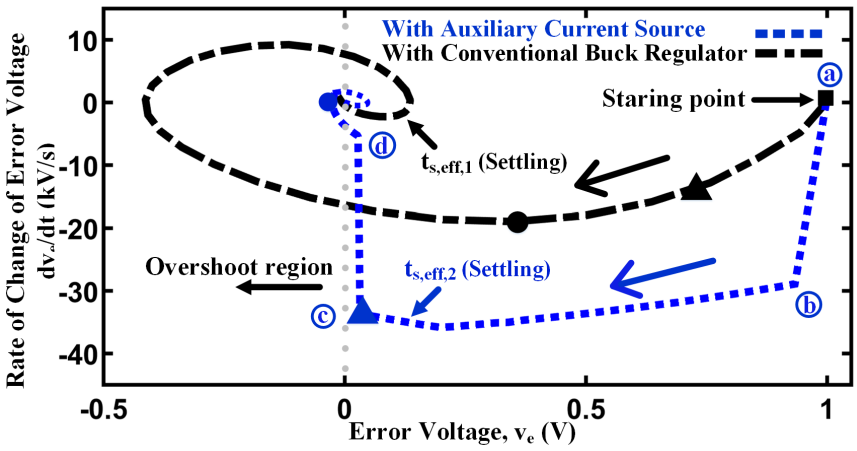


Figure 5.11: Rate of error voltage vs error voltage of a simulated system with and without auxiliary current source $I_{LX}(4A)$ in Region I with input signal step from 0.5 V to 1.5 V for buck converter designed with $L = 45.2\ \mu H$, $C = 142.5\ \mu F$, $R = 1\ \Omega$ and $V_{BB} = 4.4\ V$ at 50 kHz switching frequency. Here, time mapping symbols ■▲●, $t_{s,eff,1}$, and $t_{s,eff,2}$ represent 0, 30, 50, 250 and 27 μs respectively.

The discussed reduction in overshoot and the effective settling time is illustrated with the help of the phase portraits displayed in Fig. 5.11, which show the rate of change of the error voltage,

dv_e/dt vs. error voltage v_e, for an input step from 0.5 V to 1.5 V. It is developed with the derivative function and interchanges of axes of time-domain waveforms. As shown, the auxiliary source is turning on from point (a) to (b); the error voltage does not change immediately, but it drastically increases the rate of change of error. From (b) to (c), it quickly decreases error voltage v_e. After assisting the output voltage by quickly reducing the error signal, i.e., $|v_e| \approx 0$, the auxiliary current source I_{LX} turns off, which results in the jump from (c) to (d). After that, the velocity of the error signal decreases since it is managed by the inductor current only, which leads to a softer convergence towards its final steady state. For corresponding time instances (■▲●), the conventional system shows more error voltage than that in proposed system as shown in Fig. 5.11. In this case, simulation results show reduction in both voltage overshoot and effective settling time for about 90%.

The BBTPE is only active during Region I; however, during this region, the feedback loop of the regulator is broken due to saturation of the compensation network. Hence, the BBTPE does not participate in the closed-loop linear stability analysis. For the system during Region II, the closed loop transfer function is still governed by (5.5). Impact of the auxiliary current source on the modulator's power efficiency depends upon the input signal slew rate. If the input signal slew rate is within the buck regulator's tracking speed, the auxiliary source is not activated, and the power efficiency will be governed by the regulator itself. Furthermore, in modern modulation schemes, the transition from PBO to the peak power level is not frequent, so the power delivered by the auxiliary current source will be minimal compared with the average modulator's output power.

5.4 System Architecture, Implementation, and Experimental Results

5.4.1 System Architecture

The auxiliary switchable current source I_{LX} can be treated as an addendum in the system beside the dynamic buck regulator during Region I. For this purpose, a fast threshold voltage detector (bang-bang controller) that monitors the error signal v_e is used in the proposed agile supply modulator architecture as shown in Fig. 5.12. It activates the switchable current source

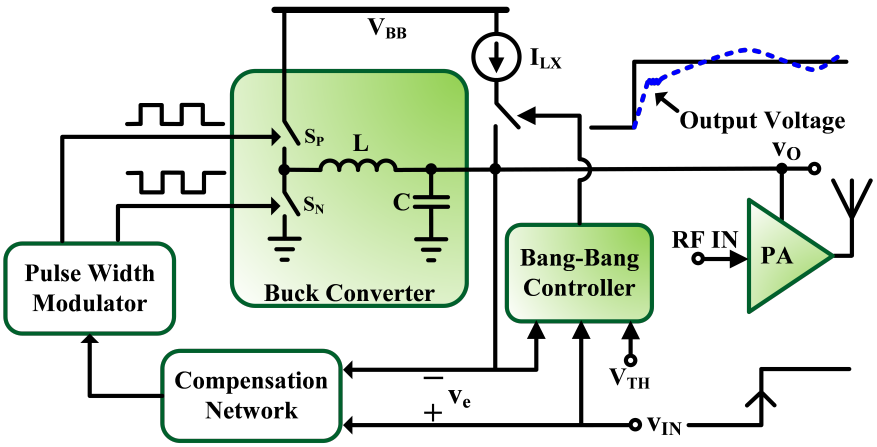


Figure 5.12: Proposed agile supply modulator architecture for envelope tracking

I_{LX} if the aforementioned error signal v_e is larger than the predefined safety margin voltage V_{SM} in Region I. As a consequence, the auxiliary switchable current source I_{LX} works as a bang-bang (ON-OFF) current source (BBCS) because it is activated only when the error voltage is greater than V_{SM}. Because the added BBCS along with its controller enhances the transient performance of the proposed agile supply modulator, it is referred to as a bang-bang transient performance enhancer (BBTPE). The value of I_{LX} is decided based upon the needed rise time. In addition, the value of V_{SM} is the allowed safety margin between the input voltage and modulator output voltage; it limits BBCS operation. The margin must be greater than the voltage ripple Δv_0 along with a settling error of the dynamic buck regulator so that a minimum steady state output voltage is greater than the minimum drain supply needed for PA to be operational. In addition, a delay by the bang-bang controller in disabling the BBCS will impact efficiency, but not PA linearity. Although a simple threshold detector is used in this prototype, more complex algorithms can be used, which may even consider the use of a predictor to anticipate fast input signal variations that can activate the BBCS in advance.

The added module BBTPE helps the dynamic buck regulator to only follow the rising edge of the envelope signal for linear PAs. During the sharp falling edge, the response of the proposed agile modulator is identical to that of a conventional modulator. For a linear PA, the drain voltage

only needs to be large enough to maintain its functionality; it does not need to follow the envelope signal during the input falling edge. In this case, the system uses the stored energy of the inductor and capacitor accumulated during the preceding operation. Moreover, in order to track the falling edge of the input signal (envelope signal), the stored energy in the capacitor and inductor of the buck converter needs to be depleted, which results in the loss of efficiency for the system (supply modulator and power amplifier) because the energy was already taken from the supply during the rising edge of the input signal and stored in the inductor and capacitor. The best solution in the case of linear PAs, that are low sensitive to drain voltage variations, is to keep the additional energy stored in the inductor and capacitor and let the PA to use it. The result is that during fast falling variations, the drain voltage remains higher than minimum needed voltage headroom for its operation. Therefore, selective tracking is an efficient and simplified approach without affecting the linear PA's functionality.

5.4.2 A Low-Frequency System Implementation and Setup

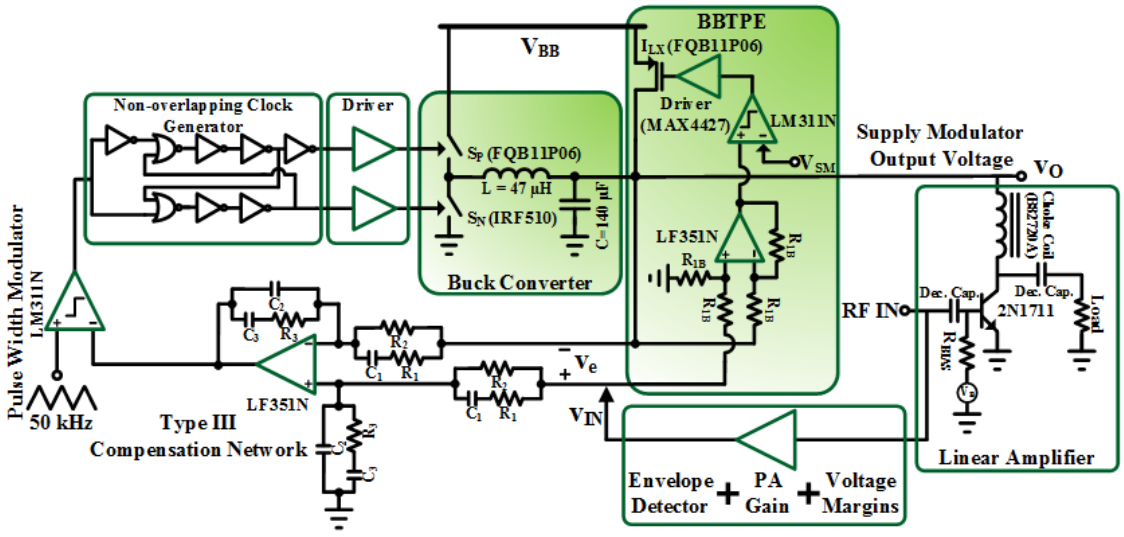


Figure 5.13: Low-Frequency Discrete Implementation Setup

In order to verify the proposed supply modulator, a discrete components-based prototype was

designed as proof of concept. Due to the limitation of the frequency response of discrete components, the frequency of operation was limited to $50\ kHz$ in system testing. The discrete implementation setup of the employed system is shown in Fig. 5.13. The dynamic buck regulator was designed for 15% of the current ripple and 0.25% of the voltage ripple with a switching frequency of $50\ kHz$, and a loop bandwidth of $7.9\ kHz$. $LC's$ Corner frequency was used at $1.96\ kHz$ using $L = 47\ \mu H$ and $C = 140\ \mu F$. A Type III compensation network was designed to provide high low-frequency gain and stability with poles at 0, $50kHz$, and $100\ kHz$, and two zeros around $2.7\ kHz$. Furthermore, the switches S_P and S_N were realized with FQB11P06 and IRF510, respectively. The driver of these switches was designed using MAX4427. The PWM modulator employs a $50\ kHz$ clock frequency. The non-overlapping clock circuit for the present system is a typical circuit as shown in Fig. 5.13. In this implementation, BBTPE has three modules: an error signal generator, a bang-bang controller, and the BBCS. The error signal generator was implemented with the help of an op-amp based subtractor, and the controller was realized employing a conventional voltage comparator. In the present prototype version, the BBCS is implemented with a single PMOS device (FQB11P06). To maintain it as a current source, voltage levels at the gate, drain, and source of the device are managed such that the device is in the saturation region while operating in Region I. The PA was modeled as a resistive load to the modulator. For linearity testing, a linear amplifier is used as a load to the supply modulator as shown in Fig. 5.13. The used discrete components are listed in Table 5.5. Here, the envelope detector was realized using a textbook circuit employing an opamp, diode, and resistor. The measurement setup of the system is presented in Fig. 5.14.

5.4.3 RF-Frequency System Implementation and Simulation Setup

To justify achievable modulation speed with the presented approach, the proposed supply modulator was also designed using TSMC 40nm and tested with WLAN standard IEEE 802.11n which has a bandwidth of $20\ MHz$ at carrier frequency of $2.4\ GHz$. In the circuit implementation, a dynamic buck regulator with conventional architecture consists of a compensation network, a PWM, a non-overlapping clock circuit, switches, and its driver along with an inductor and a ca-

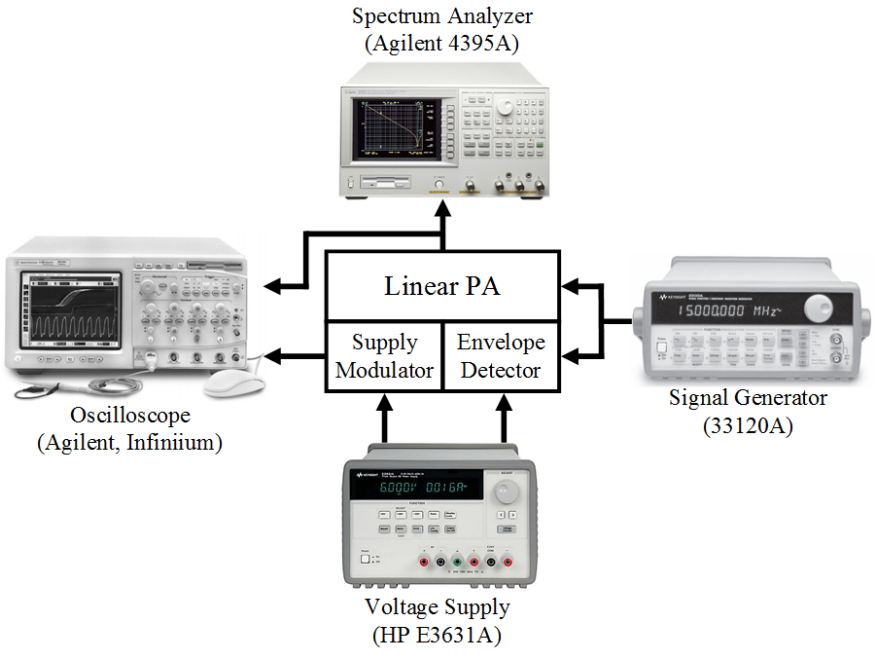


Figure 5.14: Low-Frequency Measurement Setup

Blocks	Part #
N-Switch	IRF510
P-Switch, BBCS	FQB11P06
Inductor	47 μH (WE 7443634700)
Capacitor	Electrolytic Capacitor 140 μF
Driver	MAX4427
PWM modulator	LM311N
Compensation Network	LF351N
Bang-Bang Controller	LF351N
Choke Coil	B82720A
Linear Amplifier	2N1711

Table 5.5: Discrete implementation setup part #

pacitor. A typical folded-cascode opamp was used in the compensation network. The compensation network, which was Type III, had zeros at 0.37 and 0.4 MHz, and poles at 0, 7.5, and 15 MHz. The PWM clock frequency was set at 7 MHz. The size of the switches S_P and S_N were 40.55 $mm/460$ nm and 13.98 $mm/550$ nm, respectively. The inductor and capacitor values are 13.75 μH, and 21.12 nF, respectively. The dc gain, unity gain frequency, and phase margin of

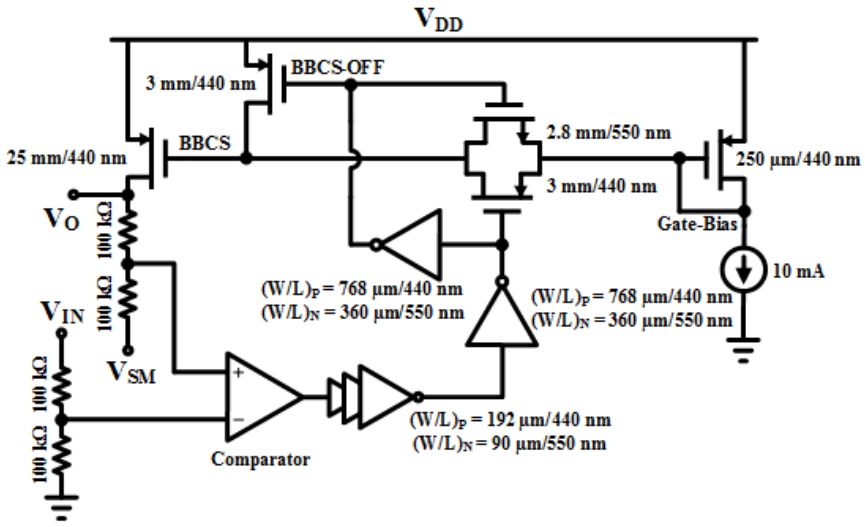


Figure 5.15: BBTPE Circuit

the regulator loop were $53\ dB$, $1.8\ MHz$ and $60°$, respectively. The circuit diagram of BBTPE is shown in Fig. 5.15. In the circuit, the comparator compares input voltage v_{IN} and output voltage v_O along with safety margin (V_{SM}) with the help of a resistive adder. If the difference between output voltage and input voltage, i.e., error voltage is greater than V_{SM}, then, the transmission gate gets enabled and it bias BBCS with a generated gate-bias. Furthermore, if the error voltage is below the safety margin; then, the BBCS-OFF transistor gets enabled and the switch-off BBCS. Due to the dynamic nature of the OFDM signal, the need for a hysteresis comparator was not observed. However, frequent switching of BBCS can be reduced to some extent with the adoption of a hysteresis comparator. The used supply for the BBTPE was 3.3 V. The slew rate of the BBTPE needs to be faster than that of the envelope signal to meet a particular standard. For a $25\ dBm$ output power using WLAN standard IEEE 802.11n with $20\ MHz$ bandwidth, the slew rate of the envelope peak transition is $\sim 13\ V/us$ which is much faster for the rest all other time constants embedded in the dynamic buck regulator; the BBTPE shows the slew rate of $15.4\ V/\mu s$.

The linear power amplifier was having a cascode configuration [158]. The sizes of the bottom and cascode transistor were set as $5\ \mu m/60\ nm$ and $20\ \mu m/270\ nm$, respectively, with 6144 fingers. The effective loads to the linear amplifier is $4/3\ \Omega$. The impedance transformation was

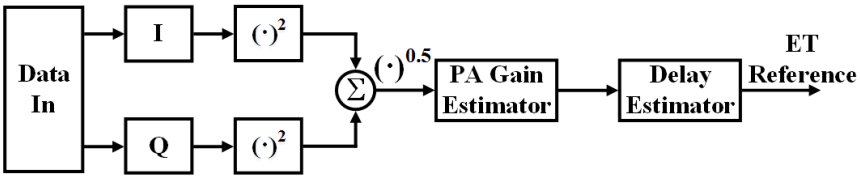


Figure 5.16: Envelope tracking input setup for simulation

achieved with the help of a cascaded L-matching network ($0.37\ nH$, $11.25\ pF$, $1.64\ nH$ and $1.33\ pF$). For simulation purposes, the envelope tracking input was obtained using a direct operation on the baseband signal. The implemented block diagram of the operation is shown in Fig. 5.16. The PA gain and path delay were obtained through characterization of PA. In practice, the envelope is generated in a digital domain (baseband processor) and its delay is equated with an in-phase (I) and quadrature (Q) baseband signal [100].

5.5 RF-Frequency System Implementation and Measurement Setup

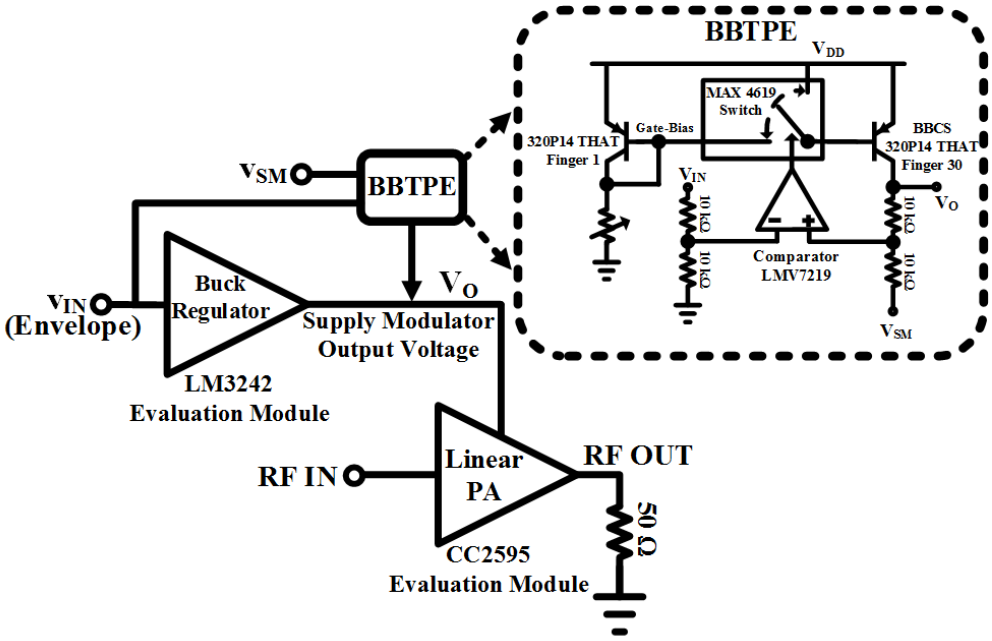


Figure 5.17: RF Frequency Implementation Setup

An RF-frequency prototype was implemented as a proof of concept. The system was designed for the LTE 16-QAM with $5\ MHz$ bandwidth at the RF frequency of $2.4\ GHz$. The implemented system setup is shown in Fig. 5.17. The dynamic buck regulator was implemented using the LM3242 evaluation board which has a PWM frequency of $6\ MHz$ with a $0.5\ \mu H$ inductance and $0.47\ \mu F$ capacitance. The linear power amplifier was employed with a CC2595 evaluation board. This is a two-stage power amplifier with an L-type matching network implemented with $1.2\ nH$ inductance and $1.5\ pF$ capacitance. Its supply is connected to the supply modulator via a $12\ nH$ choke inductor. The BBTPE architecture is shown in Fig. 5.17. In this, the BBCS gets activated when the supply modulator output voltage (v_O) is lower than the input envelope signal v_{IN} by the margin (V_{SM}). It was implemented with the help of a comparator, switch and current source. The employed component list is given in the Table 5.6. The measurement setup for the discussed system is shown in Fig. 5.18. Here, VSA 89601B software was used for the measurement of ACPR and EVM. The LTE 5 MHz wireless signal along with its envelope signal was generated with the help of the vector signal generator R&S SMW 200A.

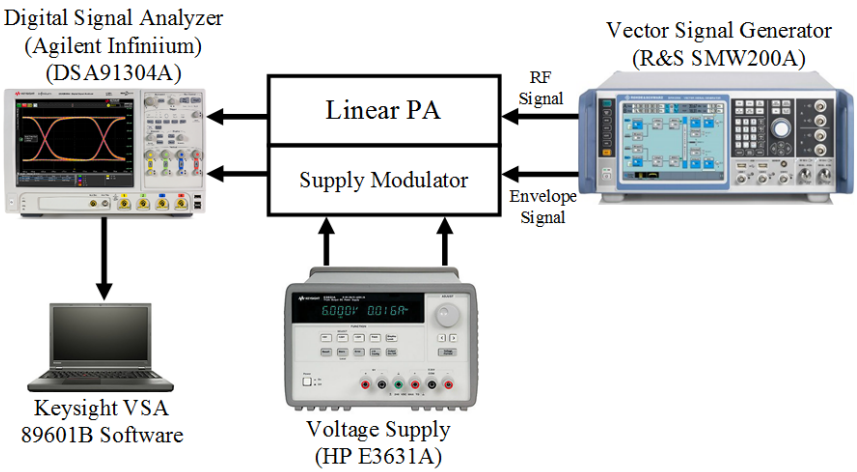


Figure 5.18: RF Frequency Measurement Setup

Blocks	Part#
Linear PA	CC2595 Evaluation Module
Buck Regulator	LM3242 Evaluation Module BBTPE
Comparator	LMV7219
Switch	MAX 4619
BBCS	320P14 THAT

Table 5.6: RF frequency discrete implementation setup part #

5.6 Experimental Results with a Low-Frequency Prototype

The system response with and without BBTPE were measured for various cases as shown in Table 5.7. For these tests, the linear amplifier was replaced by a resistive load.

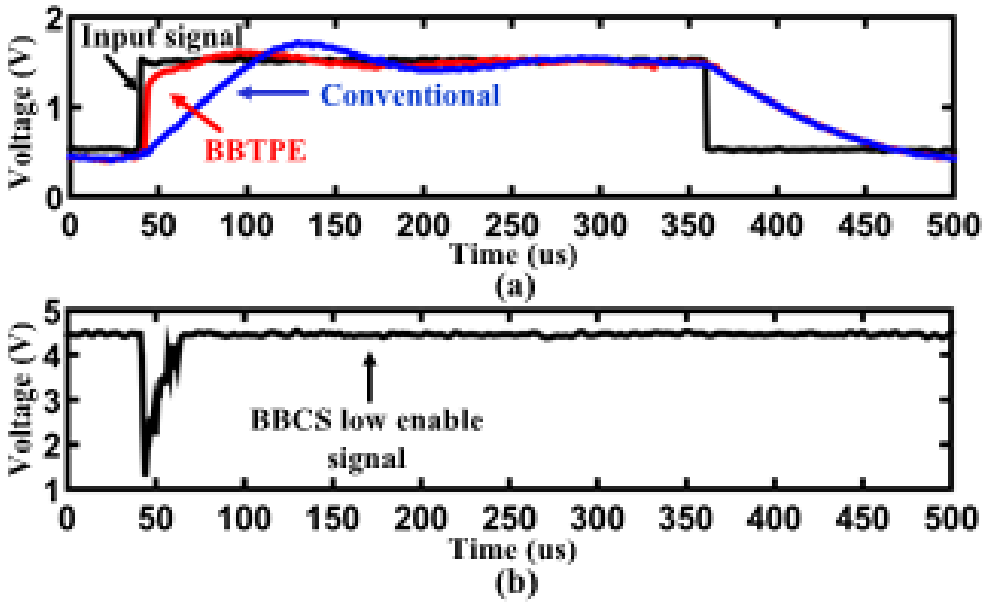


Figure 5.19: Measured response of supply modulator for rectangular wave input signal (Case#1) (a.) input signal, output with and without BBTPE and (b.) BBCS low enable signal

Fig. 5.19 shows the measured response of a discrete components-based system for Case #1 having a $50\ \Omega$ load and $100\ mV$ V_{SM} with complex conjugates closed loop dominant poles. As shown in Fig. 5.19a, the output with the BBTPE system is not only faster compared to the conven-

tional system but it also decreases both overshoot and settling time. Here, the BBTPE incorporated modulator showed improvement by a factor of almost five, from $48\ \mu s$ down to $10\ \mu s$ in rise time. Furthermore, overshoot and 5% settling time were reduced by around 60% from $210\ mV$ and $185\ \mu s$ down to $80\ mV$ and $72\ \mu s$, respectively. Settling time can be further reduced if a smaller safety margin voltage V_{SM} is used (e.g., $50mV$). In the current case, $t_{s,eff}$ is reduced by a factor of 13.7, from $179\ \mu s$ down to $13\ \mu s$. Fig. 5.19b shows the BBCS low enable signal, which was activated during the rising edge of the input signal. As the error voltage gets closer to the safety margin voltage V_{SM}, the BBCS starts turning off. As shown, when the input signal slew rate is faster than the modulator slew rate, the BBTPE takes care of it, and when the error voltage reaches the safety margin i.e., $v_e \sim V_{SM}$, the BBCS operates like a bang-bang system (on and off) until the inductance current is closer to the current demanded by the load. The measured phase portrait for this case is shown in Fig. 5.20, which shows the rate of change of the error voltage, dv_e/dt vs. error voltage v_e, for an input step. As shown, the BBTPE is activated from point (a) to (b). With the help of BBTPE, the rate of change of error increases drastically compared to the without BBTPE scenario, which helped to decrease the error voltage quickly. For corresponding time instances (■▲♦●), the BBTPE incorporated modulator showed lesser error voltage than that in the conventional system. The figure also demonstrates the improvement in the overshoot with the help of BBTPE.

Parameters	Case#1	Case#2
Input Signal (v_{IN})	1 V_{PP} Square wave at 2 kHz 1 V_{PP} with 1 V offset	1 V_{PP} Sinusoidal wave at 10 kHz 1 V_{PP} with 1 V offset
Safety Margin Voltage (V_{SM})	100 mV	50 mV
Closed Loop Dominant Poles	Complex conjugates	Negative real

Table 5.7: Testing configurations with resistive load in discrete prototype measurement

In Case #2, the system response with and without BBTPE was measured employing a $1\ Vpp$, 10 kHz sinusoidal input signal and a $10\ \Omega$ load with negative real closed loop dominant poles and

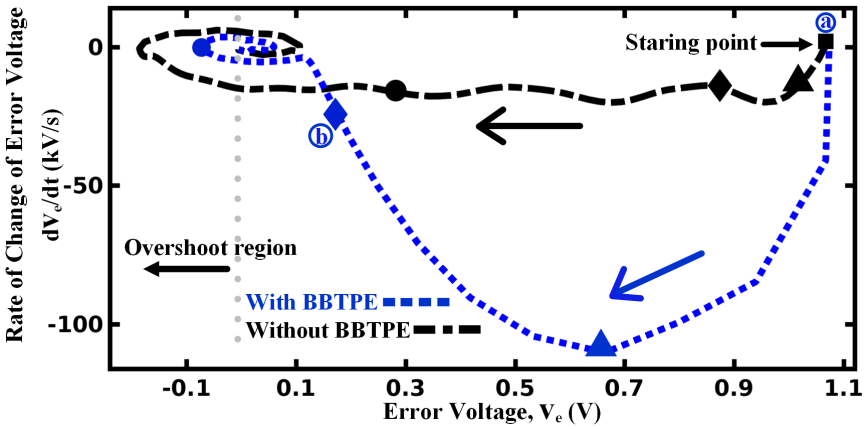


Figure 5.20: Measured rate of error voltage vs. error voltage with and without BBTPE. Here, time mapping symbols ■▲♦ and ● represent 0, 5, 10 and 49 μs respectively.

a $50\ mV$ V_{SM}. The input signal slew-rate was $31.4\ V/msec$, while the estimated modulator's slew rate was $14.5\ V/msec$. From the output responses shown in Fig. 5.21, it follow the input signal due to its slow response. However, the modulator equipped with BBTPE closely tracks the input signal during the rising edge. As previously mentioned, the BBTPE does not help the modulator to closely track the falling edge of the input signal, which is due to employed selective envelope tracking. Due to the slow response of the dynamic buck regulator and small safety margin voltage V_{SM} used, the BBTPE was active for around 35% of the input signal period as shown in Fig. 5.21b.

To measure the impact of BBTPE on the PA linearity performance, a linear amplifier was used instead of a resistive load as shown in the implementation setup in Fig. 5.21. The amplifier was built using a 2N1711 with a $120\ \Omega$ load, and for testing two tones at 106 and 107 kHz were used. The linearity (IM_3) of the amplifier with a conventional solution and the BBTPE included modulator versus output signal are shown in Fig. 5.22. Here, we can see that, when the output signal is small, the difference in linearity is also small because the conventional solution was able to track the envelope signal closely. However, as the output signal amplitude increased hence the slew rate of the envelope signal, the conventional solution was not able to track the envelope signal, and its linearity started degrading as shown in the figure. Additionally, the BBTPE incorporated

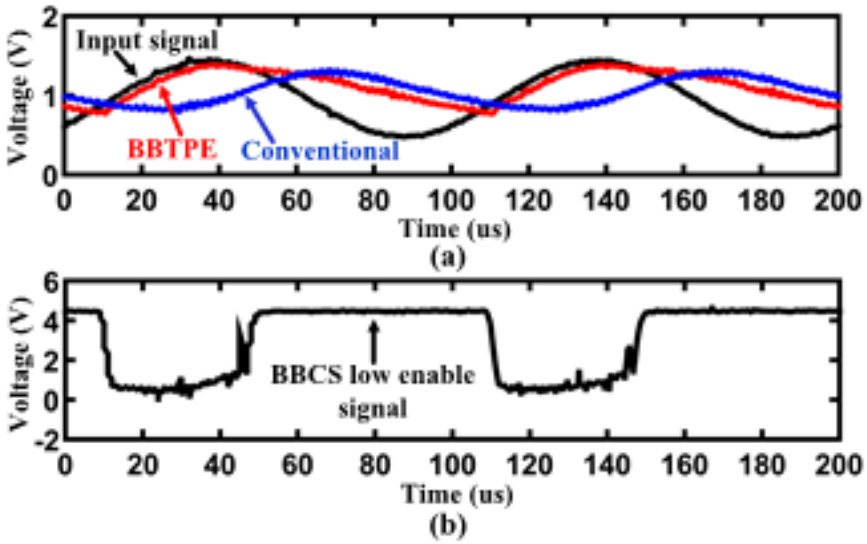


Figure 5.21: Measured response of supply modulator for sinusoidal wave input signal (Case#2) (a) input signal, as well as output with and without BBTPE and (b) BBCS low enable signal.

supply modulator was able to track the envelope signal and provided a linearity enhancement by $\sim$ 11 dB in the middle region of the figure. As the input signal kept increasing, the linearity with the BBTPE incorporated solution started degrading marginally, mainly due to the PA linearity degradation rather than by the functionality of the supply modulator.

5.6.1 Simulation Results with an RF-PA

For WLAN standard IEEE 802.11n with a 20 MHz bandwidth, the cadence-based system simulation for an output power of 25 dBm is shown in Fig. 5.23. The simulated ACPR and EVM were -35.14 dBc and -29.51 dB respectively for an output power of 25 dBm with the help of the BBTPE included modulator, which satisfied the standard requirement. The time-domain input and output signal of the PA is shown in Fig. 5.24.

To consider switching noise coupling from the BBTPE, the contribution of switching noise in the main channel power and adjacent channel was measured. Basically, it is the processing of voltage ripple and the BBTPE switching noise that lied on the carrier frequency through the transfer function of the path from the supply modulator to the RF out. For the case of 25 dBm output power, in-band switching noise power due to BBTPE increased by less than 1 dB from

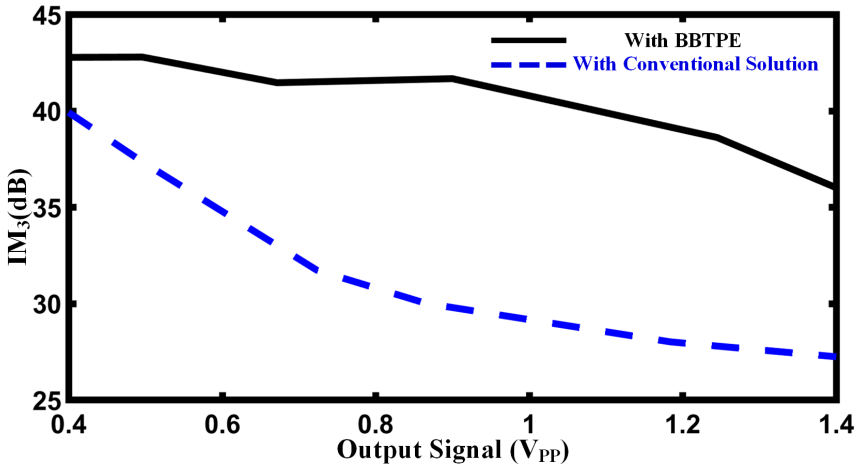


Figure 5.22: Measured PA Output IM3 versus Output Signal.

$-84.69\ dBm$ to $-83.87\ dBm$. Besides the marginal increment in the switching noise power, the absolute value is quite small compared to the main channel and adjacent channel power. Considering the performance of the PA, the impact of switching noise on ACPR and EVM was not noticeable.

With the increment of output power, the peak of output voltage increases and demands more agility in the supply modulator. As shown in Fig. 5.25, as the output power increases, the EVM degrades in the case of a conventional solution; however, with the help of the BBTPE included modulator, EVM remained below $-29\ dB$ for output power ranging from 17 to $25\ dBm$. For output power of $25\ dBm$, the improvement in EVM was $12.26\ dB$. As the transition from PBO to the peak power level is not frequent for wireless standards, the impact of using BBTPE on the modulator efficiency, which is 82.5%, is as minimal as $\sim$2% at $25\ dBm$ PA output power, and the difference becomes smaller and smaller as the output power decreases. Furthermore, system efficiency including ET and PA was almost the same for both cases.

5.6.2 Experimental Results with an RF-PA

For an input of 16-QAM LTE with $5\ MHz$ bandwidth at $2.4\ GHz$ of RF frequency, the time-domain measurement results for the system without and with BBTPE are shown in Fig. 5.26

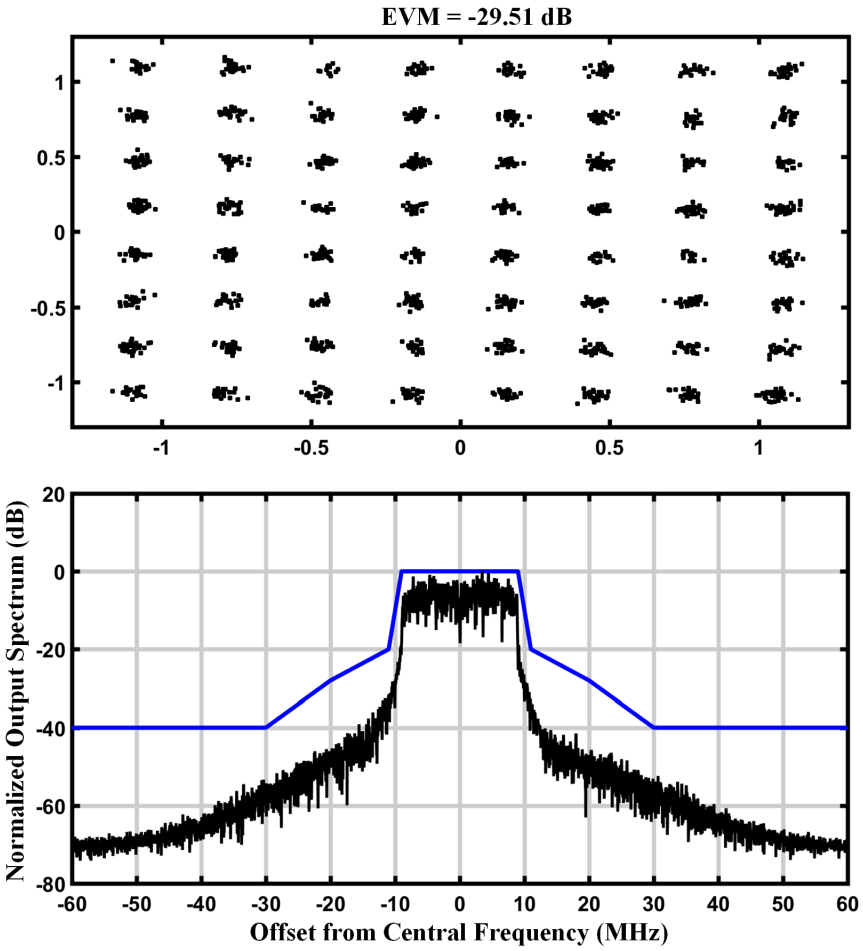


Figure 5.23: EVM and output spectrum for 802.11n 64-QAM OFDM data (Output power = 25 dBm)

and 5.27, respectively. Fig. 5.26a shows the input and output of the supply modulator without BBTPE. Due to limited bandwidth, the modulator is not able to follow the input envelope signal; a significant distortion in PA output signal is expected in this case. The corresponding PA output is shown in Fig. 5.26b. In the case of the modulator with BBTPE, the output signal is shown in Fig. 5.27a. Due to the BBTPE, the output voltage always remains equal or higher than the input envelope signal. The activity of high-enabled BBCS control signal is shown in Fig. 5.27b; this gets activated when the output signal goes below the safety margin. The corresponding RF output of the PA is shown in Fig. 5.27c. The ACPR and EVM for both configurations (with and without BBTPE) are shown in Fig. 5.28. Here, the ACPR and EVM improved by $7.68\ dB$ and 65.1%,

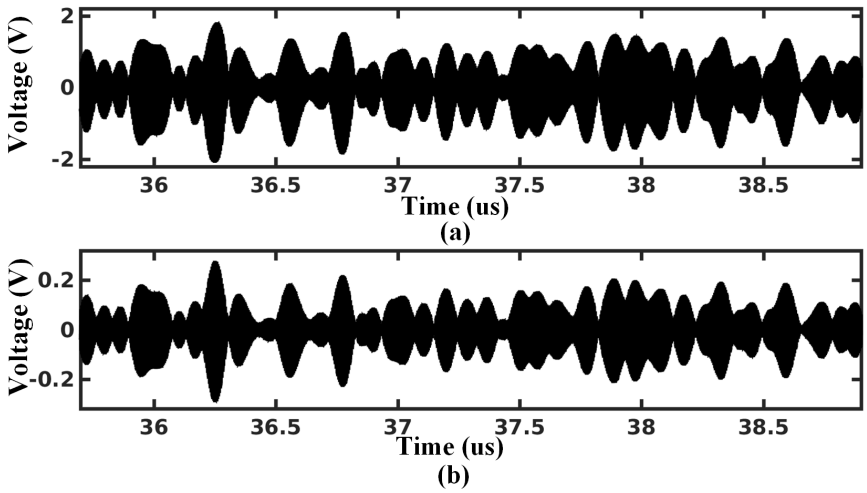


Figure 5.24: Simulated response with BBTPE for IEEE standard 802.11n 64-QAM (a) Output signal (b) input signal of the power amplifier)

respectively. The system's performance summary with and without BBTPE is shown in Table 5.8. Due to the addition of the BBTPE system including the peripherals, the modulator efficiency degraded from 83.9% to 76.1%, in which 4.2% degradation is due to the BBTPE controller. The impact of the switching noise on the PA output spectrum was not noticeable in both scenarios. A further comparison with a state-of-the-art performance with bandwidth of $5\ MHz$ is shown in Table 5.9. In this work, the output power and PAE were limited by the performance of CC2595 PA. A further improvement in the modulator efficiency can be achieved with a faster dynamic buck regulator, which can reduce BBCS activity, and an optimized BBTPE controller with power efficient switch and comparator.

Parameter	Without BBTPE	With BBTPE
ACPR (dB)	-24.42	-32.1
EVM (%)	8.07	2.82
PAE(%)	20	25.3
Modulator Efficiency (%)	83.9	76.1

Table 5.8: Performance Comparison Without and With BBTPE Configuration

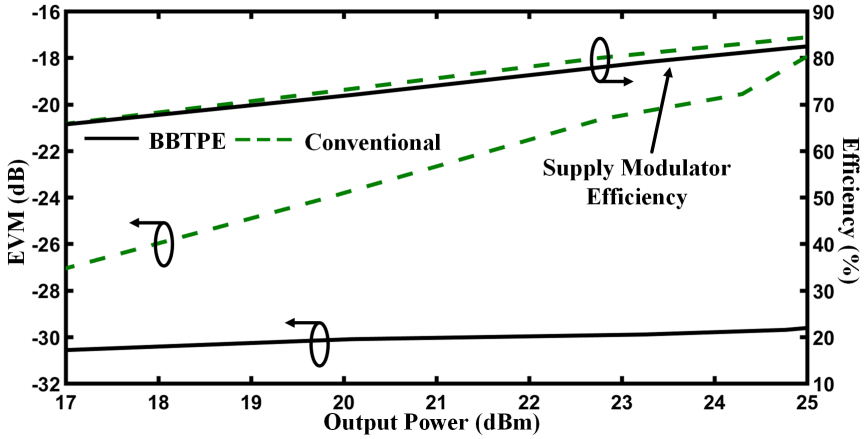


Figure 5.25: Simulated EVM and power efficiency vs output power for supply modulator with and without BBTPE

Ref.	Modulation	Signal BW (MHz)	Frequency (GHz)	PAPR (dB)	Modulator (%)	ACPR (dBc)	EVM (%)
[90]	LTE 16-QAM	5	0.78	7.5	73	-31.1	3.7
[134]	LTE 16-QAM	5	2.47	-	82.5	-	5
[140]	WiBro 16QAM	5	1.88	10.75	-	-	3.64
[141]	LTE 16-QAM	5	1.9	7.5	78.5	-	1.1
[142]	WiMAX 64QAM	5	1.88	8.6	75	-	2.98
[143]	HSUPA R6	5	-	6.7	80%	-40	$< 2\%$
This work	LTE 16-QAM	5	2.4	9.38	76.1 (80.3)	-32.1	2.82

Table 5.9: Performance comparison with state-of-the-art results

5.7 Summary

This chapter presented an agile supply modulator with enhanced transient performance for envelope tracking purposes in linear PA systems. The proposed supply modulator is comprised of BBTPE along with a dynamic buck regulator. The transient performance enhancer provided an on-demand current to output in order to improve tracking of the input signal during sharp input rising transition along with improvement in overshoot and settling time. In this way, the BBTPE was able to provide additional degrees of freedom to the buck regulator design by relaxing its requirement for transient performance. The proposed selective envelope tracking also provides an efficient and simplified solution for envelope tracking in linear PA systems. In a test scenario, the

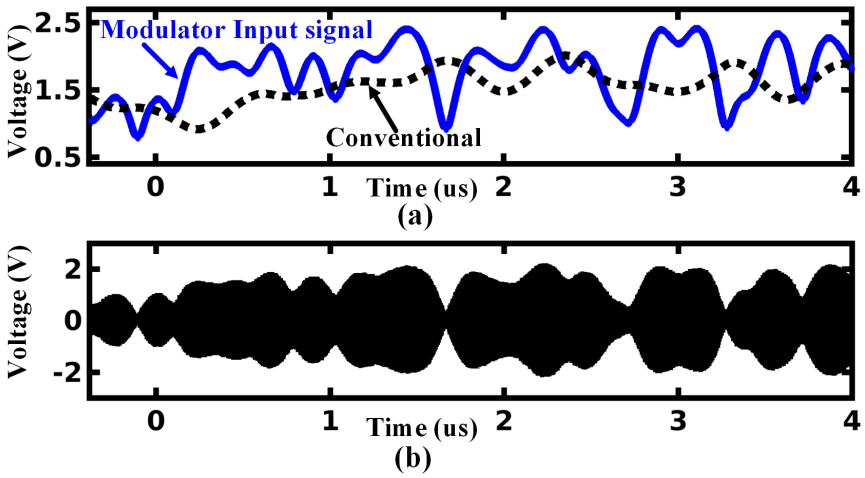


Figure 5.26: Measured response without BBTPE for 16-QAM LTE 5 MHz input signal (a) supply modulator input signal, as well as output signal and (b) Power amplifier's output signal

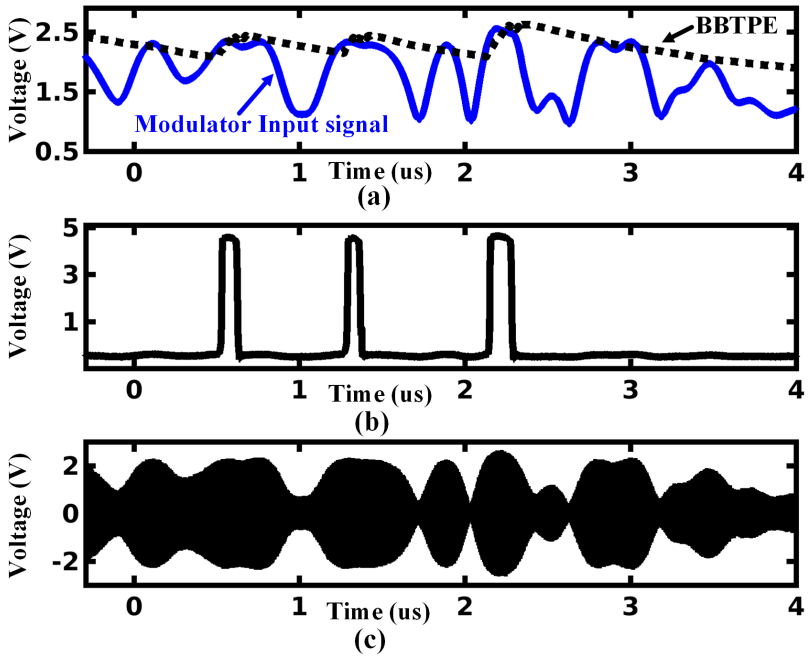


Figure 5.27: Measured response with BBTPE for 16-QAM LTE 5 MHz input signal (a) supply modulator input signal, as well as output, (b) BBCS high enable signal and (c) Power amplifier's output signal

proposed architecture showed an 80% improvement in rise time with a 60% reduction in overshoot and settling time. The effective settling time for the test scenario was reduced by 93%. When

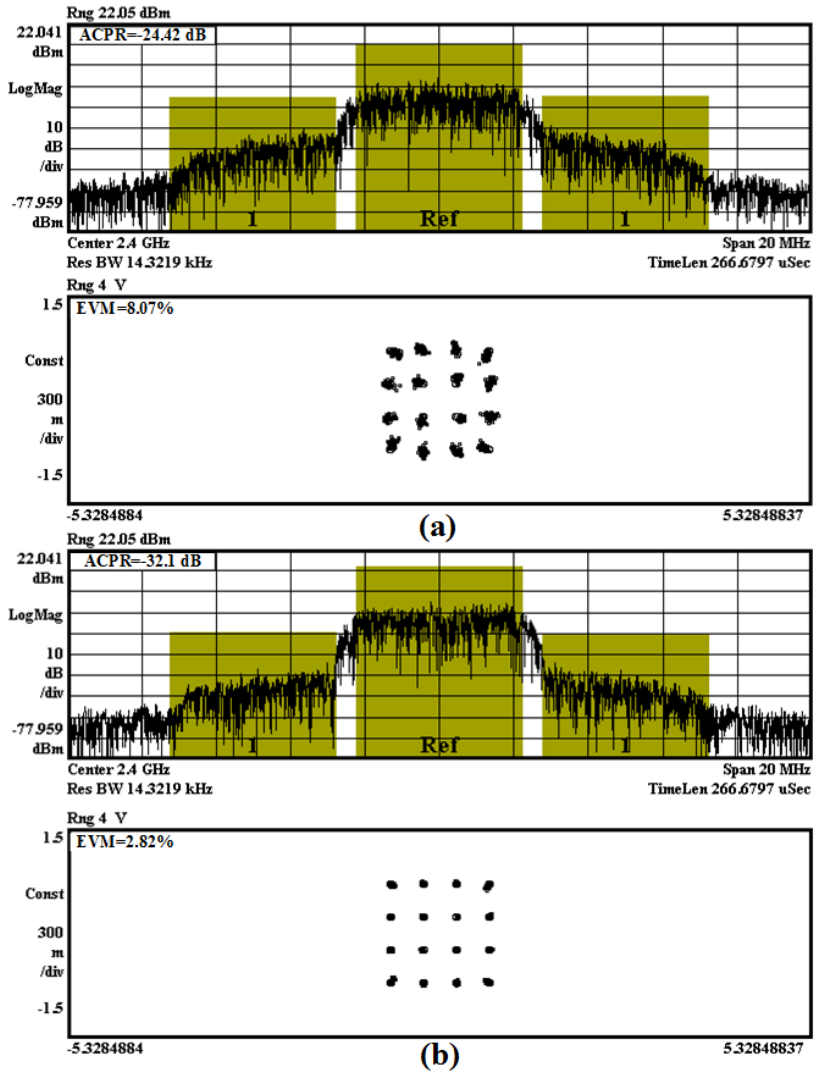


Figure 5.28: Measured output spectrum and EVM for 16-QAM LTE 5 MHz input signal (a) without BBTPE and (b) with BBTPE

compared with the results for the PA system using the conventional dynamic buck regulator, the experimental results with a 16-QAM LTE $5\ MHz$ at $2.4\ GHz$ standard showed improvement of $7.68\ dB$ and 65.1% in ACPR and EVM, respectively at $14.01\ dBm$ of output power. Finally, the benefits over improvement of overshoot and settling time along with rise time can be extended for other solutions that use auxiliary elements in parallel with switching regulators to handle fast input transition.

6. SUMMARY AND CONCLUSIONS

This dissertation mainly focused on envelope tracking for the linear power amplifier, and digital polar power amplifier. In the envelope tracking, this dissertation presented the agile supply modulator which provides optimal transient performance along with high power efficiency. For this purpose, bang-bang transient performance enhancer was introduced that provided on-demand needed current to the load, and it makes the output voltage high enough for the power amplifier to be functional. With this enhancer, the rise time of the supply modular improved along with overshoot and setting time. It was also shown that the effective settling time of the supply modulator improved significantly with this proposed work. During steady state, the output voltage is fully controlled by a dynamic buck regulator hence efficiency. Also, the introduced selective envelope tracking provided efficient envelope tracking that helped to improve the efficiency of the supply modulator. The dissertation also discussed results with 80% improvement in rise time along with 60% reduction in both overshoot and settling time compared to the conventional dynamic buck regulator-based solution. In addition, experimental results with LTE 16-QAM 5 MHz wireless standard showed the improvement of 7.68 dB and 65.1% in ACPR and EVM, respectively.

In digital polar power amplifier, this dissertation discussed two important issues and their solutions: delay mismatch between amplitude and phase, and spectral mask violation due to spectral images. In this work, the design is implemented in 40 nm CMOS technology and simulated with 64-QAM IEEE 802.11n wireless standard. For the spectral images issue, the proposed interpolation of phase and amplitude led to the improvement of around 10 dB in ACLR. For the issue of delay mismatch between amplitude and phase path, a calibration was discussed in this work. This is executed during empty transmission slots. For this, a special input pattern sequence was developed. It reduced the spectral regrowth at the output of the digital polar power amplifier. The proposed work showed the benefit of 84.35% in EVM, and 7.57 dB in ACLR for 3.5 ns mismatch between amplitude and phase path in simulation results.

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APPENDIX A

REGION I ANALYSIS

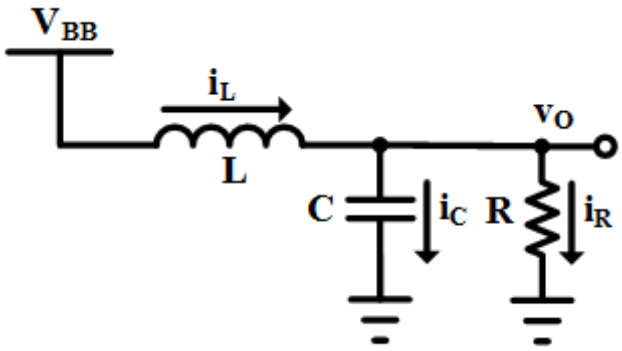

Figure A.1: Region I system configuration

The system configuration for Region I is shown in Fig. A.1. For this, switches S_P and S_N have been closed and opened respectively at time $t = 0s$. It applies input to L, C and R network. With the help of KCL at output node (v_o).

$$i_L(t) = i_C(t) + i_R(t) \tag{A.1}$$

Using ohm law and capacitor's current equation in terms of voltage difference across it.

$$i_L(t) = C\frac{dv_o(t)}{dt} + \frac{v_o(t)}{R} \tag{A.2}$$

Differentiating above equation with time,

$$\frac{di_L}{dt} = C\frac{d^2v_o(t)}{dt^2} + \frac{1}{R}\frac{dv_o(t)}{dt} \tag{A.3}$$

With the help of Maxwells equation,

$$\frac{di_L}{dt} = \frac{V_{BB} - v_o(t)}{L} \tag{A.4}$$

Equating A.3 and A.4,

$$\frac{V_{BB} - v_o(t)}{L} = C\frac{d^2v_o(t)}{dt^2} + \frac{1}{R}\frac{dv_o(t)}{dt} \tag{A.5}$$

$$LC\frac{d^2v_o(t)}{dt^2} + \frac{L}{R}\frac{dv_o(t)}{dt} + v_o(t) = V_{BB} \tag{A.6}$$

Generic solution of the above differential equation is,

$$v_o(t) = C.F. + P.I. = v_c(t) + v_p(t) \tag{A.7}$$

$$v_c(t) = Ae^{s_1t} + Be^{s_2t} \tag{A.8}$$

$$v_p(t) = V_{BB} \tag{A.9}$$

$$Here, s_1 = -\frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}}, s_1 = -\frac{1}{2RC} - \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}}$$

With the help of initial conditions,

$$A = \frac{s_2(V_{BB} - v_o(0))}{s_1 - s_2} + \frac{i_c(0)}{C(s_1 - s_2)}$$
$$B = \frac{s_1(v_o(0) - V_{BB})}{s_1 - s_2} - \frac{i_c(0)}{C(s_1 - s_2)}$$

Putting value of A and B in A.7,

$$v_o(t) = V_{BB} * \left(\frac{s_2e^{s_1t} - s_1e^{s_2t}}{(s_1 - s_2)} + 1\right) - v_o(0) * \left(\frac{s_2e^{s_1t} - s_1e^{s_2t}}{(s_1 - s_2)} + \frac{e^{s_1t} - e^{s_2t}}{RC(s_1 - s_2)}\right) + \\ + \frac{i_L(0)}{C(s_1 - s_2)}(e^{s_1t} - e^{s_2t}) \tag{A.10}$$

APPENDIX B

REGION III ANALYSIS

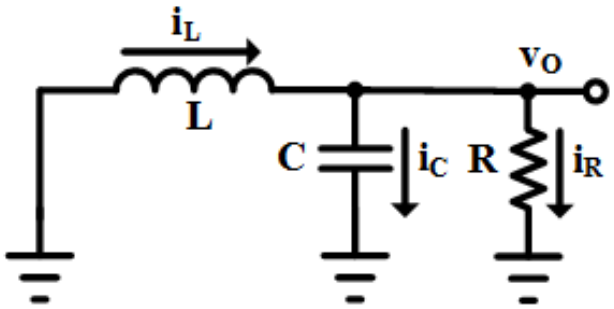

Figure B.1: Region I system configuration

The system configuration for Region III is shown in Fig. B.1. The governing equation of the output voltage $v_o(t)$ for complex conjugate poles can be obtained by putting 0 for V_{BB}. The output voltage for Region III starts at $t = t_3$ is given by B.1

$$v_o(t) = \frac{e^{-\frac{t-t_3}{2RC}}}{w_d}(v_o(t_3) * \left\{-\frac{1}{2RC}sin(w_d(t-t_3)) + w_d cos(w_d(t-t_3))\right\} + \\ + \frac{i_L(t_3)}{C} * sin(w_d(t-t_3))) \tag{B.1}$$

where, the w_d is $\sqrt{(1/LC) - (1/2RC)^2}$.

The current through the inductor in this region is given by B.2.

$$i_L(t) = C\frac{dv_o(t)}{dt} + \frac{v_o(t)}{R} \tag{B.2}$$

Substituting $v_o(t)$ from B.1 in B.2 leads to,

$$
\begin{aligned}
i_L(t) = v_o(t_3) * e^{-\frac{t-t_3}{2RC}} \left\{ \left(-\frac{1}{4R^2 C w_d} - C w_d \right) * sin(w_d(t-t_3)) \right\} + \\
+ i_L(t_3) * e^{-\frac{t-t_3}{2RC}} \left\{ \left(\frac{1}{2RC} \right) * sin(w_d(t-t_3) + cos(w_d(t-t_3)) \right\}
\end{aligned}
\tag{B.3}
$$