ABSTRACT

Title of Dissertation: INTEGRATED INDUCTIVE AND CONDUCTIVE CHARGING SYSTEM FOR ELECTRIC VEHICLES

Arun Sankar Uma Sankar, Doctor of Philosophy, 2019.

Dissertation directed by: Prof. Alireza Khaligh,
Associate Professor,
Department of Electrical and Computer Engineering

The global electric vehicle (EV) market acceleration is facilitated by supporting policies deployed by governments and cities to reap multiple benefits in the fields of transport decarbonization, air pollution reduction, energy efficiency and security. Currently conductive chargers are a customary method of storing electric energy into the storage elements present onboard of an EV which is inadequate in supporting complete autonomy. The thriving inclination towards design of autonomous vehicles have shaped wireless charging as an attractive solution in favor of complete autonomy. As long as the wireless charging infrastructure as well as interoperability standards are not completely developed, wired and wireless chargers have to co-exist onboard the vehicles for user convenience. Incorporation of an entire parallel wireless charging system on-board an EV, either during manufacturing or after-market increases size, weight, or cost, while declining the electric range of vehicle. The current requisite for multiple on-board charging options motivates the necessity for a solution for efficiently integrating wired and wireless charging systems.

In this PhD research we propose multiple charging architectures capable of integrating inductive and conductive charging systems. The proposed architectures merge

the output rectifying stage of an inductive charging system to the existing on-board charger eliminating the additional weight and volume associated with a wireless charger. Since the proposed system involves multiple power conversion stages, a system level study is carried out to select feasible topologies capable of maximizing the efficiency of an integrated system. Additionally, an extended harmonic approximation (EHA) technique is introduced to increase the accuracy of a resonant converter model facilitating the optimized design parameter selection of an inductive charging system. Furthermore, a novel analog synchronous rectification circuit is proposed and designed to enable active rectification maximizing power transfer efficiency.

For proof of concept verification, a laboratory prototype of a 3.3kW Silicon Carbide (SiC) based integrated wireless charger is developed that can be interfaced to a variable input voltage (85-265 Vrms) 50/60Hz AC grid. According to the experimental measurements, the charger draws an input current with total harmonic distortion of 1.3% while achieving an overall efficiency of 92.77% at rated output power.

INTEGRATED INDUCTIVE AND CONDUCTIVE CHARGING SYSTEM FOR ELECTRIC VEHICLES

by

Arun Sankar Uma Sankar

Dissertation submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
2019

Advisory Committee:
Professor Alireza Khaligh, Chair/Advisor
Professor Robert Newcomb
Professor Neil Goldsman
Professor Kevin Daniels
Professor Patrick McCluskey, Dean's Representative

Acknowledgments

First of all, I would like to thank my PhD advisor Prof. Alireza Khaligh, for his valuable advice and mentorship throughout my research. During the past few years at University of Maryland, Prof. Khaligh not only introduced me to high quality research in power electronics, but also educated me on various practical perspectives to be considered while analyzing research problems. He has been a constant support during my failures and motivated me to strive towards success. I would really like to thank him for his valuable advices which has helped in my professional development.

I would also like to thank Prof. Robert Newcomb, Prof. Neil Goldsman, Prof. Kevin Daniels and Prof. Patrick McCluskey for kindly taking out their valuable time to be a part of my PhD committee. Thank you for your interest in my work.

I would also like to thank all of my present and former lab mates at MPEL (Ayan Mallik, Weisheng Ding, Akshay Singh, Jiangheng Lu, Michael D'Antonio, Peiwen He, Zeyu Zhang, Shenli Zou, Shiladri Chakraborty, Apurv Kumar Yadav, Bin Wu, Chuan Shi) for their time in regular technical discussions and helping in debugging hardware at rough times. These productive discussions always helped me to learn more and think outside the box for finding solutions.

Very special thanks and sincere gratitude to my parents for their constant support, encouragement, motivation and belief in me throughout by studies. I would also like to thank my brother, friends and teachers who have motivated me throughout my life to pursue my dreams and achieve this degree.

Furthermore, this work has been sponsored by the US National Science Foundation grant numbers 1507546, 1602012 and UM Ventures Seed grant which are gratefully acknowledged.

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Chapter 1: Introduction

1.1 EV Market

Dynamic market acceptance of electric vehicles has ensued in recent years leading to a global stock of 3.1 million electric passenger cars in 2017, an increase of 57% from the previous year [1]. The global EV market spurt is facilitated by supporting policies deployed by governments and cities to reap multiple benefits in the fields of transport decarbonization, air pollution reduction, energy efficiency and security[2]. Increased sales volumes together with growing competition in the development of new technologies act as motivating factors for continuous reductions in the cost of manufacturing key components of an EV. Cost reductions in EV-related technologies further support their affordability compared with internal combustion engine vehicles.

1.2 EV Architecture

In comparison to conventional gasoline vehicles, EVs are typically powered by one or more electric motors as an alternative to an internal combustion engine (ICE). Large battery packs are used in EVs to store electric energy and are energized from the grid through plug-in charging systems. Hybrid electric vehicles (HEVs) can be powered by both fossil and electric energies. Typically, an ICE and an electric motor with a battery pack are included in HEVs. The battery pack is charged through the ICE, not the grid, therefore, HEVs do not have plug-in charging systems[3].Plug-in hybrid electric vehicles (PHEVs) also have both ICE and electric motors. However, in comparison to HEVs, the battery pack of PHEVs can be charged through both the ICE and the grid. Therefore, plug-in charging systems are required in PHEVs.

A figurative PHEV power system architecture is presented in Fig. 1.1, which consists of an electric motor, a drive inverter, a high voltage (HV) battery pack, a 12 V low voltage (LV) auxiliary battery, onboard charger (OBC) and wireless charging interface. Furthermore, an internal combustion engine is present on-board fueled by gasoline and attached to the axle through a torque coupler [4]. The electric motor serves a dual purpose in this architecture namely propulsion and regeneration. In propulsion mode, the electric motor propels the vehicle with the help of energy stored in the HV battery. The drive inverter transforms dc output of the battery to the required AC input to drive the motor. In regenerative mode, the motor acts as a generator recovering the breaking power and storing it in the HV battery. Thus the drive inverter operates in a bidirectional fashion as shown in Fig. 1.1 below.

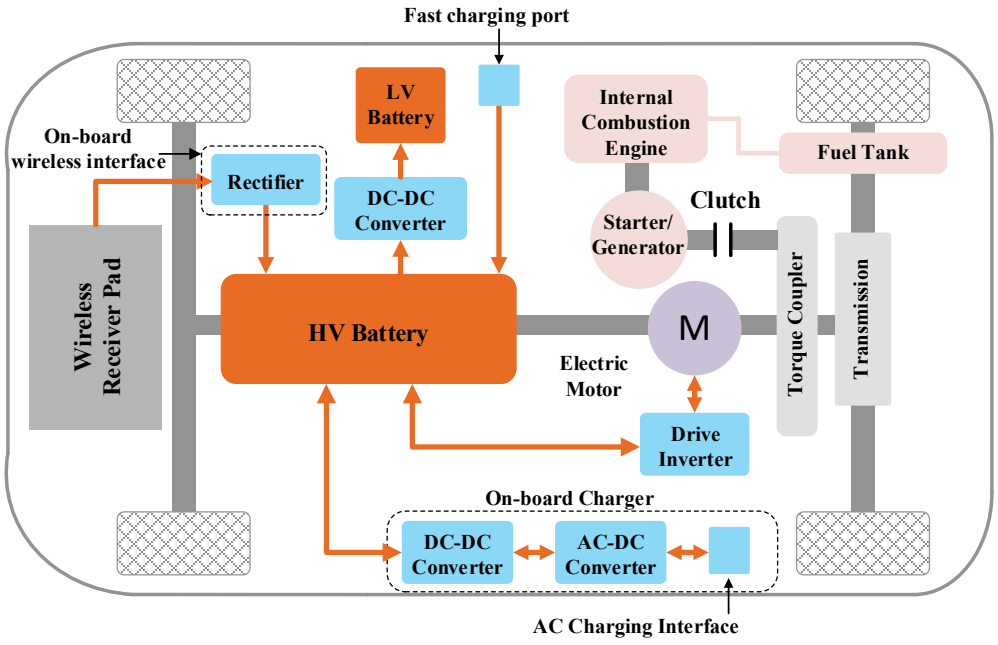


Fig. 1.1 Power electronic interfaces onboard a plug-in hybrid vehicle

A LV battery of 12V is also typically present on-board the vehicle which supplies the auxiliary loads such as air conditioning system, music system, mobile chargers, lights and

control interfaces of various on-board elements. In case of gasoline engines the starter/generator charges the auxiliary battery during propulsion while in electric vehicles there is additional on-board dc-dc converters present which facilitate high voltage to low voltage power conversion in a unidirectional fashion.

Conventionally, an on-board wired charger is an essential component of an EV aiding the charging of the main traction battery. The two charging interfaces on-board the vehicle are presented in Fig. 1.1 categorized as (i) AC charging and (ii) DC fast charging. The various classification of charging levels and the corresponding standard [1] used by electric vehicle supply equipment (EVSE) in North America are presented in Table 1.1.

Typical OBCs available in market are Level 1 or Level 2, they use the on-board AC-DC interface to convert the input single phase grid voltage to HV battery voltage typically in the range of 400V. Since, the battery voltage is dependent on the state of charge (SOC) the on-board charger needs to regulate the output voltage to variable battery voltage specifications while isolated from the grid. Furthermore, due to addition of on-board interfaces for power conversion the weight and volume of these chargers have to be minimized to increase the electric range of the vehicle. In this regards, multiple topologies have been proposed to integrate on-board power electronic interfaces [5].

Newer vehicles are equipped with DC fast charging capabilities which supplies a large amount of dc current directly to battery charging at very fast rates. The AC-DC conversion stage for DC fast chargers are placed off-board the vehicle and requires additional infrastructure to enable this charging. Even though a DC fast charger is very convenient for charging it requires a huge financial investment for widespread deployment [5].

Table 1.1 EVSE Classification in North American market [1]

	Conventional Plugs	Slow Chargers	Fast Chargers	
Level	Level 1	Level 2	Level 3	
Current	AC	AC	AC, triphase	DC
Power Rating	≤ 3.7 kW	≤ 22 kW	>22kW and ≤43.5 kW	Currently < 200 kW
Plug Type	SAE J1772 Type 1	SAE J1772 Type 1, Tesla	SAE J3068 (under development)	CCS Combo 1 (SAE J1772 & IEC 62196-3

Recently wireless charging of EVs has gained popularity due to its safety, convenience, and compatibility with fully autonomous driving technology [6]. Wireless charging typically employs either near field or far field electromagnetic (EM) fields for energy transfer. Far field EM power transfer is employed for long distance transmission while EVs typically employ near field power transfer as the air gap distance is less than a couple of centimeter's [7]. The typical on-board components of a wireless charging system are illustrated in Fig. 1.1. A receiver pad is attached to the vehicle which receives power from a transmitting pad through inductive or capacitive field that generates AC voltage. The received voltage is rectified with the help of an on-board rectifier to charge the HV battery. Similar to conductive charging solutions wireless standards are under development to define power levels, classify the efficiency requirements as well as provide guidelines for interoperability between various charging structures [6] - [8]. Table 1.2 summarizes the key requirements imposed by the SAE J2954/1 standard which is under improvement. The

different structures enabling wireless charging will be comprehensively reviewed in the following section.

Table 1.2 J2954/1 proposed WPT Power classes for inductive charging [8]

Characteristics	WPT Power Class			
	WPT1	WPT2	WPT3	WPT4
Maximum input volt amps	3.7 kVA	7.7 kVA	11.1 kVA	22 kVA
Minimum efficiency target	>85%	>85%	>85%	TBD
Minimum target efficiency at offset position	>80%	>80%	>80%	TBD
Frequency	85 kHz within international frequency band (81.38 – 90 kHz)			

1.3 Charging Structures

The various on-board charging interfaces of a conventional electric vehicle equipped with both wireless and conductive charging stages is presented in Fig. 1.2.

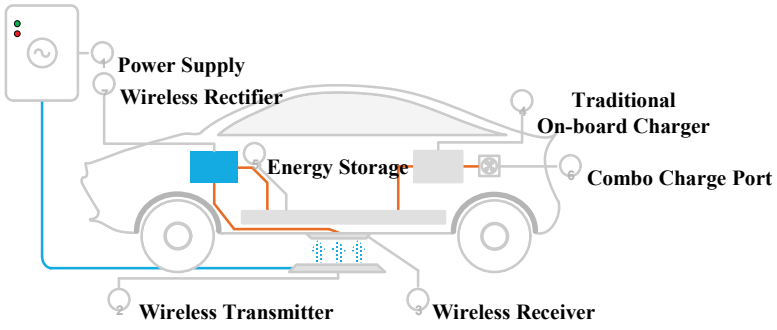


Fig. 1.2 Typical charging elements of an EV equipped with conductive and inductive charging

1.3.1 Conductive charging

A typical EV charger configuration is shown in Fig. 1.3 which consists of an AC-DC power factor correction (PFC) stage in cascade to an isolated DC-DC converter. The front-end PFC circuit aids in achieving a unity power factor (PF) at the grid side while regulating the output DC voltage to a specified value. Researchers have tried to improve the performance of this stage by proposing different topologies and control techniques[9]- [10]. The most widely accepted PFC topology adopted in single-phase OBCs are boost-derived PFCs due to their continuous input current characteristics and superior EMI performance, compared to buck-derived PFC topologies whose EMI filters are usually bulky with high losses due to the discontinuous input current operation.

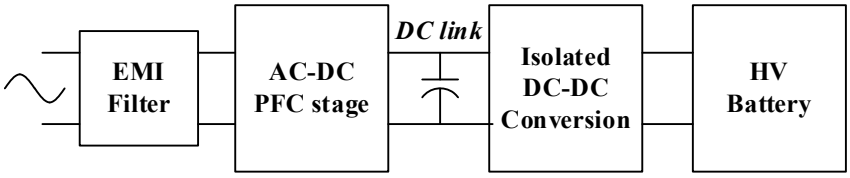


Fig. 1.3 Typical structure of on-board charger

An isolated DC-DC stage is necessary to provide isolation between grid and HV battery. Two classes of topologies are widely used for this purpose, (i) Pulse Width Modulated (PWM) converters including phase-shifted full bridge converter (PSFB) and dual-active full bridge converter (DAB) (ii) Pulse frequency modulated (PFM) converters comprising of different styles of resonant converters like LLC, LCC, CLLC. These converters operate with a fundamental difference in control technique but share several common characteristics such as capability of wide gain operation, ability to achieve soft switching technique namely zero voltage switching (ZVS) for MOSFETs.

A high efficiency two stage vehicle charger with bridgeless boost PFC circuit in cascade with phase shifted full bridge structure shown in Fig. 1.4 was developed by researchers in [11]. The proposed charger is unidirectional due to the secondary diode bridge but can easily be made bidirectional by replacing with a synchronous rectified bridge. The unidirectional charger proposed achieved a peak efficiency of 95% while operating at 200 kHz.

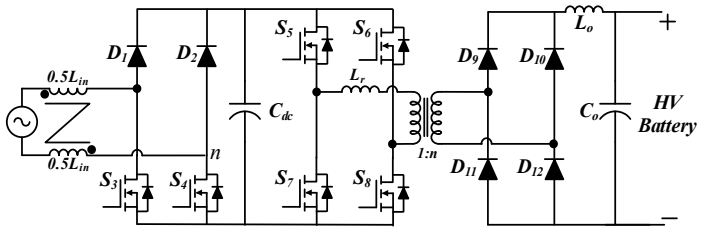


Fig. 1.4 High efficiency vehicle charger proposed in [11]

A 97.2% efficiency is recorded for the isolated DC-DC conversion stage for a bidirectional PWM resonant converter proposed by researchers in [12] for EV charging application. The modified PWM resonant converter structure is presented in Fig. 1.5.

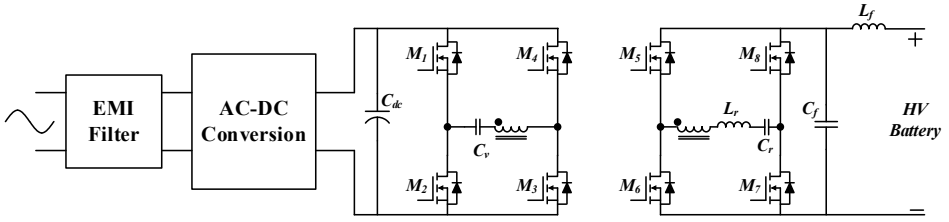


Fig. 1.5 Bidirectional PWM resonant converter proposed in [12]

Researchers in [13] have proposed a dual stage structure with interleaved totem pole PFC in cascade with a half-bridge CLLC converter as a feasible solution for OBC. The proposed OBC structure is presented in Fig. 1.6, where the use of a variable dc link voltage improves overall efficiency of the circuit. The proposed circuit claims a peak efficiency of over 94% at 2 kW output.

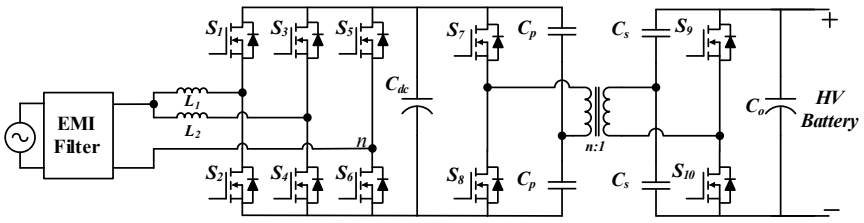


Fig. 1.6 Dual stage OBC structure proposed by researchers in [13]

Additionally, multiple bidirectional resonant converters suitable for OBC design with variable dc link voltage are proposed by researchers in [14]. An electrolytic capacitor-less bidirectional structure employing harmonic compensation was proposed by researchers in [15] for power dense OBC design.

1.3.2 Inductive charging

The inductive power transfer (IPT) system uses the near field magnetic resonance principle to transfer power wirelessly from a transmitter pad to a receiver pad with large air gap.[16] A typical block diagram representation of the various stages involved in an IPT system is illustrated in Fig. 1.7.[17]

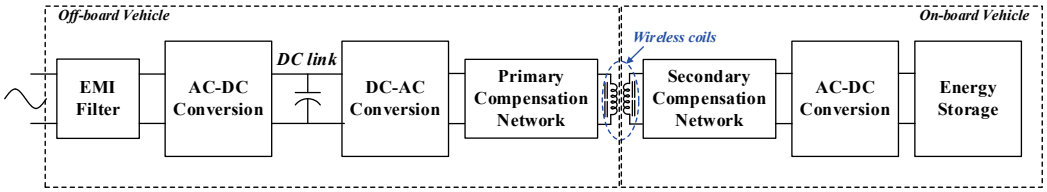


Fig. 1.7 Typical structure of an IPT system for EV charging

The off-board components designated in Fig. 1.7 facilitate the conversion of grid voltage AC to an intermediate DC voltage which is converted to a high frequency AC (HF-AC) voltage to be magnetically coupled with the on-board components. The AC-DC conversion stage is similar to the front-end PFC stage of a conductive charger. The topologies

discussed in the previous section are equally appropriate for design of this system. Detailed review and topology selection for this stage is carried out in Chapter 3.

Figure 1.8 summarizes the most common structure used by researchers for IPT charging system for EV[16], [18]–[22]. The basic structure uses an active front end rectifier followed by a voltage fed high frequency inverter. Various compensation topologies are employed to improve the power transfer capability as well as the tolerance of the system to misalignment conditions [23]–[26]. A detailed analysis of various basic compensation topologies is carried out in chapter 3. Different coil structures are also proposed by researchers to improve the coupling between the coils while reducing the weight and size of coil. [22], [27]–[31]. The secondary side of the wireless stage uses a diode bridge to rectify the high frequency AC voltage generated from the receiver to charge the battery.

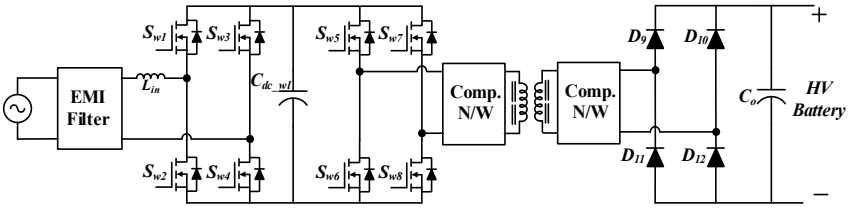


Fig. 1.8 IPT system employing a dual stage structure with voltage fed high frequency inverter network

An alternative topology for high frequency DC-AC conversion using current fed inverter is proposed by researchers in [32], [33]. The current topology inherently provides lower current stress and short circuit protection. The main disadvantage of this topology is the use of a large inductor at the input side to generate the current source leading to increased volume, additional losses and increased cost of the system[6], [32]. The current fed structure also requires an on-board rectification stage to convert high frequency AC – DC in order to charge the battery.

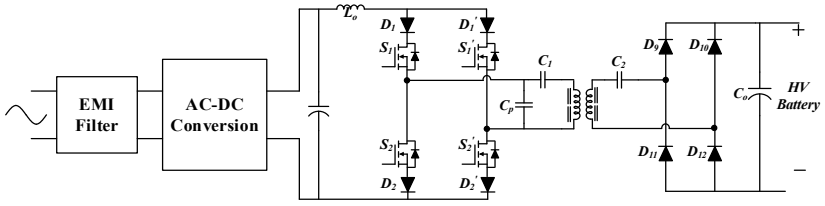


Fig. 1.9 IPT system employing a current source fed high frequency inverter[32]

A topology employing a multi-phase series connected converter to power an IPT system was proposed by researchers in [34] capable of enabling high power IPT solutions. The proposed system can be extended to an n-phase input with a series connected output current transformer which can individually control the phase of each leg to facilitate soft switching operation. The system is compensated with a series-series (SS) structure. On the output side of the converter a bridge rectifier is used to convert the high frequency AC back to DC. Even though the proposed system is feasible for high power applications it requires multiple current transformers as well as a complex phase shifting control technique increasing the overall cost of the system [6].

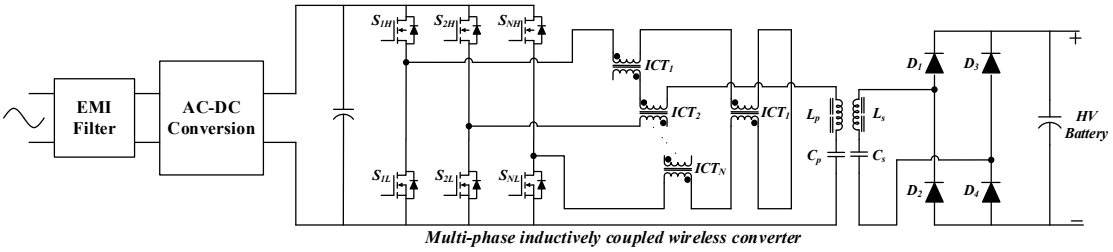


Fig. 1.10 IPT charger employing multi-phase inductively coupled wireless converter[34]

1.3.3 Capacitive charging

A capacitive power transfer (CPT) system is an alternative structure employing the near field magnetic resonance principle to transfer power wirelessly from a transmitter pad to a receiver pad with large air gap. A typical block diagram representation of the various stages involved in an CPT system is illustrated in Fig. 1.11 [35].

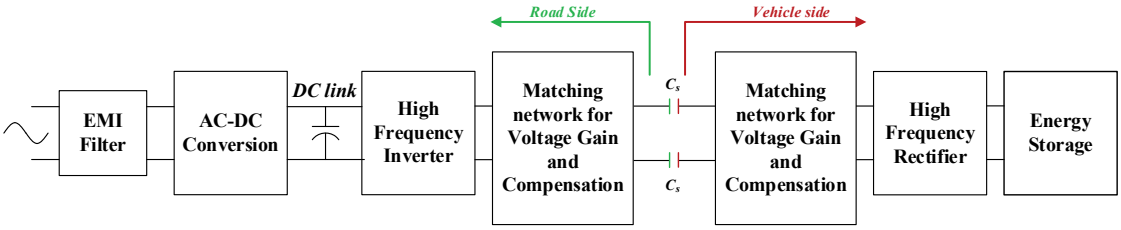


Fig. 1.11 Typical structure of a CPT system for EV charging

The vehicle side components designated in Fig. 1.11 facilitate the conversion of grid voltage AC to an intermediate DC voltage which is converted to a high frequency AC (HF-AC) voltage to be capacitievly coupled to the vehicle side components. The AC-DC conversion stage is similar to the front-end PFC stage of a conductive charger but present off-board the vehicle. Since, the capacitance formed by parallel plate structures is very low in value multi-MHz frequency operation is required for enabling resonant power transfer.

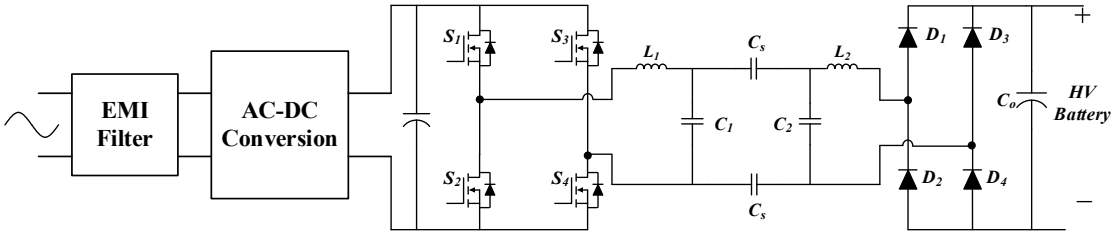


Fig. 1.12 CPT structure presented by researchers in [35]

Fig. 1.12 presents the CPT topology proposed by researchers in [35] capable of transferring 589W of power across an air gap of 12 cm with the help of a 6.78MHz switching operation. The proposed topology uses an H-bridge structure at the input inverter stage along with a LCC compensation network providing soft-switching characteristics to reduce switching losses at high frequency operation. The power transferred through the electric field in an air gap generates the secondary current which is rectified with the help of a diode rectifier to supply the high voltage battery.

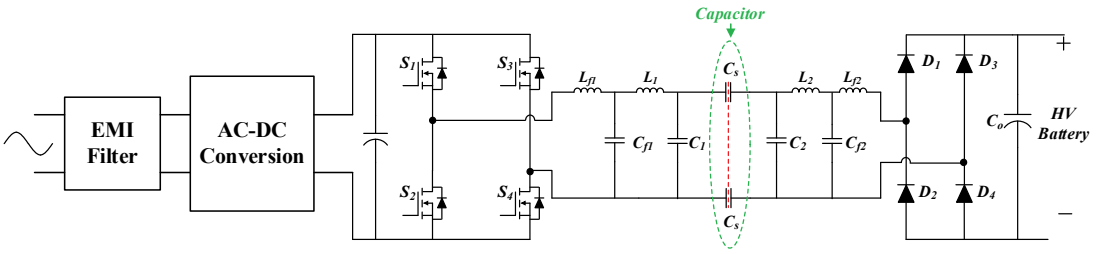


Fig. 1.13 CPT structure presented by researchers in [36]

A double sided LCC compensation based CPT system was proposed by researchers in [36]. The proposed system has reported efficiency of 90.8% for dc-dc stage alone at an air gap of 150mm when transferring 2.4kW power. The proposed converter uses a switching frequency of 1MHz with coupling capacitive pads of 610mm x 610 mm in size.

In this thesis, a CPT system is not considered for integration with conductive charger majorly because of the multi-MHz operation requirement which enforces more modification to on-board components for efficient operation. Additionally, the CPT system depends on the permittivity between the metal plates which could potentially be affected by the presence of environmental factors such as humidity.

1.4 Thesis Objectives

Currently wired charging is the customary method of delivering electric energy to the storage elements present onboard of EVs. Thriving inclination towards design of autonomous vehicles have shaped wireless charging as an attractive solution in favor of complete autonomy. Until the wireless charging infrastructure as well as interoperability standards are completely developed, wired and wireless chargers have to co-exist onboard the vehicles for user convenience. Current solutions for wireless charging requires additional components onboard the vehicle leading to increased size, weight and volume.

Incorporation of an entire parallel wireless charging system on-board an EV, either during manufacture or after-market shrinks the electric range of vehicle.

The need for co-existence of power electronic interfaces for wired and wireless chargers onboard the vehicle leads to an opportunity to develop integrated solutions. Typical OBC configuration includes an active bridge which can potentially act as a rectifier stage of wireless system. This removes the need of additional power electronics onboard the vehicle for wireless power conversion, as well as reduces cooling and cabling requirements of wireless system.

Subsequently, the major research problems on which research effort has been focused in this work are briefly as follows:

- Development of novel integration architectures to combine conductive and inductive charging system for electric vehicles
- Conducting optimized designs for different integral power conversion stages i.e. (i) off-board components including power factor correction rectifier, primary side wireless compensation network, inductive coil and (ii) vehicle onboard components including a secondary side compensation network and a rectifying stage.
- An extended harmonic analysis (EHA) method for analyzing the inductive power transfer system with multiple resonant frequencies, which will lead us in obtaining the voltage gain and calculating the component stresses of the wireless stage with higher accuracy at an operating frequency different from either of the resonant frequencies.
- Development of a novel analog circuit based phase synchronization method, which controls the switching of the devices of the onboard rectifying stage and ensures

zero voltage switching (ZVS) of all the devices without adding any sampling error based complexity unlike a digital controller and facilitates enhancement of power stage conversion efficiency.

1.5 Major Contributions

The main contributions of this research work are as listed below

1) Three novel architectures capable of integrating on-board components of wireless chargers to the existing wired chargers are proposed. Among the proposed solutions, solution III is selected to evaluate the system in laboratory as it require minimum power conversion stages.
2) A comprehensive loss evaluation of various bridgeless power factor correction (PFC) circuits are carried out to select an off-board AC-DC conversion stage for the development of a 3.3kW integrated charging structure. . The totem pole PFC structure exhibits minimum loss for 3.3 kW operating condition and hence is selected for implementation. A detailed small signal averaged model including the effects of series resistance in input inductor and output capacitor is developed to design the dual loop control structure. As a proof of concept, a laboratory prototype of the totem pole PFC is built, which achieves a full load efficiency of 97.39% while drawing input current with a power factor of 0.9993 and THD of 2.08% at a nominal grid voltage of 240 V_{rms}.
3) A wireless DC-DC stage capable of transferring 3.3 kW over an air gap of 10cm is developed in lab to evaluate the proposed charging system. A set of wireless coils using ferrite back plates are designed and manufactured in lab based on ANSYS Maxwell simulations. An EHA based modeling approach is used to analyze the

stress of various resonant components. The designed passive rectification based wireless DC-DC stage achieves a full-load efficiency of 94.2%

4) To improve the overall efficiency of proposed charging system an analog synchronous rectification circuit is proposed which uses secondary side sensed current to auto synchronize the active bridge of on-board charger. The proposed synchronization structure can enable secondary ZVS operation by generating programmed phase lead. To evaluate the improvement in efficiency by using the proposed analog circuit, a wireless DC-DC with active rectification is implemented which achieves a full load efficiency of 95.42 %. An efficiency improvement of >1.25% is achieved by active rectifier based solution compared to passive rectification over the load range.
5) Finally, the proposed integrated wireless charger is implemented using various building blocks developed by this work. A laboratory prototype is realized to evaluate the overall system characteristics. The integrated wireless charger was able to transfer 3.3kW power from grid to load with a conversion efficiency of 92.77% while drawing input current with a power factor of 0.9994 and 1.3% THD.

1.6 Synopsis of the dissertation

In Chapter 2, a comprehensive review of existing integrated conductive and inductive charger solutions are carried out. Multiple integration architectures capable of on-board topological integration of conductive and inductive chargers are proposed. Furthermore, system level implementation structures based on the proposed architectures are introduced.

In Chapter 3, the key design considerations of an off-board input rectification stage for the proposed integrated chargers are introduced. A comprehensive review of various active

front end converters is carried out; a critical loss comparison study is completed to select the most suitable topology for the charger specifications. Detailed small single modeling of the selected topology is carried out to design a suitable control structure capable of meeting the charger requirements. A laboratory prototype of the selected single phase rectifier is implemented and evaluated to validate the proposed solution.

In Chapter 4, the overall design of a wireless dc-dc stage is presented, where a brief introduction to IPT technology as well as a comprehensive review of various compensation structures are carried out to select a suitable compensation topology for the proposed charger. The design of charging coils or pads form a critical component in enabling an IPT system. Hence, various coil structures are reviewed and a suitable topology is selected for implementing laboratory level prototype based on design specifications. In order to design the compensation network a system level modeling of the wireless dc-dc conversion stage is carried out with the help of a fundamental harmonic approximation (FHA) technique. The inaccuracies in the developed system based on FHA model led to the development of a novel extended harmonic approximation (EHA) modeling method for accurate design of an IPT system. A laboratory prototype of the wireless DC-DC stage is developed and evaluated to substantiate the proposed design.

In Chapter 5, an analog synchronous rectification circuit is proposed to enable active rectification of wireless on-board rectifier. The proposed solution eliminates the need of any onboard microcontroller or high frequency synchronization signal transmission from the primary side to enable active rectification. As a proof of concept verification, a laboratory prototype is developed and assessed to quantify the improvement in system

efficiency. Additionally, an integrated wireless charger proposed in Chapter 2 is successfully built and evaluated to demonstrate the feasibility of the proposed solution.

Finally, in Chapter 6, relevant conclusions from the research work performed are summarized and several future research topics for further performance enhancement of the proposed charging structures are discussed in brief.

Chapter 2: Integrated wireless charging system architecture

2.1 Background review of existing integrated charging solutions

The strict volume and weight requirements imposed by automobile industry has always favored integration of components onboard the vehicle. The trend for integration is a potential reason for proposing the concept of an integrated wireless/onboard charger solution with a smaller battery pack reducing cost and weight of vehicle as a potential future trend [37]. Active research is being carried out by industries and research groups to develop such an integrated wireless charging solution.

Tesla Motors, Inc. currently holds a patent [38]for integration of inductive and conductive charging system with two different architectures. Fig. 2.1 illustrates a generalized block diagram from [38] where the integration takes place at the output stage of converter. The inductive and conductive system are two independent system without any reduced components leading to high volume requirement. The output battery can be simultaneously charged by both methods leading to a higher charging rate but at the expense of more cost and weight of charging system.

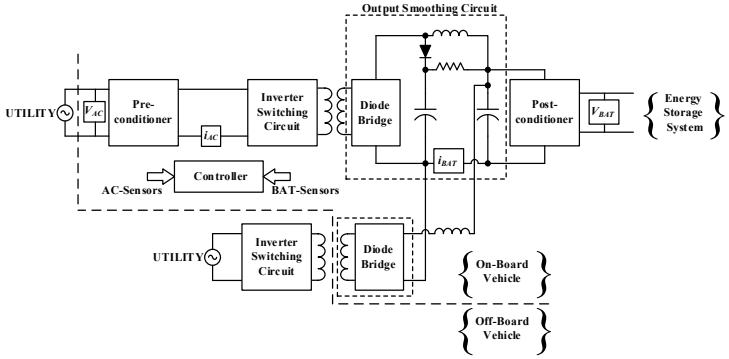


Fig. 2.1 Integrated configuration 1 proposed in [38]

An alternative solution is proposed in patent [38] as presented in Fig. 2.2 which integrates the output of wireless stage to the isolation transformer of conductive stage with help of power connectors and contactors. They have proposed the use of primary stage diode bridge to charge the output battery. The use of diode bridge as well as no provision for compensation network for wireless charging path will lead to a very low operation efficiency.

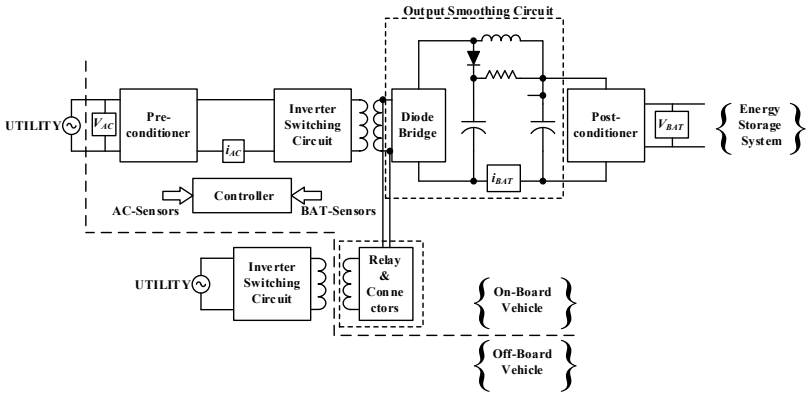


Fig. 2.2 Integrated configuration 2 proposed in [38]

Fig. 2.3 illustrates the integration of the wireless rectifier stage to the drive train boost converter as proposed by researchers in [39]. The proposed wireless system requires additional diodes to be included in the drive train circuit and leads to lower efficiency due to the conduction loss. Additionally the conductive charging system is still on-board the vehicle as an independent solution.

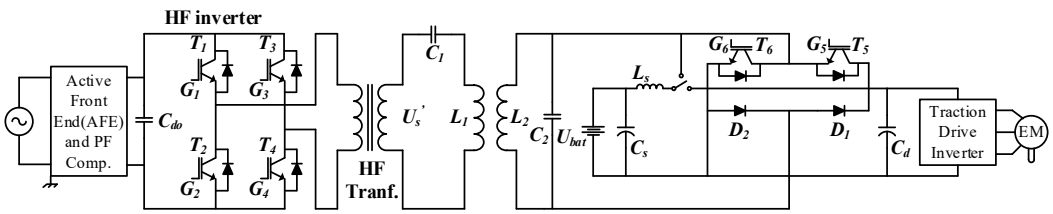


Fig. 2.3 Integrated configuration proposed in [2-3]

An alternative integration solution proposed by researchers in [40] illustrated in Fig. 2.4 uses a coupled magnetic structure that integrates the isolation transformer of plugin charger and receiver coil of inductive system. The coupled design leads to constrained parameters for both conductive and inductive charging system reducing the range of operation. Moreover, the design of isolation transformer for plugin charger with the help of ferrite plate structure leads to a lower coupling than a conventional transformer if proper design constrains are not met. Non-optimized design of transformer due to additional constraints introduced by wireless integration can impact the overall efficiency of conductive charging system.

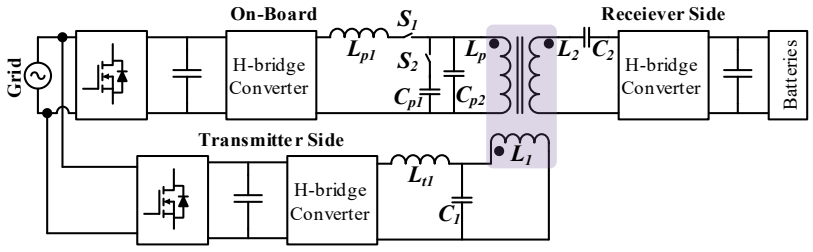


Fig. 2.4 Integrated configuration proposed in [2-4].

2.2 Proposed Integrated Wired and Wireless Charging Architecture

In this thesis, we propose a topological integration solution with existing onboard charger that reuses the existing components onboard and facilitate conductive and inductive charging independently. The aim of this charging integration is to reduce the overall weight and volume of required power electronics components onboard the vehicle. The proposed charging architecture can be classified into three different solutions based on the position of integration.

2.2.1 Solution I

Fig. 2.5 illustrates the proposed integration solution I of inductive and conductive charging system with the help of an interfacing circuit. The interfacing circuit that helps to bridge the inductive and conductive charging system is introduced before the isolated switching rectifier stage. The inductive charger reuses the switching elements of isolated switching rectifier to convert the high frequency AC output from compensation network to DC to be supplied to the energy storage element.

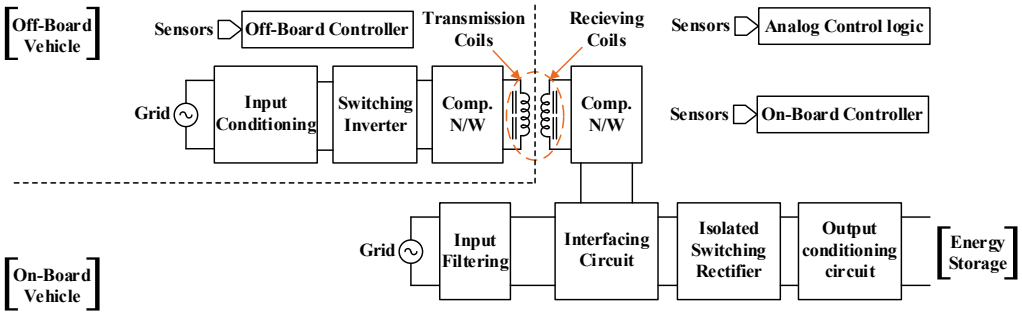


Fig. 2.5 Proposed Integration solution I at power factor correction stage of onboard charger

The main components of charging system deployed on-board vehicle as a part of Solution I are

Input filtering stage: The input from grid is connected to an EMI filtering stage of onboard stage using charging interface meeting SAE J1772 standard for grid connected system. The filtering stage may additionally include passive storage, decoupling elements required for operation of the circuit. This stage is mandatory for all the solutions proposed above to meet the current quality requirements. In Solutions II and III this stage is merged with the input conditioning stage.

Interfacing circuit: The interfacing circuit which acts as a bridge between inductive and conductive stage uses a combination of relays and connectors to provide the necessary

isolation required for independent operation of individual chargers. The interfacing circuit that helps to bridge the inductive and conductive charging system is introduced before the isolated switching rectifier stage for solution I.

Isolated switching rectifier: This stage acts as the main power factor correction (PFC) circuit which helps in rectifying AC input from grid to DC output with isolation. The major requirement of this stage for the proposed integration solution is presence of a rectifying bridge structure to act as secondary receiving side of inductive stage. Different combination of circuits could be used as a potential solution for this stage. Proposed solutions could be single stage or dual stage which meets the requirement of isolation and rectifying bridge structure.

Output conditioning circuit: The output of the isolated switching rectifier stage is connected to a conditioning circuit that can be passive or active depending on the requirement of energy storage device. The passive components could be capacitive or inductive in nature. Active circuits may include and is not limited to active buffering circuits or additional step up or step down converters to provide necessary voltage transformation.

On-Board Controller: An onboard controller provides the necessary switching signals to the interfacing circuit and rectifier circuit based on feedback signals from various sensors in circuit. The control logic depends on the isolated switching rectifier topology selected and may use different techniques such as pulse width modulation (PWM) control, pulse frequency modulation (PFM) control, phase shift modulation control or a hybrid structure including one or more control schemes based on requirement of charger. Additionally

wireless communication channels maybe integrated to the system to provide communication between off board and on board systems.

Analog Control logic: Additional analog control logic maybe included to existing onboard chargers or could be integrated to onboard controller for providing control signals to bridging circuit for efficient operation of inductive charger. Analog circuit includes current sensors, high speed comparator circuit, buffer interface, signal multiplexer, gate drive circuits and necessary interfacing connectors depending on selected topology.

Comp. N/W: Compensation network is a crucial component for on-board as well as off-board stages of wireless system to improve the power transfer ability by proper compensation logic. The compensation network may include passive component such as inductors and capacitors or active components that vary the effective impedance based on additional control logic.

Receiving Coils: Wireless receiving coils are placed on-board which is connected to the interfacing circuit through the compensation network. Different structures of wireless coils are possible based on the requirements of design.

Energy Storage: Energy storage element to be supplied could be a single battery source or a combination of different configuration of sources based on the selected topology.

Similarly, Off-board components are required for the operation of inductive stage which mainly includes

Input conditioning & Switching Inverter stage: The AC voltage from grid is converted to DC to be supplied to the switching inverter with the help of this circuit. This stage includes conditioning circuit such as EMI filter, storage elements and necessary switching elements to provide the voltage conversion. In case of a dual stage cascaded structure the input

conditioning stage deals with PFC operation while the inverter stage provides the necessary DC to AC voltage conversion at higher frequency. The switching inverter stage could be potentially integrated to the input conditioning stage in a single stage structure and can energize wireless transmitting coils through compensation network.

Transmission Coils: Wireless transmitting coils are placed off-board which is connected to primary grid through compensation network and associated switching structure. Different coil structures are possible based on the requirements of design.

Off-Board Controller: An off-board controller provides the necessary switching signals to the input conditioning stage and switching inverter network based on feedback signals from various sensors in circuit. The control logic depends on the chosen topology and could potentially employ techniques such as pulse width modulation (PWM), pulse frequency modulation (PFM), Phase shift control or a hybrid control scheme using one or more schemes. Additionally wireless communication channels, positioning control systems maybe integrated to provide communication between off board controller and on board systems.

2.2.2 Solution II

An alternate charging architecture (Solution II) is illustrated in Fig. 2.6, where AC output from receiving coil after compensation is supplied to the isolation transformer of conductive charger with the help of proper interfacing circuit structure. The proposed Solution II introduces additional level of isolation from grid stage but reduces the stages of power conversion improving conversion efficiency.

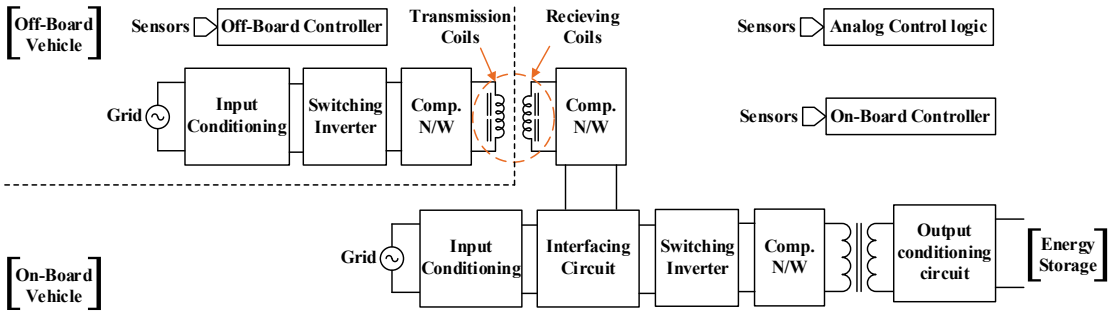


Fig. 2.6 Proposed solution II

2.2.3 Solution III

An extension to Solution II is presented in Fig. 2.7 .The proposed bridging is introduced after the isolation transformer of conductive charger. Solution III uses the output conditioning circuit rectification stage to converter the high frequency AC supplied from compensation network to DC.

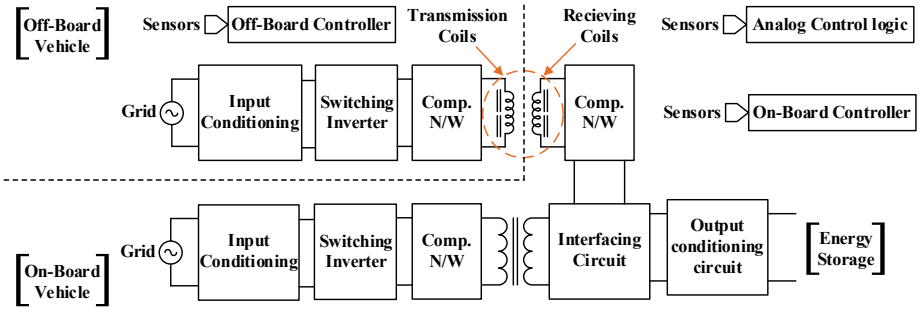


Fig. 2.7 Proposed Integration solution III

The main components of the proposed solutions II and III are summarized below:

Input Conditioning & Switching Inverter Stage: The Isolated switching rectifier stage presented as a part of Solution I is decoupled into two parts for Solution II and Solution III. Input conditioning stage merges the PFC stage as well as the EMI filter and provide a grid interface to meet the required standards. The DC output of input conditioning stage is connected with the help of interface circuit to a switching inverter to generate high

frequency AC signal. Alternatively a single stage structure could be used for Solution III where the switching inverter network is merged with input conditioning circuit and directly provides high frequency AC signal from input grid voltage.

Comp. N/W: Compensation network is an essential part of off-board and onboard stage, which helps in improving power transfer capability. This stage also helps in improving efficiency by introducing soft switching characteristics to the circuit. The compensation network may include passive component such as inductors and capacitors or active components that vary the effective impedance based on additional control logic.

Interfacing circuit: The interface circuit uses combination of relays, connectors and active devices to provide the necessary isolation required for operation of individual chargers. It may include passive compensation networks required as a part of conductive stage. The interfacing circuit is introduced before the isolation stage of the onboard charger topology in case of Solution II and hence inherently provides an extra level of isolation to the inductive stage. Alternatively, Solution III introduces bridging after the isolation transformer but removes the additional constraints on transformer design imposed by integration proposed in Solution II.

Output conditioning circuit: The output of the isolating transformer is connected to a conditioning circuit that can be passive or active depending on the requirement of energy storage device. The passive components could be capacitive or inductive in nature which can act as storage components or filtering components in case of resonant based structures. Active components may include active buffering circuits or additional step up or step down converters to provide necessary voltage transformation.

Energy Storage: Energy storage element to be supplied could be a single battery source or a combination of different configuration of sources based on the selected topology.

On-Board Controller: An onboard controller provides the necessary switching signals to the input conditioning stage, switching inverter and interfacing circuit based on feedback signals from various sensors in circuit. The control logic depends on the chosen topology and could potentially employ techniques such as pulse width modulation (PWM), pulse frequency modulation (PFM), Phase shift control or a hybrid control scheme using one or more schemes. Additionally wireless communication channels maybe required to provide communication between off board controller and on board systems for power flow control.

Analog Control logic: Additional analog control logic maybe included to existing onboard chargers or could be integrated to onboard controller for providing control signals to bridging circuit for efficient operation of inductive charger. Analog circuit includes a combination of sensors, high speed comparator circuit, buffer interface, signal multiplexer, gate drive circuits and necessary interfacing connectors depending on selected topology.

Off-Board Controller: An off-board controller provides the necessary switching signals to the input conditioning stage and switching inverter network based on feedback signals from various sensors in circuit. The control logic depends on the chosen topology and could potentially employ techniques such as pulse width modulation (PWM), pulse frequency modulation (PFM), Phase shift control or a hybrid control scheme using one or more schemes. Offboard controller integrates wireless communication channels along with position control systems to facilitate power flow control to vehicle systems.

Transmission Coils: Wireless transmitting coils are placed off-board which is connected to primary grid through compensation network and associated switching structure. Different coil structures are possible based on the requirements of design.

Receiving Coils: Wireless receiving coils are placed on-board which is connected to the interfacing circuit through the compensation network. Different structures of wireless coils are possible based on the requirements of design.

2.3 System level implementation structures for proposed solutions

Fig. 2.8 presents one of the feasible topology derived from Solution I, where the selected isolated switching network is an interleaved totem pole PFC cascaded with a half bridge CLLC converter (HB-CLLC). The output of HB-CLLC converter is fed to a capacitor which acts as the output conditioning circuit. Inductive charger uses a dual stage cascaded converter, where again a totem pole PFC circuit acts as input conditioning stage followed by a full bridge switching inverter exciting the transmission coil through a compensation network. The receiving coil is powered by transmitting coil and supplies energy to a compensation network which is integrated to conductive stage with the help of interfacing relays Rl_1 and Rl_2. The analog control logic supplies the necessary driving pulse to the input bridge for efficient operation of wireless rectifier. More detailed analysis and selection methodology will be presented in following chapter.

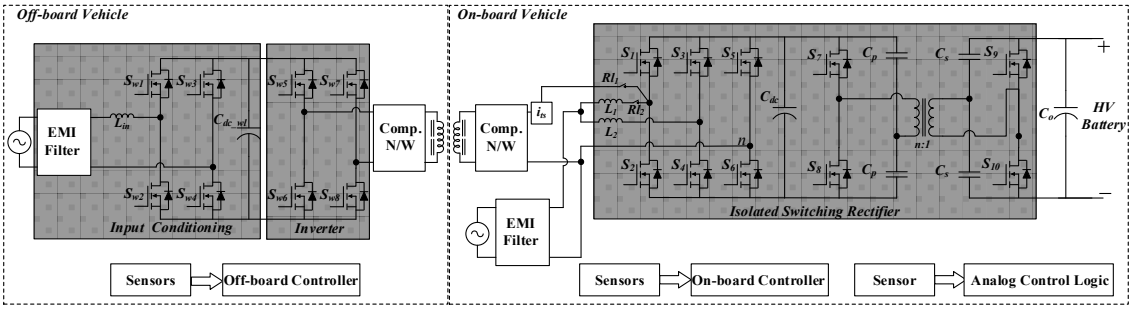


Fig. 2.8 System Level implementation of Solution I

Solution II integrates the wireless charger at the isolation stage of conductive charger onboard the vehicle as presented in Fig. 2.9. The input conditioning stage of onboard charger uses an interleaved totem pole structure connected in cascade with the primary full bridge switching inverter of an a dual active bridge (DAB) converter. The secondary output bridge of DAB along with dc capacitor acts as the output conditioning circuit supplying the high voltage (HV) battery. Off-board stage of inductive charger uses a dual stage cascaded converter, where a totem pole PFC circuit acts as input conditioning stage followed by a full bridge switching inverter exciting the transmission coil through a compensation network. The receiving coil is powered by transmitting coil and supplies energy to a compensation network which is integrated to conductive stage with the help of interfacing relay Rl_2. An additional relay Rl_1 is required to isolate the dc link of PFC circuit to prevent voltage buildup during operation of inductive circuit. The analog control logic supplies the necessary driving pulse to the input bridge for efficient operation of wireless rectifier. This solution introduces additional constraints in the design of DAB transformer as the magnetizing inductance and leakage inductance lies in active power path of inductive secondary circuit. Due to the constrained design this solution is not further pursued in the following chapter.

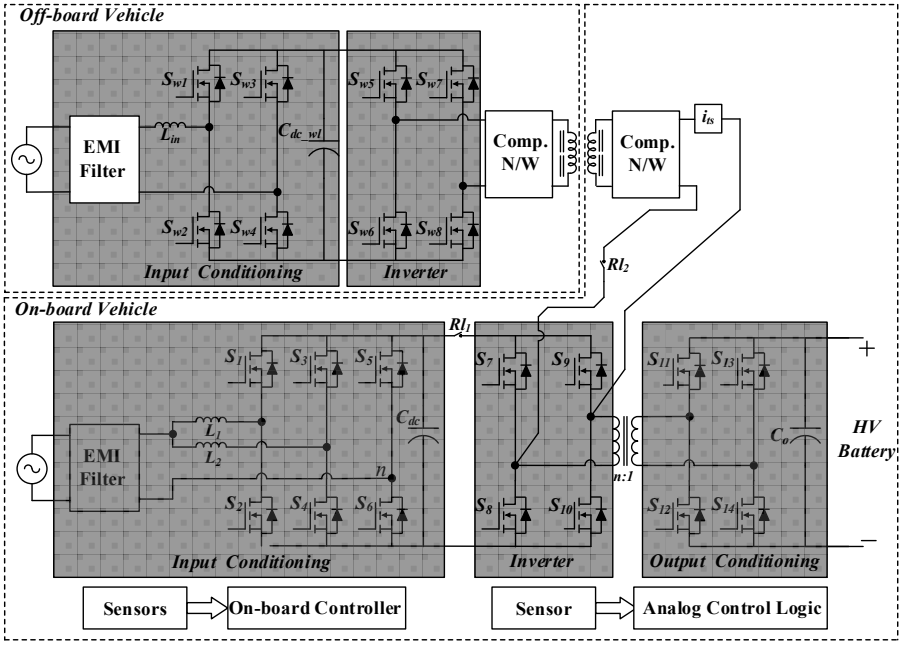


Fig. 2.9 System level implementation of Solution II

Fig. 2.10 presents a feasible system topology for Solution III. The inductive receiver output is integrated after the isolation stage of conductive charger onboard reusing the output switching bridge for rectification. Similar to solution II input conditioning stage of onboard charger uses an interleaved totem pole structure connected in cascade with the full bridge switching inverter of an a dual active bridge (DAB) converter. The output bridge of DAB along with dc capacitor acts as the output conditioning circuit supplying the high voltage (HV) battery which makes integration possible for this solution. A dual stage cascaded converter structure is used in off-board stage of inductive charger, where a totem pole PFC circuit acts as input conditioning stage followed by a full bridge switching inverter exciting the transmission coil through a compensation network. The receiving coil is powered by transmitting coil using magnetic field and supplies energy to a compensation network which is integrated to conductive stage with the help of interfacing relays Rl_1 and Rl_2. Relay Rl_1 isolates the transformer and primary side completely from power path and

hence there is no restriction imposed on the design of DAB transformer. The extra isolation introduced by the high frequency DAB transformer in case of Solution II is lacking in this solution but the wireless coils inherently introduces isolation between off-board and on-board charging elements which makes extra isolation an optional requirement. This solution can potentially give similar efficiency as that of an independent wireless system as no extra stages of conversion are added to the power flow.

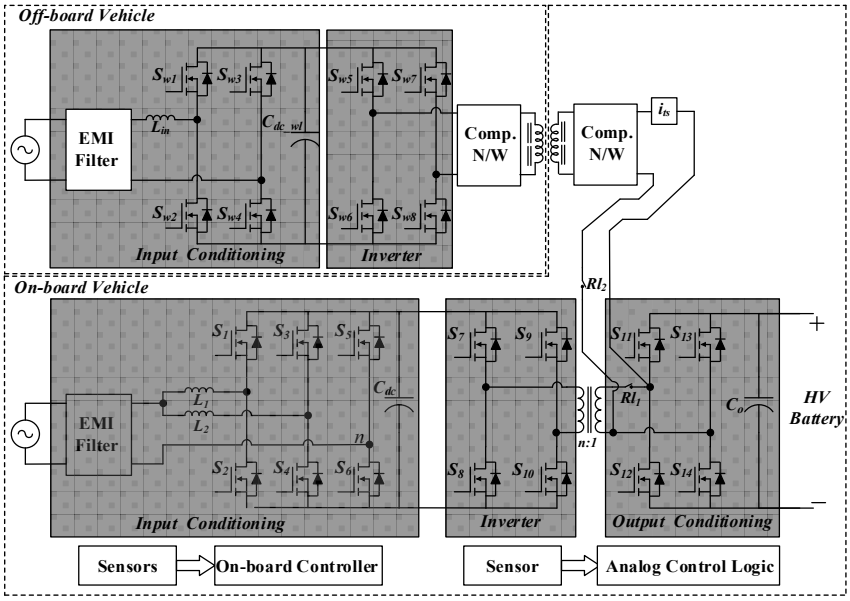


Fig. 2.10 System level implementation of Solution III

2.4 Summary

In this chapter, a comprehensive review have been carried out on the existing integrated conductive and inductive wireless charging solutions proposed by industries and research groups. Three different architectures for developing integrated inductive and conductive charging solutions are presented, classified based on position of integration of two stages. Solution I and III does not impose any additional constraints on conductive charging components while Solution II imposes additional constraints on the design of

isolation transformer parameters. Solution III has the potential of highest efficiency among the three proposed architectures, since no extra power conversion stage is introduced in inductive charging path compared to an independent wireless charging system. Finally, feasible system level implementation topologies for various architectures are introduced. In order to understand the rationale behind the selection of various structures presented as a part of system level implementation of proposed solution detailed loss analysis and topology selection is carried out in the following chapter.

Chapter 3: Design and Evaluation of Off-board AC-DC Conversion Stage

3.1 Introduction

The basic architectures capable of integrating inductive and conductive charging of electric vehicle were introduced in previous chapter. The complete system includes various stages of power conversion which has to be individually optimized to maximize the overall efficiency of system. The system includes both off-board as well as on-board components which needs to be cautiously designed to meet power transfer requirement. The target system proposed to be developed in laboratory focuses on charging a plugin hybrid electric vehicle (PHEV) with smaller battery capacity.

3.2 Off-board system design

The proposed integrated charger system requires off-board components to energize the wireless transmission stage. As presented in chapter 2 the off-board system transforms single phase AC grid voltage to DC voltage with the help of input conditioning stage. The output of AC-DC stage is supplied to a switching inverter connected in cascade to generate high frequency AC energizing the transmitting coil through appropriate compensation topology. The proposed charger is designed based on the key parameters listed in Table 3.1 derived from commercially available charging solutions meeting various standards of charging [8]-[9].

3.1 Selection of input conditioning stage

The input conditioning stage of wireless charger is an active front end rectifier or power factor correction (PFC) circuit that ensure the current drawn from the utility grid has low

distortion ensuring high power quality and high power factor [9]. As required by the Europe standard IEC 61000-3-2 [41], any power converter connected to the grid with power consumption over 75W needs to have front-end PFC stage to meet the harmonic regulation standards. Similarly, in US SAE J2894 [42], the U.S. National Electric Code (NEC) 690 [43] standards specifies the power quality requirements of any interface connected to grid.

Table 3.1 Key charger specifications

Parameter	Value
Input voltage range (single Phase)	85 - 265 Vrms
Output battery voltage range	250 – 400 V
Maximum output power rating	3.3 kW
Maximum output current	8.25 A
Maximum input current (rms)	15.1 A (@ nominal voltage)
PFC target efficiency	97.5 %
Maximum input current Total Harmonic Distortion (THD)	< 5 %
Target integrated charger efficiency	92 %

In order to charge the battery under varying voltages, supplied from universal input voltage range as specified in Table 3.1 boost derived PFC topologies are appropriate candidates for evaluation. Traditional boost based PFC topologies presented in Fig. 3.1(a) and Fig. 3.1(b) use a diode bridge in cascade with boost converter to generate high quality input current. Even though high quality current with minimum distortion can be generated, the diode bridge causes significant power loss leading to significant drop in efficiency as well as increased cooling requirements leading to reduced power density [10], [44].

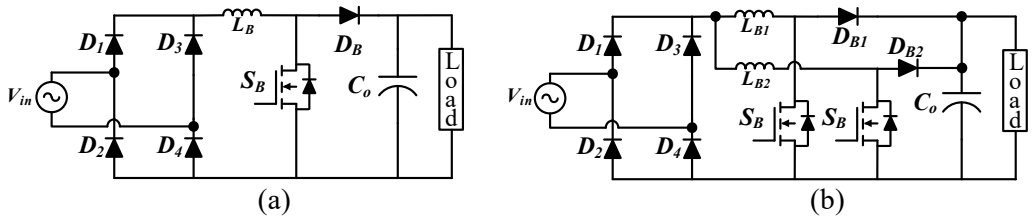


Fig. 3.1 Traditional PFC topology (a) boost PFC (b) interleaved boost PFC

Boost-derived bridgeless converters are an attractive option to meet the requirements of high efficiency, high power density and high power quality AC-DC conversion. The bridgeless topologies have lower conduction losses due to reduced number of semiconductor devices in current path leading to high efficiency operation [10], [44]. Even though adopting bridgeless PFC circuits leads to higher efficiency, they inherently introduces a considerable amount of conducted common mode (CM) noise compared to a conventional diode bridge PFC due to the presence of high frequency switch node voltage between line ground and output ground [45]. Electromagnetic interference (EMI) compliance is a critical requirement for any grid connected converter [46]–[48]. In this regard, various active and passive methods have been proposed to reduce the CM noise generated by bridgeless circuit[47]–[49]. In order to meet the key design constraints listed above, the two most suitable topologies among the alternatives presented in [10], [44] have been selected for evaluation. A quantitative loss analysis along with a qualitative volume analysis is carried out to select the appropriate topology for implementation on laboratory prototype from among two topologies presented in Fig. 3.2.

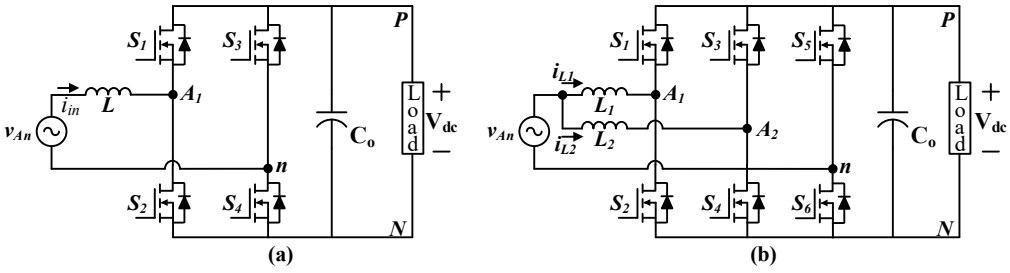


Fig. 3.2 Bridgeless boost-derived topologies (a) Totem pole or H-bridge (b) Interleaved totem pole

3.1.1 Basic operation principle and design details

The primary objective of any PFC rectifier is to shape the input current to follow input voltage with same phase and frequency. A bridge network of MOSFETs helps in shaping the grid current to follow a pure sinusoidal reference by driving each switching leg with complementary pulses separated by a dead band. The input inductor helps in boosting the voltage and filtering the input current's harmonic content. Depending on the switching scheme as well the topology the operation of the boost-derived topologies presented in Fig. 3.2 are evaluated below.

3.1.1.1 H-bridge

The overall structure of a single phase H-bridge PFC is presented in Fig. 3.2 (a). The key operating waveforms under this switching are presented in Fig. 3.3. In case of H-bridge operation, there are two switching operation per switching cycle charging and discharging the input inductor.

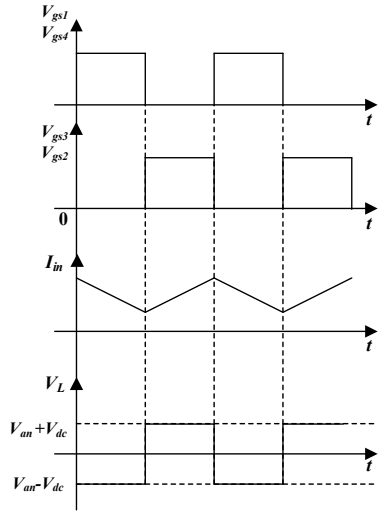


Fig. 3.3 Key operating waveforms under H-bridge switching scheme

The input voltage to the circuit is varying in a sinusoidal fashion but since the switching is happening at very high frequencies with respect to the input voltage we can essentially consider the input to be a constant voltage for every cycle. In order to shape the input current, the duty ratio which indicates the ratio of turn-on period to the switching period of a particular switch is varied in sinusoidal fashion. During positive half cycle operation of input AC voltage Fig. 3.4 shows the power flow path for the two switching intervals. It is evident from Fig. 3.4 that the neutral point of input supply is oscillating between 0 and V_{dc} and hence this topology inherently introduces higher common-mode EMI.

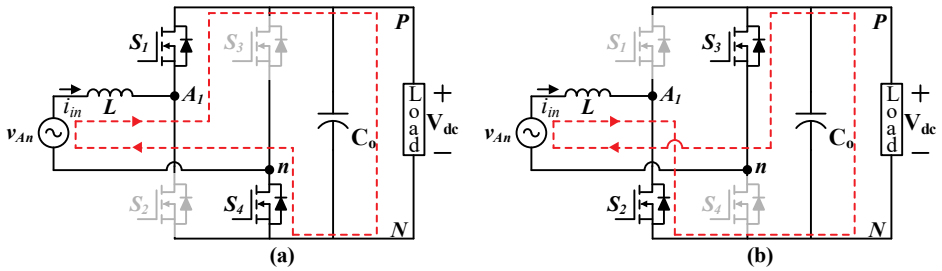


Fig. 3.4 Power flow during AC positive half-cycle under H-bridge operation (a) Discharging cycle (b) Charging cycle

3.1.1.2 Totem-Pole

The structure presented in Fig. 3.2(a) can be modulated in an alternate fashion to shape the input current with only one switching operation per cycle which is referred to as totem-pole switching scheme. The key switching waveforms under this mode of operation for positive half-cycle of input voltage are presented in Fig. 3.5.

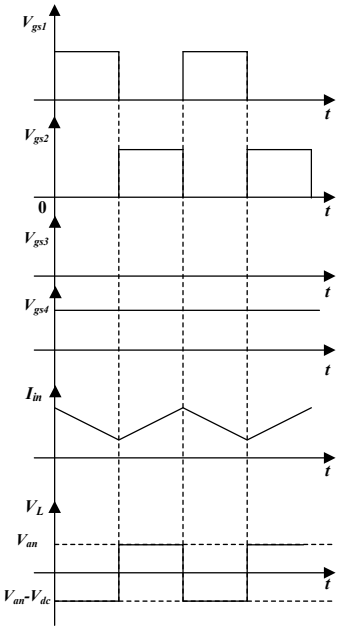


Fig. 3.5 Key operating waveforms for positive half-cycle under totem pole switching scheme

During entire positive half cycle only S_4 remains ON while S_3 remains OFF as can be inferred from Fig. 3.5. Switching transition in this leg happens only during input voltage polarity change which occurs at a rate of twice the line frequency and hence leads to negligible switching loss. The power flow path under totem pole operation is presented in Fig. 3.6. It can be concluded based on the operating principle that there is essentially no switching node voltage generated at the neutral point unlike H-bridge operation, which can potentially reduce the overall generated common mode EMI from the circuit.

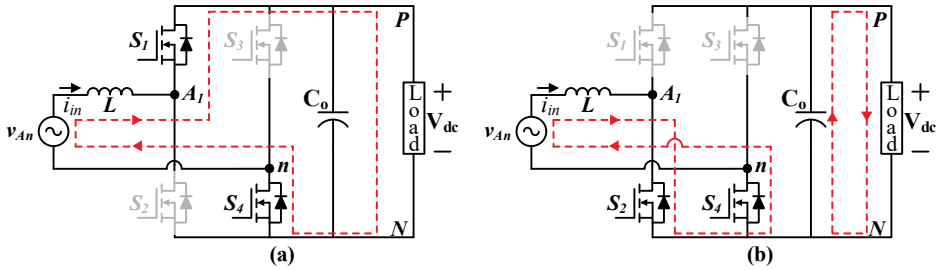


Fig. 3.6 Power flow during AC positive half-cycle under totem pole operation (a) Discharging cycle (b) Charging cycle

3.1.1.3 Interleaved Totem-Pole

In order to potentially further enhance the efficiency of PFC circuit an interleaved version of totem pole structure as shown in Fig. 3.2(b) can be used. The interleaved structure splits the total input current into two parts shared by two half bridges formed by switches $S_1 - S_4$ along with single slow switching bridge formed by S_5, S_6 carrying the return current. The power flow path of an interleaved PFC structure is presented in Fig. 3.7.

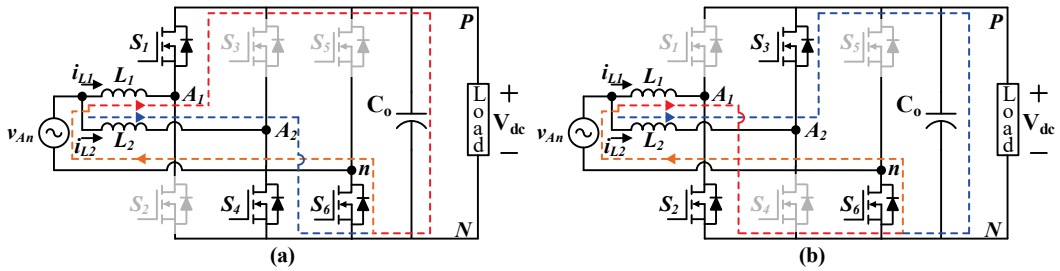


Fig. 3.7 Power flow path for AC positive half-cycle (a) L_1 discharging L_2 charging (b) L_1 charging L_2 discharging

The sharing of current can be phase shifted at 180° with each other facilitating ripple cancellation along with reduced input inductor value per phase. Since two half bridges are sharing the current, two switching operations per cycle are required for power flow carrying half the current through each switch which reduces the conduction loss in the switches. The key switching waveforms of the converter for positive half cycle operation is presented in Fig. 3.8.

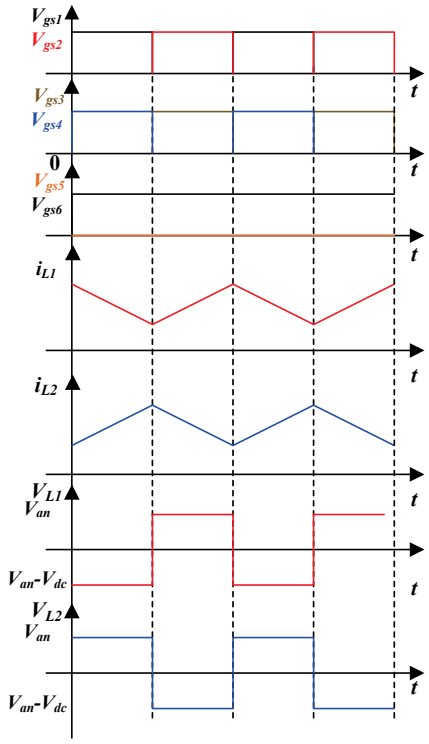


Fig. 3.8 Key operating waveforms for positive half-cycle operation with interleaved totem pole-structure

3.1.2 Discussions

The key characteristics of the proposed solutions are summarized in Table 3.2. The H-bridge topology leads to higher number of switching per cycle compared to totem pole structure but similar to interleaved totem pole. Interleaved totem-pole structure requires two switching per cycle but the current flowing through the switches are halved compared to H-bridge leading to reduced overall losses. Similarly, compared to other structure interleaved totem-pole requires 2 boost inductors but with reduced values due to ripple cancellation and can lead to potentially lower volume requirements. In order to select the topology for implementation a critical loss evaluation of all proposed topologies is carried out in the following section.

Table 3.2 Key characteristics of topologies under evaluation

Topology	# of switching per cycle	EMI generation	# of Boost inductors
H-bridge	2	High	1
Totem-pole	1	Lower	1
Interleaved Totem-pole	2	Lower	2

3.2 Loss Comparison

The proposed integrated wireless charging solution involves multiple stages of power conversion and hence maximizing efficiency over each stage is a critical requirement in order to meet overall charger efficiency. The target efficiency for PFC stage as proposed in Table 3.1 is 97.5% at full load of 3.3 kW.

η_{max} @ full load = 97.5 %

Total loss budget = (1-0.975)*3300 =82.5 W

Nominal input voltage = 240 Vrms

Minimum power factor @ full load = 0.99

$$i_{inrms} = \frac{P_{out}}{\eta_{int} V_{inrms} pf} = \frac{3300}{0.92*240*0.99} = 15.096\ A\ \approx 15.1\ A \qquad (3.1)$$

3.2.1 Capacitor Selection

The output capacitor is sized so as to maintain output voltage within a specified ripple value Since all the proposed topologies leads to double frequency ripple at output the selected capacitor values can be used for all the proposed structures and switching schemes.

Max ripple (r_{cap}) = 5 %

Ripple requirement

$$C_o \geq \frac{P_o}{2.\pi.f_{ripple} r_{cap}.V_{dc}^2} = \frac{3300}{2*\pi*120*0.05*400^2} = 0.55mF \quad (3.2)$$

$$i_{ripple} = \frac{C.\mathrm{r_{cap}}.V_{dc}.\omega_{ripple}}{\sqrt{2}} = 5.86A \quad (3.3)$$

A capacitor from nichicon LLG2W681MELC45 with 680µF, 450V rating is selected as the output capacitor. From, manufacturer datasheet [50] we can infer that at 120Hz ripple the maximum ripple current that can be supplied by this capacitor is 2.82 Arms. From (3.3) we know that we have to supply 5.86A to sustain a ripple value of 5%. A combination of 3 capacitors in parallel is selected to sustain the ripple current equation.

$$r_{capn} = \frac{P_o}{2.\pi.f_{ripple} C_o.V_{dc}^2} * 100\% = \frac{3300}{2*\pi*120*2.04*10^{-3}*400^2} * 100\% = 1.3\% \quad (3.4)$$

$$i_{ripplen} = \frac{C.\mathrm{r_{capn}}.V_{dc}.\omega_{ripple}}{\sqrt{2}} = 5.66A \quad (3.5)$$

$$tan\,\delta = \omega C R_{esr} \quad (3.6)$$

$$R_{esr} = \frac{tan\delta}{2\pi f C} = \frac{0.2}{2*\pi*120*680\mu} = 390m\Omega \quad (3.7)$$

$$R_{eff} = \frac{R_{esr}}{3} = 130\ m\Omega \quad (3.8)$$

$$P_{Lcap} = i_{ripplen}^2 * R_{eff} = 5.66^2 * 130\ m = 4.16\ W \quad (3.9)$$

3.2.2 Design of input inductor

The value of input inductor is selected to maintain the maximum ripple to be less that specified value. Maximum ripple for each structure is derived based on volt-second balance condition [51] and is used to design the initial input inductor value based on the maximum allowable ripple requirements. As presented in previous section the ripple constraint for

interleaved totem pole structure is more relaxed compared to other structure due to inherent ripple cancellation. The initial core selection is based on Energy vs part number curve provided in manufacturer website. A flowchart for design of input inductor is presented in Fig. 3.9. The key design equations [51] required to complete the design process are given below.

$$N = \sqrt{\frac{L}{A_L}} \tag{3.10}$$

$$N_{new} = \frac{N}{A_L factor} \tag{3.11}$$

$$L_{new} = N_{new}^2 * A_{Lnew} \tag{3.12}$$

$$B = \frac{L\Delta I}{NA_e} \tag{3.13}$$

$$P_{core} = kf^a B_{pk}^b V_{core} \tag{3.14}$$

where N, N_{new} stands for # of turns, A_L stands for ratio of inductance to square of turns, $A_{Lfactor}$ stands for reduction % of A_L value due to DC bias, B represents the flux density, A_e is the area of selected core. Table 3.3 presents the ripple equation used to select the input inductor value. The coefficients k, b, a are loss constants provided by manufacturer of material to determine the core loss P_{core} which is directly proportional to frequency of operation (f), peak flux swing B_{pk} and core volume V_{core} [51]After design of inductor the total winding length as well as the rms current through the winding has to be calculated to compute the winding loss per inductor. The winding resistance for a given wire depends on the gauge of wire as well as the length of wire as presented in 3.15.

$$R_{litz} = \frac{\rho l}{A} \tag{3.15}$$

Table 3.3 Inductor design constraints

Topology	Design constraint	$i_{ripple}(\%)$	Δi_{Lmax}	$L(\mu H)$
H-bridge	$L \geq \frac{V_{dc}}{2\Delta i_{Lmax} f_s}$	20	3	960
Totem-pole	$L \geq \frac{V_{dc}}{4\Delta i_{Lmax} f_s}$	20	3	480
Interleaved totem-pole	$L \geq \frac{V_{dc}}{4\Delta i_{Lmax} f_s}$	50	3.75	381

The effective rms value of current flowing through inductor can be represented as a sum of rms input current plus a ripple of max magnitude which leads to $i_{winding}$ as defined below [3-14]

$$i_{winding}(rms) = \sqrt{\left(i_{inrms}^2 + \frac{\Delta i_L^2}{12}\right)} \tag{3.16}$$

The winding loss generated in inductor can be quantified as below

$$P_{winding} = i_{winding}^2 R_{litz} \tag{3.17}$$

Table 3.4 presents the final inductor design and the loss elements calculated using equations (3.14) and (3.17)

Table 3.4 Final designed inductor with loss analysis

Topology	H-bridge	Totem-pole	Interleaved totem-pole
Core part no:	3 x C058195A2	1 x 0058620A2	1 x C058195A2
Core Type	High-Flux powder	High-Flux powder	High-Flux powder
$L_{final}(\mu H)$	1010	556.88	395.46
# of inductors	1	1	2
N_{new}	36	45	39
$B(mT)$	61.25	51.56	83.02
Wire Gauge	12 AWG	12 AWG	15 AWG
$R_{litz}(m\Omega)$	45	27	45
$i_{winding}\ (A)$	15.13	15.13	7.63
P_{core}	17.16	10.36	2 x 14.3
$P_{winding}$	10.53	6.18	5.24
Total Loss	27.69	16.54	33.84

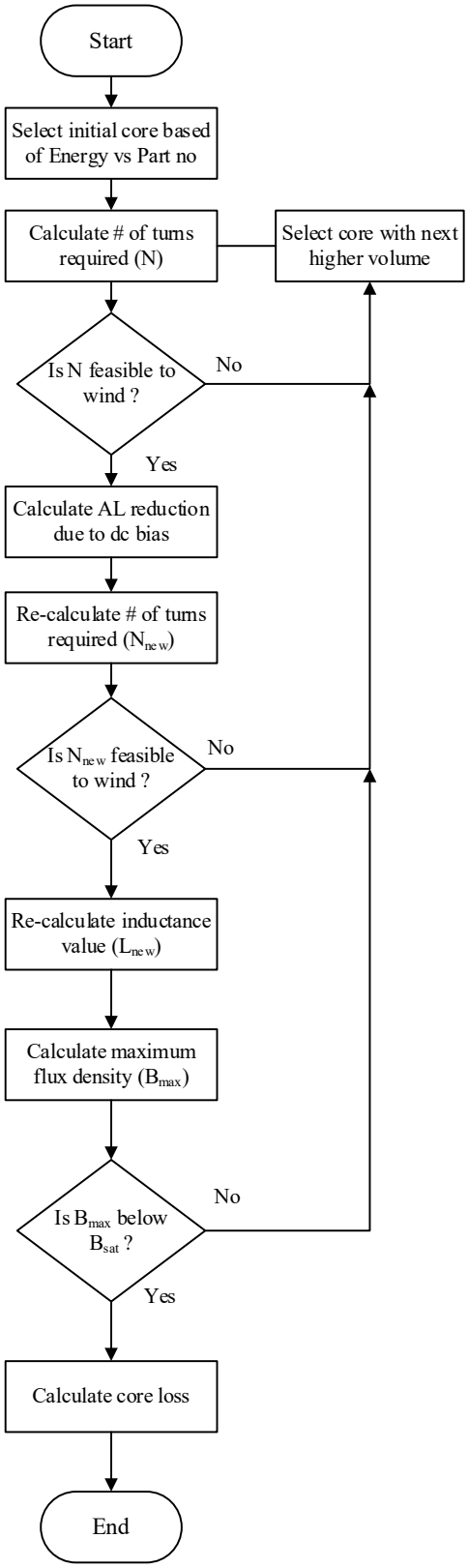


Fig. 3.9 Inductor design flowchart

3.2.3 Switching Loss evaluation

The totem pole structure working under continuous conduction mode (CCM) was a not popular choice for PFC due to inherent reverse recovery losses caused by silicon switches [10]. The advancements in field of semiconductors leading to development of WBG SiC switches with fast switching capability and minimum reverse recovery losses have helped in developing highly efficient totem pole PFC. Hence, to design the laboratory prototype SiC MOSFETs are used to design the PFC bridge.

Conduction Loss –Depending on no of switches in conduction the general expression for conduction loss can be evaluated as below

$$P_{cond} = N_c * i_{winding}^2 * R_{dson} \tag{3.18}$$

Where, N_c is the total number of switches in conduction

In case of totem-pole structure, there are 3 switches conducting per cycle where 2 of them carry half the input current value and the third carry full input current which is used to calculate the total conduction loss

Switching Loss – During turn ON or turn OFF instant some of switches are hard switched whereas the others are always soft switched hence the total switching loss is given by

$$P_{sw} = N_s * \frac{V_{dc} . I_{swrms} . f_s . (t_r + t_f)}{2} \tag{3.19}$$

$$I_{swrms} = I_{windingpk} \sqrt{\frac{4V_{pk}}{3 * \pi * V_{dc}}} \tag{3.20}$$

Where, N_s represents the number of hard switching per cycle, V_{pk} represents the peak input voltage, V_{dc}represents the output dc link voltage.

The switching loss for all the topologies are calculated using the loss equations presented above and tabulated in Table 3.5. It is evident that the switching loss for interleaved totem-pole structure is the lowest as two switches carry half the input current reducing overall conduction as well as switching losses.

Table 3.5 Switching loss estimation

Parameters	Topologies under evaluation		
	H-bridge	Totem-pole	Interleaved totem-pole
N_c	2	2	3
N_s	2	1	2
$i_{winding}$ (A)	15.1	15.1	7.63
i_{swrms}	12.82	12.82	6.48
MOSFET	C2M0080120D		
R_{dson} (mΩ)	80		
t_r (ns)	20		
t_f (ns)	19		
P_{cond}	36.48	36.48	27.58
P_{sw}	14	7	7
Total Loss	50.48	43.48	34.58

3.3 Selected Topology

A comprehensive loss evaluation of various active PFC topologies presented in Fig. 3.2 is completed in the previous section. Table 3.6 summarizes the results of loss evaluation. It

is evident from the total loss values that all the selected topologies could meet the potential target of 97.5% efficiency. Since efficiency maximization is a key requirement for the charger totem-pole structure is the ideal candidate for lab-implementation.

Table 3.6 Loss comparison of PFC topologies under evaluation

Loss Category		Topology		
		H-bridge	Totem-pole	Interleaved Totem-pole
Magnetic	Core loss	17.16	10.36	28.6
	Winding loss	10.53	6.18	5.24
Switches	Conduction loss	36.48	36.48	27.58
	Switching loss	14	7	7
Capacitor	ESR loss	4.16	4.16	4.16
Total Loss		82.33	64.18	72.54

3.4 Modeling and control

The key requirement of a PFC circuit is to shape the input current to follow input voltage with minimum harmonic injection to grid. A dual loop control structure is required to shape the input current while meeting the power requirements. In order to include the effects of non-ideal components used in the system a detailed small signal model is developed considering the effects of inductor winding resistance as well as dc link capacitor effective series resistance (ESR). The totem pole PFC circuit cycles through 4 modes of operation during a line cycle. Since the operation is symmetric in nature only positive half cycle operation is evaluated for modeling of the system. The equivalent circuits for positive half cycle of operation is presented in Fig. 3.10 below. The mathematical relationships in

positive half cycle is presented in Table XX. For negative half cycle operation, S3 remains ON and D period (S_1 ON) and (1-D) period (S_2 ON) is interchanged with respect to positive half cycle.

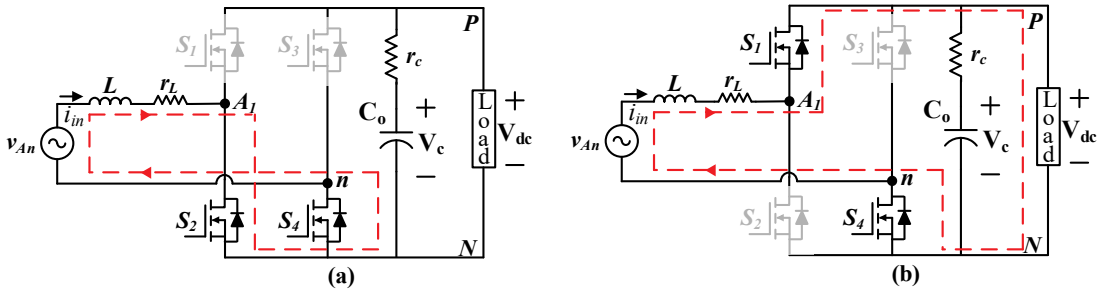


Fig. 3.10 Totem pole PFC equivalent circuit of operation positive half-cycle (a) D period (b) (1-D) period

Table 3.7 Mathematical Expressions for half cycle operation

D period	(1-D) period
$V_{in} = L\frac{di_{in}}{dt} + i_{in}r_L$	$V_{in} = L\frac{di_{in}}{dt} + i_{in}r_L + v_{dc}$
$i_c = C\frac{dv_c}{dt}$	$i_c = C\frac{dv_c}{dt}$
$V_c = -i_c(R_L + r_c)$	$i_{in} = i_c + \frac{v_{dc}}{R_L}$
$v_{dc} = v_c + i_c r_c$	$v_{dc} = v_c + i_c r_c$

3.4.1 Averaged large-signal model of totem pole PFC circuit

The averaged large-signal model of the circuit reproduces the average behavior of the power converter. Since, the converter cross-over frequency (f_c) is much lower than the switching frequency ($f_c \ll f_s$), the error between an averaged model and real behavior of the totem pole PFC is insignificant for control purposes. The averaged large-signal model neglects the effect of current and voltage ripples as it is computed over a switching period

(T_s). An adequately low switching period is selected in comparison to system period to meet the requirements of averaged model [52].

The averaged large-signal model neglects the effects of high-frequency switching introduced by S_1 and S_2 which results in a continuous time model without any high frequency dynamics. The system can be modeled with the help of state equations for each switching interval as presented below. The state space model for the PFC for D period when S_2 and S_4 is ON is given by equations 3.21-3.22.

$$\underbrace{\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{-r_L}{L} & 0 \\ 0 & \frac{-1}{C(R_L+r_c)} \end{bmatrix}}_{A_1} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B_1} v_{in} \tag{3.21}$$

$$v_{dc} = \underbrace{\begin{bmatrix} 0 & \frac{R_L}{(R_L+r_c)} \end{bmatrix}}_{C_1} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} \tag{3.22}$$

where, A_1, B_1 and C_1 denote co-efficient matrices during D period of operation.

Similarly, for (1-D) period of operation we have

$$\underbrace{\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{-1}{L}\left(r_L + \frac{R_L r_c}{R_L+r_c}\right) & \frac{-1}{L}\left(\frac{R_L}{R_L+r_c}\right) \\ \frac{1}{C}\left(\frac{R_L}{R_L+r_c}\right) & \frac{-1}{C(R_L+r_c)} \end{bmatrix}}_{A_2} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B_2} v_{in} \tag{3.23}$$

$$v_{dc} = \underbrace{\begin{bmatrix} \frac{R_L r_c}{(R_L+r_c)} & \frac{R_L}{(R_L+r_c)} \end{bmatrix}}_{C_2} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} \tag{3.24}$$

where, A_2, B_2 and C_2 denote co-efficient matrices during (1-D) period of operation.

The averaged large-signal model requires that the state variables are time-continuous variables, implying $i_{in}$and v_c cannot change abruptly in the operating region between t_{on} andt_{off}. This model can be derived as presented in equations 3.25-3.28

$$\dot{x} = (A_1 x + B_1 vin)D + (A_2 x + B_2 v_{in})D' \tag{3.25}$$

$$v_{dc} = (C_1 x)D + (C_2 x)D' \tag{3.26}$$

$$\dot{x} = \underbrace{(A_1 D + A_2 D')}_{A} x + \underbrace{(B_1 D + B_2 D')}_{B} v_{in} \tag{3.27}$$

$$v_{dc} = \underbrace{(C_1 D + C_2 D')}_{C} x \tag{3.28}$$

Where A,B and C are the coefficient matrices of the averaged large-signal model of the totem pole PFC boost converter, D is a duty cycle, D' = 1 - D, t_{on} = D. T_s, and t_{off} = (1 - D)·T_s. Coefficients of A , B and C matrices are given in equations 3.29 – 3.30

$$\underbrace{\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{-1}{L}\left(r_L + \frac{D'R_L r_c}{R_L + r_c}\right) & \frac{-1}{L}\left(\frac{D'R_L}{R_L + r_c}\right) \\ \frac{1}{C}\left(\frac{D'R_L}{R_L + r_c}\right) & \frac{-1}{C(R_L + r_c)} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B} v_{in} \tag{3.29}$$

$$v_{dc} = \underbrace{\begin{bmatrix} \frac{D'R_L r_c}{(R_L + r_c)} & \frac{R_L}{(R_L + r_c)} \end{bmatrix}}_{C} \underbrace{\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}}_{x} \tag{3.30}$$

3.4.2 Averaged Small Signal model for totem pole PFC

The totem pole PFC converter can be perturbed by small variations in v_{in}, resulting in small variations in i_{in} and v_c with respect to their steady state values. The control system needs to modify D to control the state variables. The small signal variation around equilibrium point can be expressed as below

$$D = \widehat{D} + \tilde{d}\,; v_{in} = \widehat{V_{in}} + \widetilde{v_{in}}\,; x = \hat{X} + \tilde{x}\,; v_{dc} = \widehat{V_{dc}} + \widetilde{v_{dc}} \tag{3.31}$$

where,$\widehat{D}, \widehat{V_{in}}, \hat{X}$ and $\widehat{V_{dc}}$ represents the values at equilibrium point, while $\tilde{d}, \widetilde{v_{in}}$, $\tilde{x}$ and $\widetilde{v_{dc}}$ denotes the small-signal variations around the equilibrium point.

The average model presented in equations 3.27-3.28 can be rewritten by substituting D, v_{in}, x and v_{dc} from equation 3.31

$$\frac{d}{dt}(\hat{X}+\tilde{x}) = \left[A_1(\hat{D}+\tilde{d}) + A_2(1-\hat{D}-\tilde{d})\right](\hat{X}+\tilde{x}) + \left[B_1(\hat{D}+\tilde{d}) + B_2(1-\hat{D}-\tilde{d})\right](\widehat{V_{in}}+\widetilde{v_{in}}) \quad (3.32)$$

$$\widehat{V_{dc}} + \widetilde{v_{dc}} = \left[C_1(\hat{D}+\tilde{d}) + C_2(1-\hat{D}-\tilde{d})\right](\hat{X}+\tilde{x}) \quad (3.33)$$

where, $\frac{d}{dt}(\hat{X}) = 0$

Equations (3.32) and 3.33 are nonlinear in nature due to product of time-dependent variables. The non-linear model can be linearized around the equilibrium point under the following assumptions: $\widehat{V_{in}} \gg \widetilde{v_{in}}, \hat{X} \gg \tilde{x}, \hat{D} \gg \tilde{d}, \widehat{V_{dc}} \gg \widetilde{v_{dc}}$, implying that the small signal perturbations are insignificant compared to signal magnitude. Consequently the magnitude of $\tilde{d}\tilde{x}, \tilde{d}\widetilde{v_{in}}$ are negligible in comparison to magnitudes of $\widehat{V_{in}}, \hat{X}$ and $\hat{D}$ and can be ignored. The nonlinear model developed under these assumptions can be expressed as below

$$\dot{\tilde{x}} = A\hat{X} + B\widehat{V_{in}} + A\tilde{x} + B\widetilde{v_{in}} + \left[(A_1 - A_2)\hat{X} + (B_1 - B_2)\hat{X}\right]\tilde{d} \quad (3.34)$$

$$\widehat{V_{dc}} + \widetilde{v_{dc}} = C\hat{X} + C\tilde{x} + \left[(C_1 - C_2)\hat{X}\right]\tilde{d} \quad (3.35)$$

3.4.3 Steady state model

The steady state model can be obtained by setting all the time derivate expression to 0 in equations 3.34-3.35. The characteristic matrix A has to be invertible to obtain the appropriate steady state matrix values

$$\frac{d}{dt}\hat{X} = A\hat{X} + B\widehat{V_{in}} = 0 \quad (3.36)$$

$$\hat{X} = -A^{-1}B\widehat{V_{in}} \tag{3.37}$$

$$\widehat{V_{dc}} = C\hat{X} \tag{3.38}$$

$$\widehat{V_{dc}} = -CA^{-1}B\widehat{V_{in}} \tag{3.39}$$

$$\hat{X} = \begin{bmatrix} \widehat{i_{in}} \\ \widehat{v_c} \end{bmatrix} = \begin{bmatrix} \frac{\widehat{V_{in}}}{\left(r_L + \frac{D'R_L}{R_L + r_c}(r_c+1)\right)} \\ \frac{\widehat{V_{in}}D'R_L}{\left(r_L + \frac{D'R_L}{R_L + r_c}(r_c+1)\right)} \end{bmatrix} \tag{3.40}$$

$$\widehat{V_{dc}} = \frac{\widehat{V_{in}}D'R_L}{\left(r_L + \frac{D'R_L}{R_L + r_c}(r_c+1)\right)} \tag{3.41}$$

3.4.4 Linearized small signal and s-domain models

Linear control laws can be developed based on the linearization of the model around the steady state point. The linearized state-space small-signal model of the totem pole PFC can be calculated by substituting, (3.40) and (3.41) in (3.34) and (3.35) respectively. The linearized model around the steady state point can be expressed as below:

$$\frac{d}{dt}\tilde{x} \triangleq A\tilde{x} + B\widetilde{v_{in}} + \underbrace{\left[(A_1 - A_2)\hat{X} + (B_1 - B_2)\hat{X}\right]}_{K}\tilde{d} \tag{3.42}$$

$$\widetilde{v_{dc}} = C\tilde{x} + \left[(C_1 - C_2)\hat{X}\right]\tilde{d} \tag{3.43}$$

$$\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} \triangleq \underbrace{\begin{bmatrix} \frac{-1}{L}\left(r_L + \frac{D'R_Lr_c}{R_L+r_c}\right) & \frac{-1}{L}\left(\frac{D'R_L}{R_L+r_c}\right) \\ \frac{1}{C}\left(\frac{D'R_L}{R_L+r_c}\right) & \frac{-1}{C(R_L+r_c)} \end{bmatrix}}_{A} \begin{bmatrix} \widetilde{i_{in}} \\ \widetilde{v_c} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{B} \widetilde{v_{in}}$$

$$+ \underbrace{\begin{bmatrix} \frac{1}{L}\left(\frac{R_Lr_c}{R_L+r_c}\right) & \frac{1}{L}\left(\frac{R_L}{R_L+r_c}\right) \\ \frac{-1}{C}\left(\frac{R_L}{R_L+r_c}\right) & 0 \end{bmatrix}}_{K} \begin{bmatrix} \widehat{i_{in}} \\ \widehat{v_c} \end{bmatrix} \tilde{d} \tag{3.44}$$

$$\widetilde{v_{dc}} = \underbrace{\begin{bmatrix} \frac{D' R_L r_c}{(R_L + r_c)} & \frac{R_L}{(R_L + r_c)} \end{bmatrix}}_{C} \begin{bmatrix} \widetilde{i_{in}} \\ \widetilde{v_c} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{-R_L r_c}{(R_L + r_c)} & 0 \end{bmatrix}}_{P} \begin{bmatrix} \widehat{i_{in}} \\ \widehat{v_c} \end{bmatrix} \tilde{d} \tag{3.45}$$

The transfer function for totem pole PFC converter can be derived from linearized state space model presented in equations (3.44) – (3.45). The relationships between state and control variables are calculated under the following assumptions

$$\frac{\tilde{x}(s)}{\widetilde{v_{in}}(s)} = (sI - A)^{-1} B \text{ , with } \tilde{d} = 0 \tag{3.46}$$

$$\frac{\tilde{x}(s)}{\tilde{d}(s)} = (sI - A)^{-1} K \text{ , with } \widetilde{V_{in}} = 0 \tag{3.47}$$

$$\frac{\widetilde{v_{dc}}(s)}{\tilde{d}(s)} = C(sI - A)^{-1} K + P \text{ , with } \widetilde{v_{in}} = 0 \tag{3.48}$$

The relevant transfer functions required to design the controllers are computed by replacing the characteristic matrices A, B, C, K and P in expressions (3.46) – (3.48).

3.4.5 Design of Control System

The totem pole PFC converter requires a two-loop cascade control structure composed of Proportional-Integral (PI) linear controllers as shown in Fig. 3.11. The two feedback loops includes an inner current control loop and an outer voltage control loop; two-loop cascade control is proposed to shape the input current while controlling the output power to desired value. Simulation and design of the control loops were performed using Matlab. The fast dynamics of inner current control-loop helps in tracking the input voltage waveform (V_{in}) , allowing unity PF to be reached. i_{in} exhibits fast dynamics and its control system must ensure high bandwidth and fast time response while rejecting the switching noise at f_s. The bandwidth of the current controller (BW_i) must be small in comparison with f_s which is ensured by designing the current controller bandwidth to be meet the constraint $BW_i \leq$

0.1f_s. Outer and slow voltage control-loop is designed to regulate the voltage while meeting the power requirements. The bandwidth of the voltage controller (BW_v) must be small in comparison with BW_i to ensure that any perturbation on current is settled before the action of voltage controller. In addition, the voltage control loop must reject the double frequency ripple introduced in output voltage due to power pulsations, i.e. $BW_v \leq 120Hz$. The designed cascaded control system must be able to reject perturbations caused by small variations of input voltage and load current.

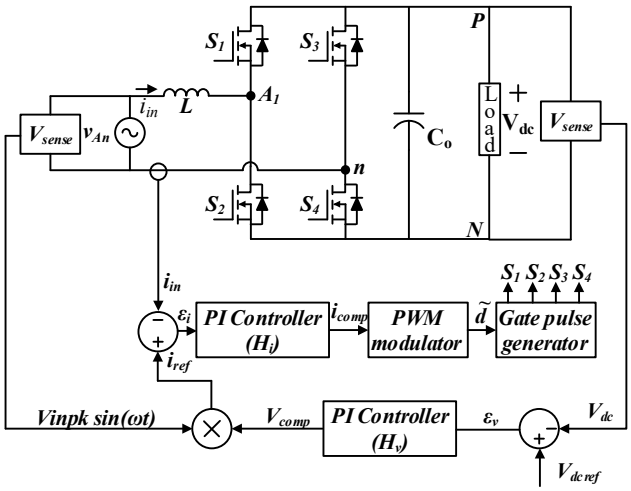


Fig. 3.11 Totem pole PFC dual loop control structure

In the proposed control scheme presented in Fig. 3.11, the output voltage signal V_{dc} is sensed with the help of a hall-effect sensor which is filtered to remove the high frequency content and sensed using an ADC channel of the microcontroller. The sensed signal is compensated and compared with the reference voltage (V_{dcref}) to generate the voltage error (ε_v) signal, which is processed using a PI controller (H_v) to generate a power reference (V_{comp}). The power reference multiplied with sensed input voltage waveform generates the current reference (i_{ref}). The current error (err_i) signal is generated by comparing sensed current i_s with the reference (i_{ref}) which gets filtered through a PI

controller generating the control signal (i_{comp}). The control signal is compared with a high frequency triangular waveform generating the modulation signal ($\tilde{d}$) which is used to generate gate pulses for all the MOSFETs.

The equivalent small signal model of the proposed control scheme is presented in Fig. 3.12, when a small signal perturbation is applied in the current loop the gain of voltage loop reduces to 1. This is based on the primary assumption that the voltage control loop is very slow compared to the current control loop.

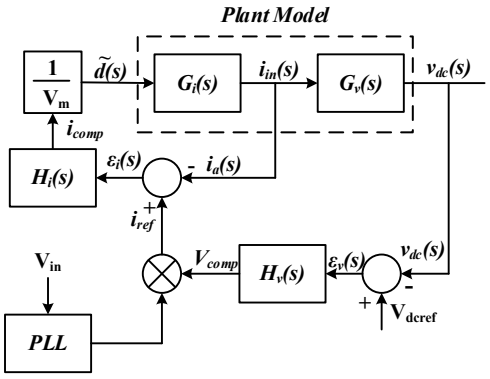


Fig. 3.12 Small signal control block diagram for totem pole converter

The effective plant model for inner loop to be compensated can be summarized as below

$$G_i'(s) = \frac{\varepsilon_i(s)}{i_{in}(s)} * \frac{i_{in}(s)}{\tilde{d}(s)} * \frac{\tilde{d}(s)}{i_{comp}} \tag{3.49}$$

The operating point for a totem pole PFC is varying over the line cycle which leads to different plant model linearized at various operating condition. The bode plot for the uncompensated system at various points of input line cycle is presented below. Near zero crossing of input voltage the plant model reduces to a first order system with very low gain, as the input voltage increases the system shows second order behavior. The gain at line

cycle is minimum at the peak point and hence the compensator is designed at this point to satisfy the gain requirements with high phase margin.

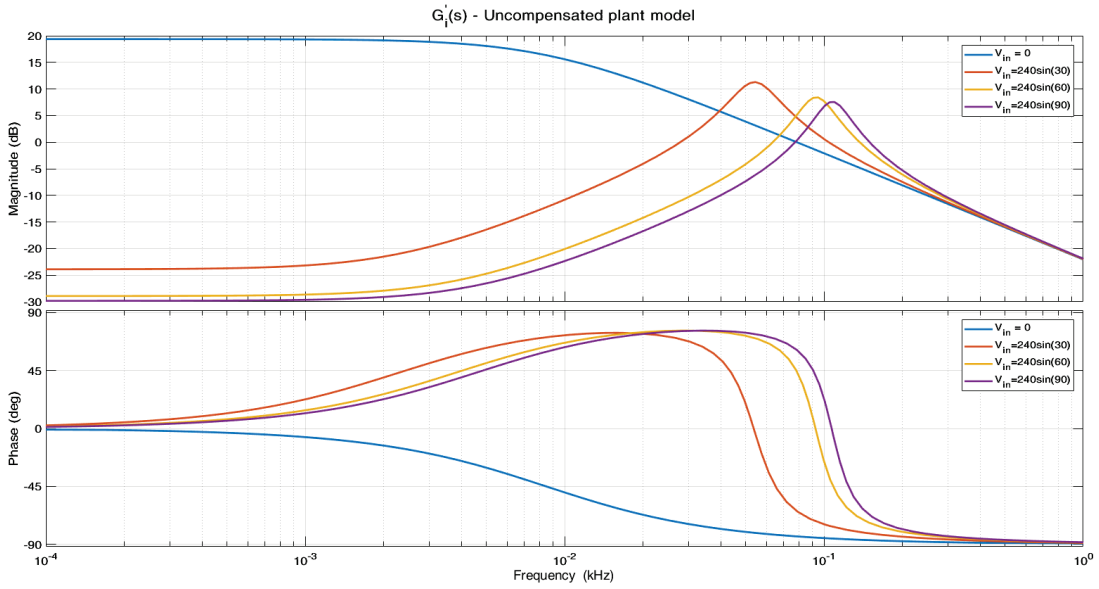


Fig. 3.13 Bode plot: Uncompensated plant model for current loop

The designed compensator should be fast enough to follow the reference current while attenuating the second harmonic component of grid frequency introduced by output voltage ripples. Hence the gain to low frequency components should be as small as possible. The steady state error of the loop depends on the dc gain of the system and it is recommended to have a high dc gain so that the error is minimized. The compensator is designed to meet these constraints. The designed compensator is as given below:

$$H_i(s) = \left(k_p + \frac{k_i}{s}\right) = \left(0.2 * 125 + \frac{1500*125}{s}\right) \tag{3.50}$$

A family of bode plots for the compensated system varying under line cycle is presented in Fig. 3.14. Since, the primary target is to track the input current at 60Hz the open loop transfer function gain should be very high at the operating point. Additionally, as presented earlier the bandwidth of the compensated system should be less than $0.1f_s$ to prevent

current distortion from high frequency components. The designed current controller has a phase margin of 62.1^0 while the gain margin is infinite with a bandwidth of 2.24 kHz.

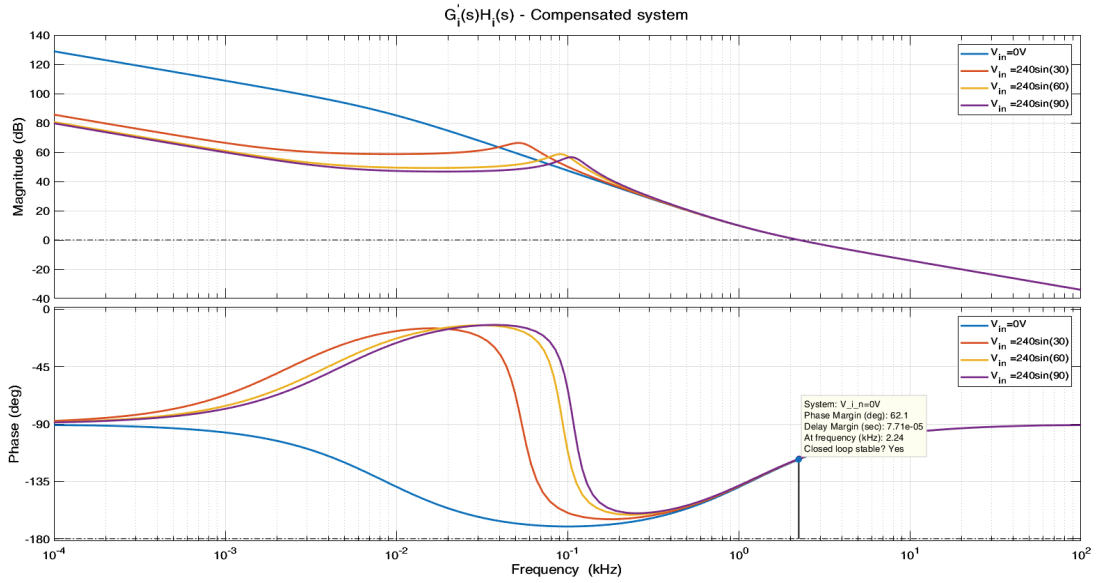


Fig. 3.14 Bode plot: Compensated plant model for current loop

The current controller is designed based on the assumption that the output voltage loop is slow and hence will not affect the dynamics of the current loop. Under this assumption, to design the voltage controller loop the current controller gain can be considered as 1 since the loop is fast and any change in reference is tracked immediately. The simplified plant model to be compensated is as presented below

$$G_v'(s) = \frac{\varepsilon_v(s)}{v_{dc}(s)} * \frac{\widetilde{v_{dc}}(s)}{\tilde{d}(s)} * \frac{\tilde{d}(s)}{v_{comp}} = 1 * \frac{\widetilde{v_{dc}}(s)}{\tilde{d}(s)} * \frac{P_{out}}{V_{inrms}^2} \tag{3.51}$$

The uncompensated plant transfer function is computed by substituting equation (3.48) in (3.51) and the corresponding family of bode plot is presented in Fig. 3.15. The uncompensated system provides high gain to low frequency as well as switching frequency components. In order to shape the PFC current while maintaining the voltage the loop has to be compensated to reject high frequency as well as double line frequency components.

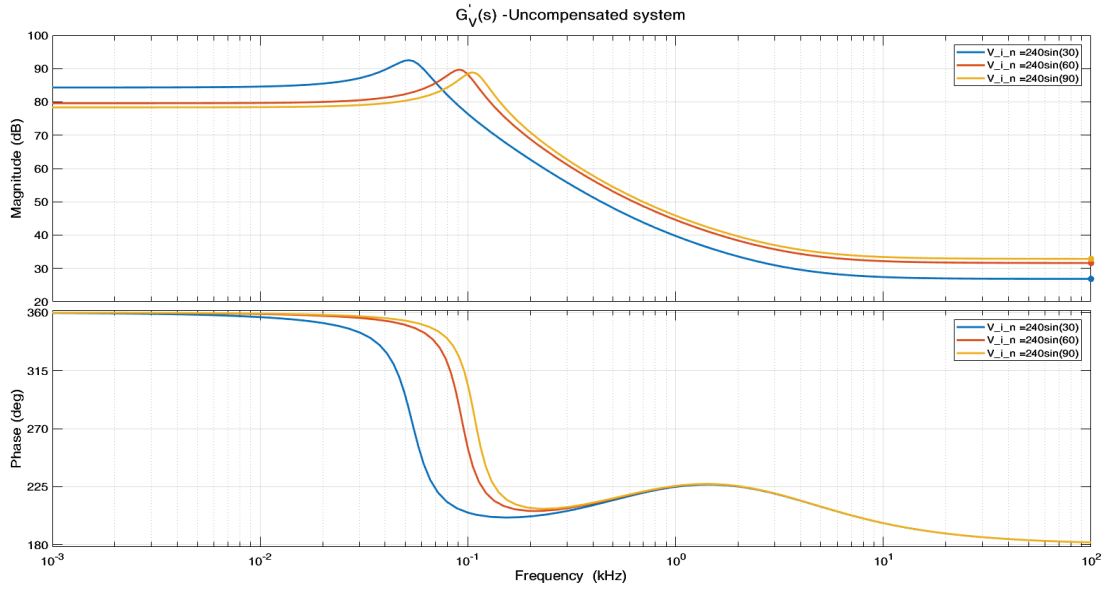


Fig. 3.15 Bode plot: Uncompensated voltage transfer function

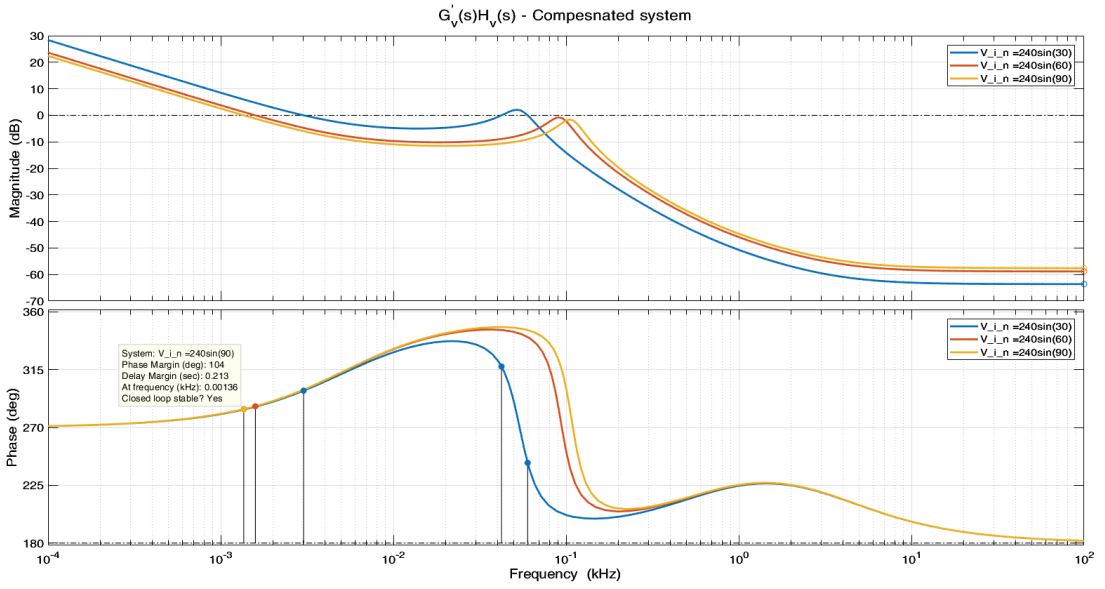


Fig. 3.16 Bode plot: Compensated open loop transfer function

The designed compensator should attenuate low frequency components while operating with high dc gain to achieve low steady state error. The designed compensator is presented below

$$H_v(s) = \left(k_{pv} + \frac{k_{iv}}{s}\right) = \left(0.00003 + \frac{0.01}{s}\right) \tag{3.52}$$

A family of bode plots corresponding to the compensated system is presented in Fig. 3.16. The controller is designed to be very slow with approximately 1Hz bandwidth to attenuate the double frequency ripple introduce by rectification as well as the high frequency switching components.

3.5 Simulation Results

A simulation study is carried out using MATLAB Simulink to understand the behavior of single phase PFC under varying operating conditions. The parameters of the simulated system are presented in Table 3.1. The totem-pole switching logic is evaluated using MATLAB simulations and the key results at full load conditions are presented in Fig. 3.17. The voltage and current controller designed in previous section is used to simulate the closed loop operation of the converter. As can be inferred from the results the input voltage and current are perfectly in phase producing an output ripple <2.5%.

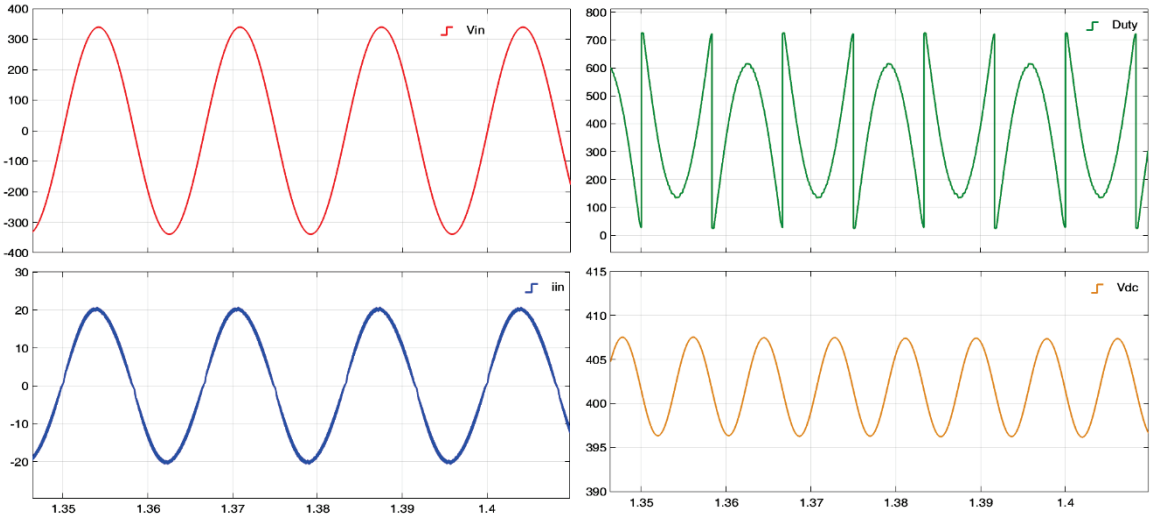


Fig. 3.17 Key Operating waveforms for Totem-pole scheme at 3.3kW (a) Input voltage (V_{in}) (b) Input current (i_{in}) (c) Duty ratio(D) (d) Output Voltage (V_{dc})

3.6 *Experimental Verification*

As a proof of concept verification of the totem pole PFC circuit, a 3.3kW laboratory prototype is built according to the specifications presented in Table 3.1.The key componets are labelled in the laboratory prototype shown in

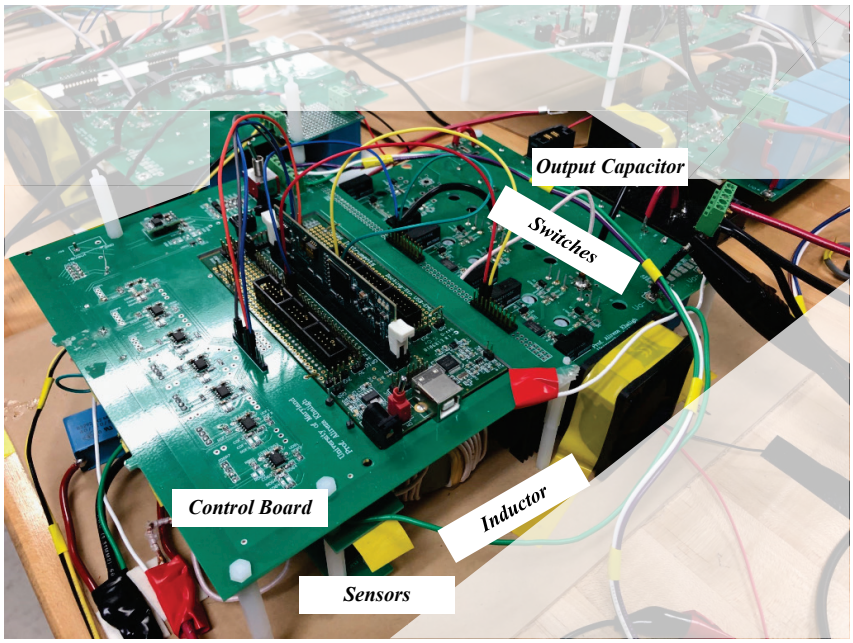


Fig. 3.18 Laboratory implemented prototype of 3.3kW PFC

The key operating waveforms of the implemented prototype are presented in Fig. 3.19.As can be inferred from the figure the input voltage and current is perfectly in phase with minimum low frequency harmonics. The captured experimental results at 3.3kW exhibits a conversion efficiency of 97.39% with a THD of 2.08%, which meets the input grid requirements (<5% THD) for the converter. The output dc voltage ripple is less than 1% (±4V) as can be seen from Fig. 3.19.

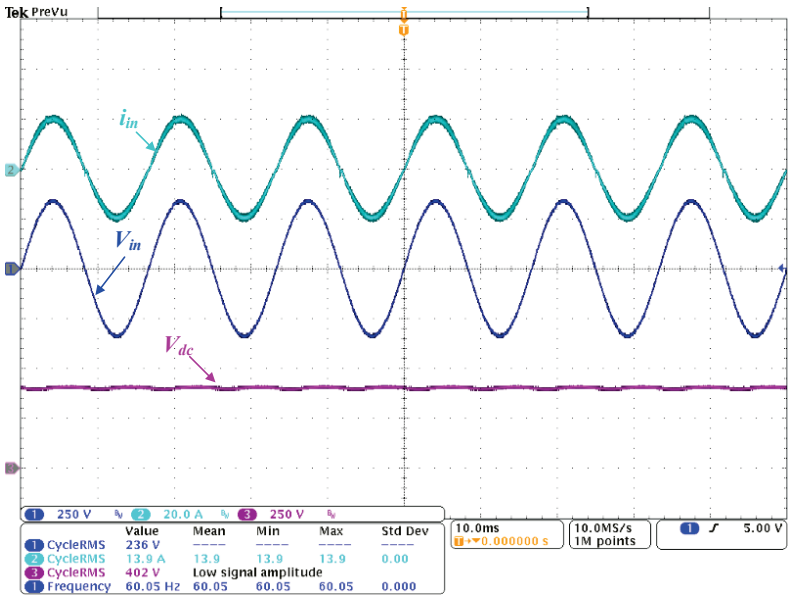


Fig. 3.19 Key operating waveforms for totem pole PFC @ V_{in}=240Vrms, V_{dc}=400V, P_{out}= 3.3 kW output power

The input current harmonic injection is an important measure of power quality of any grid connected interface. The injected harmonics of developed prototype is computed using Fourier analysis till 30th harmonic and presented in Fig. 3.20. The harmonics content is quantified with the ratio of peak current value at a specific harmonic frequency (I_h) to the peak value of fundamental (I_1) frequency. The magnitude of low frequency harmonics injected to the grid is very low as can be concluded from Fig. 3.20.

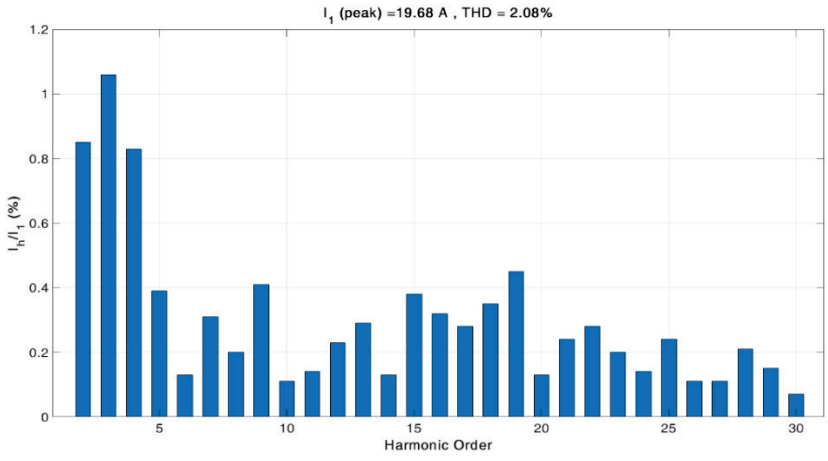


Fig. 3.20 Harmonic spectrum of input current under nominal voltage and full load condition

Additionally, to evaluate the performance of designed system the efficiency characteristics are captured with the help of power analyzer Tektronix PA3000. The power measurements presented in Fig. 3.21(a) is captured under full load conditions.

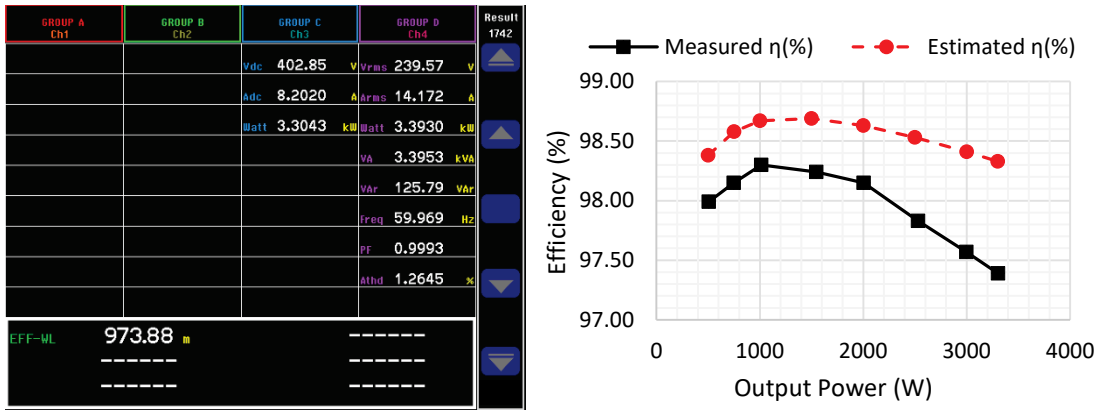


Fig. 3.21 (a) Tektronix power measurements (b) Estimated vs Measured efficiency plot over the power range

Fig. 3.21(b) presents the comparison of measured efficiency with the estimated efficiency for low power to full load conditions while maintain constant output voltage. The overall losses of the circuit are estimated using relations presented in section 3.2 over varying power level while working under nominal operating voltage of 240Vrms. The circuit generates a peak efficiency of 98.2% @ 1.5kW and drops due to increased conduction losses at higher power which is proportional to square of current. The measured and estimated efficiencies exhibit a maximum difference of ~1% under full load conditions. The difference in estimated values compared to measured values can be attributed to various non-linearities of circuit elements such as parameter dependence on temperature, trace resistance and inductances etc. which are ignored during loss estimation.

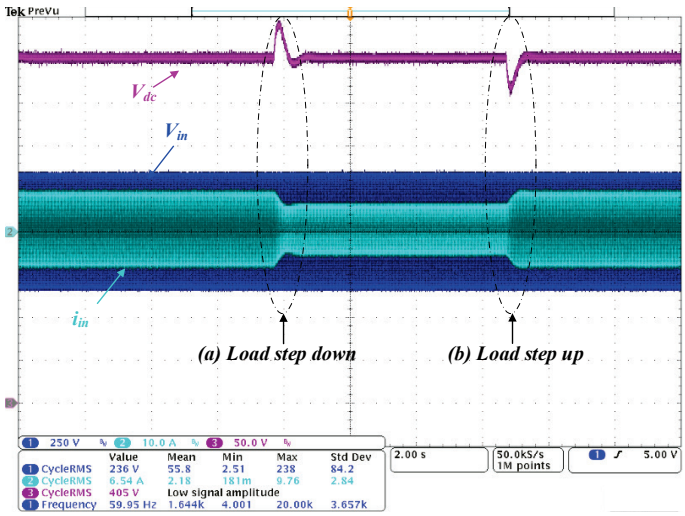


Fig. 3.22 PFC transient results (a) Load step from 1.5 kW to 1 kW (b) Load step from 1 kW to 1.5 kW

In Section 3.4, a dual loop control structure was designed to shape the input current while maintaining a constant output voltage. In order to test the stability of the designed loop under transient conditions, a load step of 500 W is introduced with the help of an electronic load. The transient results obtained during the load step is captured in Fig. 3.22.

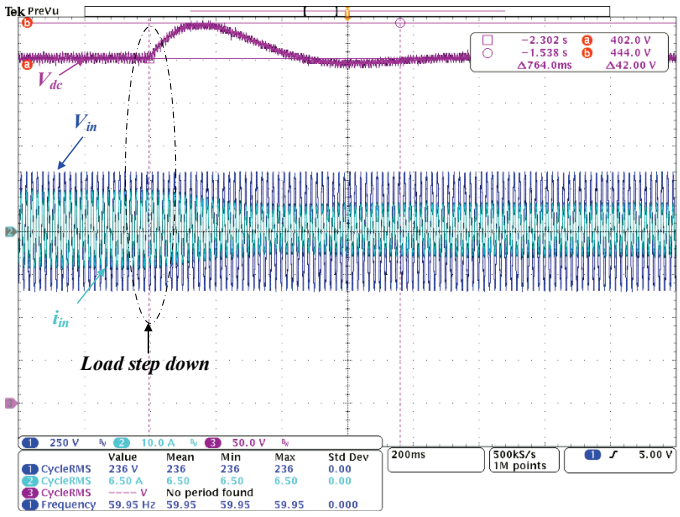


Fig. 3.23 Key transient waveforms under load step from 1.5kW to 1kW

The overshoot and undershoot in output voltage lies within allowed bandwidth of $\pm 10\%$. The controller settles to 5% of reference voltage within 320ms while it takes 764ms to settle to 0.5% as presented in Fig. 3.23.

3.7 Summary

In this chapter, a comprehensive study has been carried out to select the suitable topology for AC-DC conversion stage of the proposed integrated charger. Multiple bridgeless topologies are evaluated and a single phase totem pole PFC structure is selected based on its efficiency characteristics. Detailed small signal modeling of the system is carried out and the voltage and current controllers are designed to shape the input current. A 3.3kW laboratory prototype is developed to evaluate the proposed design which is capable of achieving a full load efficiency of 97.39% while operating with a power factor 0f 0.9993 and THD of 2.08%.

Chapter 4: Design and development of DC-DC Wireless Stage

In previous section we analyzed different bridgeless PFC structures and selected the totem-pole PFC as potential solution for input conditioning facilitating AC-DC conversion. In order to complete the design of off-board stage of the proposed integrated charger the wireless DC-DC converter has to be appropriately realized. The typical configuration enabling inductive power transfer is presented in Fig. 4.1.

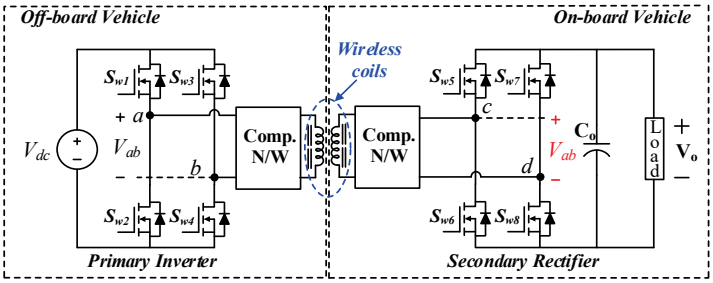


Fig. 4.1 Wireless DC-DC power transfer stage of inductive charging circuit

The primary inverter structure along with compensation network and primary coil can be classified as off-board elements which is connected in cascaded to the totem-pole PFC. The receiver pad along with compensation network and secondary rectifier are incorporated on-board the vehicle. The rectifier stage is integrated to on-board conductive stage as a part of the proposed solutions in chapter 2.

4.1 Fundamentals of Inductive power transfer

An inductive power transmission (IPT) system, which transfers power to load via an air-cored transformer without any physical contact, is a convenient and flexible energy transmission method. IPT technique is realized with the help of near field magnetic coupling and magnetic resonance phenomenon [3-16].IPT systems have been under development from 1800's when Nikola tesla successfully demonstrated the powering of

incandescent bulbs wireless over a distance of up to 100 feet [53]. The history and development of IPT techniques over the years are presented in [54].

IPT uses a loosely coupled transformer that involves a large separation between the primary and secondary windings with no magnetic core between them. Due to the large winding separation, it has a relatively large leakage inductance on both sides. Furthermore, the magnetizing flux is significantly reduced, which results in a much lower magnetizing inductance and mutual inductance. The weak coupling limits the power transferability and coil-to-coil efficiency of the IPT system. In order to improve the efficiency, the compensation networks are added to both the transmitter side and receiver side [55], [56].

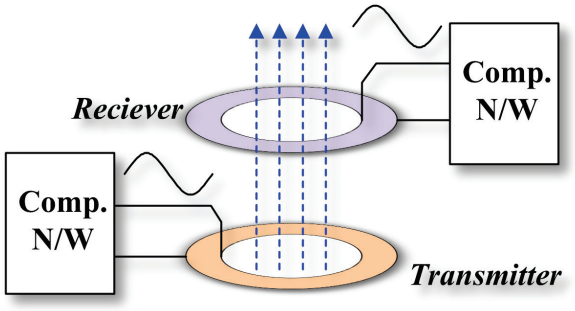


Fig. 4.2 Inductive power transfer technique principle of operation

The compensation networks are usually composed of capacitors, which can be either external capacitors or the parasitic capacitors of the coils. The capacitance values are selected according to the resonant frequency. The basic operation principle of IPT is illustrated in Fig. 4.2, where the primary inverter converts the input dc to high frequency ac and excites the transmitter coil, the generated magnetic field induces voltage on receiver coil, which is rectified by secondary bridge and delivered to the load.

4.2 Compensation Topologies

Compensation network structures are used on primary and secondary sides to neutralize the effect of high leakage inductance introduced by the wireless coils. The simplest structures of compensation are classified based on the location of capacitors on primary and secondary side networks, four basic compensation structures are SS, SP, PS and PP, where S stands for series and P stands for parallel in the primary and secondary network respectively[55].

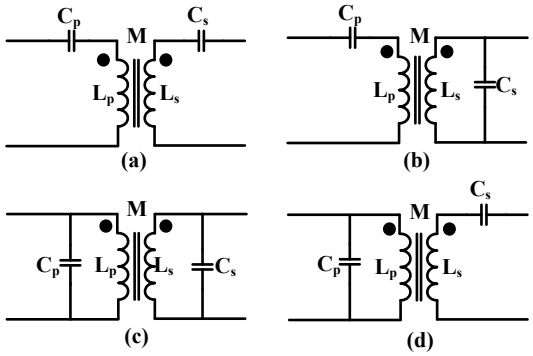


Fig. 4.3 Basic compensation topologies (a) Series-Series (SS) (b) Series- Parallel (SP) (c) Parallel-Parallel (PP) (d) Parallel-Series(PS)

Among these four basic topologies shown in Fig. 4.3, the SS compensation (Fig. 4.3(a)) is popular for its simplicity. The resonant capacitors C_p and C_s can be selected to compensate either the self-inductance values or leakage inductance of the wireless coil. A load independent behavior is presented by the resonant network compensated to leakage inductance while self-inductance compensation leads to coupling independent behavior of the circuit. Since, the wireless coils are air cored transformer structures the coupling is dependent on alignment conditions. The voltage stress on the resonant capacitors of the series-series compensated system is high and hence requires capacitor banks to maintain reliable operation of the circuit. The power transferability of SS compensated system is

significantly influenced by the coupling between the coils, so additional control method or specific design of coils is required to deal with the misalignment between the coils.

In case of SP compensation (Fig. 4.3(b)), voltage across the resonant elements L_s and C_s are lower, which reduces insulation requirements and leads to a lower electric stray field [57]. A disadvantage of this structure is the circulating reactive current in the receiver-side parallel resonant circuit that exhibits load independent behavior. The high circulating current in receiver coil results in additional losses affecting the transmission efficiency under partial load conditions. Furthermore, the resonant frequency of a parallel compensated IPT systems depends on the load and the magnetic coupling. This complicates the control and may lead to hard-switching of the full-bridge inverter under certain loading conditions or coil positions [58].

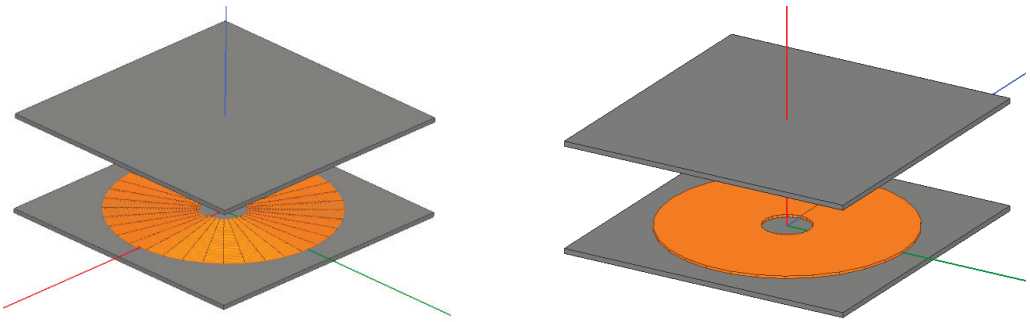
A parallel compensation of the transmitter coil is also possible [55] presented as PP and PS, but requires an additional inductor connected in series between the resonant circuit and the power converter to achieve soft-switching of the primary inverter. This topology is mainly useful for systems, where a constant current behavior is required in the transmitter coil for power transfer. Additional higher order compensation topologies are proposed recently which has been comprehensively evaluated by researchers in [23] and categorized on basis of current-source behavior and voltage-source behavior.

For the work presented in this dissertation, a series-series compensation network is chosen mainly for the higher transmission efficiency during partial load conditions and for the load and magnetic coupling independent resonant frequency characteristics.

4.3 Inductive coil modeling

Wireless power transfer coils or pads forms a major component of any IPT system. Optimized coil design is a key requirement to maximize the overall transfer efficiency of the system. Various coil structures have been developed by researchers across the world focusing on maximization of coupling characteristics and quality factor [6]. Typical IPT system coil designs are adapted from conventional magnetic core topologies such as pot, U and E core [6], [27], [58], [59].Planar coil structures derived from pot core are widely reported in design of wireless coupler for EVs. In order to improve the coupling characteristics over a larger air gap alternate coupling pad solutions such as DD,DDQ, bipolar have been proposed in literature [6], [27], [59]. These topologies exhibit more coupling with less pad area even under misalignment. The planar coil structure with ferrite back plate is an attractive solution for high power transfer design due to several advantages such as (i) low profile (ii) Single sided magnetic field with reduced leakage (iii) Lower loss due to shielding [6], [27], [58]. The major disadvantage of planar coil structure is the requirement of high diameter of pad to facilitate power transfer over high air gap [27].

Analytical equations have been developed to compute the inductances of planar coils with air core [60] and infinite-size ferrite plate [61]–[66]. There is no simple analytical model developed for planar coils placed over a finite-size ferrite plate. Numerical methods are more suitable to analyze the inductance values in this scenario. A typical set of planar coils is presented in Fig. 4.4(a). A circular spiral winding is placed over a square ferrite plate. Circular winding is chosen because of its easy fabrication with minimum copper area. The choice of square ferrite plate is to facilitate development with commercially available components.



(a) (b)

Fig. 4.4 (a) Planar coil structure with spiral windings (b) Simplified coil model with single-turn lumped model for finite element analysis (FEA)

The design process of magnetic coils includes optimization of various parameters such as inner radius (R_{inner}), Outer radius (R_{outer}) of winding, no of turns (N) and wire size. Finite element analysis has to be carried out to optimize the different parameters. Since, the planar coil structure presented in Fig. 4.4(a) is computationally intensive a simplified lumped model is developed as shown in Fig. 4.4(b). The accuracy of the simulated inductances and coupling factor using simplified model are good enough to match physical design parameters [67].

In this work, a planar coil structure is chosen to implement the transmitter and receiver coil with ferrite back plate to maximize the coupling between the coils. The simplified model presented in Fig. 4.4(b) is implemented using MAXWELL to simulate the coefficients of reference coil. Self-inductance L for the coils with N turns of winding illustrated in Fig. 4.4(a) is computed from the self-inductance value L_0 of a simplified model in Fig. 4.4(b) as below

$$L = N^2 L_0 \tag{4.1}$$

The wire size needs to be carefully chosen to reduce the skin and proximity effect which increases the effective ac resistance of coil leading to higher loss and low quality factor. In this design, an appropriate value of litz wire is chosen based on ac factor selection technique proposed in [68]. The parameters of current coil developed in lab are summarized in Table 4.1.

Table 4.1 Parameters of reference coil developed in lab

Parameter		**Measured Value**	**Simulation Results**
Inductance (μH)	Primary self (L_1)	273.8	282.86
	Secondary self (L_2)	275.3	282.94
	Mutual (L_m)	62.75	75.73
	Coupling factor (k)	0.23	0.27
Coil Parameters	# of turns	34	
	Distance between coils	100mm	
	Wire dimension	AWG 13	
	Strand dimension	AWG 44	
	# of strands	1200	
	R_{inner}	25 mm	
	R_{outer}	126.5 mm	

Since the key focus of this research is to verify the proposed integrated wireless charging technique, an optimized design presented by researchers in [69] is used as a reference to develop the initial coil parameters. The proposed coil parameters requires further optimization to maximize efficiency which will be carried out as a part of future work.

4.4 Modeling of DC/DC stage

The generalized topology of wireless DC/DC stage is presented in Fig. 4.1. The primary inverter bridge generates a high frequency square wave from DC input and excites the resonant tank formed by the compensation network and transmitter coil. The frequency of operation is chosen to be near the resonant frequency of the tank which leads to cancellation of high leakage impedance created by the wireless coils facilitating current flow through the network. This high frequency current generates a varying magnetic field at the transmitter side which cuts the secondary coil and generates voltage. The secondary side is also tuned to the same primary resonant frequency and hence facilitate current flow to load through rectifier bridge.

The key waveforms of the primary and secondary side of the converter employing a quasi-square wave generation on primary side and uncontrolled diode rectification on secondary side operating at resonant frequency are presented in Fig. 4.5. The resonant tank of the wireless converter is excited with the help of a square wave ($v_{ab}(t)$) generated by switching of primary bridge structure. The input voltage can be expressed using Fourier expansion as below:

$$v_{ab}(t) = \left(\frac{4}{\pi}\right)(V_{dc}).\sum_{\substack{m=0 \\ k=2m+1}}^{\infty} \frac{\cos\left(\frac{k\alpha}{2}\right)}{k}\sin(2\pi k f_s t) \qquad (4.2)$$

where t is the time parameter, k is an integer parameter for the Fourier series expansion, f_s is the switching frequency of the converter, α is the phase shift angle between primary bridge legs, and V_{dc} is the input dc voltage to the primary bridge.

Similarly, the output bridge voltage $v_{cd}(t)$ referred to primary side can be expressed as follows:

$$v_{cd}(t) = \left(\frac{4}{\pi}\right)(nV_o).\sum_{k=2m+1}^{\infty}{}_{m=0}\frac{1}{k}\sin(2\pi k f_s t - \varphi_k) \tag{4.3}$$

where φ_k is the phase shift with respect to input voltage, n is the step down ratio of wireless coils and V_o is the output dc voltage.

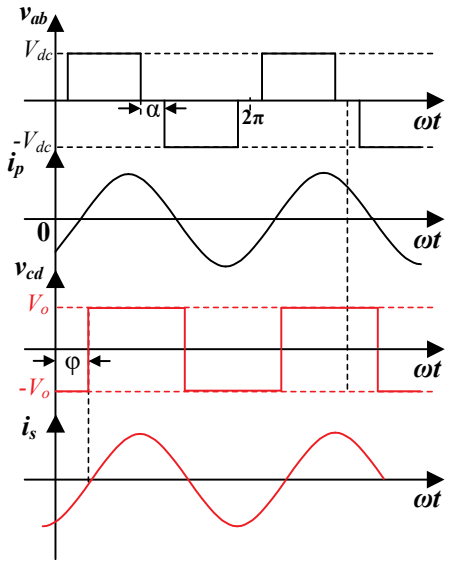


Fig. 4.5 Key operating waveforms of DC-DC Converter

The generalized AC equivalent circuit of the resonant converter obtained based on the analysis above is illustrated in Fig. 4.6(a). The wireless coils are replaced with the transformer equivalent model for AC circuit analysis. The equivalent circuit can be further simplified to the model illustrated in Fig. 4.6(b), where the impedances $Z_1(\omega), Z_2(\omega), Z_3(\omega)$ for different compensation topologies are presented in Table 4.2.

Traditionally, first harmonic approximation (FHA) model is used to analyze resonant circuits as the resonant network attains low pass characteristic attenuating the higher order harmonic content present in the input square wave voltage. The generalized equivalent circuit can be reduced to its first harmonic form to extract the gain characteristics of the converter.

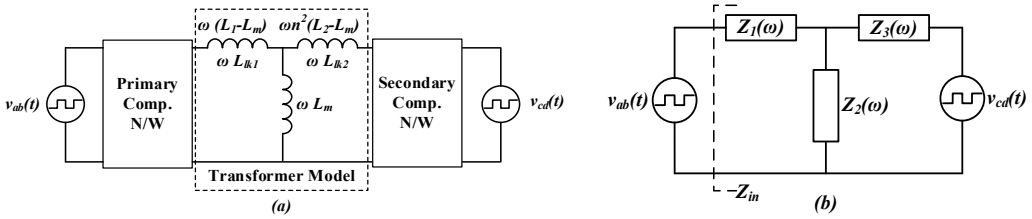


Fig. 4.6(a) Generalized AC equivalent circuit (b) Simplified equivalent model

Table 4.2 Equivalent Model Parameters for basic compensation topologies

Topology (Primary/Secondary)	$Z_1(\omega)$	$Z_2(\omega)$	$Z_3(\omega)$
SS	$j\left(\omega L_{lk1} - \frac{1}{\omega C_1}\right)$	$j(\omega L_m)$	$j\left(\omega L_{lk2} - \frac{1}{\omega C_2}\right)$
SP	$j\left(\omega L_{lk1} - \frac{1}{\omega C_1} + \frac{n^2\omega^2 L_m L_{lk2}}{\sigma_2 - \omega L_m}\right)$	$-j\left(\frac{n^2 L_m}{C_2(\sigma_2 - \omega L_m)}\right)$	$-j\left(\frac{n^4 L_{lk2}}{C_2(\sigma_2 - \omega L_m)}\right)$
PS	$-j\left(\frac{L_{lk1}}{C_1(\sigma_1 - \omega L_m)}\right)$	$-j\left(\frac{L_m}{C_1(\sigma_1 - \omega L_m)}\right)$	$j\left(n^2\omega L_{k2} - \frac{n^2}{\omega C_2} + \frac{\omega^2 L_m L_{lk1}}{\sigma_1 - \omega L_m}\right)$
PP	$-j\left(L_{lk1}\chi_1 - \frac{2L_m\chi_1(\gamma_1+\gamma_2)}{\chi_1+\chi_2-\gamma_1-\gamma_2}\right)$	$-j\left(\frac{2L_m\chi_1\chi_2}{\chi_1+\chi_2-\gamma_1-\gamma_2}\right.$	$-j\left(n^2 L_{lk2}\chi_2 - \frac{2L_m\chi_2(\gamma_1+\gamma_2)}{\chi_1+\chi_2-\gamma_1-\gamma_2}\right)$

where , $\sigma_1 = \omega L_{lk1} + 2\omega L_m - \frac{1}{\omega C_1}$ (4.4) $\sigma_2 = 2\omega L_m + n^2\left(2\omega L_{lk2} - \frac{1}{\omega C_2}\right)$ (4.5)

$\gamma_1 = \frac{\omega^2 L_{lk1}}{\sigma_1}$ (4.6) $\gamma_2 = \frac{n^2\omega^2 L_{lk2}}{\sigma_2}$ (4.7)

$\chi_1 = \frac{1}{C_1\sigma_1}$ (4.8) $\chi_2 = \frac{n^2}{C_2\sigma_2}$ (4.9)

4.4.1 FHA Analysis

For the period of operation of the converter near resonant frequency, the input voltage can be approximated with its fundamental sine wave. From (4.2) the fundamental value of input voltage $v_{ab1}(t)$ is given below

$$v_{ab1}(t) = \left(\frac{4}{\pi}\right)(V_{dc}).\cos\left(\frac{\alpha}{2}\right)\sin(2\pi f_s t) = |V_{ab1}|\angle 0 \qquad (4.10)$$

The output bridge voltage $v_{cd}(t)$ can be replaced by an equivalent output resistance (R_{FHA}) given by (4.11)

$$R_{FHA} = \left(\frac{8}{\pi^2}\right)n^2 R_L \qquad (4.11)$$

Using the FHA method, the generalized impedance model presented in Fig. 4.6(b) can be reduced to FHA model operating at a given angular frequency ω_s, as illustrated in Fig. 4.7.

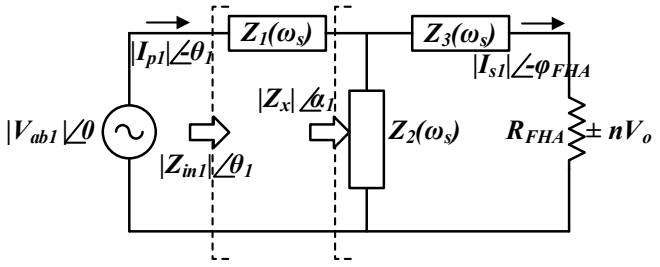


Fig. 4.7 FHA model for wireless DC-DC converter

4.4.1.1 Input Impedance

The impedances $Z_1(\omega_s), Z_2(\omega_s), Z_3(\omega_s)$ for different compensation topologies are presented in Table 4.2. Using the impedance values corresponding to the selected compensation topology and the equivalent resistance the input impedance can be evaluated as follows ($|Z_{in}|\angle\theta$)

$$Z_{in1}(\omega) = Z_1(\omega) + [Z_2(\omega)//(Z_3(\omega) + R_{FHA})]$$

(4.12)

Converting $Z_{in}(\omega)$from rectangular to polar form we have

$$|Z_{in1}| = \sqrt{Re\big(Z_{in1}(\omega)\big)^2 + Im\big(Z_{in1}(\omega)\big)^2} \tag{4.13}$$

$$\theta_1 = \arg(Z_{in1}) = \tan^{-1}\left(\frac{Im(Z_{in1}(\omega))}{Re(Z_{in1}(\omega))}\right) \tag{4.14}$$

4.4.1.2 Gain Derivation

Using FHA model presented in Fig. 4.7 the relationship for the fundamental component of primary tank current i_{p1} can be expressed as below

$$i_{p1}(t) = \frac{v_{ab1}(t)}{Z_{in1}(\omega)} = \frac{|V_{ab1}|<0}{|Z_{in1}|<\theta_1} = \big|i_{p1}\big|\angle - \theta_1 \tag{4.15}$$

where $v_{ab1}(t)$ is the fundamental component of primary bridge voltage given by (4.10)

The fundamental component of secondary tank current $i_{s1}(t)$ can be calculated using the current divider rule as shown below

$$i_{s1}(t) = |I_{s1}|\angle - \varphi_{FHA} = \frac{Z_2(\omega)}{Z_2(\omega)+Z_3(\omega)+R_{FHA}}\big|I_{p1}\big|\angle - \theta_1 \tag{4.16}$$

Let, $Z_{x1}(\omega)$ define the current divider ratio which leads to the following relations

$$Z_{x1}(\omega) = \frac{Z_2(\omega)}{Z_2(\omega)+Z_3(\omega)+R_{FHA}} = |Z_{x1}|\angle\delta_1 \tag{4.17}$$

$$i_{s1}(t) = |I_{s1}| < -\varphi_{FHA} = |Z_{x1}|\big|i_{p1}\big|\angle\delta_1 - \theta_1$$

(4.18)

Using AC analysis on impedance model presented in Fig. 4.7 we have

$$nv_o(t) = i_{s1}R_{FHA} = Z_{x1}(\omega)i_{p1}(t)R_{FHA} \tag{4.19}$$

Combining equations (3.30), (3.35) and (3.39) and extracting the dc component, we can find the expression for normalized DC gain G_{nFHA} of the converter as presented below

$$G_{nFHA} = \frac{nV_o}{V_{dc}} = R_{FHA} \cos\left(\frac{\alpha}{2}\right) \frac{|Z_{x1}|}{|Z_{in1}|} \tag{4.20}$$

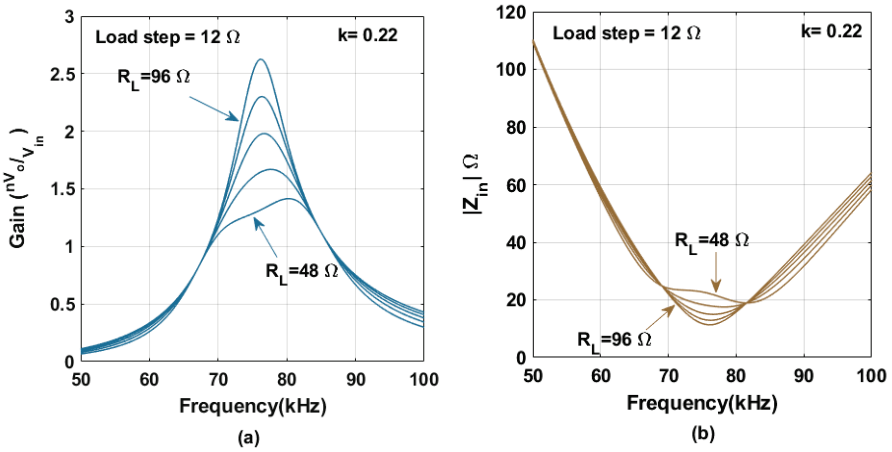
4.4.1.3 Series-Series resonant compensation

As presented in previous section the SS topology is selected to implement the primary and secondary compensation in this work due to higher efficiency at partial load and coupling independent resonant frequency characteristics of the structure. Dual compensation structure leads to two resonant frequencies defined as below

$$f_{pri} = \frac{1}{2.\pi.\sqrt{L_1 C_p}} \tag{4.21}$$

$$f_{sec} = \frac{1}{2.\pi.\sqrt{L_2 C_s}} \tag{4.22}$$

The leakage inductance values are computed using numerical simulations from Ansys Maxwell using simplified model presented in Fig. 4.4(b). The resonant frequency is chosen to be 85 kHz at nominal condition satisfying SAE J2954 [8] restricted operating frequency range of 80-90kHz .



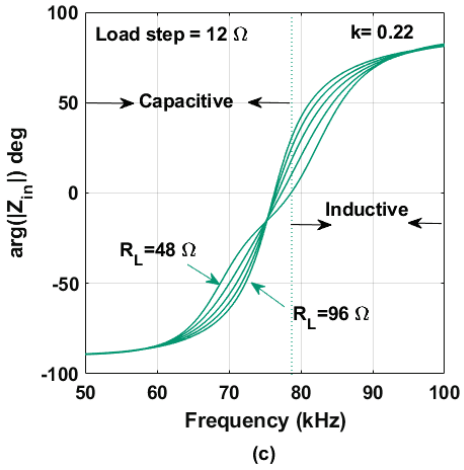


Fig. 4.8 Frequency characteristics of IPT system designed (a) Voltage gain G_{nFHA} (b) Magnitude of input impedance $|Z_{in}|$ (c) angle of input impedance $< Z_{in}$

Fig. 4.8 (a) presents the gain variation with respect to frequency with fixed coupling and varying load condition. It can been inferred from the graph that the gain at nominal operating frequency is a fixed value under varying load conditions if the coupling value is maintained constant. The input impedance variation under load change is analyzed in Fig. 4.8(b), where the impedance increases with higher load resistance. In order to prevent the switching bridge from incurring turn-on losses, soft switching technique such as Zero voltage switching (ZVS) or Zero current switching (ZCS) is a preferred operation mode for the switching bridges. The inductive region of operation for full load condition is shown in Fig. 4.8(c) which ensures ZVS operation in the primary side. Furthermore, at nominal operating frequency the circuit always works in inductive region facilitating ZVS.

4.4.1.4 Limitations of FHA model

In order to verify the accuracy of FHA model, the dc gain expression is computed for a SS compensated wireless system. The equivalent model parameters presented in Table 4.2 along with the design parameters presented in Table 4.1 and Table 4.4 is used to graph the

gain curve for the converter. From Fig. 4.9 it can be inferred that the experimental values obtained are not matching the calculated gain parameters using FHA model. A maximum deviation of 28% is observed between the experimental gain values and the calculated values.

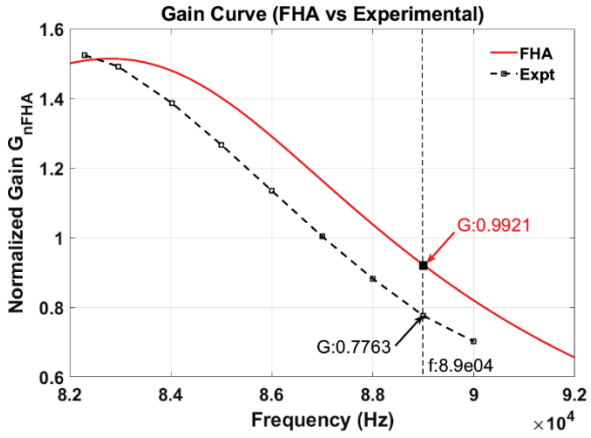


Fig. 4.9 Normalized DC gain curve for SS compensated System

The deviation of calculated gain curve values is majorly due to the invalidation of fundamental assumption that the maximum power transferred occurs through fundamental mode of operation, when the operating frequency is farther away from resonant frequency. The SS compensated DC-DC converter can be categorized as a CLLC converter with the possibility of symmetrical or asymmetrical tank structure. For symmetrical tank structure both the primary and secondary tanks have same resonant frequency leading to a unique resonant frequency of operation for the converter. In case of asymmetrical tank structure there is no unique resonant frequency defined for the converter leading to inaccuracy in converter analysis using FHA. From, Table 4.4 we can see that the converter under study has asymmetrical tank structure which leads to inaccuracies in calculation by FHA. The imprecision in the values can lead to overdesigning the converter parameters and reducing repeatability of the working parameters of converter. Hence, to improve the accuracy of

model an extended harmonic analysis is introduced in next section and an improved expression for peak tank current and gain is derived.

4.4.2 Extended Harmonics analysis

The generalized equivalent model for wireless DC-DC converter employing basic compensation topologies, derived based on (4.2) and (4.3) is presented in Fig. 4.6(b).The input square wave $v_{ab}(t)$ can be decomposed to a string of sinusoidal voltage sources connected in series including fundamental and harmonic components as presented in (4.2). Due to the small ripple across the output capacitor, the reactive power transfer from the secondary side can be assumed to be zero and hence the load can be modeled with the help of an equivalent resistance R_{eq}.The secondary current $i_s(t)$ is composed of fundamental and harmonic contents that generates the output square voltage $v_{cd}(t)$ satisfying (4.3). An extended harmonic impedance (EHA) model can be derived based on the above proposition satisfying (4.2) and (4.3) as illustrated in Fig. 4.10(a). The proposed model encompasses the effects of harmonics previously ignored in FHA model.

The proposed model introduces the concept of an equivalent resistance R_{eq} which has to be evaluated in terms of known circuit parameters for complete analysis of the circuit. Let us consider the output power equation which can be expressed as below

$$P_{out} = \frac{V_o^2}{R_L} = i_{srms}^2 R_{eq} \tag{4.23}$$

where R_L corresponds to the output load resistance, V_o to the output dc voltage and i_{srms} is the rms value of secondary current flowing through equivalent resistance.

EHA model presented in Fig. 4.10(a) comprises of a set of series connected input voltage sources connected to a passive network, hence superposition theorem can be used to

compute the effect of each voltage source on output current. Fig. 4.10(b) illustrates the equivalent circuit for the k^{th} harmonic input, which can be used to evaluate the k^{th} harmonic current as follows. The k^{th} harmonic component of input voltage is specified by

$$v_{abk}(t) = \left(\frac{4}{\pi}\right)\left(\frac{1}{k}\right) V_{dc} cos\left(\frac{\alpha}{2}\right) \sin(2\pi k f_s t) = |V_{ink}|\angle 0 \tag{4.24}$$

Input impedance of circuit for k^{th} harmonic is given by

$$Z_{ink}(k\omega) = Z_1(k\omega) + \left[Z_2(k\omega)//\left(Z_3(k\omega) + R_{eq}\right)\right] \tag{4.25}$$

$$|Z_{ink}| = \sqrt{Re\left(Z_{ink}(k\omega)\right)^2 + Im\left(Z_{ink}(k\omega)\right)^2} \tag{4.26}$$

$$\theta_k = \arg(Z_{ink}) = \tan^{-1}\left(\frac{Im(Z_{ink}(k\omega))}{Re(Z_{ink}(k\omega))}\right) \tag{4.27}$$

Using (4.24), (4.25) and extending (4.15) to k^{th} harmonic, input current i_{pk} is given by

$$i_{pk} = \frac{v_{abk}}{Z_{ink}(k\omega)} = \frac{|V_{abk}|<0}{|Z_{ink}|<\theta_k} = \left|I_{pk}\right|\angle -\theta_k \tag{4.28}$$

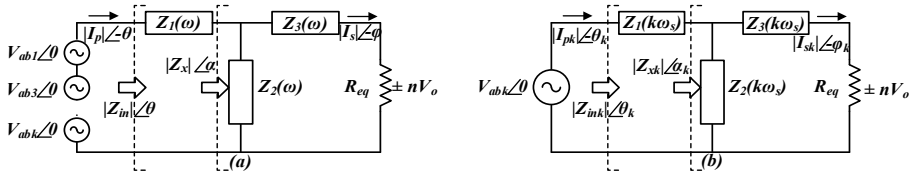


Fig. 4.10(a) Generalized Extended Harmonic Model (b) k^{th} harmonic model

Applying current divider rule on primary current i_{pk} we can evaluate i_{sk} as an extension to steps (4.18)-(4.20)

$$i_{sk} = |I_{sk}|\angle -\varphi_k = |Z_{xk}|\left|i_{pk}\right|\angle \alpha_k - \theta_k \tag{4.29}$$

where, $Z_{xk}(k\omega) = \frac{Z_2(k\omega)}{Z_2(k\omega)+Z_3(k\omega)+R_{eq}} = |Z_{xk}|\angle\alpha_k$ (4.30)

From (4.29) the phase shift required by each harmonic content φ_k is given by

$$\varphi_k = \arg(Z_{ink}(k\omega)) - \arg(Z_{xk}(k\omega)) = \theta_k - \alpha_k \tag{4.31}$$

The output voltage of the proposed equivalent circuit is a square wave $v_{cd}(t)$ as evaluated in (4.3). The net output current can be evaluated using following analysis.

$$i_s(t) = \frac{v_{cd}(t)}{R_{eq}} \tag{4.32}$$

$$i_s(t) = \sum_{\substack{m=0 \\ k=2m+1}}^{\infty} \left(\frac{4}{\pi}\right)\left(\frac{nV_o}{R_{eq}}\right)\left(\frac{1}{k}\right)\sin(2\pi k f_s t - \varphi_k) \tag{4.33}$$

$$i_s(t) = \sum_{\substack{m=0 \\ k=2m+1}}^{\infty} i_{sk}\sin(2\pi k f_s t - \varphi_k) \tag{4.34}$$

where $i_{sk} = \left(\frac{4}{k\pi}\right)\left(\frac{nV_o}{R_{eq}}\right)$, φ_k is the net phase shift for the k^{th} harmonic computed from (4.31).

To evaluate the net output power the rms value of secondary current i_{srms} has to computed as below

$$i_{srms}^2 = \left(\frac{1}{2\pi}\right)\int_0^{2\pi}\left[\sum_{\substack{m=0 \\ k=2m+1}}^{\infty} i_{sk}\sin(k\omega t - \varphi_k)\right]^2 d(\omega t) \tag{4.35}$$

The integral of function $\left[\sum_{\substack{m=0 \\ k=2m+1}}^{\infty} i_{sk}\sin(k\omega t - \varphi_k)\right]^2$ can be evaluated in two parts as shown in (4.36).

$$i_{srms}^2 = \left(\frac{1}{2\pi}\right)\left[\int_0^{2\pi}\sum_{\substack{m=0 \\ k=2m+1}}^{\infty} i_{sk}^2\sin^2(k\omega t - \varphi_k)\, d(\omega t)\right] +$$

$$\left(\frac{1}{2\pi}\right)\underbrace{\left[2\int_0^{2\pi}\sum_{\substack{m=0 \\ p,q=2m+1 \\ p\neq q}}^{\infty} i_{sp}i_{sq}\sin(p\omega t - \varphi_p)\sin(q\omega t - \varphi_q)\, d(\omega t)\right]}_{0} \tag{4.36}$$

The time average of products of two sine functions with different frequencies over a switching cycle is zero. Hence, the second part of equation reduces to 0, implying that the

net energy content in a signal with different frequencies equals to the sum of energy contents of the individual signals.

$$i_{srms}^2 = \left(\frac{1}{2}\right)\left[\sum_{k=2m+1}^{\infty}{}_{m=0}\left(\frac{4nV_o}{k\pi}\left(\frac{1}{R_{eq}}\right)\right)^2\right] = \frac{8n^2V_o^2}{\pi^2R_{eq}^2}\left[\sum_{k=2m+1}^{\infty}{}_{m=0}\left(\frac{1}{k^2}\right)\right] \quad (4.37)$$

Substituting (34) in (20) we have

$$\frac{V_o^2}{R} = \frac{8n^2V_o^2}{\pi^2R_{eq}}\left[\sum_{k=2m+1}^{\infty}{}_{m=0}\left(\frac{1}{k^2}\right)\right] \quad (4.38)$$

$$R_{eq} = \frac{8n^2R}{\pi^2}\left[\sum_{k=2m+1}^{\infty}{}_{m=0}\left(\frac{1}{k^2}\right)\right] \quad (4.39)$$

4.4.2.1 Gain Derivation

The gain equation for the proposed model can be evaluated with the help of power balance equation

$$P_{in} = P_o = \frac{V_o^2}{R} \quad (4.40)$$

Using superposition theorem to calculate the net input power for each harmonic source P_{ink}, we have

$$P_{ink} = \frac{1}{2}|v_{abk}|.\left|i_{pk}\right|.\cos(\theta_k) = \frac{|v_{abk}|^2}{2.Z_{ink}(k\omega)}\cos(\theta_k) \quad (4.41)$$

The net input power P_{in} is the sum of individual harmonic power as there is no power transfer between components of voltages with different frequencies.

$$P_{in} = \sum_{k=2m+1}^{\infty}{}_{m=0}\left[\frac{|v_{abk}|^2}{2.Z_{ink}(k\omega)}\cos(\theta_k)\right] = \left[\frac{|v_{ab1}|^2}{2.Z_{in1}(\omega)}\cos(\theta_1) + \left(\frac{1}{3^2}\right)\frac{|v_{ab3}|^2}{2.Z_{in3}(3\omega)}\cos(\theta_3) + \cdots\right] \quad (4.42)$$

$$P_{in} = \frac{|v_{ab1}|^2}{2}\sum_{k=2m+1}^{\infty}{}_{m=0}\left(\frac{1}{k^2}\right)\left[\frac{1}{Z_{ink}(k\omega)}\cos(\theta_k)\right] \quad (4.43)$$

Substituting (40) and (22) in (37) we have

$$\frac{8V_{dc}^2\cos^2\left(\frac{\alpha}{2}\right)}{\pi^2}\sum_{\substack{m=0\\k=2m+1}}^{\infty}\left(\frac{1}{k^2}\right)\left[\frac{1}{Z_{ink}(k\omega)}\cos(\theta_k)\right]=\frac{V_o^2}{R} \tag{4.44}$$

The normalized gain expression is given by

$$G_{nEHA}=\frac{nV_o}{V_{dc}}=\sqrt{\left(\left(\frac{8}{\pi^2}\right)n^2R\cos^2\left(\frac{\alpha}{2}\right)\sum_{\substack{m=0\\k=2m+1}}^{\infty}\left(\frac{1}{k^2}\right)\left[\frac{1}{Z_{ink}(k\omega)}\cos(\theta_k)\right]\right)} \tag{4.45}$$

In order to comprehend the improvement in normalized gain calculations from the EHA model a comparison curve is plotted in Fig. 4.11. As can be seen from the plot, maximum deviation from experimentally determined value has reduced from 28% in case of FHA model to 9.6% in case of EHA model. The gain curve evaluated by EHA model presented in Fig. 4.11 uses harmonic content up to 101st harmonic and leads to a better estimate than FHA model. The deviation in gain, as the frequency increases, can be attributed to the non-idealities in the circuit components, which is not modelled for reducing complexity of evaluation. The non-idealities in inductances, switches and diodes leads to loss as well as voltage drop, reducing the gain of the circuit.

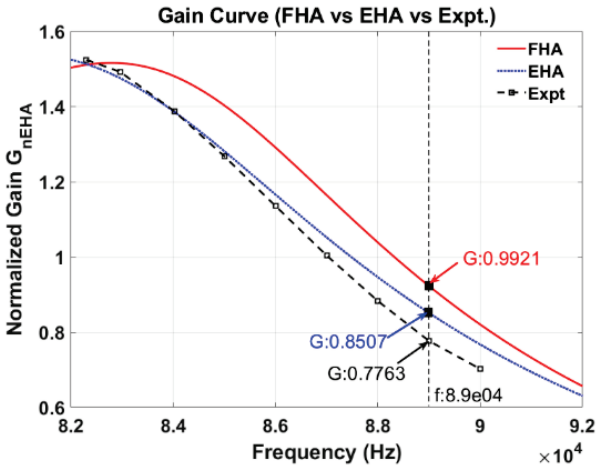


Fig. 4.11 Normalized DC gain curve comparison for SS compensated system

4.4.3 Selection of Parameters

A series-series IPT can be designed under two conditions of operation (i) compensation capacitors resonating with leakage-inductances (ii) compensation capacitors resonating with self-inductances.

Let the resonant frequencies of primary and secondary side given by equation (4.21) and (4.22) be equal and represented as below

$$f_{pri} = f_{sec} = f_o = \frac{1}{2\pi\sqrt{LC}} \tag{4.46}$$

Researchers in [56] define a boundary condition for the resonance of leakage inductance with compensation capacitors as below

$$f_s \geq \frac{f_o}{\sqrt{1-k}} \tag{4.47}$$

where f_s represents the switching frequency, f_o the resonant frequency of combination, k the coupling co-efficient between primary and secondary pad.

Under the boundary condition presented in (4.47) the fundamental harmonic approximation is still valid and the equivalent circuit of operation is given by Fig. 4.7. Since the primary and secondary inductances are consider equal for simplified analysis we can write the following relations based on the equivalent model

$$Z_1 = j\left(\omega L(1-k) - \frac{1}{\omega C}\right) \tag{4.48}$$

$$Z_2 = j\omega kL \tag{4.49}$$

$$Z_3 = j\left(\omega L(1-k) - \frac{1}{\omega C}\right) \tag{4.50}$$

The input impedance when operating under the boundary conditions given in (4.47) can be derived as below from (4.12)

$$Z_{in1} = Z_1 + \left(\frac{Z_2*(Z_3+R_{FHA})}{Z_2+Z_3+R_{FHA}}\right) = \frac{j\omega_s kL*R_{FHA}}{j\omega_s kL+R_{FHA}} \tag{4.51}$$

Using equations (4.15) - (4.20) the expression for voltage gain at the boundary condition can be computed as below

$$i_{p1} = \frac{V_{in1}}{Z_{in1}} = \frac{V_{in1}}{j\omega_s kL*R_{FHA}}(j\omega_s kL + R_{FHA}) \tag{4.52}$$

$$i_{s1} = i_{p1} * \frac{Z_2}{Z_2+Z_3+R_{FHA}} = \frac{V_{in1}}{R_{FHA}} \tag{4.53}$$

$$nV_o = V_{in1} \tag{4.54}$$

In case of operation strictly at the boundary condition presented by (4.47) unity gain is obtained for SS compensation. Smaller output voltages are realized with either phase-shift or setting switching frequency higher than the boundary value. The benefits of operating at boundary condition is the easier controllability of output voltage [70] and avoidance of bifurcation under varying load conditions [55], [70], [71]. The main disadvantage of this operating point is the dependency of the operating frequency to coupling. Since the laboratory prototype is currently being evaluated for a stationary condition with negligible change in k value this point of operation is apt to satisfy control requirements.

Using conditions (4.21), (4.22) and (4.47) the parameters are selected to meet the operating frequency requirements. The characteristic curves of the proposed design based on simulated results using FHA model are shown in Fig. 4.12. As predicted there is no variation in gain for load change as presented in Fig. 4.12(a). Additionally, to achieve soft switching the tank characteristic should lie in inductive region which is satisfied under the selected operating point as can be inferred from Fig. 4.12(b).

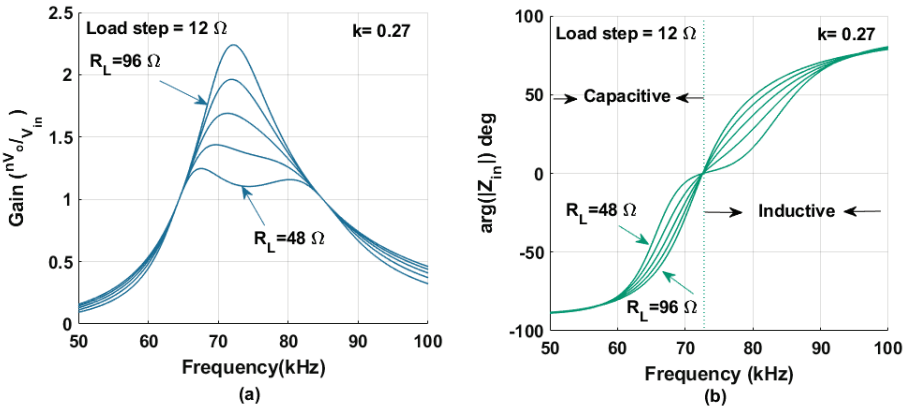


Fig. 4.12 Frequency characteristics of initial IPT system (a) Voltage gain G_{nFHA} (b) angle of input impedance $< Z_{in}$

In order to select the resonant capacitor the voltage rating of the capacitor has to be properly evaluated. Using parameters from Table 4.3 and equations (4.25), (4.28) the primary and secondary current values can be evaluated from EHA model. From, Fig. 4.13 it can be seen that the peak primary capacitor voltage can be as high as 2kV while secondary capacitor voltage reaches 1.5 kV rating for full rated output current condition.

Table 4.3 Initial parameters for IPT system design

Parameters	Values
Coil separation (cm)	10
Resonant frequency f_{pri}, f_{sec} (kHz)	72.62
Switching frequency f_s (kHz)	85
Primary self-inductance L_p (μH)	283
Secondary self-inductance L_p (μH)	283
Mutual-inductance L_m (μH)	76
Primary Capacitance C_p (nF)	17
Secondary Capacitance C_s (nF)	17

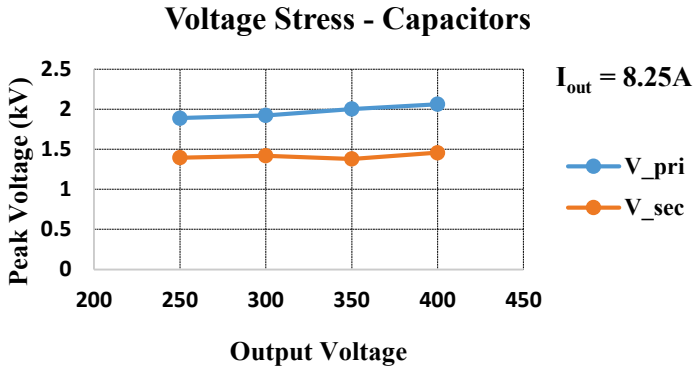


Fig. 4.13 Voltage stress evaluation on resonant capacitors

A capacitor bank is built to meet the high voltage stress requirements of the resonant capacitor. Film capacitor B32652A2472K000 has a peak DC rating of 2kV but under 100 kHz condition the voltage carrying capacity is de rated to 700 V peak based on manufacturer data sheet and hence an array of capacitors is built. The selected array size and the experimentally obtained value is specified in Table 4.4.

Table 4.4 Final resonant tank parameters

Capacitor Location	# in series	# in parallel	Capacitance (value)
Primary	5	17	15.98 nF
Secondary	3	10	15.67 nF

4.5 Control Strategy

The basic requirement of wireless dc-dc stage is to maintain a constant output voltage as requested by the battery management system. From equation (4.45) we can formulate two different control schemes to facilitate output voltage and current control.

4.5.1 Pulse frequency modulation (PFM) control

PFM is a very common control technique employed for control of resonant circuits. According to equation (4.45) it can be concluded that output voltage is a function of frequency. Furthermore, for a fixed input dc voltage supplied by the input conditioning circuit the switching frequency of circuit can be varied to change the output voltage of the circuit enabling the operation of converter under varying battery voltage condition. A typical control structure for PFM technique is presented in Fig. 4.14.

Wireless DC-DC converter block in Fig. 4.14 symbolizes the topology presented in Fig. 4.1. The primary side switches are supplied using gate pulses generated from the control loop while the secondary rectifier bridge uses diode bridge for rectification. Fast SiC diodes are available in market capable of high frequency switching with very low reverse recovery and on-state voltage drop which can be employed for rectification. The basic control loop uses sensed output voltage from on-board battery which is shared to off-board stage with the help of a Wi-Fi communication channel. The sensed voltage is compared with the required reference value which is passed through a PI controller which generates the Δf_s value which is subtracted from a center frequency or the nominal operating frequency. The output of the block generates the new switching frequency required to stabilize the output voltage to required value. An oscillator generates a 50% duty cycle pulse of the required frequency which is supplied to the gate drivers of primary inverter circuit.

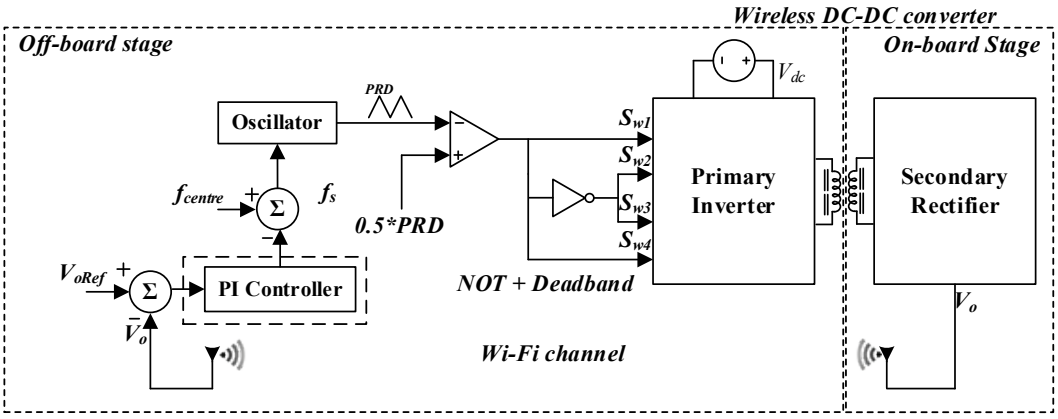


Fig. 4.14 Control block diagram for PFM

PFM works on the principle of gain variation proportional to operating frequency. In case of wireless systems this control technique may lead to high oscillation in output due to limited resolution of digital controller which limits the variation of frequency. Additional constraints have to be imposed to properly control the circuit using this structure. The main advantage of this technique is that under varying coupling conditions the change in resonant frequency can be accounted to and frequency shift can be made possible facilitating higher efficiency.

4.5.2 Primary side phase shift control

In previous section the basic operation principle of wireless dc-dc stage has been analyzed. The primary inverter bridge of dc-dc stage generates a quasi-square wave with variable fundamental magnitude as shown in Fig. 4.5. The fundamental magnitude of square wave applied to the resonant wireless network is quantified in equation (4.2). It is evident from this equation that by controlling α the phase shift between the primary switching legs we can change the zero portion of quasi square wave which leads to change in input voltage. Furthermore, for a fixed operating frequency the gain of the circuit is held constant which enables the control of output voltage by varying input excitation magnitude.

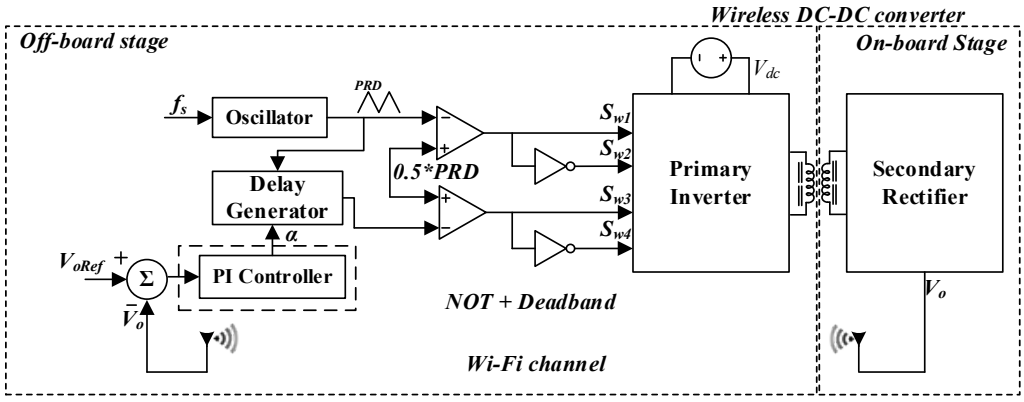


Fig. 4.15 Control block diagram for primary side phase control

A control diagram enabling primary side phase shift control of wireless dc-dc stage is presented in Fig. 4.15. The control loop uses sensed voltage data that is shared wirelessly to off-board components using a Wi-Fi channel. The error in sensed voltage is fed to a PI control which generates the appropriate α value capable of reducing the error to zero. The generated phase shift is used as an input to a delay generator block which outputs triangular waveform with fixed frequency f_s phase shifted by a magnitude of α with respect to the reference. The gate pulses to various switches are generated by comparing the two phase shifted triangular waveforms to half its magnitude resulting in a square pulse of 50% duty cycle which is delayed to each other by the required amount.

Since, fundamental voltage magnitude variation is the key control parameter enabling phase shift control, it indirectly reduces the amount of primary side tank current which helps in reducing the overall conduction losses of wireless stage. Even though the primary current is reduced due to quasi input voltage waveform the lagging leg of off-board inverter bridge has the possibility of losing ZVS which leads to additional losses. Since, the basic operation principle relies on magnitude reduction this control scheme is not suitable for any boost function and may need to be supplemented with a PFM loop depending on

application. Additionally, the detuning of circuit caused by misalignment may lead to unachievable power transfer condition along with loss of ZVS operation in bridges which has to be taken into consideration during the design of resonant network.

4.6 Simulation Results

A simulation study is carried out using MATLAB Simulink to understand the behavior of system under varying conditions as well as to validate the various modeling study carried out in previous section. The system under study uses parameter from Table 4.3. Fig. 4.16 presents the key operating waveforms of wireless DC-DC stage designed in previous sections. Since, the operating frequency was decided to be 85 kHz the designed system at full load should be able to provide the output maximum voltage at this operating frequency for primary phase shift control.

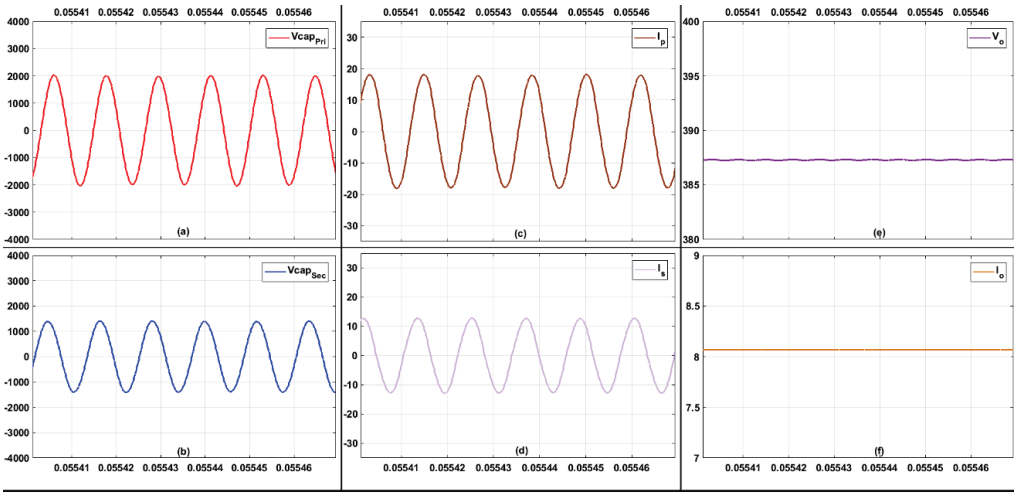


Fig. 4.16 Wireless DC-DC simulation using initial parameters @ 85 kHz (a) Primary resonant capacitor voltage (b) Secondary resonant capacitor voltage (c) Primary tank current (d) Secondary tank current (e) Output voltage (f) Output current

It can be inferred from the waveforms that the output voltage is not able to reach 400V at this operating frequency with the designed tank parameters. The difference in value is due

to the increased gain predicted by FHA model in Fig. 4.12(a). With the help of frequency control the desired output voltage can be reached. The waveforms presented delivers highest output current of 8.25A which is the maximum value supplied by the system.

A new set of simulations is completed to analyze the operation of system with the parameters of measured coil inductances and the designed capacitor bank values. The key parameters used to simulate the system are presented in Table 4.5.

Table 4.5 IPT System parameters for laboratory prototype

Parameters	Values
Coil separation (cm)	10
Resonant frequency f_{pri} (kHz)	78.06
Resonant frequency f_{sec} (kHz)	73.17
Switching frequency f_s (kHz)	85
Primary self-inductance L_p (μH)	275.3
Secondary self-inductance L_p (μH)	273.8
Mutual-inductance L_m (μH)	63.29
Primary Capacitance C_p (nF)	15.98
Secondary Capacitance C_s (nF)	15.67

The simulated system generates an output voltage of 400V while supplying full load output current of 8.25A. A PFM based control strategy is employed to simulate the performance of the system. The key waveforms obtained from MATLAB simulation are presented in Fig. 4.17 (a) – (f). The peak capacitor voltages on primary and secondary capacitors are below the maximum voltage rating of the designed capacitor array.

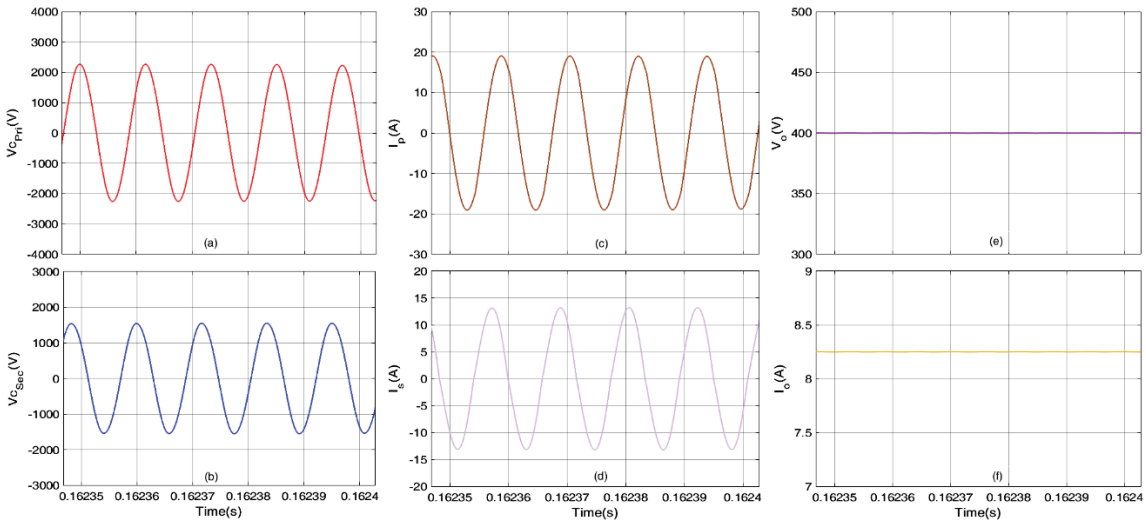


Fig. 4.17 Wireless DC-DC simulation based on laboratory prototype @ 85 kHz (a) Primary resonant capacitor voltage (b) Secondary resonant capacitor voltage (c) Primary tank current (d) Secondary tank current (e) Output voltage (f) Output current

4.7 Experimental Verification

As a proof of concept verification of the operation of wireless dc-dc stage of the proposed charger, a laboratory prototype is built with the help of key components, presented in Table 4.6.

Table 4.6 Key Components enabling lab prototype development

Parameters	Part no	Specification
Coil Ferrite core	B66291P0000X187	N87 Ferrite Core, 5mm thickness
Primary MOSFETs	C2M0080120D	1200V, 24 A, 80mΩ
Secondary Diodes	VS-60APU06-N3	600V, 60A, 1.35V
Resonant Capacitor	B32652A2472K000	4.7nF, 2kV DC

The initial prototype structure is presented in Fig. 4.18, where the dc input source is a SL series Magna-Power power supply. The DC input is fed to a primary inverter bridge made of SiC Cree MOSFET rated at 1.2 kV with a typical on-state resistance of 80mΩ. The

output generated by the bridge acts as the input to resonant tank and energizes the primary transmitting coil. The receiving coil is placed at a separation of 10cm which feeds the rectifier network made of diodes and feeds Chroma DC electronic load emulating battery.

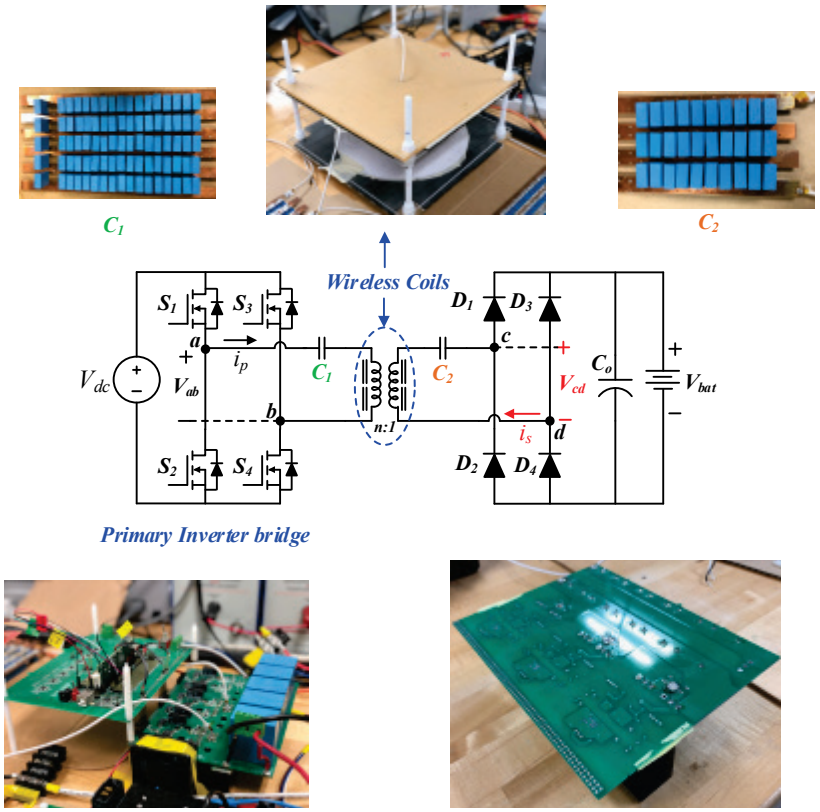


Fig. 4.18 Initial laboratory prototype of wireless DC-DC converter

Fig. 4.19 presents the key operating waveforms of wireless DC-DC converter measured in the course of experiments. Differential voltage probe P5200A and high precision current probe TCP0030A from Tektronix are used to measure the operating waveforms. The primary current lags the differential voltage V_{ds4} showing inductive nature of circuit and zero voltage switching (ZVS) operation as highlighted in Fig. 4.19. The secondary current i_s is in phase with diode voltage V_{D4} operating under zero current switching (ZCS). The soft switching introduced in primary and secondary side leads to negligible switching losses while the high current at turn off of primary side switches introduces turn off loss in the system.

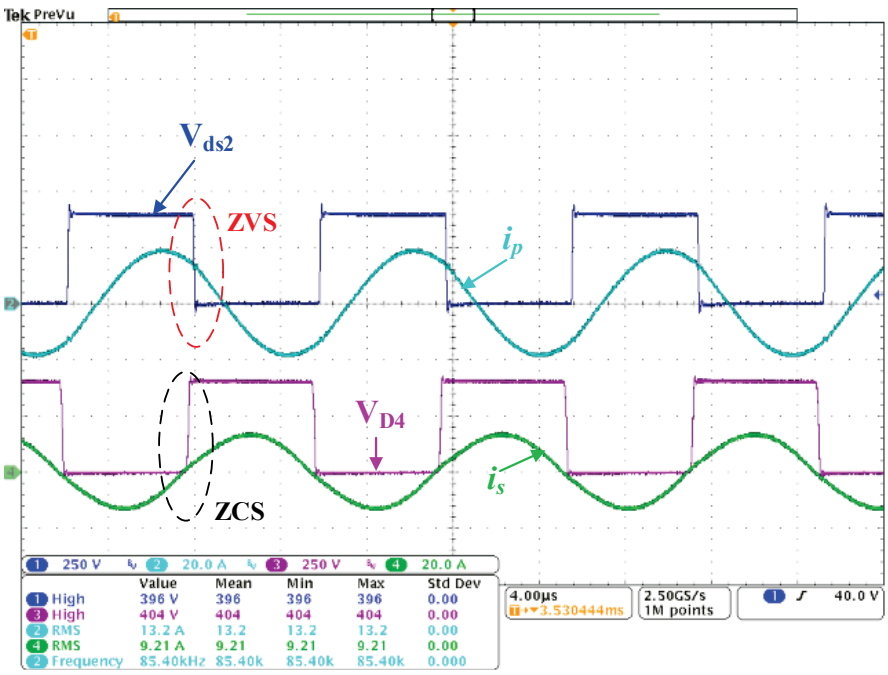


Fig. 4.19 Key Operating waveforms of wireless DC-DC stage

The efficiency of wireless stage is recorded with the help of Tektronix power analyzer shows an efficiency of 94.17% at 3.3 kW. Group D or CH4 presents the input values while Group C or CH3 presents the output parameters of the circuit. The resonant parameters used generates unity gain at an operating frequency of 85.4kHz.

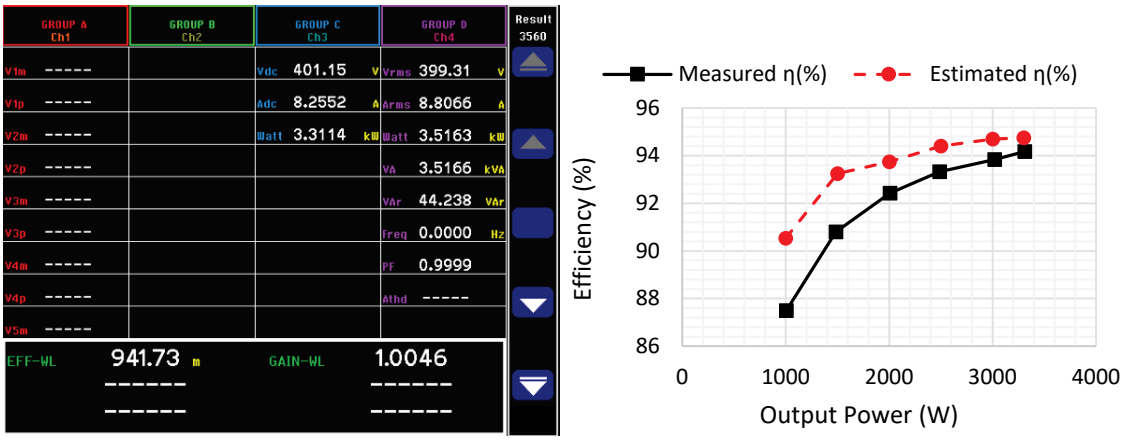


Fig. 4.20(a)Efficiency measurement from Tektronix power analyzer (b)Estimated vs Measured efficiency over load range

A loss study is carried out on the DC-DC stage using the major loss producing components presented in Table 4.7.

Table 4.7 Parameters generating major loss in Wireless DC-DC stage

	Parameter	Value
Primary Side	Capacitor ESR	0.25 Ω
	Switch resistance	0.08 Ω
	Coil Resistance	0.165 Ω
Secondary Side	Capacitor ESR	0.2 Ω
	Diode drop	1.45 V
	Coil Resistance	0.165 Ω
	Switching frequency	85.4 kHz

The comparison results of measured efficiency along with estimated efficiency is presented in Fig. 4.20(b). The efficiency under low load conditions is affected by conduction losses in primary side introduced due to increased reactive power flow. As the power increases the net reactive power supplied is not varying drastically which improves the efficiency of system. The differences in estimated and measured values are introduced due to idealized modeling used for loss evaluation.

Fig. 4.21 presents the estimated loss split of the prototype built in lab at 3.3kW output with a total loss of 183W. The key loss producing components are the resonant capacitors and wireless coil accounting to 59% of total loss. The resonant capacitor bank assembled using an array of film capacitors leads to a high amount of loss due to effective series resistance (ESR) as inherently the loss dissipation factor of film capacitor is high. Alternate, low ESR but high cost capacitors available in market can potentially reduce this loss and increase

efficiency by 3%. Recently, ceramic capacitors capable of high voltage blocking are introduced in market which could also potentially serve as a replacement to film capacitors with reduced losses. Additionally, use of secondary side diodes account for 15% of total loss from on-state drop which can potentially be reduced with the help of use of synchronous rectification.

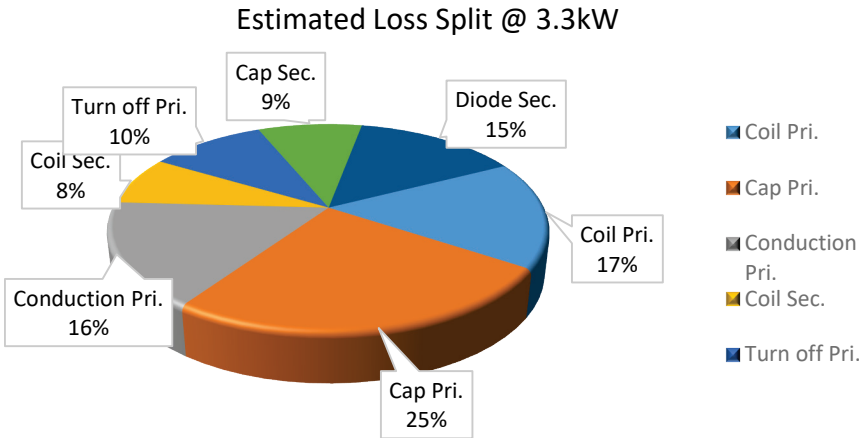


Fig. 4.21 Wireless DC-DC converter estimated loss split @ 3.3kW

4.8 Summary

In this chapter, a system level design of wireless DC-DC stage of the proposed integrated charger has been completed. A series-series compensation topology with resonant frequency tuned to leakage inductance is selected to achieve better output controllability with minimum resonant components. The conventional modeling of resonant converter is based on the assumption that the majority of power transfer happens at the fundamental frequency which is invalidated in the proposed compensation strategy. In order to improve the modeling accuracy of wireless DC-DC stage an extended harmonic analysis (EHA) method is introduced which uses superposition of multiple frequency components to quantify the effects of harmonic power transfer. The proposed EHA method is applied to

select the various components of the wireless system. As a proof of concept, a 3.3 kW laboratory prototype of the system is designed to operate from a 400V input to charge a 400V battery. According to the experimental results, a peak efficiency of 94.17% is obtained at full load, where the combined losses from coil and capacitor bank accounts for 59% of total losses (183W).

Chapter 5: Analog Synchronous Rectification based Integrated Charging System

In previous chapters, various off-board components of the integrated charging system has been critically evaluated and selected to achieve high efficiency operation. The key focus of this research is to develop an integrated wired and wireless charging system capable of topological integration with an existing on-board charger with minimum modifications. The selected charging structure uses a single phase totem pole PFC in cascade with a series-series compensated wireless DC-DC stage to charge the battery. The on-board rectification stage of the proposed charger is integrated to the existing on-board charger components.

Conventionally, wireless charging system uses a diode bridge based rectification circuit on-board the vehicle to convert high frequency AC output to DC battery voltage. Since, the on-board rectifier is merged with an active bridge from vehicle on-board charger it may be required to parallel additional diodes. The body diodes of high frequency switches compared to the MOSFETs suffers from reverse recovery, higher voltage drop, and reduced current rating. This results in system derating, degraded system efficiency, thermal performance, and electromagnetic interference (EMI) performance. Furthermore, all existing on-board chargers may not have additional parallel diodes, which may require redesign of the circuit board not satisfying the minimum modification requirement. This leads to the need of a unique solution on-board the vehicle to facilitate the proposed charging strategy. An analog synchronous rectification circuit is proposed to use the active bridge on-board the vehicle without the need of additional diodes with minimum modification to existing on-board circuit.

5.1 Synchronous Rectification (SR)

Synchronous rectification (SR) using an active bridge circuit is one of the well-known methods employed to reduce the conduction losses of diode bridge based rectification stage. The interest in bidirectional operation of on-board chargers facilitating vehicle to grid (V2G) operation has already led to the use of active bridges on primary and secondary side of on-board converters. Active rectification on output stage of such high frequency enabled converters requires the exact knowledge and control of phase shift between primary and secondary side bridges. A synchronization technique for bidirectional WPT system is introduced by researchers in [72], where an auxiliary sense winding is employed to extract a synchronization signal proportional to primary current. Since, the sense winding current affects the field generated complicated processing is required to extract the exact information of primary current which is required to synchronize power flow. An improved bidirectional pq based control technique is proposed in [73] which uses analog multipliers and low pass filtering circuits with phase shift to compute the instantaneous real and reactive power flow in circuit which is used to generate the synchronizing angle. The proposed control technique requires the use of a microcontroller system to facilitate bidirectional power control. The researchers in [74] have proposed a FHA based model to predict the phase shift between primary and secondary side of a half bridge bidirectional CLLC converter employed in on-board charger. Similarly, an improved phase estimation is provided by extended harmonic analysis (EHA) in [75] which includes the effect of harmonic power improving accuracy of estimation. The phase estimation techniques proposed by the researchers requires proper synchronization between primary and secondary side bridges which is enabled by the control from a single microcontroller. In

case of wireless charging systems the primary and secondary sides are separated by an air gap with different controllers which generates synchronization issues due to the need of high frequency trigger transmission. Analog high frequency SR ICs using drain to voltage detection for synchronization are currently available for low voltage applications (<50V) which was tested successfully by researchers in [76] for low voltage wireless power transfer. Since, wireless EV charging operation requires analog SR ICs capable of working with high voltage (>400V) signals commercially available solutions are not viable for implementation. Thus to implement the proposed integrated charging solution a novel analog synchronization method is proposed which requires an on-board current sensor and opamp based compensation circuits without the need for an onboard controller for SR operation. The proposed system can operate under frequency modulation based control since there are no sampling limitations nor bandwidth constraints as synchronization is carried out using analog zero crossing detection circuits.

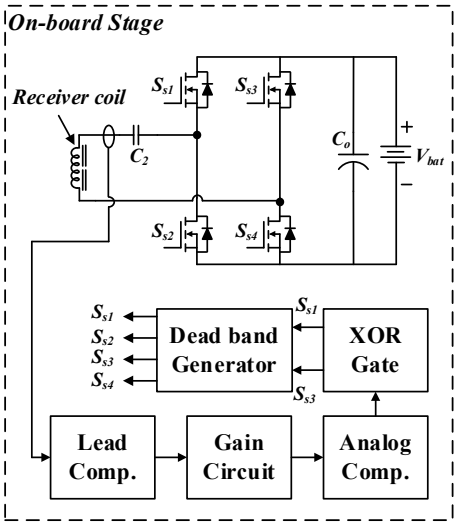


Fig. 5.1 Proposed analog SR block diagram

The block diagram for the proposed analog solution is presented in Fig. 5.1.The secondary side sensed current is processed using a lead compensation network to nullify any sensing

delay introduced by sensing network. The compensated signal is passed through a non-inverting summer circuit to synthesize a unipolar sine wave which is further compared with the dc-offset to generate a stable zero crossing signal using a high speed compensator. Since, the active rectifier bridge requires four driving signals the generated pulse is passed through an XOR gate followed by a dead-time circuit to generate the required gate pulses. The different circuits used to realize the various blocks of the analog synchronization circuit are presented below

5.1.1 Lead compensation network

As per SAE J2954 standard for wireless charging of electric vehicles, the wireless power transfer circuit uses 85 kHz as the transmission frequency. The secondary side current sensing at such frequencies may generate a phase lag between the original signal and sensed output due to bandwidth limitations of the sensor. A typical industrial current sensor like LEM LA 55-P is capable of sensing signals upto 200 kHz range based on datasheet parameters. From practical measurements the current sensor generates a phase delay in the range of 30^{o} at 85 kHz. Additionally, high frequency noise signals generated by switching propagate through the sensed currents especially near zero crossings that needs to be eliminated by low pass filtering circuits to generate stable zero crossing signals. The use of filtering circuits also introduces additional phase delay in the sensed signals.

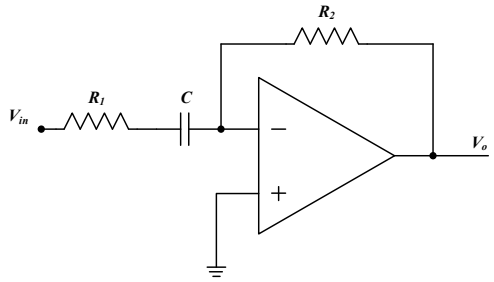


Fig. 5.2 Proposed lead compensation network

To achieve accurate SR operation, the delay introduced in sensed signals needs to be compensated with the help of a lead compensation network. The proposed lead compensation network is presented in Fig. 5.2. The transfer function of the proposed network can be evaluated as below

$$\frac{v_{in}-0}{R_1+\frac{1}{sC}} = \frac{0-v_o}{R_2} \tag{5.1}$$

$$G = \frac{v_o}{v_{in}} = -\frac{scR_2}{1+scR_1} \tag{5.2}$$

The phase generated by the compensation network can be quantified as below

$$< G = -90 - \tan^{-1}\omega CR_1 = \underbrace{270 - \tan^{-1}\omega CR_1}_{\varphi_{lead}} \tag{5.3}$$

Where, $180 < \varphi_{lead} < 270$

Alternatively, if the output is considered as an inverted sine wave the lead angle φ'_{lead} is bounded by

$$0 < \varphi'_{lead} < 90 \tag{5.4}$$

The output waveform generated by the compensation network for a sinusoidal input is presented in Fig. 5.3.

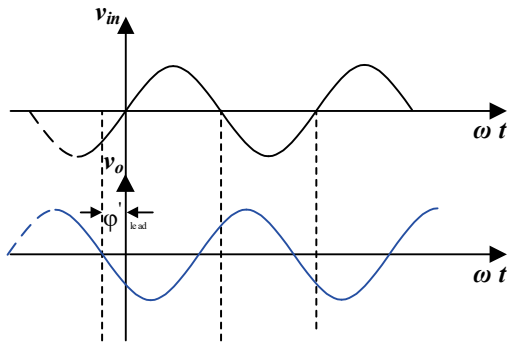


Fig. 5.3 Key operating waveforms of the proposed compensation network

The value of φ'_{lead} required for the design is calculated from the delay between sensed input and output signals. In case of a delay between sensed input and output signals the switching pulses are generated with a delay compared to the zero crossing of the current. The delay in pulse generation acts as a lead in current with respect to switch node voltage that helps in generating zero voltage switching (ZVS) characteristics of the active bridge. The proposed compensation network can generate any lead value between (0 and 90^o) which can be properly tuned to achieve ZVS characteristics with minimum reactive power. The key design equations for the proposed network are presented below

$$|G| = \sqrt{\frac{\omega^2 C^2 R_2^2}{1+\omega^2 C^2 R_1^2}} = 1 \tag{5.5}$$

$$90^o - \tan^{-1} \omega C R_1 = \varphi'_{lead} \tag{5.6}$$

The sensed output current generates a phase lag of 55^o due to cascaded effect of sensor delay and low pass filter used in circuit. A phase lag of 20^o is provided to generate ZVS characteristics of active bridge. The compensator parameters are designed to generate of lead of 35^o at 85 kHz to meet the target operating point. The system parameters designed based on equations (5.5) - (5.6) are presented in Table 5.1

Table 5.1 Compensation parameters required to generate φ'_{lead}

Parameter	**Value**
C	3.3 nF
R_1	810 Ω
R_2	988 Ω

The designed system is simulated using MATLAB Simulink and the input and output waveforms are presented in Fig. 5.4. The output waveform is leading the input waveform with a phase angle of 35° with unity gain as designed.

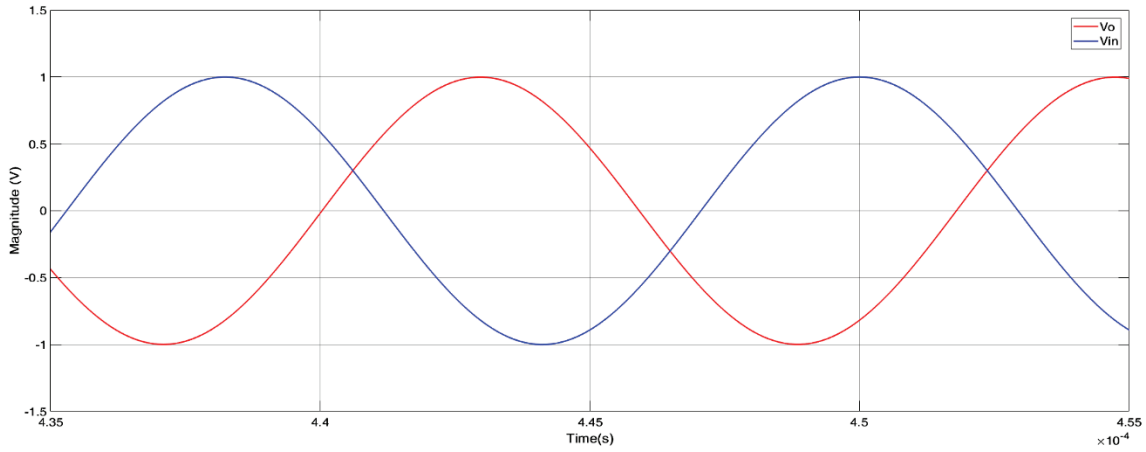


Fig. 5.4 Phase relationship between input and output waveform of proposed lead compensator

As evident from Fig. 5.4 the compensated sense signal is an inverted version of the original current waveform even though the zero crossing point leads the input waveform. The inversion caused by the compensation network has to be negated at the gate signal generation point for proper operation of the circuit.

5.1.2 Gain circuit

The proposed analog SR circuit uses the gain stage to introduce a dc-offset to the compensated signal. The bipolar current signal is converted to a unipolar version to remove common mode noise effects at zero crossings. The unipolar signal is generated with the help of a unity gain non-inverting summing amplifier as presented in Fig. 5.5. The output of the circuit can be expressed in terms of various resistors as below

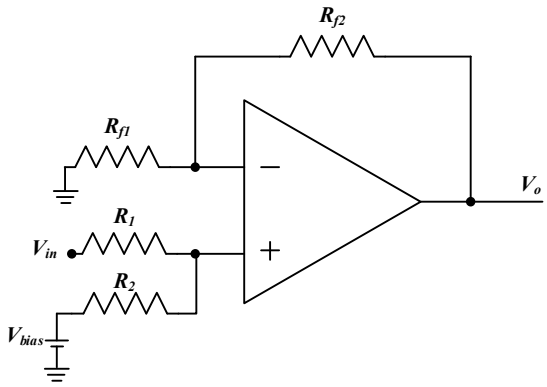


Fig. 5.5 Non-inverting summing amplifier circuit

$$v_o = \left(\frac{v_{in}}{R_1} + \frac{V_{bias}}{R_2}\right) * \left(1 + \frac{R_{f2}}{R_{f1}}\right) * \left(\frac{R_1 R_2}{R_1 + R_2}\right) \tag{5.7}$$

To obtain unity gain we use the following constraint on (5.7)

$$R_1 = R_2 = R_{f1} = R_{f2} = R \tag{5.8}$$

$$v_o = v_{in} + V_{bias} \tag{5.9}$$

The bias voltage V_{bias} is generated from a stable source with minimum variations to ensure accurate zero crossing detection. The magnitude of V_{bias} is selected to be $\frac{V_{spk}}{2}$ where V_{spk} is the peak voltage of the sensed signal. The output gate pulses generated from the analog SR is designed to be compatible with a 3.3V logic of microcontrollers and hence the V_{cc} of following stages are selected to be 3.3V. Due to the constraints on the supply voltage of the opamp the dc offset bias voltage is selected to be 1.55V.

5.1.3 Comparator circuit

The compensated sensed current signal is processed using gain stage which acts as the input to the comparator circuit. A high speed analog comparator IC with very low propagation delay is required to generate the zero crossing signals as the sensed signals are in 85 kHz range. The low pass filter applied on the sensed signals may result in attenuated

noise propagation as the corner frequency of low pass filter is constrained due to phase lag generated at the output. To aid stable output generation a small hysteresis band is introduced which help in improving the noise immunity of the comparator near the zero crossing instants. The proposed comparator circuit with hysteresis band is presented in Fig. 5.6.

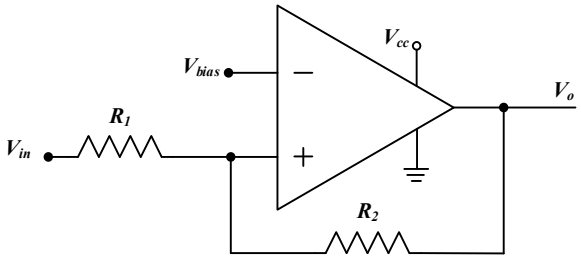


Fig. 5.6 Analog comparator circuit with hysteresis band

The output switches from low to high when V_{in} rises above the high threshold value V_{in1} given by

$$V_{in1} = V_{bias} * \left(1 + \frac{R_1}{R_2}\right) \tag{5.10}$$

The low threshold value V_{in2} where the output switches from high to low output is given by

$$V_{in2} = V_{bias} * \left(1 + \frac{R_1}{R_2}\right) - V_{cc} * \left(\frac{R_1}{R_2}\right) \tag{5.11}$$

The hysteresis band across the input voltage Δv can be evaluated as below

$$\Delta v = V_{in2} - V_{in1} = V_{cc} * \left(\frac{R_1}{R_2}\right) \tag{5.12}$$

5.1.4 Complementary pulse + dead band generation

The high speed comparator circuit generates a single ZCD signal which acts a reference for generating four gate pulse to control the active bridge. The two legs of active bridge circuit are controlled by complementary signals which is generated from the reference ZCD signal with the help of XOR gate logic. The Boolean expression for an XOR gate is given below

$$A \oplus B = \overline{A}B + A\overline{B} \tag{5.13}$$

The truth table of operation used to generate the bridge control signal is presented in

Table 5.2 Truth table for XOR based control signal generation

A	B	$A \oplus B$	Comment
0	0	0	Buffered input signal with propagation delay
1	0	1	
0	1	1	Complementary signal
1	1	0	

where, A and B represents the inputs to the XOR gate.

The control signal generated from XOR logic needs to be further processed to control the active bridge. Due to non-ideal switching behavior such as rise time and fall time of the switches, a finite dead-time or blanking interval is required to prevent shoot through of the leg. An external dead band generation logic has to be developed using digital gates or with gate drive circuit with inbuilt dead band generation capability.

5.1.5 Implementation of the proposed SR circuit

The various constraints and requirements imposed by each block of the proposed SR solution (Fig. 5.1) is introduced in previous sections. Table 5.3 summarizes the key components selected for the design of proposed synchronization logic.

Table 5.3 Key components selected for SR design

	Component	Part no	Key Features
Opamp	Lead compensation Non-inverting summing amplifier	TLV172IDR TLV172IDR	10 MHz bandwidth 10V/µs slew $\pm 18V$ supply
Comparator	High speed Precision comparator	LMV761MA	120 ns propagation delay with overdrive of 50mV 3.3V compatible
XOR logic	Quad output XOR gates	SN746ND	Max propagation delay at 3.3V logic 12.5 ns
Dead time generator	Gate drive with inbuilt dead-time generation logic	Si82394AD	200ns max dead-time

The schematic diagram for implementing the proposed logic is presented in Fig. 5.7. The onboard receiver current is sensed with the help of an LEM sensor LA55P with capacitive filter at the output. The sensed current generates a phase lag of 55^o which is reduced to a targeted lead of 20^o with the help of a high bandwidth opamp (TLV172IDR) based lead compensator. The compensated signal is further processed using a unity gain non-inverting summing amplifier to generate a unipolar sine wave. A ZCD signal is synthesized with the help of a high speed comparator (LMV761) operating at 3.3V logic by comparing unipolar

sine wave with dc offset. The ZCD signal acts as the reference to generate complementary half bridge reference pulses using XOR logic that is fed to gate drive IC Si83294AD driving the active bridge.

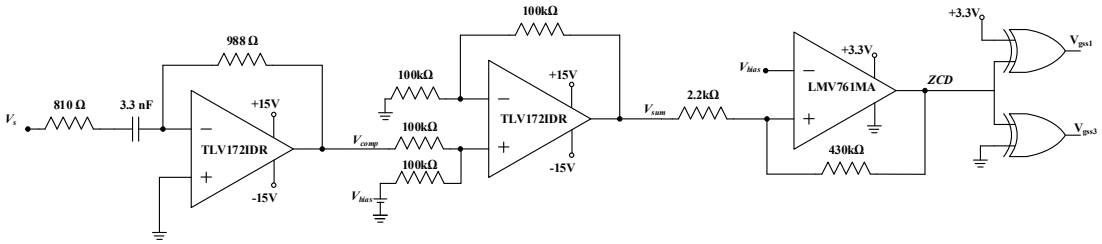


Fig. 5.7 Schematic diagram of the proposed analog synchronization circuit

5.2 Experimental Verification of Analog SR circuit

As a proof of concept verification of the proposed SR, a laboratory prototype is developed using the key components in Table 5.3. The experimental prototype presented in Fig. 5.8 generates the gate pulse to control an on-board full bridge structure developed with SiC based MOSFETs from CREE (C2M0080120D).

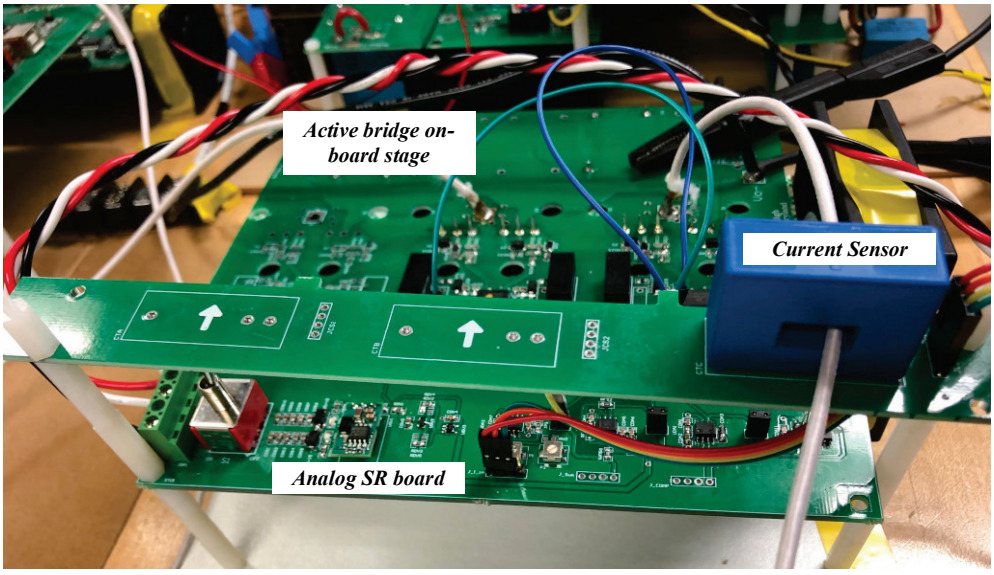


Fig. 5.8 Experimental prototype of proposed analog SR stage

The equivalent circuit diagram as well as measurement conventions followed on the experimental prototype are presented in Fig. 5.9. The primary side current i_p flowing out of the bridge and the secondary side current i_s flowing into the bridge are considered as positive reference directions. The drain to source voltages of low side switches are measured on primary and secondary bridge.

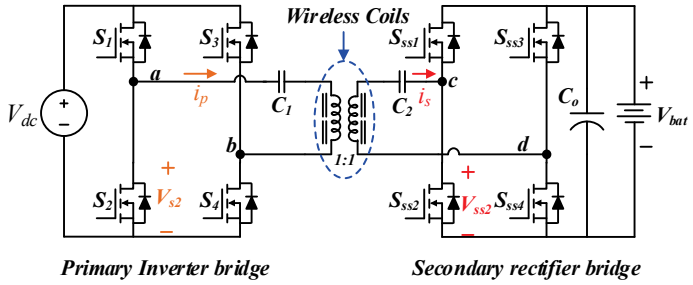


Fig. 5.9 Wireless DC-DC equivalent circuit with active rectification

The wireless DC-DC converter with active rectification is tested till 3.3 kW and the key operating waveforms are presented in Fig. 5.10.

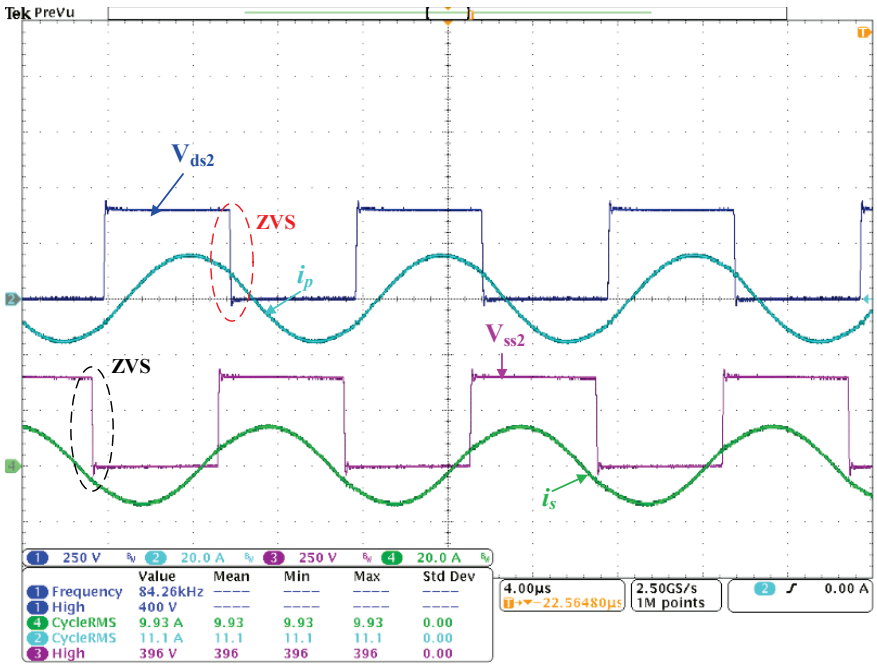


Fig. 5.10 Key operating waveforms of wireless DC-DC stage with active rectification

The differential voltage V_{ds2} measured indicates that during turn ON of the switch S_2 the current i_p is positive which indicates soft switching operation as the body diode of the switch is conducting during dead time interval. Similarly, if the secondary current is negative at the switch turn ON instant the body diode will be under conduction leading to ZVS turn ON for switch V_{ss2}. The soft switching instants of primary and secondary side bridges are indicated in Fig. 5.10.

The operating efficiency as well key parameters of the converter at full load is presented in Fig. 5.11(a). A full load efficiency of 95.42 % is achieved by the system using proposed analog SR based active rectification. The efficiency under various loading condition for wireless system with diode rectification and active rectification is compared in Fig. 5.11(b). The wireless converter with active rectification stage has improved full load efficiency by 1.25 % and generates a 2.6% increase in efficiency at 1kW operation. The proposed SR circuit helps in improving the efficiency of wireless stage as predicted from analysis.

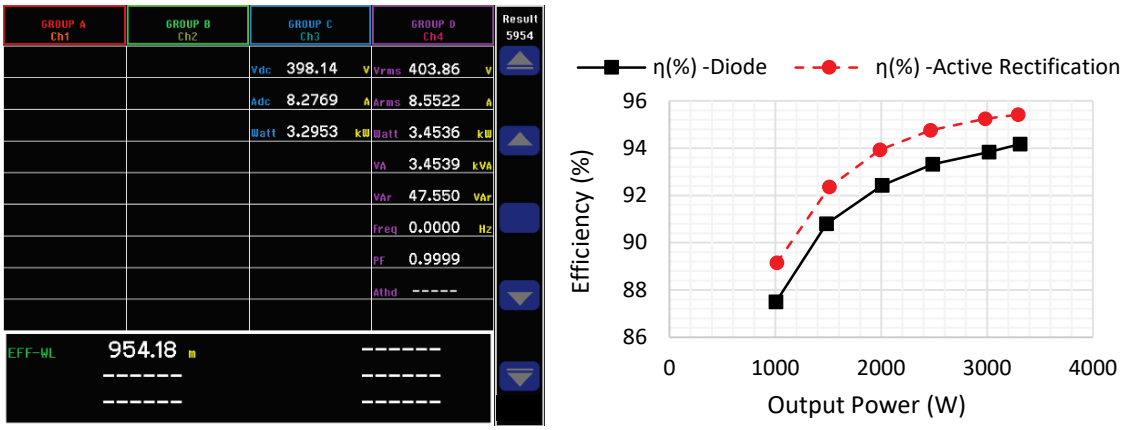


Fig. 5.11 (a) Power analyzer measurements (b) Efficiency comparison between wireless DC-DC stage with diode rectification and proposed active rectification

5.3 Experimental verification of integrated wireless charging solution

Multiple topologies capable of merging wireless rectification stage to on-board chargers were proposed in Chapter 2. From the various proposed solutions, an integrated charging structure based on solution III architecture presented in Fig. 2.10 is selected as the candidate topology to verify the proposed design.

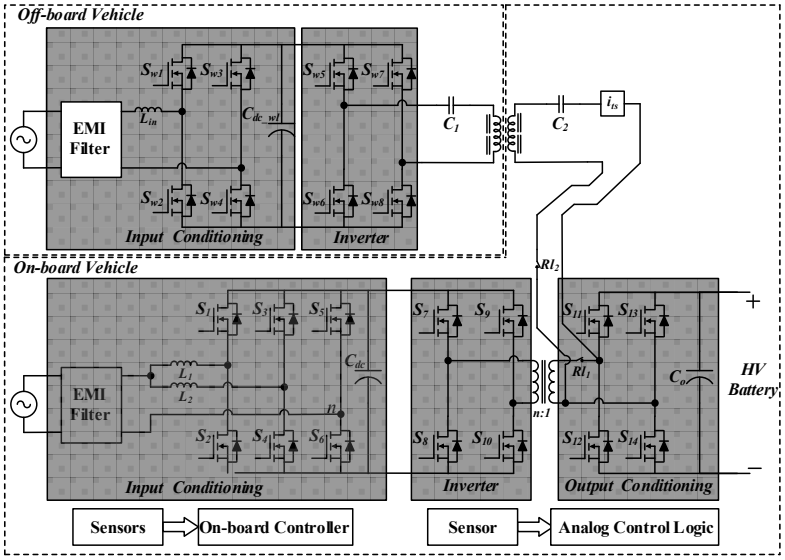


Fig. 5.12 System level implementation of charging solution III

The selected topology is redrawn as Fig. 5.12 for quick reference. The relays Rl_1 and Rl_2 facilitates the integration of inductive and conductive chargers.

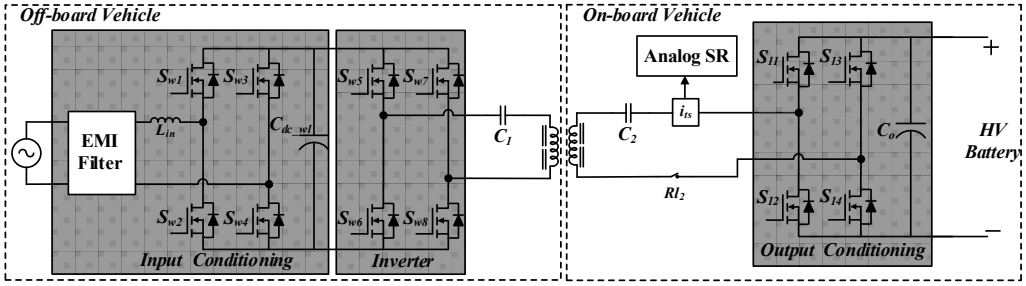


Fig. 5.13 Equivalent circuit of operation for wireless charging mode of solution III

During conductive charging mode the relay Rl_2 remains open while Rl_1 remains closed so as to ensure proper electrical de-energization of the inductive stage. Similarly, under

inductive charging mode system relay Rl_1 remains open while Rl_2 remains closed. The equivalent circuit of the integrated charger under wireless charging mode is presented in Fig. 5.13. A laboratory testing prototype as shown in Fig. 5.14 is assembled to test the proposed charging solution. The key parameters of the prototype under test are summarized in Table 5.4.

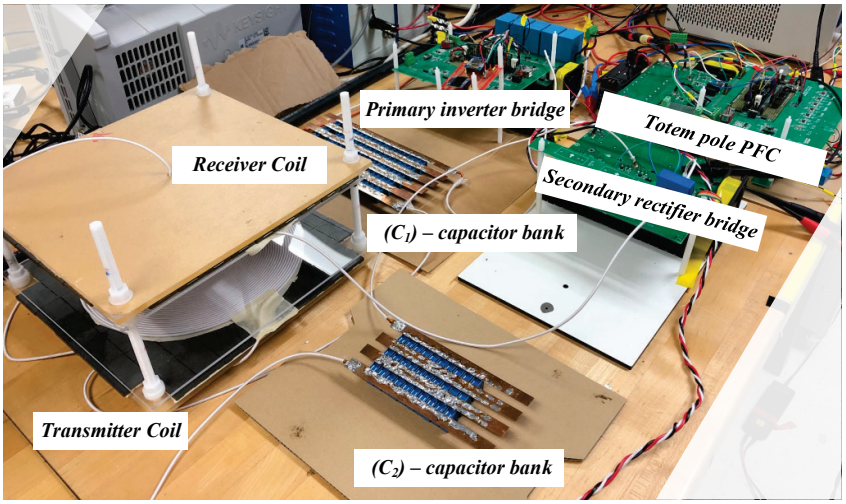


Fig. 5.14 Test setup for verification of integrated charging solution

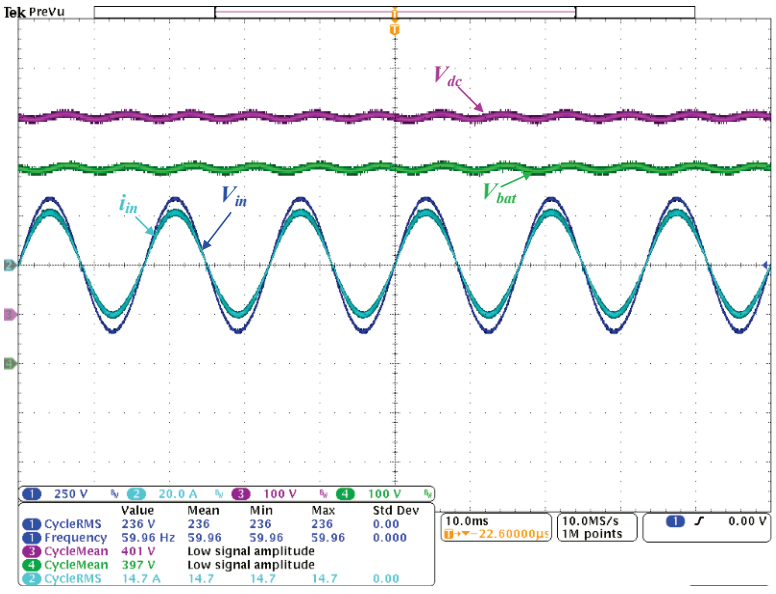


Fig. 5.15 Key operating waveforms of integrated wireless DC-DC stage with OBC

The key operating waveforms of the integrated charger working under full load is presented in Fig. 5.15. The input totem pole PFC stage operates with a switching frequency of 70 kHz to minimize switching loss as well as EMI generation, while wireless power transfer stage is tuned to operate at 85 kHz following SAE J2954 standard. The input voltage and current are in phase with a current THD of 1.3% and less than 1% output voltage ripple at the intermediate link.

Table 5.4 Key parameters of system under test

	Parameters	Part no	Specification
PFC Stage	Nominal Input voltage (Vrms)		240
	Maximum output power (kW)	-	3.3
	Dc Link capacitance	LLG2W681MELC45	680 µF ,450V – 3
	Primary side inductance L_{in} (µH)	-	500
	$S_{w1} - S_{w4}$	C2M00820120D	1200V, 36A, 80mΩ
	Dc link voltage (V)	-	400
Wireless Stage	Output battery voltage range (V)	-	250-420 V
	Resonant Capacitor (C_1)	B32652A2472K000	4.7nF, 2 kV, 5 x17
	Resonant Capacitor (C_s)	B32652A2472K000	4.7nF, 2 kV, 3 x10
	Primary resonant inductance L_{lp} (µH)	-	212.15
	Secondary resonant inductance L_{ls} (µH	-	210.65
	Magnetizing inductance L_m (µH)	-	63.15
	Turns ratio (n)	-	1:1
	Output DC capacitance C_0 (µF)	C4AEHBW5300A3JJ	60
	$S_{w5} - S_{w8}$, $S_{11} - S_{14}$	C2M00820120D	1200V, 36A, 80mΩ

A full load efficiency of 92.77% is obtained for the integrated charging system developed by cascading the totem pole PFC with active rectified wireless DC-DC stage. To

understand the improvement in efficiency over the load range of operation a comparative study is carried out between integrated charger using diode bridge rectification with an integrated solution using active rectification. From, Fig. 5.16 (b) we can observe that the overall efficiency improves by more than 1% for active rectified solution

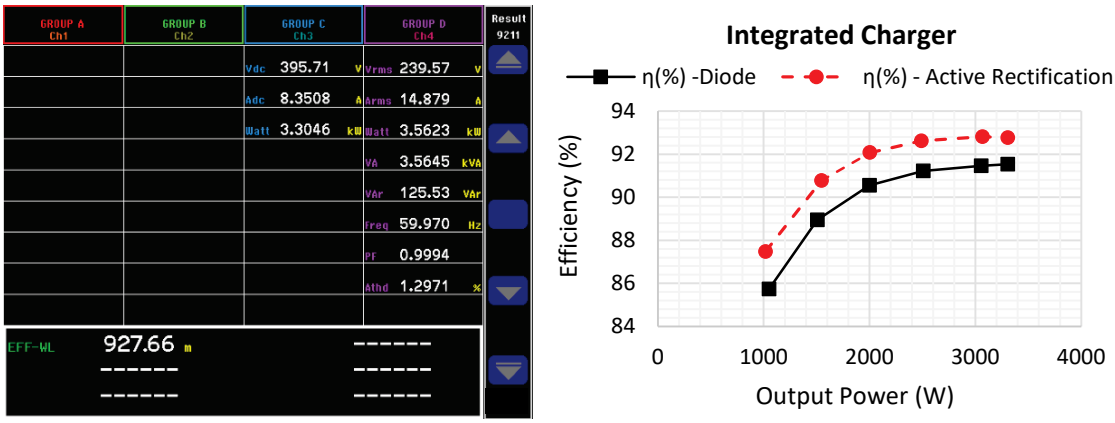


Fig. 5.16 (a) Efficiency measurement from power analyzer (b) Efficiency comparison between integrated charger employing diode rectification with charger employing proposed active rectification

5.4 Summary

In this chapter, an analog synchronous rectification circuit is proposed to implement active rectification on secondary side of the wireless DC-DC stage. The key components enabling the proposed solution are analyzed and designed to develop a laboratory prototype. A full load (3.3kW) efficiency of 95.42% is attained by wireless DC-DC stage employing active rectification which is 1.25% more than diode bridge rectifier based solution. Furthermore, a laboratory prototype of an integrated wireless charger is built employing the proposed active rectification scheme and tested at full load conditions. The laboratory prototype achieves an overall efficiency of 92.77% while drawing an input current with THD of 1.3% from grid.

Chapter 6: Conclusion and Future Research Work

6.1 Conclusions

The major focus of this dissertation work is to propose novel power electronic interfaces to integrate on-board components of wired and wireless charging systems for electric vehicles. Furthermore, the proposed interfaces target minimum modifications to existing components while reducing the weight, cost and volume associated with wireless stage.

In this work, a set of three integration architectures are proposed for wired and wireless charging, classified based on the position of integration. The key requirement of the on-board charger enabling the proposed integration is the presence of a controllable and accessible full bridge.

The proposed architectures require an off-board input conditioning stage converting grid side AC input to DC output for maintaining input power quality. In the initial stage of this work, a comprehensive loss model is developed to evaluate an active front end converter suitable for development of a 3.3kW integrated wireless charging solution. A totem pole bridgeless converter is selected based on the results obtained from the comprehensive loss model.

In the second stage of this work, an improved extended harmonic approximation (EHA) model is proposed to estimate the various characteristics of multi frequency resonant converters. The proposed EHA modeling technique includes the effect of harmonic power which is ignored in case of conventional fundamental harmonic approximation (FHA)

based modeling leading to inaccuracies in gain and stress evaluation. An EHA model based stress evaluation study is carried out for the appropriate design of resonant components.

In order to improve the efficiency of proposed integration structure with minimum modifications, a novel synchronous rectification circuit for on-board full bridge is proposed using secondary side sensed current and low cost opamp based circuits. The proposed circuit can auto synchronize the full bridge structure under a frequency modulation scheme as well generate a programmed phase lead for enabling soft switching operation.

Finally, the proposed integrated wireless charger is implemented using various building blocks developed in this work. The developed laboratory prototype of the integrated wireless charger was able to transfer 3.3kW power from grid to load at an air gap of 10 cm. The implemented charger achieved a conversion efficiency of 92.77% while drawing input current with a power factor of 0.9994 and 1.3% THD.

6.2 Future Work

6.2.1 Secondary side control of series compensated wireless system with reduced communication requirements

The closed loop control scheme for any conventional resonant converter uses the error signal between sensed battery voltage and reference level to generate modulation signals of either the duty ratios or frequency of the primary side switching pulses. However for a wireless charging system, the output voltage sensor circuitry and the PWM controller for the secondary side switches will reside in the vehicle side, whereas the switching controller for the primary side will reside on the charging station side for a wireless converter. Therefore, during this process, it is absolutely necessary to exchange signal information

between the primary and secondary side, which necessitates establishing an additional communication channel. Also, additional considerations need to be taken on the signal propagation delay and synchronizing the processor clocks on both sides. Therefore, a cost-effective and relatively simpler solution would be to conduct the PWM control only on the secondary (vehicle) side without requiring any information from the primary side. The proposed analog synchronization scheme could be extended to act as a potential external trigger for enabling secondary side control for the wireless system. The technical challenge in this regard will be to estimate the voltage/current conditions on the primary side using the secondary side voltage information and, hence, to regulate the power flow and voltage gain. Detailed and rigorous technical analyses on establishing the control loop structure and power flow regulation strategy needs to be investigated and performed in the future research.

6.2.2 Multi-objective optimization of integrated wireless charging system

This work will target for optimized designs at component level for the proposed integrated wired and wireless charging system, which comprises of a power factor correction (PFC) rectifier followed by the wireless DC/DC stage. Based on the selected power conversion stages in a wireless power transfer system and design space parameters, the resulting current and voltage waveform expressions need to be developed for each component, which are then used to optimize the EMI filter, wireless coil and capacitor banks in the compensation network. The proposed extended harmonic analysis (EHA) model can improve the accuracy of stress calculations of various resonant components.

In the Pareto optimization, all available degrees of freedom, i.e. all design space variables (passive component values, DC link voltage, inner and outer diameters of the coil, ferrite

plate dimensions, and shield dimensions) are considered. Then each component is optimized independently with an iterative temperature/loss calculation, in order to take the temperature dependent losses into account.

For the design of the coil, the quality factor and leakage flux parameters are the major constraints. The figure of merit (FOM) of a wireless coil is given by $FOM = kQ$ where k stands for the coupling while Q stand for quality factor. To design a high quality wireless coil we need to maximize the FOM. The k and Q values of a coil are dependent on the inner and outer diameters as well the construction of field shaping ferrite back plates. ANSYS Maxwell FEA based simulations have to be employed to extract an optimum design for given power and dimension constraint while maximizing FOM of the coil.

The optimization of the resonant capacitor bank in the wireless stage is very important to maximize efficiency. Applying statistical trend on the database of film, ceramic, and aluminum capacitors from TDK, EPCOS, and Dublier shows that the volume of the capacitor can be expressed as a linear combination of stored energy, capacitance and voltage i.e. $Vol_{cap} = k_{C1}CV_c^2 + k_{C2}C + k_{C3}V_c$. The proportional coefficients k_{C1}, k_{C2}, k_{C3} vary for different types of capacitors. An extensive database of various types of capacitors with their voltage ratings needs to be formed in a future study for making the optimum selection. Furthermore, after calculating the quasi peak noise spectrum, the optimal EMI output filter is found by searching through all LC parameters that do not violate the power quality constraints and yield to the minimum passive volume.

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