Nanotechnology

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To cite this article before publication: Mircea L Dragoman *et al* 2019 *Nanotechnology* in press https://doi.org/10.1088/1361-6528/ab4832

RECONFIGURABLE HORIZONTAL-VERTICAL CARRIER TRANSPORT IN GRAPHENE/HfZrO FIELD-EFFECT TRANSISTORS

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Abstract

We have fabricated at wafer level field-effect-transistors (FETs) having as channel graphene monolayers transferred on a HfZrO ferroelectric, grown by atomic layer deposition on a doped Si (100) substrate. These FETs display either horizontal or vertical carrier transport behavior, depending on the applied gate polarity. In one polarity, the FETs behave as a graphene FET where the transport is horizontal between two contacts (drain and grounded source) and is modulated by a back-gate. Changing the polarity, the transport is vertical between the drain and the back-gate and, irrespective of the metallic contact type, Ti/Au or Cr/Au, the source-drain bias modulates the height of the potential barrier between HfZrO and the doped Si substrate, the carrier transport being described by a Schottky mechanism at high gate voltages and by a space-charge limited mechanism at low gate voltages. Vertical transport is required by three-dimensional integration technologies for increasing the density of transistors on chip.

1. Introduction

Reconfigurable nanoelectronic devices have emerged recently in the context of atomically thin materials or 2D materials. Several nanoelectronic device functionalities, which are normally performed by different devices, could be produced in a single, reconfigurable device, via electrostatic doping, i.e. a single or several gate voltages determine the carrier type (*n* or *p*) and the corresponding densities, replacing chemical doping. It is worth mentioning that, although electrostatic doping is not a technique exclusively used for 2D materials without (as graphene) or with bandgap (as transition metal dichalcogenides), in the case of 2D materials it is very often the only option for doping.

For example, in graphene, the carrier type is selected by a gate voltage that shifts the Fermi level above or below the Dirac point, where the density of carriers is zero, inducing *n* or *p* doping [1], whereas electrostatic doped contacts can be used also to implement *n* and *p* MOSFETs in a single device with an on/off ratio of 10^4 and black phosphorus as channel [2]. The same concept, with buried electrode to reconfigure a field-effect transistor (FET) as an *n* or *p* transistor, was used in the case of FETs based on a monolayer WSe_2 channel [3]. A similar reconfigurable FET, with buried electrode and a WSe_2 channel, was shown to function as either one of three fundamental devices: *p-n* diode, MOSFET or bipolar junction transistor [4].

Electrostatic doping is used not only to implement several devices in a single one, but also to obtain multiple circuits functionalities in a single device. In particular, graphene barristors have demonstrated reconfigurable logic gates [5], while OR, XOR or majority gates were implemented using a single field-effect device electrostatically doped by various metallic gates [6]. Moreover, reconfigurable microwave switches and resonators were demonstrated based on the metal-semiconductor transition in MoS_2 monolayers induced by a DC voltage [7, 8], whereas gated metal-insulator transition in $MoTe_2$ was proven experimentally recently [9]. In addition, electrostatic doping could be used in a large range of devices that are not based on 2D materials, such as Schottky barrier MOSFETs, reconfigurable FETs based on nanowires, carbon nanotubes,

or tunneling FETs, providing a very good control on carrier concentration profiles [10]. For instance, single-walled carbon nanotubes connected by two metallic electrodes in a buried gate configuration work as either a *p-n* diode or as ambipolar FET, depending on the applied gate voltages [11].

Reconfigurable nanoelectronic devices based on atomically thin materials could have a very important role in future architecture electronics, since the implementation of multiple functionalities in a single device could reduce drastically the dimensions of circuits, being thus an enhancement of Moore's law, based on CMOS transistors, as it reaches its limits. In this respect, our paper describes a FET which is able to reconfigure into a horizontal or vertical FET depending on the gate voltage. The transistor, consisting of a *p*-Si substrate, which plays the role of a backgate G, on which a thin layer of HfZrO is grown, on top of which a graphene monolayer is deposited and source S and drain D electrical contacts are patterned, changes not only the direction of current flow but also the charge carrier source and transport mechanisms as the gate voltage polarity is changed. Moreover, the ability to work in a vertical transport regime is of particular interest for three-dimensional integration of nanoelectronic devices – a technology that promises a significant increase in the density of transistors on chip [12].

2. Operation principle and fabrication of the reconfigurable graphene/HfZrO transistor

A schematic diagram of the device is represented in Fig. 1, which indicates also the two possible current flow directions in the three-terminal device (see red arrows in the left side figures). The band diagrams in both cases are displayed for $V_D = 0$ and $V_G = 0$. Irrespective of the voltage values on the *p*-Si contact, there is a horizontal current flow, as represented in Fig. 1(a). In the band diagram in Fig. 1(a), ϕ_m denotes the workfunction of metal M from which the S and D electrodes are fabricated. On the other hand, there is a possibility for vertical current flow between *p*-Si and the drain D contact because the HfZrO layer is very thin, the structure being equivalent to a metal-insulator-semiconducting configuration with well-known rectification

characteristics. Therefore vertical transport occurs only for positive voltages applied on the *p*-Si contact. The relevant band diagram in this case is represented in Fig. 1(b) for $V_D = 0$ and $V_G = 0$.

As a consequence, when the gate voltage V_G applied on the *p*-Si substrate is negative, the device behaves as a usual graphene FET (the vertical current flow being disabled), the current measured between the S and D electrodes (the drain current I_D) flowing in the horizontal direction and being channelled by graphene, HfZrO playing the role of the gate dielectric. In this case *p*-Si, and the S and D electrodes fulfil their expected roles, these roles being indicated in the parentheses. As V_G increases in absolute value (becomes more negative), the Fermi level in graphene moves in the direction indicated by the arrow at right.

However, if the voltage applied on *p*-Si is positive, the two current paths mentioned above are both enabled, but the vertical current is dominant since the charge carrier concentration in p-Si is much larger than in graphene. As a result, the overall direction of current flow becomes vertical, the charge carriers collected by the drain electrode originating mainly from *p*-Si. Thus, *p*-Si becomes the effective S electrode, fact that is suggested by the parentheses in Fig. 1(b), left. These positive charges have to overcome the potential barrier between *p*-Si and HfZrO before traversing the graphene layer and being collected by the D electrode. Although apparently the device should transform into a diode, the third electrode is able to modulate the current between *p*-Si and S, and hence the former S electrode plays the role of gate (role that is indicated in the parenthesis). To understand this modulation effect, it should be noted that the ultrathin HfZrO layer becomes polarized by the proximity with the doped Si layer and graphene, which is equivalent to the application of a weak electric field on the ferroelectric material. As V_D (the voltage between S and D electrodes) increases towards positive values the equivalent electric field on HfZrO decreases (dashed red lines in the figure at right as response to the shift of the Fermi level in graphene represented by the arrow) and the barrier height seen by charge carriers from *p*-Si increases. As a result, the current collected by the D electrode decreases.

The considerations above indicate that the three-terminal device proposed in this paper is a transistor in the sense that the voltage applied on one terminal modulates the current flowing through the other two terminals. However, it is not a typical FET because the role of source and gate electrodes changes with the polarity applied on p-Si.

The graphene/HfZrO transistors were fabricated following several steps. In the first step, 6 nm of $Hf_xZr_{1-x}O_2$ thin film was grown on a 4 inch *p*-doped Si (100) wafer by the atomic layer deposition (ALD) method. Further, a high-quality CVD-grown monolayer of graphene (Graphenea, https://www.graphenea.com) was transferred on $Hf_xZr_{1-x}O_2$ over the entire wafer.

The wafer was cut in two chips, one being used for graphene/ferroelectric memories [13] and the other for the present study. Therefore, details regarding the ALD growth method and the structural characterization of $Hf_xZr_{1-x}O_2$ are found in [13] and the accompanying supporting information. Before graphene transfer, a detailed structural analysis was performed for $Hf_xZr_{1-x}O_2$. X-ray photoelectron spectroscopy (XPS) analysis dedicated to find the precise chemical composition of $Hf_xZr_{1-x}O_2$ indicated that $x = 0.45$, so that the HfZrO thin film that we refer to is in fact $Hf_{0.45}Zr_{0.55}O_2$. The thickness of HfZrO, measured by spectroscopic ellipsometry, is 5.8±0.2 nm using an optical model reported before [14, 15]. GIXRD patterns for HfZrO revealed the occurrence of the $HfO_2(ZrO_2)$ orthorhombic phase, with Pbc21 symmetry. Extensive PFM (Piezoelectric Force Microscopy) analysis was carried out to establish the ferroelectricity of the samples, while Raman spectroscopy confirmed the quality of the graphene monolayer, by showing only the 2D and G peaks with a ratio > 1.9 over 80% of the wafer area; further details are given in [13] and the corresponding supporting information.

The graphene channels were patterned in a bow-tie shape by e-beam, using a RAITH e-Line, and then etched by RIE in oxygen plasma (equipment: SENTECH Etchlab 200) (see Fig. 2(a)). Two types of graphene/HfZrO FETs metallic electrodes for source S and drain D were then patterned on top of the graphene channel: Cr (5 nm)/Au (100 nm) and Ti (5 nm)/Au (100 nm), with dimensions of 150 μm ×150 μm. The S and D electrodes were patterned by e-beam

lithography and deposited by an e-beam Temescal FC200 evaporation system. Figure 2(b) shows the optical image of the chip containing graphene/HfZrO FETs at right and the SEM of one fabricated device at left. The FETs had channel lengths of L = 400 nm and widths of W = 300 nm for both types of contacts. 50 FETs were fabricated on a single chip of graphene/HfZrO/Si, 25 FETs for each type of contacts.

As mentioned before, we investigated the effect of two types of contacts: Ti/Au and Cr/Au on the device operation. The reason of studying these two types of contacts is that they are among the most common used contacts and because their contact resistivity in graphene-based devices is quite different [16]. As such, devices with these two types of contacts could have dissimilar characteristics, since graphene plays a major role, being either channel or modulating the HfZrO barrier.

3. Electrical characterization of the device and discussions

The electrical characterization of graphene/HfZrO FETs was performed using a Keithley SCS 4200 station, all three channels being equipped with low noise amplifiers and connected to a probe station enclosed in a Faraday cage, where all on-chip measurements were carried out. We have measured all 50 transistors on the chip, and found that 6 did not work because the metallic contacts were exfoliated during measurements. We have not used any fitting algorithms during or after measurements, and all measurements were double-swept at various sweeping rates to guarantee the accuracy of measurements.

Typical drain current I_D versus gate voltage V_G characteristics for different drain voltage V_D values indicated in the legend for graphene/HfZrO FETs with Ti-Au contacts are shown in Fig. 3(a). One can observe from this figure a linear I_D–V_G region for large drain voltages, with small current values at negative V_G (detailed also in the inset), and a non-linear I_D–V_G region, with large current values and hysteretic behavior, for positive gate voltages. These two behaviors can be attributed to the horizontal and vertical transport regimes, respectively, corresponding to

the situations where the charge carriers are transported by the graphene channel (characterized by a relatively small density of states) between source and drain and, respectively, flow between the gate electrode and drain, through the doped silicon/HfZrO interface. The transition between these two transport regimes is illustrated by the humps in the I_D current in the inset for small positive V_G values. Although the I_D–V_G dependence in the inset seems to be linear, so that the graphene FET does not go in an off state, a closer examination of the inset for low V_D values show (see Fig. 3(b), where only the graphene FET behavior/negative V_G region is of interest) that in this case the characteristics are non-linear and that there is at least a two-orders-of-magnitude variation in the drain current when the gate voltage is swept from near 0 to -20 V. This suggests that there is a small ferroelectric-induced bandgap, of about 180 meV, which, however, can easily be overcome for drain voltages of a few volts. This finding is similar to theoretical predictions of bandgap opening in bilayer graphene when transferred on a ferroelectric layer and is attributed to the spontaneous polarization field of the ferroelectric [17]. Note that the almost constant I_D value in Fig. 3(b) for V_D = 2 V and small positive values of V_G corresponds to the humps in the I_D current in the inset in Fig. 3(a) mentioned before, and indicates a transition region between horizontal and vertical transport regimes.

Moreover, we have recently performed atomistic simulation regarding graphene/HfZrO and we have observed the occurrence of an induced bandgap by the ferroelectric HfZrO due to orbital hybridization and locally deformed graphene structure [18]. The bandgap of 0.18 eV is very near to the theoretical value of 0.25 eV for atomistic strictures formed by graphene/HfZrO and terminated with Hf atoms. This fact is of outmost importance since only haexagonal boron nitride (h-BN) is known to induce a bandgap in graphene. However, h-BN is difficult to be grown at the wafer level for graphene logical applications, while HfZrO can be grown on Si wafers of any size.

Another observation that can be made from Fig. 3(a) is that, whether the gate voltage modulates the charge density in the graphene channel (for negative V_G values/positive I_D), as

expected, in the vertical transport regime (for positive V_G values/negative I_D), the V_D bias seems to shift the gate voltage value at which the current starts to increase/takes negative values. This shift is almost linear in V_D, with a slope of 1.74, as can be seen from Fig. 3(c). The third observation is that, in the vertical transport regime, where V_G plays the role of the drain voltage, the charge transport mechanism seems to change with V_D, from a hysteresis-free, abrupt variation for V_D = 0, to a slower variation, associated to a significant hysteresis for large V_D values.

Based on the considerations above, we investigated the transport mechanism at V_D = 0 V and 6 V, respectively. In the first case, a double-logarithmic I_D–V_G dependence, shown in the inset of Fig. 4(a), revealed a $I_D = V_G^{\alpha}$ dependence with α = 4 for low V_G values and α = 1.4 for high gate voltages. The first case is consistent with a space charge limited current mechanism, in which the negatively-charged traps/residual impurities related to the hydroxyl groups in the interfacial layer that forms between HfZrO and the Si substrate during ALD deposition [19, 20], enhance the applied electric field. On the other hand, Fig. 4(a) shows that at high V_G values the transport mechanism is consistent with Schottky emission, the experimental data fitting well the relation :

$$I_D \propto \exp\left[-\frac{e\left(\phi_B - \sqrt{eE/4\pi\varepsilon}\right)}{k_B T}\right] \quad (1)$$

where ϕ_B is the barrier height, E the applied electric field (proportional to V_G), ε the permittivity of the material, k_B the Boltzmann constant and T the room temperature. As suggested by Fig. 3(b), the height of ϕ_B is modulated by the drain voltage. The slope of the $\ln(I_D)$–$(V_G)^{1/2}$ dependence is about 0.66, as can be seen from Fig. 4(a), from which the relative permittivity of HfZrO is found to be about 28 taking into account the potential drops on Si and the ferroelectric

layer with a thickness of 6 nm. This value of the relative permittivity of HfZrO is in very good agreement with that in Ref. [21].

A similar ln(I_D)–ln($V_{G,sh}$) dependence for V_D = 6 V, where $V_{G,sh}$ is the (shifted) V_G value measured from the gate voltage at which I_D = 0 (see the shift of V_G with V_D discussed above), shows that for all V_G values the α exponent in $I_D = V_G^{\alpha}$ is almost equal to or higher than 2, indicating again a space charge limited current mechanism. Note that as V_D increases, the effective barrier height at the Si/HfZrO interface also increases, as can be seen from the decrease in the I_D value. Thus, for large V_D values the traps in the interfacial layer between HfZrO and the Si dominate the charge transport, a fact supported also by the appearance of hysteretic behavior, illustrated in Figs. 3(a) and 4(b).

Figure 5 depicts the gate voltage dependence of the parameter $g_m = \Delta I_D / \Delta V_G$ in the graphene/HfZrO FET with Ti-Au contacts discussed previously. In the horizontal transport regime g_m is identical to the transconductance of the FET, while in the vertical transport regime it should be identified with the conductance of the device, since in this case the role of gate and drain contacts interchange. However, as can be seen from this figure, g_m takes values higher than 3 mS, which shows that the current can be significantly modulated by changing V_G.

Typical I_D–V_G dependences for different drain voltage values in the legend for graphene/HfZrO FETs with Cr-Au contacts are shown in Fig. 6(a), the inset illustrating a detail of these dependencies for the horizontal transport regime, through the graphene channel, case in which the current takes positive values. Neither in this regime, nor in the vertical transport regime, for which I_D is negative, are the characteristics linear, but the hysteretic behavior observed in the vertical transport regime in FETs with Ti-Au contacts is barely observable. Although the I_D–V_G characteristics are nonlinear for negative V_G voltages, the graphene/HfZrO FET seems not to go into an off state for high V_D values, as for the case of FETs with Ti-Au contacts. However, a logarithmic dependence of the curves in the inset of Fig. 6(a) for small drain voltages, shown in Fig. 6(b), indicate again a strong variation of current between on and off

states, of at least three orders of magnitude, when V_G sweeps between positive and negative values. This current variation is larger than for the devices with Ti-Au contacts, suggesting that a higher ferroelectric-induced bandgap opens in this case, of about 180 meV.

In addition, in comparison to the FETs with Ti-Au contacts, the current at $V_D = 0$ is smaller, but can be enhanced significantly at negative V_D values, this parameter modulating again the effective barrier at the Si/HfZrO interface. The shift of the gate voltage at which the sign of the current changes with V_D is illustrated in Fig. 6(c). At negative V_D values this shift could be fitted by a linear dependence with a slope of 0.95, while at positive V_D values the slope of the linear fit changes to 2.3. All these findings suggest that the unavoidable trap distributions at the ferroelectric/contact interface are different in the two situations studied in this paper.

To identify the conduction mechanism in FETs with Cr-Au contacts in the vertical transport regime, we have once again plotted the $\ln(I_D)$–$\ln(V_G)$ dependence for $V_D = 0$ (low current, slower I_D variation with V_G) and, respectively, the $\ln(I_D)$–$\ln(V_{G,sh})$ characteristic for V_D = -12 V (high current, rapid I_D variation with V_G). The corresponding results are illustrated in Figs. 7(a) and (b). In the first case, at low V_G values, the experimental data can be fitted by a $I_D = V_G^{\alpha}$ dependence, with α = 3.8, which suggests a space charge limited current mechanism, the same mechanism being also responsible for charge transport at high V_G values, where α = 1.8. The latest value is close to 2, i.e. to the Child's square law dependence. The fit in the inset of Fig. 7(a) supports this transport mechanism. However, when V_G decreases, the $\ln(I_D)$–$\ln(V_{G,sh})$ curve suggests a space charge limited transport at low gate voltages (α = 2.76, as can be seen from the inset in Fig. 7(b)), but at high voltages the current can again be fitted with a Schottky emission law, as shown in Fig. 7(b). What is remarkable is that the slope of the dependence $\ln(I_D) = f(V_G^{1/2})$, i.e. 0.64, is very close to the 0.66 value found for FETs with Ti-Au contacts. This fact supports the identification of Schottky emission as the dominant mechanism in the low-potential-barrier at the Si/HfZrO interface regime, because the obtained relative permittivity of

the ferroelectric is comparable in the two situations. In this case the value of this parameter is about 31. The potential barrier at the Si/HfZrO interface is modulated by V_D.

The possibility of modulating the current via the gate voltage, expressed by the g_m parameter, is illustrated in Fig. 8, g_m taking again values up to 3 mS. The same considerations related to the interpretation of this parameter as for FETs with Ti-Au contacts hold also in this case.

4. Conclusions

We have demonstrated a CMOS-technology compatible graphene/HfZrO FET fabricated at wafer level where the transport or carriers is either horizontal, at negative gate voltages between drain-source, or vertical via HfZrO/Si interface at positive gate voltages. Thus, the direction of the transport is controlled by the polarity of the gate voltage. In addition, the value of the current differs significantly for the two gate polarities, emphasizing the change of the source of charge carriers.

In the horizontal transport regime, we have found that the ferroelectric layer induces a small bandgap in the device channel, the magnitude of which depends on the contacts. This bandgap is apparent for transport at low drain voltages and induces an on/off current ratio of at least two orders of magnitude for FETs with Ti-Au contacts and at least three orders of magnitudes for FETs with Cr-Au contacts.

In the vertical transport, at high voltages the current can be fitted with a Schottky emission, while at low-voltages we have a space charge limited current, and traps are dominating the transport. We have found that the trap distribution depends on the interface ferroelectric/contacts, being different for Ti/Au and Cr/Au contacts on HfZrO, contacts which have a different resistivity in graphene-based devices.

In conclusion, the reconfigurable graphene/HfZrO FET is able to change the transport direction from vertical to horizontal via a change in the gate polarity, which makes it among the

first devices able to work in either a two-dimensional or a three-dimensional nanoelectronic architecture, essential for high-density electronics. In addition, our results have emphasized the fact that, although the conduction mechanisms are the same, irrespective of the metal contact type, different contacts influence significantly the performance of the reconfigurable graphene/HfZrO FETs.

Some of the authors (MD, MA, AD and DD) acknowledge the financial support of project number PN-III-P4-ID-PCCF-2016-0033.

Acknowledgments.

The authors would like to thanks Prof. Marco Farina, Dr. Andreea Di Donato and Dr. Eleonora Pavoni from Università Politecnica delle Marche, Ancona, Italy for performing the Piezoresponse Force Microscopy measurements on our samples. Some of the authors (MD, AD and DD) acknowledge the financial support of project number PN-III-P4-ID-PCCF-2016-0033.

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Figure captions

Fig. 1 Schematic configuration of the device and relevant band diagrams for the (a) horizontal, and (b) vertical transport regimes for V_D = 0 and V_G = 0. The red lines in the figures at left indicate the direction of current flow.

Fig. 2 (a) Graphene monolayer channel cut in a bowtie shape. (b) Optical image of the chip containing graphene/HfZrO FETs (right) and SEM of one FET (left), showing the graphene channel between S and D.

Fig. 3 (a) I_D–V_G dependences in graphene/HfZrO FETs with Ti-Au contacts, for different V_D values shown in the legend. Inset: detail for positive I_D values. (b) Logarithmic scale representation for the detail in (a) for small drain voltages. (c) V_D dependence of the shift of V_G values for which I_D = 0 for the same FETs.

Fig. 4 Fittings of the I_D– V_G dependences in Fig. 3(a) for negative I_D values for (a) V_D = 0 and (b) V_D = 6 V

Fig. 5 Gate voltage dependence of g_m for graphene/HfZrO FETs with Ti-Au contacts

Fig. 6 (a) I_D–V_G dependences in graphene/HfZrO FETs with Cr-Au contacts, for different V_D values shown in the legend. Inset: detail for positive I_D values. (b) Logarithmic scale representation for the detail in (a) for small drain voltages. (c) V_D dependence of the shift of V_G values for which I_D = 0 for the same FETs.

Fig. 7 Fittings of the I_D– V_G dependences in Fig. 6(a) for negative I_D values for (a) V_D = 0 and (b) V_D = -12 V

Fig. 8 Gate voltage dependence of g_m for graphene/HfZrO FETs with Cr-Au contacts

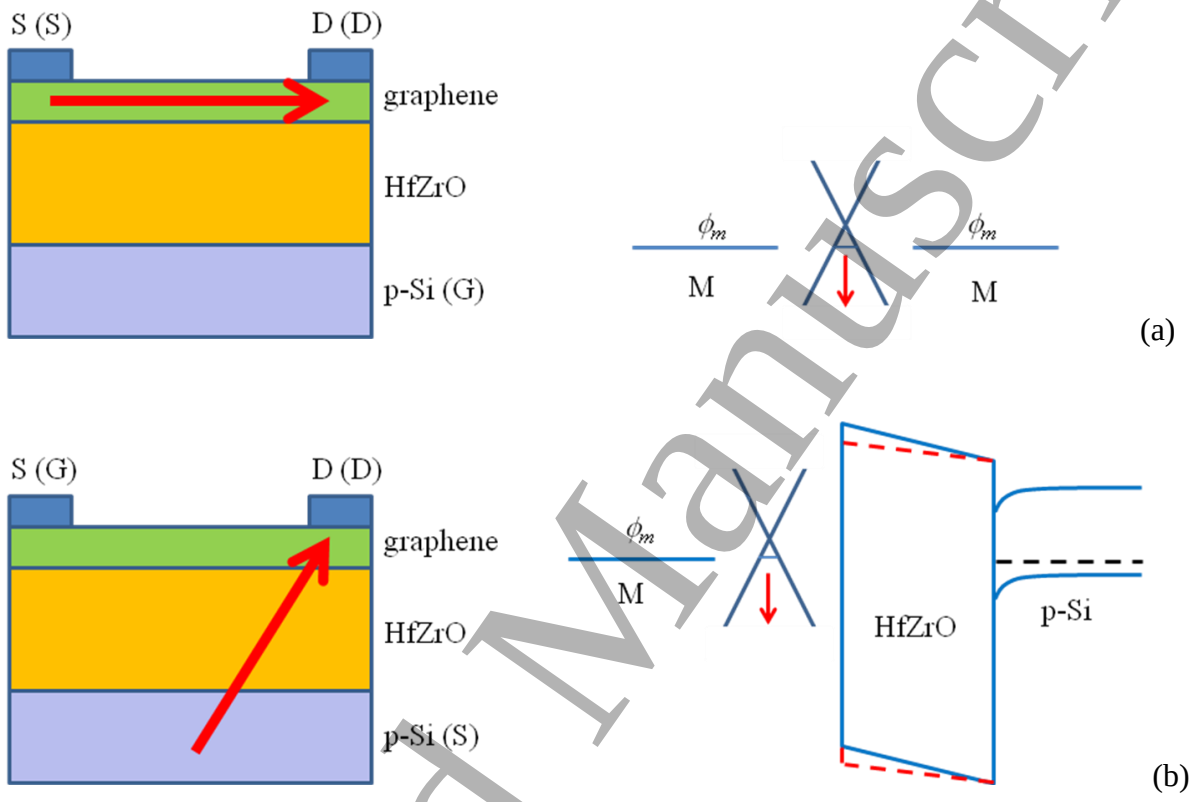
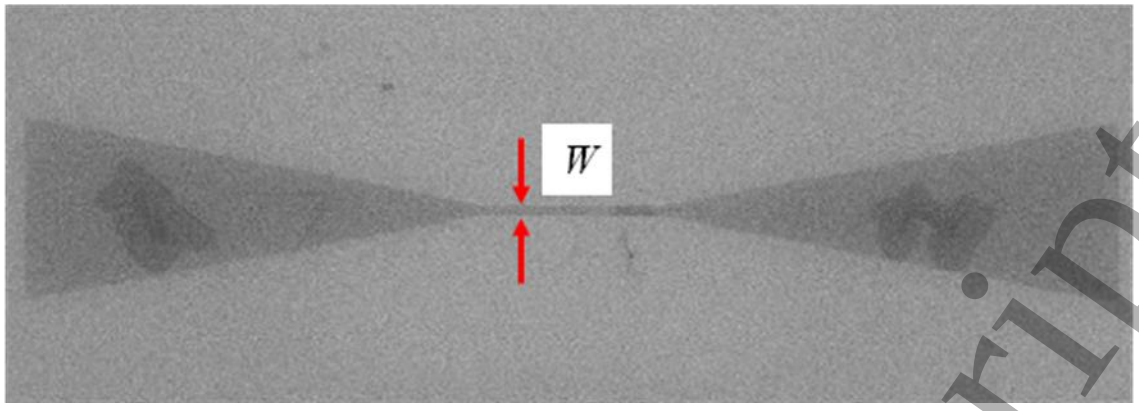
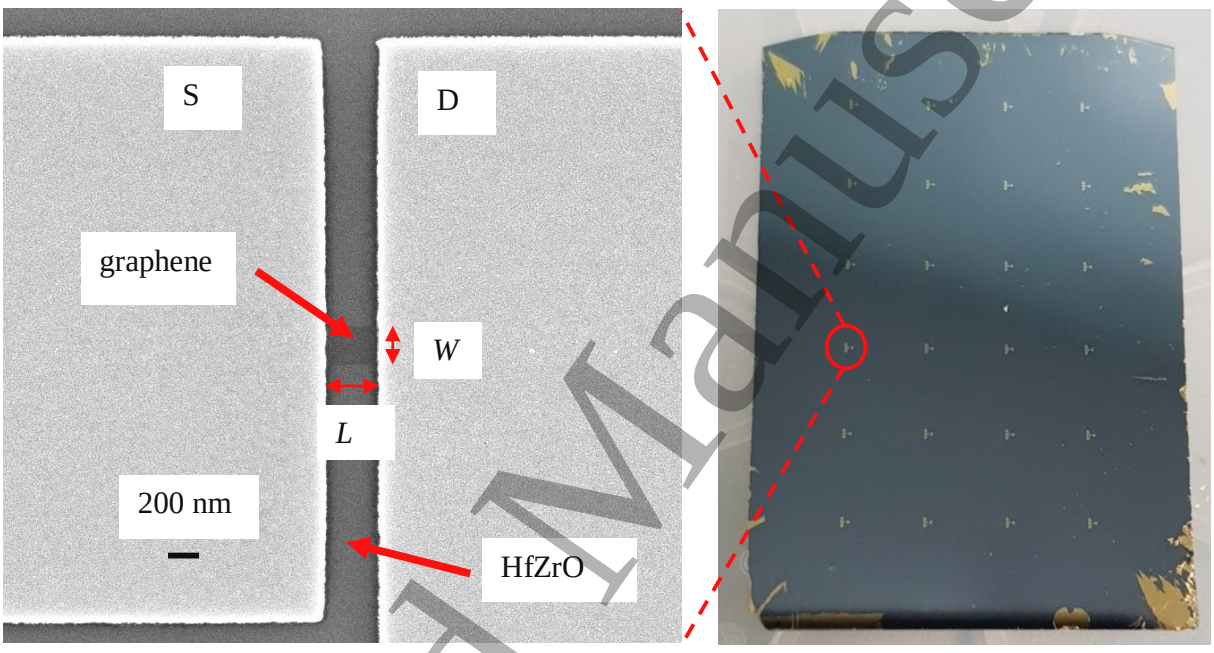


Fig. 1

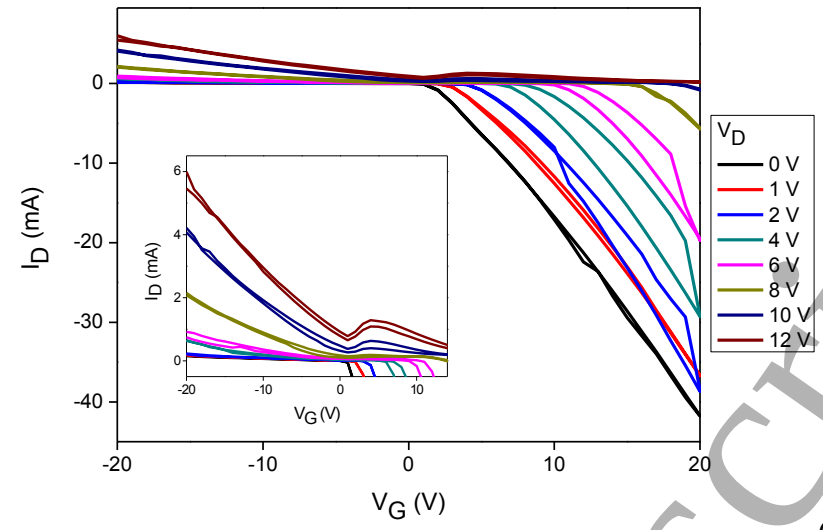


(a)

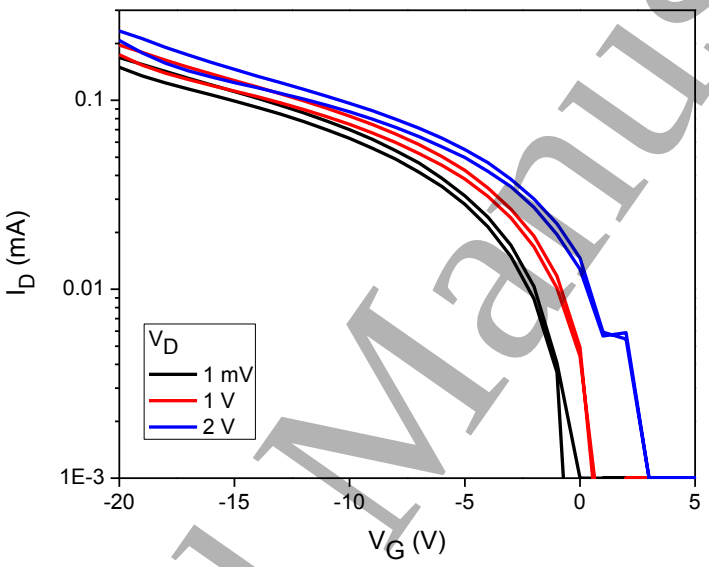


(b)

Fig. 2



(a)



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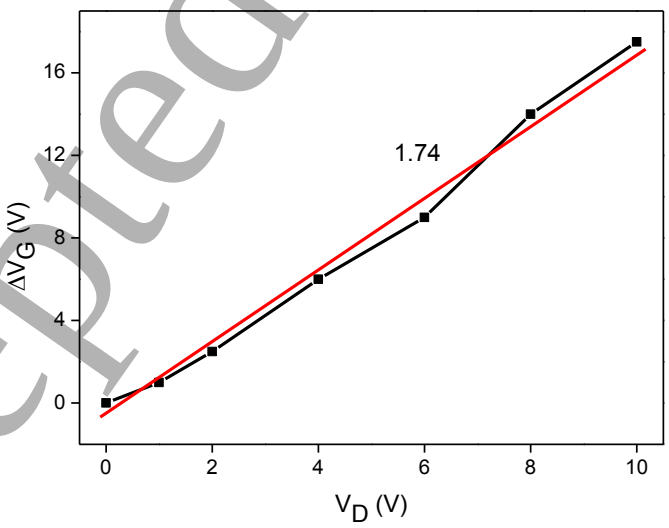
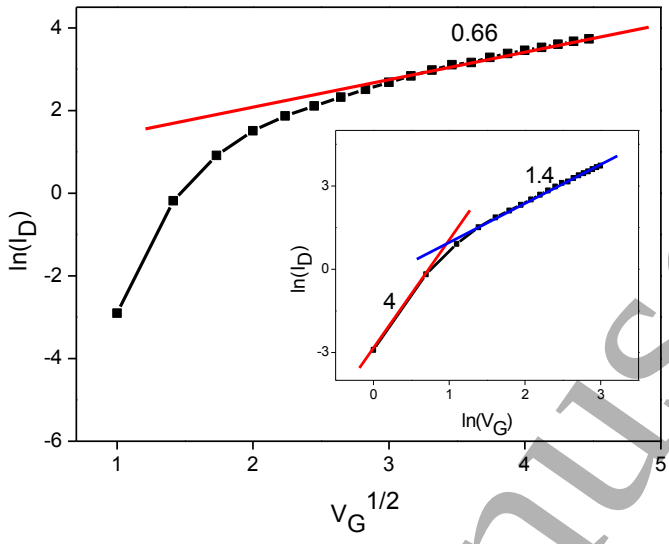
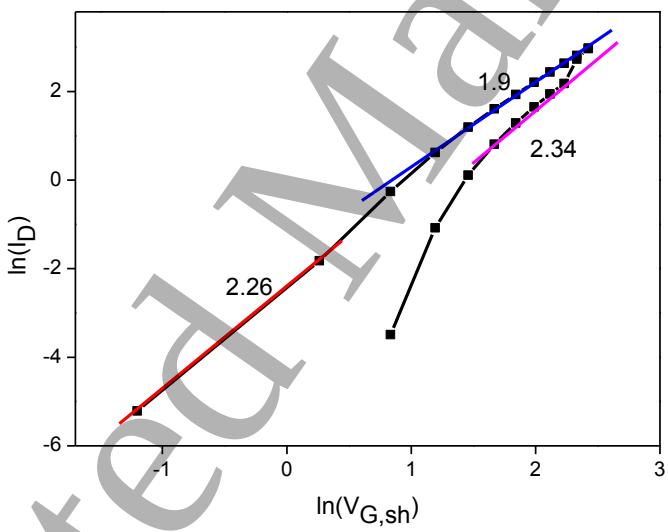


(c)

Fig. 3



(a)



(b)

Fig. 4

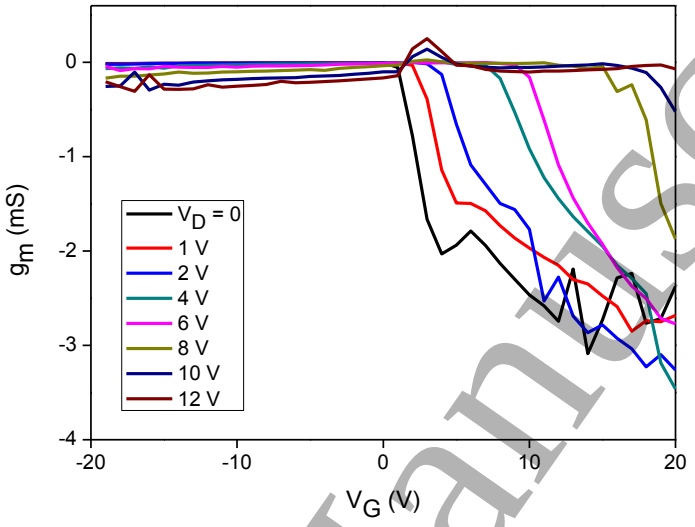
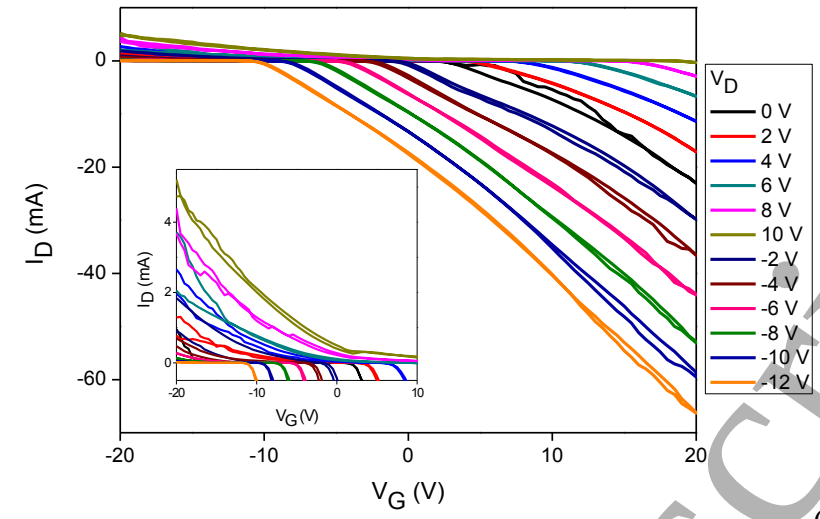
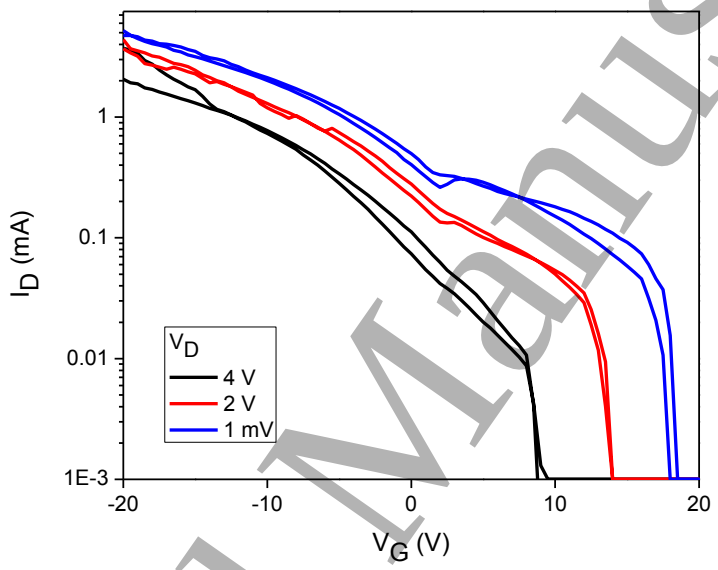


Fig. 5



(a)



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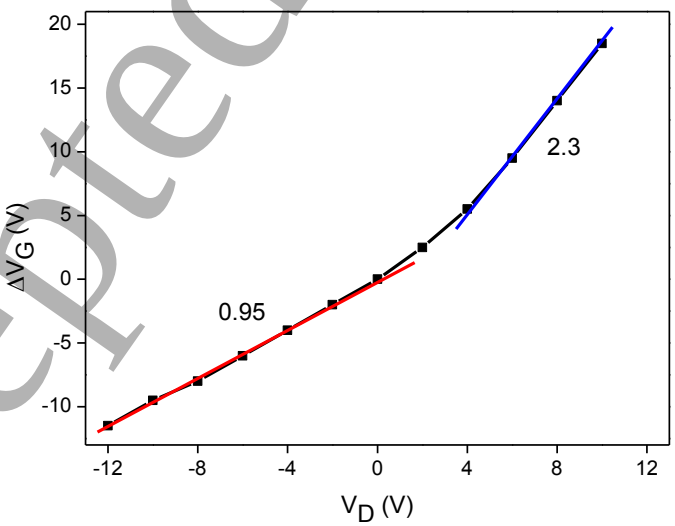
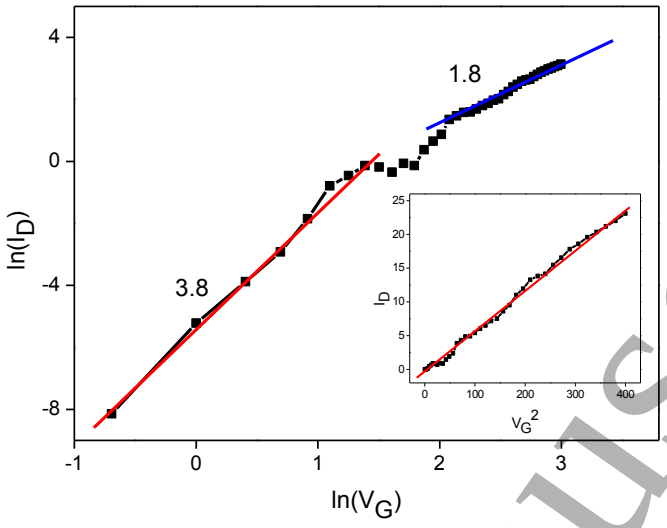
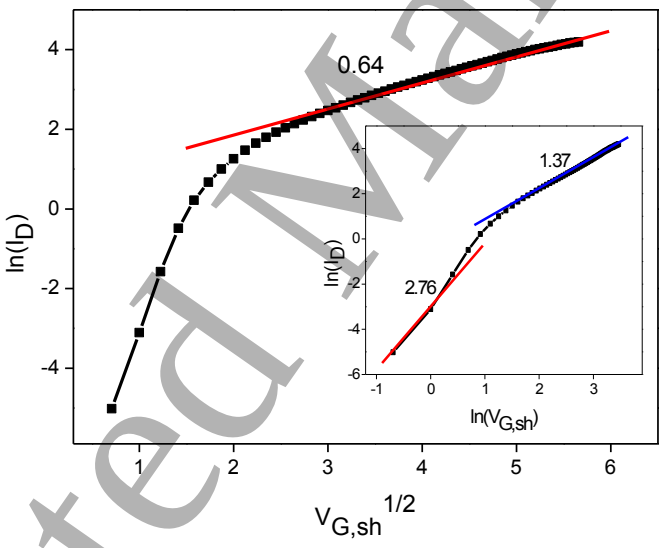


(c)

Fig. 6



(a)



(b)

Fig. 7

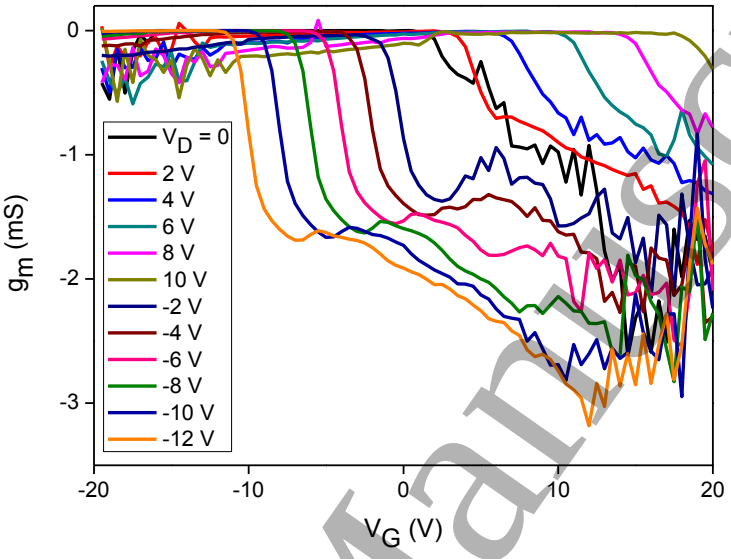


Fig. 8