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DESIGN FOR TESTABILITY METHOD AT REGISTER TRANSFER LEVEL

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A thesis submitted in fulfilment of the
requirements for the award of the degree of
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To my beloved family.

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ABSTRACT

The testing of sequential circuit is more complex compared to combinational circuit because it needs a sequence of vectors to detect a fault. Its test cost increases with the complexity of the sequential circuit-under-test (CUT). Thus, design for testability (DFT) concept has been introduced to reduce testing complexity, as well as to improve testing effectiveness and efficiency. Scan technique is one of the mostly used DFT method. However, it has cost overhead in terms of area due to the number of added multiplexers for each flip-flop, and test application time due to shifting of test patterns. This research is motivated to introduce non-scan DFT method at register transfer level (RTL) in order to reduce test cost. DFT at RTL level is done based on functional information of the CUT and the connectivity of CUT registers. The process of chaining a register to another register is more effective in terms of area overhead and test application time. The first contribution of this work is the introduction of a non-scan DFT method at the RTL level that considers the information of controllability and observability of CUT that can be extracted from RTL description. It has been proven through simulation that the proposed method has higher fault coverage of around 90%, shorter test application time, shorter test generation time and 10% reduction in area overhead compared to other methods in literature for most benchmark circuits. The second contribution of this work is the introduction of built-in self-test (BIST) method at the RTL level which uses multiple input signature registers (MISRs) as BIST components instead of concurrent built-in logic block observers (CBILBOs). The selection of MISR as test register is based on extended minimum feedback vertex set algorithm. This new BIST method results in lower area overhead by about 32.9% and achieves similar higher fault coverage compared to concurrent BIST method. The introduction of non-scan DFT at the RTL level is done before logic synthesis process. Thus, the testability violations can be fixed without repeating the logic synthesis process during DFT insertion at the RTL level.

ABSTRAK

Pengujian litar jujukan lebih kompleks berbanding litar gabungan kerana ia memerlukan jujukan corak ujian untuk mengesan kerosakan di dalam litar jujukan. Kos pengujiannya meningkat dengan kerumitan litar-bawah-pengujian (CUT) jujukan. Oleh itu, konsep rekabentuk untuk pengujian telah diperkenalkan untuk mengurangkan kerumitan pengujian dan juga untuk memperbaiki keberkesanan dan kecekapan pengujian. Teknik pengimbas adalah satu kaedah rekabentuk untuk kebolehujian yang selalu digunakan. Walau bagaimanapun, ia mempunyai overhed kos dari segi kawasan kerana bilangan tambahan pemultipleks untuk setiap flip-flop, dan penggunaan masa ujian yang disebabkan oleh penganjakan corak ujian. Motivasi kajian ini memperkenalkan kaedah rekabentuk untuk kebolehujian bukan pengimbas di aras pindahan daftar (RTL) untuk tujuan mengurangkan kos pengujian. Rekabentuk untuk kebolehujian di aras RTL dilakukan berdasarkan maklumat fungsi CUT dan kaitan penyambungan CUT di antara daftar. Proses perantaian daripada satu daftar kepada daftar lain lebih berkesan dari segi overhed kawasan dan penggunaan masa ujian. Sumbangan pertama kerja ini ialah pengenalan kaedah rekabentuk untuk kebolehujian tanpa-pengimbas di aras RTL yang mempertimbangkan maklumat keboleh kawalan dan keperhatian terhadap CUT yang boleh diekstrak daripada huraian RTL. Ia telah dibuktikan melalui keputusan simulasi yang kaedah ini mempunyai liputan kerosakan yang lebih tinggi, sekitar 90%, penggunaan masa ujian yang lebih rendah, penjanaan masa ujian yang lebih rendah dan pengurangan 10% terhadap overhed kawasan berbanding dengan kaedah lain di literatur kebanyakan litar tanda aras. Sumbangan kedua kerja ini ialah pengenalan kaedah ujian-sendiri terbina-dalam di aras RTL yang menggunakan daftar tandatangan berbilang input sebagai komponen ujian-sendiri terbina-dalam dan bukannya pemerhati blok logik terbina-dalam serempak. Pemilihan daftar tandatangan berbilang input sebagai daftar ujian berdasarkan algoritma set bucu minimum lanjutan. Kaedah baru ujian-sendiri terbina-dalam ini menghasilkan overhed kawasan yang lebih rendah sebanyak 32.9% dan mencapai liputan kerosakan yang lebih tinggi berbanding dengan kaedah ujian-sendiri-terbina-dalam serempak. Pengenalan rekabentuk untuk kebolehujian tanpa-pengimbas di aras RTL dilakukan sebelum proses sintesis logik. Oleh itu, perlanggaran kebolehujian boleh diperbaiki tanpa mengulangi proses sintesis logik semasa penambahan rekabentuk untuk kebolehujian di aras RTL.

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LIST OF ABBREVIATIONS

AO	-	Area Overhead
ATE	-	Automatic Test Equipment
ATPG	-	Automatic Test Pattern Generation
BIST	-	Built-In Self-Test
CBILBO	-	Concurrent Built-In Logic Block Observer
CLB	-	Combinational Logic Block
CUT	-	Circuit-Under-Test
DFT	-	Design for Testability
FF	-	Flip-Flop
IC	-	Integrated Circuit
ITC	-	International Test Conference
LFSR	-	Linear Feedback Shift Register
LBIST	-	Logic Built-In Self-Test
MUX	-	Multiplexer
MFVS	-	Minimum Feedback Vertex Set
PI	-	Primary Input
PO	-	Primary Output
RA	-	Response Analyser
RTL	-	Register Transfer Level
SFF	-	Scan Flip-Flops
TC	-	Test Control
TEM	-	Time Expansion Model
TTL	-	Transistor-Transistor Logic
TPG	-	Test Pattern Generator
VHDL	-	Very High Speed Integrated Circuit HDL
VLSI	-	Very Large Scale Integration

XOR - Exclusive-OR

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LIST OF SYMBOLS

X_0 - Inputs of LFSR

Z_{0-3} - Outputs of LFSR

Q_{0-3} - State of LFSR

$\wedge$ - AND logic operation

$\vee$ - OR logic operation

$\neg$ - NOT logic operation

$=$ - Equal

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CHAPTER 1

INTRODUCTION

1.1 Background

Nowadays, an integrated circuit (IC) can simply have millions of gates and thus, its design becomes more complex. According to Moore's Law, the number of components per chip doubles roughly every 24 months. Design performance has improved following Moore's Law but testing suffers from tremendous pressure to keep up with the new semiconductor technology without impacting the design and production costs. Figure 1.1 depicts the manufacturing test is performed on chips before delivering to customers. Prior to that, test development is accomplished to obtain test data to be used in manufacturing test, such as test patterns and expected test responses. IC testing is an important step to identify the correctness of manufactured circuits. Furthermore, testing is definitely essential to ensure high yield of good quality product. Fault coverage is an indicator of testing quality. High fault coverage obtained using standard commercial automatic test pattern generator (ATPG) is important because the test vectors could filter out most of the defective IC. However, it is difficult to achieve high fault coverage in some sequential circuits. In order to obtain high fault coverage that becomes a major concern in testing, design for testability (DFT) is introduced.

DFT refers to a method that augments a given circuit to become easily testable. In other words, DFT is used to improve the testability of the circuit. Basically, four parameters are needed to be measured when introducing DFT: (1) fault coverage, (2) test generation time, (3) test application time and (4) area overhead. Among these four parameters, although area overhead is incurred, DFT improves fault coverage, test application time and test generation time.

Fault coverage is the ratio of the number of faults detected to the total number of faults. Fault coverage is measured using fault model such as stuck-at fault, stuck-at-open, path delay and bridging fault. Stuck-at-fault model is the most common model in logic circuits (Adallatif, 2009). Equation 1.1 shows the fault coverage measurement.

$$\text{Fault coverage} = \frac{\text{detected fault}}{\text{total faults}} \tag{1.1}$$

Test generation time is the computation time needed to generate test patterns. Normally, test generation time for sequential circuit is longer than that of combinational circuit. This is because of the feedback path in the sequential circuit. Test application time is the total time required to apply test patterns on the circuit-under-test (CUT) and capture its test responses. Test application time of circuits augmented by DFT method called partial scan (Cheng and Agrarwal, 1990) is shorter than the full scan design because the length of the scan chain is reduced in the former. Another parameter, area overhead, is defined as the ratio of extra gates added to the total number of original circuit gates. For example, extra multiplexers are considered as area over when they are added to the CUT under partial scan method to improve the testability of the CUT. Therefore, the area of multiplexers are considered as extra area that needs to be calculated.

Since the trend of top-down design has become more popular, process of introducing DFT is also moved from gate level to RTL aiming at further improving the test generation time and area overhead. DFT method can be categorised into scan, non-scan and BIST. Each category can be applied at both RTL and gate level except full scan method that included is applied at gate level only. DFT at RTL is applied in early design before generating netlist process (Greene and Samiha, 2002).

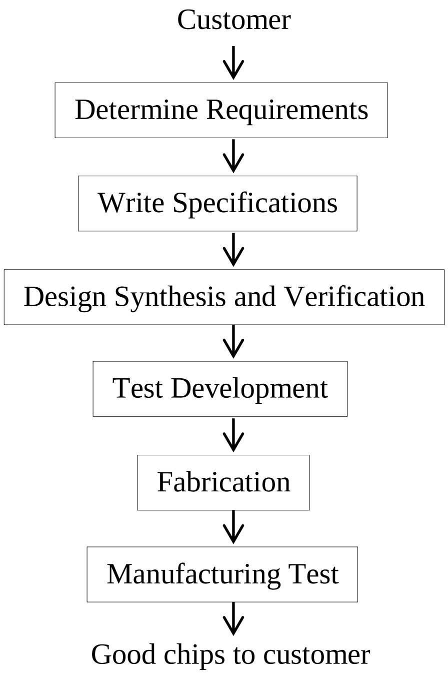
Customer
Determine Requirements
Write Specifications
Design Synthesis and Verification
Test Development
Fabrication
Manufacturing Test
Good chips to customer

Figure 1.1 Testing flow in VLSI realization process (Bushnell and Agrawal, 2002)

1.2 Problem Statement

Sequential circuit consists of combinational logic and flip-flops. Different from combinational circuit which needs only a single test vector to detect a fault, the testing of sequential circuit is more complex because it needs a sequence of vectors to detect a fault in a sequential circuit. The sequence of vectors is generated by initializing a circuit to a known state, activate the fault and propagate the fault to a primary output. Its test cost will be increased accordingly due to the complexity of testing sequential circuit. Therefore, DFT concept has been introduced to reduce the testing complexity, as well as to improve testing effectiveness which is always measured by test application time, fault coverage and test generation time. DFT of scan technique such as full scan and partial scan [16] is one of the popular methods. However, it has limitations of area overhead due to number of added multiplexer at each flip-flop and test application time due to shifting of test pattern.

Based on the problems discussed above, two research questions are raised: (1) Can the area overhead of DFT be further reduced? (2) Can the test application time of DFT be further shortened? To answer the questions, first, the root cause of each problem should be identified and discussed. Area overhead is the first issue need to be addressed. Area overhead is incurred due to the addition of multiplexers into selected flip-flop to enhance the controllability and observability of the storage element such as flip-flop in scan technique. When the DFT is done at gate level, the addition of multiplexer is merely determined by the structural information such as feedback loop of the sequential circuit. This can be avoided if functional information at the RTL design of the CUT is known during DFT. High area overhead will be incurred if extra sequential circuit, known as test plan, is added between controller and data path like approach by Ohtake, Wada, Masuzawa and Fujiwara (2000). Test plan is required to generate test patterns to data path. They also insert multiplexer if necessary during generation of control path and observation path.

The second issue addressed is test application time. Chaining a scan flip-flop to another scan flip-flop based on only structural information is the main factor that leads to the long test application time. If functional information such as registers' connectivity is known during DFT, chaining a register to another register more effectively in term of area overhead and test application time is possible and this allows RTL non-scan DFT that generally has shorter test application time.

However, RTL non-scan DFT method still requires expensive automatic test equipment (ATE) to provide external test patterns and to observe the test responses. Besides ATE cost incurred from basic components in tester such as probe card and interface card, ATE cost also includes yearly maintenance cost. Furthermore, high performance ATE is essential especially testing of timing defects. On contrary, the built-in self-test (BIST) method does not require external test patterns. It can generate the test patterns by itself through the test pattern generator integrated into the circuit. However, the BIST approach suffered from the area overhead if using concurrent built in logic block observer (CBILBO) as test register which can operates as test pattern generator and test response compacter. The BIST approach also has drawback of long test application time based on test-per-scan scheme because each test pattern needs to be scanned in and scanned out through the register.

The main challenge of DFT insertion is how to reduce test cost by obtaining high fault coverage with an acceptably less test application time, test generation time and low area overhead without incurring unacceptably low fault coverage. In other words, fault coverage is a more crucial parameter need to be considered compared to area overhead, test application time and test generation time. However, there is a trade-off between fault coverage and test application time and between fault coverage and area overhead. It is also possible to obtain high fault coverage and low area overhead and short test application time.

1.3 Objectives

The objectives of this research are:

1. To develop a RTL non-scan DFT method that has high fault coverage, low area overhead, low test application time and low test generation time.
2. To develop a RTL BIST method that has high fault coverage and low area overhead.

1.4 Scope of Work

The scope of the research covers the following:

a) Focus on introducing non-scan RTL DFT method.
b) RTL design that written in VHDL description.
c) ITC’99 circuits and RTL design circuit like greatest common division (GCD) is used as benchmark circuits to show the effectiveness of the proposed method.
d) Stuck-at-fault model is used as fault model.

e) The tools like Altera Quartus, Design Vision, Tetramax, VHDL and Perl script are used in this research.
f) This research considers functional test; parametric test is out of scope of this work.

1.5 Contributions

This thesis has two main contributions. The first contribution is the introduction of a non-scan DFT method at RTL that considers the information of controllability and observability of CUT that is extractable from RTL description. The information at RTL is extracted in order to reduce the extra hardware such as multiplexers to make the CUT easily tested. Therefore, the area overhead of the proposed non-scan RTL DFT can be reduced. High fault coverage, less test application time and less test generation time are achieved compared to the previous method.

The second contribution is the introduction of BIST technique at RTL, which is using multiple input signature register (MISR) as BIST component instead of CBILBO. The BIST component selection is based on the new concept of extended minimum feedback vertex set (extended MFVS), where a number of registers is selected to be BIST component such that minimum cost function of hardware overhead is considered. MISR can still generate test patterns and compact test responses simultaneously similar to CBILBO. By using MISR, definitely area overhead can be reduced. All combinational blocks are tested simultaneously such that the test application time is short. This new BIST method results in lower area overhead and slightly lower fault coverage compared to the concurrent BIST-able method for all the benchmark circuits.

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