INTERCONNECTION AND DAMPING ASSIGNMENT PASSIVITY-BASED CONTROLLER FOR MULTILEVEL INVERTER

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To my lovely mother, who gave me endless love, trust, constant encouragement over the years, and for her prayers.

To my husband, kids, my mother in law and siblings, for their patience, support, love, and for enduring the ups and downs during the completion of this thesis.

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ABSTRACT

This thesis proposes an Interconnection and Damping Assignment Passivity-Based Controller (IDA-PBC) to control a 5-level Cascaded H-Bridge Multilevel Inverter (CHMI). The proposed IDA-PBC uses the Port-Controlled Hamiltonian (PCH) theory to modify the CHMI system energy by adding damping, thereby modifying dissipation structures related to dynamics and stability. The objective is to maintain output voltage regulation, resulting in fast response and low Total Harmonic Distortion (THD) values. Although the proposed IDA-PBC control algorithm showed outstanding performance during transient and nonlinear load condition, further improvements are required during no-load condition. To address this, improvements in the form of modification to the proposed IDA-PBC algorithm was made by adding a single loop Proportional-Integral (PI) controller at the voltage side, which was aimed at regulating the voltage before it was fed back into the IDA-PBC. In order to verify the viability of the proposed IDA-PBC-PI controller for the CHMI, a simulation study was conducted using MATLAB/Simulink at a 20 kHz switching frequency and 1 µs sample time. The controller was tested at five load conditions, namely, steady state, no-load to full-load, load uncertainty, structural uncertainty and nonlinear load condition. The performance of the proposed controller showed regulated output voltage while maintaining THD values below 5% in all load conditions and a maximum of 220 µs response time during load uncertainty. The simulation results revealed the superiority of the proposed controller compared to the conventional double loop PI controller and the conventional IDA-PBC in terms of transient response, THD value, as well as regulation of the output voltage. The feasibility of the proposed IDA-PBC-PI controller was validated by developing its proof-of-concept hardware prototype. The simulation and experimental results obtained based on a 3 kHz switching frequency and 38 µs sample time were found to be consistent, which confirmed the capability of the proposed controller in controlling the 5-level CHMI output voltage.

ABSTRAK

Tesis ini mengusulkan Penetapan Terhadap Sambungan dan Redaman bagi Pengawal yang Berasaskan Konsep Pasif (IDA-PBC) untuk mengawal 5-aras Penyongsang Jejambat-H Pelbagai Aras (CHMI). IDA-PBC yang diusulkan menggunakan teori Kawalan-Port Hamiltonian (PCH) untuk mengubah suai tenaga CHMI dengan menambah redaman dan mengubah suai struktur pelesapan yang berkaitan dengan dinamik dan kestabilan. Objektif kawalan adalah untuk mengekalkan aturan voltan keluaran, serta menghasilkan masa tindak balas yang cepat dan Jumlah Gangguan Harmonik (THD) yang rendah. Walaupun algoritma kawalan IDA-PBC yang diusulkan menunjukkan prestasi cemerlang semasa keadaan peralihan dan beban yang tidak linear, penambahbaikan diperlukan semasa keadaan ketiadaan beban. Oleh itu, pengubahsuaian kepada algoritma IDA-PBC yang diusulkan telah dilaksanakan dengan menambah kawalan Berkadar-Kamiran (PI) pada bahagian voltan, untuk mengawal selia voltan sebelum ia disuap-balik ke dalam IDA-PBC. Bagi mengesahkan kebolehupayaan kawalan ini, kajian simulasi dijalankan menggunakan MATLAB/Simulink pada frekuensi pensuisan 20 kHz dan 1 µs sampel masa. Pengawal ini diuji pada lima keadaan beban iaitu pada keadaan tetap, tiada beban kepada beban penuh, beban yang tidak menentu, ketidakpastian struktur dan beban yang tidak linear. Prestasi pengawal yang diusulkan menunjukkan voltan keluaran adalah teratur selain mengekalkan nilai THD bawah 5% dan masa tindak balas maksimum sehingga 220 µs. Keputusan simulasi mendedahkan keunggulan pengawal yang dicadangkan berbanding pengawal PI dua gegelung konvensional dan pengawal IDA-PBC konvensional dari segi masa tindakbalas, nilai THD serta aturan voltan keluaran. Semua pelaksanaan pengawal IDA-PBC-PI yang dicadangkan telah disahkan dengan membangunkan perkakasan prototaip berdasarkan konsep-pembuktian. Keputusan simulasi dan eksperimen yang diperolehi berdasarkan frekuensi pensuisan 3 kHz dan 38 µs sampel masa adalah didapati konsisten, yang mengesahkan keupayaan pengawal yang dicadangkan dalam mengawal voltan keluaran bagi 5-aras CHMI.

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LIST OF ABBREVIATIONS

| А | - | Ampere |
|----------------|---|--|
| A _c | - | Amplitude of the carrier signal |
| A_m | - | Amplitude of the modulating signal |
| A/D | - | Analog/Digital |
| CHMI | - | Cascaded H-bridge Multilevel Inverter |
| CPU | - | Central Processing Unit |
| DC | - | Direct Current |
| DSP | - | Digital Signal Processor |
| EMI | - | Electromagnetic Interference |
| EV | - | Electric Vehicle |
| FFT | - | Fast Fourier Transform |
| FPGA | - | Field-Programmable Gate Array |
| I/O | - | Input/Output |
| IGBT | - | Insulated-Gate Bipolar Transistor |
| kHz | - | kilo Hertz |
| m | - | Number of staircase level |
| m_a | - | Amplitude modulation ratio |
| MLI | - | Multilevel Inverter |
| Ν | - | Harmonic order |
| PS-PWM | - | Phase-shift Pulse Width Modulation |
| PV | - | Photovoltaic |
| PWM | - | Pulse Width Modulation |
| r1, r2 | - | Random number in a range of 0 to 1 |
| n | - | Number of single phase full bridge inverters |
| THD | - | Total Harmonic Distortion |
| V | - | Volt |
| Var | - | Volt amperes reactive |
| VDC1 | - | DC supply module 1 |
| VDC2 | - | DC supply module 2 |

| Vc | - | Capacitor output voltage of CHMI |
|----|---|----------------------------------|
| W | - | Watt |
| μs | - | micro seconds |
| θ | - | Angle |

CHAPTER 1

INTRODUCTION

1.1 Introduction

The rapid evolving industry in recent years has demanded higher power equipment which now reaches up to Megawatt level. These high power applications need to be connected to medium-voltage power electronics devices. In order to cater the demand, multilevel inverter has been introduced [1]. Multilevel inverters are built by a row of power semiconductors and voltage sources. This inverter structure is able to create staircase sinusoidal like voltages. The required output voltage of the inverter can be obtained by summing up the total of the DC voltage sources. This structure allows the multilevel inverter to produce higher output voltage, with less voltage for each semiconductor device to withstand. Thus, multilevel inverter structure increases the capability of the power converters to operate in mediumvoltage grid.

Since its introduction in 1981 [1], its amazing and interesting properties in medium and high power application has attracted a large interest among researchers. This includes its capability to operate in higher voltage operation with low switching losses and reduced harmonics [2], [3]. As compared to conventional inverters, multilevel inverters are also preferred due to the low voltage stress on the power

switches where lower $\frac{dv}{dt}$ is applied to the components since the voltages are divided into smaller values to perform the switching [4]. This cost-effective solution not only enables the inverters to meet high power ratings, but also capable to operate in low power operations such as in renewable energy application [5]–[7]. Other applications include tractions [8], [9], active power filtering [4], [10], VAR compensation [11], flexible AC transmission system [12] and induction motor drives [13].

Providing a clean and stable sinusoidal output voltage regardless of any perturbations is the main requirement of a well-designed multilevel inverter. It is also important to ensure that the multilevel inverter can provide fast transient recovery time caused by load uncertainties or disturbances. Moreover, in the case of the presence of a non-linear load, the multilevel inverter will produce a highly distorted load current and in return will cause deterioration in the output voltage quality. The severe effects of the current and voltage distortion in power system quality have been reported in various cases [14], [15]. Thus, it is very important to maintain a regulated output voltage with fast transient response and low Total Harmonic Distortion (THD) of below 5% [16]. In order to achieve these, a reliable closed-loop control scheme is needed.

There are two main approaches of ensuring output regulation of a multilevel inverter which are; linear or nonlinear strategies. One of the most frequently applied linear controllers is the Proportional Integral (PI) controller of which control objective is to regulate the output signals and reduce the steady state error to zero [17]. Although offering the advantage of constant switching frequency, this controller, however, is very sensitive to perturbations and variations of a system's parameters. Since the mathematical model of the inverter itself is nonlinear, it is strongly agreed that a nonlinear control strategy from the nonlinear structure of the system will lead to better achievement in terms of performance. An example of a commonly used nonlinear approach is determining the inverter switching by using hysteresis comparator. This method has been proven to achieve a good dynamic response in multilevel inverter applications [18], [19]. However, the variable switching frequency has become a major drawback of this approach.

Another nonlinear controller that has gained researcher's interest in recent years is a method based on energy function shaping known as Passivity-based Controller (PBC). The growing interest in PBC implementation in power electronics devices [20]–[22] has resulted in a very successful development of the so-called Interconnection and Damping Assignment PBC (IDA-PBC). This controller produces a closed-loop system based on Hamiltonian structure. In this structure, the closed-loop energy is required to have a minimum desired equilibrium point to assure its stability. The main advantage of the IDA-PBC algorithm is that the Lyapunov function is obtained naturally by the dynamic structure of the system itself, leading to the desired operating point, rather than imposing external dynamics which conventional controllers mostly do. The IDA-PBC has proven to be useful and efficient to meet regulatory objectives in various applications [22]–[25].

1.2 Problem Statement

The nonlinear nature of the multilevel inverters' nonlinear equations is caused by the multiplication of the state variables by the control inputs. Traditional linear control methods as presented in [17], [27] often neglect the nonlinear characteristics of the multilevel inverter and physical characteristics of the LC filter. This in turn, leads to instability problems on the power converter system. In comparison to the linear controller, nonlinear controllers deal with a wider class of systems that are nonlinear, time-variant or both. It is generally applied to real-world systems that are often governed by nonlinear equations [28]. The nonlinear control systems can be classified into two major groups which are non-model based and model based. Non-model based controllers do not consider essential information of the system parameters and hence no mathematical model for the controller is needed. The controllers are more robust than their model based counterparts. An example of a non-model based controller in the market is Fuzzy Logic Controllers (FLC) [29]. This technique is useful to approximate a system because the fuzzy sets boundaries can be unclear or indefinite due to the gradual transition between membership and non-membership [30]. In CHMI, FLC has been applied successfully in improving power quality by minimizing the harmonics in the output voltage waveform [31]–[33]. However, these non-model based controllers are lacking in standard design guidelines and are normally designed in heuristic manners. Their performances are quite unpredictable and are generally difficult to optimize [34].

On the other hand, model-based controllers require a precise mathematical model of the multilevel inverter in order to design the controller's algorithm. Its design procedure is systematically structured and is widely accepted by the control system community [35]. A common design environment provided in a model-based controller design enhances general communications between the elements of power systems, provide easier data analysis and allow system verification. The impact of the controller's design and modification in terms of time and cost can be reduced by synthesizing and troubleshooting the errors in the system as early as possible. It is also easier to reuse or upgrade the existing developed system especially for a system with expanded capabilities.

1.3 Thesis Objective

This thesis proposes a model-based nonlinear controller which is a modified IDA-PBC for the control of a Cascaded H-bridge Multilevel Inverter (CHMI). This structured controller model enhances the stability and dynamical performance of the CHMI by adding damping elements and modifying the dissipation structure. The proposed modified IDA-PBC in this thesis improves the transient stability of power systems by proposing a new solution of the matching partial derivative equation through the desired interconnection matrix. The new matrix function for the interconnection and damping matrices shows outstanding performance during transient response and during the presence of a nonlinear load. However, in order to improve the performance of the controller during transition from no load to full load condition, and vice versa, a complementary PI controller is proposed to be added to the voltage part of the controller. This controller is referred to as the IDA-PBC-PI controller which is able to minimize the steady-state error between the actual output voltage with the equilibrium point before it is injected back into the IDA-PBC system. This results in the improvement of the inverter's performance especially during the transition from no load to full load. This controller is able to maintain output voltage regulation with fast transient response while maintaining low THD value with various load conditions. This thesis critically looks into the aspect of the design, analysis, implementation and performance evaluation of both the IDA-PBC and IDA-PBC-PI controllers. The objectives of this thesis are:

- 1. To study the multilevel inverter concept, topologies and control methods that has been implemented as well as the concept and types of Passivity-Based Controllers (PBC).
- To implement through simulation and experimental work the concept of Interconnection and Damping Assignment Passivity-Based Controller (IDA-PBC) on Cascaded H-bridge Multilevel Inverters (CHMI).

 To develop the related IDA-PBC mathematical model, design procedures and control performance evaluation in terms of output voltage regulation and transient response while maintaining the acceptable range of Total Harmonic Distortion (THD) percentage.

1.4 Thesis Scope

The thesis covers the development of the mathematical model and implementation of both the proposed IDA-PBC and IDA-PBC-PI controllers for a 5level CHMI. Performance evaluation of the controllers is based on maintaining output voltage regulation with fast transient response and low THD under various loading conditions. The performance is verified through both simulation and experimental work of the proposed controllers for the 5-level CHMI.

1.5 Thesis Contribution

In implementing the concept of IDA-PBC as applied to a 5-level CHMI, the following contributions are attained:

• Two new matching equations of damping and injection matrices have been proposed in the controller's algorithm. These equations are obtained by solving the Partial Differential Equation (PDE) derived from the structure of the 5-level CHMI. These two matrices are developed by following propositions that are subjected to the IDA-PBC control law.

 A new IDA-PBC-PI controller to improve the overall CHMI output voltage performance during no load condition. Although IDA-PBC itself is robust and performs well throughout various loading conditions, the PI controller added at the voltage part of the IDA-PBC has shown improved performance.

1.6 Organization of Thesis

This thesis consists of this introductory chapter and four other chapters organized as follows:

Chapter 2 provides literature review on the various multilevel inverter topologies and controllers. The significance of choosing the 5-level CHMI is also included.

Chapter 3 explains the research methodology of the thesis. It is divided into three sections namely, the mathematical model for the 5-level CHMI circuit and the development of IDA-PBC control algorithm, simulation model of the system and the experimental set-up.

Chapter 4 presents the simulation and experimental results of the proposed controllers. The performance of each controller is evaluated in terms of output voltage regulation and THD as well as transient response during no load to full load transition, load uncertainty and structural uncertainty. Comparison of the two proposed controllers with the double-loop PI controller is also included.

Chapter 5 provides conclusions of the thesis and recommendation for future works is also included in this chapter.

REFERENCES

- H. A. A. Nabae, I.Takahashi, "A new neutral-point clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523.
- [2] G. S. Shehu, A. B. Kunya, I. H. Shanono, and T. Yalcinoz, "A Review of Multilevel Inverter Topology and Control Techniques," vol. 4, no. 3, pp. 233– 241, 2016.
- [3] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, vol. 52. pp. 1114–1128, 2011.
- [4] P. Y. Lim and N. a. Azli, "A modular structured multilevel inverter active power filter with unified constant-frequency integration control for nonlinear AC loads," in *Proceedings of the International Conference on Power Electronics and Drive Systems*, 2007, pp. 244–248.
- [5] S. S. Katkamwar, "Cascaded H-Bridge Multilevel PV Inverter With MPPT For Grid Connected Application," pp. 641–646, 2016.
- [6] C. Boonmee and Y. Kumsuwan, "Control of single-phase cascaded H-bridge multilevel inverter with modified MPPT for grid-connected photovoltaic systems," *IECON 2013 - 39th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 566– 571, 2013.
- [7] C. S. Kiruba Samuel and K. Ramani, "Multilevel inverter control for windphotovoltaic generation systems," 2012 Int. Conf. Comput. Electron. Electr. Technol. ICCEET 2012, pp. 457–462, 2012.
- [8] N. Chauhan and K. C. Jana, "Cascaded multilevel inverter for underground traction drives," *PEDES 2012 - IEEE Int. Conf. Power Electron. Drives Energy Syst.*, 2012.
- [9] J. N. Chiasson, B. Özpineci, and L. M. Tolbert, "A five-level three-phase hybrid cascade multilevel inverter using a single DC source for a PM synchronous motor drive," *Conf. Proc. IEEE Appl. Power Electron. Conf.*

Expo. - APEC, vol. 2, pp. 1504–1507, 2007.

- [10] R. A. Ahmed, S. Mekhilef, and H. W. Ping, "A three-Phase shunt active power filter with unified constant frequency integration control with RLC connection circuit," in *International Conference for Technical Postgraduates* 2009, TECHPOS 2009, 2009.
- [11] L. Haw, M. S. a Dahidah, and H. a F. Almurib, "SHE-PWM Cascaded Multilevel Inverter With Adjustable DC Voltage Levels Control for STATCOM Applications," *Power Electron. IEEE Trans.*, vol. 29, no. 12, pp. 6433–6444, 2014.
- [12] X. X. X. Xu, Y. Z. Y. Zou, K. D. K. Ding, and F. L. F. Liu, "A STATCOM based on cascade multilevel inverter with phase-shift SPWM," 2004 Int. Conf. Power Syst. Technol. 2004. PowerCon 2004., vol. 1, pp. 1139–1143, 2004.
- [13] Yashobanta Panda, "Analysis of Cascaded Multilevel Inverter Induction Motor Drives," pp. 1–108.
- [14] W. Are et al., "Electrical Power Systems Quality, Second Edition."
- [15] A. F. Cupertino, L. P. Carlette, F. Perez, J. T. Resende, S. I. Seleme, and H. A. Pereira, "Use of control based on passivity to mitigate the harmonic distortion level of inverters," 2013 IEEE PES Conf. Innov. Smart Grid Technol. ISGT LA 2013, 2013.
- [16] D. Committee of the IEEE Power and E. Society, "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems IEEE Power and Energy Society."
- [17] S. T. J. C. and N. R. P. M. H. M. K. Rathi, "PI Control of Multi Level Inverter Based Shunt Active Power Filter for Harmonic Mitigation in Three Phase Systems," in 2015 International Conference on Circuit, power and Computing Technologies, 2015.
- [18] A. Shukla, A. Ghosh, and A. Joshi, "Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, pp. 518–529, 2008.

- [19] A. Visintin, "Mathematical models of hysteresis," in *The Science of Hysteresis*, vol. 1, 2006, pp. 1–123.
- [20] J. Zeng, Z. Zhang, and W. Qiao, "An interconnection and damping assignment passivity-based controller for a DC-DC boost converter with a constant power load," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2314–2322, 2014.
- [21] M. Böttcher, J. Dannehl, and F. W. Fuchs, "Interconnection and Damping Assignment Passivity-Based current control of grid-connected PWM converter with LCL-filter," *Proc. EPE-PEMC 2010 - 14th Int. Power Electron. Motion Control Conf.*, pp. 20–26, 2010.
- [22] G. V. Santos, A. F. Cupertino, V. F. Mendes, and S. I. Seleme, "Interconnection and damping assignment passivity-based control of a PMSG based wind turbine for maximum power tracking," *IEEE Int. Symp. Ind. Electron.*, vol. 2015–Septe, no. x, pp. 306–311, 2015.
- [23] M. Hilairet, O. Bethoux, T. Azib, and R. Talj, "Interconnection and damping assignment passivity-based control of a fuel cell system," *IEEE Int. Symp. Ind. Electron.*, pp. 219–224, 2010.
- [24] Y. Yao and Y. Jiang, "Attitude stabilization of spacecraft with two movingmass via interconnection and damping assignment," *Chinese Control Decis. Conf. 2008, CCDC 2008*, pp. 5115–5118, 2008.
- [25] K. Nunna, M. Sassano, and A. Astolfi, "Constructive Interconnection and Damping Assignment for Port-Controlled Hamiltonian Systems," *IEEE Trans. Automat. Contr.*, vol. 60, no. 9, pp. 2350–2361, 2015.
- [26] D. Jeltsema, R. Ortega, and J. M. A. Scherpen, "An energy-balancing perspective of interconnection and damping assignment control of nonlinear systems," *Automatica*, vol. 40, no. 9, pp. 1643–1646, 2004.
- [27] S. Golestan, M. Ramezani, M. Monfared, and J. M. Guerrero, "A D-Q synchronous frame controller for single-phase inverter-based islanded distributed generation systems," *Int. Rev. Model. Simulations*, vol. 4, no. 1, pp. 42–54, 2011.
- [28] J. F. W. Eds et al., Nonlinear Control of Vehicles and Robots. 2011.

- [29] L. A. Zadeh, "Fuzzy Sets," Inf. Control, no. 8, pp. 338–353, 1965.
- [30] P. Iniyaval and S. R. Karthikeyan, "Fuzzy Logic Based Quasi Z-Source Cascaded Multilevel Inverter with Energy Storage for Photovoltaic Power Generation system," *Emerg. Trends Eng. Technol. Sci. (ICETETS), Int. Conf.*, 2016.
- [31] N. a Azli and S. N. Wong, "Development of a DSP-based Fuzzy P1 Controller for an Online Optimal PWM Control Scheme for a Multilevel Inverter," *Ieee Peds* 2005, pp. 1457–1461, 2005.
- [32] Y. L. Kameswari, "Mitigation of Harmonics in Multilevel Inverter Controlled by Fuzzy Logic Controller," pp. 1–5.
- [33] K. Yamini, B. Vasudha, A. Sharma, and P. Ponnambalam, "Implementation of Fuzzy Logic Controller for Cascaded Multilevel Inverter with Reduced Number of Components," vol. 8, no. January, pp. 278–283, 2015.
- [34] B. Shanthi, "FPGA based Fuzzy Logic Control for Single Phase Multilevel Inverter," vol. 9, no. 3, pp. 10–18, 2010.
- [35] H. Taheri, "Modeling and Nonlinear Control of Multilevel Inverter for Photovoltaic Application," 2016 IEEE Can. Conf. Electr. Comput. Eng., 2016.
- [36] T. V. Narmadha and T. Thyagarajan, "Fuzzy Logic Based Position-Sensorless Speed Control of Multi Level Inverter Fed PMBLDC Drive," J. Adv. Inf. Technol., vol. 1, no. 1, pp. 52–58, Feb. 2010.
- [37] C. R. Baier, M. Torres, J. A. Muñoz, J. M. Mauricio, J. Rohten, and M. Rivera, "Nonlinear Control Strategy for Current Source Cascaded H-bridge Inverters An Approach Considering Single-Phase DQ Components," pp. 3079–3084, 2015.
- [38] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in 2010 International Power Electronics Conference - ECCE Asia -, IPEC 2010, 2010, pp. 492–501.
- [39] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.

- [40] R. A. Ahmed, S. Mekhilef, and H. W. Ping, "New multilevel inverter topology with minimum number of switches," in *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, 2010, pp. 1862–1867.
- [41] M. Malinowski, S. Member, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," vol. 57, no. 7, pp. 2197–2206, 2010.
- [42] D. Raveendhra, M. K. Pathak, and A. Panda, "Power conditioning system for solar power applications: Closed loop DC-DC convertor fed FPGA controlled diode clamped multilevel inverter," 2012 IEEE Students' Conf. Electr. Electron. Comput. Sci. Innov. Humanit. SCEECS 2012, pp. 0–3, 2012.
- [43] F. Bouchafaa, D. Beriber, and M. S. Boucherit, "Modeling and control of a gird connected PV generation system," 18th Mediterr. Conf. Control Autom. MED'10 - Conf. Proc., pp. 315–320, 2010.
- [44] A. B. Sankar and R. Seyezhai, "ANALYSIS OF CARRIER BASED MODULATION STRATEGIES FOR AN ACTIVE NEUTRAL POINT CLAMPED MULTILEVEL INVERTER FOR WIND APPLICATIONS."
- [45] S. Y. Gadgune, P. T. Jadhav, L. R. Chaudhary, and M. M. Waware, "Implementation of shunt APF based on Diode Clamped and Cascaded Hbridge multilevel inverter," *Proc. 2015 IEEE Int. Conf. Electr. Comput. Commun. Technol. ICECCT 2015*, 2015.
- [46] A. Alqudah, I. Altawil, and L. Quraan, "Control of Variable Speed Drive based on Diode Clamped Multilevel Inverter," *Control*, vol. 2, no. 1, pp. 0–5, 2013.
- [47] R. V. Thomas, E. Rakesh, J. Jacob, and A. Chitra, "Identification of Optimal SVPWM Technique for Diode Clamped Multilevel Inverter based Induction Motor Drive," 2015.
- [48] W. K. Lee, S. Y. Kim, J. S. Yoon, and D.-H. Baek, "A Comparison of the Carrier-based PWM Techniques for Voltage Balance of Flying Capacitor in the Flying Capacitor Multilevel Inverter," *Twenty-First Annu. IEEE Appl. Power Electron. Conf. Expo. 2006. APEC '06.*, pp. 1653–1658, 2006.

- [49] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, 2002.
- [50] S. P. Gawande, S. Khan, and M. R. Ramteke, "Voltage sag mitigation using multilevel inverter based distribution static compensator (DSTATCOM) in low voltage distribution system," 2012 IEEE 5th India Int. Conf. Power Electron., pp. 1–6, 2012.
- [51] N. Devarajan and A. Reena, "Reduction of switches and DC sources in Cascaded Multilevel Inverter," *Bull. Electr. Eng. Informatics*, vol. 4, no. 3, pp. 186–195, 2015.
- [52] A. Nordvall, "Multilevel Inverter Topology Survey Master of Science Thesis in Electric Power Engineering Division of Electric Power Engineering Multilevel Inverter Topology Survey," p. 78, 2011.
- [53] M. ArulKumar, A; Prabha, N.Rathina; Kalarathi, "PI Controller Based Shunt Active Power Filter with Cascaded Multilevel Inverter," *Int. J. Innov. Res. Sci. Eng. Technol.*
- [54] a. Dell'Aquila, V. G. Monopoli, and M. Liserre, "Control of H-bridge based multilevel converters," *Ind. Electron. 2002. ISIE 2002. Proc. 2002 IEEE Int. Symp.*, vol. 3, pp. 766–771, 2002.
- [55] K. S. Rao and R. Mishra, "Comparative study of P, PI and PID controller for speed control of VSI-fed induction motor," *Int. J. Eng. Dev. Res.*, vol. 2, no. 2, pp. 2321–9939, 2014.
- [56] K. Sundararajan, A. Nachiappan, and G. Veerapathiran, "Comparison of Current Controllers for a Five-level Cascaded H-Bridge Multilevel Inverter," *Ijcer*, vol. 2, no. 6, pp. 5–7, 2012.
- [57] B. Jayawardhana, R. Ortega, E. García-Canseco, and F. Castaños, "Passivity of nonlinear incremental systems: Application to PI stabilization of nonlinear RLC circuits," *Syst. Control Lett.*, vol. 56, no. 9–10, pp. 618–622, Sep. 2007.
- [58] M. Miloševic, "Hysteresis current control in three-phase voltage source inverter," pp. 1–15, 2003.
- [59] R. Gupta, A. Ghosh, and A. Joshi, "Multiband hysteresis modulation and

switching characterization for sliding-mode-controlled cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2344–2353, 2010.

- [60] M. K. Menshawi, M. N. Abdul Kadir, and S. Mekhilef, "Voltage vector approximation control of multistage - Multilevel inverter using simplified logic implementation," *IEEE Trans. Ind. Informatics*, vol. 9, pp. 2052–2062, 2013.
- [61] H. Mao, X. Yang, Z. Chen, and Z. Wang, "Improved hysteresis current control of multilevel inverters with constant switching frequency," in *IECON Proceedings (Industrial Electronics Conference)*, 2010, pp. 511–515.
- [62] R. Ortega and M. W. Spong, "Adaptive motion control of rigid robots: a tutorial," *Proc. 27th IEEE Conf. Decis. Control*, no. 85, 1988.
- [63] C. Batlle, "Passive control theory I," *IEEE Control Syst. Mag.*, 2005.
- [64] H. Ma, F. Xu, L. Du, and X. Chen, "Discrete-time passivity-based slidingmode control of single-phase current-source inverter," 2009 35th Annu. Conf. IEEE Ind. Electron., no. 1, pp. 403–407, Nov. 2009.
- [65] R. O. A. L. P. er J. N. H. Sira-Ramirez;, "Passivity-based Control of Euler-Lagrange Systems:"
- [66] H. Sira-Ramirez and R. Ortega, "Passivity-based controllers for the stabilization of DC-to-DC power converters," *Proc. 1995 34th IEEE Conf. Decis. Control*, vol. 4, no. December, pp. 3471–3476, 1995.
- [67] a Y. Achour, B. Mendil, S. Bacha, and I. Munteanu, "Passivity-based current controller design for a permanent-magnet synchronous motor.," *ISA Trans.*, vol. 48, no. 3, pp. 336–46, Jul. 2009.
- [68] A. Loría and H. Nijmeijer, "Passivity Based Controller," Control Syst. Robot. Autom., vol. XIII.
- [69] R. Ortega, A. Loria, R. Kelly, and L. Praly, "On passivity-based output feedback global stabilization of euler-lagrange systems," *Int. J. Robust Nonlinear Control*, vol. 5, no. 4, pp. 313–323, 1995.
- [70] H. A. Abdel Fattah and K. A. Loparo, "Passivity-based torque and flux

tracking for induction motors with magnetic saturation," *Automatica*, vol. 39, no. 12, pp. 2123–2130, Dec. 2003.

- [71] L. Shiau, J. Lin, and Y. Yeh, "Passivity based control for induction motor drives with voltage-fed," vol. 59, pp. 1–11, 2001.
- [72] J. Linares-Flores, J. L. Barahona-Avalos, H. Sira-Ramirez, and M. A. Contreras-Ordaz, "Robust passivity-based control of a buck-boostconverter/DC-Motor system: An active disturbance rejection approach," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2362–2371, 2012.
- [73] D. Noriega-Pineda and G. Espinosa-Perez, "Passivity- based Control of Multilevel Cascade Inverters: High Performance with Reduced Switching Frequency," 2007 IEEE Int. Symp. Ind. Electron., pp. 3403–3408, 2007.
- [74] D. Noriega-Pineda, "On the Passivity-based Control for Multilevel Inverters,"... Congr. 10th IEEE, 2006.
- [75] D. Noriega-Pineda, G. Espinosa-Pérez, V. Cárdenas, and J. Alvarez-Ramírez, "Passivity-based control of multilevel cascade inverters: High-performance with reduced switching frequency," *Int. J. Robust Nonlinear Control*, p. n/an/a, 2009.
- [76] H. Miranda, V. Cárdenas, G. Espinosa-Pérez, and D. Noriega-Pineda, "Multilevel cascade inverter with voltage and current output regulated using a passivity-based controller," in *Conference Record - IAS Annual Meeting* (*IEEE Industry Applications Society*), 2006, vol. 2, pp. 974–981.
- [77] H. Miranda, V. Cardenas, G. Sandoval, and G. Espinosa-Perez, "Hybrid Control Scheme for a Single-Phase Shunt Active Power Filter Based on Multilevel Cascaded Inverter," in *Power Electronics Specialists Conference*, 2007. PESC 2007. IEEE, 2007, pp. 1176–1181.
- [78] R. Ortega, A. Van Der Schaft, I. Mareels, and B. Maschke, "Putting energy back in control," *Control Syst. IEEE*, vol. 21, no. 2, pp. 18–33, 2001.
- [79] R. Ortega and E. García-Canseco, "Interconnection and Damping Assignment Passivity-Based Control: A Survey," *Eur. J. Control*, vol. 10, no. 5, pp. 432– 450, 2004.

- [80] H. Miranda and D. Unam, "Multilevel Cascade Inverter with Voltage and Current Output Regulated Using a Passivity – Based Controller," vol. 0, no. c, pp. 974–981, 2006.
- [81] R. Ortega, A. Van der Schaft, B. Maschke, and G. Escobar, "Interconnection and damping assignment passivity-based control of port-controlled Hamiltonian systems," *Automatica*, vol. 38, no. 4, pp. 585–596, 2002.
- [82] G. Escobar, A. J. van der Schaft, and R. Ortega, "A Hamiltonian viewpoint in the modeling of switching power converters," *Automatica*, vol. 35, no. 3, pp. 445–452, Mar. 1999.
- [83] C. Batlle, A. Dòria-Cerezo, and E. Fossas, "IDA-PBC controller for a bidirectional power flow full-bridge rectifier," *Proc. 44th IEEE Conf. Decis. Control. Eur. Control Conf. CDC-ECC '05*, vol. 2005, pp. 422–426, 2005.
- [84] Y. Wang, D. Cheng, and X. Hu, "Problems on time-varying port-controlled Hamiltonian systems: Geometric structure and dissipative realization," *Automatica*, vol. 41, no. 4, pp. 717–723, 2005.
- [85] Y. Wang, C. Li, and D. Cheng, "Generalized Hamiltonian realization of timeinvariant nonlinear systems," *Automatica*, vol. 39, no. 8, pp. 1437–1443, 2003.
- [86] Q. Zhang and G. Liu, "Precise Control of Elastic Joint Robot Using an Interconnection and Damping Assignment Passivity Based Approach," *IEEE/ASME Trans. Mechatronics*, vol. 4435, no. c, pp. 1–1, 2016.
- [87] V. Muralidharan, M. T. Ravichandran, and A. D. Mahindrakar, "Extending interconnection and damping assignment passivity-based control (IDA-PBC) to underactuated mechanical systems with nonholonomic Pfaffian constraints: The mobile inverted pendulum robot," *Proc. IEEE Conf. Decis. Control*, pp. 6305–6310, 2009.
- [88] H. L. H. Li, X. W. X. Wang, and T. T. T. Tian, "The performance research of induction motor systems controlled by the IDA-PBC method and its speed sensorless implementation," *Electr. Mach. Syst. (ICEMS), 2010 Int. Conf.*, pp. 0–3, 2010.

- [89] H. González, M. a. Duarte-Mermoud, I. Pelissier, J. C. Travieso-Torres, and R. Ortega, "A novel induction motor control scheme using IDA-PBC," J. *Control Theory Appl.*, vol. 6, no. 1, pp. 59–68, Mar. 2008.
- [90] J. Li, Y. Liu, C. Li, and B. Chu, "Passivity-based nonlinear excitation control of power systems with structure matrix reassignment," *Inf.*, vol. 4, no. 3, pp. 342–350, 2013.
- [91] a. R. Ram??rez-L??pez, N. Visairo-Cruz, C. a. N????ez-Guti??rrez, J. J. Lira-P??rez, and H. Sira-Ram??rez, "Input-output linearization and Generalized PI control of a single-phase active multilevel rectifier," *Progr. Abstr. B. - 2010 7th Int. Conf. Electr. Eng. Comput. Sci. Autom. Control. CCE 2010*, vol. 27, no. Cce, pp. 22–27, 2010.
- [92] D. Gerardo and Z. Universitaria, "Interconnection and Damping Passivity-Based Control applied to a Single-Phase Voltage Source Inverter," no. 2, pp. 229–234, 2010.
- [93] A. Tofighi and M. Kalantar, "Interconnection and damping assignment and Euler-Lagrange passivity-based control of photovoltaic/battery hybrid power source for stand-alone applications," *J. Zhejiang Univ. Sci. C*, vol. 12, no. 9, pp. 774–786, 2011.
- [94] S. R. Bowes and Y. S. Lai, "Investigation into optimising high switching frequency regular sampled PWM control for drives and static power converters," *Electr. Power Appl. IEE Proc.*, vol. 143, no. 4, pp. 281–293, 1996.
- [95] I. Sarkar and B. G. Fernandes, "Modified Hybrid Multi-Carrier PWM Technique for Cascaded H-Bridge Multilevel Inverter," *Ind. Electron. Soc. IECON 2014 - 40th Annu. Conf. IEEE*, pp. 4318–4324, 2014.
- [96] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-19, 1983.
- [97] H. Miranda and V. Cardenas, "Hybrid control scheme for a single-phase shunt active power filter based on multilevel cascaded inverter," *Power Electron.* ..., no. 51050, pp. 1176–1181, 2007.

- [98] G. Sandoval, H. Miranda, G. Espinosa–Pérez, and V. Cárdenas, "Passivitybased control of an asymmetric nine-level inverter for harmonic current mitigation," *IET Power Electron.*, vol. 5, no. 2, p. 237, 2012.
- [99] R. Ortega and E. García-Canseco, "Interconnection and Damping Assignment Passivity-Based Control: A Survey," *Eur. J. Control*, vol. 10, no. 5, pp. 432– 450, Jan. 2004.
- [100] M. Gonzalez, V. Cirdenas, and F. Pazos, "DQ transformation development for single-phase systems to compensate harmonic distortion and reactive power," *9th IEEE Int. Power Electron. Congr. 2004. CIEP 2004*, vol. 0, pp. 177–182, 2004.
- [101] H. Kim and S. K. Sul, "Analysis on output LC filters for PWM inverters," 2009 IEEE 6th Int. Power Electron. Motion Control Conf. IPEMC '09, vol. 3, pp. 384–389, 2009.
- [102] H. Kim and S. K. Sul, "A novel filter design for output LC filters of PWM inverters," J. Power Electron., vol. 11, no. 1, pp. 74–81, 2011.
- [103] B. Urmila and D. Subbarayudu, "Multilevel Inverters : A Comparative Study of Pulse Width Modulation Techniques," vol. 1, no. 3, pp. 3–7, 2010.
- [104] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converters, Applications, and Design*, vol. 4. 2007.