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Millimeter Wave Band Reconfigurable Circuits (from 30 to above 100 GHz) in BiCMOS-MEMS Technology

Author
Julio César Heredia Vega

Thesis Advisors
Prof. Lluís Pradell i Cara (Dept. TSC, UPC)
Dr.-Ing Mehmet Kaynak (IHP – Leibniz-Institut für innovative Mikroelektronik)

with special counseling by
Prof. Miquel Ribó i Pal (Salle-URL)

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Dripping water hollows out stone,
not through force but through persistence
-Ovid

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ABSTRACT

Nowadays, there has been an increased use of mobile devices and growth in the need for information, and because of this, wireless systems with higher data rates and wider bandwidths are demanded every year. Additionally, multi-applications systems need to operate at several frequency bands, which brings the need for compact frequency-reconfigurable devices.

In order to offer solutions for the demands mentioned above, in this Thesis, compact frequency-reconfigurable low-noise amplifiers (LNAs) using RF-MEMS and HBT based switches for frequencies above 100 GHz are presented for the first time. Multimodal coupled microstrip and three-line microstrip (TLM) structures are implemented in the amplifier matching networks to achieve more-compact designs.

To demonstrate the potentialities of the TLM structures, a novel compact multimodal TLM impedance tuner is presented. It features a Smith-chart impedance coverage of 70% in a large frequency bandwidth (1.4 to 3.2 GHz). The impedance tuner uses variable capacitors implemented with varactors to create asymmetries in the structure and interactions among the three-line microstrip modes. This results in an increase of the equivalent electrical size of the circuit thus reducing the overall physical size of the impedance tuner.

Three frequency-reconfigurable D-band compact BiCMOS LNAs have been designed. The three designs consist of two cascode stages and were fabricated using a 0.13 µm SiGe:C BiCMOS process which includes an embedded RF-MEMS switch module. The first and second LNA designs operate at 125/140 GHz, while the third design operates at 125/143 GHz. The area of the designs is minimized by using only one RF-MEMS switch to select the frequency band and multimodal structures (a coupled microstrip structure and a TLM structure in the input matching networks of the first and third design respectively). A systematic design method to obtain balanced gain and noise figure for both frequency states is presented.

An even more compact 120/140 GHz LNA design is accomplished by using an HBT-based switch instead of a RF-MEMS switch. It was fabricated with the same 0.13 µm SiGe:C BiCMOS process and using the same multimodal TLM structure in the input matching network as the third design mentioned above.

The measurements of all the LNAs are in good agreement with the obtained simulations thus validating all the circuit designs and the systematic design method.

CONTENTS

CHAPTER ONE

Introduction

In this chapter, the motivation for the development of this work is described in a detail manner. After that, established objectives are described, and finally, a brief description of the outline of this Thesis is included.

1.1 Motivation

The mm-wave frequency region spanning from 100 GHz to 300 GHz and the terahertz region spanning from 300 GHz to 3 THz are rising an increasing interest thanks to the recent development made on semiconductor technologies. Some important applications are shown in Fig. 1.1 and described as follows [1]:

- **Radar and Imaging.** The terahertz and mm-wave bands offer wide bandwidth, and new radar and imaging systems can benefit from that. This would lead to superior resolution and improved detection capabilities [2] [3].

- **Medical science.** Biological molecules resonate with frequencies that range in the terahertz band. A lot of biomedical imaging and spectroscopy applications can benefit from this characteristic. Also, this type of energy (along with mm-wave energy) is non-ionizing, so it can be used safely on the human body [4]. This feature has been also exploited at mm-wave band, leading to the development of probes for tissue analysis [5].

- **Security.** Drugs [6], weapons and explosives [7] can be detected using mm-wave sensors and terahertz spectroscopy, thanks to the difference in the resonation of the molecules. Due to its ability to penetrate through different kind of materials (clothes, paper, cardboard, among others), mm-wave and terahertz band have a potential use at security control portals at airports and package inspection.

- **Space science.** Earth environmental monitoring and telescopes have been already using the mm-wave and terahertz bands. The Earth Observing System Microwave Limb Sounder (EOS-MLS), uses frequencies as high as 118, 190, 240, 640 GHz and 2.5 THz. It was launched in 2004 and has been monitoring the chemicals in the atmosphere since then [8].

- **Industrial applications.** Mm-wave and terahertz imaging can be used as a non-invasive method for the inspection of materials, parts and final products of several industrial processes [9]. This method has been already implemented for the inspection of foam materials used for space shuttles fuel tanks [10].

- **Wireless communication networks.** The 100-300 GHz mm-wave band is ideal for the development of future wireless networks. In the present time, the 60 GHz band is the standard for high-speed wireless communication systems with data rates of 6 to 7 Gbps (IEEE 802.11ad) [11]. However, in order to reach even higher data rates, the carrier frequency has to be increased greater than 100 GHz.

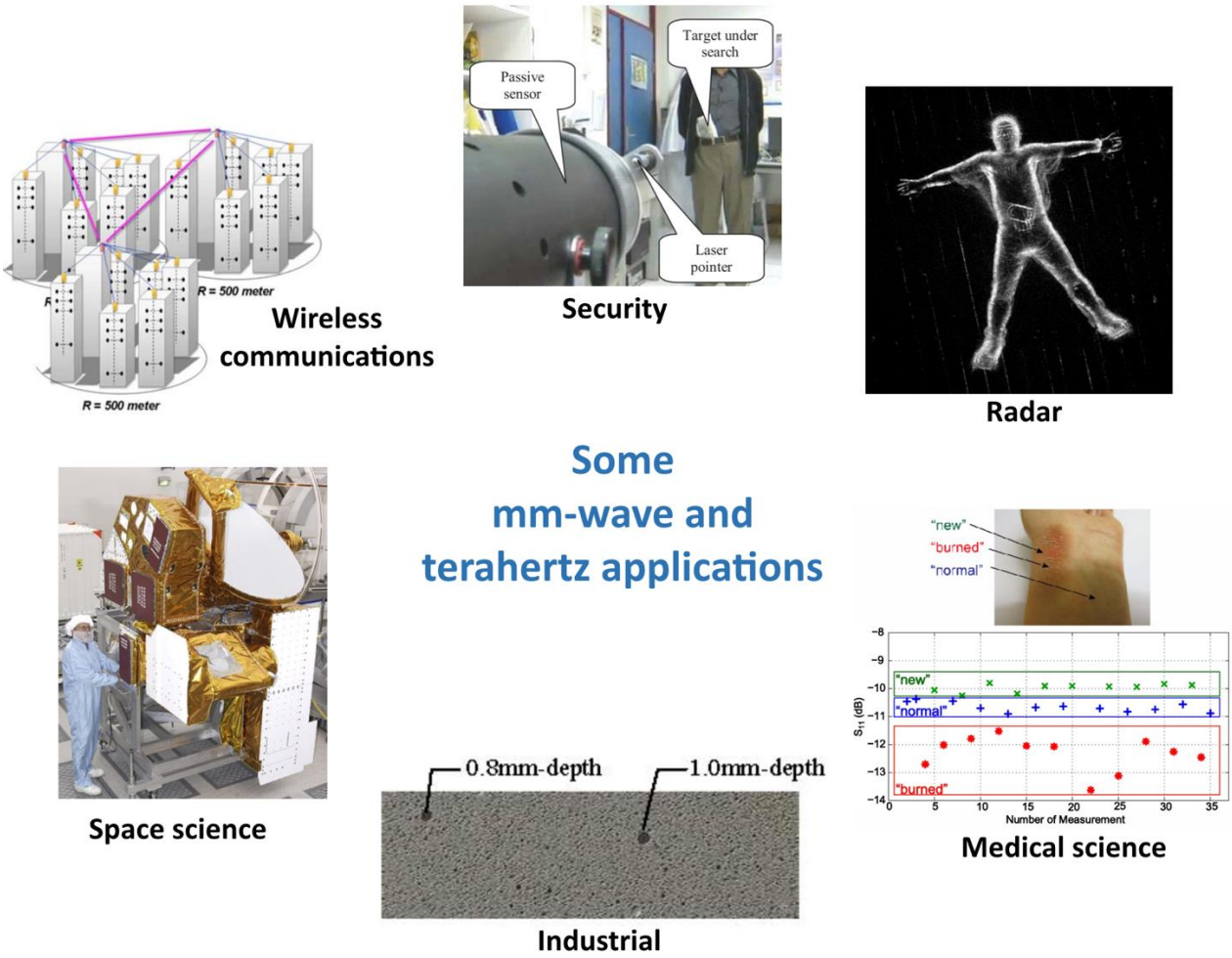


Fig. 1.1. Mm-wave and terahertz band applications. **Security**: mm-wave sensor for concealed object detection [7]. **Radar**: scanning of a person with concealed phone using radar [3]. **Medical science**: burned skin measurement [5]. **Industrial**: pore detection on ceramic [9]. **Space science**: picture of the EOS-MLS [8]. **Wireless communications**: concept of wireless link communication network for D-band [12].

As seen from these applications, 100-300 GHz mm-wave and terahertz bands have shown a lot of potential for future applications; especially in the wireless communications field. Due to the increased use of mobile devices and growth of consumed information, higher-speed data rates and more bandwidth are demanded every year. Future wireless networks and links can beneficiate from the high-speed data rate and wide bandwidth achieved in this frequency band. In the near future, wireless systems will move beyond 100 GHz, where data speed rates as high as 100 Gbps can be reached. Specifically the D-band (frequency band that ranges from 110 to 170 GHz) has attracted the wireless systems community because it further widens the available channel bandwidths, and because is allocated in a good atmospheric attenuation window [13].

The RF front-end is a key component of the wireless systems. It is mainly composed by a band-pass filter, a low-noise amplifier (LNA) and a mixer used along with a local oscillator, which down-convert the frequency of the signal. Modern systems and devices need to work at several frequency bands (multiband system) in order to be functional for different applications; this implies that several RF front-ends have to be implemented in a single device. However, increasing the number of components leads to an increase in size, cost and power consumption, which are critical characteristics of the system. One solution is to use wideband components to cover all the frequency bands needed by the system, but the problem with this approach is that, if the fundamental frequencies of the carrier waves are too close to each other, there will be undesired out-of-band signals. Another practical solution is the use of reconfigurable systems. This allows the RF front-end to select each frequency needed by the device in a more selective way, thus avoiding interference problems.

In the RF front-end a reconfigurable filter would require low losses and a wide tuning frequency range, which is very difficult to attain. Because of this, a reconfigurable LNA would require high selectivity and top performance characteristics to avoid undesired out-of-band signals [14]. Also, an LNA intended for future wireless systems needs to achieved reconfigurability, high gain, low-noise figure, and high stability at frequencies above 100 GHz.

In addition to reconfigurable components, a further size reduction of the system is possible by using multimodal waveguides, such as three-line microstrip (TLM). This kind of structures allows the propagation of more than one fundamental mode in the same circuit area. These additional modes increase the equivalent electrical length of the circuit and result in compact-size designs. Multimodal circuits have demonstrated reconfiguration capabilities and compact size in structures such as filters [15]. Moreover, multimodal equivalent circuits have been developed for complex multimodal structures which can be easily implemented with electronic design software without using electromagnetic analysis [16].

Recent improvement in SiGe BiCMOS (Silicon-Germanium bipolar complementary metal-oxide-semiconductor) technology have demonstrated its capability for the implementation of applications above 100 GHz. It has reach cut-off frequencies (highest frequency at which the transistor gain current is equal to one) as high as 500 GHz and maximum oscillation frequencies (highest frequency for which the transistor power gain is equal to one) up to 300 GHz [17]. This technology has the uniqueness of including both heterojunction bipolar transistors (HBTs) and the complementary metal-oxide-semiconductor (CMOS) technology thus allowing the combination of analog and digital circuits in a single chip. RF designers can take advantage of the benefits provided by the SiGe HBTs such as high gain, low noise, good linearity and good power handling in order to fulfill the requirements of the mm-wave and terahertz systems.

Besides all of these benefits, it has been also demonstrated the integration of micro-electro-mechanical systems (MEMS) modules into the BiCMOS process. Techniques such as bond-wire or flip-chip provide more parasitics than the monolithic

integration of the RF-MEMS switch [18]. This level of integration allows high isolation and low losses up to 250 GHz [19]. Also, a wafer level package (WLP) encapsulation for RF-MEMS switches has been already demonstrated in the SiGe BiCMOS technology. WLP is preferable to other packaging techniques approaches, such as wire bonding, because it requires less steps in the fabrication process and occupy less area than WLP [20] thus decreasing in cost and low losses.

Several mm-wave components have been demonstrated using SiGe BiCMOS technology with excellent performance for frequencies beyond 100 GHz. In [21] an on-chip antenna for D-band applications has been designed using SiGe BiCMOS technology. Using micromachining techniques, the authors have overcome the thin insulator problem typical of antennas (separation between the top and bottom metal of SiGe BiCMOS technology usually doesn't exceed 15 μm), which leads to low efficiency. In [22], a D-band LNA was developed, showing high gain and low-noise figure comparable to other III-V technologies. In [2] a single-chip transmit-receive module for F-band radar systems with embedded RF-MEMS switches have been designed and fabricated, demonstrating that several functionalities can be integrated into a single SiGe BiCMOS chip. All of these examples and many others, confirm the potential of the SiGe BiCMOS technology for the development of low-cost and high-performance mm-wave systems beyond 100 GHz.

1.2 Objectives

The main goal of this PhD Thesis is the design of compact multimodal structures and reconfigurable LNAs using SiGe BiCMOS technology (taking advantage of its RF-MEMS switch integration), with special attention to frequencies above 100 GHz. Since standardization activities for the D-band are still pending [23], the selected LNAs design frequencies correspond to the specified by the ITU regulations (specifically 122.5 to 123 GHz and 141 to 148.5 GHz) [24]. Possible applications for LNAs above 100 GHz are point-to-point or point-to-multipoint backhaul systems and short-range communications which are emerging in the D-band [12]. However, other applications could be envisaged. Taking this into consideration, the main objectives of this Thesis are:

- **Development of multimodal compact matching networks** proposing new designs and multimodal models, and compare the advantages and disadvantages with respect to conventional line-plus-stub (LPS) matching networks.

- **Design, fabrication, and characterization of a compact TLM impedance tuner for low frequency,** using the multimodal structure designs and models already developed.

- **Study of the advantages, disadvantages, and characteristics of SiGe BiCMOS-MEMS technology** from IHP (Innovations for High Performance Microelectronics), and also explore no-reconfigurable LNAs configurations for D-band (since reconfigurable LANs for this band have not been yet reported) and reconfigurable configurations below 100 GHz.

- **Design, fabrication, and characterization of reconfigurable compact LNAs using RF-MEMS switches** in IHP's 0.13 μm SiGe:C BiCMOS technology for the 122.5 to 123 GHz-band and 141 to 148.5 GHz-band [24][12].

- **Design, fabrication, and characterization of reconfigurable compact LNAs using transistor-based switches** in IHP's 0.13 μm SiGe:C BiCMOS technology for the 122.5 to 123 GHz-band and 141 to 148.5 GHz-band. Even if transistor-based switches have a low performance for high frequencies, very compact designs can be achieved with them. Also, it is interesting to compare the performance of reconfigurable LNAs using RF-MEMS switches with transistor-based switches.

1.3 Thesis outline

This dissertation is divided into seven chapters as follows:

- **Chapter 1** describes the motivation for this work, the main intended objectives and the outline of this thesis.

- **Chapter 2** studies the concepts of IHP's SiGe:C BiCMOS technology. It describes the technology, the HBT transistor, metallization layers, and the RF-MEMS switch.

- **Chapter 3** focuses on the study of multimodal theory and multimodal models for coupled microstrip line and TLM structures.

- **Chapter 4** presents the design, simulation, fabrication, and characterization of a compact impedance tuner using the TLM structures already studied in Chapter 3. It uses six variable capacitances created using parallel-connected varactors, which interact among the TLM modes to obtain a minimal Smith-chart coverage of 70% in an 85% fractional bandwidth from 1.4 to 3.2 GHz.

- **Chapter 5** describes the design, fabrication, and characterization of compact reconfigurable LNAs for the 122.5 to 123 GHz-band and 141 to 148.5 GHz-band. All the designs have two stages using a cascode configuration, a bias of 2.5 V and a single RF-MEMS switch to achieve frequency reconfigurability. The first design includes a conventional LPS input matching network, the

second one uses a coupled microstrip line stub included in the input matching network, and a third one avails a TLM compact structure for the input matching network.

- **Chapter 6** describes the design, fabrication, and characterization of a compact reconfigurable LNA using a transistor-based switch for the 122.5 to 123 GHz-band and 141 to 148.5 GHz-band.

- **Chapter 7** provides the conclusions, summarizing the contributions of this dissertation and presenting suggested future research lines to enhance the proposed designs.

CHAPTER TWO

SiGe BiCMOS-MEMS TECHNOLOGY

Thanks to the recent improvements in the SiGe BiCMOS technology, high performance circuits for frequencies at D-band are now a reality. Also, the addition of RF-MEMS structures to the process flow leads to the design of new reconfigurable circuits for frequencies above 100 GHz.

In this chapter, a brief description of the SiGe BiCMOS technology is presented. The basic concepts and process flow of the technology are described; after that, the IHP's 0.13 μm SiGe:C BiCMOS-MEMS technology is discussed. IHP's technology studied in this chapter will be used in Chapter 5 and Chapter 6 for the development of frequency-reconfigurable amplifiers for D-band applications.

2.1. SiGe BiCMOS technology

The SiGe BiCMOS technology has the uniqueness of including both HBT and CMOS technology in the same process flow, thus allowing the combination of analog and digital circuits in a single chip. Bipolar devices have high speed, low noise, high gain and driving capabilities, while CMOS devices are very attractive for digital applications thanks to its low power and high packing density. The combination of both technologies allows not only the improvement of present-day circuits, but the development of completely new designs [25].

Introducing Ge into Si improves the carrier mobility with respect to Si, this is why HBTs can reach higher frequencies compared to standard bipolar transistors. Because a practical SiGe film must be thin and defect-free, it is the perfect candidate for the base of a bipolar transistor, which must be thin to achieve high-frequency operation. SiGe BiCMOS technology beneficiates from the RF and analog performance advantages of the SiGe HBT as well as existing CMOS process schemes like deep and shallow trench isolation and back-end-of-line (BEOL) low-loss metallization layers, which translates in cost savings [26].

2.2. SiGe BiCMOS technology process flow

In Fig. 2.1 the process flow for an NPN heterojunction bipolar transistor of a standard SiGe BiCMOS technology is shown. The Si substrate is doped to implant a N^+ buried layer (NBL) using a SiO_2 film (Fig. 2.1a); usually the dopant for this implantation is As or Sb. Shallow-trench and deep-trench isolation regions are created using etching in order to avoid current leaks between the transistor and nearby devices (Fig. 2.1b). After that, an oxide film (SiO_2) is deposited to implant the collector sinkers to reduce the resistance between the collector-contacts and the NBL (Fig. 2.1c). Then, the base is deposited using SiGe (Fig. 2.1d), and over the base, the emitter is deposited using Si (Fig. 2.1e). A dielectric stack (SiO_2 and Si_3N_4) is used as an insulator between the polysilicon emitter and the base (Fig. 2.1e). The SIC (selectively implanted collector) is implanted through the emitter opening (Fig. 2.1f), and after that, the polysilicon emitter is deposited (Fig. 2.1g); the metal contacts are deposited as final step (Fig. 2.1h) [27].

The process depicted above is used only for the fabrication of HBTs, while the steps used for the fabrication of CMOS devices are the same employed in a conventional CMOS technology process.

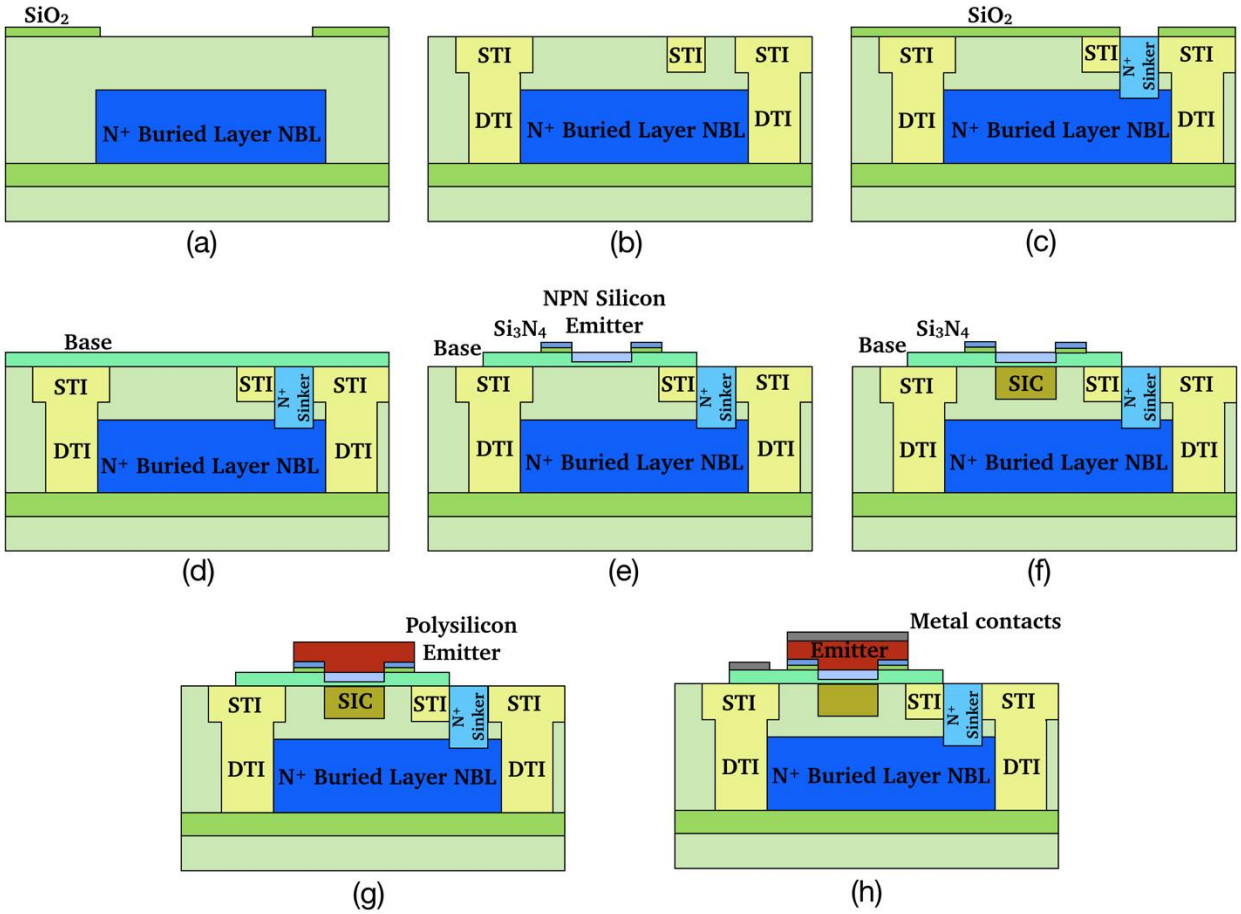


Fig. 2.1. Process flow of the SiGe BiCMOS technology.

2.3. IHP's 0.13 µm SG13G2 SiGe:C BiCMOS-MEMS technology

2.3.1. Technology process

The 0.13 µm SG13G2 SiGe:C BiCMOS-MEMS technology provided by IHP includes HBTs with cut-off frequencies as high as 500 GHz and maximum oscillation frequencies up to 300 GHz. This technology was developed under the goals of the European project DOTFIVE, with the objective of reach HBT cut-off frequencies as high as 500 GHz. This technology can be used in applications such as mm-wave sensing and imaging; high-data-rate wireline and wireless communications; and automotive radar [28].

Fig. 2.2a illustrates a schematic cross section of the HBT. The collector well is fabricated by ion implantation and rapid thermal processing (RTA). The emitter is grown using in-situ As as dopant and the elevated base is grown by in-situ Si epitaxy with B as dopant [17]. Fig. 2.2b shows a transmission electron microscopy cross

section image of a fabricated HBT and Table 2.1 illustrates the parameters for an eight-emitter HBT measured in parallel.

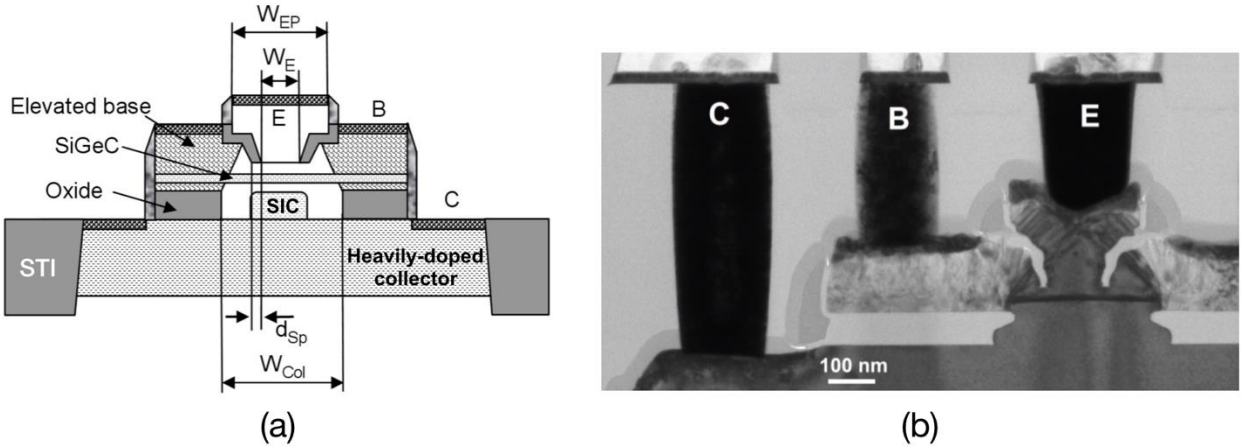


Fig. 2.2. (a) Schematic cross section of the HBT: W_E is the Si emitter width, W_{EP} is the poly-Si emitter width, d_{Sp} is the emitter spacer width and W_{Col} is the collector width [17]. (b) Transmission electron microscopy cross section image of the HBT [28].

Table 2.1. HBT parameters for IHP's 0.13 µm SG13G2:C BiCMOS technology. Devices with eight emitters in parallel were measured [17].

Parameter	Unit	Measurement condition	SG13G2 technology
W_E	µm	Emitter width	0.12
L_E	µm	Emitter length	0.96
A_E	µm²	Emitter area	0.92
W_{EP}	µm	Poly-Si emitter width	0.3
W_{Col}	µm	Collector width	0.31
ß		V_{BE}=0.7	700
BV_{EBO}	V	$j_E = \frac{I_E}{A_E} = 10\ \frac{\mu A}{\mu m^2}$ Emitter-base breakdown voltage	1.6
BV_{CBO}	V	$j_C = \frac{I_C}{A_C} = 0.5\ \frac{\mu A}{\mu m^2}$ Collector-base breakdown voltage	5.1
BV_{CEO}	V	$V_{BE} = 0.7\ V$ Collector-emitter breakdown voltage	1.6

The SG13G2 SiGe:C BiCMOS-MEMS technology substrate is illustrated in Fig. 2.3. It is composed by seven metallic layers: Metal1 (M1), Metal2 (M2), Metal3 (M3), Metal4 (M4), Metal5 (M5), TopMetal1 (TM1) and TopMetal2 (TM2); the isolator between the metallic layers is oxide.

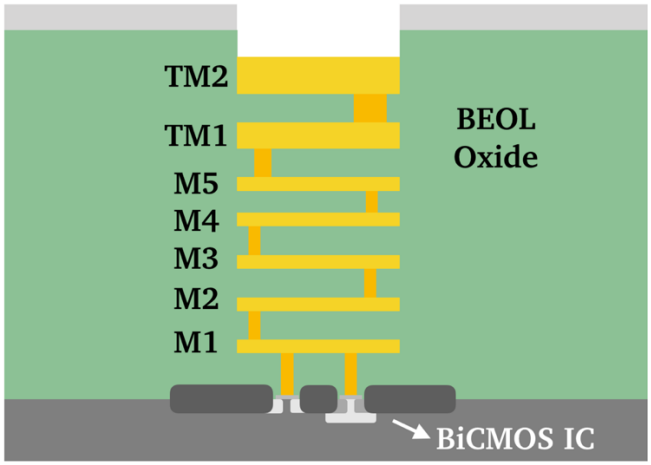


Fig. 2.3. IHP's 0.13 µm SG13G2 SiGe:C BiCMOS-MEMS technology substrate [18].

2.3.2. RF-MEMS module

IHP's 0.13µm SG13G2 SiGe:C BiCMOS-MEMS technology includes a RF-MEMS module embedded in the BEOL. The RF-MEMS is designed for a 110 to 170 GHz frequency band, which is ideal for applications at D-band. It is fabricated using a wafer-level process and is encapsulated using the TM2 layer as shown in Fig. 2.4.

The RF-signal line is realized using M5 and the high-voltage electrodes using M4. The movable membrane is fabricated using TM1 and the encapsulation plate with releasing holes is designed using TM2. The membrane is released using hydrofluoric acid vapor phase etching (HFVPE) through the TM2 grid down to M4 high-voltage electrodes.

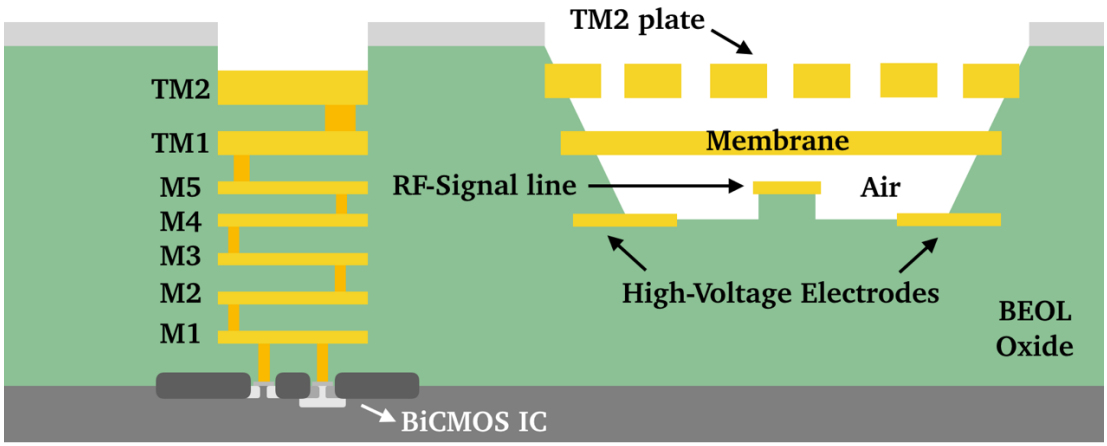


Fig. 2.4. RF-MEMS module of the SG13G2 BiCMOS-MEMS technology [18].

The fabricated RF-MEMS accomplish an insertion loss better than 0.67 dB and isolation better than 16 dB at all D-band [20]. The contact air capacitances C_{OFF} and C_{ON} are 9.8 and 211.6 fF respectively, nevertheless, these values can change due to

variations in the fabrication process, layers thickness and the mechanical behavior of the membrane (stress); the actuation voltage is 65 V.

A schematic top view and a scanning electron microscopy (SEM) image of the RF-MEMS switch before encapsulation is shown in Fig. 2.5.

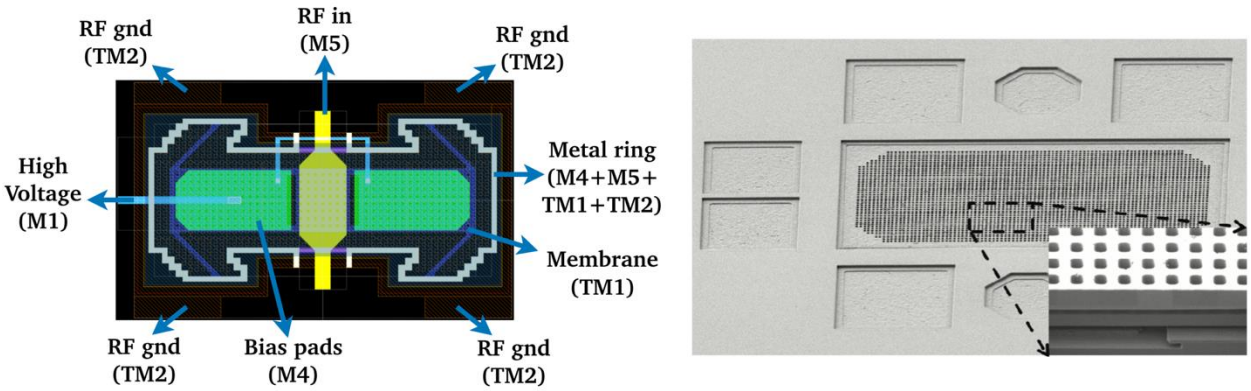


Fig. 2.5. Schematic top view of the embedded RF-MEMS switch (left) and SEM image of the RF-MEMS before encapsulation (right) [20].

2.4. Conclusions

Taking in consideration all the characteristics that offers the IHP's 0.13 µm SiGe:C BiCMOS technology, clearly it results ideal for the development of mm-wave devices for applications at D-band. Additionally, the embedded MEMS module that this technology offers, paves the way to the design of high-performance reconfigurable devices.

Several mm-wave devices have been reported in the literature using the IHP's SiGe BiCMOS technology. In [29] planar filters at 140 GHz using the IHP's SiGe BiCMOS technology is presented. In [30] a D-band power detector intended for passive imaging systems implemented with the IHP's SiGe BiCMOS technology is reported. LNAs with low-noise figure above 100 GHz have been also reported for this technology. In [31] a D-band LNA with a noise figure (F) below 6.1 dB across all the frequency band is presented. Also, some other applications have been demonstrated using the RF-MEMS module of the IHP's SiGe BiCMOS technology. In [2] a transmit-receive module for F-band is reported. The module uses a SPDT RF-MEMS switch to change from the transit to the receive path and vice versa. In addition to the applications mentioned above, some other have been already described in Chapter 1.

Due to its excellent performance for D-band applications, resulting low-noise figure for amplifiers, and the embedded RF-MEMS switch module being included in the design-kit library, the IHP's 0.13 µm SiGe BiCMOS technology is ideal for the applications intended for this Thesis.

CHAPTER THREE

MULTIMODAL CIRCUITS

In this chapter, the multimodal theory is studied and multimodal models for coupled microstrip and three-line microstrip structures are developed.

Some planar transmission lines contain more than one fundamental mode coexisting together. Usually some fundamental modes are considered spurious and some techniques have been developed to suppress them. However, these spurious modes can be exploited to develop compact and reconfigurable structures.

The study of models that predict the behavior of such multimodal structures is essential for the design of this kind of circuits. Performing the design of multimodal circuits using electromagnetic simulation tools provides accurate results, but it is very time-consuming. As an alternative, the multimodal models allow to design multimodal circuits in an easy way and less time-consuming. The multimodal models studied in this chapter will be used in Chapter 4, 5 and 6 for the design of reconfigurable circuits and compact matching networks.

3.1. Electromagnetic modes and planar transmission lines

An electromagnetic mode describes the pattern of the electric and magnetic field of a propagating electromagnetic wave. Depending on the geometry of the transmission structure, different types of modes are produced. Transmission lines that have two or more conductors may support transverse electromagnetic waves (TEM) and handle more than one mode.

Planar transmission lines have become the standard for the design of integrated microwave circuits. They have overcome other type of structures (like waveguide and coaxial) due to their low cost, compactness and high integration level with active components. Fig. 3.1 shows different types of planar transmission lines.

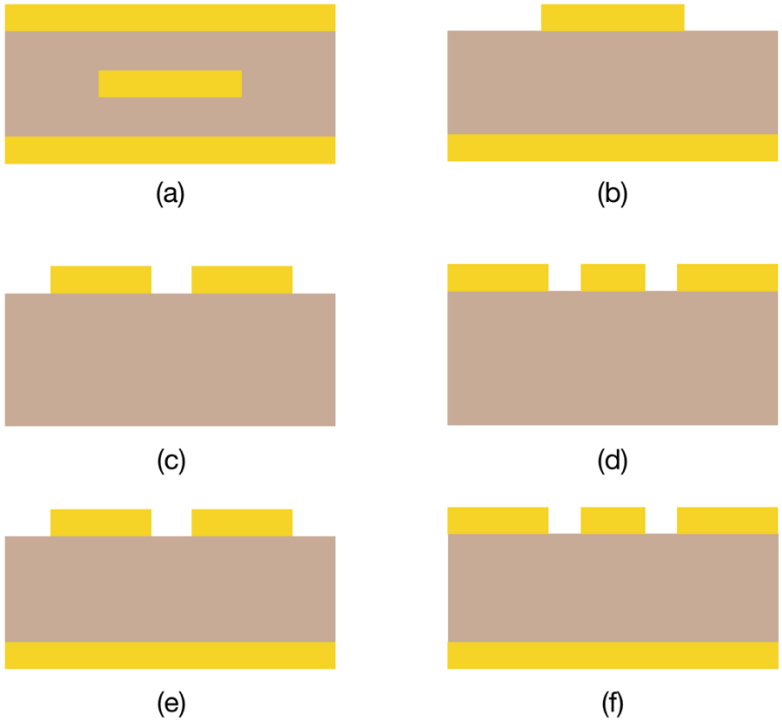


Fig. 3.1. Cross section of common planar transmission lines: (a) stripline, (b) microstrip, (c) coupled lines, (d) coplanar waveguide, (e) coupled line microstrip and (f) three-line microstrip.

Since stripline is fabricated inside a substrate (Fig. 3.1a), all the propagating waves are contained in the same dielectric (homogeneous medium), so it supports TEM waves. Other type of planar transmission lines like microstrip (Fig. 3.1b), coupled lines (Fig. 3.1c), coplanar waveguide (Fig. 3.1d), couple line microstrip (Fig. 3.1e) and TLM (Fig. 3.1f) are fabricated over a substrate, so a portion of the waves propagates in the dielectric region and the other one in the air region. This complicates the behavior of the energy and TEM waves are not supported by these planar lines. However, in most practical applications, the substrate used for planar transmission lines is very thin, so that the traveling waves behave almost as TEM waves (quasi-TEM) [32].

3.1.1. Microstrip line

The microstrip line (Fig. 3.2) is a planar transmission line composed of a single conductor (strip) fabricated over a dielectric substrate with a ground plane. Since the dielectric is inhomogenous (due the difference of air and dielectric relative permittivity ε_0 and ε_r), the fields are quasi-TEM. The microstrip line is characterized by a propagation constant and a characteristic impedance. The microstrip line is considered a mono-modal line, since the waves only propagate with one pattern (shown in Fig. 3.2).

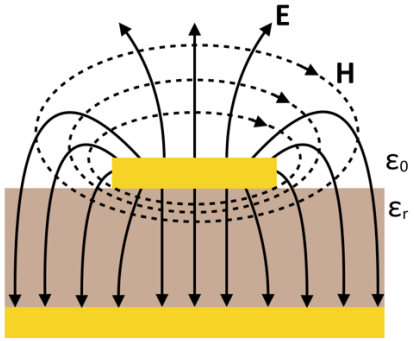


Fig. 3.2. Electromagnetic field pattern of a microstrip line.

3.1.2. Coupled microstrip line

The coupled microstrip line is a planar transmission line that is composed of two strips fabricated on a dielectric substrate with a ground plane (Fig. 3.1e). The electromagnetic field contained in the coupled microstrip line is quasi-TEM and can be propagated in two fundamental modes called the even mode and the odd mode. In the even mode, the voltage is defined between the two strips and the ground plane, and in the odd mode it is defined from one strip to the other one. Each mode is characterized by a propagation constant and a characteristic impedance. Fig. 3.3 shows the electromagnetic field pattern of the coupled microstrip line.

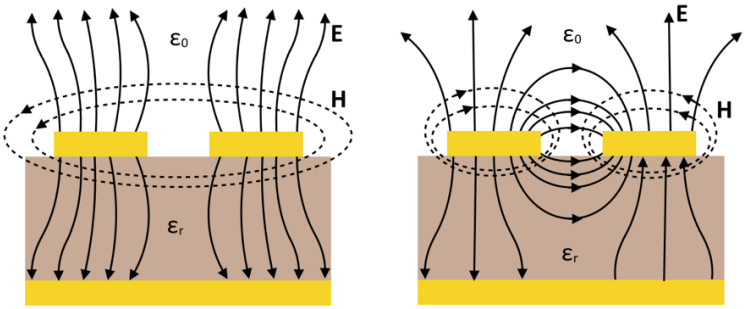


Fig. 3.3. Electromagnetic field of the even (left) and odd mode (right) of the coupled microstrip line.

The even and odd modes may be generated simultaneously in the coupled microstrip line; therefore, the resulting wave will be a superposition of both modes. Fig. 3.4 shows the voltage and current definition for the even and odd modes in the coupled microstrip line. While I_{1e} and I_{1o} are the even- and odd-mode currents propagating through strip 1, I_{2e} and I_{2o} are the even- and odd-mode currents propagating through strip 2. V_{1e} and V_{1o} are the even- and odd-mode voltages between strip 1 and ground plane, while V_{2e} and V_{2o} are the even- and odd-mode voltages between strip 2 and ground plane; V_o is the odd-mode voltage between strips 1 and 2 (this is only true for the odd mode). The even mode drives current in both strips in the same direction, and the voltage travels between the ground and the two strips. The odd mode drives current in both strips but in the opposite direction, and the voltage travels from one strip to the other one [33].

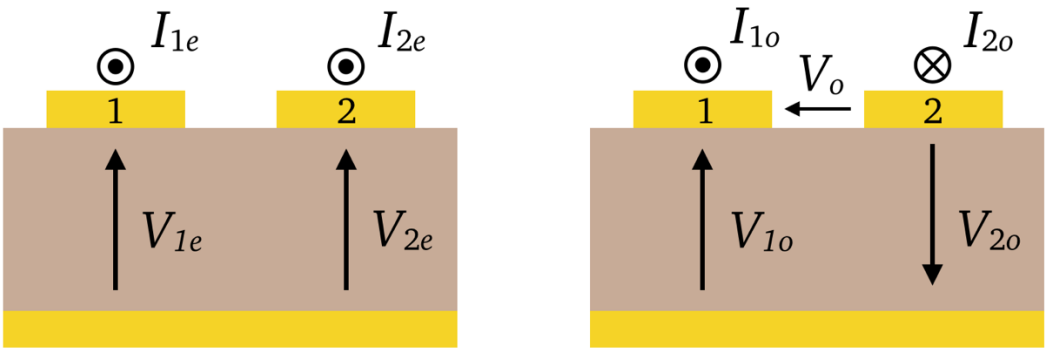


Fig. 3.4. Voltage and current definitions for the even (left) and odd mode (right) of the coupled microstrip line.

3.1.3. Three-line microstrip

The three-line microstrip (TLM) is a planar transmission line composed of three parallel strips fabricated over a dielectric substrate with a ground plane (Fig. 3.1f). The electromagnetic field propagates in three fundamental modes: the *oo* mode (similar to the CPW even mode) which is quasi-TEM, the *oe* mode (similar to the CPW odd mode) which is no-TEM and the *ee* mode (similar to the microstrip mode) which is quasi-TEM. The three fundamental modes may be generated simultaneously in the TLM; therefore, the resulting wave will be a superposition of the three modes. Each mode is characterized by a propagation constant and characteristic impedance.

Fig. 3.5 shows the electromagnetic pattern and the voltage/current definitions for the three fundamental modes of a symmetric TLM. I_{1ee}, I_{1oo} and I_{1oe} are the microstrip-, even- and odd-mode current propagating through strip 1. The even-, odd- and microstrip-mode currents traveling through strip 2 and 3 are I_{2oo}, I_{2oe}, I_{2ee} and I_{3oo}, I_{3oe} and I_{3oo}, respectively. While V_{1oo}, V_{1oe}, and V_{1ee} are the even-, odd- and microstrip-mode voltage between ground plane and strip 1, V_{3oo}, V_{3oe} and V_{3ee} are the even-, odd- and microstrip-mode voltages between ground plane and strip 3; V_{2oo}, and

V_{2ee} are the even- and microstrip-mode voltages between ground plane and strip 2. In the *oo* mode, the voltage is defined between the three strips and ground plane, and the current flows through the central strip and returns through the outer strips (Fig. 3.5a). Concerning the *oe* mode, the voltages are defined between the outer strips and the ground plane (Fig. 3.5b). In this case, the current flows through one of the outer strips and returns through the other one. With respect to the *ee* mode, the voltages are defined between the three strips and the ground plane (Fig. 3.5c); the current flows through the three strips and returns through the ground plane [27][28].

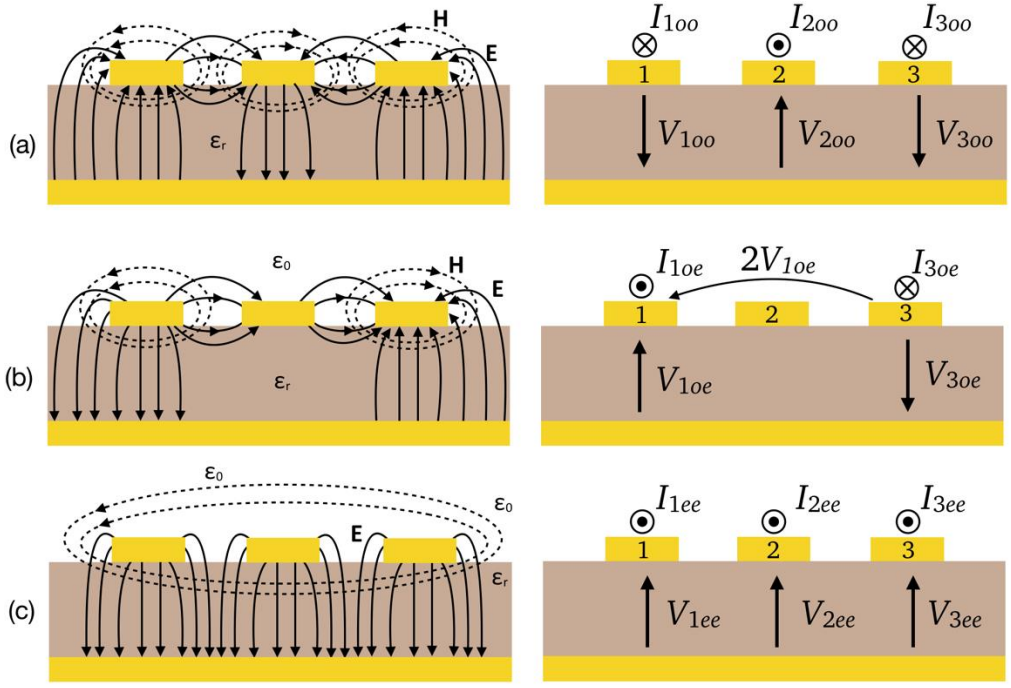


Fig. 3.5. Electromagnetic field pattern (left) and voltage/current definitions (right) of the *oo* mode (a), *oe* mode (b) and *ee* mode (c) of the TLM.

3.2. Coupled microstrip line multimodal models

The two fundamental modes on a coupled microstrip line will interact with each other in asymmetries and transitions. Considering these interactions, multimodal models have been proposed to study the behavior of coupled microstrip line structures. In this Section, these models are applied to several coupled microstrip line transitions that will be used to implement multimodal tuners (Chapter 4) and matching networks (Chapter 5). In order to develop the multimodal models, a relationship between the even- and odd-mode currents/voltages and the physical (circuit) currents/voltages is obtained in the next subsection.

3.2.1. Coupled microstrip line circuit-modal model

The currents and voltages shown in Fig. 3.4 are portions of the total even- and odd-mode currents and voltages. If both strips of the coupled microstrip line have the same width, the structure is symmetric and for the even mode, $I_{1e} = I_{2e} = \frac{1}{2}I_e$, where I_e is the total even-mode current. Concerning the voltage, it is defined as $V_{1e} = V_{2e} = V_e$, where V_e is the total even-mode voltage. With respect to the odd mode, the current is defined as $I_{1o} = I_{2o} = I_o$, where I_o is the total odd-mode current. The voltage is defined as $V_{1o} = V_{2o} = \frac{1}{2}V_o$, where V_o is the total odd-mode voltage. Considering these definitions, a relationship between modal and circuit currents and voltages can be obtained as shown in Fig. 3.6. While I_1 and I_2 are the circuit currents, V_1 and V_2 are the circuit voltages.

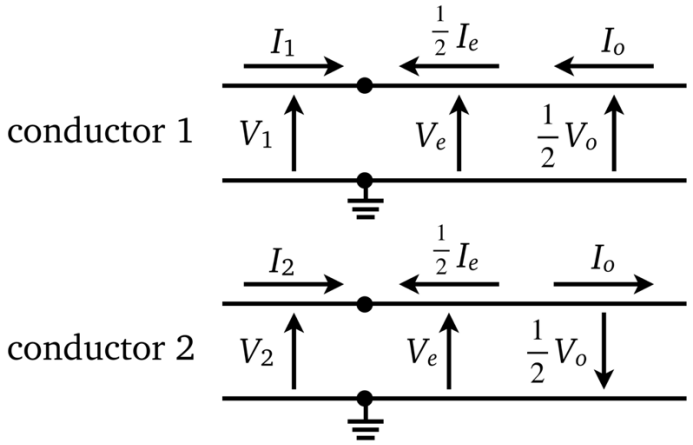


Fig. 3.6. Modal and circuit currents and voltages definitions of the symmetric coupled microstrip line.

The equations that describe the relationship of modal and circuit currents and voltages are obtained from the analysis of Fig. 3.6:

$$I_1 = -\frac{I_e}{2} - I_o \tag{1}$$

$$I_2 = -\frac{I_e}{2} + I_o \tag{2}$$

$$V_e = \frac{V_2}{2} + \frac{V_1}{2} \tag{3}$$

$$V_o = V_1 - V_2 \tag{4}$$

Based on these equations, a coupled microstrip line multimodal model is implemented (Fig. 3.7). This model can perform a circuit-modal transformation of currents and voltages, and since the above equations are all linear, transformers are used to maintain the circuit and modal currents equivalence. While ports 1 and 2 are the physical ports, ports 3 and 4 are the multimodal ports. Z_e and Z_o are the even- and odd-mode characteristic impedances and β_e and β_o are the even- and odd-mode phase constants.

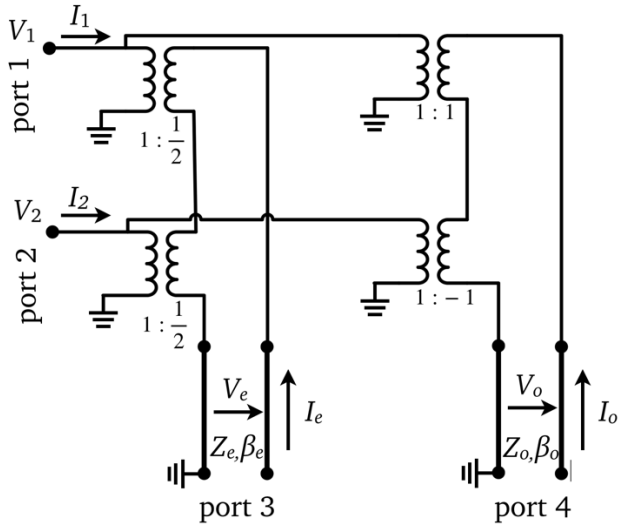


Fig. 3.7. Coupled microstrip line circuit-modal model.

This obtained general model can be seen as a particular case of the model proposed in [16], and used for the analysis of a wide set of coupled microstrip line transitions. Also, simpler models for each of those transitions can be derived from this model as will be shown in the following subsections.

3.2.2. Coupled microstrip line modal characteristic impedances and phase constants

The modal characteristic impedances (Z_e and Z_o) and phase constants (β_e and β_o) of the coupled microstrip line are obtained using the method described in [36]. A touchstone file is obtained from a 4-port electromagnetic analysis of the coupled microstrip line using Agilent Momentum, and a MATLAB routine is used to obtain the modal characteristics. Fig. 3.8 shows the simulated coupled microstrip line structure. The simulated frequency range is 1 to 200 GHz using the IHP's SG13G2 substrate described in Chapter 2 (Fig. 2.3). The TM2 layer is used for the coupled microstrip line metallization and Metal1 is used as ground plane.

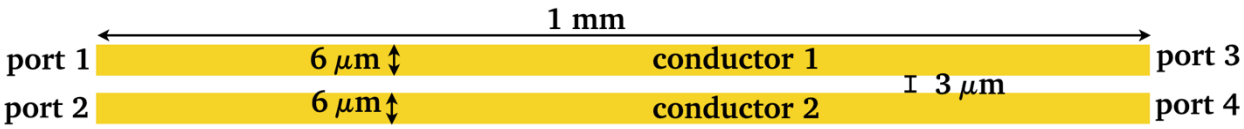


Fig. 3.8. Simulated coupled microstrip line structure.

Fig. 3.9 shows the modal characteristic impedances and the phase constants obtained. The even- and odd-mode characteristic impedances are 103 and 33 Ω respectively, and the constant phases are 40.17° and 41.65° for the even- and odd-mode respectively (calculated at 1 GHz).

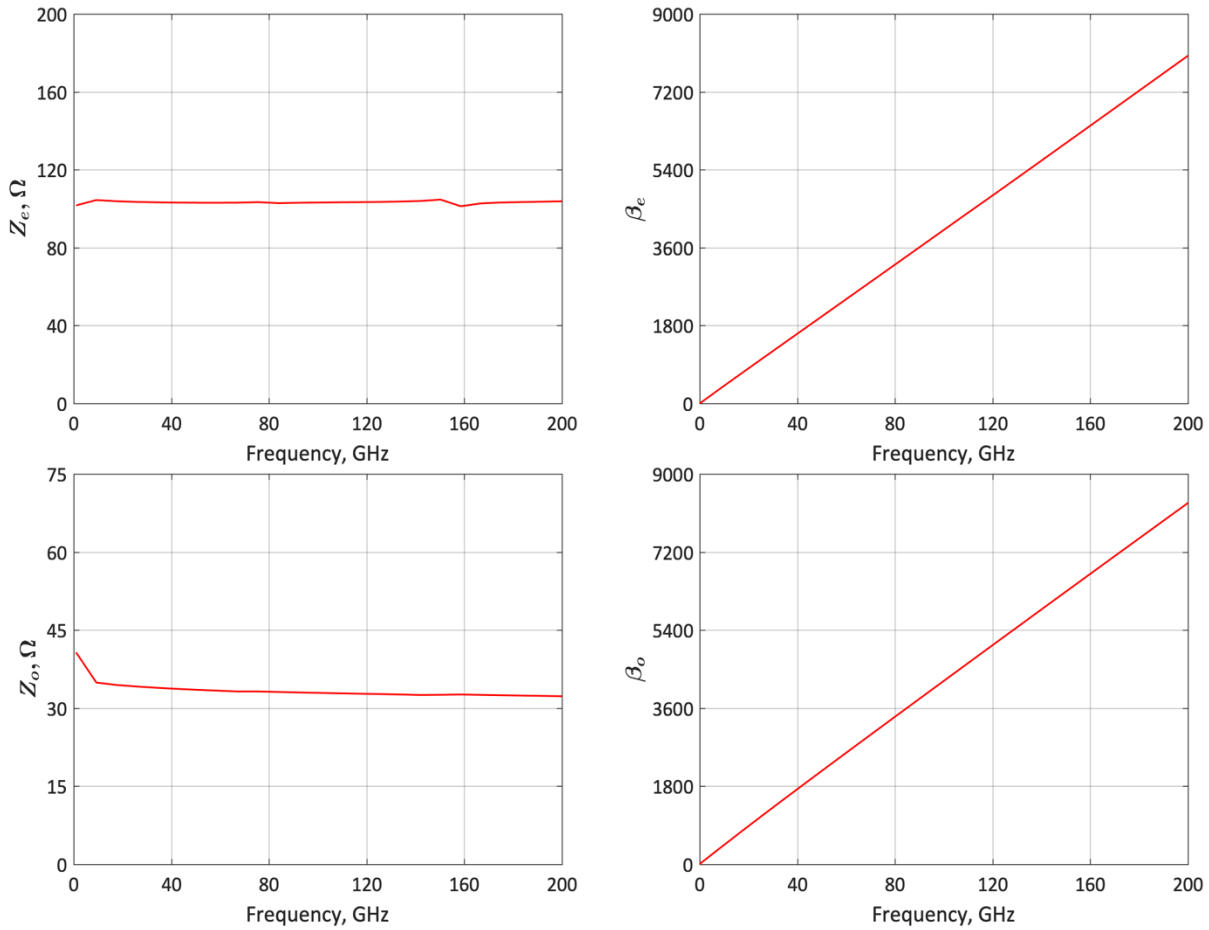


Fig. 3.9. Modal characteristic impedances (left) and constant phases (right) of the coupled microstrip line structure.

3.2.3. Microstrip-coupled microstrip line transition model

The microstrip-coupled microstrip line transition is composed by a microstrip line connected to both strips of a coupled microstrip line structure. Fig. 3.10 shows the top view of the microstrip-coupled microstrip line transition; the microstrip and

coupled microstrip lines have a bottom ground plane. Since the two strips of the coupled microstrip line are connected to the microstrip line, the voltage is the same in both of them suppressing the odd mode in this transition.

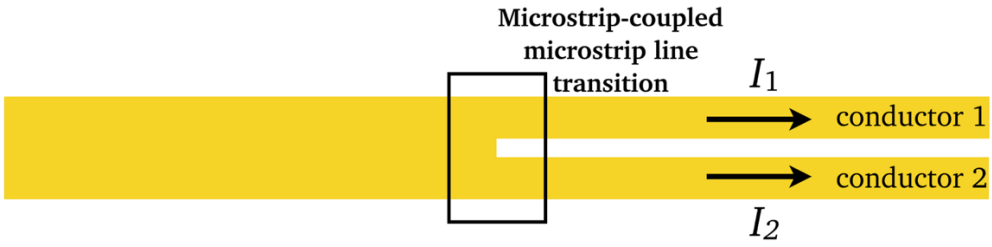


Fig. 3.10. Top view of the microstrip-coupled microstrip line transition.

Using the circuit-modal model of Fig. 3.7, a multimodal model for the microstrip-coupled microstrip line transition can be obtained. As shown in Fig. 3.11 the two physical ports of the circuit-modal (port 1 and 2) model are connected to each other resulting in a single physical port to which the microstrip line section is connected. The resulting model allows the analysis of interaction and energy exchange between the microstrip mode and the coupled microstrip modes.

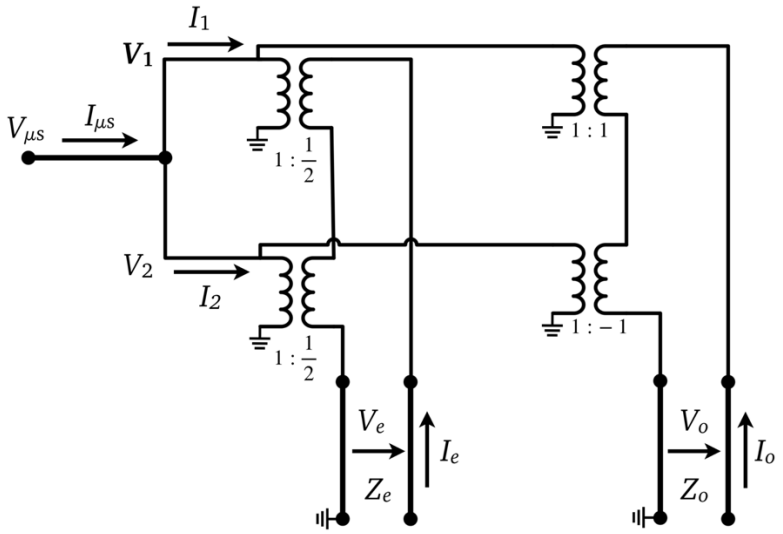


Fig. 3.11. Coupled microstrip line circuit-modal model connected to a microstrip line.

The relationship between modal and circuit currents and voltages is described by the following equations obtained from the analysis of Fig. 3.11:

$$I_{\mu s} = -I_e \tag{5}$$

$$V_e = V_{\mu s} \tag{6}$$

$$V_o = 0 \tag{7}$$

These equations are used to implement a microstrip-coupled microstrip line multimodal model as shown in Fig. 3.12 [33]. $Z_{\mu s}$ is the characteristic impedance of the microstrip line.

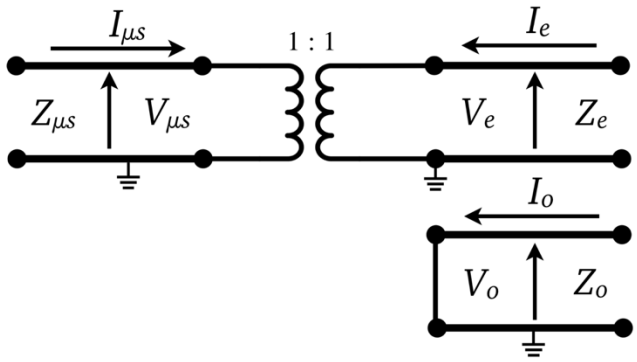


Fig. 3.12. Microstrip-coupled microstrip line transition model.

3.2.4. Coupled microstrip line asymmetric series impedance transition model

The coupled microstrip line asymmetric series impedance transition is composed of a coupled microstrip line to which a series impedance has been connected in each strip (Fig. 3.13). In a general case the two series impedances are different thus producing an interaction between the even and odd mode. The multimodal model developed for this transition takes in consideration the energy exchange between modes produced by the impedances [33].

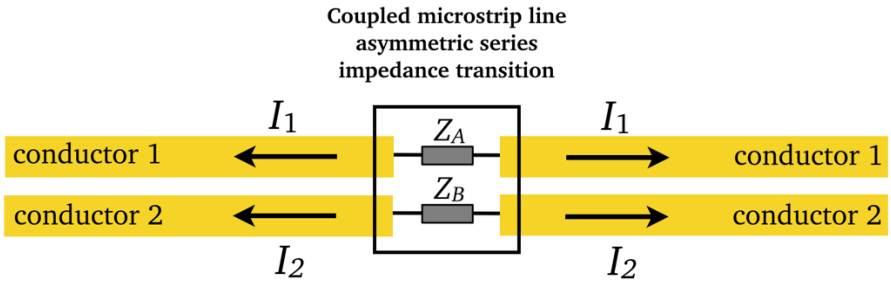


Fig. 3.13. Top view of the coupled microstrip line asymmetric series impedance transition.

Using the circuit-modal model of Fig. 3.7 and an analytical procedure similar to the one shown in subsection 3.2.3, the multimodal model for the series impedance transition can be obtained as shown in Fig. 3.14 [33]. An all-modal-ports model allows to easily connect in cascade other transition models.

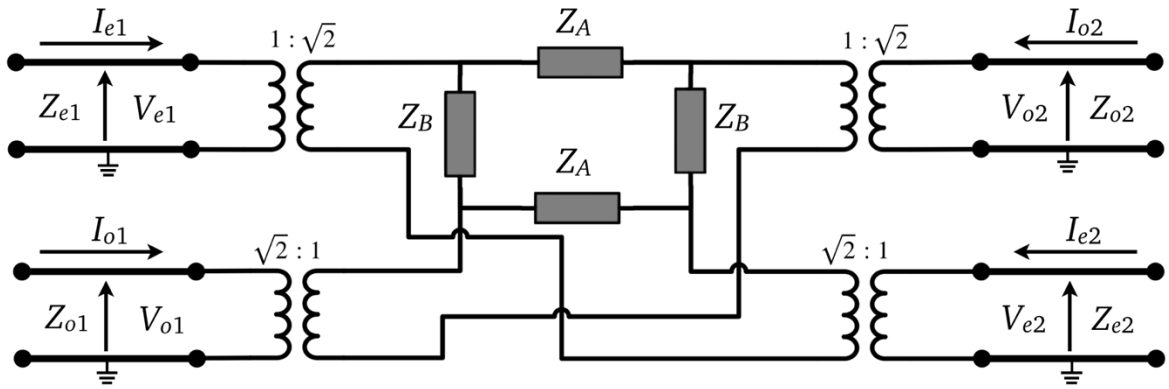


Fig. 3.14. Coupled microstrip line asymmetric series impedance transition model.

3.2.5. Coupled microstrip line asymmetric shunt impedances transition model

The coupled microstrip line asymmetric shunt impedance transition consists of two shunt impedances connected between the two strips and ground plane of a coupled microstrip line (Fig. 3.15). In a general case the two impedances are different thus producing an interaction between the even and odd modes.

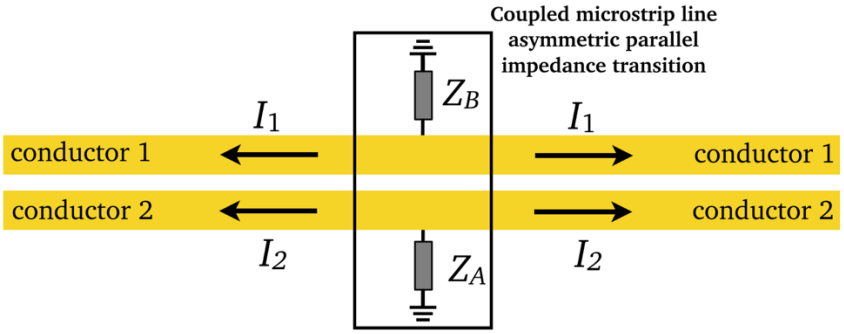


Fig. 3.15. Top view of the coupled microstrip line asymmetric shunt impedance transition.

As it was done with the previous transitions, the multimodal model of the shunt impedance transition can be obtained using the circuit-modal model of Fig. 3.7 and an analytical procedure similar to the one illustrated in subsection 3.2.3, as shown in Fig. 3.16 [33] [37]. The model allows the analysis of interaction and energy exchange between the coupled microstrip modes produced by the shunt impedances. As it was mentioned before, an all-modal-ports model allows to easily connect in cascade other transition models.

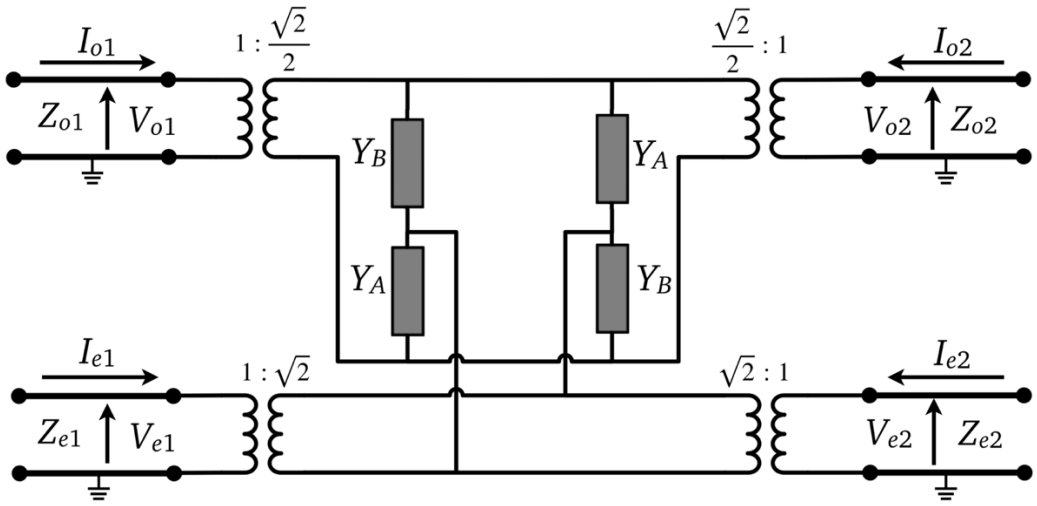


Fig. 3.16. Coupled microstrip line asymmetric shunt impedances transition model.

3.3. Three-line microstrip multimodal models

In this Section, multimodal models for TLM structures have been studied. The obtained multimodal models of the TLM structures show good agreement when compared to its electromagnetic simulation counterpart; they can be used for the analysis and design of complex multimodal circuit.

As explained before, the fundamental modes of the TLM will interact with each other in asymmetries and transitions, and multimodal models can be proposed to study their behavior. The *oo*-, *oe*- and *ee*-modes total currents/voltages can be analyzed to achieve a model that describes their interaction with the physical (circuit) currents\voltages.

3.3.1. Three-line microstrip circuit-modal model

In order to obtain a model able to perform a circuit-modal transformation, the *oo*-, *oe*- and *ee*-mode currents/voltages of a TLM are analyzed. The currents/voltages shown in Fig. 3.5 are portions of the total *oo*-, *oe*- and *ee*-mode currents/voltages. In the case of a symmetric TLM structure (same outer-strip width) the modal currents propagating through the outer strips will be the same for each mode ($I_{1oo} = I_{3oo} = \frac{x}{x+y} I_{oo}$, $I_{1oe} = I_{3oe} = I_{oe}$ and $I_{1ee} = I_{3ee} = \frac{1}{2}\frac{y}{x+y} I_{ee}$,) and the central strip currents will be defined as $I_{2oo} = \frac{1}{2}\frac{1}{x+y} I_{oo}$ and $I_{2ee} = \frac{1}{x+y} I_{ee}$. Concerning the voltages, they will be the same in each outer strip for each mode ($V_{1oo} = V_{3oo} = \frac{1}{2} V_{oo}$, $V_{1oe} = V_{3oe} = \frac{1}{2} V_{oe}$ and $V_{1ee} = V_{3ee} = V_{ee}$) and for the central strip the voltages will be defined as $V_{1oo} = \frac{y}{2} V_{oo}$ and $V_{1ee} = x V_{ee}$. The x and y parameters describe the relationship of voltages/currents traveling through the outer strips (strips 1 and 3) with those propagating through

the central strips [38]. Using these definitions and the diagram shown in Fig. 3.5, a relationship between circuit and modal currents/voltages can be obtained as shown in Fig. 3.17. While I_1, I_2 and I_3 are the physical currents, V_1, V_2 and V_3 are the physical voltages of each strip. Concerning the modal characteristics, I_{oo}, I_{oe} and I_{ee} are the modal currents, while V_{oo}, V_{oe} and V_{ee} are the modal voltages.

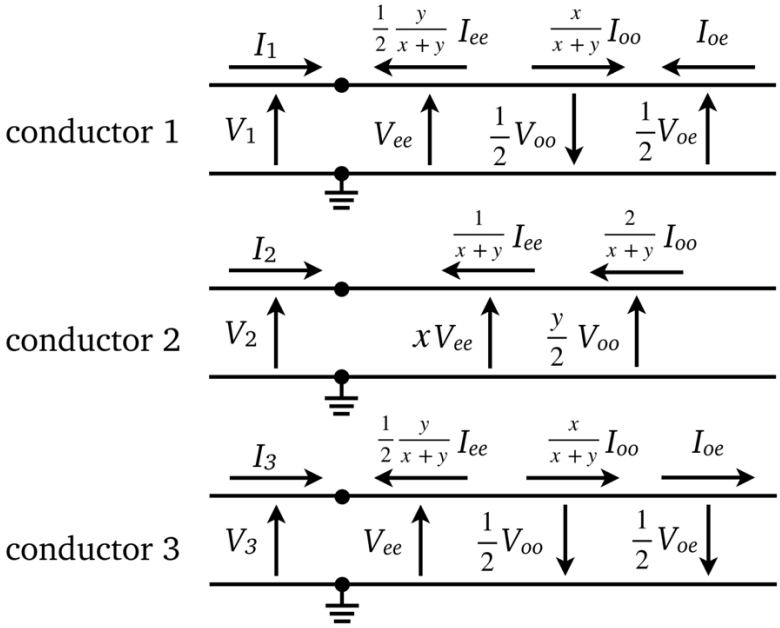


Fig. 3.17. Modal and circuit currents/voltages definitions of a TLM.

The relationship between modal and circuit currents/voltages is described by the following equations obtained from the Kirchhoff analysis of Fig. 3.17:

$$I_1 = -\frac{1}{2}\frac{y}{x+y}I_{ee} + \frac{x}{x+y}I_{oo} - I_{oe} \tag{8}$$

$$I_2 = -\frac{1}{x+y}I_{ee} - \frac{2}{x+y}I_{oo} \tag{9}$$

$$I_3 = -\frac{1}{2}\frac{y}{x+y}I_{ee} + \frac{x}{x+y}I_{oo} + I_{oe} \tag{10}$$

$$V_{oo} = -\frac{x}{x+y}V_1 + \frac{2}{x+y}V_2 - \frac{x}{x+y}V_3 \tag{11}$$

$$V_{oe} = V_1 - V_3 \tag{12}$$

$$V_{ee} = \frac{1}{2}\frac{y}{x+y}V_1 + \frac{1}{x+y}V_2 + \frac{1}{2}\frac{y}{x+y}V_3 \tag{13}$$

A circuit-modal transformation model is implemented using these equations as shown in Fig. 3.18. While port 1, 2 and 3 are the physical ports, ports 4, 5 and 6 are the multimodal ports. Z_{oo}, Z_{oe} and Z_{ee} are the modal characteristic impedances; β_{oo}, β_{oe} and β_{ee}, are the constant phases. This model transforms physical currents/voltages of the TLM into their modal counterpart; it also can be used to obtain other TLM transitions and asymmetries models.

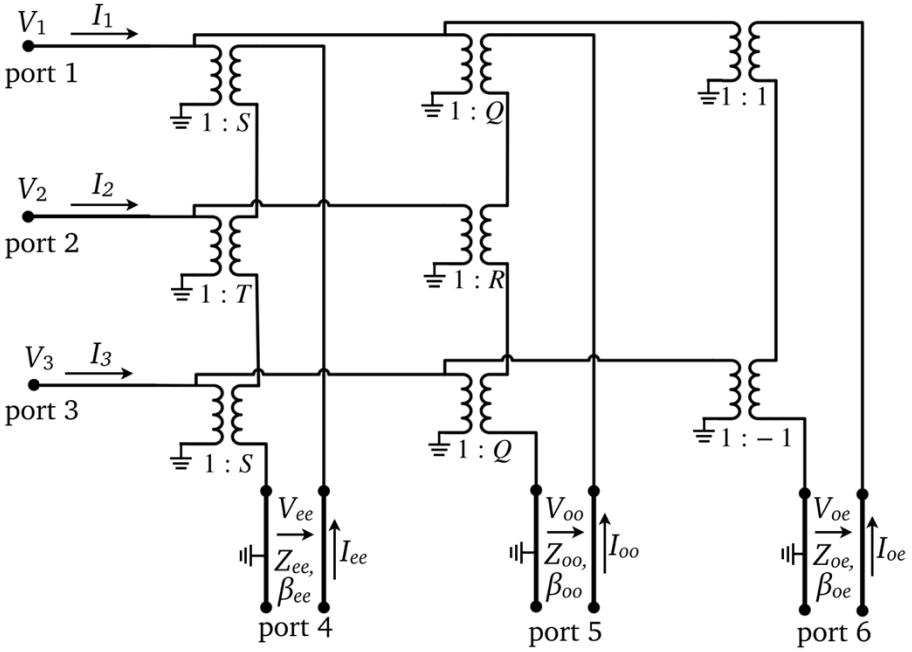


Fig. 3.18. Circuit-modal model of the TLM.

The parameters Q, R, S and T (transformer ratios in Fig. 3.18) are defined as follows:

$$Q = -\frac{x}{x+y} \tag{14}$$

$$R = \frac{2}{x+y} \tag{15}$$

$$S = \frac{1}{2}\frac{y}{x+y} \tag{16}$$

$$T = \frac{1}{x+y} \tag{17}$$

This general model can be seen as a particular case of the model proposed in [16], and used for the analysis of a wide set of coupled microstrip line transitions. Also, simpler models for each of those transitions can be derived from this model as will be shown in the following subsections.

3.3.2. Three-line microstrip modal characteristic impedances and phase constants

The modal characteristic impedances (Z_{oo}, Z_{oe} and Z_{ee}) and phase constants (β_{oo}, β_{oe} and β_{ee}) of the TLM are obtained using the method described in [38]. A MATLAB routine is applied to a touchstone file obtained from a 6-port electromagnetic analysis using Agilent Momentum and the modal characteristics are obtained. Fig. 3.19 shows the simulated coupled microstrip line structure. The IHP's SG13G2 substrate described in Chapter 2 (Fig. 2.3) is used for the simulation of the TLM; the TopMetal2 layer is used as the metallization of the lines and Metal1 is used as ground plane. The simulated frequency range is 1 to 200 GHz.

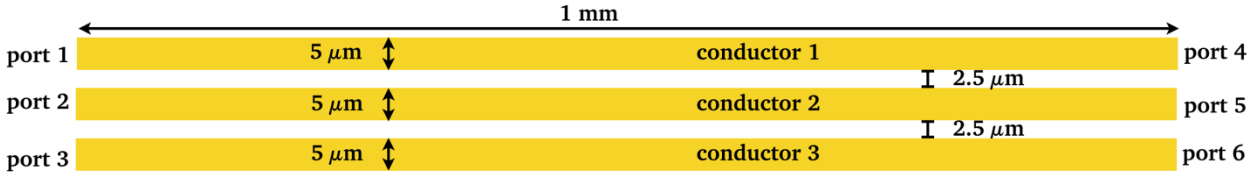


Fig. 3.19. Simulated TLM.

Fig. 3.20, 3.21 and 3.22 show the modal characteristic impedances and constant phases for the *oo*, *oe* and *ee* modes obtained. The *x* and *y* parameters, characteristic impedances and constant phases are shown in Table 3.1 (the phase constants are calculated at 1 GHz).

Table 3.1. Modal characteristics of the TLM.

Modal characteristics	Value
Z_{oo}	21.85 Ω
Z_{oe}	47.03 Ω
Z_{ee}	126.8 Ω
β_{oo}	43.35°
β_{oo}	41.28°
β_{oo}	40.25°
x	1.07
y	2.29

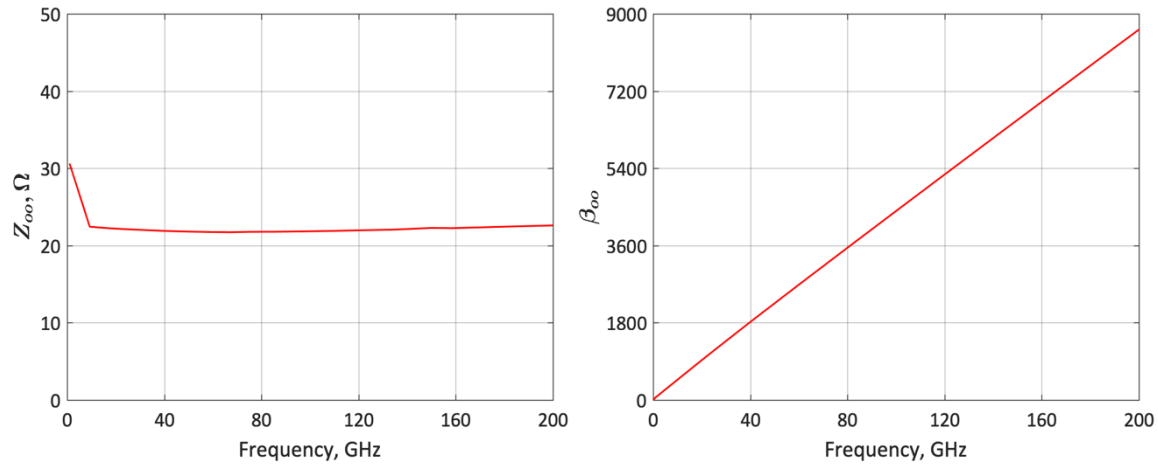


Fig. 3.20. Characteristic impedance (left) and phase constant (right) for the TLM *oo* mode.

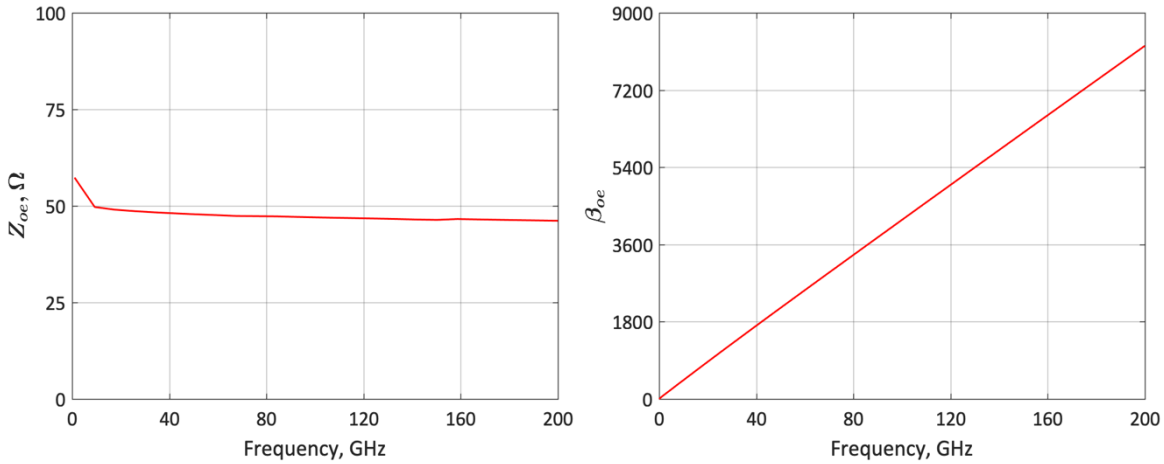


Fig. 3.21. Characteristic impedance (left) and phase constant (right) for the TLM *oe* mode.

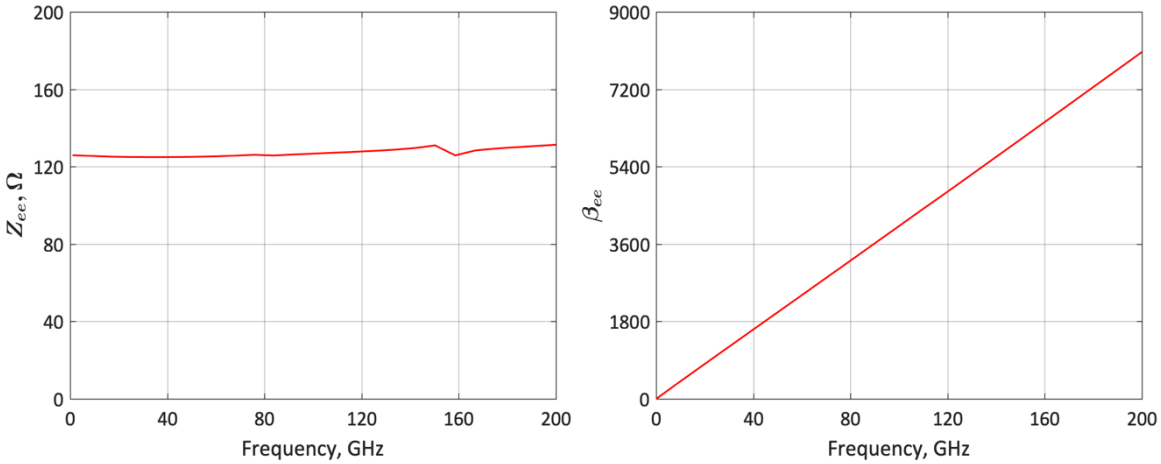


Fig. 3.22. Characteristic impedance (left) and phase constant (right) for the TLM *ee* mode.

3.3.3. Microstrip-TLM transition model

The microstrip-TLM transition is composed of a microstrip line connected to a TLM section as shown in Fig. 3.23. Since the three strips of the TLM are connected together, the voltage is the same, thus suppressing the *oe* mode (similarly to the microstrip-coupled microstrip line transition). The *oo* and *ee* modes still coexist and the way they interact is determined by the transition. A multimodal model developed for this transition needs to take in consideration these interactions.

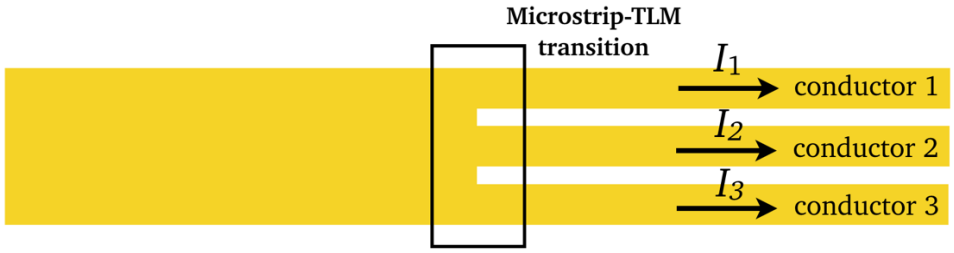


Fig. 3.23. Microstrip-TLM transition.

The circuit-modal model obtained in Fig. 3.18 is used to obtain the microstrip-TLM transition model. The physical ports of the model (ports 1, 2 and 3) are connected together using a microstrip line section as shown in Fig. 3.24. The resulting model allows an analysis of interaction between the microstrip line mode and the modes of the TLM structure. It transforms the physical current ($I_{\mu s}$) and voltage ($V_{\mu s}$) of the microstrip line into modal current and voltages.

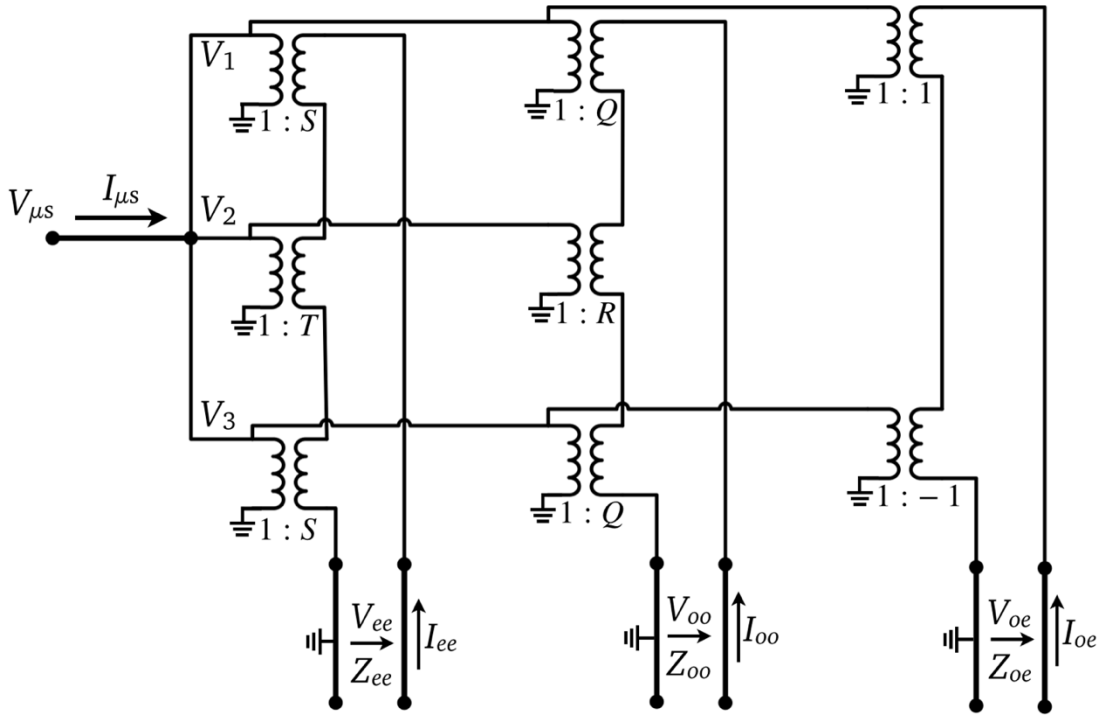


Fig. 3.24. TLM circuit-modal model connected to a microstrip line.

The circuit-modal model from Fig. 3.24 is analyzed in order to obtain a simpler circuit model topology, and the equations that describe the interaction of the modal currents and voltages are obtained:

$$I_{\mu s} = -\frac{y+1}{x+y} I_{ee} - 2\frac{1-x}{x+y} I_{oo} \tag{18}$$

$$V_{oo} = 2\frac{1-x}{x+y} V_{\mu s} \tag{19}$$

$$V_{oe} = 0 \tag{20}$$

$$V_{ee} = \frac{y+1}{x+y} V_{\mu s} \tag{21}$$

The microstrip-TLM multimodal model is implemented using the above equations as shown in Fig. 3.25 [34][39]. $Z_{\mu s}$ is the characteristic impedance of the microstrip line. As it was mention before, the *oe* mode is suppressed, so that the odd-mode line section is connected to ground. An all-modal-ports model allows to easily connect in cascade other transition models.

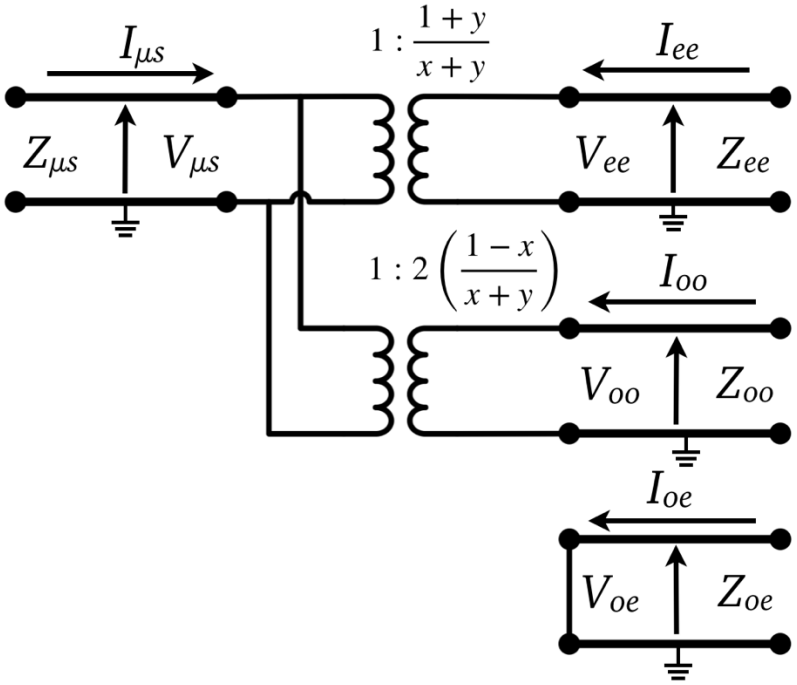


Fig. 3.25. Microstrip-TLM multimodal model.

3.3.4. TLM asymmetric-outer strip series impedance transition model

The TLM asymmetric-outer strip series impedance transition consists of a TLM to which a series impedance has been connected in each outer strip (Fig. 3.26). In a general case the two series impedances are different thus producing an interaction between the even, odd and microstrip modes. The multimodal model developed for this transition takes in consideration the energy exchange between modes produced by the presence of the impedances in the structure.

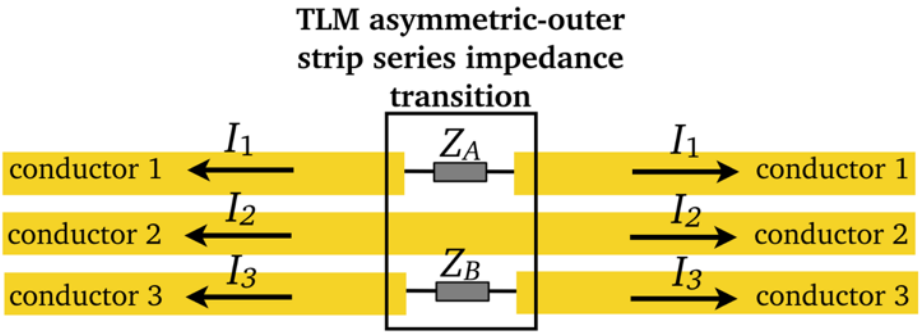


Fig. 3.26. Top view of the TLM asymmetric-outer strip series impedance transition.

In order to obtain the multimodal model of the series impedance transition, a similar analysis performed in subsection 3.3.3 using the circuit-modal model shown in Fig. 3.18 is implemented. The series impedances Z_A and Z_B are connected to the physical ports of two circuit-modal TLM models and the complete model is obtained as shown in Fig. 3.27 [34][39].

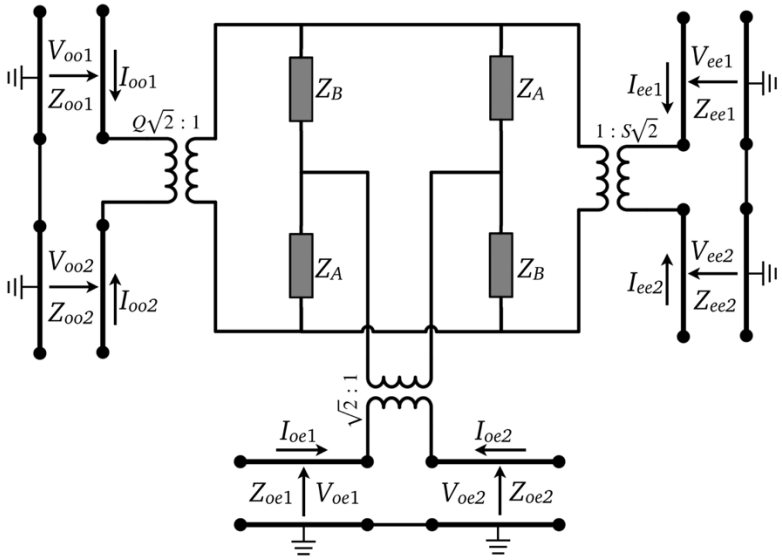


Fig. 3.27. TLM asymmetric-outer strip series impedance transition model.

3.3.5. TLM asymmetric-outer strip shunt impedance transition model

The TLM asymmetric-outer strip shunt impedance transition is composed of two shunt impedances connected between the two outer strips and the ground plane of the TLM (Fig. 3.28). In a general case the two parallel impedances are different thus producing an interaction between even, odd and microstrip modes. The multimodal model developed for this transition takes in consideration the energy exchange between modes produced by the presence of the impedances in the structure.

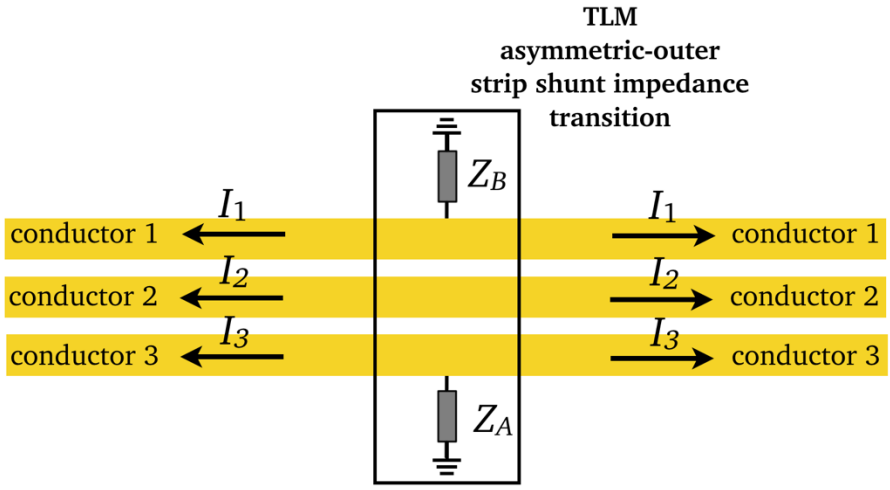


Fig. 3.28. Top view of the TLM asymmetric-outer strip shunt impedance transition.

In the same way as it was done for previous models, a similar analysis performed in subsection 3.3.3 using the TLM circuit-modal model of Fig. 3.18 is used to obtain que TLM shunt impedance model of Fig. 3.29 [34][39]. An all-modal-ports model allows to easily connect in cascade other transition models.

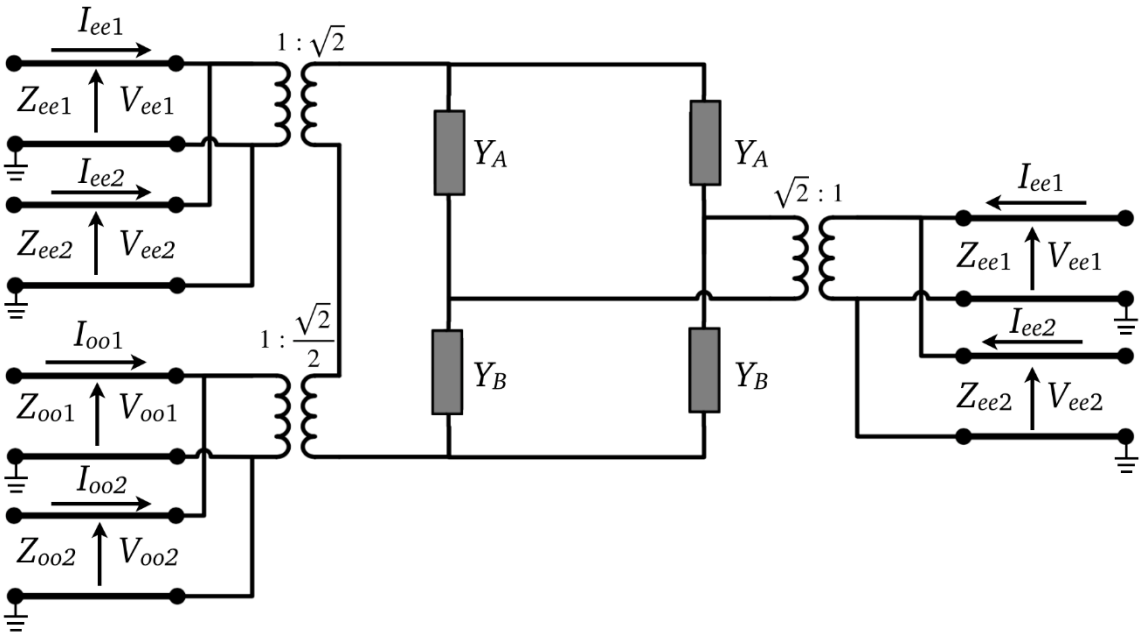


Fig. 3.29. TLM asymmetric-outer strip shunt impedance transition model.

3.3.6. TLM asymmetric-central shunt impedances model

The TLM asymmetric-central shunt impedances transition consists of a TLM to which two impedances have been connected between the outer strips and the central strip as shown in Fig. 3.30. In a general case the two parallel impedances Z_A and Z_B are different thus producing an interaction between the *oo*, *oe* and *ee* modes. The multimodal model developed for this transition takes in consideration the energy exchange between modes produced by the presence of the impedances in the structure.

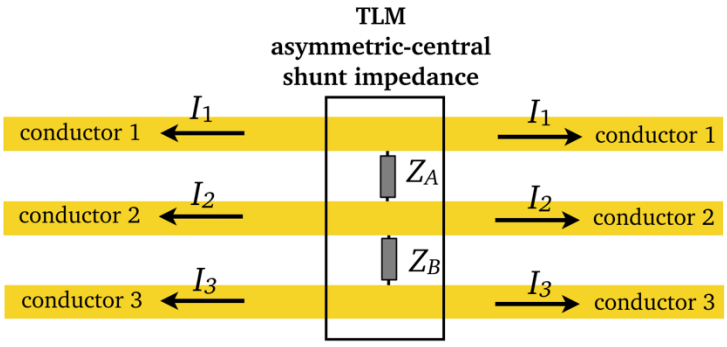


Fig. 3.30. Top view of the TLM asymmetric-central shunt impedances transition.

In the same way as it was done for previous models, a similar analysis performed in subsection 3.3.3 using the circuit-modal model shown in Fig. 3.18 is implemented to obtain the TLM central shunt impedance model of Fig. 3.31 [39]. As

it was mentioned before, an all-modal-ports model allows to easily connect in cascade other transition models.

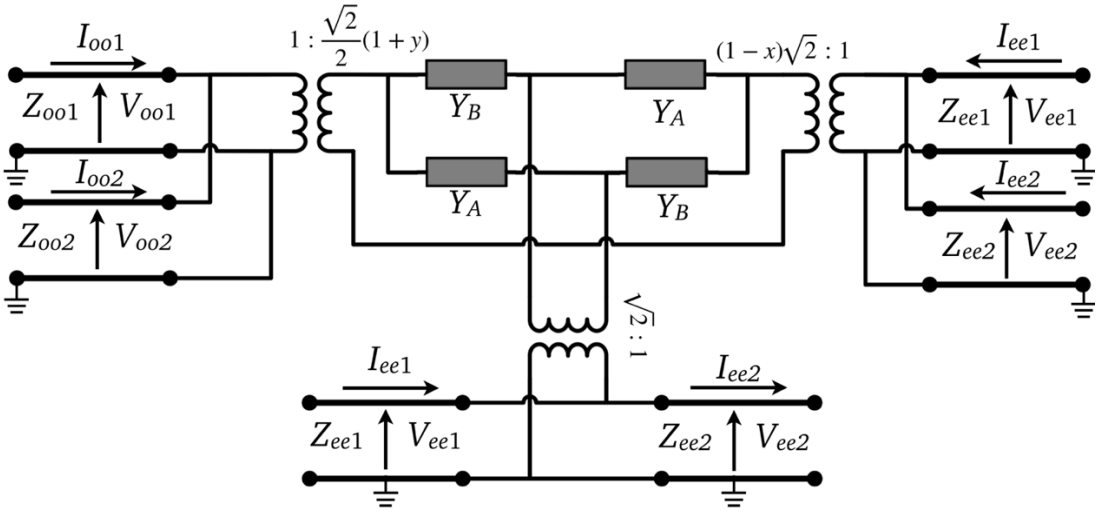


Fig. 3.31. TLM asymmetric-central shunt impedance transition model.

3.4. Fabrication and analysis of TLM structures

The developed multimodal models can be used for the design of complex multimodal coupled microstrip and TLM structures. In this Section, the proposed TLM structure shown in Fig. 3.32 is analyzed in order to obtain a multimodal model.

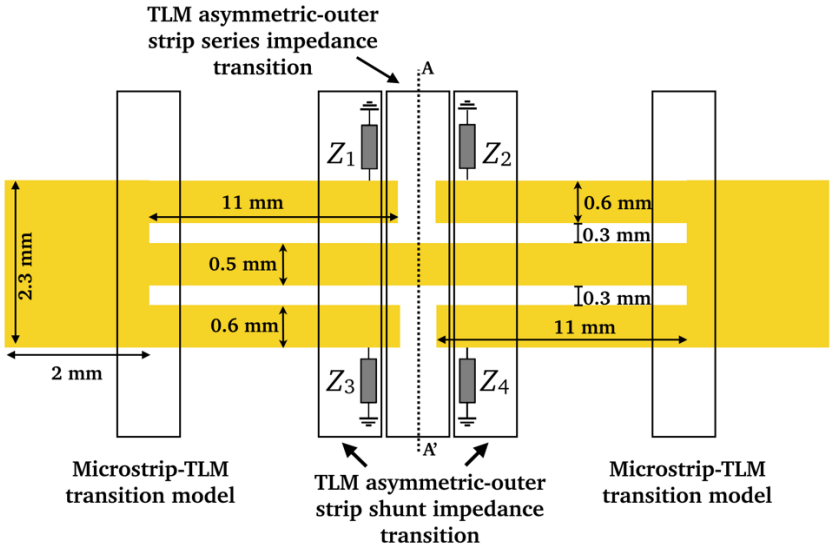


Fig. 3.32. Studied TLM multimodal structure.

Next, the structure is fabricated on a Rogers 4003 substrate with ε_r = 3.55, h = 0.81 mm and tan(δ)=0.0022. The simulated $|S_{11}|$ and $|S_{21}|$ obtained from multimodal

model are compared to the measurements of the fabricated structure in order to validate the multimodal circuit model.

3.4.1. Multimodal model of the proposed TLM structure

The structure shown in Fig. 3.32 involve several transitions already studied which can be easily identified. From left to right, a microstrip section is followed by a microstrip-TLM transition. A TLM section and a TLM asymmetric-outer strip shunt impedance transition follow. Next, in the center of the structure a TLM asymmetric outer-strip series impedance transition follows. The second half of the TLM structure consists of the same transition topology described before using vertical symmetry with respect to the AA' axis.

The multimodal models for the described transitions have been already obtained in previous sections. The models are connected in cascade and the complete multimodal model of the TLM tuner structure is obtained (Fig. 3.33). The impedances included in each model are replaced with the appropriate circuit models corresponding to the elements of Fig. 3.32. The TLM asymmetric-outer strip shunt impedance transition models include two outer-strip impedances, while Z_{Ap1} and Z_{Bp1} correspond to Z_1 and Z_3, Z_{Ap2} and Z_{Bp2} correspond to Z_2 and Z_4. Concerning the TLM asymmetric-outer strip series impedance transition model, Z_{As} and Z_{Bs} correspond to open circuits.

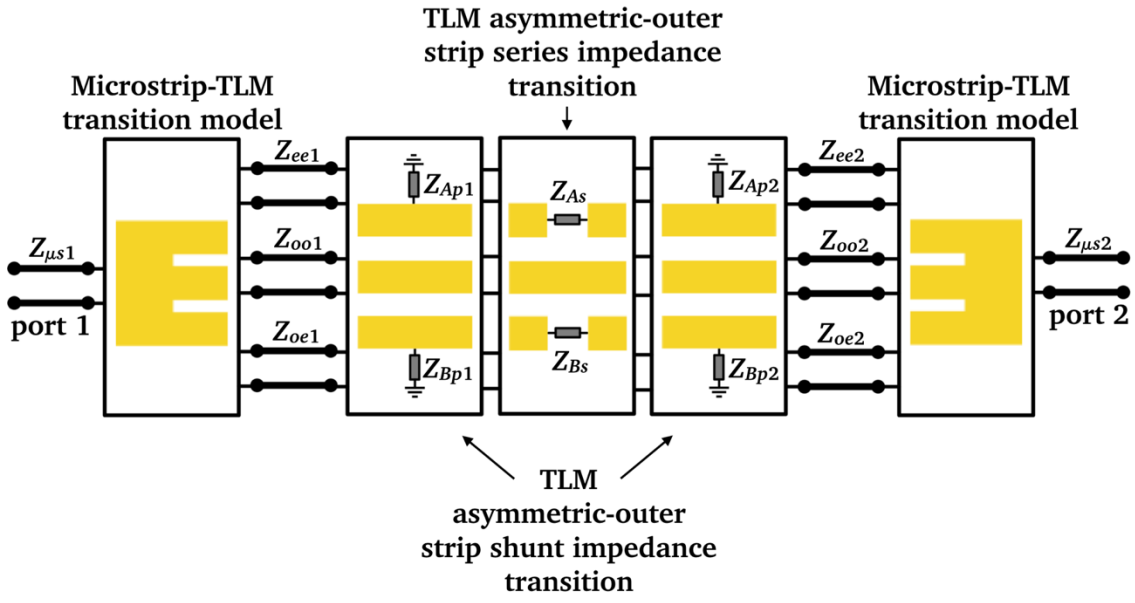


Fig. 3.33. Multimodal model of the proposed TLM structure.

3.4.2. Fabrication of the proposed TLM structure

Different elements like via holes, open circuits and microstrip line stubs (short and open) can be used to implement the impedances Z_1, Z_2, Z_3, and Z_4. The selected structures for fabrication are shown in Fig. 3.34. Impedances Z_1 and Z_4 of the TLM structure shown in Fig. 3.34a correspond to open circuits and impedances Z_2 and Z_3 are implemented with open-circuited microstrip line stubs. In the case of the structure shown in Fig. 3.34b, Z_1 correspond to an open circuit and Z_4 to a short circuit, and Z_2 and Z_3 are open-circuited microstrip line stubs. Concerning the structure shown in Fig. 3.34c, while Z_2 and Z_4 correspond to open circuits, Z_1 correspond to an open-circuited microstrip line stub and Z_3 to a short-circuited microstrip line stub. Finally, in the structure shown in Fig. 3.34d Z_1 and Z_3 are open-circuited microstrip line stubs, Z_2 and Z_4 correspond to open circuits.

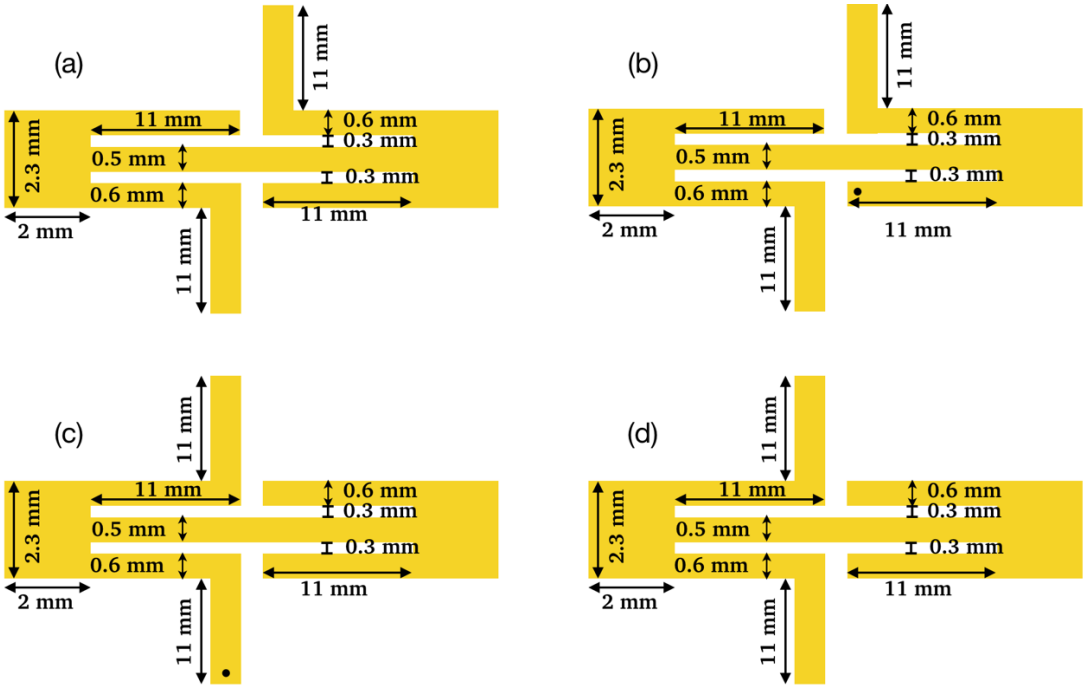


Fig. 3.34. TLM structures selected for fabrication.

The TLM structures shown in Fig. 3.34 were fabricated with the Rogers 4003 substrate mentioned before. Fig. 3.35 shows a picture of the fabricated TLM structures. Microstrip-to-coaxial transitions (0 to 18 GHz SMA-connector) are used to provide an easy way for RF access and S-Parameter measurement. An equivalent circuit for the SMA-connector is depicted in Chapter 4.

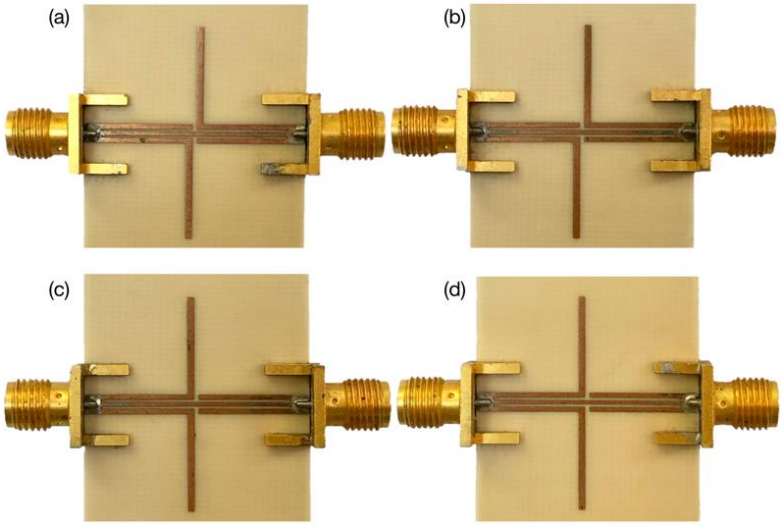


Fig. 3.35. Fabricated TLM structures.

3.4.3. Experimental characterization of the proposed TLM structure

The measurement set-up shown in Fig. 3.36 is used to measure the S-Parameters of the TLM structures illustrated in Fig. 3.35. An Agilent N5245A network analyzer is used to obtain the S-Parameters and the measurement range is 0.3 MHz to 6 GHz. Fig. 3.37, 3.38, 3.39 and 3.40 compares the simulated $|S_{11}|$ and $|S_{21}|$ obtained from multimodal models to the measured results of the TLM structures, showing a good agreement, thus validating the use of multimodal circuit models in complex TLM structures.

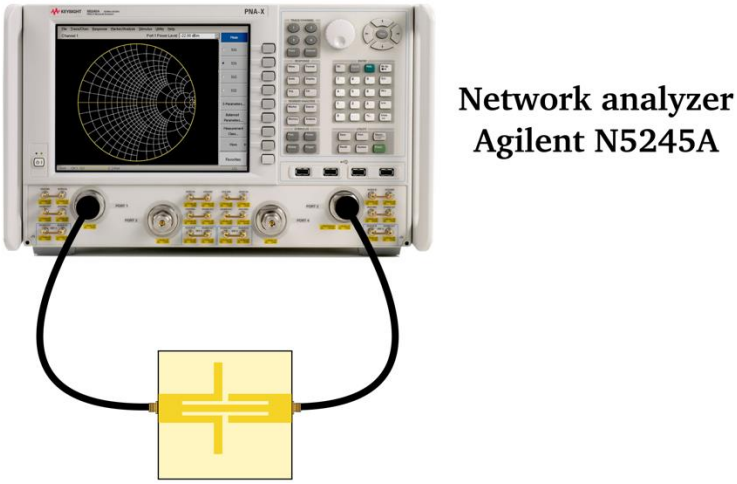


Fig. 3.36. Measurement set-up used for the experimental characterization of the TLM structures.

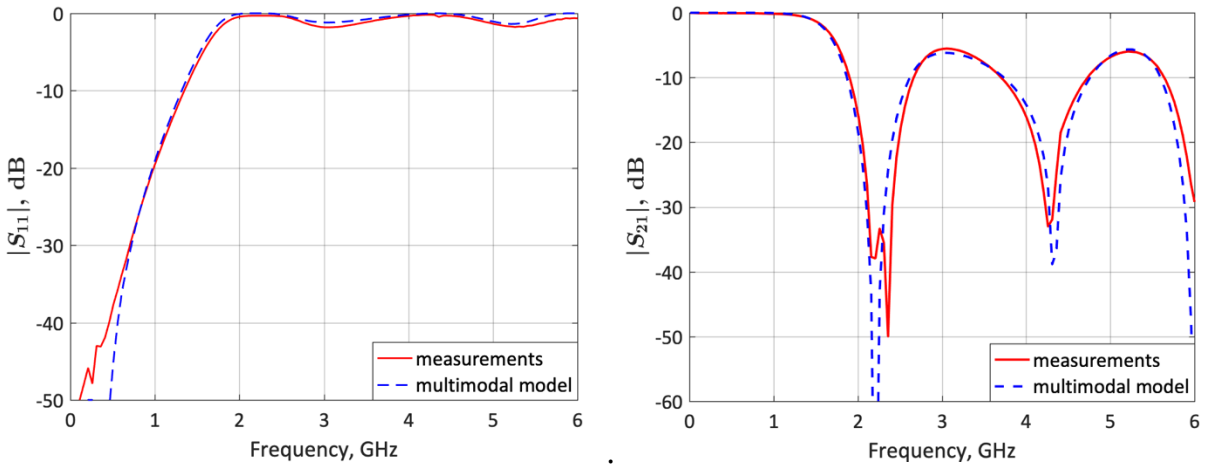


Fig. 3.37. Multimodal model simulations (dashed blue line) compared with the measurement results (red line) of the structure shown in Fig. 3.34a.

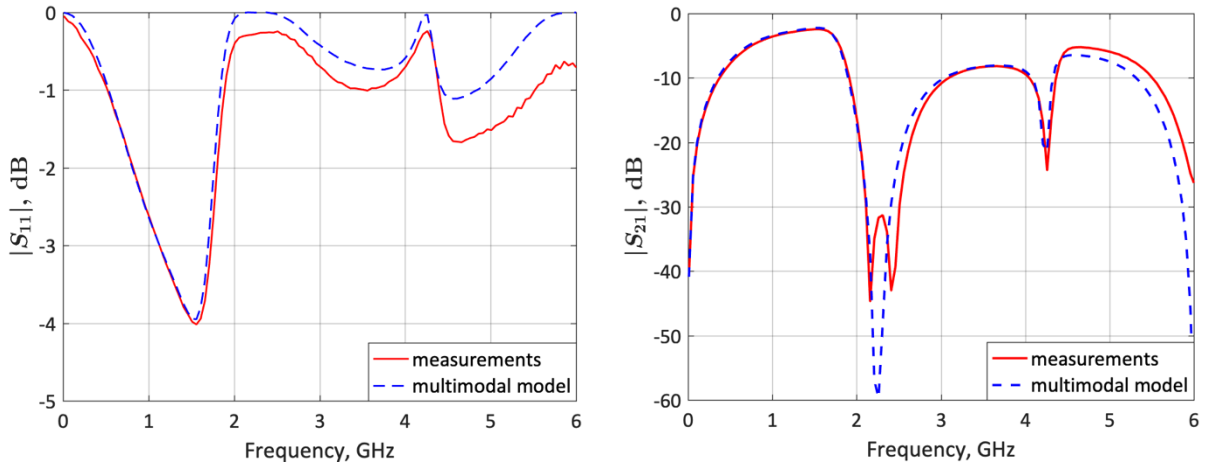


Fig. 3.38. Multimodal model simulations (dashed blue line) compared with the measurement results (red line) of the structure shown in Fig. 3.34b.

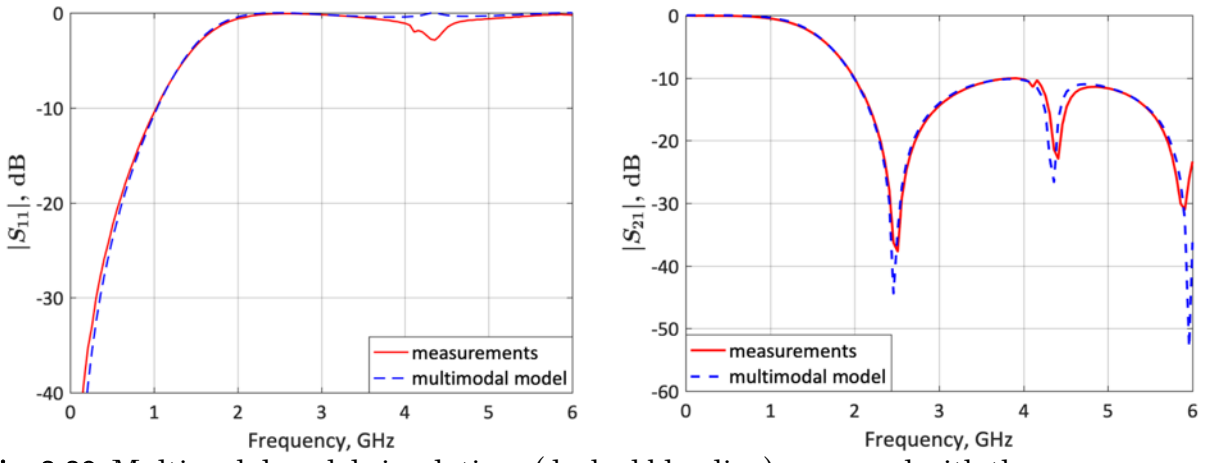


Fig. 3.39. Multimodal model simulations (dashed blue line) compared with the measurement results (red line) of the structure shown in Fig. 3.34c.

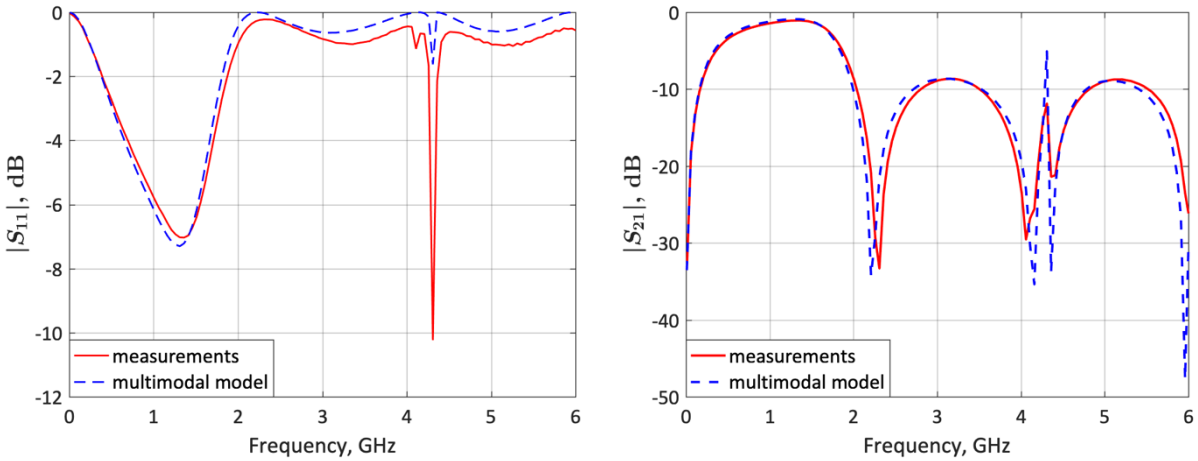


Fig. 3.40. Multimodal model simulations (dashed blue line) compared with the measurement results (red line) of the structure shown in Fig. 3.34d.

3.4.4. Parametric analysis of the proposed TLM structure

Since the multimodal model of the TLM structure obtained in subsection 3.4.3 (Fig. 3.33) has been validated, it can be used to explore the performance of such structures for different circuit applications. To this end, a parametric analysis of the TLM structure has been performed using a wide range of combinations of short/open microstrip line stubs and short/open circuits as impedances Z_1, Z_2, Z_3 and Z_4 (Fig. 3.32). After this analysis, the structure has demonstrated promising results as an impedance tuner and as a compact matching network. The length of the TLM sections and microstrip line stubs are varied in simulation to change the input impedance of the structure. The three TLM structures showing widest Smith chart coverage are illustrated in Fig. 3.41. Using these structures, a wide range of impedances can be achieve covering almost completely the Smith chart with a compact dimension.

The TLM total electrical length (ℓ_1+ℓ_2) and stubs electrical length (ℓ_{S1} and ℓ_{S2}) were varied from 0 to $\frac{\lambda}{8}$ (45˚) at the design frequency (2 GHz), and the S_{11} parameter was calculated. The simulated S_{11} parameter Smith-chart coverage is shown in Fig. 3.42. The modal characteristics of the TLM sections are obtained as described in subsection 3.3.2 (Z_{oo}= 49.3 Ω, Z_{oe} = 77.8 Ω, Z_{ee} = 122.1 Ω, β_{oo} = 31.7˚, β_{oe} = 32.6˚, β_{ee} = 35.8˚, x = 1.08 and y = 2.4). The simulated frequency is 2 GHz using the Rogers 4003 substrate mentioned before.

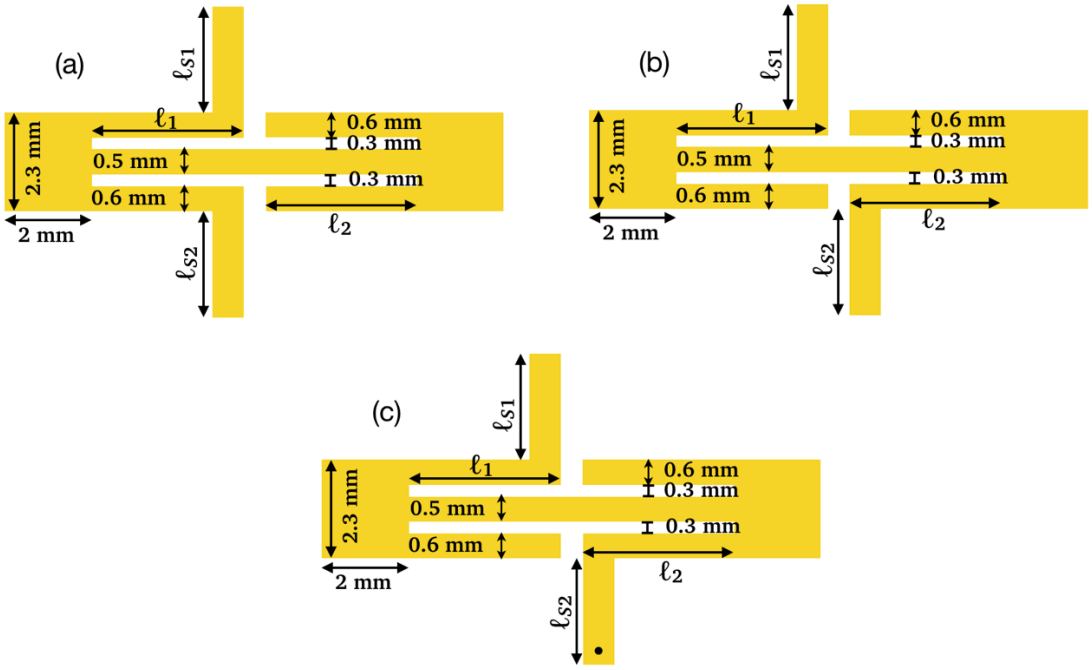


Fig. 3.41. Basic TLM structures selected for maximum Smith-chart coverage.

The impedances Z_1, Z_2, Z_3 and Z_4 shown in Fig. 3.32 are replaced with the appropriate circuit models corresponding to the elements of the structures shown in Fig. 3.41. As it is shown in Fig. 3.42, the structure illustrated in Fig. 3.41b accomplishes a better Smith-chart coverage. However, the structure in Fig. 3.41c covers an area of the Smith chart that the structure in Fig. 3.41b does not cover.

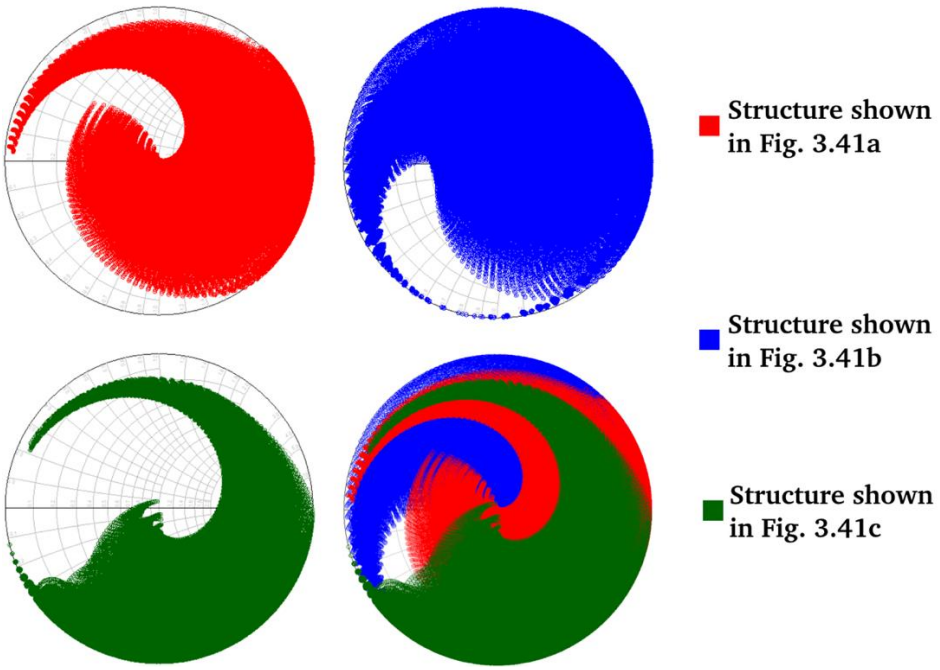


Fig. 3.42. Simulated S_{11} Smith-chart coverage obtained using the structures shown in Fig. 3.41 at 2GHz.

3.5. Conclusions

The multimodal structures studied in this Chapter have demonstrated excellent capabilities such as wide Smith-chart impedance coverage that can be useful for the implementation of tuners and matching networks. Besides of this, the compactness of multimodal structures makes them ideal for the size reduction of circuits. On the other hand, specific multimodal models have been developed for these structures which resulted in a fast and accurate tool to analyze the circuits. The electromagnetic simulation tools used for the analysis of planar structures are accurate but very time-consuming and they cannot be used as a design tool. Since the models developed in this Chapter predict the behavior for multimodal structures in an easy and low time-consuming way, they are very useful for the improvement on the design and simulation processes.

Due to the advantages of multimodal structures and their studied models, they will be implemented in this Thesis for the design of reconfigurable devices and as compact matching networks.

CHAPTER FOUR

MULTIMODAL IMPEDANCE TUNER

Impedance tuners have been extensively used in load pull measurements [40] and as reconfigurable matching networks for mismatch-compensation between antennas and the RF front-ends. Mechanical tuners offer low losses and good range Smith-chart coverage; they have high power handling and high-level accuracy [41][42]. However, they are heavy, bulky-size and have low operation speed. In this chapter, the multimodal TLM structure developed in Chapter 3 (Fig. 3.32) is loaded with varactors and used to implement a wideband impedance tuner at 2 GHz, with a wide, uniform Smith-chart coverage in the whole operation band (1.4 to 3.2 GHz). This design demonstrates the utility of the multimodal circuits studied in Chapter 3.

4.1. Multimodal three-line microstrip structure

The rigorous analysis of the multimodal structures studied in Chapter 3 shows that TML structures can be used as wide coverage impedance (S_{11}) tuners. As seen in Chapter 3, when the TLM structure length (Fig. 3.32) is tuned and different open-circuited/short-circuited stubs are connected to the two series-outer strip gaps, almost a 100% Smith-chart coverage is obtained. Based on this analysis, a multimodal TLM impedance tuner is proposed as shown in Fig. 4.1. It consists of a TLM section connected to input/output microstrip lines (to provide an easy access using microstrip-to-coaxial transitions), with two series gaps in its outer strips, and six variable capacitances. It can be observed that instead of stubs, four capacitors (C_{sg1}, C_{sg2}, C_{sg3}, and C_{sg4}) are connected to the two series-outer strip gaps, which, in addition to capacitors C_{is1} and C_{is2} connected to lower slot of the TLM structure, provide the required tunability.

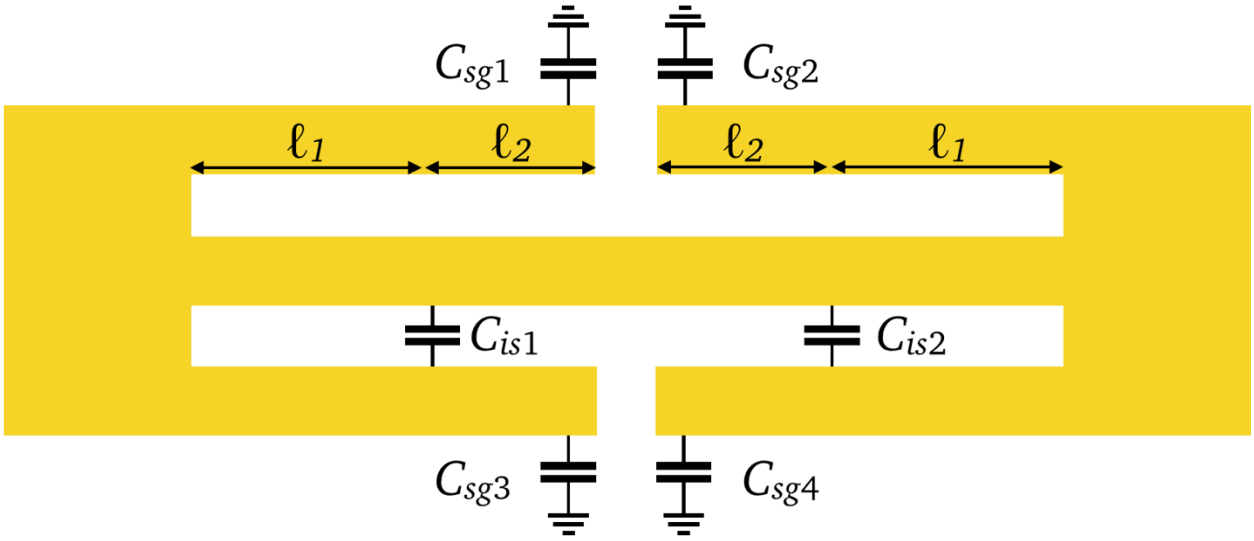


Fig. 4.1. Proposed TLM structure for the impedance tuner.

As explained in Chapter 3 the TLM propagates three fundamental modes, the *ee*, *oo*, and *oe* modes [38]. The microstrip mode basically generate *ee* modes at the microstrip-to-TLM transitions, which then excite (and afterwards interact with) the *oo* and *oe* modes at the gaps and capacitors, which in turn resonate in the TLM section. Thus, a rich resonant *oo*–*oe* structure coexists with the exciting *ee* structure in the same physical circuit area, resulting in an increase of the equivalent electrical size of the circuit with respect to a conventional tuner structure composed by a microstrip transmission line and the same number of capacitances.

4.2. Multimodal model of the impedance tuner

A multimodal model for the TLM structure illustrated in Fig. 4.1 can be easily obtained by properly identifying the transitions involved (Fig. 4.2). The models for each transition had been previously analyzed in Chapter 3, showing good results when compared with measurements (see subsection 3.4.3). From left to right, a microstrip-TLM transition is followed by a TLM section. After that, the isle that includes the inter-strip varactors can be easily identified as TLM asymmetric-central shunt impedances. In this case, one of the impedances is represented by the varactor, while the other one is an open circuit. After a short TLM section, a TLM asymmetric-outer strip shunt impedance transition follows, in which the varactors implement the two shunt impedances. This transition is followed by a TLM symmetric-outer strip series impedance transition, where series impedances are implemented using two open circuits. The second half of the TLM structure consists of the same transition topology described before using vertical symmetry with respect to the AA' axis.

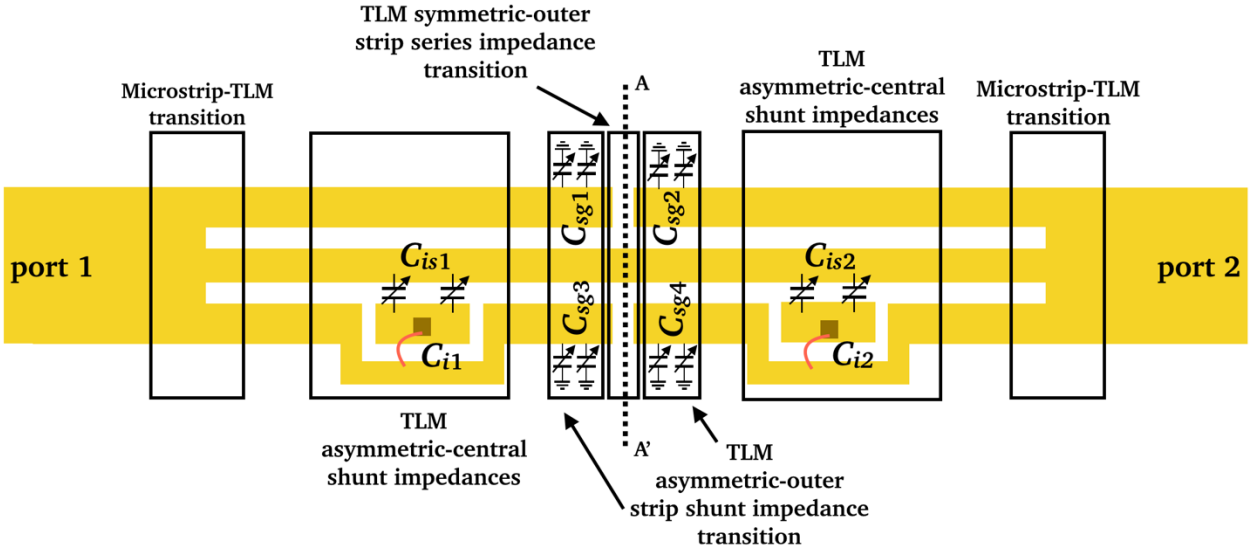


Fig. 4.2. Multimodal transitions and loads of the proposed TLM tuner structure.

The above transitions have been already studied in Chapter 3, and a multimodal model has been obtained for each one. The models are connected in cascade and the complete multimodal model of the TLM tuner structure is obtained (Fig. 4.3). The impedances included in each model are replaced with the appropriate circuit models corresponding to the elements (varactors and series gaps) of Fig. 4.2. From left to right in Fig. 4.3, the TLM asymmetric-central shunt impedance model includes two inter-strip impedances, Z_{Ac1} (open circuit) and Z_{Bc1} (capacitance C_{is1} in parallel with capacitor C_{i1}). Concerning the TLM symmetric outer-strip shunt impedance transition model, Z_{Ap1} and Z_{Bp1} correspond to capacitances C_{sg1} and C_{sg3}, respectively. With respect to the TLM series asymmetric impedance transition model, Z_{As} and Z_{Bs} correspond to the gaps in the outer strips.

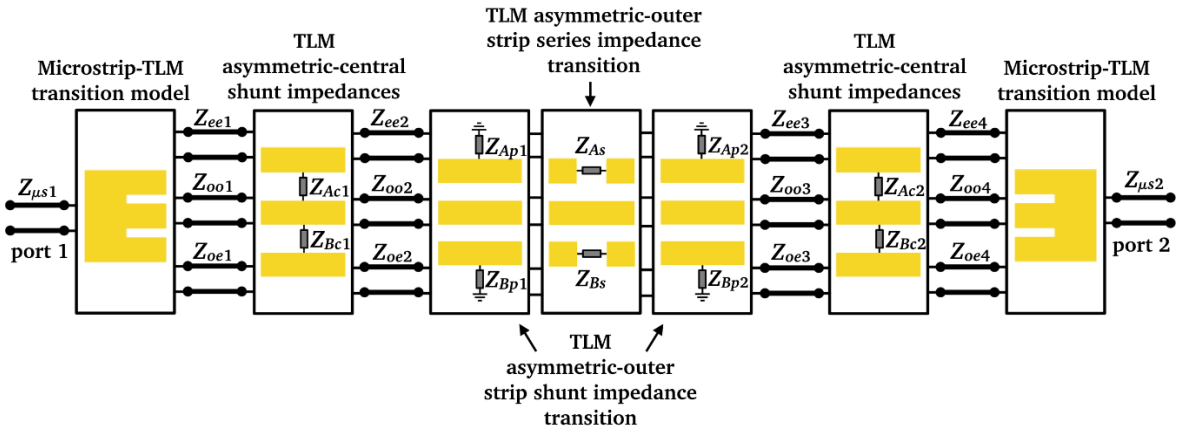


Fig. 4.3. Multimodal model of the proposed TLM tuner structure.

While the impedances Z_{ee}, Z_{oo} and Z_{oe} are the modal characteristic impedances of the TLM sections, $Z_{\mu s1}$ and $Z_{\mu s2}$ are the characteristic impedances of the microstrip line sections. In order to obtain the modal characteristic impedances Z_{ee}, Z_{oo} and Z_{oe} and the modal phase constants β_{ee}, β_{oo}, β_{oe}, and parameters x and y corresponding to the TLM sections, an electromagnetic analysis using Agilent Momentum is performed. Fig. 4.4 shows the simulated TLM structure. A touchstone file is obtained from a 6 ports simulation, and a MATLAB routine is used to obtain the modal characteristics (Table 4.1.) as described in Chapter 3.

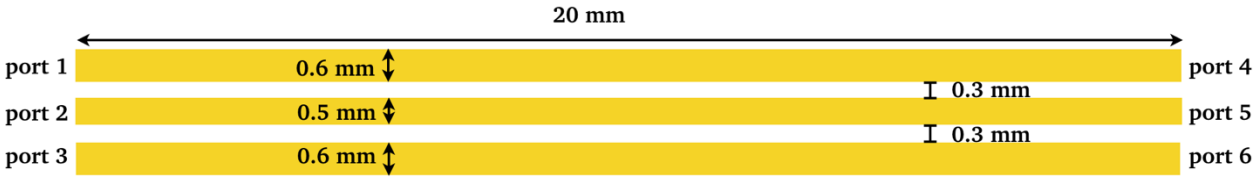


Fig. 4.4. Simulated TLM structure.

Table 4.1. Modal characteristics of the TLM structure (2 GHz). β is obtained for 1 GHz.

Z_{ee} (Ω)	Z_{oo} (Ω)	Z_{oe} (Ω)	β_{ee} (deg)	β_{oo} (deg)	β_{oe} (deg)	x	y
122.1	49.3	77.8	3.5	3.1	3.2	1.08	2.4

Using the obtained modal characteristics and the multimodal model shown in Fig. 4.3, a circuit simulation was performed. The results were compared with an electromagnetic simulation (Keysight's Momentum) of the tuner structure in order to validate the multimodal model. Fig. 4.5 compares the simulated $|S_{11}|$ and $|S_{21}|$ obtained from multimodal models to the electromagnetic simulation, showing a good agreement, thus validating the multimodal circuit model. Note that the TLM sections in the multimodal model simulation do not include loss and for this particular case, all the capacitances are set to 0.5 pF.

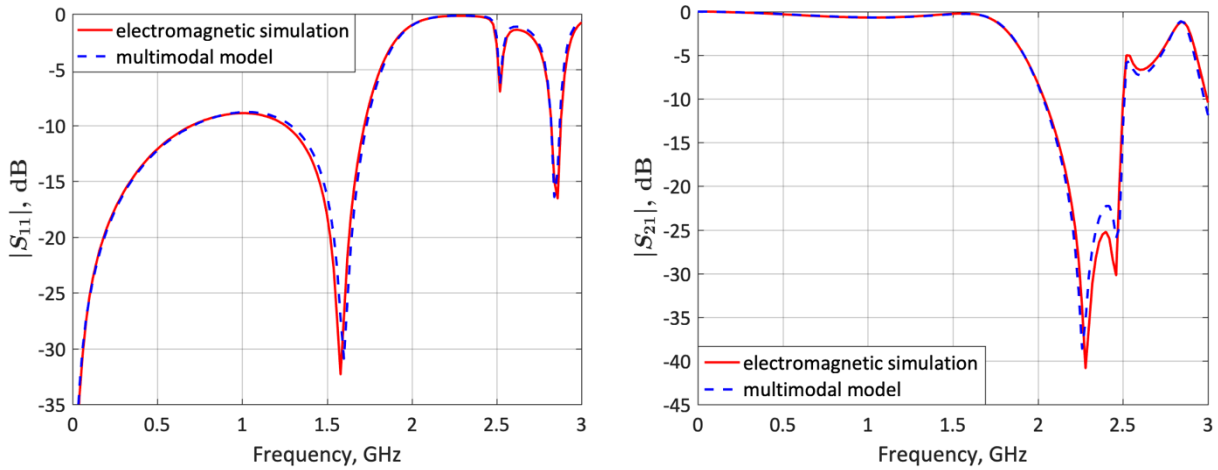


Fig. 4.5. Multimodal model simulation (dashed blue line) compared with the electromagnetic simulation (red line).

Fig. 4.6 compares the simulated tuner reflection coefficient obtained from the multimodal model to the simulated reflection coefficient of a conventional microstrip tuner with same electrical length and same number of uniformly-distributed, shunt-connected variable capacitances as the TLM tuner. Lossless lines and a 0–3.9 pF capacitance range were assumed for both simulations. The conventional microstrip structure tuner has a 54% Smith chart coverage, while the proposed tuner achieves 100%. Using the conventional microstrip tuner a larger structure (1.5λ) would be required to achieve a complete coverage of the Smith chart.

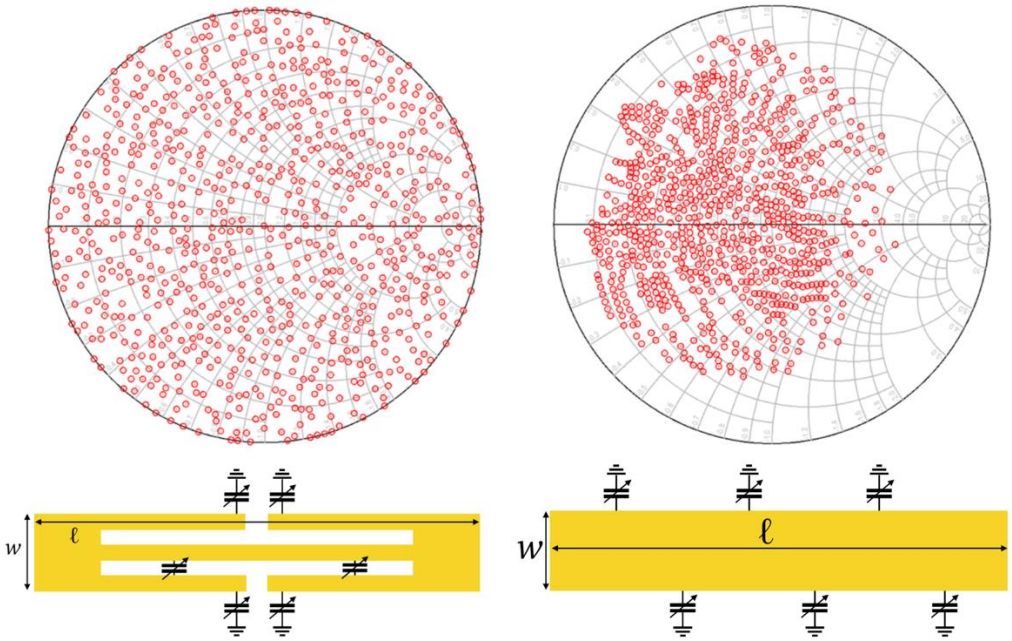


Fig. 4.6. Comparison of the simulated tuner coverage (S_{11}) at 2 GHz using TLM (left) and a conventional microstrip structure (right).

4.3. Implementation of the impedance tuner

A detailed schematic of the proposed multimodal impedance tuner is shown in Fig. 4.7. The electrical length of the TLM structure at the designed frequency (2 GHz) is λ/8 (45°) without taking in consideration the input/output microstrip line sections. The gaps and line widths of the TLM structure are defined using a parametric study and the multimodal analysis of Chapter 3. The selected TLM dimensions assure a maximal Smith-chart coverage.

Variable capacitances are implemented with two shunt varactors to increase the capacitance range (0.23 to 3.9 pF). 108 pF parallel-plate capacitors (C_{i1}, C_{i2}) are used to decouple varactors C_{is1} and C_{is2} in RF. The islands on the lower strips were used to provide a bias access for varactors C_{is1} and C_{is2}. 510 pF ground capacitors (C_{gp1}, C_{gp2}, C_{gp3} and C_{gp4}) and via holes are used to connect the outer-strip varactors (C_{sg1}, C_{sg2}, C_{sg3}, and C_{sg4}) to ground. 10 kΩ bias resistors (R_{b1}, R_{b2}, R_{b3}, R_{b4}, R_{b5} and R_{b6}) are used to provide bias to the varactors. Microstrip-to-coaxial transitions are used to provide an easy way for RF access and S-Parameter measurement.

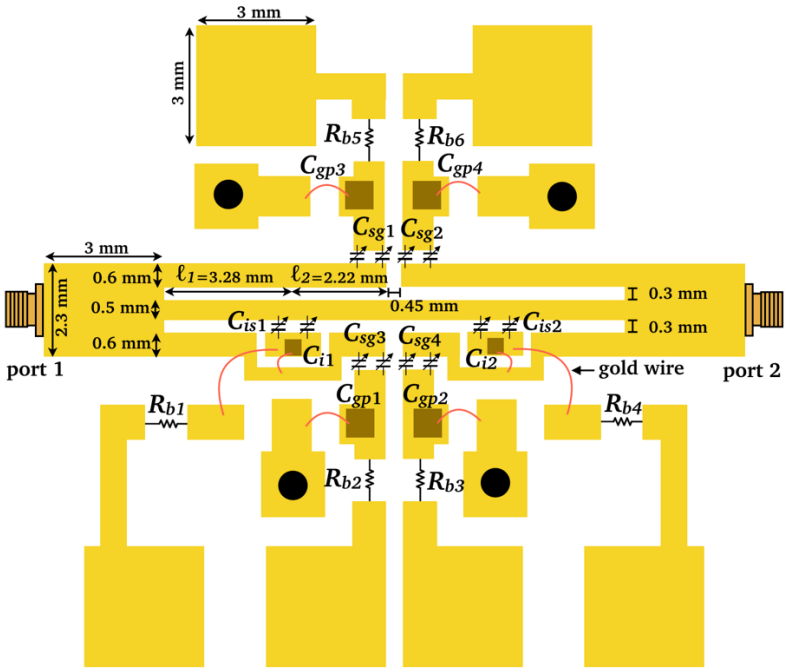


Fig. 4.7. Proposed multimodal impedance tuner design. Copper metallization is shown in yellow.

The relative positions of the two shunt inter-strip varactors (C_{is1} and C_{is2}) on the TLM structure define the planes where the modes *oo* and *oe* are excited by the fundamental mode *ee*, so that the resulting Smith-chart coverage of the tuner can change depending on where they are placed. The positions of the inter-strip varactors are optimized using a parametric study to achieve maximal Smith-chart coverage.

From multimodal simulation, it is obtained that the optimal length ratio $r = l_1/l_2$ is $r = 1.48$.

4.3.1. Lumped element models

Two varactors MACOM MA46580 with a capacitance range from 0.115 to 1.95 pF (corresponding to a bias voltage range of 18-0 V) are combined in parallel to implement the six variable capacitances C_{sg1}, C_{sg2}, C_{sg3}, C_{sg4}, C_{is1} and C_{is2} (Fig. 4.7), therefore the total range for each capacitance is 0.23 to 3.9 pF. In order to obtain a simulation closer to reality, equivalent circuit models for the varactor, parallel-plate capacitors (C_{i1} and C_{i2}) and bias resistors (R_{b1}, R_{b2}, R_{b3} and R_{b4}) were obtained from measurements.

Fig. 4.8 shows the experimental test-fixture, where the three devices are mounted in a slotline structure fabricated on a Rogers 4003 substrate with $\varepsilon_r = 3.55$, $h = 0.81$ mm and tan(δ)=0.0022. The metallization is copper with a thickness of 17.5 μm. Gold patches are soldered on each end of the metallization (copper) to assure a good contact with the RF Ground-Signal (GS) probes. The devices were measured using a Cascade-Microtech 9000 probe station with GS-SG 250 μm pitch probes and an Agilent N5245A network analyzer. The varactor was biased from 0 to 18 V using a DC power supply Agilent N5752A.

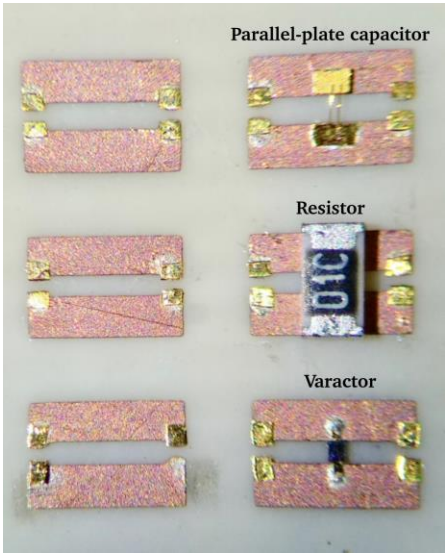


Fig. 4.8. Test-fixture of the varactor, 108 pF parallel-plate capacitor and bias resistor mounted in a Rogers 4003 substrate.

a) Varactor

The equivalent circuit model of the varactor was obtained by fitting the circuit of Fig. 4.9 to the measured S-Parameters. L_p and C_p are the parasitic inductance and capacitance associated to the gold patches and the GS-SG probes, R_v and L_v

correspond to the varactor parasitic resistance and inductance, Z_{0cl} and l_{cl} are the characteristic impedance and length of the slotlines and C_v is the varactor variable capacitance. The attenuation and phase constant of the slotlines are 3.8 $\frac{dB}{m}$ and 31.2˚at 2 GHz.

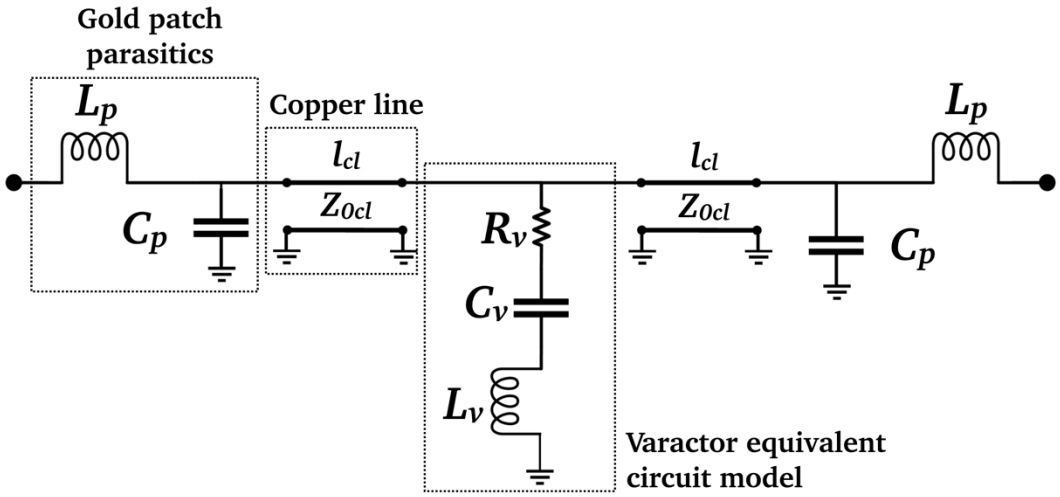


Fig. 4.9. Varactor equivalent circuit model.

Table 4.2 lists the values obtained for the varactor variable capacitance. Table 4.3 lists the values obtained for the parasitic elements of the equivalent circuit model.

Table 4.2. Variable capacitance of the varactor equivalent circuit model.

Volatage (V)	C_v (pF)
0	1.95
1	1.33
2	0.87
4	0.495
6	0.34
8	0.235
10	0.19
15	0.125
18	0.115

Table 4.3. Elements values of the varactor equivalent circuit model.

L_p (nH)	C_p (pF)	R_v (Ω)	L_v (nH)	Z_{0cl} (Ω)	l_{cl} (mm)
0.2	0.03	0.5	0.25	118	0.8

Fig. 4.10 compares the varactor S-Parameters obtained from measurements and from the equivalent circuit simulation, for a particular bias voltage of 2 V. Both,

simulation and measurement show a very good agreement, which validates the equivalent circuit.

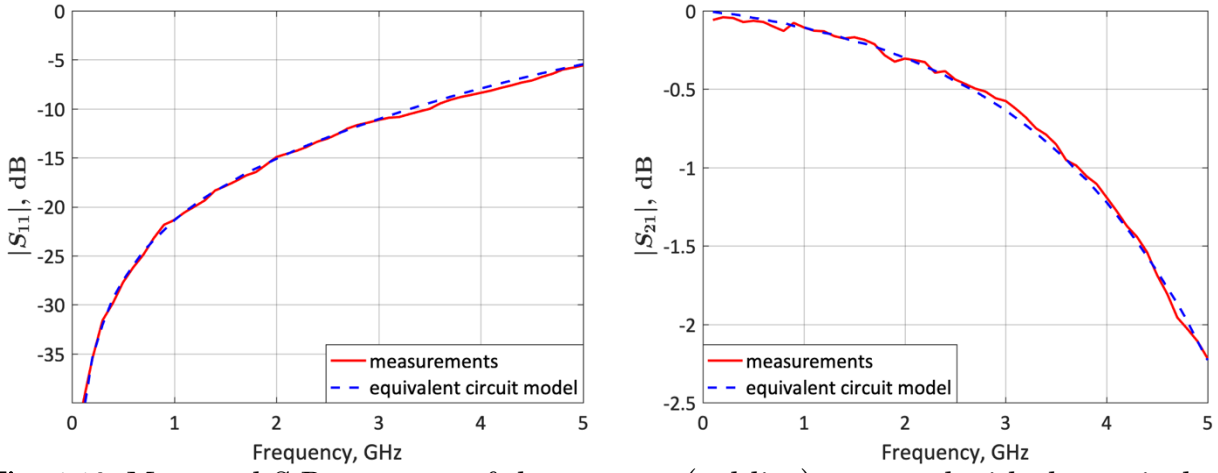


Fig. 4.10. Measured S-Parameters of the varactor (red line) compared with the equivalent circuit model simulation (dashed blue line). The bias voltage is 2 V.

b) 108 pF parallel-plate capacitor

The equivalent circuit model of the 108 pF parallel-plate capacitor (D20BV151K5PX) was obtained by fitting the circuit of Fig. 4.11 to the measured S-Parameters. In Fig. 4.11 R_c and L_c correspond to the parallel-plate capacitor parasitic resistance and inductance. Table 4.4 lists the obtained values for the parasitic elements and the capacitance of the parallel-plate capacitor equivalent circuit model.

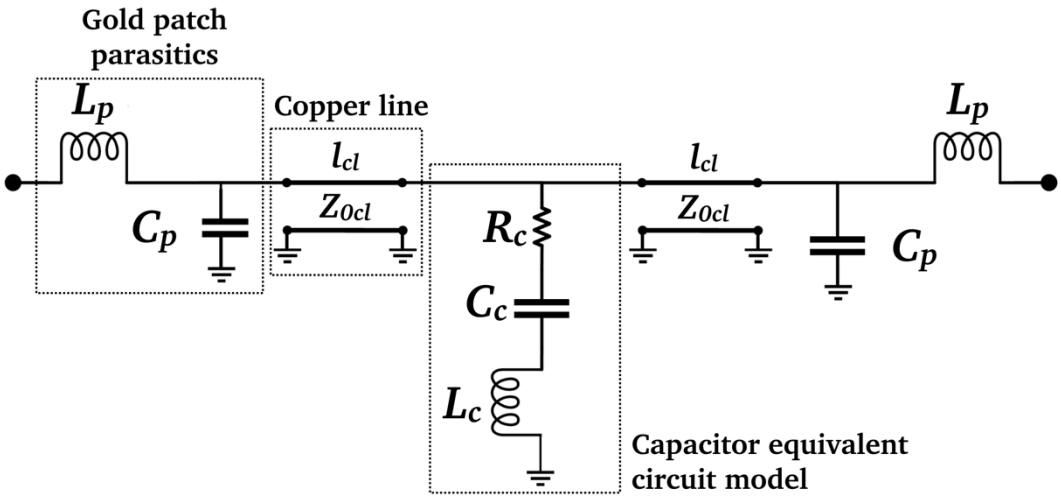


Fig. 4.11. Parallel-plate capacitor equivalent circuit model.

Table 4.4. Elements values of the parallel-plate capacitor equivalent circuit model.

L_p (nH)	C_p (pF)	R_c (Ω)	L_c (nH)	C_c (pF)	Z_{0cl} (Ω)	l_{cl} (mm)
0.2	0.03	0.5	0.237	108	119	0.8

Fig. 4.12 compares the parallel-plate capacitor S-Parameters obtained from measurements and from the equivalent circuit simulation. Both, simulation and measurement show a very good agreement, which validates the equivalent circuit.

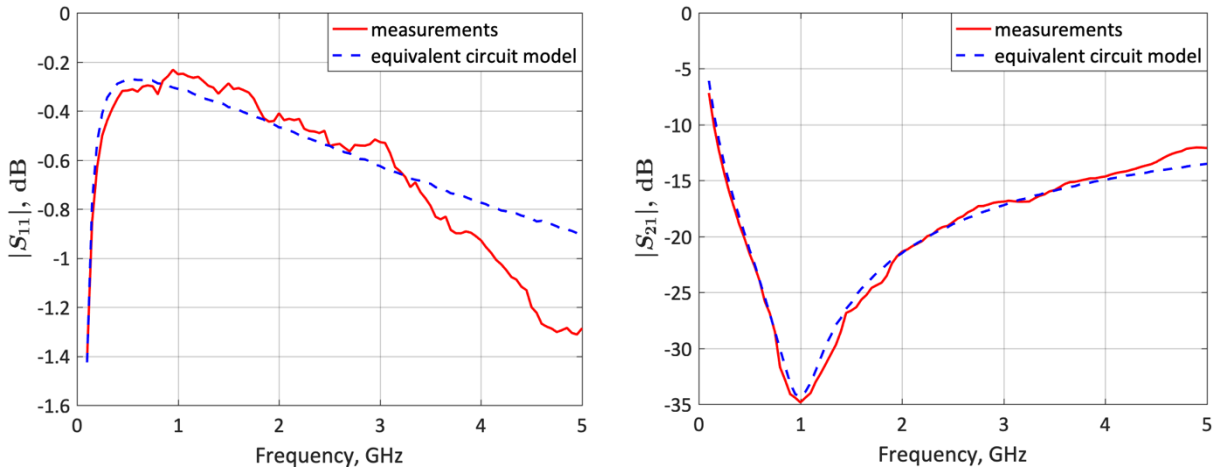


Fig. 4.12. Measured S-Parameters of the parallel-plate capacitor (red line) compared with the equivalent circuit model simulation (dashed blue line) of the 108 pF parallel-plate capacitor.

c) Bias resistor

The equivalent circuit model of the bias resistor (surface-mount resistor 0603) was obtained by fitting the circuit of Fig. 4.13 to the measured S-Parameters. In Fig. 4.13, L_r and C_r correspond to the resistor parasitic inductance and capacitance, and R_r is the resistance of the bias resistor. Table 4.5 lists the obtained values for the parasitic elements and the resistance of the resistor equivalent circuit model.

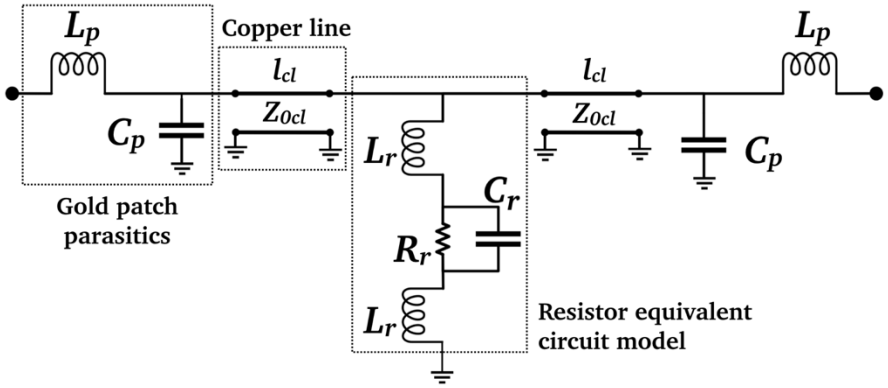


Fig. 4.13. Bias resistor equivalent circuit model.

Table 4.5. Elements values of the bias resistor equivalent circuit model.

L_p	C_p (pF)	L_r (nH)	C_r (pF)	R_r (kΩ)	Z_{0cl} (Ω)	l_{cl} (mm)
0.2	0.03	0.6	0.051	10	113	0.8

Fig. 4.14 compares the varactor S-Parameters obtained from measurements and from the equivalent circuit simulation. Both, simulation and measurement show a very good agreement, which validates the equivalent circuit.

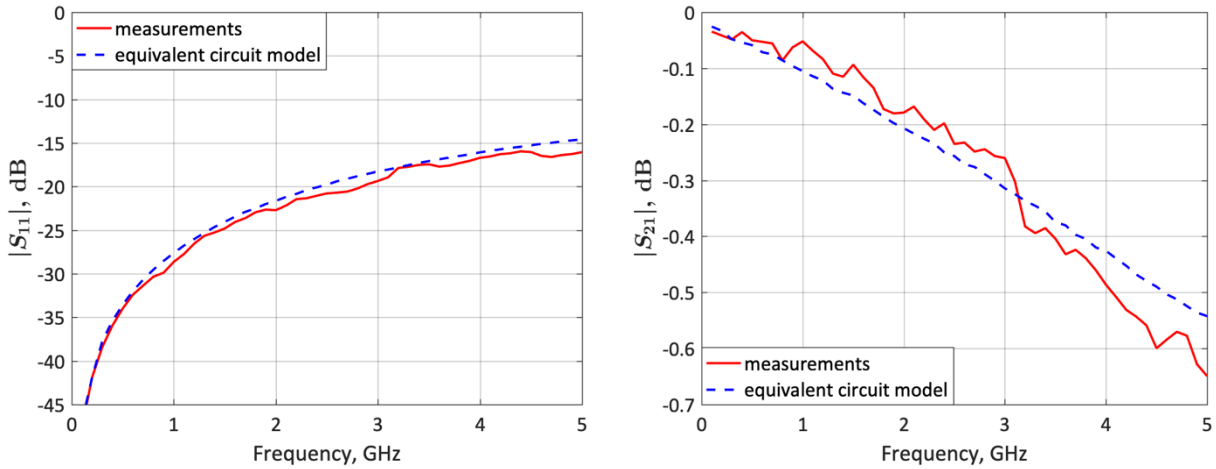


Fig. 4.14. Measured S-Parameters (red line) compared with the equivalent circuit model simulation (dashed blue line) of the bias resistor.

d) SMA coaxial connector

In addition to the above circuit elements, the SMA connector characteristics also impact the performance of the tuner. To assess the SMA-connector effect, a microstrip line with a length of 26.45 mm and width of 2.3 mm was fabricated, and SMA connectors were mounted to the microstrip line ends (Fig. 4.15), in order to obtain an equivalent circuit model from measurement. The SMA-connector frequency range is 0 to 18 GHz.

Fig. 4.15. Coaxial connectors and the fabricated microstrip line.

The proposed SMA-connector equivalent circuit is shown in Fig. 4.16. The connector characteristic impedance (Z_{0x}) is 49 Ω and the added length (l_x) produced by the connector is 7 mm. L_x, C_x and R_x are the connector parasitic inductance (0.15 nH), capacitance (0.072 pF) and resistance (0.001 Ω). The characteristic impedance ($Z_{0m\mu}$) and length ($l_{m\mu}$) of the fabricated microstrip line are 42.3 Ω and 26.45 mm.

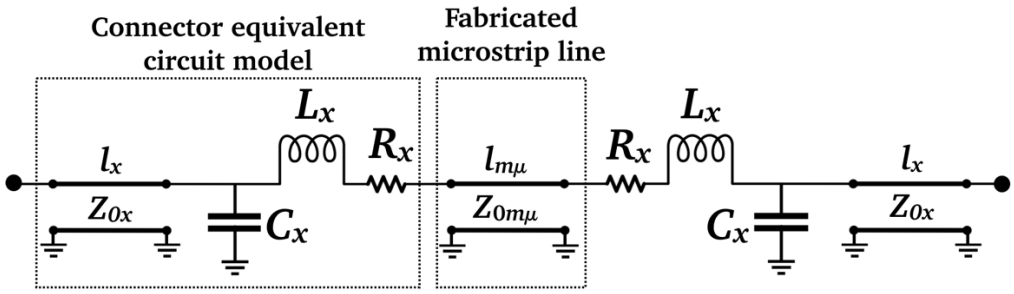


Fig. 4.16. Equivalent circuit model of the SMA 50 Ω connector.

The equivalent circuit simulation results agree very well with the microstrip line measured S-Parameters (Fig. 3.13). This validates the connector equivalent circuit.

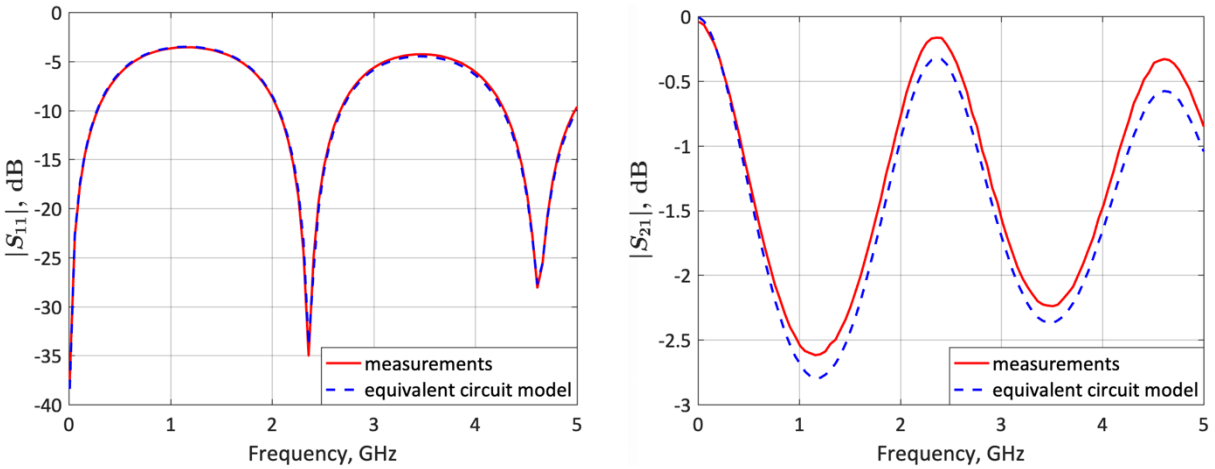


Fig. 4.17. Comparison between the measured (red line) and equivalent circuit model S-Parameters (dashed blue line) of the SMA connector.

4.4. Multimodal impedance tuner simulations

To evaluate the total coverage of the multimodal impedance tuner before fabrication, circuit/electromagnetic co-simulations were performed using Keysight ADS and Momentum. The equivalent circuit models obtained in subsection 4.3.1 of each element were included in the simulations as shown in Fig. 4.18 (the 510 pF capacitor use the same model as the 108 pF capacitor).

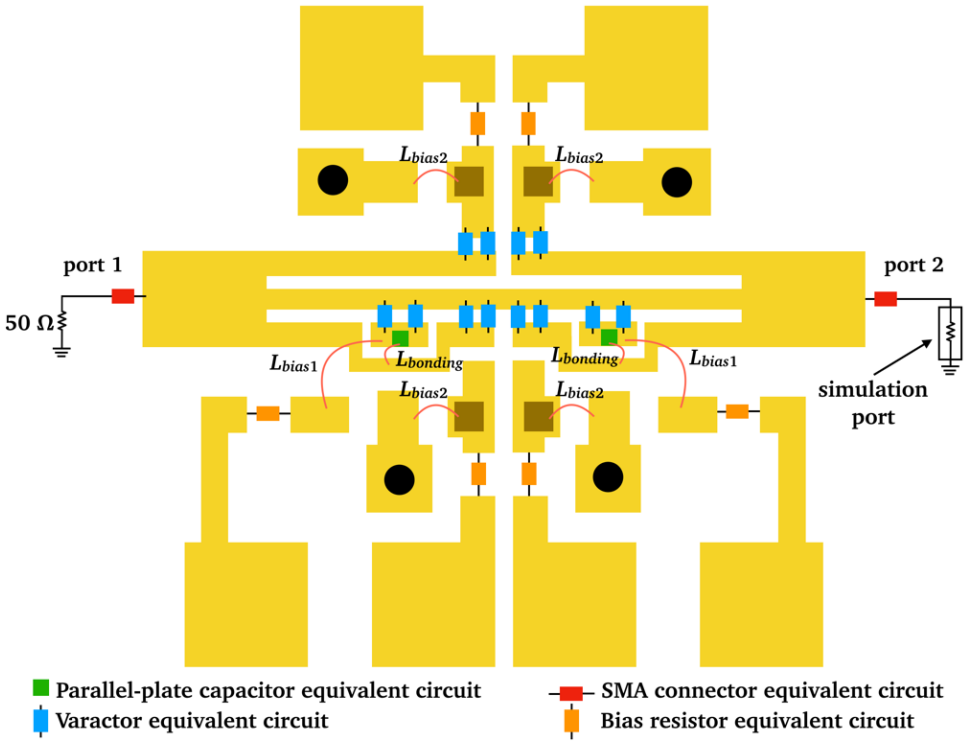


Fig. 4.18. Schematic drawing used for the simulations of the impedance.

The TLM structure and bias lines (both shown in yellow on Fig. 4.18) were analyzed using electromagnetic simulations. A co-simulation element was obtained from the electromagnetic analysis, to which the equivalent circuit models of each element (obtained in the preceding subsections) were connected. One single simulation port was used to obtain the tuner output reflection coefficient (S_{22}), with a 50 Ω ideal resistor connected to port 1. The simulations were performed at three single frequencies (1.4, 2 and 3.2 GHz), sweeping the capacitance of each varactor from 0.115 to 1.95 pF.

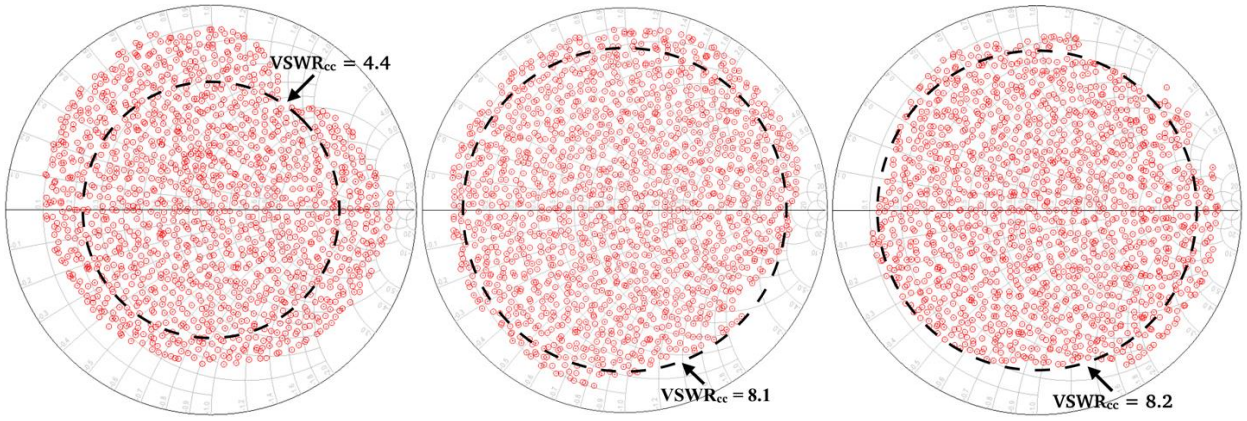


Fig. 4.19. Simulated reflection coefficient Smith-chart coverage of the impedance tuner for 1.4 (left), 2 (center) and 3.2 GHz (right).

Fig. 4.19 shows the Smith chart coverage obtained. The coverage percentage at 1.4 GHz is 70%, 76% at 2 GHz and 72 % at 3.2 GHz. A complete coverage of all reflection coefficients with voltage standing-wave ratio (VSWR) up to $VSWR_{CC}$ = 4.4 is achieved at 1.4 GHz, up to $VSWR_{CC}$ =8.1 at 2 GHz and up to $VSWR_{CC}$ =8.2 at 3.2 GHz.

4.5. Fabrication and experimental characterization of the impedance tuner

4.5.1. Fabrication

The impedance tuner was fabricated with the Rogers 4003 substrate mentioned before. Fig. 4.20 shows a picture of the fabricated TLM tuner.

Via holes were used to connect the varactors to the ground plane. Gold patches were used to allow a proper bonding of the gold wires using wire bonding technique. Double gold wires were used to connect the parallel-plate capacitors in order to reduce the parasitic inductance. The fabricated tuner features a total size of 17.45 × 16 mm (11.45 × 6.55 mm excluding the bias circuit and the SMA connector microstrip line).

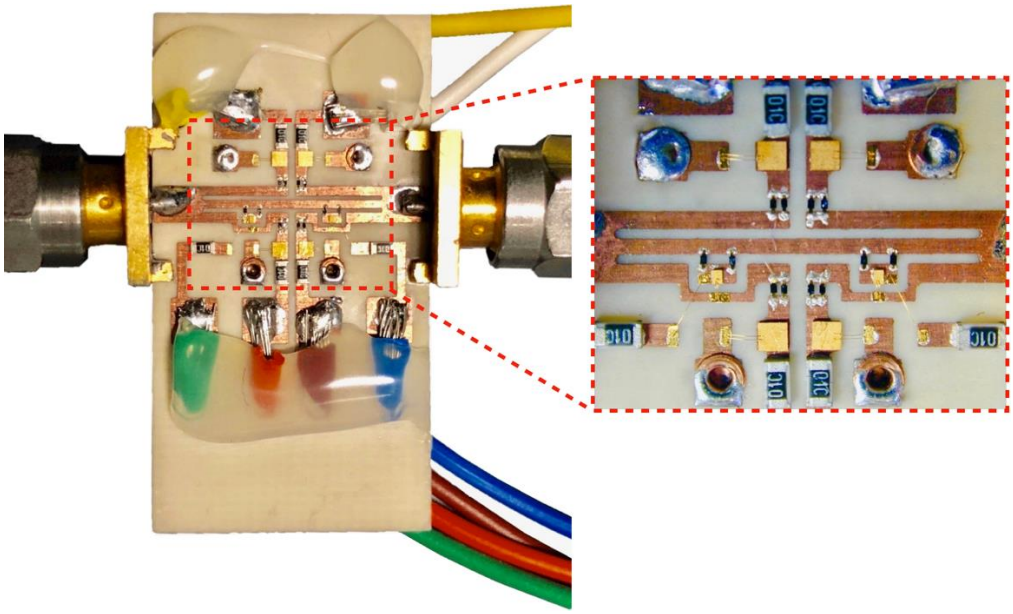


Fig. 4.20. Picture of the fabricated impedance tuner.

4.5.2. Experimental characterization

The set-up shown in Fig. 4.21 was used to measure the S-Parameters of the impedance tuner. Two power supplies (Agilent N6700B and HP 6629A) were used to provide bias to the varactors and an Agilent N5245A network analyzer was used to obtain the S-Parameters. A MATLAB routine was implemented to control the network analyzer and the power supplies (using a GPIB interface) and automatize the measurement. A total number of 1500 states were measured at 2 GHz, for a full capacitance-range variation of the varactors. Fig. 4.22 compares the simulated and measured results of the tuner input reflection coefficient S_{22}.

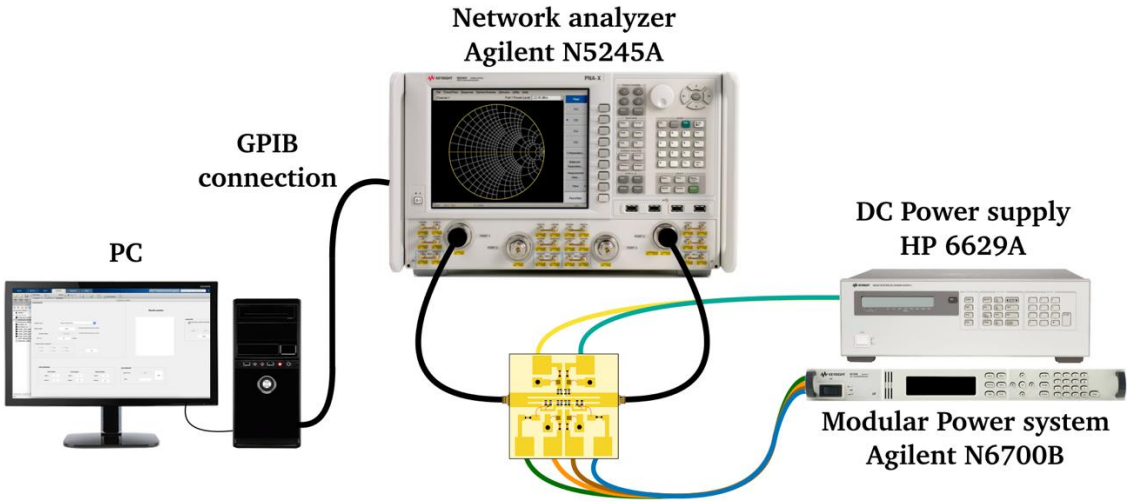


Fig. 4.21. Measurement set-up used for the experimental characterization of the impedance tuner.

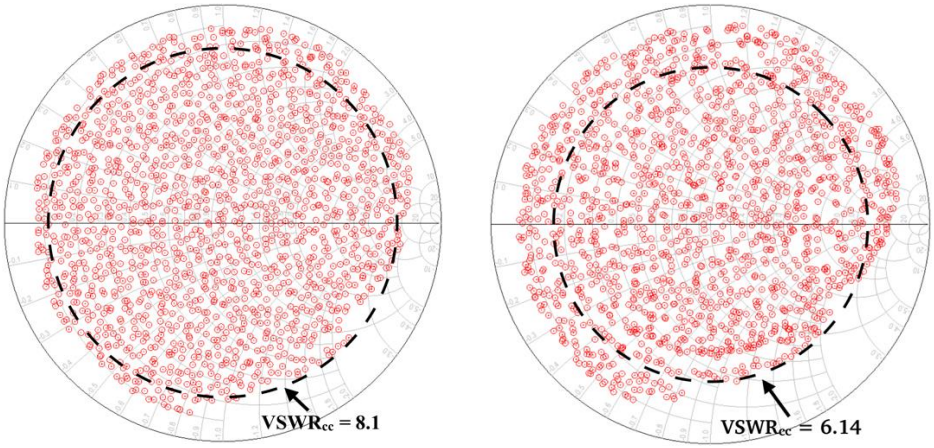


Fig. 4.22. Simulated (left) and measured (right) tuner coverage S_{11} at 2 GHz.

The measured Smith-chart impedance coverage is 73.2%, and its $VSWR_{CC}$ is 6.14. These results agree with the simulations (76.3% Smith chart coverage and VSWR = 8.1). The error ε between each simulated and measured state i (i=1 to 1500),

defined as $\varepsilon = \left|S^{i}_{22(meas)} - S^{i}_{22(sim)}\right|$ has a mean $m_\varepsilon = 0.038$ and a standard deviation $S_\varepsilon = 0.037$. A histogram of ε is illustrated in Fig. 4.23, it shows that the distribution of the error is around 0.02 at 2 GHz. The good agreement between simulations and measurement results validates the multimodal analysis as a useful design tool for the proposed TLM tuner.

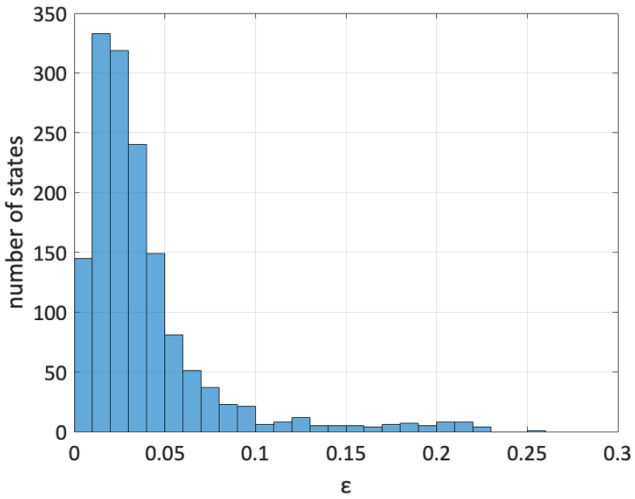


Fig. 4.23. Error histogram at 2 GHz.

To assess the tuner behavior as a function of frequency, measurements at 1.4 and 3.2 GHz were also performed. Fig. 4.24 and Fig. 4.25 compare the simulated and measured states at 1.4 and 3.2 GHz, respectively. The minimal measured Smith-chart impedance coverage is 70% and its $VSWR_{CC}$ is 3.4 in the whole 1.4–3.2 GHz frequency band. The fractional bandwidth is 85%, and $VSWR_{CC} > 6.14$ for the 2–3.2 GHz frequency band. The error histograms for 1.4 and 3.2 GHz are shown in Fig. 4.26. m_ε is 0.068 and 0.082, while S_ε is 0.038 and 0.065 for 1.4 and 3.2 GHz respectively. A histogram of ε at 1.4 and 3.2 GHz is shown in Fig. 4.26. It illustrates an error distribution of around 0.05 at 1.4 and 3.2 GHz.

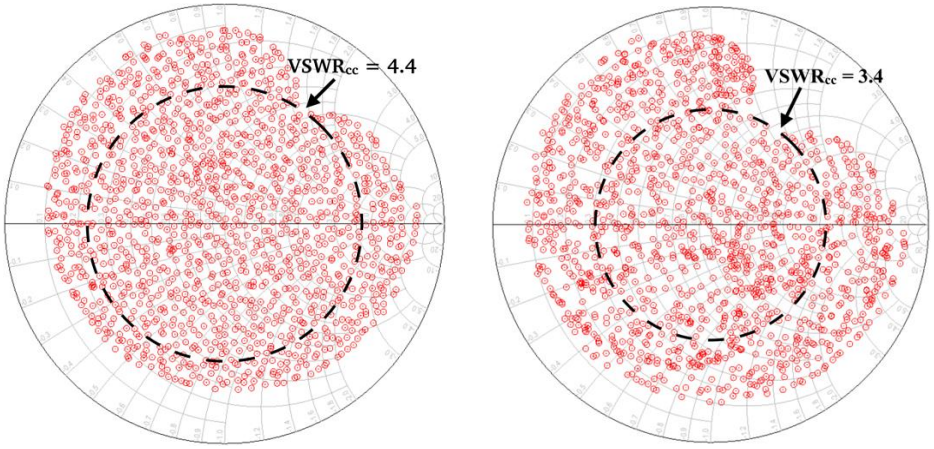


Fig. 4.24. Simulated (left) and measured (right) S_{22} tuner coverage at 1.4 GHz.

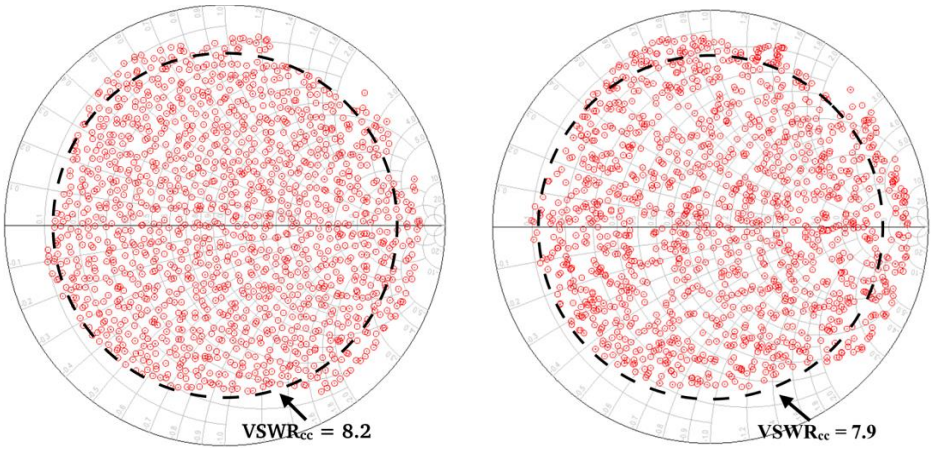


Fig. 4.25. Simulated (left) and measured (right) S_{22} tuner coverage at 3.2 GHz.

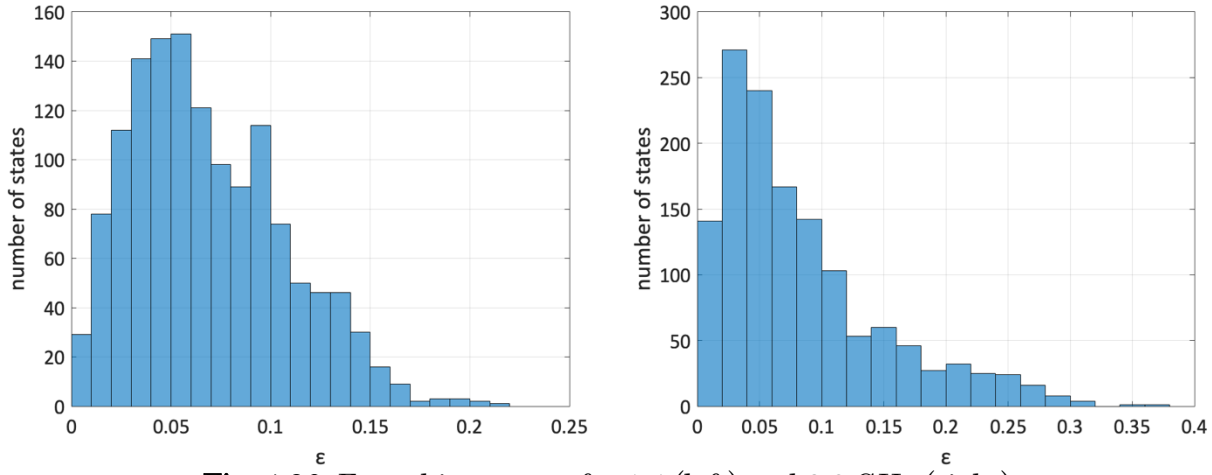


Fig. 4.26. Error histograms for 1.4 (left) and 3.2 GHz (right).

4.6. Conclusions

The proposed multimodal impedance tuner has demonstrated a wide Smith-chart impedance coverage above 70% for the 1.4 to 3.2 GHz frequency band (73.2% for the designed frequency 2 GHz), a good fractional bandwidth of 85% and a $VSWR_{CC}$ > 6.14 for the 2 to 3.2 GHz frequency band. It features a total size of 17.45 × 16 mm (11.45 × 6.55 mm excluding the bias circuit and the SMA connector microstrip line). The state-of-the-art performance and size of the proposed impedance tuner corroborates the usefulness of the multimodal structures and their studied models. Since the verification of the multimodal models and advantages of multimodal structures has been demonstrated, they are used in the next Chapters as compact matching networks in order to reduce the overall size of LNA designs.

CHAPTER FIVE

RECONFIGURABLE BICMOS LOW-NOISE AMPLIFIER USING A RF-MEMS SWITCH

LNAs are a key component of the RF-front end in every wireless device. With the increasing demand for higher data-rates and wideband, is crucial to increase the operation frequency of LNAs. Also, the different frequency bands at which novel systems have to operate, increase the need for reconfigurable devices.

In this Chapter, frequency-reconfigurable LNAs with a single RF-MEMS switch for D-band are presented. Three different amplifiers have been designed using IHP's 0.13 μm SG13G2 SiGe:C BiCMOS-MEMS technology. Two of the presented amplifiers include multimodal structures in the input matching network which are designed using the models already studied in Chapter 3. The use of multimodal structures in the matching networks allows a further size reduction of the amplifiers. Also, a systematic method for the design of two-stage frequency-reconfigurable amplifiers is presented. The LNAs have been designed, simulated, fabricated, and characterized.

5.1. State-of-the-art low-noise amplifiers

A vast number of LNAs amplifiers have been already demonstrated at D-band and higher frequencies [43][22][44][45]. In [43] two D-band LNA amplifiers are presented; the first design is a three-stage cascode amplifier with a peak gain of 24 dB at 158 GHz and F of 8.2 dB, while the second design is a five-stage common-emitter amplifier with a peak gain of 17.2 dB at 183 GHz with F of 8 dB. A two-stage D-Band LNA with a gain of 20 dB and F of 6.5 dB is presented in [22] for a 110 to 140 GHz frequency range. In [44] a 130 GHz three-stage D-band cascode LNA with a 24.3 dB gain, F of 6.8 dB and a 3 dB bandwidth of 20 GHz is presented. A four-stage 132 to 160 GHz LNA with a gain of 21 dB, a F of 8.5 dB and a 3 dB bandwidth of 28 GHz at 145 GHz is presented in [45].

Only a few mm-wave frequency-reconfigurable amplifier have been reported [46][47]. In [46] a two-stage 24 to 79 GHz frequency-reconfigurable LNA is presented. The LNA uses two RF-MEMS switches as reconfigurable devices and achieves a gain of 25/18 dB and a simulated F of 4.3/8.5 dB at 24 and 74 GHz respectively. In [47] a two-stage 60 to 77 GHz frequency-reconfigurable LNA is demonstrated. The gain is 20/22 dB and F is 7/8 dB at 60 and 77 GHz respectively; two RF-MEMS switches are implemented as reconfigurable devices.

5.2. Low-noise amplifier configurations

The majority of available D-band LNAs implement cascode, common-emitter or common-base configurations (illustrated in Fig. 5.1). The selection of the appropriate configuration will depend on the designer needs, since each of them has unique characteristics.

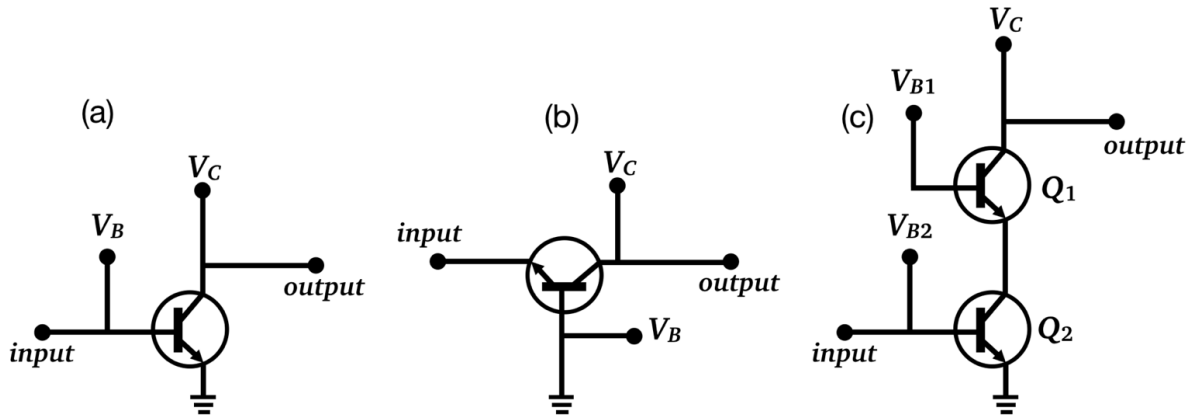


Fig. 5.1. Standard LNAs configurations: common-emitter (a), common-base (b) and cascode (c).

The most common configuration implemented for LNAs is the common-emitter due its low noise. More than one stage is usually used to achieve a high gain at high

frequencies. However, due to the Miller effect, the gain and bandwidth of the common emitter configuration decreases at frequencies above 100 GHz. The Miller effect is the phenomenon in which the parasitic collector-base capacitance increases its value with frequency and creates a feedback between the output and input of the configuration, causing a degradation of the LNA performance.

The common-base configuration has a higher F compared to the common-emitter configuration, however, it is commonly used because of its higher gain. Since the RF-signal input of the common-base configuration is the transistor emitter and the parasitic collector-emitter capacitance is very small [48], there is not feedback between the input and output. This allows a higher gain and bandwidth at frequencies above 100 GHz.

The cascode configuration is composed of two transistors connected as shown in Fig. 5.1c. The transistor Q_1 is implemented as a common-base configuration and transistor Q_2 as a common-emitter configuration. Although the cascode configuration has a higher F than other configurations it is widely used due to its high gain and wide bandwidth. Since the base of Q_1 is connected to ground (Fig. 5.1c), the parasitic collector-base capacitance does not decrease the gain of the configuration.

Table 5.1 compares the simulated gain, F and power consumption of the three configurations (calculated at 125 GHz) using the HBTs of IHP's 0.13 μm SG13G2 SiGe:C BiCMOS technology. All the characteristics are obtained using a single stage for each configuration.

Table 5.1. Comparison of the characteristics of the three most-common used configurations for LNAs (calculated at 125 GHz).

	Common emitter	Common base	Cascode
Gain (dB)	10.09	13.661	20.24
NFmin (dB)	3.49	3.89	4.33
Power consumption (mW)	16	18	21

The cascode configuration shows the higher gain with an increase of less than 1 dB in F compared to the other two configurations. Even though the power consumption is higher for the cascode configuration, the common-emitter and common-base configurations would require at least two stages to achieve the same gain. Using two stages for the common-emitter and common-base configurations would increase the power consumption even further than the cascode configuration. Due to its high gain, good reverse isolation and wide bandwidth, the cascode configuration is selected for the amplifier designs presented in this Thesis.

5.3. Frequency-reconfigurable LNA design with a multimodal input matching network

The first proposed amplifier is a two-stage frequency-reconfigurable cascode LNA designed using IHP's 0.13 µm SG13G2 SiGe:C BiCMOS-MEMS technology (described in Chapter 2). The frequency-reconfigurable LNA operates at two frequencies (125 and 140 GHz) which are selected using a single RF-MEMS switch. The two cascode stages of the LNA are optimized to provide high gain and low noise.

5.3.1. Design methodology of the frequency-reconfigurable LNA

The amplifier is designed to achieve low noise, but also maintaining a high gain. This criterion is taken into consideration for the selection of the reflection coefficients at the input and output of both stages of the amplifier. Fig. 5.2 shows the block diagram of the proposed LNA.

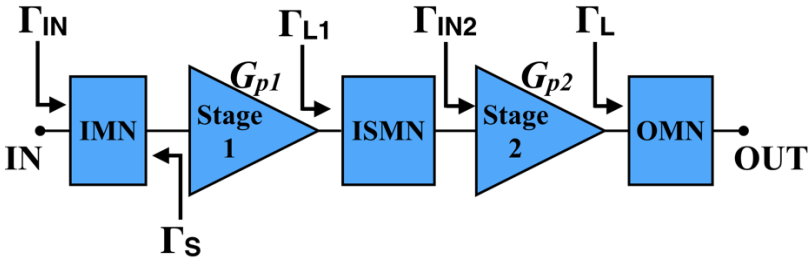


Fig. 5.2. Block diagram of the 125 to 140 GHz frequency-reconfigurable LNA.

The output matching network (OMN) synthesizes a load reflection coefficient Γ_L in order to obtain a balanced high gain for both frequency states (125 and 140 GHz) using the microstrip line L_7 and microstrip line short stub L_8 (Fig. 5.3). The calculated gain for the second stage (G_{p2}) is 10.6 dB at 125 GHz and 9.8 dB at 140 GHz, while the maximal gain ($G_{p2\,max}$) is 14.7 dB at 125 GHz and 13.5 dB at 140 GHz. Since $|S_{12}|$ is very small ($|S_{12}| < -40$ dB) for both stages, the input reflection coefficient of Stage 2, Γ_{IN2}, is basically independent of the particular value of the reflection coefficient Γ_L.

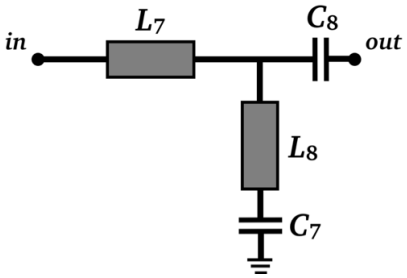


Fig. 5.3. Output matching network of the frequency-reconfigurable LNA.

The first-stage load reflection coefficient Γ_{L1} is synthesized using the inter-stage matching network (ISMN). The ISMN is designed to balance the power gain of each stage, G_{p1} and G_{p2} (and thus the LNA power gain G_p) at both frequency states (125 GHz and 140 GHz), at the expense of being slightly lower than G_{pmax}. The ISMN consists of a two-segment short-circuited stub composed of microstrip lines L_6 and L_9, the microstrip line L_5, and capacitors C_4, C_9, C_{10} and C_{11} (Fig. 5.4). The RF-MEMS switch selects the length of the two-segment stub between L_6 and $L_6 + L_9$. When the RF-MEMS switch is in "up" state (actuation voltage is 0 V), the total length of the two-segment stub is equal to the length of $L_6 + L_9$ (the operation frequency is 125 GHz). When the RF-MEMS switch is in "down" state (actuation voltage is 65 V), the total length of the two-segment stub is equal only to the length of L_6 (the operation frequency is 140 GHz).

The stub L_5 was added to the ISMN in order to adequately place the RF-MEMS switch and achieve a compact design. Capacitor C_{11} was set to 30 fF so that its area allows the required current density flow through it.

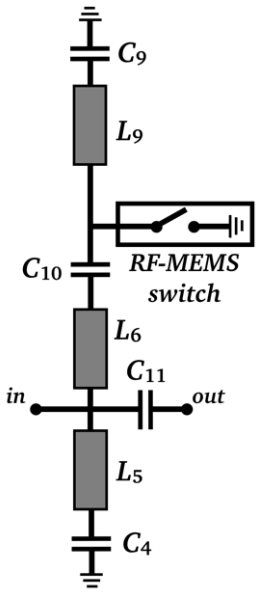


Fig. 5.4. Inter-stage matching network of the frequency-reconfigurable LNA.

The input matching network (IMN) consists of two microstrip lines (L_1 and L_3), a multimodal coupled microstrip line (L_2) and decoupling capacitors C_1 and C_2. The IMN allows to attain a balance between low noise and a low return loss value. The reflection coefficient Γ_S is synthesized using the microstrip lines L_1 and L_3; and the coupled microstrip line short-circuited stub L_2 (Fig. 5.5).

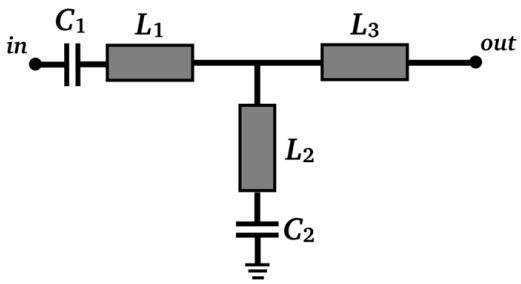


Fig. 5.5. Input matching network of the frequency-reconfigurable LNA.

The geometrical locus of constant F (for a selected Γ_S) and $|\Gamma_{IN}|$ in the Γ_{L1} plane is a circle (plotted in discontinuous line in Fig. 5.6). As shown in Fig. 5.6, these circles intersect the Γ_{L1} required to obtain G_{p1} = 8.8 dB and 7.8 dB at 125 and 140 GHz respectively. At 125 GHz, the obtained F for the selected Γ_S is 5.5 dB, 0.15 dB higher than F_{min}. Concerning the 140 GHz frequency state, the noise obtained F is 6.1 dB, 0.2 dB higher than F_{min}. Hence, the described requirements F, $|\Gamma_{IN}|$ and G_p for the LNA are fulfilled for both frequency states using the proposed IMN and ISMN. Table 5.2 shows the obtained calculated performance of the LNA design.

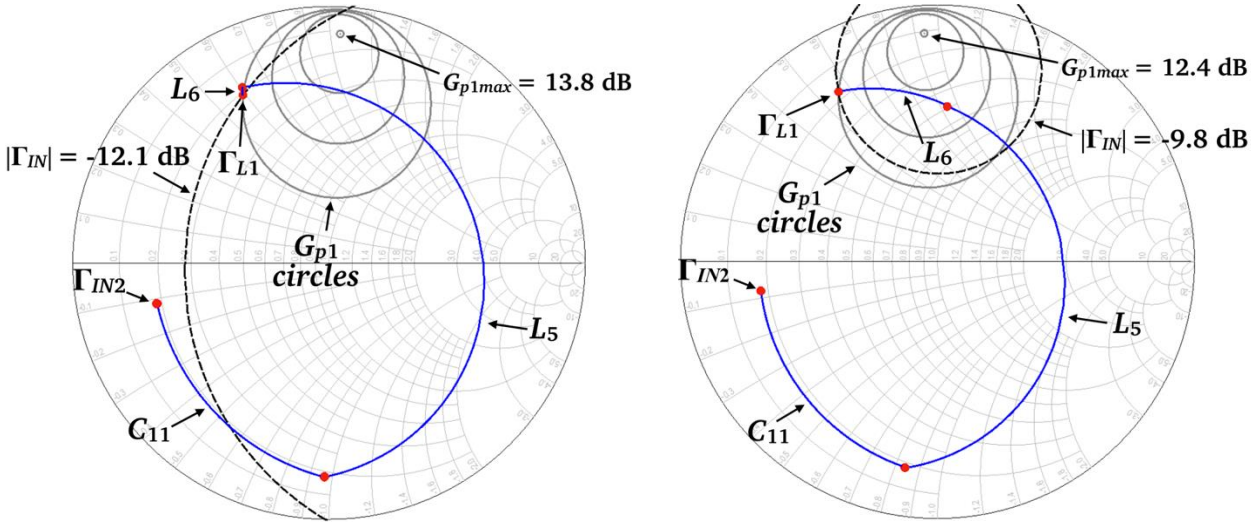


Fig. 5.6. Constant F, $|\Gamma_{IN}|$ and G_{p1} circles at 125 (left) and 140 GHz (right).

Table 5.2. Gain, F and $|\Gamma_{IN}|$ obtained for the LNA design at both frequency states.

	125 GHz	140 GHz
G_{p1} (dB)	8.8	7.8
G_{p2} (dB)	10.6	3.9
G_p (dB)	9.7	18
F (dB)	5.5	6.1
$\|\Gamma_{IN}\|$ (dB)	–12.1	–9.8

Fig. 5.7 illustrates the complete schematic of the frequency-reconfigurable LNA. All lines on the IMN (L_1, L_2 and L_3), ISMN (L_5, L_6 and L_9) and OMN (L_7 and L_8), as well as line L_4 are microstrip lines. The top-most metal layer of the IHP's SG13G2 technology (TM2 in Fig. 2.3) is used for the design of L_1, L_2, L_3, L_5, L_6, L_7 and L_8. L_9 is designed using the TM1 layer. Finally, a stack of three metallic layers (M2, M3 and M4) is used to design L_4.

The amplifier is biased with a V_{CC} = 2.5 V and I_{CC} = 15 mA using current mirrors (Q_5 Q_6, Q_7 and Q_8) and bias resistors (R_1 and R_2). The two cascode stages are unconditionally stable at all frequencies. The Stage 1 is composed of transistors Q_1 and Q_2, with 5 and 10 emitter fingers respectively, and is biased with a collector current of 4.8 mA. The Stage 2 is composed of transistors Q_3 and Q_4 with 10 emitter fingers each, and is biased with a collector current of 8.2 mA. This selected configuration allows obtaining a high gain while achieving an overall low noise.

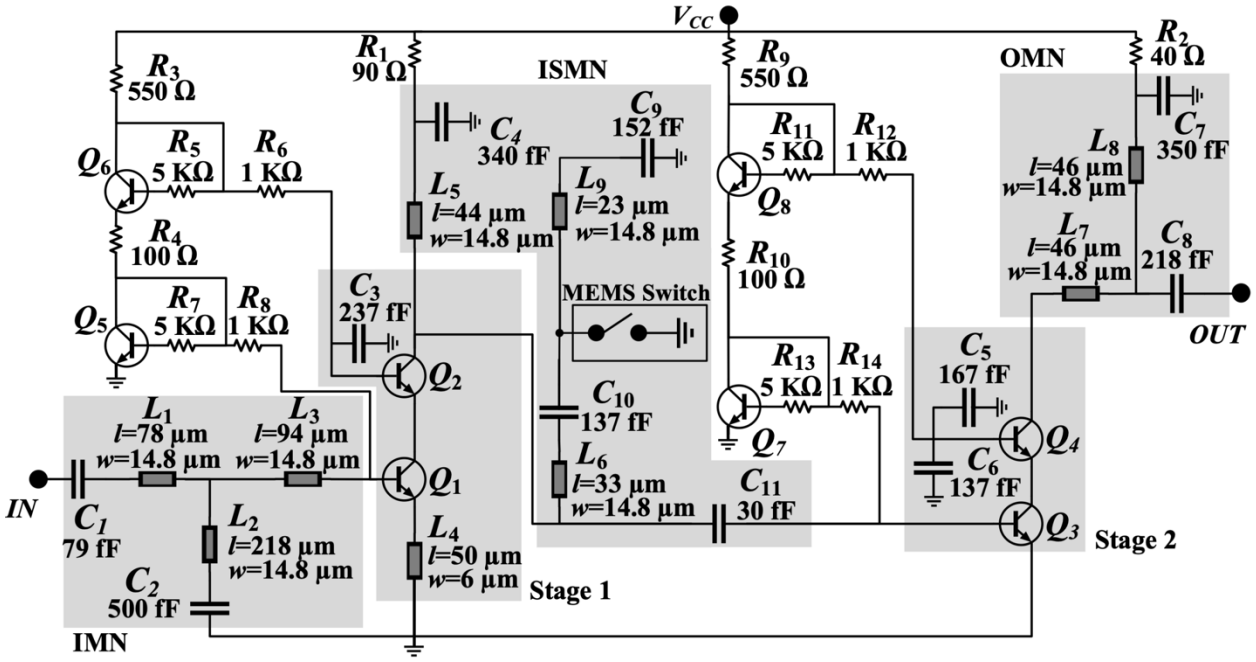


Fig. 5.7. Schematic of the 125 to 140 GHz frequency-reconfigurable LNA.

5.3.2. Multimodal matching network

The IMN, as mentioned before, includes a multimodal coupled microstrip line short stub. It consists of a coupled microstrip line, which ends are connected to microstrip lines, with a gap on the end of one of the strips (Fig. 5.8a).

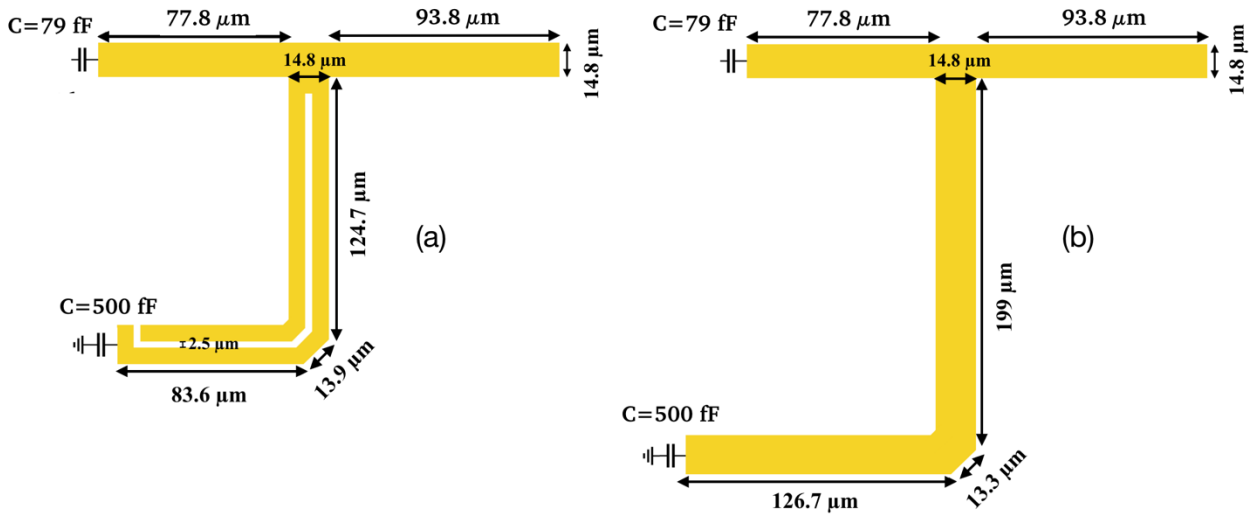


Fig. 5.8. Multimodal coupled microstrip line IMN (a) and standard microstrip IMN (b).

The coupled microstrip line propagates the two coupled microstrip line fundamental modes odd and even. The modes interact with each other at the asymmetries of the multimodal structure, which results in a stub with larger overall electrical size. The length of the multimodal stub is 222.2 μm which is shorter compared to a standard stub (344.5 μm) with the same electrical length. Compared to a standard microstrip stub, the proposed structure achieves a length reduction of 35.5%.

A multimodal model of the coupled microstrip line short stub can be easily obtained using the models studied in Chapter 3 (Fig. 5.9).

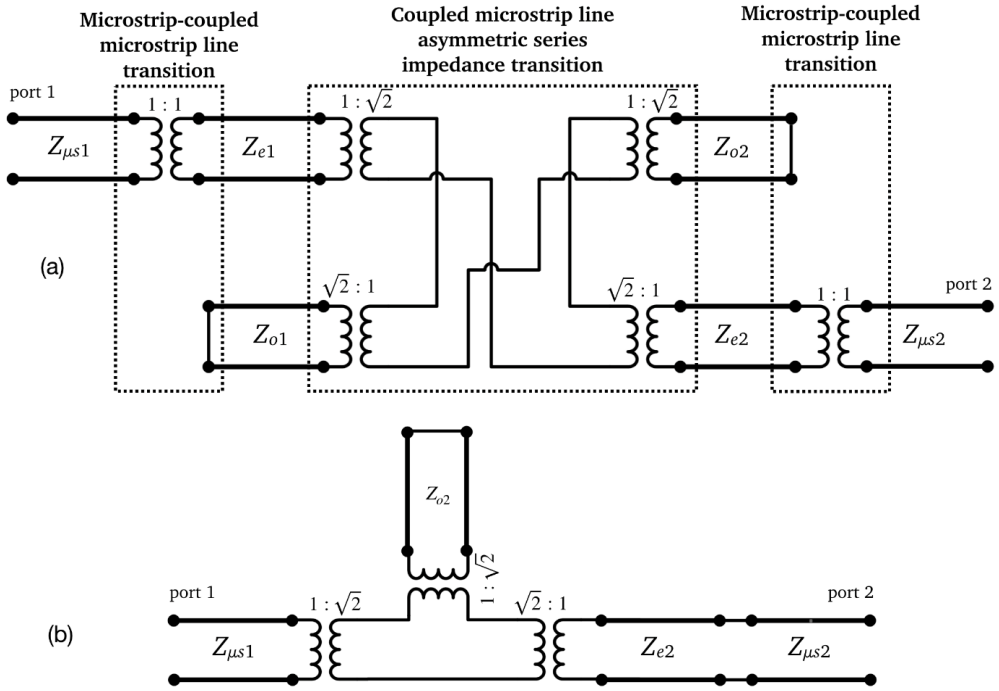


Fig. 5.9. Complete (a) and simplified version (b) of the coupled microstrip line stub multimodal model.

The lengths of the multimodal coupled microstrip line stub L_2, and microstrip lines L_1 and L_3 of the IMN are optimized to synthesize the required Γ_S. The multimodal model of the coupled microstrip line stub allows to easily optimize the length without using electromagnetic simulations (which is very time-consuming).

5.3.3. S-Parameters and noise figure simulations

In order to evaluate the S-Parameters of the frequency-reconfigurable LNA before fabrication, circuit/electromagnetic co-simulations were performed using Keysight ADS and Momentum. The obtained equivalent circuit models of transistors and resistors are included in the simulations as shown in Fig. 5.10.

The microstrip lines of the matching networks, bias network lines, capacitors and ground plane (shown in yellow, gray, green and blue on Fig. 5.10 respectively) were analyzed using electromagnetic simulation. A co-simulation element is obtained from the electromagnetic analysis, to which the IHP's design kit models of transistors, resistors and RF-MEMS switch are connected. A two-port simulation is implemented to obtain the S-Parameters and F of the frequency-reconfigurable LNA. The RF-MEMS switch element can be adjusted to "up" or "down" state in order to obtain the S-Parameters at both frequency states. The simulations were performed for a 110 to 170 GHz frequency range.

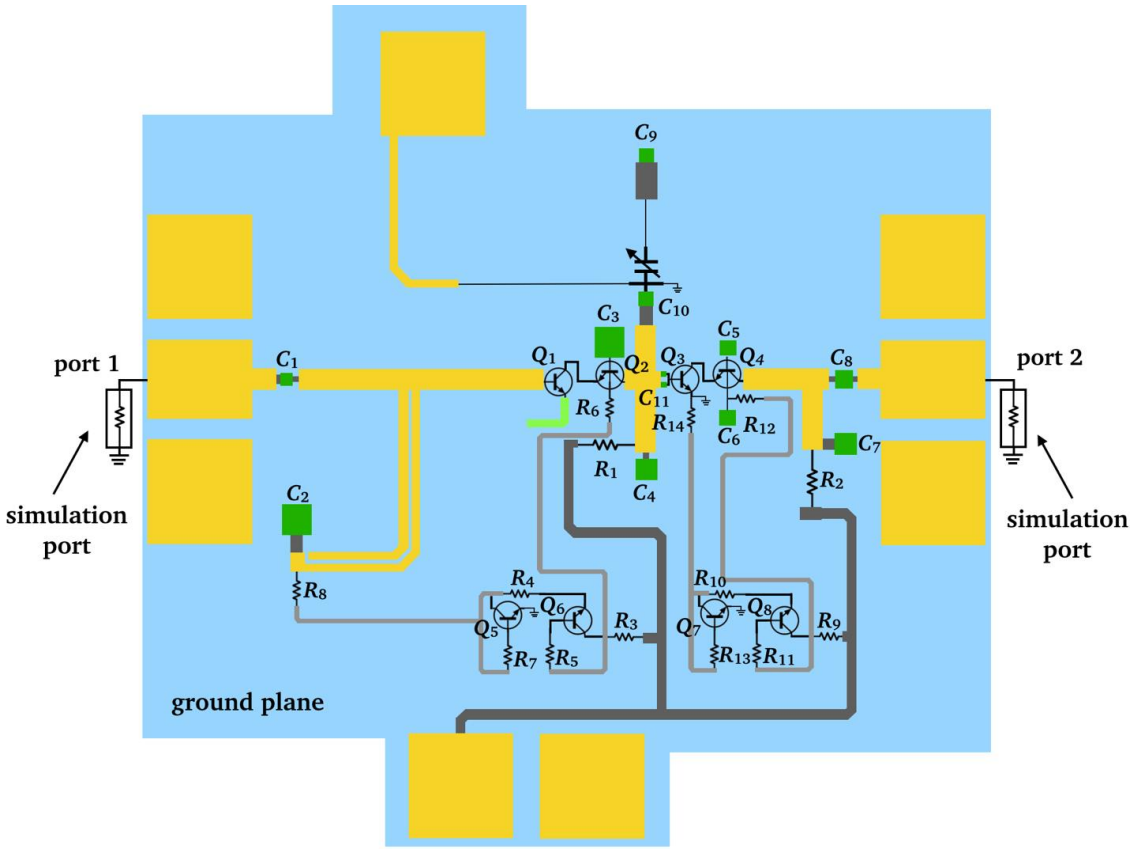


Fig. 5.10. Schematic drawing of the frequency-reconfigurable LNA.

Fig. 5.11 and 5.12 illustrate the S-Parameters and the obtained F from the simulations for a 110 to 170 GHz frequency range. For the lower-frequency state the simulated S-Parameters $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ are 19.9, –11.9, –42.5 and –7.4 dB respectively. For the upper-frequency state the simulated S-Parameters $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ are 17, –11.1, –42.1 and –1.7 dB respectively.

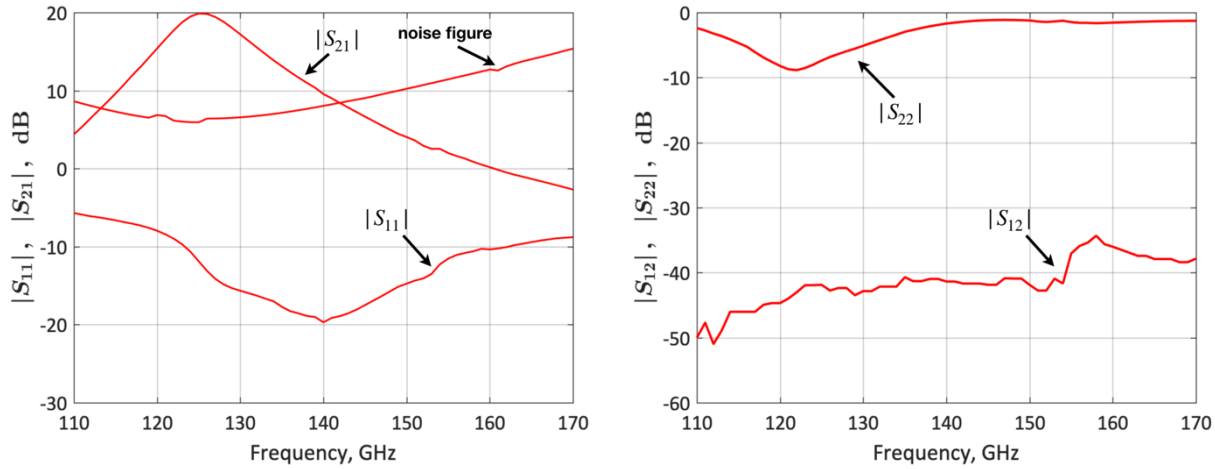


Fig. 5.11. Simulated S-Parameters and F of the frequency-reconfigurable LNA for the lower-frequency state (125 GHz).

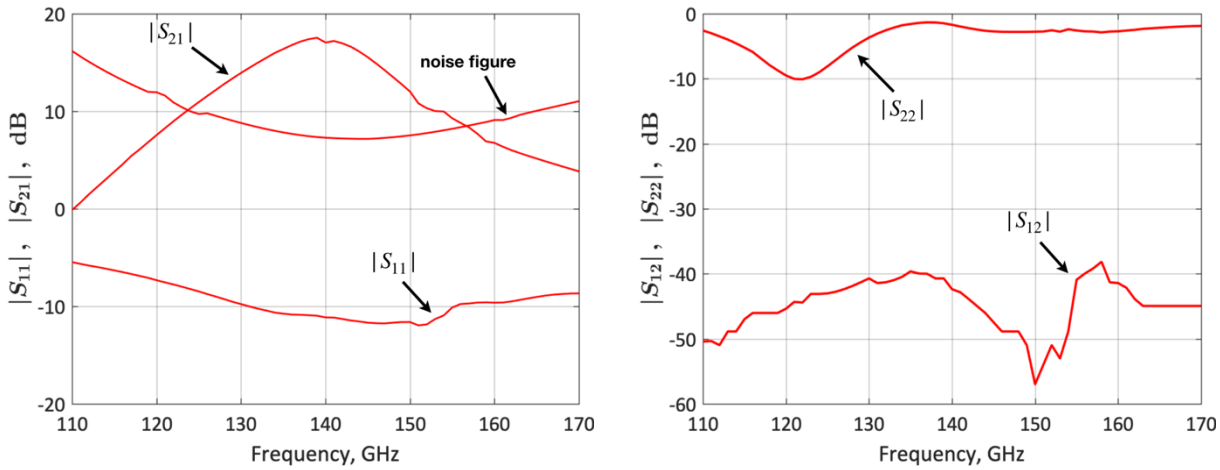


Fig. 5.12. Simulated S-Parameters and F of the frequency-reconfigurable LNA for the upper-frequency state (140 GHz).

5.3.4. Fabrication and experimental characterization of the frequency-reconfigurable LNA

The frequency-reconfigurable LNA was fabricated using the IHP's 0.13-μm SG13G2 SiGe:C BiCMOS technology described in Chapter 2. Fig. 5.13 shows a picture of the fabricated frequency-reconfigurable LNA. The chip area is 651.4 µm × 583.3

μm including the RF and DC pads and 400.1 μm × 379.1 μm without including the RF and DC pads (core area).

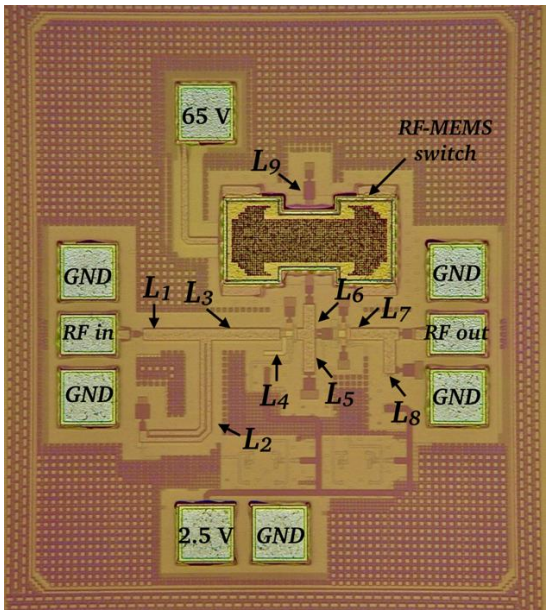


Fig. 5.13. Picture of the fabricated frequency-reconfigurable LNA.

The S-Parameters measurements were performed at the IHP's facilities. Fig. 5.14 and Fig. 5.15 compare the measured and simulated LNA S-Parameters for the lower- and upper-frequency states, respectively. The bias voltage applied to the LNA is 2.5 V and the lower-frequency state S-Parameters are obtained. After that, the RF-MEMS switch is actuated using external 65 V voltage to obtain the upper-frequency state S-Parameters. The voltage of 65 V might also be generated with an on-chip capacitive charge pump (CP) using stacked BEOL capacitors as charge/discharge capacitors [49], but a CP is not included in this design. The input power used for the measurement of both frequency states is -20 dBm.

The LNA features a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 18.4, –9.2, –42.5 and –6.5 dB respectively for the lower-frequency state. Concerning the upper-frequency state, a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 16.8, –10.5, –47.5 and –1.4 dB respectively are obtained.

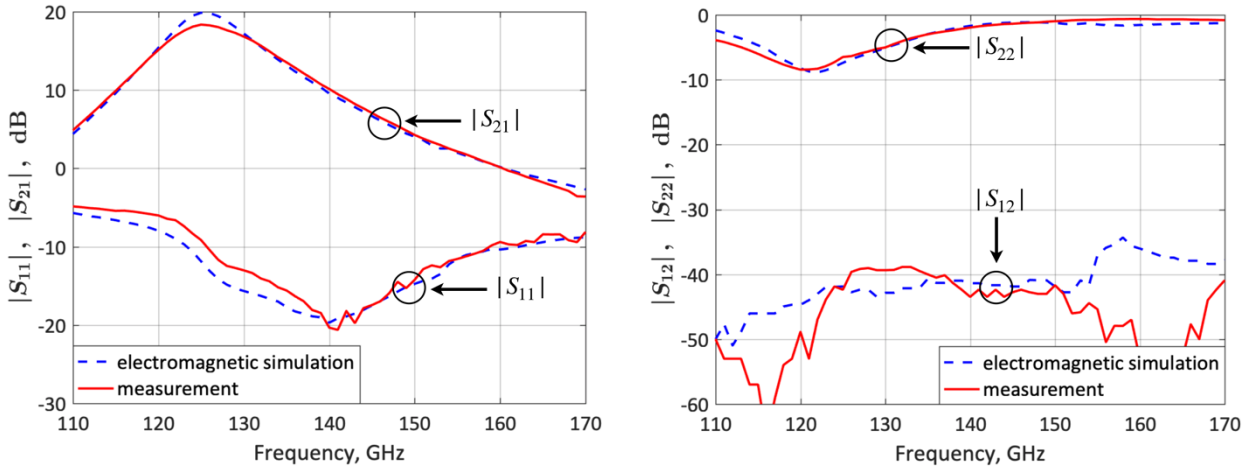


Fig. 5.14. Measured and simulated LNA S-Parameters for the lower-frequency state (125 GHz).

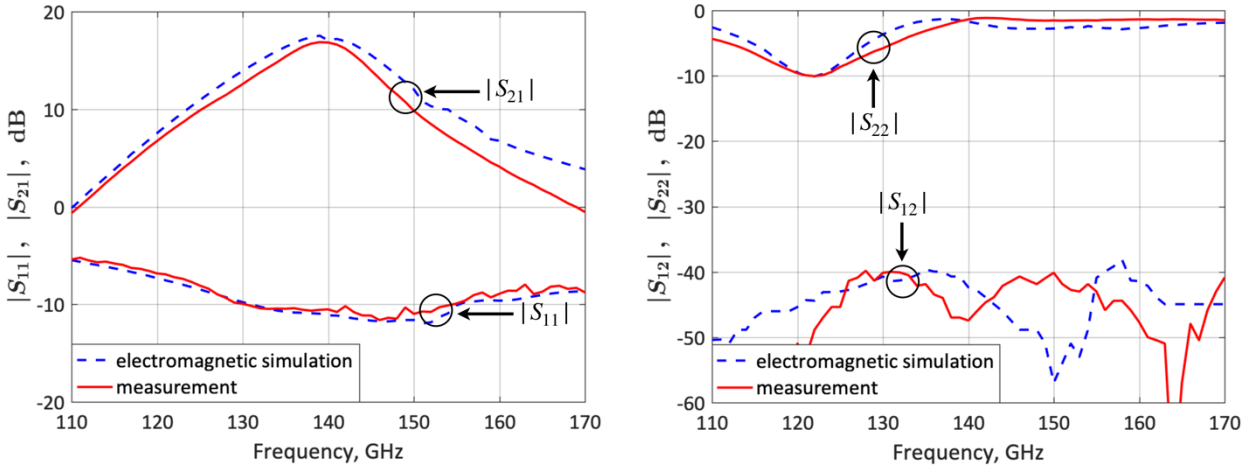


Fig. 5.15. Measured and simulated LNA S-Parameters for the upper-frequency state (140 GHz).

The F measurements of the LNA were performed in the VTT-Millimeter Wave Laboratory of Finland (VTT-Millilab). The measurement was performed on wafer using the Y-factor method. Hot and cold noise temperatures are produced by a noise diode Elva-1 ISSN-06. The noise power is down-converted to a 50 MHz IF using a subharmonic mixer with amplifier-multiplier chain Virginia Diodes Inc.-MixAMC-192 as LO, and measured using a noise figure analyzer Agilent N8973A.

The F simulations compared to the measured results are shown in Fig. 5.16. The measured F is 7.3 dB for the lower-frequency state and 7.9 dB for the upper-frequency state. The good agreement between simulations and measurements of the S-Parameters and F validates the proposed LNA concept and design methodology.

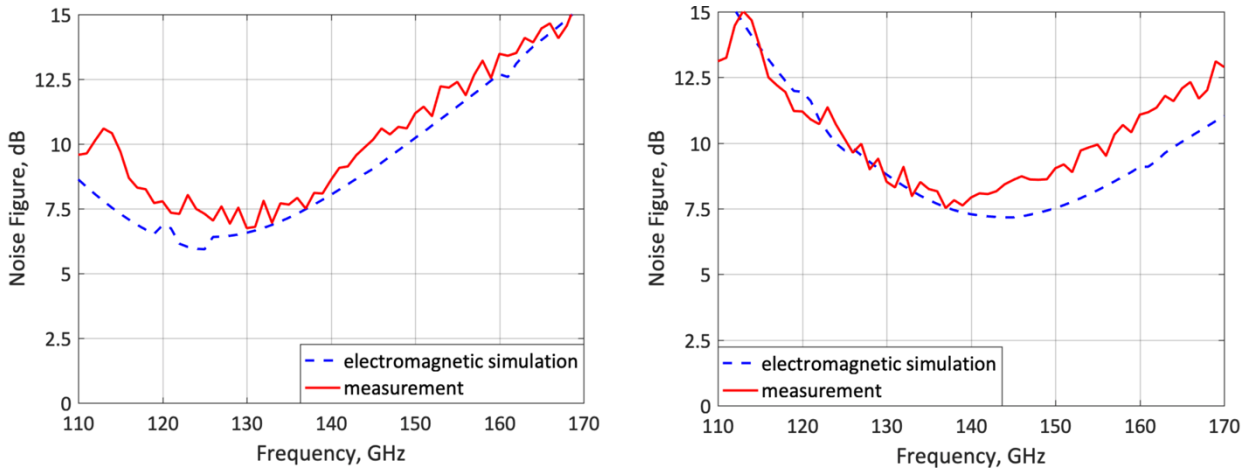


Fig. 5.16. Measured and simulated F for the lower- (125 GHz; left) and upper-frequency state (140 GHz; right).

5.3.5. Stability

The μ and μ' factors are simulated in order to obtain the stability of the frequency-reconfigurable LNA. The μ and μ' factors are defined in [50] as follows:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^{*}\Delta| + |S_{21}S_{12}|} \tag{22}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^{*}\Delta| + |S_{21}S_{12}|} \tag{23}$$

The condition μ > 1 or μ' >1 is necessary and sufficient for a two-port circuit to be unconditionally stable.

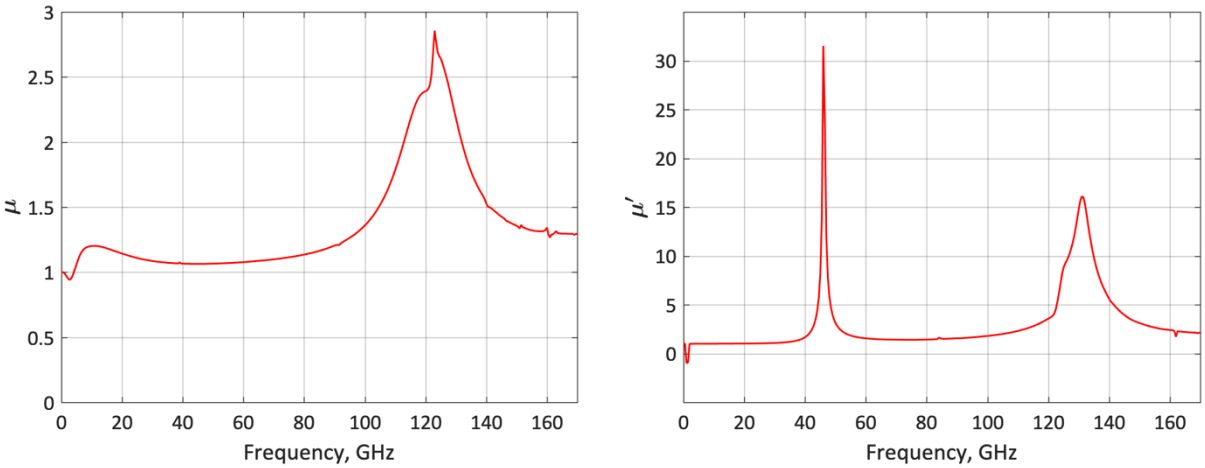


Fig. 5.17. Simulated μ (left) and μ' (right) factors for the frequency-reconfigurable LNA for the lower-frequency state (125 GHz).

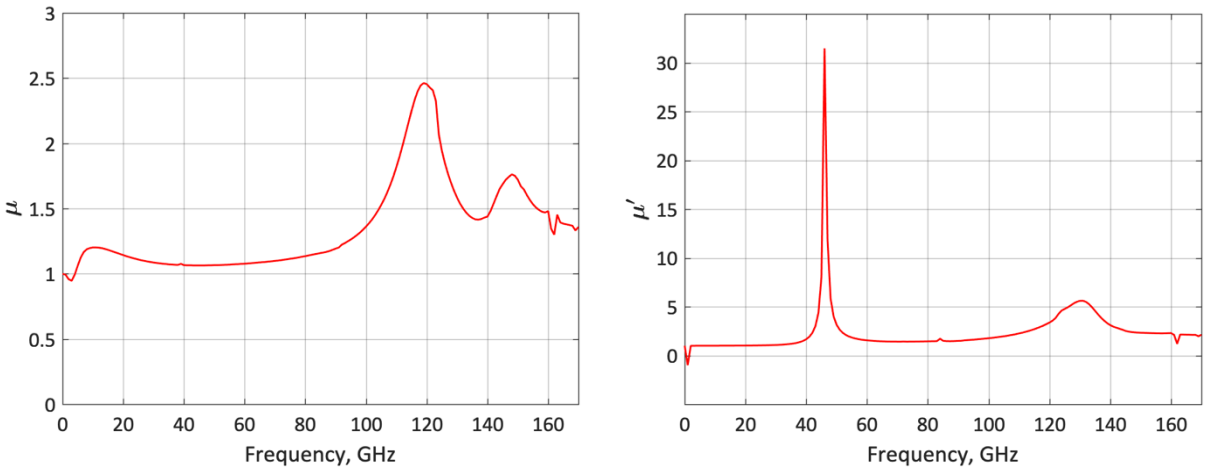


Fig. 5.18. Simulated μ (left) and μ' (right) factors for the frequency-reconfigurable LNA for the upper frequency state (140 GHz).

The μ and μ' factors are simulated in a frequency range from DC to 170 GHz for the lower- (Fig. 5.17) and upper-frequency (Fig. 5.18) states. For both frequency states, the LNA is unconditionally stable at all frequencies greater than 4 GHz. The minimal μ and μ' factors are μ = 1.005 and μ' = 1 from DC to 170 GHz. The stability factors μ and μ' are also calculated using the measurements of the fabricated LNA; the frequency range is 110 to 170 GHz (Fig. 5.19 and Fig. 5.20).

Fig. 5.19 illustrates the calculated μ and μ' factors obtained from the measurements for the lower-frequency state. Both stability factors are above 1 for the measured 110 to 170 GHz frequency range. The minimal μ and μ' factors are μ = 1.07 and μ' = 1.71, which confirm that the LNA is unconditionally stable for the 110 to 170 GHz frequency range.

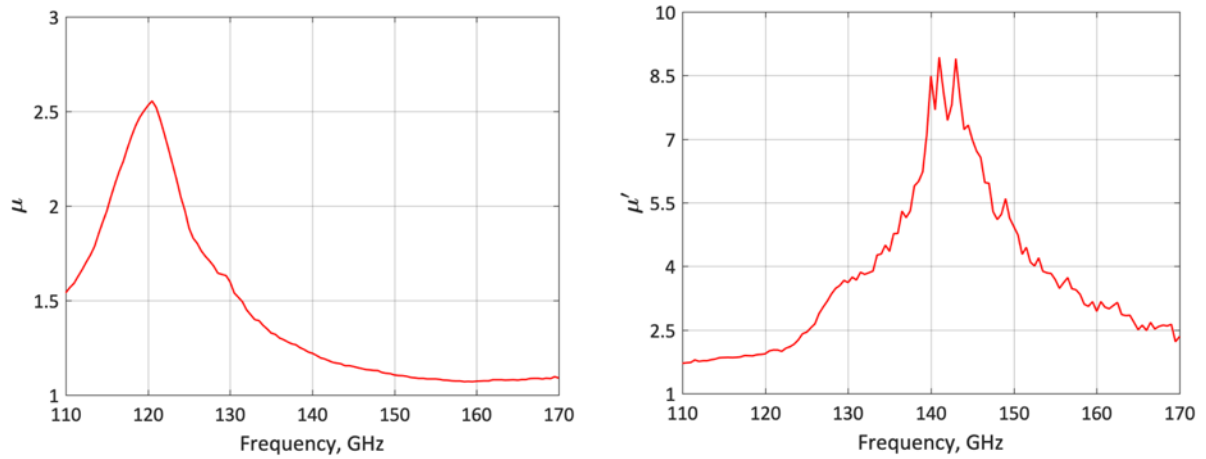


Fig. 5.19. Calculated μ (left) and μ' (right) factors obtained from measurements for the frequency-reconfigurable LNA for the lower frequency-state (125 GHz).

Concerning the upper-frequency state, the measured μ and μ' stability factors are illustrated in Fig. 5.20. Both stability factors are above 1 for the measured frequency range, and the minimal μ and μ' factors are μ = 1.03 and μ' = 1.5.

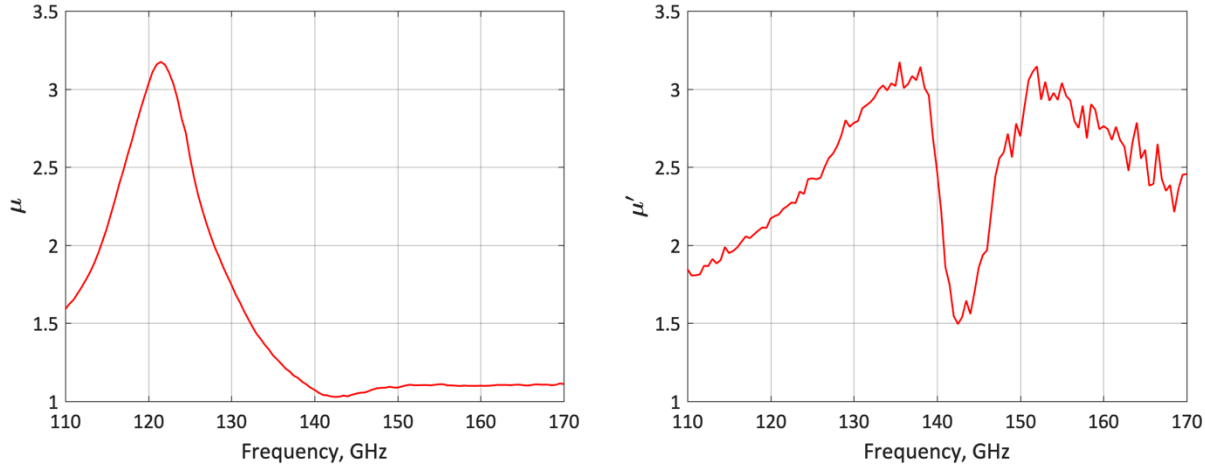


Fig. 5.20. Calculated μ (left) and μ' (right) factors obtained from measurements for the frequency-reconfigurable LNA for the upper frequency state (140 GHz).

These results confirm that the LNA is unconditionally stable for the 110 to 170 GHz frequency range for the upper-frequency state.

5.3.6. 1-dB gain compression point

The 1-dB gain compression point is defined as the input power (P_{in}) applied to and amplifier that causes the output power (P_{out}) to decrease 1 dB compared to the theoretical small-signal power output.

The simulated amplifier output power for an input power range from -50 dBm to 0 dBm is illustrated in Fig. 5.21 for both frequency states.

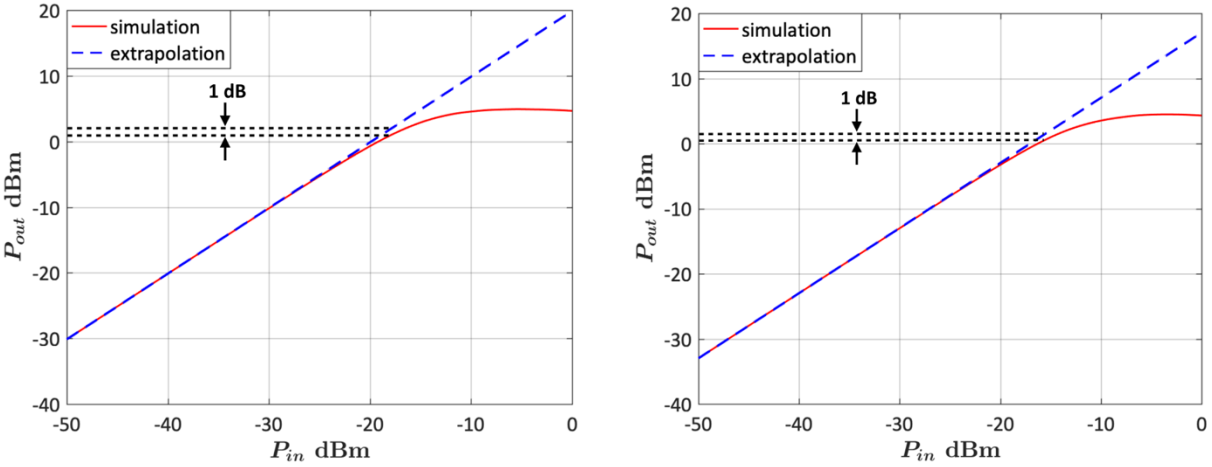


Fig. 5.21. 1-dB gain compression point for the lower- (left) and upper-frequency (right) states.

The obtained output power is compared to the theoretical small-signal output power, and the input 1-dB compression point (Input P1dB) is obtained. The calculated

Input P1dB is –17.8 dBm for the lower-frequency state and –15.2 dBm for the upper frequency state.

5.3.7. Bias circuit of the LNA: current mirror

A cascode current mirror circuit is used to bias all the transistor bases of the frequency-reconfigurable LNA. It has been designed to provide the required collector currents, and the necessary base-emitter voltages (V_{BE}) to maintain the transistors operating in their active mode.

The main goal of the standard current mirror is to produce a constant current in an active device that is copied from another active device. The voltage of the diode (V_D) illustrated in Fig. 5.22a depends on the temperature and the current flowing through it. If the diode current increases, V_D will increase and V_{BE} will be also incremented. This causes the emitter current to rise, thus increasing the collector current, which means the transistor emitter current will match the diode current. If the diode current is modified using the resistor R_{in}, then the transistor's emitter current is also modified. A transistor with a feedback and the same size as transistor Q_{mc1} can be used instead of a diode as shown in Fig. 5.22b (standard current mirror circuit).

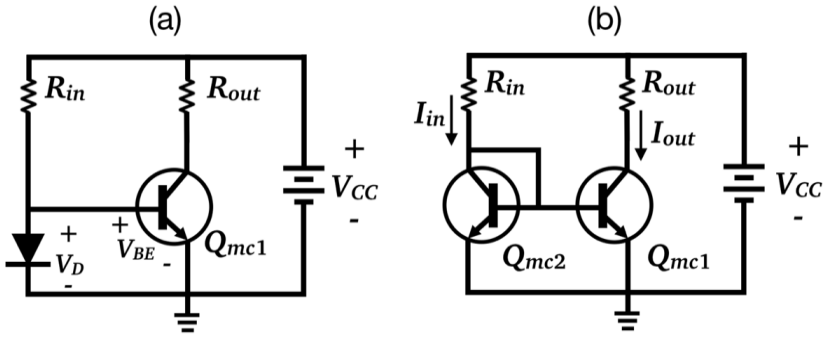


Fig. 5.22. Diode connected to the emitter-base junction of a transistor (a) and the standard current mirror circuit (b).

The equation that describes the relationship between I_{in} and I_{out} can be obtained from the analysis of the circuit shown in Fig. 5.22b [51]:

$$I_{out} = I_{in}\left(1 - \frac{2}{\beta_f + 2}\right) \tag{24}$$

where β_f is the common-emitter current gain of the transistor. Since β_f is usually large, equation 24 can be rewritten as follows:

$$I_{out} \approx I_{in} \tag{25}$$

If transistors Q_{mc1} and Q_{mc2} are not the same size (different number of emitter fingers), the current gain will be $A = {}^{M}/_{N}$, where M and N are the number of emitter fingers of transistors Q_{mc1} and Q_{mc2} respectively. In other words, if a gain higher than 1 is needed, the transistor Q_{mc1} must have a larger number of emitter fingers than transistor Q_{mc2}.

An alternative to the standard current mirror approach is the cascode current mirror (Fig. 5.23). In this case Q_{mc3} and Q_{mc4} are connected as a standard current mirror, and Q_{mc2} biases the base of Q_{mc1}.

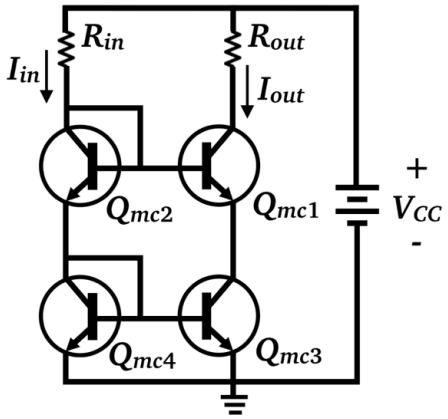


Fig. 5.23. Cascode current mirror circuit.

In the same way as it was done for the standard current mirror, an equation that relates I_{in} and I_{out} can be obtained from the analysis of the circuit shown in Fig. 5.23:

$$I_{out} = I_{in}\left(1 - \frac{4\beta_f + 2}{\beta_f^2 + 4\beta_f + 2}\right) \tag{26}$$

and since β_f is usually large, the above equation can be rewritten as:

$$I_{out} = I_{in}\left(1 - \frac{4}{\beta_f + 4}\right) \tag{27}$$

This equation shows that the difference between the currents I_{in} and I_{out} is larger when compared to its standard current mirror counterpart. Despite of this, the cascode current mirror is preferred since the configuration implemented in the LNA is also cascode.

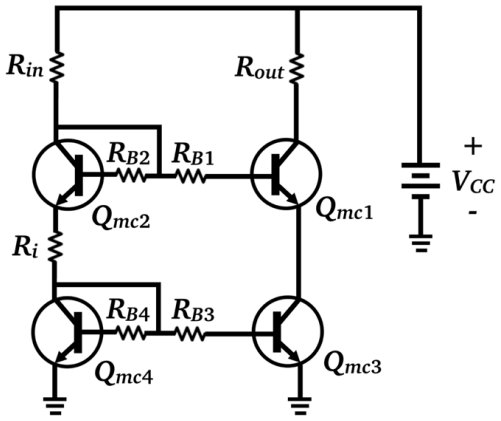


Fig. 5.24. Cascode current mirror circuit included in the frequency-reconfigurable LNA design.

Fig. 5.24 illustrates the cascode current mirror circuit implemented in the LNA design. The added resistor R_i maintains the transistor Q_{mc3} in the active mode by increasing negatively its base-collector voltage (V_{BC}). Resistors R_{RB1} and R_{RB3} prevent the RF signal from interfering with the bias circuit while letting the DC pass. For this case, the current gain is defined only by the size of transistor Q_{mc3}, but also it can be controlled using R_{RB2} and R_{RB4} without modifying the size of Q_{mc3}.

In the same way as it was done for the previous current mirror circuits, an equation that relates currents I_{in} and I_{out} can be obtained from the analysis of the circuit shown in Fig. 5.24. However, since the transistors Q_{mc1} and Q_{mc3} used in the LNA design (Q_1, Q_2, Q_7 and Q_8 of Fig. 5.7) are different in size from Q_{mc2} and Q_{mc4}, the β_f of the transistors is also different. Taking this into account, I_{out} is obtained:

$$I_{out} = \frac{\beta_4\beta_1\beta_3}{(\beta_4+1)(\beta_1+1)\beta_3 + \beta_1\beta_3 + \beta_1(\beta_4+1)} I_{in} \tag{28}$$

Since β_1, β_3 and β_4 are usually large, the above equation can be rewritten as follows:

$$I_{out} \approx I_{in} \tag{29}$$

5.4. Frequency-reconfigurable LNA design with a standard input matching network

A second frequency-reconfigurable LNA was designed, simulated, fabricated and characterized. The only difference between the previous and the new design is the IMN. The LNA of the second design includes a standard line-stub-line IMN (shown in Fig. 5.8b) but the other matching networks, the implemented transistors

and values of resistors and capacitors remain the same. The operation frequencies (125 and 140 GHz), design methodology and simulation procedure are the same used for the previous LNA design.

The design is also fabricated using IHP's 0.13-μm SG13G2 SiGe:C BiCMOS technology. Fig. 5.25 shows a picture of the second LNA design. The chip area is 700 µm × 583.3 µm including the RF and DC pads and 452.8 µm × 379.1 µm without including the RF and DC pads. Compared to the previous design, the size of the chip is increased by 7.5%/13.2% with/without the RF and DC pads respectively.

The comparison between the measured and simulated S-Parameters is shown in Fig. 5.26 for the lower-frequency state and in 5.27 for the upper-frequency state. The S-Parameters measurements were also performed at the IHP's facilities.

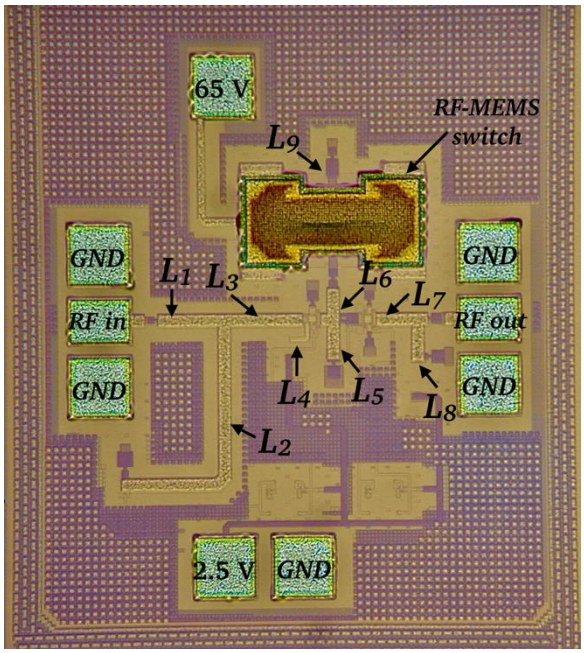


Fig. 5.25. Picture of the fabricated second frequency-reconfigurable LNA design.

The LNA features a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 16.9, –9, –42 and –7.5 dB respectively for the lower-frequency state. Concerning the upper-frequency state, a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 16, –11.1, –43 dB and –1.7 respectively were obtained.

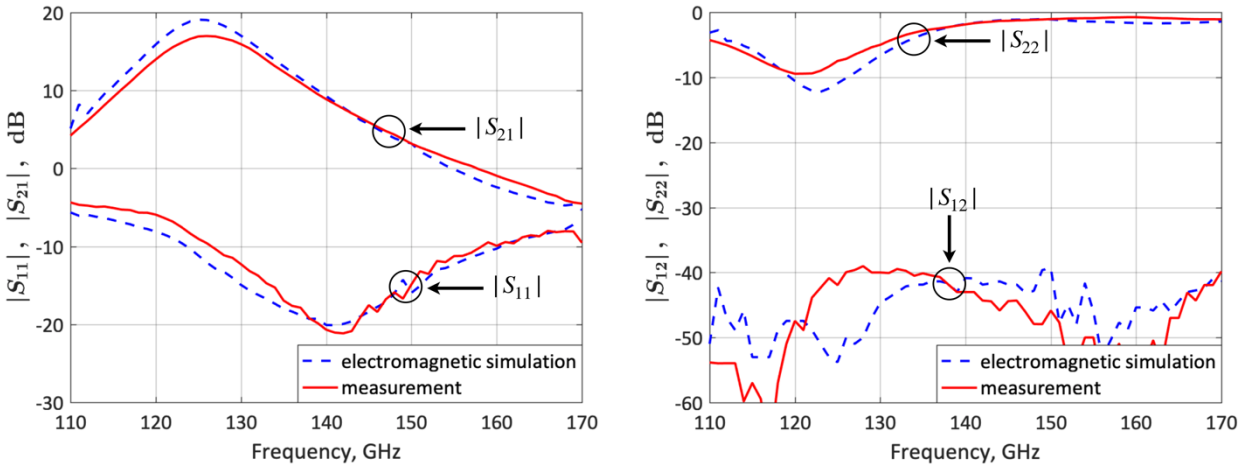


Fig. 5.26. Measured and simulated lower-frequency state (125 GHz) S-Parameters for the second LNA design.

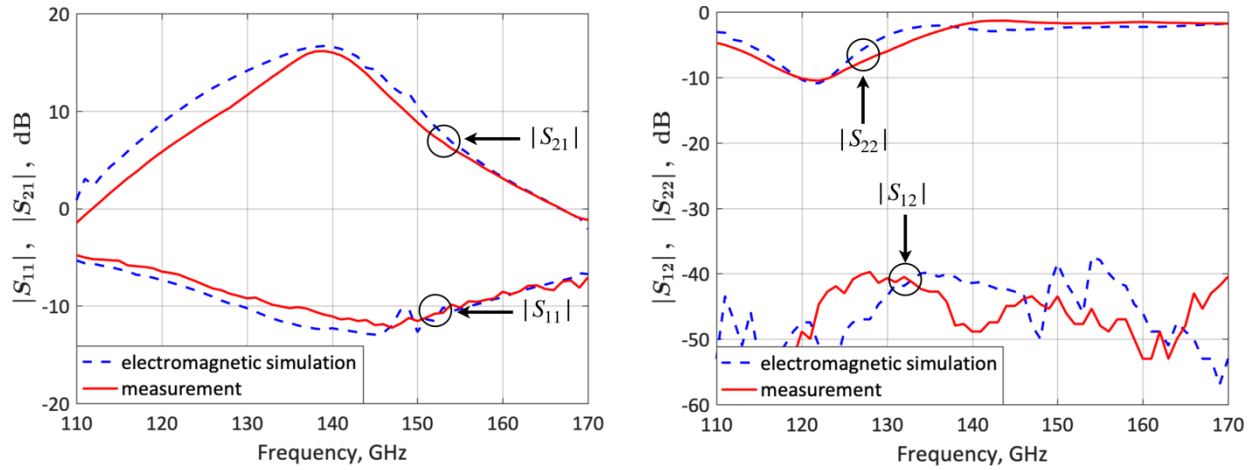


Fig. 5.27. Measured and simulated upper-frequency (140 GHz) state S-Parameters for the second LNA design.

The F measurements of the LNA were also performed in the VTT-Millilab premises. The F simulations compared to the measurements are shown in Fig. 5.28. The measured F is 7.3 dB for the lower-frequency state and 7.9 dB for the upper-frequency state. The S-Parameters and F measurements are in good agreement with the obtained simulations thus validating the second LNA design concept.

The simulated μ and μ' factors were obtained and show that the frequency-reconfigurable LNA is unconditionally stable at all frequencies greater than 4.2 and 4.7 GHz for the lower- and upper-frequency states respectively. The minimal simulated μ and μ' are μ=1.001/μ'=1.01 and μ=1.001/μ'=1.002 for the lower- and upper-frequency states respectively. The calculated μ and μ' factors using the obtained measurements are both above 1 for the measured frequency range of 110 to 170 GHz for both lower- and upper-frequency states. The minimal measured μ and μ'

are μ=1.1/μ'=1.63 and μ=1.13/μ'=1.73 for the lower- and upper-frequency states respectively.

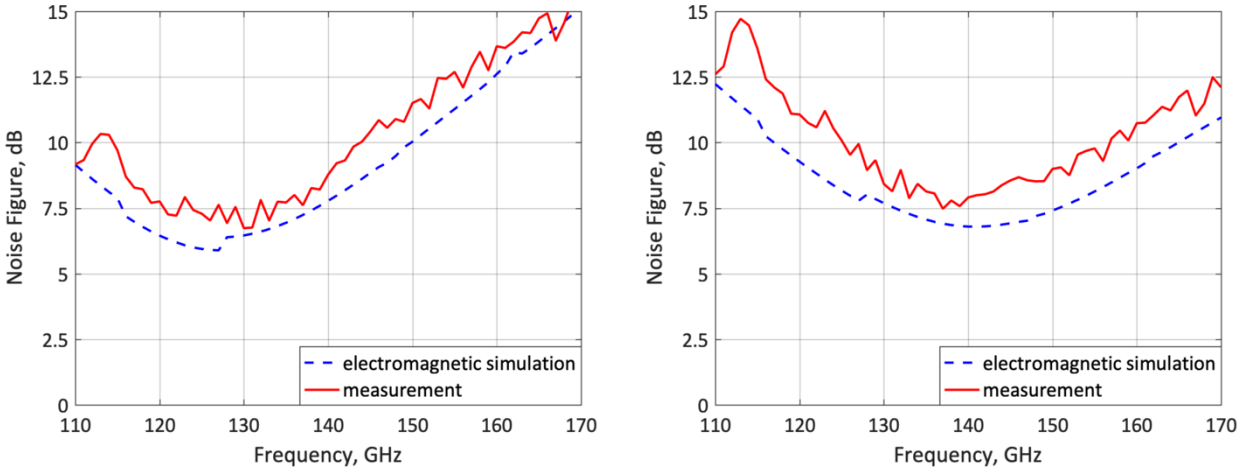


Fig. 5.28. Measured and simulated *F* for the lower- (125 GHz; left) and upper-frequency state (140 GHz; right) for the second LNA design.

The simulated Input P1dB is –16 dBm for the lower-frequency state and –11.2 dBm for the upper-frequency state.

The performance of the LNA design with standard microstrip line IMN is compared to the LNA design with multimodal IMN in Table 5.3.

Table 5.3. Comparison of the measured performance of the two LNA designs.

	Coupled microstrip line IMN (125GHz/140GHz)	Standard microstrip line IMN (125GHz/140GHz)
$\lvert S_{21} \rvert$ (dB)	18.4/16.8	16.9/16
$\lvert S_{11} \rvert$ (dB)	−9.2/−10.5	−9/−11.1
$\lvert S_{12} \rvert$ (dB)	−42.5/−47.5	−42/−43
$\lvert S_{22} \rvert$ (dB)	−6.5/−1.4	−7.5/−1.7
F (dB)	7.3/7.9	7.3/7.9
Power consumption (mW)	37.5	37.5
Input P1dB (dBm)	−17.8/−15.2	−16/−11.2
Size with pads (mm²)	0.38	0.408
Size without pads (mm²)	0.151	0.171

5.5. Frequency-reconfigurable LNA design with a multimodal TLM input matching network

The TLM structures already studied in Chapter 3, have demonstrated a wide Smith chart-impedance coverage and compactness, which make them suitable to implement impedance tuners (discussed in Chapter 4) and impedance matching networks. As demonstrated in Chapter 3, almost a 100% Smith chart coverage is obtained when the TLM structure length (Fig. 3.32) is tuned and a proper combination of open-circuited/short-circuited stubs is connected to the two series-outer strip gaps. Based on this analysis, a multimodal TLM input matching network is proposed for a third design of the frequency-reconfigurable LNA. The new multimodal IMN and a rearrangement of the pads and the amplifier bias network allow a considerable size reduction of the design. Some minor changes in some microstrip line lengths and capacitors values are also made in order to improve the LNA performance. Although the lower-frequency state remains at 125 GHz, a frequency of 143 GHz was achieved for the upper-frequency state.

5.5.1. Design methodology of the frequency-reconfigurable LNA

The design methodology is the same implemented for the LNAs described in Section 5.3. The amplifier was designed to achieve low noise, but also maintaining a high and balanced gain at the two frequency states.

As it was done for the previous designs, the load reflection coefficient Γ_L (Fig. 5.2) is selected to attain a high and balanced gain at both frequency states (125 and 143 GHz) using the microstrip line and stub of the OMN (L_7 and L_8) illustrated in Fig. 5.3. The obtained gain for the second stage (G_{p2}) is 11.6 dB at 125 GHz and 9.1 dB at 143 GHz, while the maximal gain (G_{p2max}) is 14.8 dB at 125 GHz and 13.2 dB at 140 GHz.

The reconfigurable ISMN is composed by the microstrip lines L_5, L_6 and L_9; the RF-MEMS switch and capacitors C_4, C_9, C_{10} and C_{11} as shown in Fig. 5.4. A load reflection coefficient Γ_{L1} is synthesized through these elements in order to balance the power gain of each stage, G_{p1} and G_{p2} (and thus the LNA power gain G_p) at both frequency states (125 GHz and 143 GHz), at the expense of being slightly lower than G_{pmax}. The achieved gain G_{p1} for the selected Γ_{L1} is 11.2 dB at 125 GHz and 9.9 dB at 143 GHz. The computed gain of the LNA G_p is 19.5 dB at 125 GHz and 18.4 dB at 143 GHz, 2.4 and 2.9 dB less than the maximal gain respectively.

The IMN was then designed using the multimodal TLM structure already studied in Chapter 4 (Fig. 3.32) to simultaneously accomplish a low F and $|\Gamma_{IN}|$, both balanced at the two frequency states. As it was done for the previous designs, the $|\Gamma_{IN}|$ circle is plotted on the Smith chart in the Γ_{L1} plane as shown in Fig. 5.29. The calculated F for the selected Γ_S is 5.9 dB at 125 GHz and 6.2 dB at 143 GHz, which is

0.3 and 0.2 dB higher than the F_{min} respectively. The F and $|\Gamma_{IN}|$ circles intersect the Γ_{L1} required to obtain a G_{p1} of 11.2 and 9.9 dB at 125 and 143 GHz respectively.

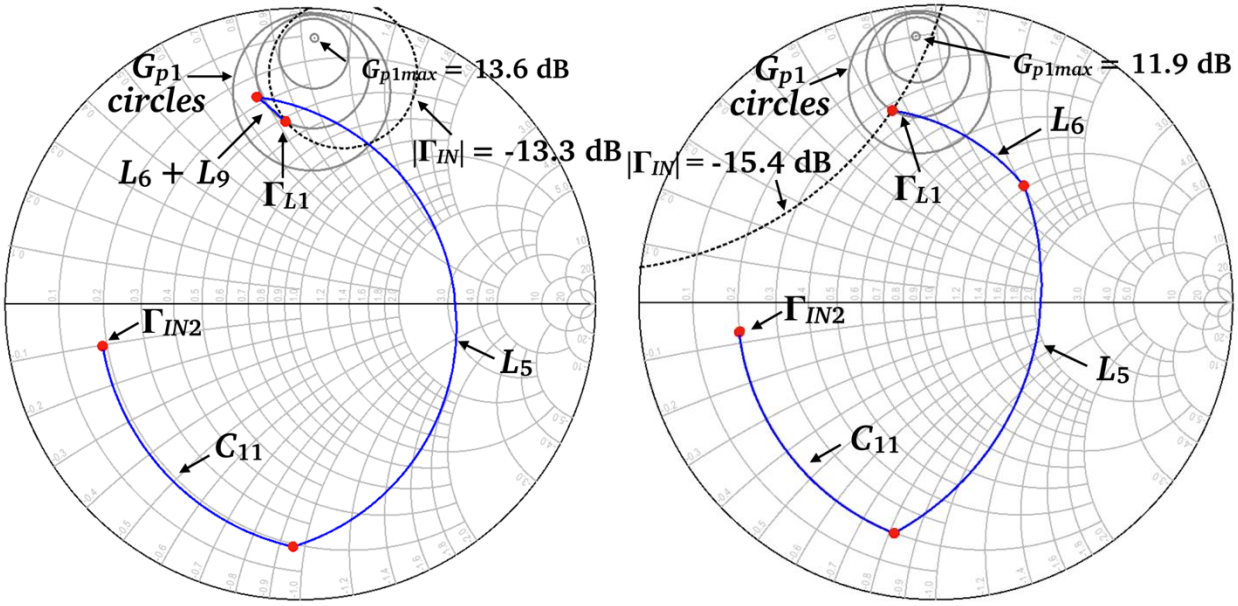


Fig. 5.29. Constant F and $|\Gamma_{IN}|$ circles and G_{p1} circles at 125 (left) and 143 GHz (right).

The proposed frequency-reconfigurable LNA is illustrated in the schematic of Fig. 5.30. As it was mentioned before, the IMN is implemented with a multimodal TLM structure which allows a size reduction of the overall LNA. The capacitance value of capacitor C_2 is increased in order to accomplish a better decoupling of the RF-signal. The ISMN follows the same reconfiguration principle of the previous designs with a slight change in the length of L_5 and a major increase in the length of L_9; the length of L_6 and capacitance values of capacitors C_9, C_{10} and C_{11} remain the same as the previous designs. Concerning the OMN, the lengths of L_7 and L_8 also remain the same.

As in the previous designs, the ISMN (L_5, L_6 and L_9) and OMN (L_7 and L_8), as well as line L_4 are microstrip lines. The IMN multimodal TLM structure and microstrip lines L_5, L_6, L_7 and L_8 are designed with the top-most metal layer of the IHP's SG13G2 technology (TM2), while L_9 is designed using the TM1 layer and L_4 using a stack of three metallic layers (M2, M3 and M4).

The amplifier is biased with a V_{CC} = 2.5 V and I_{CC} = 15 mA using current mirrors (Q_5 Q_6, Q_7 and Q_8) and bias resistors (R_1 and R_2). The two cascode stages are unconditionally stable at all frequencies. All the transistors used in both stages are the same size as those used for the previous designs. While the Stage 1 of LNA (Fig. 5.30) is composed by transistors Q_1 and Q_2, with 5 and 10 emitter fingers respectively (biased with a collector current of 4.8 mA), the Stage 2 is composed by transistors Q_3 and Q_4 with 10 emitter fingers each (biased with a collector current of 8.2 mA).

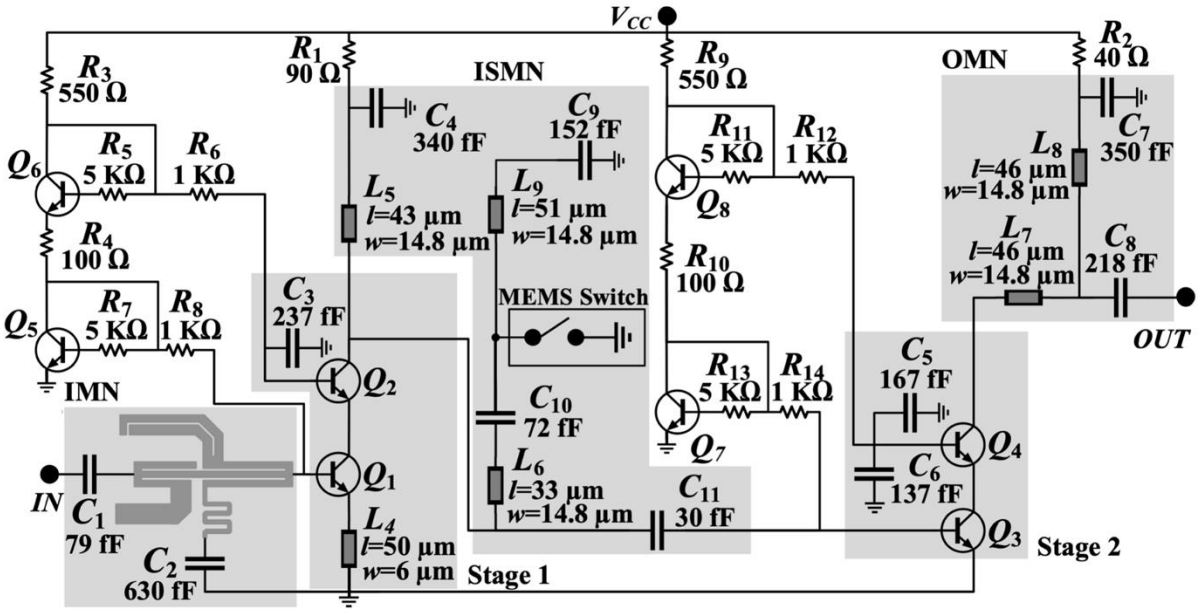


Fig. 5.30. Schematic of third frequency-reconfigurable LNA design.

5.5.2. Multimodal TLM input matching network

The major change included in this new LNA design is the implementation of a multimodal TLM structure in the IMN. Since the IMN is one of the biggest elements of the circuit, replacing the standard line-stub-line IMN with a multimodal TLM compact structure allows reducing the overall size of the LNA. The multimodal IMN consists of a TLM section with two series gaps in its outer strips and one short-circuited, one open-circuited, and one open-circuited coupled microstrip stub connected to them (Fig. 5.31). The three fundamental modes, *ee*, *oo* and *oe* propagate simultaneously in the TLM structure, and interact at any asymmetry or transition. With these interactions, a large overall electrical size is attained in a compact circuit area. The *oo* and *oe* modes are excited at the gaps and TLM-to-stub transitions by the *ee* mode, as shown in Fig. 3.32 (Chapter 3).

The dimensions illustrated in Fig. 5.31 are optimized using the modal equivalent circuits already studied in Chapter 3 (Fig. 3.33) to synthesize the required Γ_S. The size of the proposed structure is 126 µm × 103 µm and achieves a 75.6% area reduction compared to a standard line-plus-stub microstrip matching network (234 µm × 227 µm).

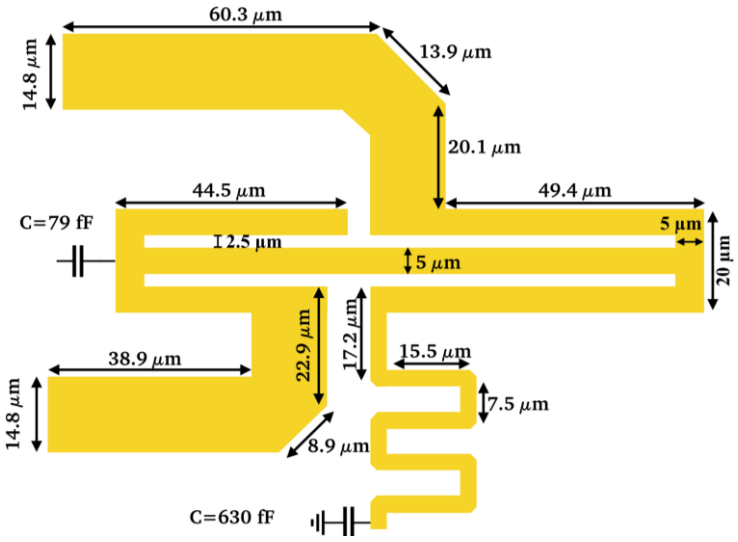


Fig. 5.31. Multimodal TLM structure implemented in the IMN.

5.5.3. Fabrication and experimental characterization of the frequency-reconfigurable LNA

The LNA described in this Section is fabricated with the IHP's 0.13-μm SG13G2 SiGe:C BiCMOS technology described in Chapter 2. A picture of the fabricated LNA is illustrated in Fig. 5.32. The chip area is 536 μm × 480 μm and the core area is 327 μm × 326 μm.

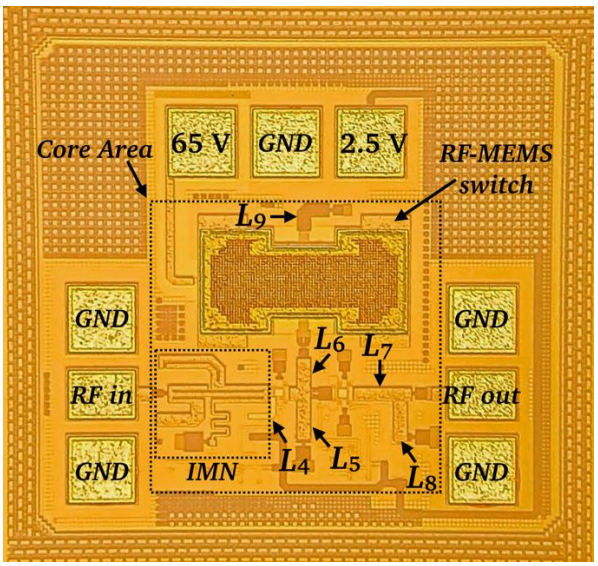


Fig. 5.32. Picture of the fabricated third frequency-reconfigurable LNA design including a multimodal TLM IMN.

Circuit/electromagnetic co-simulations are performed using Keysight ADS and Momentum. Microstrip lines, pads and capacitors are simulated using electromagnetic simulation and a co-simulation element is created from it. The IHP's design kit models of transistors, resistors and the RF-MEMS switch are connected to the co-simulation element. After that, a 110 to 170 GHz two-port simulation is performed to obtain the S-Parameters and F of the frequency-reconfigurable LNA. The RF-MEMS switch model can be adjusted to "up" or "down" state to perform the simulations for the lower- and upper-frequency states respectively.

Fig. 5.33 and 5.34 compare the simulated S-Parameters to the measured results of the frequency-reconfigurable LNA at lower- and upper-frequency states respectively. The LNA features a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 18.2, –9.7, –40.1 and –5.6 dB respectively for the lower-frequency state. Concerning the upper-frequency state, a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 16.1, –12.2, –45 and –2.1 dB respectively were obtained.

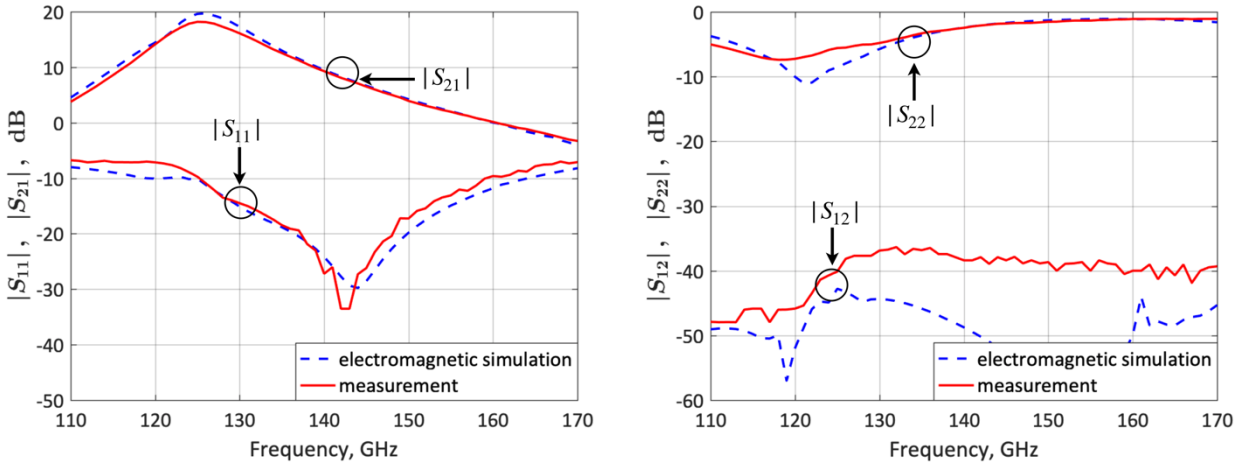


Fig. 5.33. Measured and simulated LNA S-Parameters for the lower-frequency state (125 GHz) of the third LNA design.

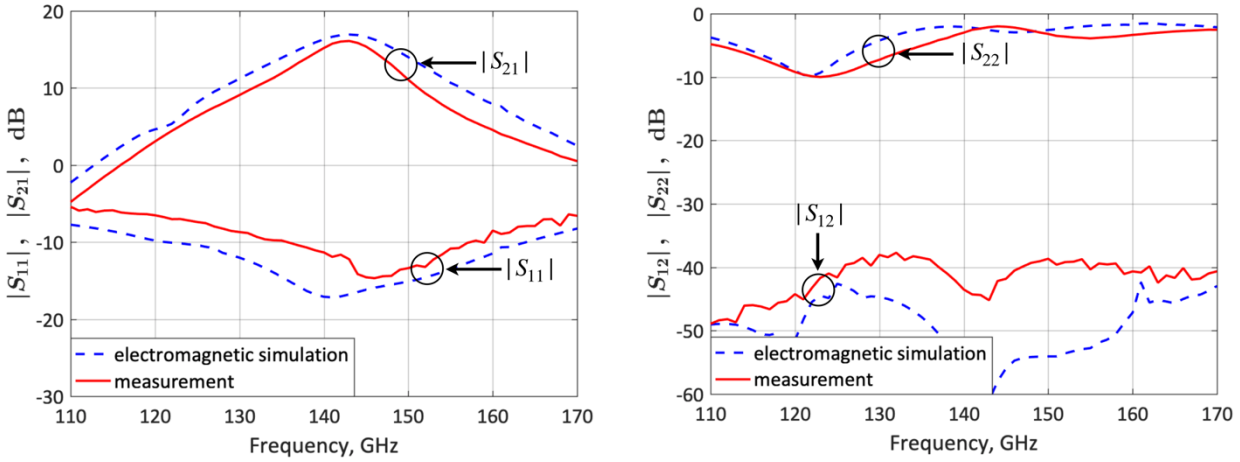


Fig. 5.34. Measured and simulated LNA S-Parameters for the upper-frequency state (143 GHz) of the third LNA design.

The F measurements of the LNA were performed on wafer using the Y-factor method in the VTT-Millilab premises. The details of the Y-factor method for noise measurements are described in subsection 5.3.4.

Fig. 5.35 compares the F simulations to the measurements. The measured F is 7 dB for the lower-frequency state and 7.7 dB for the upper-frequency state. The S-Parameters and F measurements are in good agreement with the obtained simulations thus validating the frequency-reconfigurable LNA concept.

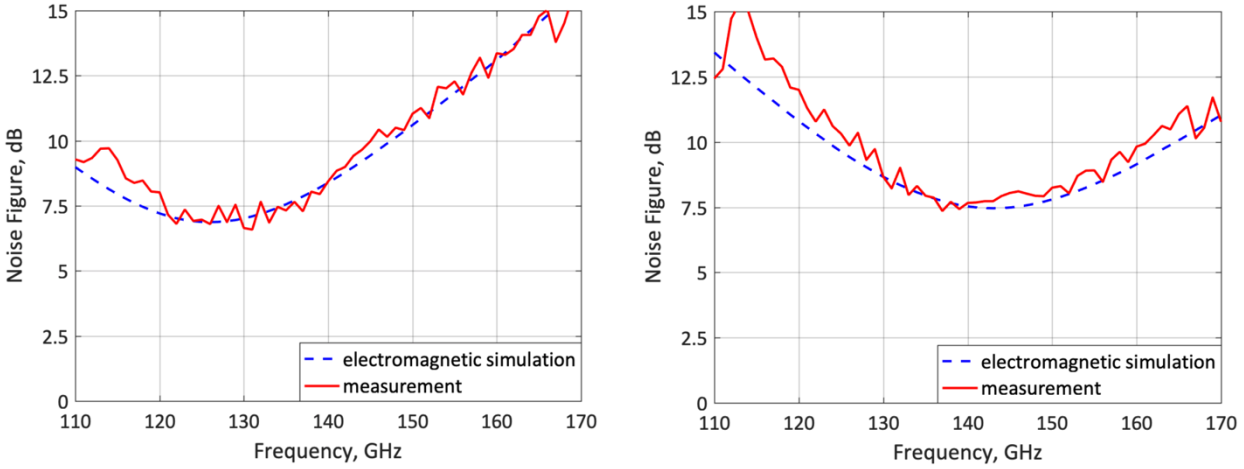


Fig. 5.35. Measured and simulated F for the lower- (125 GHz; left) and upper-frequency state (143 GHz; right) for the third LNA design.

Table 5.4. Comparison of the measured performance of the three LNA designs.

	Coupled microstrip line IMN (125 GHz/140 GHz)	Standard microstrip line IMN (125 GHz/140 GHz)	Coupled microstrip line IMN (125 GHz/143 GHz)
$\lvert S_{21} \rvert$ (dB)	18.4/16.8	16.9/16	18.2/16.1
$\lvert S_{11} \rvert$ (dB)	−9.2/−10.5	−9/−11.1	−9.7/−12.2
$\lvert S_{12} \rvert$ (dB)	−42.5/−47.5	−42/−43	−40.1/−45
$\lvert S_{22} \rvert$ (dB)	−6.5/−1.4	−7.5/−1.7	−5.6/−2.1
F (dB)	7.3/7.9	7.3/7.9	7/7.7
Power consumption (mW)	37.5	37.5	37.5
Input P1dB (dBm)	−17.8/−15.2	−16/−11.2	−17.3/−15.9
Circuit area (mm^2)	0.38	0.408	0.257
Core area (mm^2)	0.151	0.171	0.106

The μ and μ' factors are simulated in order to obtain the stability factor of the frequency-reconfigurable LNA. According to the simulation results, the LNA is unconditionally stable (μ > 1 and μ' >1) at all frequencies greater than 3 GHz for the lower- and upper-frequency states. The minimal simulated μ and μ' are μ=1.024/μ'=1.002 for both lower- and upper-frequency states. The μ and μ' factors are also obtained from the measured S-Parameters for the 110 to 170 GHz frequency range. According to the measured μ and μ' factors, the LNA is unconditionally stable (μ > 1 and μ' >1) in all the frequency range (110 to 170 GHz). The minimal calculated μ and μ' obtained from the measurements are μ=1.124/μ'=2.152 and μ=1.193/μ'=1.856 for the lower- and upper-frequency states respectively.

The simulated input-referred 1-dB gain compression point is -17.3 dBm for the lower-frequency state and -15.9 dBm for the upper-frequency state.

The performance of the LNA design with a multimodal TLM IMN is compared to the previous designs in Table 5.4.

5.6. Conclusions

The three frequency-reconfigurable LNA designs presented in this Chapter have demonstrated state-of-the-art performance for the D-band. The LNAs have been designed using IHP's 0.13μm SiGe:C BiCMOS technology (described in Chapter 2). All three LNAs have a gain higher than 16 dB and a F below 7.9 dB for both lower- and upper-frequency states. To the best knowledge of the author this is the first time the design, simulation and characterization of a frequency-reconfigurable LNA at D-band has been reported. A single RF-MEMS switch has been implemented in the ISMN as reconfigurable device in order to change the operation frequency.

A systematic method is presented in this Thesis for the design of frequency-reconfigurable LNAs. It can also be used for other amplifiers that requires two stages even if they are not reconfigurable.

The multimodal structures have demonstrated its compactness capabilities with the implementation of a coupled microstrip multimodal IMN and a TLM multimodal IMN in two of the designs presented (Section 5.3 and Section 5.5). The use of a coupled microstrip multimodal IMN achieves a core area reduction of 12%, while the implementation of a TLM multimodal IMN accomplish a core area reduction of 35%.

CHAPTER SIX

RECONFIGURABLE LOW-NOISE AMPLIFIER USING AN HBT-BASED RF SWITCH

RF-MEMS switches are key components for the implementation of reconfigurable circuits at D-band. They have lower losses, higher isolation, lower power consumption and higher linearity when compared to CMOS or bipolar RF switches. However, the implementation of CMOS or bipolar RF switches can still be useful when the main goal is accomplishing a compact design.

In this Chapter, a frequency-reconfigurable 120/140 GHz LNA with a HBT-RF switch is presented. It has been designed using the same method used for the LNA presented in Chapter 5. The LNA has been designed using IHP's 0.13 μm SG13G2 SiGe:C BiCMOS-MEMS technology. The obtained results are compared with the LNA designs presented in Chapter 5 and the advantages and disadvantages for the two approaches (using RF-MEMS switch or HBT-RF switch) are discussed. The LNA was simulated, fabricated and characterized in the 110 to 170 GHz frequency band.

6.1. HBT-based RF switch design

Using a RF-MEMS switch for the design of frequency-reconfigurable LNAs provides good performance at frequencies above 100 GHz due to its low losses, high linearity and high isolation, however it uses a large area of the circuit. An alternative to this approach is a HBT-based RF switch, which is very small in size compared to a RF-MEMS switch. Even if the HBT-RF switch does not have a good performance as the RF-MEMS switch, the LNA designs can take advantage of it to achieve very compact circuits.

An HBT-RF switch has been designed using the IHP's 0.13µm SG13G2 SiGe:C BiCMOS technology. The topology of the switch (Fig. 6.1) consists of three HBTs connected in cascade. The emitters serve as the input and the collectors as the output of the switch.

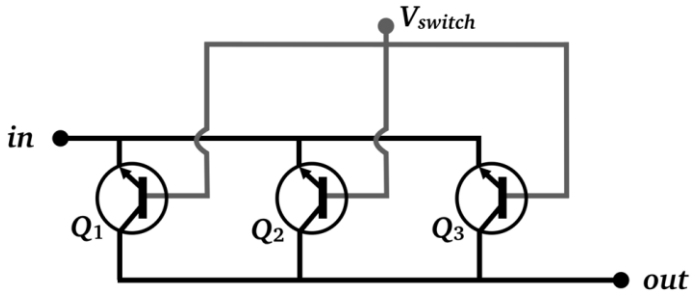


Fig. 6.1. HBT-RF switch topology.

When V_{switch} is set to 0 V, the transistors are in the cut-off region mode and they behave as a high impedance in parallel with a parasitic capacitance; the RF energy cannot pass from the input to the output of the switch. Fig. 6.2a illustrates the equivalent circuit for the HBT-RF switch in "OFF" state (C_{OFF} = 7.2 fF and R_{OFF} = 1.6 kΩ).

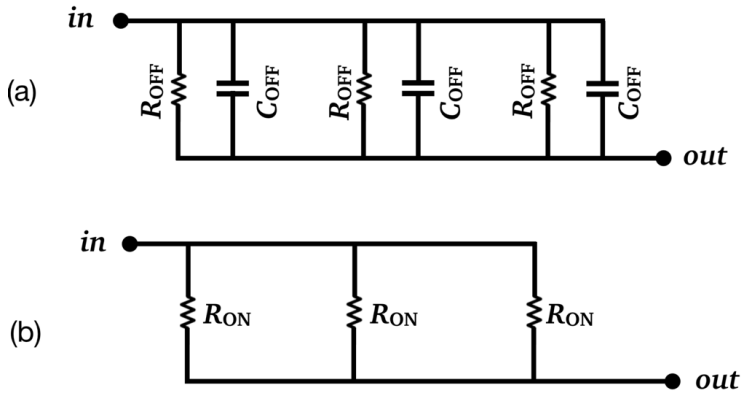


Fig. 6.2. Equivalent circuit for the HBT-RF switch in "OFF" (a) and "ON" (b) states.

When V_{switch} is set to 1 V, the transistors are in the saturation region mode and they behave as a low impedance (R_{ON} = 10 Ω). The equivalent circuit for the HBT-RF switch in "ON" state is shown in Fig. 6.2b.

Since the HBT-RF switch is intended to be used as reconfigurable device for the LNA designs presented in Chapter 5, it is connected as shown in Fig. 6.3. Connecting the HBTs of the switch in reverse saturation mode (transistor is flipped) isolates the emitter from the silicon substrate which reduces the parasitic capacitance between them. Also, the impedance in the "OFF" state is larger since the potential barrier in the conduction band in the emitter is larger than the collector [52]. The HBT-RF switch is composed by the transistors Q_1, Q_2 and Q_3 with 7 emitter fingers each. The base current is 5 mA for each transistor and the collector current is 1.9 mA for Q_1 and 1.7 mA for Q_2 and Q_3. By using three transistors R_{ON} is reduced thus improving the performance of the switch for the "ON" state. Since the gain for each stage is less at the upper-frequency state, improving the performance for the HBT-RF switch at the "ON" state make the total gain more balanced at 120 and 140 GHz.

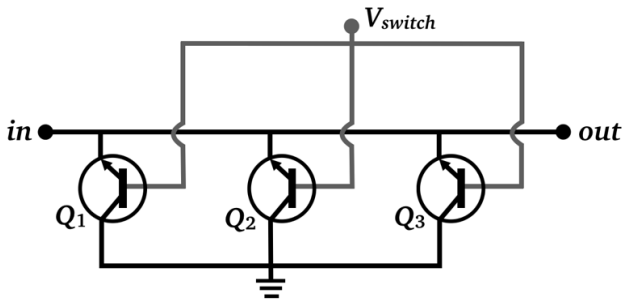


Fig. 6.3. Schematic of the HBT-RF switch connected to ground.

6.2. Frequency-reconfigurable LNA design using an HBT-based RF switch

The proposed amplifier introduced in this Chapter is a two-stage frequency-reconfigurable cascode LNA designed using IHP's 0.13 μm SG13G2 SiGe:C BiCMOS-MEMS technology (described in Chapter 2). The design concept is very similar to the one implemented for the previous proposed LNAs. However, instead of an RF-MEMS switch, a single HBT-based RF switch is used to select the operation frequency (120 or 140 GHz). The optimization of the LNA is focused on achieving a high gain and low noise at both frequencies, while maintaining a compact design. The LNA includes the same multimodal TLM IMN implemented in the design of Section 5.5.

6.2.1. Design methodology of the frequency-reconfigurable LNA

The methodology design is the same as the one described in subsections 5.3.1 and 5.5.1. The matching networks are optimized in order to obtain a low noise and high gain at both frequency-states.

The implemented OMN is the same used for the previous designs (illustrated in Fig. 5.3). A high and balanced gain are achieved for both frequency states selecting and appropriate reflection coefficient Γ_L (Fig. 5.2) by optimizing the microstrip line (L_7) and stub (L_8) of the OMN. The second stage gain (G_{p2}) is 11.2 dB at 120 GHz and 9.6 dB at 140 GHz, while the maximal gain (G_{p2max}) is 15.7 dB at 120 GHz and 13.8 dB at 140 GHz.

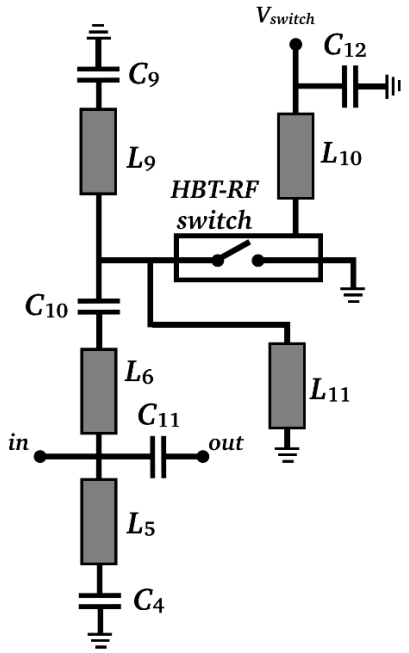


Fig. 6.4. Inter-stage matching network of the frequency-reconfigurable LNA.

The ISMN was designed to balance the power gain of each stage, G_{p1} and G_{p2} (and thus the LNA power gain G_p) at both frequency states (120 GHz and 140 GHz), at the expense of being slightly lower than G_{pmax}. It consists of microstrip line L_5, capacitors C_4, C_9, C_{10} and C_{11}, and a two-segment short stub composed by lines L_6 and L_9 (Fig. 6.4). The HBT-RF switch selects the length of the two-segment stub between $L_6 + L_9$ or L_6. If the voltage applied to the HBT-RF switch is 0 V ("OFF" state), the total length of the two-segment stub is equal to the length of $L_6 + L_9$ and the operation frequency is 120 GHz. If the voltage applied to the HBT-RF switch is 1 V ("ON" state), the total length of the two-segment stub is equal to the length of L_6 and the operation frequency is 140 GHz. Two new lines L_{10} and L_{11} are used in the ISMN. L_{11} adds an inductance in parallel to the HBT-RF switch transistors. This added inductance resonates with the transistors capacitances allowing to reduce their effect on the

switch in the "OFF" state. L_{10} is a $\lambda/4$ stub used as RF choke for the biasing of the HBT-RF switch, and C_{12} is a decoupling capacitor. The load reflection coefficient Γ_{L1} is synthesized using the ISMN trough lines L_5, L_6 and the capacitors C_{11} and C_{10}; L_9 is only used at 120 GHz. The achieved gain G_{p1} for the selected Γ_{L1} is 9.6 dB at 120 GHz and 8.9 dB at 140 GHz. The computed gain of the LNA G_p is 18.1 dB at 120 GHz and 16.9 dB at 140 GHz, 4.4 less than the maximal gain for both states.

The IMN is implemented using the multimodal TLM structure presented in Section 5.5. The dimensions of the structure (Fig. 5.31) are optimized to accomplish a low-noise figure and small $|\Gamma_{IN}|$ at both frequency states. The circle for a constant F and $|\Gamma_{IN}|$ is plotted in the Γ_{L1} plane as illustrated in Fig. 6.5. For the selected Γ_S the calculated F is 6.1 dB at 120 GHz and 6.5 dB at 140 GHz, which are 0.3 and 0.2 dB higher than F_{min} respectively. These circles intersect the Γ_{L1} necessary to obtain a G_{p1} of 9.6 dB and 8.9 dB for the lower- and upper-frequency states respectively. Therefore, using the proposed IMN and ISMN the required F, $|\Gamma_{IN}|$ and G_p for the LNA are achieved for both frequency states.

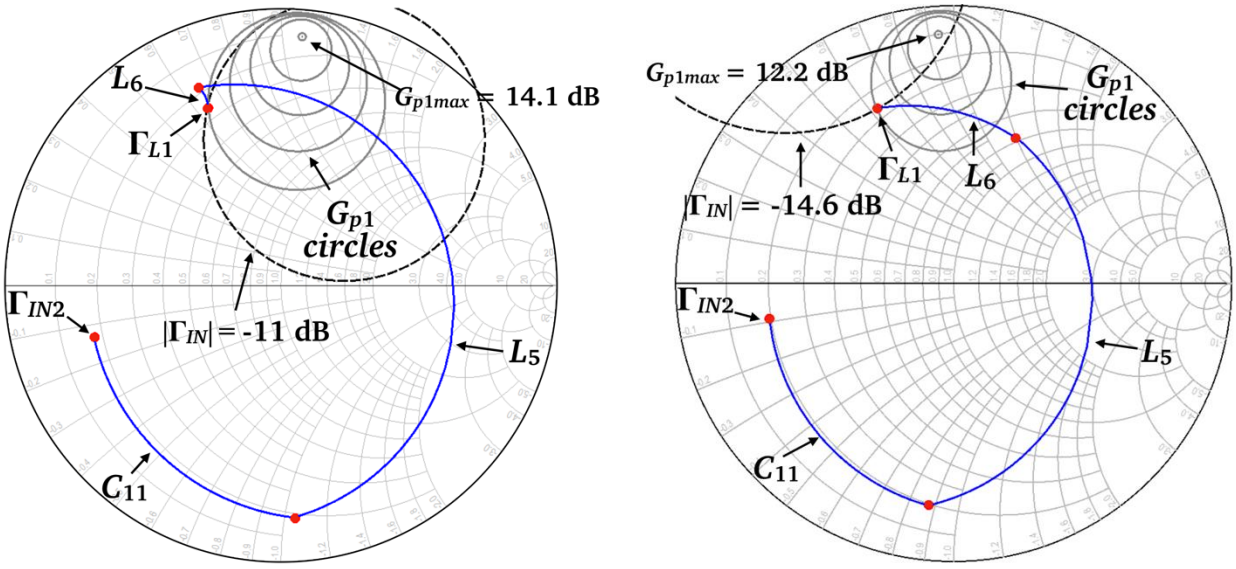


Fig. 6.5. Constant F, $|\Gamma_{IN}|$ and G_{p1} circles at 120 (left) and 140 GHz (right).

The proposed frequency-reconfigurable LNA is shown in the schematic of Fig. 6.6. As it was mentioned before, the IMN is composed by a multimodal TLM structure. The capacitances of the decoupling capacitors C_1 and C_2 are the same as that used in the third design of Chapter 5 (Fig. 5.30). The ISMN follows a similar reconfigurability principle of previous designs, as it was described above. L_5, L_6, C_9 and C_{11} remain the same as previous designs. The OMN remains without any change from the designs presented in Chapter 5.

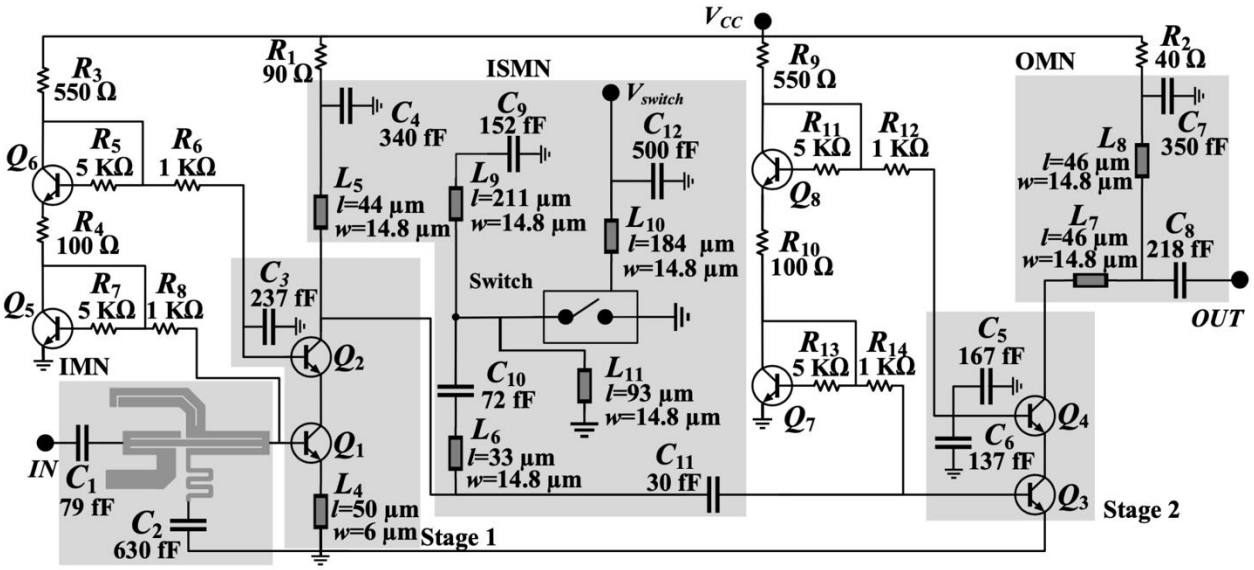


Fig. 6.6. Schematic of the proposed 120 to 140 GHz frequency-reconfigurable LNA including an HBT-RF switch.

All the lines on the ISMN (L_5, L_6, L_9, L_{10} and L_{11}) and OMN (L_7 and L_8), as well as line L_4 are microstrip lines. L_5, L_6, L_7, L_{10}, L_{11} and the multimodal TLM structure of the IMN are designed with the TM2 layer of the IHP's SG13G2 technology, while L_9 is designed using the TM1 layer and L_4 using a stack of three metallic layers (M2, M3 and M4).

The amplifier is biased with a V_{CC} = 2.5 V and I_{CC} = 15 mA using current mirrors (Q_5 Q_6, Q_7 and Q_8) and bias resistors (R_1 and R_2). The transistors used in both stages and bias network are the same size of those used for the designs of Chapter 5. The Stage 1 of LNA (Fig. 5.7.) is composed by transistors Q_1 and Q_2 (5 and 10 emitter fingers respectively) and is biased with a collector current of 4.6 mA. The Stage 2 is composed by transistors Q_3 and Q_4 (10 emitter fingers each) and is biased with a collector current of 8 mA. The HBT-RF switch consume a DC current of 15 mA for the "ON" state.

6.2.2. Fabrication and experimental characterization of the frequency-reconfigurable LNA

The frequency-reconfigurable LNA was fabricated using the IHP's 0.13-μm SG13G2 SiGe:C BiCMOS technology described in Chapter 2. A picture of the LNA is shown in Fig. 6.7. The chip area is 515 µm × 382 µm and the core area is 331 µm × 274 µm.

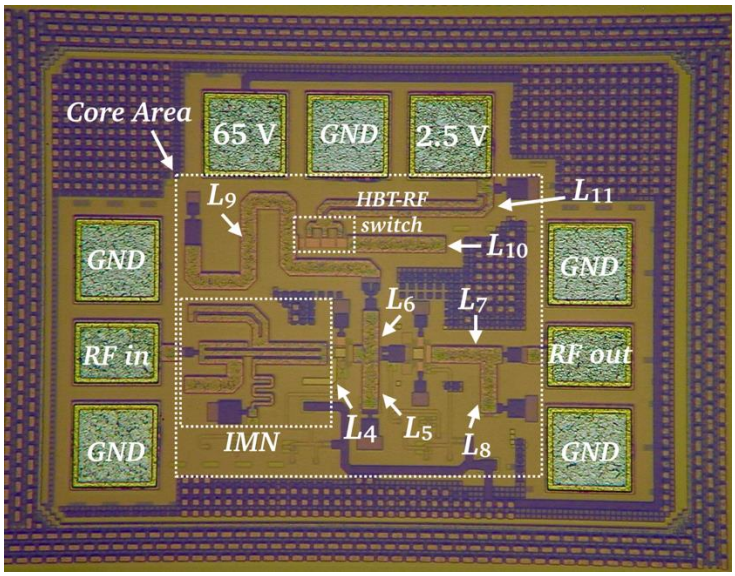


Fig. 6.7. Picture of the fabricated frequency-reconfigurable LNA including an HBT-RF switch.

The LNA implemented with an HBT-RF switch as reconfigurable device accomplish a chip area and core area reduction of 23.5% and 15% respectively, compared with the most compact LNA design implemented with RF-MEMS switch (Section 5.5).

In the same way as it was done for the designs in Chapter 5, circuit/electromagnetic co-simulations were performed using Keysight ADS and Momentum. The multimodal TLM structure of the IMN, microstrip and bias lines, as well as capacitors were simulated using electromagnetic simulation and a co-simulation element was created. The IHP's design kit models for transistors and resistors were connected to the co-simulation element on an ADS schematic in order to perform a two-port simulation. The S-Parameters and F were obtained from the simulations for a 110 to 170 GHz frequency range. A voltage of 0 or 1 V can be applied to adjust the HBT-RF switch to "OFF" or "ON" state in order to perform the simulations for the lower- and upper-frequency states respectively.

The S-Parameter measurements were performed at the IHP facilities. A bias voltage of 2.5 V and an input power signal of -20 dBm was applied to the LNA to obtain the lower-frequency state S-Parameters. After that, a bias voltage of 1 V was applied to the HBT-RF switch to obtain the upper-frequency state S-Parameters. The simulated S-Parameters are compared to the measured results for the lower- and upper-frequency states in Fig. 6.8 and Fig. 6.9 respectively.

The LNA features a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 14.2, –6.6, –46 and –8.1 dB respectively for the lower-frequency state. Concerning the upper-frequency state, a measured $|S_{21}|$, $|S_{11}|$, $|S_{12}|$ and $|S_{22}|$ of 14.2, –14, –37.9 and –2.5 dB respectively were obtained.

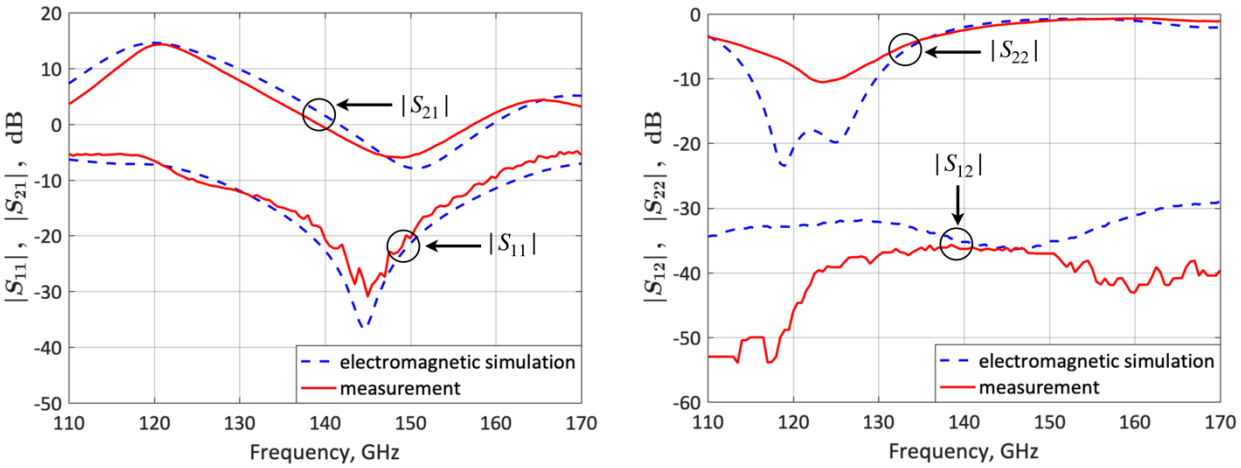


Fig. 6.8. Measured and simulated LNA S-Parameters for the lower-frequency state (120 GHz) for the LNA design including an HBT-RF switch.

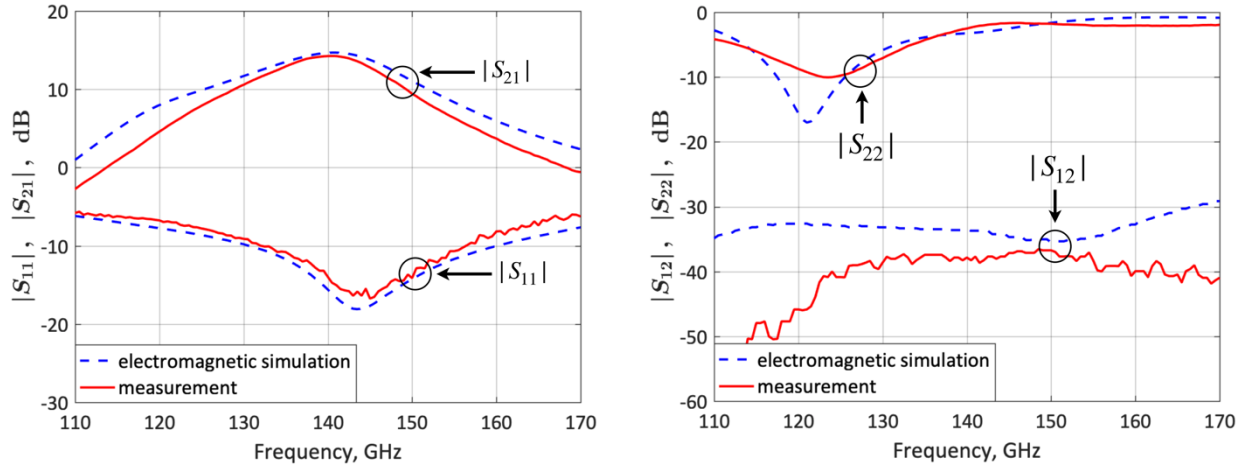


Fig. 6.9. Measured and simulated LNA S-Parameters for the upper-frequency state (140 GHz) for the LNA design including an HBT-RF switch.

The F measurements were performed in the VTT-Millilab facilities using the Y-factor method described in subsection 5.3.4. The simulated F is compared to the measured results for the lower- and upper-frequency states in Fig. 6.10. The measured F is 8.2 dB for both lower- and upper-frequency states. The S-Parameters and F measurements are in good agreement with the obtained simulations thus validating the frequency-reconfigurable LNA concept.

The stability of the LNA is obtained using the μ and μ' factors. According to the simulations results performed in the DC to 170 GHz frequency band, the LNA is unconditionally stable for all the frequencies (μ > 1 and μ' > 1) for both lower- and upper-frequency states. The minimal simulated μ and μ' are μ=1/μ'=1 for both lower- and upper-frequency states.

The μ and μ' stability factors were also obtained from the measured results demonstrating that the LNA is unconditionally stable in all the 110 to 170 GHz

frequency band ($\mu > 1$ and $\mu' > 1$) for both lower- and upper-frequency states. The minimal calculated μ and μ' obtained from the measurements are μ=1.07/μ'=1.82 for the lower- frequency state and μ=1.02/μ'=1.45 for the upper-frequency states.

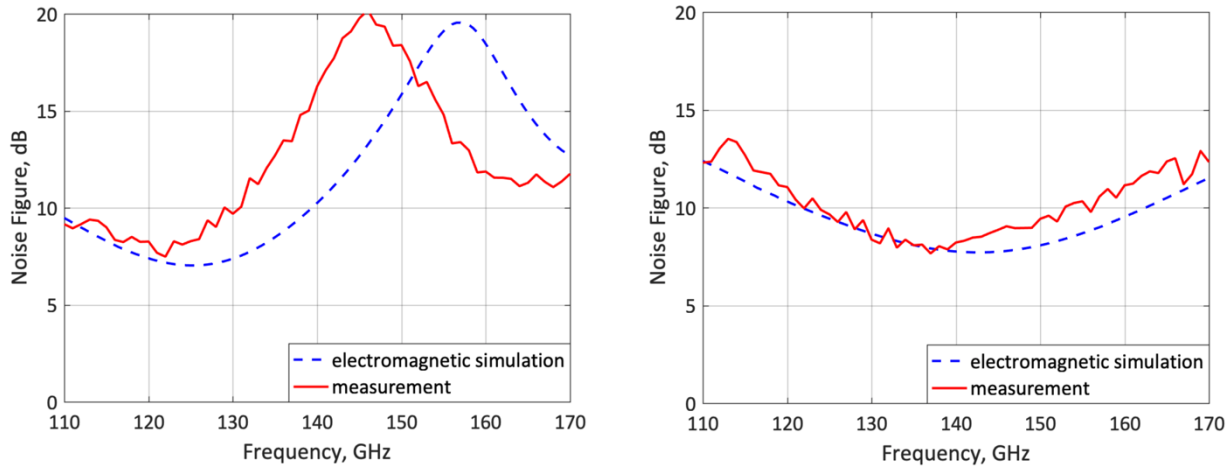


Fig. 6.10. Measured and simulated *F* for the lower- (125 GHz; left) and upper-frequency state (143 GH; right) for the LNA design including an HBT-RF switch.

Table 6.1. Comparison of the measured performance of the four LNA designs presented in this Thesis.

	RF-MEMS switch			HBT-RF switch
	Coupled microstrip line IMN (125 GHz/140 GHz)	Standard microstrip line IMN (125 GHz/140 GHz)	Coupled microstrip line IMN (125 GHz/143 GHz)	Coupled microstrip line IMN (120 GHz/140 GHz)
$\lvert S_{21} \rvert$ (dB)	18.4/16.8	16.9/16	18.2/16.1	14.2/14.2
$\lvert S_{11} \rvert$ (dB)	−9.2/−10.5	−9/−11.1	−9.7/−12.2	−6.6/−14
$\lvert S_{12} \rvert$ (dB)	−42.5/−47.5	−42/−43	−40.1/−45	−46/−37.9
$\lvert S_{22} \rvert$ (dB)	−6.5/−1.4	−7.5/−1.7	−5.6/−2.1	−8.1/−2.5
F (dB)	7.3/7.9	7.3/7.9	7/7.7	8.2/8.2
Power consumption (mW)	37.5	37.5	37.5	37.5/51.5
Input P1dB (dBm)	−17.8/−15.2	−16/−11.2	−17.3/−15.9	−12.4/−13.6
Chip area (mm^2)	0.38	0.408	0.257	0.19
Core area (mm^2)	0.151	0.171	0.106	0.09

The Input P1dB obtained from simulations is –12.4 dBm for the lower-frequency state and –13.6 dBm for the upper-frequency state.

The performance of the LNA design implementing an HBT-RF switch as reconfigurable device is compared to the previous designs in Table 6.1.

6.3. Conclusions

In this Chapter, a frequency-reconfigurable LNA using an HBT-RF switch has been designed, simulated and fabricated with the IHP's 0.13 μm SG13G2 SiGe:C BiCMOS technology. The design is very similar to those proposed in Chapter 5 with exception of the HBT-RF switch implemented in the ISMN which selects the operation frequency (120 or 140 GHz). The achieved gain and F are 14.2 dB and 8.2 dB respectively, for both lower- and upper-frequency states. The systematic design method described in Chapter 5 is also used in this case.

The use of an HBT-RF switch in the LNA design allows a 15% core area reduction when compared to the LNA implemented with a RF-MEMS switch as reconfigurable device. Even if the performance for the LNA proposed in this Chapter is not as good as the LNAs implemented with a RF-MEMS switch, it can be used when the compactness is a priority.

CHAPTER SEVEN

CONCLUSIONS

In this Chapter, the conclusions of this Thesis are discussed. Also, all the results obtained are summarized and future research lines that arise from these studies are discussed.

7.1. Main conclusions

The necessity for multiband systems that can work for different applications is increasing. Also, the growth of required information, data rate and bandwidth, calls for the need of increasing the operation frequency at which these systems need to operate. Hence, the work presented in this Thesis focused in the design of reconfigurable LNAs for applications above 100 GHz. Since compactness has been always a desirable characteristic in circuit design, multimodal compact structures were also studied for its implementation as compact matching networks and impedance tuners.

Multimodal coupled microstrip line and TLM structures were studied and their circuit models were obtained. Three frequency-reconfigurable LNAs using a single RF-MEMS switch as reconfigurable device were designed, simulated, fabricated and characterized. Two of the designs implement the studied multimodal structures in order to reduce the overall size of the circuits. A fourth LNA using an HBT-based switch was also designed, simulated, fabricated and characterized.

7.1.1. Multimodal Circuits

Multimodal coupled microstrip line and TLM structures were studied. The asymmetries and transitions in the structures cause interaction between the fundamental models; multimodal models were presented in detail. In Section 3.2 the models of the multimodal coupled microstrip line structure were discussed and in Section 3.3 the models for multimodal TLM structures were presented. Some TLM structures were fabricated and characterized in order to validate the studied multimodal models.

The TLM structure shown in Fig. 3.32 was studied in detail to corroborate its Smith-chart impedance coverage capabilities. Since this structure demonstrated compactness and good performance, it was implemented as a multimodal impedance tuner and for the design of a compact matching network.

These multimodal circuits bring the solution for the development of more-compact design, and since they consist of microstrip structures, they can be implemented in an easy way in a large variety of circuits.

7.1.2. Multimodal impedance tuner

A multimodal impedance tuner was designed, simulated, fabricated and characterized at 2 GHz, using the multimodal TLM structure developed in Chapter 3 (Fig. 3.32). A multimodal model of the impedance tuner was obtained in order to simulate its behavior. The implementation of a multimodal model results in an easier and less-time consuming way to design the impedance tuner compared to an electromagnetic simulation tool. The impedance tuner simulations were compared to

the measurement results demonstrating a good performance for the 1.4 to 3.2 GHz frequency band. The impedance tuner features a Smith-chart impedance coverage above 70% for the 1.4 to 3.2 GHz frequency band (73.2% for the designed frequency 2 GHz), a good fractional bandwidth of 85% and a voltage standing-wave ratio featuring complete coverage ($VSWR_{CC}$) > 6.2 for the 2 to 3.2 GHz frequency band. The total size of the impedance tuner is 17.45 × 16 mm (11.45 × 6.55 mm excluding the bias circuit and the SMA connector microstrip line).

The presented impedance tuner offers a very wide Smith-chart impedance coverage with a good fractional bandwidth in a small area. This demonstrates that complex multimodal structures can be easily implemented for the design of compact devices.

7.1.3. Reconfigurable BiCMOS LNA using a RF-MEMS switch

Three different frequency-reconfigurable LNAs were designed, simulated, fabricated and characterized using the IHP's 0.13 μm SiGe:C BiCMOS technology. Also, a systematic method for the design of frequency-reconfigurable LNAs is presented. This method could also be used for other amplifiers that require two stages even if they are not reconfigurable. The design of the matching networks focused on achieving a balanced high gain while maintaining a low-noise figure at two operation frequencies. With the exception of the IMN, the OMN and ISMN are very similar for the three LNA designs.

The first design includes a multimodal coupled microstrip line stub in the IMN which reduce the overall size of the LNA. Concerning the second design, it includes a standard line-stub-line IMN. With respect to the third design, it implements a multimodal TLM structure in the IMN which reduce the overall size of the LNA even further than the first design.

The LNAs were designed using a two-stage cascode topology and a RF-MEMS switch was implemented in the ISMN which selects between two operation frequencies. If the actuation voltage of the RF-MEMS is set to 0 V, the lower-frequency state is selected which is 125 GHz for the three designs. If the actuation voltage of the RF-MEMS is set to 65 V, the upper-frequency state is selected which is 140 GHz for the first and second designs and 143 GHz for the third design.

The three LNA designs are biased with a V_{CC} = 2.5 V using current mirrors and bias resistors. They were fabricated using the IHP's 0.13 μm SiGe:C BiCMOS technology. The core areas achieved for each LNA are 0.151 mm^2, 0.171 mm^2 and 0.106 mm^2 for the first, second and third designs respectively. All three LNAs have a gain higher than 16 dB and a F below 7.9 dB for both lower- and upper-frequency states. The good agreement of the simulated and measured S-Parameters and F validate the proposed designs. To the best knowledge of the author this is the first reported frequency-reconfigurable LNA at D-band.

7.1.4. Reconfigurable LNA using an HBT based RF switch

A 120/140 GHz frequency-reconfigurable LNA using an HBT-RF switch was designed, simulated, fabricated and characterized using the IHP's 0.13 μm SiGe:C BiCMOS technology. The LNA design is very similar to the other three LNAs discussed above. Since the RF-MEMS is the largest device in the designed LNAs, it is replaced with an HBT-RF switch which reduces the area of the overall circuit. Even if this LNA does not have a performance as good as the other designs, it achieves the smallest core area (0.09 mm^2) of all the LNAs presented in this Thesis. This LNA design could be used when compactness is an essential characteristic. The achieved gain and F are 14.2 and 8.2 dB respectively, for both lower- and upper-frequency states. The good agreement of the simulated and measured S-Parameters and F validates the proposed design.

The HBT-RF and RF-MEMS switch based LNAs presented in this thesis meet the necessary performance and compactness to offer a competitive solution for future applications that requires more than one operation frequency in a single system at D-band. Moreover, the systematic method for the design of reconfigurable LNAs can be used for D-band amplifiers implemented with other technologies.

7.2. Future research lines

The developed work accomplished with this Thesis paves the way for future research lines:

- Expanding the study of other multimodal coupled-line microstrip and TLM structures with different asymmetries and transitions, can lead to the development of more-compact impedance tuners and matching networks.

- Performing a detailed study of the losses of the TLM structure presented in this Thesis and proposing other multimodal coupled line microstrip and TLM structures, could lead to an impedance tuner with a wider Smith-chart impedance coverage. Also, by reducing losses the implementation of general multimodal structures as reconfigurable matching networks could be possible.

- An extended study and more simulations of the impedance tuner presented in this Thesis using other substrates and varactors, can improve the Smith-chart impedance coverage.

- A study of the cascode configuration can be done for higher frequencies in order to know its limitations and increase the operation frequencies of the LNAs.

- The implementation of the systematic methodology presented in this Thesis using other technologies can be done in order to extend its validation.

- More stages could be used in order to increase the gain of the frequency-reconfigurable LNAs presented in this Thesis. Since more than one ISMN would be used in this case, new design methodologies and new ways of implementing the reconfigurable devices (RF-MEMS and HBT-RF switches) could be developed.

- Expanding the study of parasitic inductances and capacitances associated to via holes could be useful to develop more realistic transmission lines models for more accurate simulations.

- The implementation of techniques like double-parallel stages [53] can increase the power handling of the frequency-reconfigurable LNA presented in this Thesis.

- Other HBT-RF switch configurations could be studied in order to increase the performance of the HBT-RF switch frequency-reconfigurable LNA.

- Since frequency-reconfigurable LNAs at D-band have been demonstrated in this Thesis, the door is open for other reconfigurable active circuits like VCOs.

APPENDIX A

IMPEDANCE TUNER SIMULATIONS AND CHARACTERIZATION

A.1 Simulation details of the multimodal impedance tuner

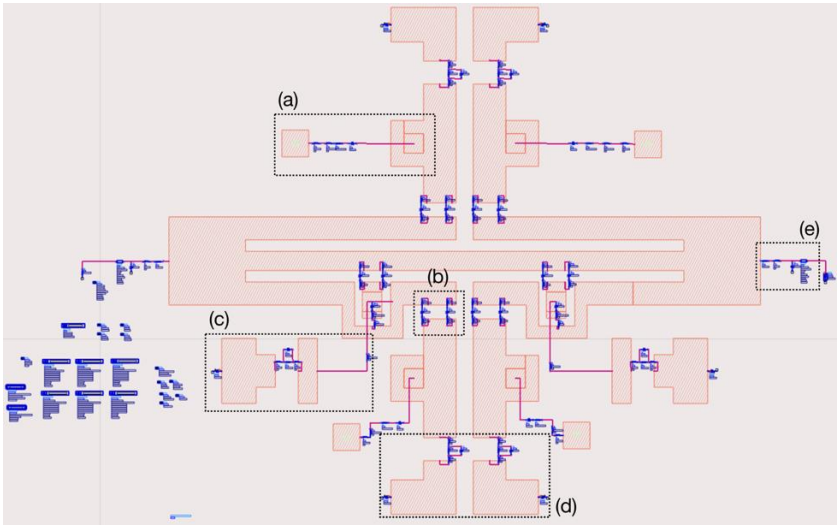


Fig. A.1. ADS schematic of the impedance tuner: (a) ground capacitor, (b) two parallel-connected varactors, (c) bias resistor for the isle varactors, (d) bias resistor for the outer-strip varactors and (e) SMA coaxial connector.

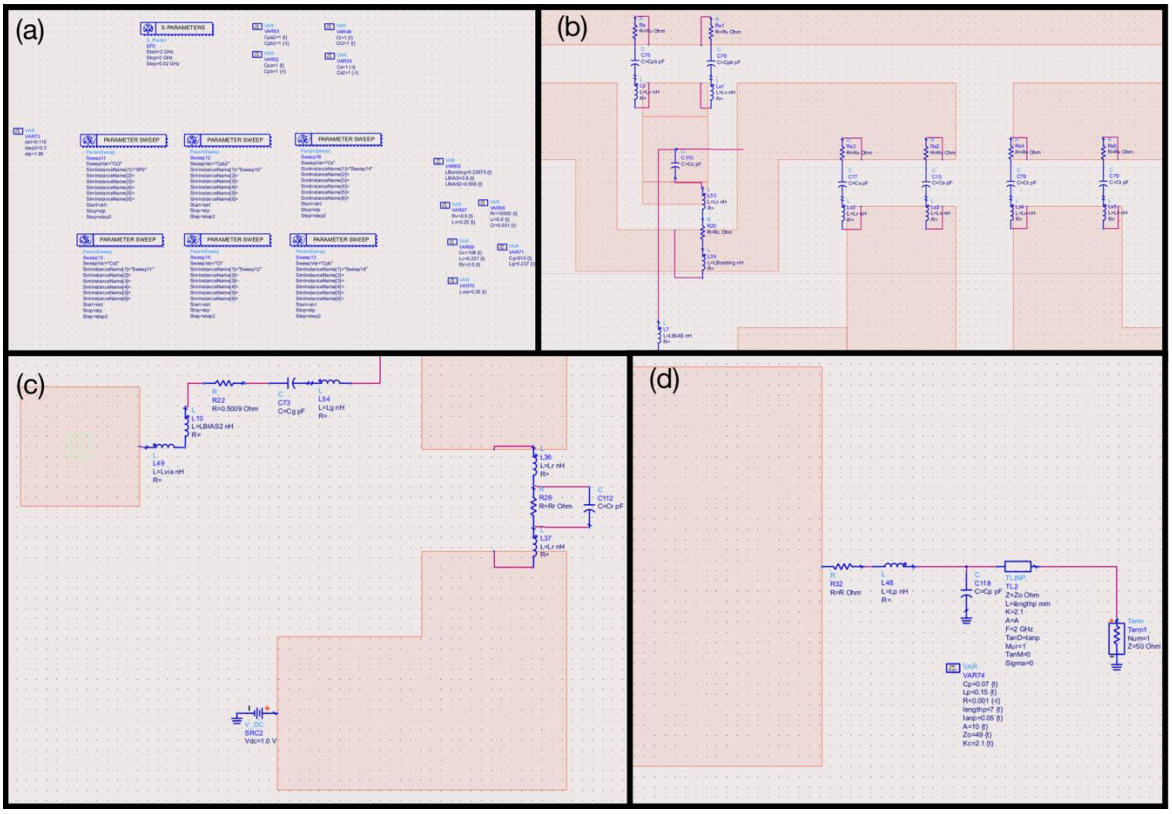


Fig. A.2. Details of the ADS schematic of the impedance tuner: (a) simulation definitions; (b) isle varactors, 108 pF parallel-plate capacitor and outer-strip varactors; (c) ground capacitor and bias resistor for the outer-strip varactors and (d) SMA coaxial connector.

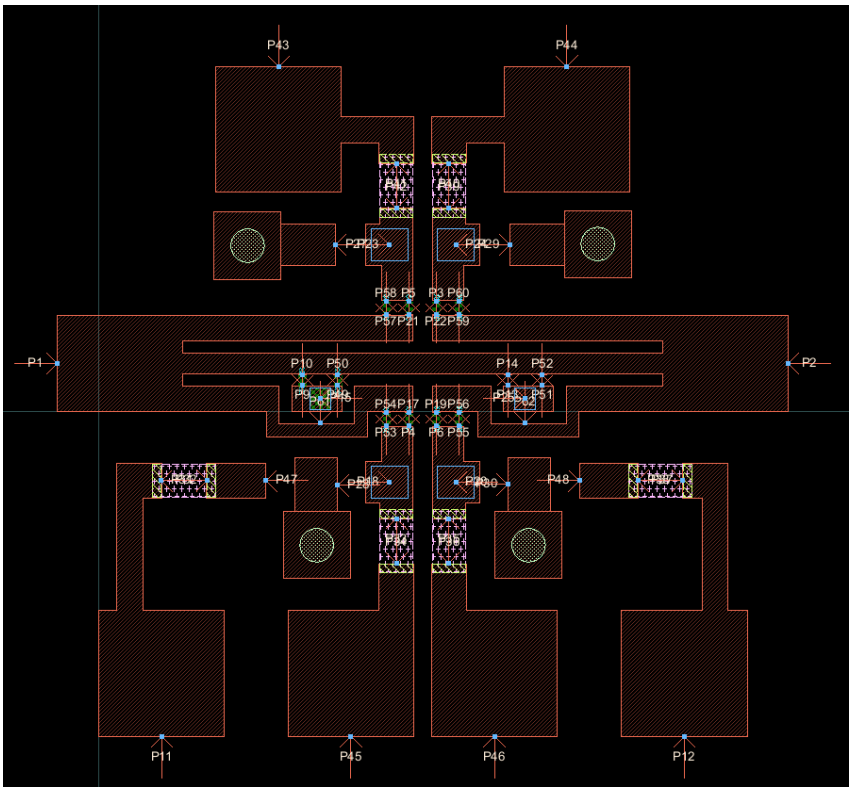


Fig. A.3. Momentum layout for the electromagnetic simulation of the impedance tuner.

A.2 MATLAB routine for the management of the number of simulated states of the multimodal impedance tuner

A graphical user interface (GUI) application software was developed in MATLAB to reduce the number of reflection coefficients S_{11} obtained from measurements/simulations of the impedance tuner. The obtained reflection coefficients are evenly distributed on the Smith chart which results in a better view of the total coverage. The GUI application is also capable of selecting reflection coefficients from specific zones of the Smith chart. The application is shown in Fig. A.4 and each function is described below.

Fig. A.4. GUI software application used to process the simulated/measured reflection coefficients.

The data to be processed has to be contained in a *.xlsx* file that can be loaded using the "Load" button. The application has three functions: "xlsx to mdf file", "Zone" and "Quadrant". The user can select each function by activating the correspondent checkbox. Each function generates a *.mdf* file that contains the processed reflection coefficients. The "xlsxl to mdf file" function does not modify the data, only a *.mdf* file is obtained. The "Quadrant" function selects the data for only a quarter of the Smith chart, and the "Zone" function select it for a delimited area of the Smith chart defined by the user. After selecting one of the above functions, the user can activate the "Coefficient reflection" field to obtain a reduced number of reflection coefficients evenly distributed on the Smith chart. If the number on the "Tolerance" field is bigger, a lower number of reflection coefficients is obtained.

a) "xlsx to mdf file" function

This function generates a *.mdf* file using a *.xlsx* file, and if the "Coefficient reflection" function is active, a smaller number of evenly distributed reflection coefficients will be obtained. Fig. A.5 compares the simulated results of the input reflection coefficient using ADS (left) with those processed by the GUI application.

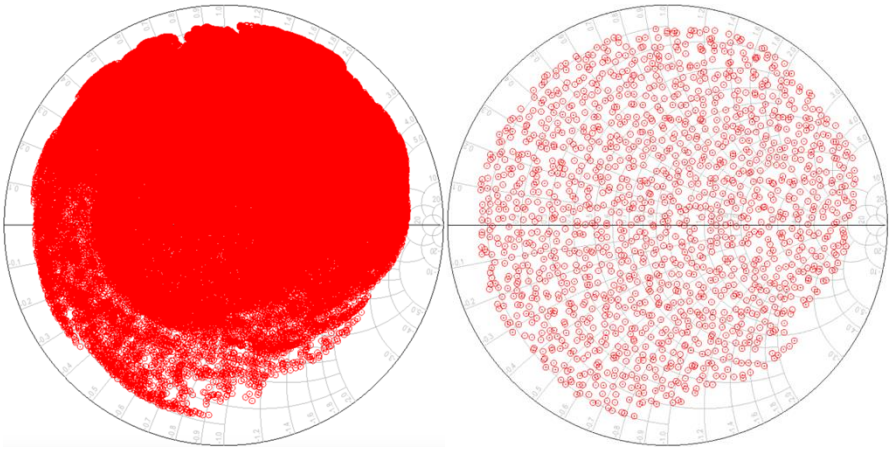


Fig. A.5. Original simulated reflection coefficients (left) and processed reflection coefficients at 2 GHz (right).

b) "Zone" function

This function selects only a portion of the simulated reflection coefficients (Fig. A.6) and write them in a *.mdf* file. The selected portion is delimited by two angles and a magnitude on the Smith chart. The user can specify two angles writing on the field "Angle" and a magnitude on the field "Minimum Magnitude".

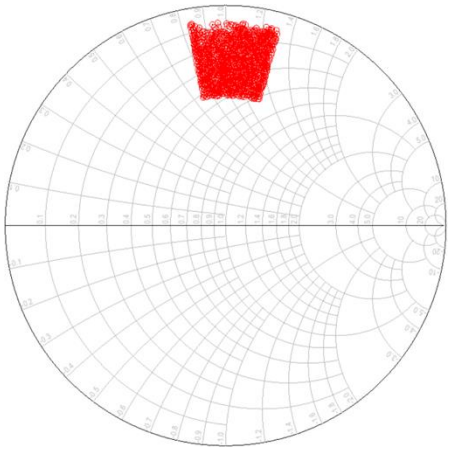


Fig. A.6. Selected portion of the simulated reflection coefficients at 2 GHz.

c) "Quadrant" function

This function selects only a quarter of the simulated reflection coefficients on the Smith chart (Fig. A.7) and write them in a *.mdf* file. The Smith chart quarter is selected by writing a number from 1 to 4 on the field "Quadrant":

- Number 1: reflection coefficients with an angle of 0 to 90˚ are selected.
- Number 2: reflection coefficients with an angle of 90 to 180˚ are selected.

- Number 3: reflection coefficients with an angle of -180 to -90˚ are selected.
- Number 4: reflection coefficients with an angle of -90 to 0˚ are selected.

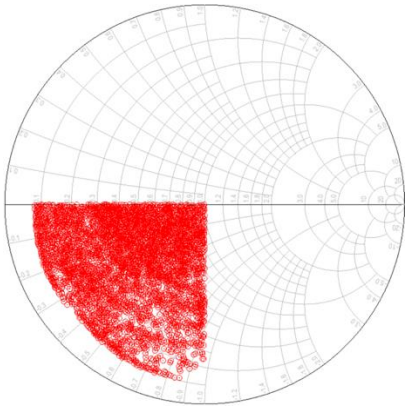


Fig. A.7. Simulated impedance tuner reflection coefficients at 2 GHz selected from the quadrant number 3.

A.3 MATLAB routine for the characterization of the multimodal impedance tuner

A graphical user interface (GUI) application software was developed in MATLAB to automatize the S-Parameters measurement of the impedance tuner (Fig. A.8). The application communicates with two power supplies (Agilent N6700B and HP 6629A) and an Agilent N5245A network analyzer using a GPI interface. The power supplies are used to bias the six varactors and the network analyzer is used to obtain the S-Parameters.

The application communicates with power supplies Agilent N6700B and HP 6629A (used to bias the varactors); and with an Agilent N5245A network analyzer (used to obtain the S-Parameters) using a GPI interface.

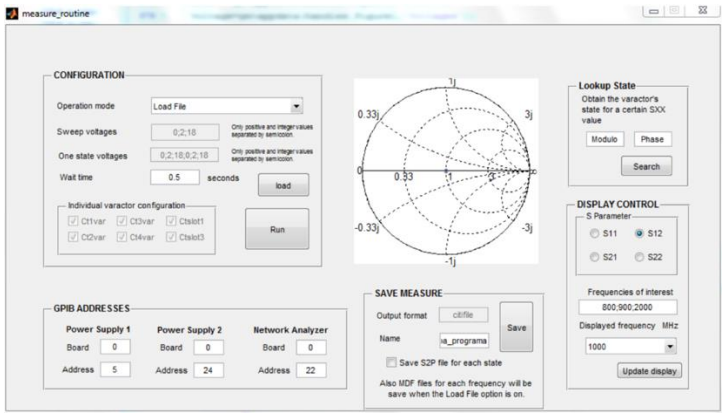


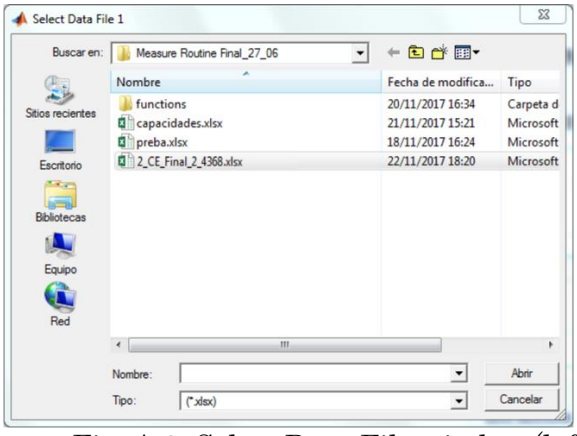
Fig. A.8. GUI software application used for the measurement of the tuner.

The measurement steps are described as follows:

1. In the "Operation mode" popup menu, "Load File" is selected.

2. The "load" button is clicked and the "Select Data File" dialog box appears (Fig. A.8).

3. A "*.xlsx*" file is selected from the dialog box and then "Open" is clicked. The file contains the capacitance values of each varactor for each state to be measured (Fig. A.9).



	scalar	scalar	scalar	scala
1	Type : Real	Type : Real	Type : Real	Type
2	1	2.000 GHz	0,11	
3	2	2.000 GHz	0,11	
4	3	2.000 GHz	0,11	
5	4	2.000 GHz	0,11	
6	5	2.000 GHz	0,11	
7	6	2.000 GHz	0,11	
8	7	2.000 GHz	0,11	
9	8	2.000 GHz	0,11	
10	9	2.000 GHz	0,11	
11	10	2.000 GHz	0,11	
12	11	2.000 GHz	0,11	
13	12	2.000 GHz	0,11	
14	13	2.000 GHz	0,11	

Fig. A.9. Select Data File window (left) and "*.xlsx*" file in detail (right).

1. The "Wait Time" is set to 0.5 seconds. This is the time the network analyzer will wait before make the next measurement. The "GPIB ADRESSES" fields contain the GPIB addresses used for establish communication between the GUI application and the power supplies and network analyzer.

2. The "Run" button is clicked and the measurement initiates.

3. The "Save" button is clicked and the measurement is saved for the frequencies shown in the field "Frequencies of interest" (Fig. A.8).

4. The software generates a "*.mdf*" file for each frequency specified in the field "Frequencies of interest".

APPENDIX B

IMPEDANCE TUNER LUMPED ELEMENTS DATA SHEETS

B.1 MA46580 varactor data sheet

MA46580 & MA46585

Beam Lead Constant Gamma GaAs Tuning Varactor

Rev. V4

Features

- Constant Gamma = 1.0 & 1.25 available
- High Q (3000 minimum at 4V 50MHz)
- Strong Beam Construction (Minimum 10 gram beam strength)
- Low Parasitic Capacitance
- Close Capacitance tracking
- Lead-Free (RoHs Compliant) equivalents available with 260°C reflow compatibility

Description

The MA46580 & MA46585 series beam lead constant gamma tuning varactors are hyper-abrupt junction gallium arsenide diodes with a constant gamma of 1.0 or 1.25. The high Q values and the elimination of package parasitics make these varactors very attractive for voltage controlled oscillators that require linear tuning. These tuning diodes are useful at frequencies as high as 40 Ghz.

The beam lead design eliminates almost all of the package parasitics resulting in improved linearity of the junction capacitance change with applied reverse bias voltage. This improves tracking between diodes and can improve VCO linearity.

Absolute Maximum Ratings @ T_A=+25 °C

(Unless Otherwise Noted) [1]

Parameter	Absolute Maximum
Reverse Voltage	18V
Operating Temperature	-65°C to +150°C
Storage Temperature	-65°C to +200°C
Power Dissipation	25mW at 25 °C
Beam Strength	10 grams minimum

1. Operation of this device above any one of these parameters may cause permanent damage.

Applications

These beam lead constant gamma tuning varactors are particularly useful in broadband VCO's, where linear frequency tuning is an important feature. They are also very useful for FM modulating a source for telecommunication transmitter and in many cases such circuits can be designed without a linearization circuit.

Electrical Specifications @ T_A = +25 °C

Gamma = 1.0[2]

Gamma4 = 0.9 - 1.1, VR = 2 - 12 Volts
Breakdown Voltage @ I_R = 10µA, V_b = 18 V Min
Reverse Leakage Current @ V_R =14V, I_R = 50 nA Max

Part Number	Case Style	Total Capacitance[1] +/-20%	Total Capacitance Ratio	Q Minimum
		Vr=4V	Vr=2V / Vr=12V	Vr=4V f=50MHz
		(pF)	-	-
MA46585-1209	1209	0.5	3.2-5.2	3000

Electrical Specifications @ T_A = +25 °C

Gamma = 1.25[2]

Gamma4 = 1.13-1.38, VR = 2 - 12 Volts
Breakdown Voltage @ I_R = 10µA, V_b = 18 V Min
Reverse Leakage Current @ V_R =14V, I_R = 50 nA Max

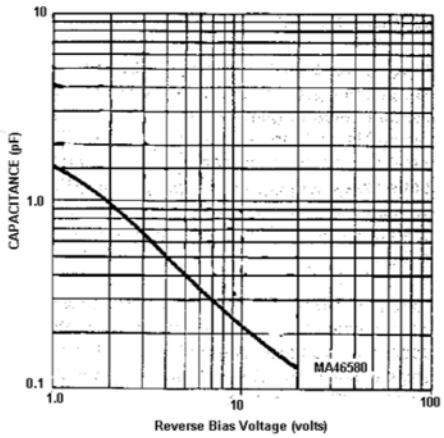
Part Number	Case Style	Total Capacitance[1] +/-20%	Total Capacitance Ratio	Q Minimum
		Vr=4V	Vr=2V / Vr=12V	Vr=4V f=50MHz
		(pF)	-	-
MA46580-1209	1209	0.5	4.5-6.5	3000

Notes:
1. Capacitance is measured at 1 MHz.
2. All junctions are hyperabrupt with nominal Γ= 1.0 or 1.25
3. Reverse voltage (VB) is measured at 10 microamps.

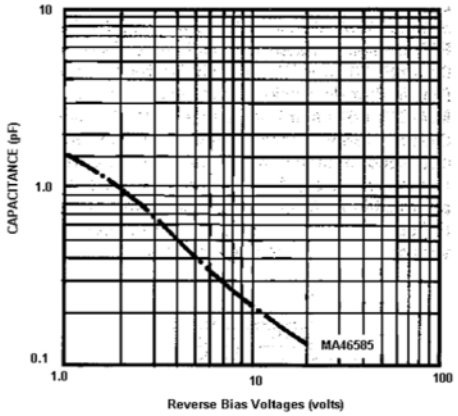
• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298
Visit www.macomtech.com for additional data sheets and product information.

Typical Performance Curves @ 25°C

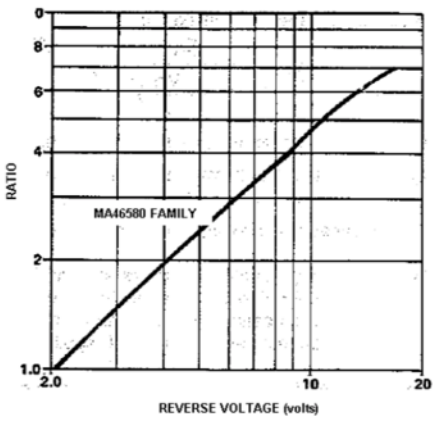
Capacitance vs. Voltage



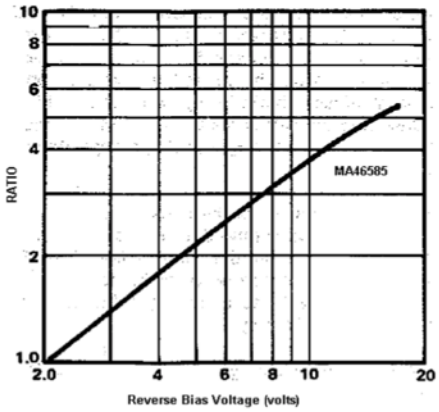
Capacitance vs. Voltage



Capacitance Ratio CT2V/CTV



Capacitance Ratio CT2V/CTV



- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macomtech.com for additional data sheets and product information.

MA46580 & MA46585

Beam Lead Constant Gamma GaAs Tuning Varactor

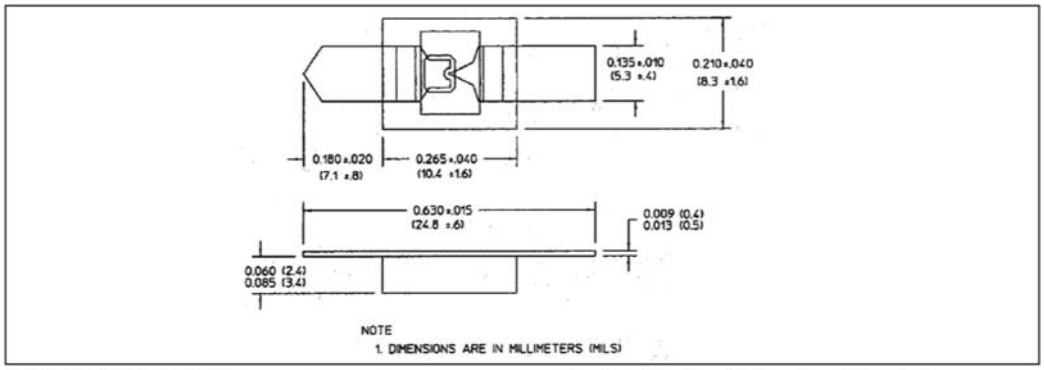
Rev. V4

Environmental Ratings PER MIL-STD-750

	Method	Level
Storage Temperature	1031	See maximum ratings
Temperature Cycle	1051	10 cycles, -65°C to +175°C
Shock	2016	500 g's
Vibration	2056	15 g's
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days
Constant Acceleration	2006	20,000 g's
Humidity	1021	10 days

Case Styles

ODS-1209



BONDING BEAM LEAD DIODES

The preferred methods for bonding a beam lead diode are thermal compression bonding and parallel gap welding. For thermal compression bonding, the beam lead diode is placed down (gold beam to gold plated substrate) with the leads resting flat on the pad and the bond is made by using a heated wedge. Heat and pressure form a metallurgical bond. A minimum of 100 microinches of gold on the substrate is recommended for optimum bonding.

In the parallel gap technique, current is first passed through the substrate metallization, then through the device lead. Most of the heat is generated at the interface. Care must be taken to see that the step welder does not discharge through the diode junction or the diode will be destroyed. The bonding pressure should be approximately 900 gms/mm².

The major advantage of the parallel gap technique is that a cold ambient may be used. Heat is only generated in the vicinity of the bond itself. Caution must be taken when making the second bond because if the diode is placed in tension, the lead may break.

The following precautions will ensure better results when bonding beam leads:

To minimize the lead inductance, the wedge, or heated tips should be placed as close as possible to the edge of the chip without touching it. The chip is very easily damaged, and care must be taken that the bonding tip does not contact the chip at any time during the bonding process.

The bonding tip must be perpendicular to the beam during bonding, to prevent a torsional force which will pull the beams apart. This is particularly important when bonding the second lead.

BONDING TO SOFT CIRCUITS

Beam lead diode can be soft soldered, epoxied or parallel gap welded to Teflon fiberglass or soft circuit boards if low bond pressure is used. Bonding pressure must be reduced to a minimum to prevent diode breakage by forcing the beam into the board.

In general, soft soldering or reflow soldering is the preferable technique. The circuit board should be pretinned with solder or a solder plating to obtain the best wetting. Solder melting temperatures of 225-300°C are most satisfactory. Usually, the circuit board manufacturer's solder recommendations should be followed.

Conductive solder paste such as high conducting silver filled epoxy will also result in good low loss bonds. Care should be taken to ensure that the wet paste does not run up the beam lead and short it.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
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- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macomtech.com for additional data sheets and product information.

B.2 D20BV101K1PX capacitor data sheet

DiCap®

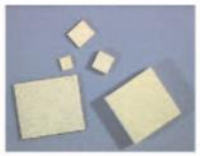
High Performance Single-Layer Capacitors for

Functional Applications:

- DC Blocking
- RF Bypass
- Filtering
- Tuning
- Submounts

Benefits:

- Gold Metallization for wire bonding
- Rugged Construction
- Custom sizes at commercial prices
- Thin Film Technology
- ESD Proof



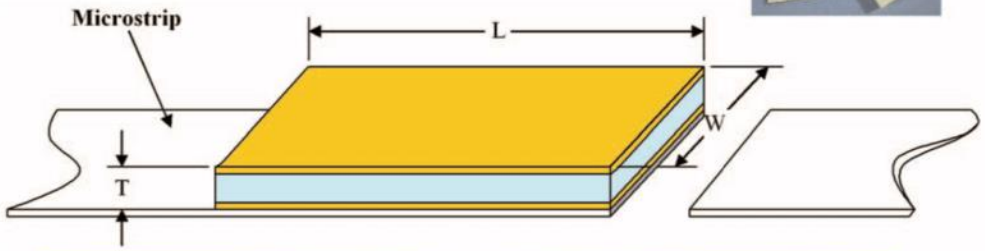


Table of Standard Values (pF)

0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09	0.1
0.15	0.2	0.25	0.3	0.35	0.4	0.45	0.5	0.55
0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95	1
1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9
2	2.2	2.4	2.7	3	3.3	3.6	3.9	4.3
4.7	5.1	5.6	6.2	6.8	7.5	8.2	9.1	10
11	12	13	15	16	18	20	22	24
27	30	33	36	39	43	47	51	56
62	68	75	82	91	100	110	120	130
150	160	180	200	220	240	270	300	330
360	390	430	470	510	560	620	680	750
820	910	1000	110	1200	1300	1500	1600	1800
2000	220	2400	2700	3000	3300	3600	3900	4300
5300	6500	10,000						

DiCap® Dimensions

Style	W Width		L Length (Maximum)		T Thickness (50 Volts)		T Thickness (100 Volts)		Standard Capacitance Range
	Inches	mm	Inches	mm	Inches	mm	Inches	mm	pF
D10	.010 + .000 - .003	.254 + .000 - .076	.010	.254	.004 ±.001	.102 ±.025	-	-	.02 - 100
D12	.012 + .002 - .003	.305 + .051 - .076	.015	.381	.004 ±.001	.102 ±.025	-	-	.03 – 200
D15	.015 + .000 - .003	.381 + .000 - .076	.020	.508	.004 ±.001	.102 ±.025	.006 ± .001	.152 ± .025	.04 -350
D20	.020 + .000 - .003	.508 + .000 - .076	.020	.508	.004 ±.001	.102 ±.025	.006 ± .001	.152 ± .025	.06 – 470
D25	.025 + .000 - .003	.635 + .000 - .076	.030	.762	.004 ±.001	.102 ±.025	.006 ± .001	.152 ± .025	.10 – 800
D30	.030 + .000 - .003	.762 + .000 - .076	.030	.762	.004 ±.001	.102 ±.025	.006 ± .001	.152 ± .025	.15 – 1000
D35	.035 ± .005	.889 ± .127	.040	1.016	.004 ±.001	.102 ±.025	.007 ± .002	.178 ± .051	.20 – 1500
D50	.050 ± .010	1.270 ± .254	.060	1.524	-	-	.007 ± .002	.178 ± .051	.30 – 3700
D70	.070 ± .010	1.778 ± .254	.080	1.778	-	-	.008 ± .002	.203 ± .051	.55 – 6500
D90	.090 ± .010	2.286 ± .254	.100	2.540	-	-	.010 ± .004	.254 ± .102	.65 – 10,000

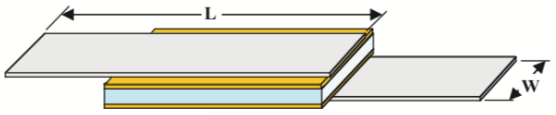
Maximum thickness does not apply for capacitance values below 0.5pF
UX thickness only available in .005", .010" and .015"

Dielectric Laboratories Inc.
2777 Route 20 East
Cazenovia, New York, USA
13035-9433
phone 315.655.8710
fax 315.655.0445
www.dilabs.com
email sales@dilabs.com
or europesales@dilabs.com
or asiasales@dilabs.com

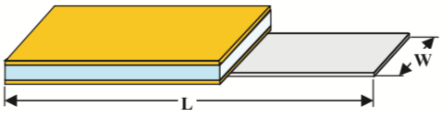
Leaded DiCap® Dimensions

Style	W Lead Width (Minimum)		W Lead Width (Maximum)		L Lead Length (Minimum)	
	Inches	mm	Inches	mm	Inches	mm
D10	.0035	.0889	.007	.1778	.250	6.350
D12	.0045	.1143	.009	.2286	.250	6.350
D15	.0065	.1651	.013	.3302	.250	6.350
D20	.0085	.2159	.017	.2159	.250	6.350
D25	.011	.2794	.022	.5588	.250	6.350
D30	.0135	.3429	.027	.6858	.250	6.350
D35	.015	.381	.030	.762	.250	6.350
D50	.020	.508	.040	1.016	.250	6.350
D70	.030	.762	.060	1.524	.250	6.350
D90	.040	1.016	.080	2.032	.250	6.350

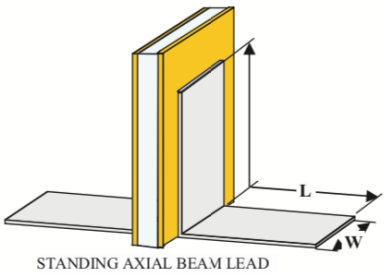
- **See DiCap® Termination Code Table for available lead configurations.**
- **Lead material is 0.002" pure silver, (Ag), 0.002" ± .0005" thick.**
- **Leads are attached with Au Sn, 80%/20% eutectic alloy. Re flow temperature is 280 °C minimum.**
- **Pure Gold, (Au) leads are ava ilable. Consult factory for details.**
- **Chip dimensions per DiCap® Dimensions table.**
- **Custom Lead dimensions are available. Consult factory for details.**



AXIAL BEAM LEAD



SINGLE BEAM LEAD



STANDING AXIAL BEAM LEAD

DiCap® Designer Kits
160 Capacitors, 10 Each of 16 Values

Part Number	Capacitor Width	10 Capacitors of each value								
		Dielectric	pF	Tol.	pF	Tol.	pF	Tol.	pF	Tol.
D10XXKITA5PX	.010"	Class I, see codes on pg. 5	.1 .4	B B	.6 1.0	C C	1.5 2.2	C D	2.7 3.3	D D
		Class II, see codes on pg. 5	3.9 4.7	D D	5.6 6.2	M M	8.2 10	M M	20 33	M M
D15XXKITA5PX D20XXKITA5PX	.015" .020"	Class I, see codes on pg. 5	.1 .4	B B	.6 1.0	C C	1.5 2.2	C C	3.3 5.6	D D
		Class II, see codes on pg. 5	6.8 8.2	K K	10 15	K K	20 33	M M	50 100	M M
D25XXKITA5PX D30XXKITA5PX	.025" .030"	Class I, see codes on pg. 5	.4 .6 1.0	B C C	1.5 2.2 2.7	C C C	3.3 4.7 5.6	D D D	8.2 10 20	K K K
		Class II, see codes on pg. 5	33	M	50	M	100	M	180	M

DLI reserves the right to substitute values as required.
Customer may request specific cap value and material for sample kit.

9

50 Volt SLC

Capacitance Range vs. Case size by Dielectric Material

Style		Class I Dielectric materials														
		LA	PI	PG	AH	CF	NA	CD	NG	CG	DB	NP	NR	NS	NU	NV
D10	Min	0.02	0.03	0.04	0.06	0.07	0.06	0.10	0.15	0.20	0.20	0.25	0.45	0.80	1.6	2.4
	Max	0.02	0.05	0.06	0.10	0.10	0.10	0.15	0.20	0.35	0.35	0.40	0.80	1.5	3.0	4.3
D12	Min	0.03	0.04	0.06	0.08	0.10	0.09	0.15	0.20	0.30	0.30	0.35	0.65	1.2	2.4	3.6
	Max	0.06	0.10	0.10	0.20	0.25	0.20	0.35	0.45	0.75	0.75	0.90	1.7	3.0	6.2	9.1
D15	Min	0.04	0.06	0.08	0.15	0.15	0.15	0.25	0.25	0.45	0.45	0.50	1.0	1.8	3.6	5.6
	Max	0.08	0.15	0.20	0.30	0.35	0.30	0.55	0.65	1.1	1.1	1.3	2.4	4.7	9.1	13
D20	Min	0.06	0.09	0.15	0.20	0.20	0.20	0.35	0.40	0.65	0.65	0.75	1.5	2.7	5.6	8.2
	Max	0.10	0.20	0.25	0.40	0.50	0.45	0.75	0.90	1.4	1.5	1.8	3.3	6.2	12	18
D25	Min	0.10	0.20	0.25	0.35	0.45	0.40	0.65	0.75	1.2	1.3	1.5	2.7	5.1	11	16
	Max	0.20	0.40	0.50	0.80	0.95	0.90	1.5	1.7	2.7	2.7	3.3	6.2	12	24	36
D30	Min	0.15	0.25	0.30	0.45	0.55	0.50	0.85	0.95	1.6	1.6	1.9	3.6	6.8	15	20
	Max	0.25	0.45	0.60	0.95	1.1	1.0	1.8	2.0	3.3	3.3	3.9	7.5	13	27	43
D35	Min	0.20	0.35	0.50	0.70	0.85	0.80	1.3	1.5	2.7	2.7	3.0	5.6	11	22	33
	Max	0.50	0.85	1.1	1.8	2.0	1.9	3.3	3.6	6.2	6.2	7.5	13	27	51	75

Style		Class II Materials											
		BF	BD	BG	BC	BE	BL	BJ	BN	BT	BU	BV	UX*
D10	Min	1.2	1.8	2.4	3.6	3.3	5.6	9.1	12	12	22	36	
	Max	2.2	3.6	4.3	6.2	6.2	10	16	22	22	43	68	100
D12	Min	1.8	3.0	3.6	5.1	5.1	8.2	13	18	18	36	56	
	Max	4.7	7.5	9.1	13	13	20	33	47	47	91	130	200
D15	Min	2.7	4.3	5.6	7.5	7.5	12	20	27	27	51	82	
	Max	6.8	11	13	20	18	30	51	68	68	130	200	350
D20	Min	4.3	6.2	8.2	12	12	18	30	43	43	75	120	200
	Max	9.1	13	18	27	24	39	68	91	91	180	270	470
D25	Min	8	12	16	22	22	36	56	82	82	150	240	270
	Max	18	27	36	51	51	82	130	180	180	330	510	800
D30	Min	10	16	20	30	30	47	75	100	100	200	300	360
	Max	22	33	43	62	62	91	160	220	220	390	620	1000
D35	Min	16	27	33	47	47	75	120	160	160	300	510	560
	Max	39	62	75	110	110	180	270	390	390	750	1200	1500

* UX capacitors are 16 volt rated

Part Number Identification

D	10	CF	0R1	B	5	P	X

Product
D = Single Layer Capacitor (DiCap®)

Case Size
10
12
15
20
25
30
35
50
70
90

Material
See Material Tables on page 5 in the General Section.

Capacitance(pF)
R02 = 0.02 pF
0R5 = 0.5 pF
1R0 = 1.0 pF
5R1 = 5.1 pF
100 = 10 pF
101 = 100 pF
432 = 4300 pF
See Capacitance tables for available values. Consult Factory for custom solutions.

Tolerance
A = ± 0.05pF
B = ± 0.10pF
C = ± 0.25pF
D = ± 0.5pF
F = ± 1%
G = ± 2%
J = ± 5%
K = ± 10%
L = ± 15%
M = ± 20%
Z = + 80% -20%

Voltage
C = 16V
5 = 50V
1 = 100V

Termination
P = Ni / Au
T = Ni / AuSn
M = Au
L = Single Beam Lead
A = Axial Beam Lead
S = Standing Axial Beam Lead

Test Level
Y, X, A, B, C, D and E. SeeTest Level Codes on page 7 in General section.

Dielectric Laboratories Inc.
2777 Route 20 East
Cazenovia, New York, USA
13035-9433
phone 315.655.8710
fax 315.655.0445
www.dilabs.com
email sales@dilabs.com
or europesales@dilabs.com
or asiasales@dilabs.com

100 Volt SLC

Capacitance Range vs. Case Size By Dielectric Material

Style		Class I Dielectric Materials														
		LA	PI	PG	AH	CF	NA	CD	NG	CG	DB	NP	NR	NS	NU	NV
D15	Min	0.03	0.04	0.06	0.08	0.1	0.09	0.15	0.20	0.30	0.30	0.35	0.65	1.2	2.4	3.6
	Max	0.05	0.10	0.10	0.20	0.25	0.20	0.35	0.45	0.70	0.75	0.85	1.6	3.0	6.2	9.1
D20	Min	0.04	0.06	0.08	0.15	0.15	0.15	0.25	0.30	0.45	0.45	0.55	1.0	1.9	3.9	5.6
	Max	0.08	0.10	0.15	0.25	0.30	0.30	0.50	0.60	0.95	1.0	1.2	2.2	3.9	8.2	12
D25	Min	0.07	0.15	0.20	0.25	0.30	0.30	0.45	0.50	0.85	0.85	1.0	1.9	3.6	7.5	11
	Max	0.15	0.25	0.35	0.50	0.65	0.60	1.0	1.1	1.9	1.9	2.2	4.3	8.2	16	24
D30	Min	0.09	0.15	0.20	0.35	0.40	0.35	0.60	0.65	1.1	1.1	1.3	2.7	4.7	9.1	15
	Max	0.15	0.30	0.40	0.65	0.75	0.70	1.2	1.4	2.2	2.2	2.7	5.1	9.1	18	27
D35	Min	0.15	0.20	0.25	0.40	0.45	0.45	0.70	0.80	1.3	1.4	1.6	3.0	5.6	12	18
	Max	0.30	0.55	0.75	1.2	1.4	1.3	2.2	2.4	3.9	4.3	5.1	9.1	18	36	51
D50	Min	0.30	0.50	0.60	0.95	1.1	1.1	1.7	2.0	3.3	3.3	3.9	7.5	15	30	43
	Max	0.75	1.3	1.7	2.7	3.0	3.0	4.7	5.6	9.1	9.1	11	20	39	82	120
D70	Min	0.55	0.95	1.2	1.9	2.4	2.2	3.6	4.3	6.8	6.8	8	15	30	56	91
	Max	1.10	2.0	2.7	3.9	4.7	4.3	7.5	8.2	13	15	16	33	62	120	180
D90	Min	0.65	1.2	1.5	2.4	3.0	2.7	4.3	5.1	8.2	8.2	10	20	36	68	110
	Max	1.80	3.0	3.9	6.2	7.5	6.8	12	13	22	22	27	51	91	180	270

Style		Class II Materials											
		BF	BD	BG	BC	BE	BL	BJ	BN	BT	BU	BV	UX*
D15	Min	1.8	3.0	3.6	5.6	5.1	8.2	13	18	18	36	56	
	Max	4.3	6.8	9.1	13	13	20	33	47	47	82	130	350
D20	Min	2.7	4.3	5.6	8	8	13	20	30	30	56	82	200
	Max	6.2	9	12	18	16	27	47	62	62	120	180	470
D25	Min	5.6	8	11	16	15	24	39	56	56	100	160	270
	Max	12	18	24	33	33	51	82	120	120	220	360	800
D30	Min	6.8	11	15	20	20	33	51	68	68	130	220	360
	Max	13	22	27	43	39	62	100	130	130	270	430	1000
D35	Min	9.1	13	18	24	24	39	62	91	91	160	270	560
	Max	24	39	51	75	75	120	180	270	270	510	750	1500
D50	Min	22	33	43	62	62	100	160	220	220	390	620	1200
	Max	56	91	120	160	160	270	430	560	560	1100	1800	3700
D70	Min	43	68	91	120	120	200	330	430	430	820	1300	2200
	Max	91	130	180	270	240	390	680	910	910	1600	2700	6500
D90	Min	51	82	110	150	150	240	390	510	510	1000	1600	3500
	Max	130	220	270	390	390	620	1000	1300	1300	2700	4300	10,000

* UX capacitors are 16 volt rated

APPENDIX C

FREQUENCY-RECONFIGURABLE LNA SIMULATIONS AND MASKS

C.1 Simulation details of the frequency-reconfigurable LNA design using RF-MEMS switch and multimodal coupled microstrip IMN

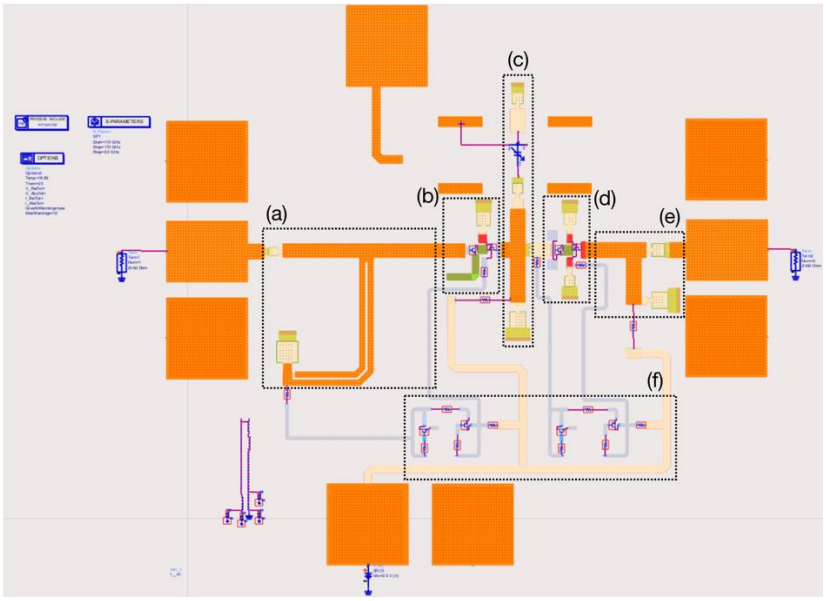


Fig. C.1. ADS schematic of the first LNA design (Section 5.3): (a) IMN, (b) stage 1, (c) ISMN, (d) Stage 2 and (e) OMN and (f) bias network.

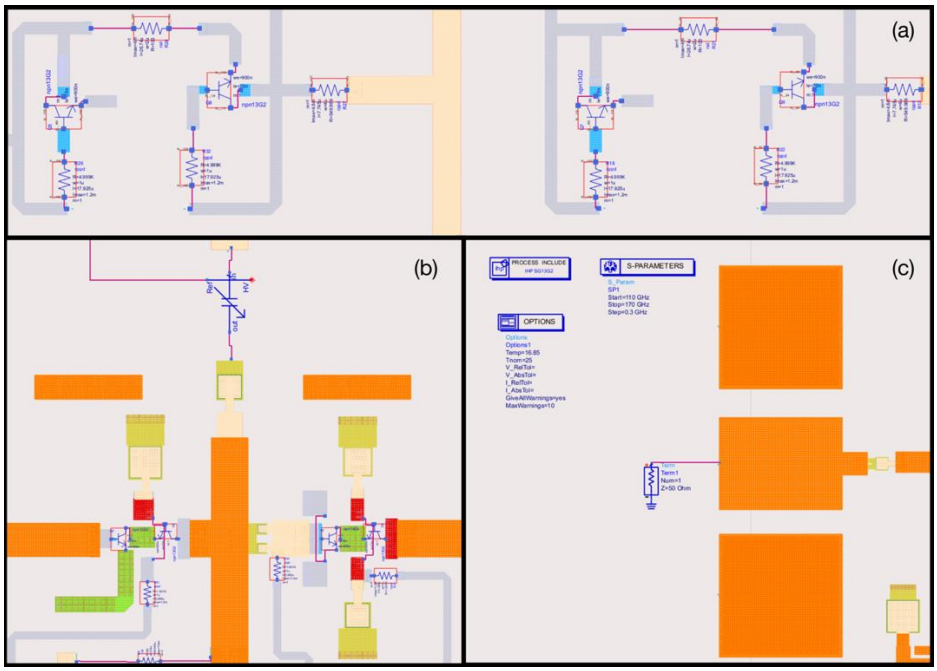


Fig. C.2. Details of the ADS schematic of the first LNA design (Section 5.3): (a) bias network; (b) Stage 1, Stage 2 and RF-MEMS switch; (c) simulation definitions.

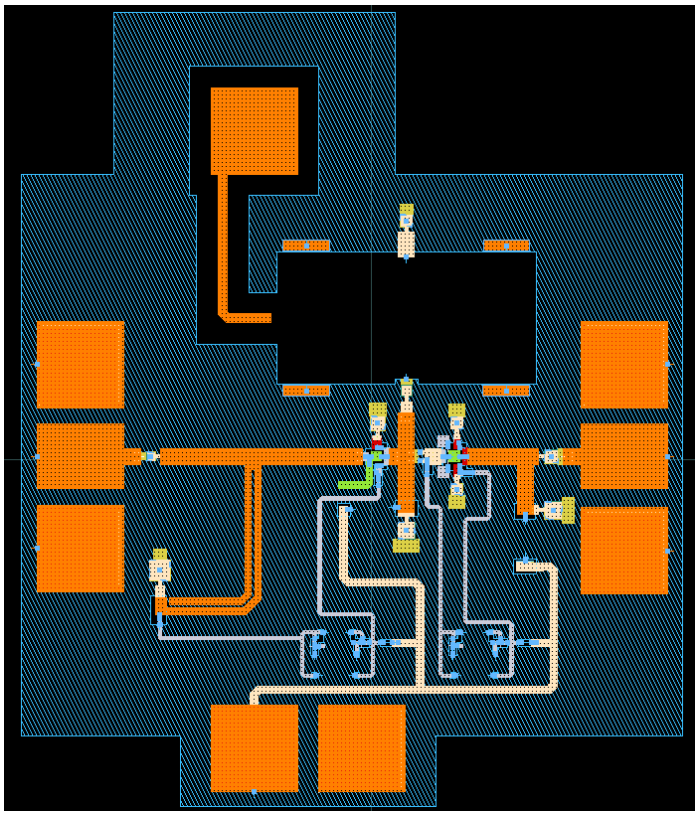


Fig. C.3. Momentum layout for the electromagnetic simulation of the first LNA design (Section 5.3).

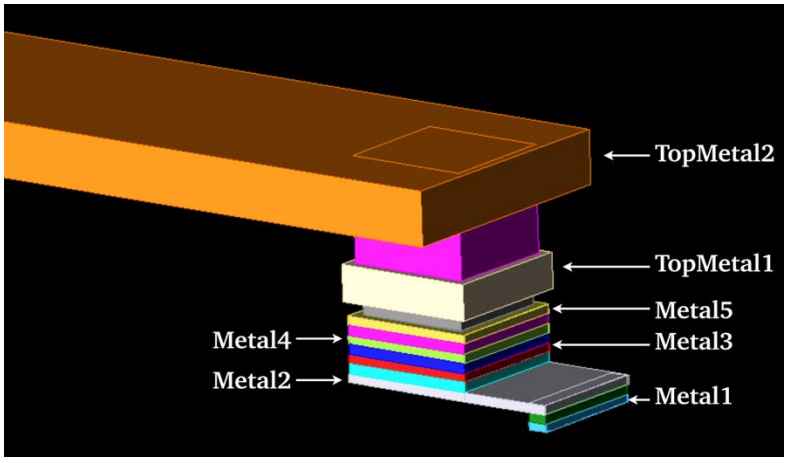


Fig. C.4. Connection between microstrip line L_3 and transistor Q_1 shown in detail (Fig. 5.7).

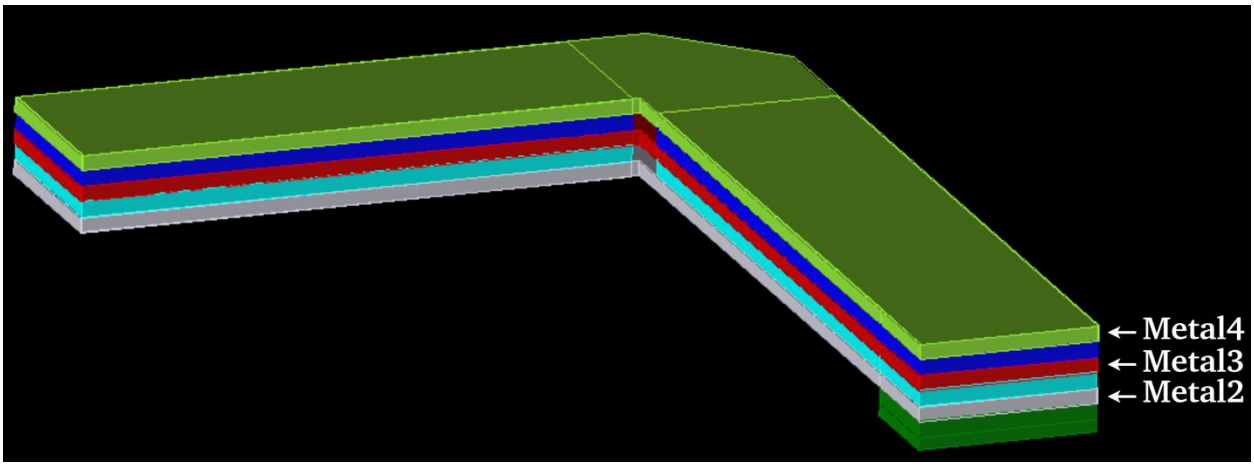


Fig. C.5. Three-stack L_4 line (Fig. 5.7) shown in detail in Momentum's layout.

C.2 Ready-for-construction Momentum masks of the LNA designs

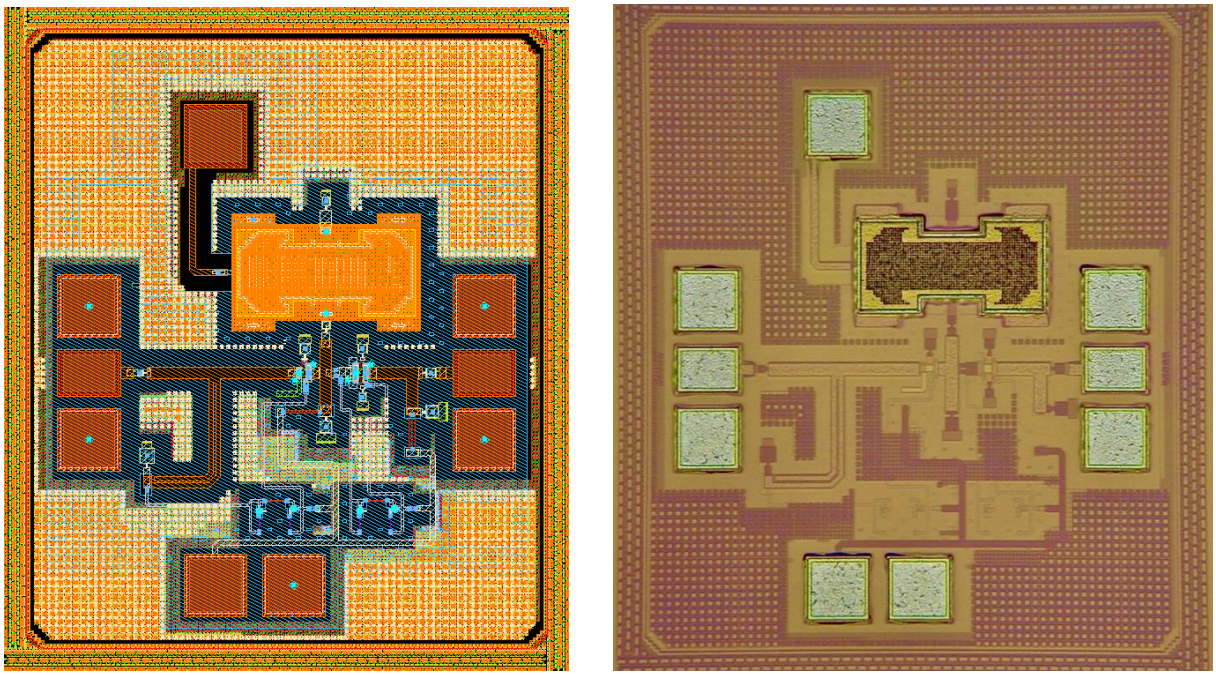


Fig. C.6. Momentum mask (left) and fabricated chip (right) of the first LNA design (Section 5.3).

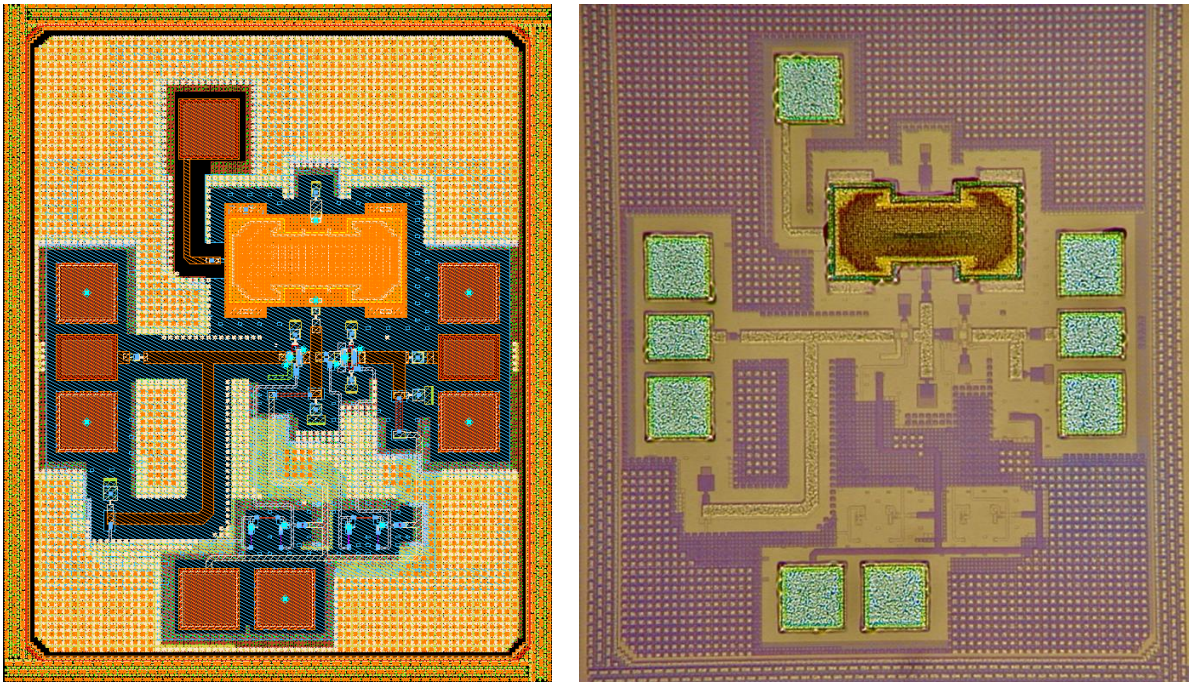


Fig. C.7. Momentum mask (left) and fabricated chip (right) of the second LNA design (Section 5.4).

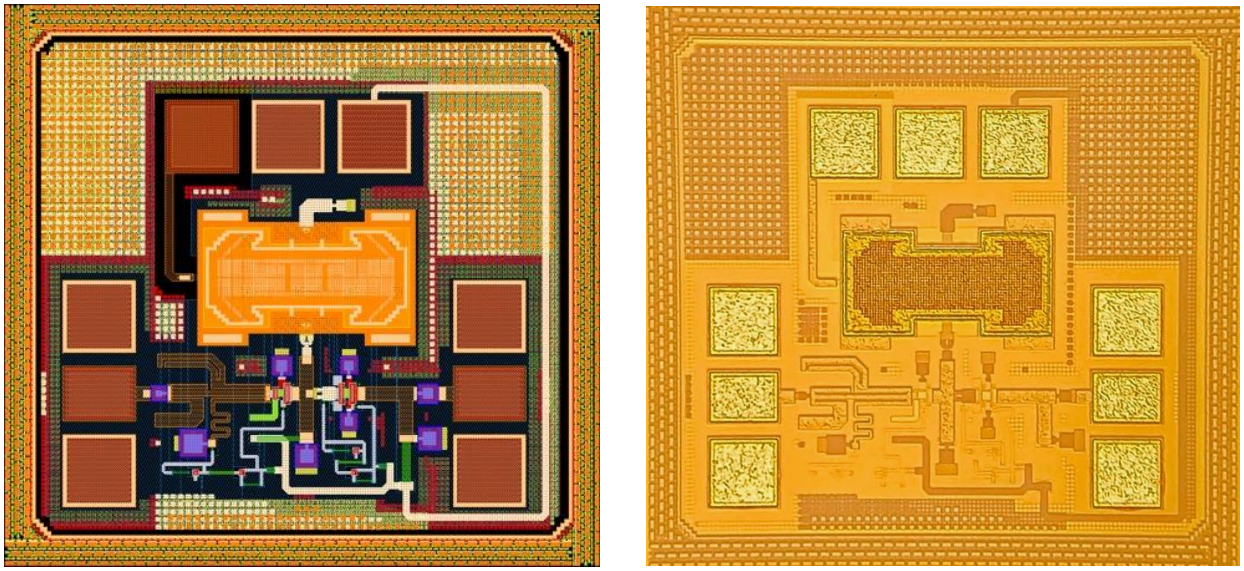


Fig. C.8. Momentum mask (left) and fabricated chip (right) of the third LNA design (Section 5.5).

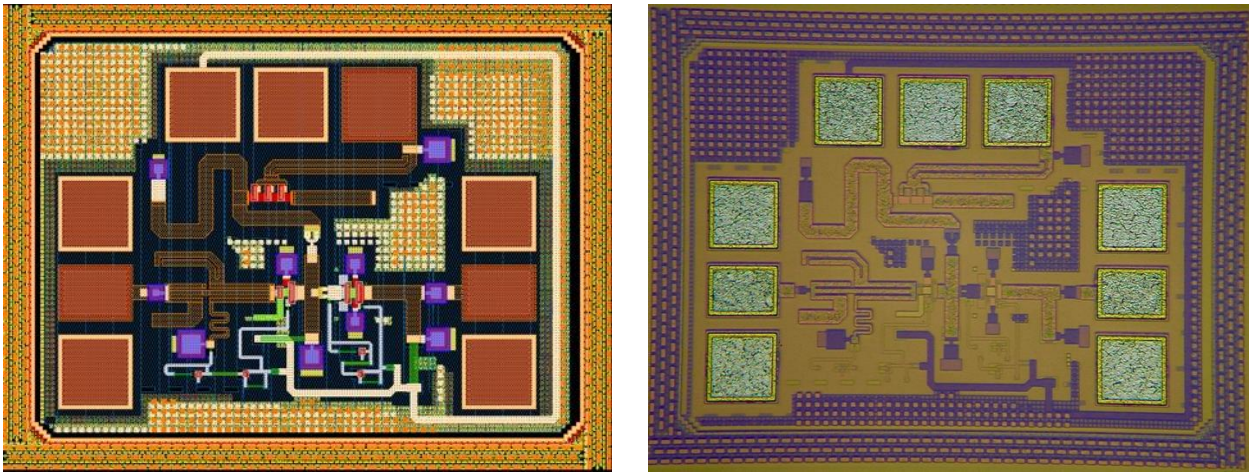


Fig. C.9. Momentum mask (left) and fabricated chip (right) of the LNA design using a HBT-RF switch (Chapter 6).

LIST OF FIGURES

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LIST OF ACRONYMS

BEOL	Back end of line
BiCMOS	Bipolar complementary metal-oxide-semiconductor
CMOS	Complementary metal-oxide-semiconductor
CP	Charge pump
F	Noise figure
HBT	Heterojunction bipolar transistor
HFVPE	Hydrofluoric acid vapor phase etching
IHP	Innovations for high performance
IMN	Input matching network
ISMN	Inter-stage matching network
LNA	Low-noise amplifier
LPS	Line-plus-stub
M1	Metal1
M2	Metal2
M3	Metal3
M4	Metal4
M5	Metal5
MEMS	Micro-electro-mechanical systems
NBL	N^+ buried layer
OMN	Output matching network
RTA	Rapid thermal process
SEM	Scanning electron microscopy
SiGe	Silicon-Germanium
TEM	Transverse electromagnetic wave
TLM	Three-line microstrip
TM1	TopMetal1
TM2	TopMetal2
VSWR	Voltage standing-wave ratio
WLP	Wafer level package

LIST OF PUBLICATIONS

1. **J. Heredia**, M. Ribó, and L. Pradell, "Compact, wideband impedance tuner using a three-line-microstrip structure," *Electronics Letters*, vol. 54, no. 9, pp. 572–574, May 2018.
2. **J. Heredia**, M. Ribó, L. Pradell, S. Tolunay Wipf, A. Goritz, M. Wietstruck, C. Wipf and M. Kaynak, "A 125–143-GHz Frequency-Reconfigurable BiCMOS Compact LNA Using a Single RF-MEMS Switch," *IEEE Microwave Wireless Components Letters*, vol. 29, no. 5, pp. 339–341, May 2019.
3. A. Contreras, J. Casals-Terré, L. Pradell, M. Ribó, **J. Heredia**, F. Giacomozzi, B. Margesin, "RF-MEMS switches for a full control of the propagating modes in uniplanar microwave circuits and their application to reconfigurable multimodal microwave filters," *Microsystem. Technologies*, vol. 23, no. 12, pp. 5959–5975, Dec. 2017. (*this paper is on RF-MEMS switches design, but not related to the Thesis contents*)
4. Submitted for publication: **J. Heredia**, M. Ribó, L. Pradell, S. Tolunay Wipf, A. Goritz, M. Wietstruck, C. Wipf and M. Kaynak, "Miniature switchable millimeter-wave BiCMOS low-noise amplifier at 120/140 GHz using an HBT switch,".

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