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Thermal Management in 3D IC Designs for Nano-CMOS Technologies: Analysis on Graphene- vs. Graphite-based TIM

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Abstract --- With a high thermal conductivity of 3000-5000 W/m-K, Graphene outstands almost all materials in effective lateral heat spreading. Will introduction of 2D monolayer graphene in 3D-IC help in vertical heat conduction too? In this work, we investigate the impact of Graphene- and Graphite- -based inter-die thermal interface material (TIM) on the peak temperature of the 3D-IC. We compare configurations of additional intermediate layer (IL) of monolayer graphene, graphite and copper materials along with TIM. Simulations show a peak temperature reduction of up to 50^0C in GSRC benchmarks. Role of thermal conductivity and the additional IL critical thickness in peak temperature reduction is also investigated. Our discussion encompasses the vertical thermal profile impact on TSV delay and peak temperature dependence on TIM material, thermal-conductivity and thickness. Lastly, of all configurations, we suggest to further investigate a very promising cost-effective graphite-based inter-die TIM along with graphite-based heat spreaders, to compensate the poor heat dissipation problem in 3D ICs.

Keywords -- 3D IC, graphene, graphite based TIM, heat removal in 3D IC, thermal aware TSV performance

I. INTRODUCTION

Through-Silicon-Via (TSV) based three dimensional integrated circuits (3D ICs) are progressively re-assuring for nano-CMOS technologies with their wire length reduction benefits[1] outperforming the 2D technology. The promising 3D IC technology suffers from increased power density, and still lacks good heat removal techniques. Several publications have addressed the problem of thermal management in 3D ICs at various stages of physical design flow including floorplanning and packaging levels. While most of the research is focused on reducing the chip temperature, impact of the vertical thermal gradient in evaluating the interconnect power and performance remains less explored [2].

Some published papers discuss the suitable materials for the TSVs for effective vertical heat conduction. Carbon nanotubes (CNT) are one of the most widely-accepted among them. Other papers focus on the design and materials of the heat spreaders in 3D ICs. With its very high thermal conductivity of 3000-5000 W/m-K, graphene was early explored in 2D designs as a material for heat spreaders. Barua et al.,[3] explored graphene based heat spreaders in 3D ICs and discussed simulation results of monolayer and few layer graphene (FLG) in substantially reducing the on-chip temperature. Though the thermal interface material's (TIM) role in 3D ICs is little known, authors in [4] recently

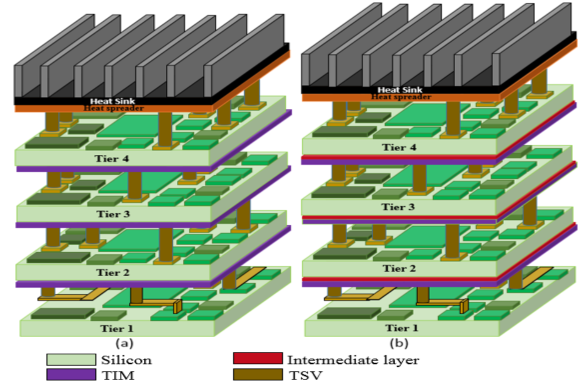

Figure1:3D-IC configuration with (a)TIM and (b)TIM and IL

investigated graphite based TIM in the 2D chips. Authors in [5, p.], consider the 3D IC configuration and in addition to the heat spreaders and TIM, , insert an intermediate layer (IL) of graphene at each device level in 3D IC, as shown in Fig1(b). They claim that it will help in EMI shielding and effective heat spreading. However, no practical or theoretical results have been published in support of this claim.

In this paper, we investigate various 3D IC configurations with three different TIM and IL materials. We consider monolayer graphene, graphite and copper, and we vary thickness of these layers to see if IL of graphene really helps in heat spreading. We also discuss the need for optimization in thermal conductivity and thickness needed to see a reduction in chip peak temperature. Impact of the vertical thermal gradient on TSV performance is also considered.

The organization of this paper is as follows. In Section II, we discourse impact of vertical thermal gradient on the TSV delay in a TSV-based 3D IC. Section III discourses the motivation of why we use intermediate layer of graphene, graphite and copper. Different 3D IC layer configurations are discussed in Section IV. Analysis on the influence of TIM and IL materials and their thicknesses, in reduction of peak temperature are given in Section V. Concluding remarks are presented in Section VI.

II. TSV BASED 3D-IC MODEL AND IMPACT OF TEMPERATURE ON TSV DELAY

In recent years, the state-of-the-art research to address heat removal and alleviating device layer hotspots in 3D ICs is focused on thermal aware floorplanning. The parameters of interconnects are all calculated at room temperature, 27^oC. To the best of our knowledge no work considers the impact of the vertical thermal gradient on the interconnect

performance evaluation. Assuming heat sink on the bottom of the 3D stack and an existing vertical thermal profile, we analyzed the temperature dependence of 3D interconnects, spanning multiple device layers, and 2D wire segments, contained totally on one device layer in our previous work [2]. In that work we were ignoring TSVs. In this paper, we discuss the thermal impact on TSV performance and show a significant underestimation of TSV delay when temperature is not considered. For computing TSV RC delay, we have used simplified TSV coupling capacitance and resistance model proposed by Kim et al. [6] Resistance dependence on temperature is given as,

$$R_{TSV}\ (T) = \ R_{TSV}\ (1 + \beta(T - T_0)) \qquad (1)$$

R_{TSV} is the TSV resistance at room temperature, T (27C), β is the temperature coefficient of the metal. TSV capacitance has two main components, TSV-to-TSV coupling (C_{TT}) and TSV-to-wire coupling (C_{TW}). The electrical parameters and TSV dimensions used are given in Table 1(b). Temperature dependent-TSV delay is computed by,

$$Total\ Delay_{TSV} = \frac{1}{2} R_{TSV(T)} C_{TSV} N_{TSV}^2 \qquad (2)$$

where, N_{TSV} is the number of TSVs in a 3D IC estimated using the probabilistic model proposed in [7].

In this work, all the analysis is done on four-tier final floorplans of GSRC benchmarks [8]. All the floorplans are generated with the non- deterministic floorplanning tool [7]that has been built on the frame of the 3D Floorplanner [9] In this floorplanner, blocks and TSVs are co-placed simultaneously and nets are assigned to TSV islands within the optimization stages. Table 1(a) shows sizes of TSV islands (in the number of TSVs) and the estimated number of TSVs for three GSRC benchmarks.

TABLE 1(a): Impact of device layer temperature on total TSV delay contribution

Benchmark	n100	n200	n300
Array Size	7x6	10x9	11x10
#TSVs	1008	2160	2640

TABLE 1(b): TSV electrical parameters and dimensions at 45nm technology node

Parameter	Value
(Diameter, pitch, height)	(3μ , 6μ , 30μ)
R_{TSV}	71.3 mΩ
C_{TSV}	14.65 fF

A comparison of total TSV delay at room temperature with TSV delay as a function of vertical thermal profile for four device layers are shown in Fig 2. An average 27% underestimation of TSV delay is observed when the metal resistance dependence on temperature is not taken into account. These results again emphasize an importance of considering the temperature dependent interconnect parameters in evaluating 3D IC performance. We show a simplified analysis of TSV performance with the device layer temperature assigned to the TSVs on that layer. A more detailed analysis can be performed considering the TSV going through different material layers of 3D-IC, with each having a different temperature gradient of its own.

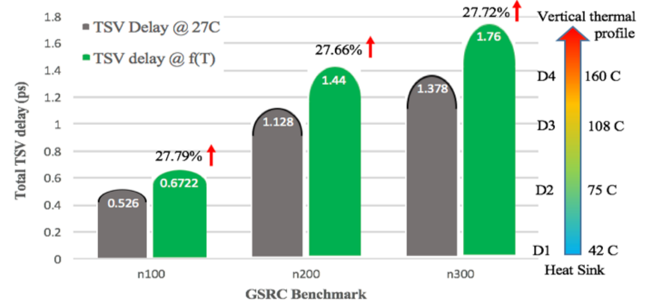

Figure 2: Comparison of total TSV delay in n200 GSRC benchmark at room temperature and with a vertical thermal profile.

III. GRAPHENE/GRAPHITE/COPPER INTERMEDIATE LAYER PROPERTIES

With their high thermal conductivity, graphene and graphite can aid the state-of-the-art thermal optimization techniques in 3D ICs. We investigate how an additional carbon-based IL in 3D IC configuration will help in reducing the unacceptable high peak temperature. The thermal properties of the considered IL materials are thus discussed. The thermal conductivity, κ of a material relates the heat flux per unit area, $\vec{q}$(W/m2) to the temperature gradient as given in Eq 3.

$$\vec{q} = - \kappa \nabla T \qquad (3)$$

The negative sign in the relationship indicates the heat flow from high to low temperature. Graphene is known for its superior heat conducting ability with a very high in-plane (along x-y plane) thermal conductance of 3000-4000 W/m-K, as given in Table 2 and shown in Fig 2. Due to this worthy thermal property of graphene, Du et al., [5, p.] put forth the idea of better heat dissipation in 3D-IC with an inter-die layer of graphene. However, it is important to note that the heat flow in cross-plane (along z-axis) of graphene is weak and limited by the inter-plane van der Waals interactions. The high thermal conducting property becomes merely ~6 W/m-K for cross-plane conduction and actually becomes a vertical thermal dissipation bottleneck.

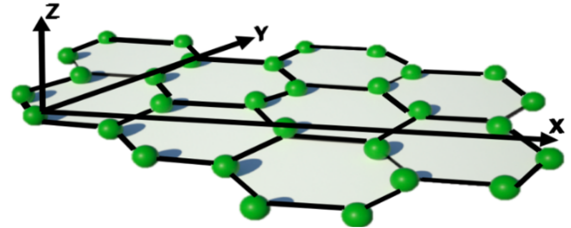

Figure 2: Weak inter-plane van der Waals interactions in the cross plane direction of Graphene (along z-plane)

On the other hand, >1000 W/m-K thermal conductivity of graphene for lateral heat spread is achievable only in its purest form, which is challenging to fabricate and also cannot be suspended freely in 3D ICs. When graphene is supported by SiO_2, the in-plane heat conducting property of graphene degrades to ~600 W/m-K[10], yet still higher than other metals like copper with κ of 389 W/m-K. With κ of

500 W/m-K , with its relatively ease of fabrication, graphite, another possible IL material, is thus also considered in our experiments to enable a good density of the carbon material for vertical heat conduction. Though metals like copper have lower in-plane κ value compared to graphene, it has to be noted that unlike graphene, copper exhibits the same κ in cross-plane as well. Hence, these three materials are used in our work to investigate the effect of additional IL in 3D IC heat removal in the following sections.

Table 2: Material thermal properties in 3D-IC

Material	Thermal conductivity (W/m-K)	Thickness(m)
Pure Graphene	4000[11]	3.35E-10
Supported Graphene (on SiO_2)	600	3.35E-10
Graphite	500	3.35E-10
Copper	389	3.35E-10
Si substrate	142.8	0.00078
TIM	4	2.00E-05

IV. 3D IC LAYER CONFIGURATION TEST CASES

We use HotSpot[12] to simulate temperature distribution, in GSRC benchmarks, for various configurations of 3D IC layers with the IL introduced between the TIM and Si substrate. The test cases considered in our analysis are given in Table 3. With Fig 1(a) being the baseline(TC 0)configuration as highlighted in Table 3, we look at cases with IL introduced (Fig 1(b)) of different materials and thickness.

TABLE 3: Simulated test cases using HotSpot Tool

Test Case #	Configuration
TC 0	Default TIM
TC 1	TIM +Graphene
TC 2	TIM + Graphite(with TIM thickness)
TC 3	TIM + Copper(with graphene thickness)
TC 4	TIM + Copper(with TIM thickness)
TC 5	Graphite-based TIM
TC 6	No TIM, only monolayer Graphene IL used

In TC1, an IL of monolayer graphene is used and simulated with a κ of 600 W/m-K. While this case suffers from the weak van der Waals interactions mentioned in Section 3, we consider graphite as IL material with thickness equivalent to the TIM to enable vertical heat conduction. Copper, with it's property of maintaining the same κ value in-plane and in cross-plane direction, is also studied with varying thickness of TIM and monolayer graphene. TC 5 and 6 are variations of the baseline configuration with different TIM materials and no IL. We also investigate for the critical thickness of the IL beyond which the 3D-IC peak temperature will not decrease any further. The benchmark floorplan for each material case is simulated. We start with graphene monolayer and then increase the thickness by a single layer for each run until the peak temperature reduction is saturated. These cases provide a useful insight for 3D IC designers to understand how the temperature of 3D IC is altered with these materials and configurations. All the thermal simulations are done with Hotspot V6.0 tool[12] at 45nm technology node. GSRC benchmarks of n100, n200 and n300 are simulated with the above configurations. These benchmarks come with only block level connectivity data and no power density information. We thus assume power densities in range of 0.9 to 2.0 W/mm^2 which are randomly generated for each block. We take into account the block size for estimating the block power and a product of the generated power density and block area is used for the total power of the block. Heat sink is assumed to be on top of the 3D IC stack in this work.

V. RESULT ANALYSIS

The floorplanner and HotSpot V6.0 tools were performed on a 4xDual Core Sun SPARC IV CPUs at 1.35 GHz and total 32 GB RAM. The generated final floorplans are used for thermal evaluation in HotSpot tool.

Our initial intent was to observe peak temperature reduction in 3D-IC when a monolayer-graphene is inserted at the interface of inter-die in between TIM and Si. However, when simulated, the peak temperature spiked up unacceptably. Due to this increase, graphene's impact on lateral heat spreading could not be observed. It was evident from the results that this unusual behavior of graphene is because of its very low thickness (one atom thick).

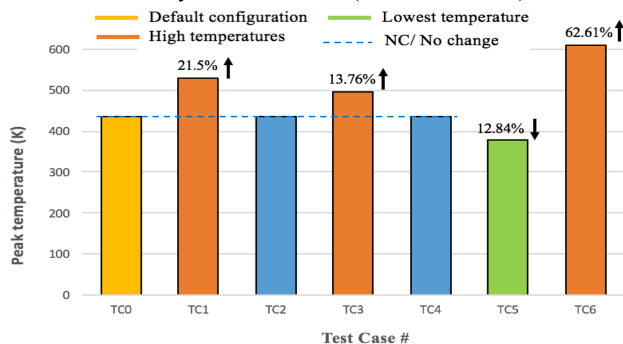

Figure 3: Peak temperatures in n200 benchmark for different configuration. Graphite based TIM achieving the lowest peak temperature can be observed in TC5.

The corresponding increase/decrease of peak temperatures in each configuration compared to the default case for n200 benchmark are given in Fig 3. From test cases 1, 3 and 6 it is evident that, irrespective of the material used for the intermediate layer, the peak temperature of the 3D IC will continue to escalate if the material does not have enough thickness. This is due to the thermal resistive and capacitive components used in the node temperature calculation, given in Eq. 4.

$$C_{th} = area * thickness * volumetric\ heat\ capcity \quad (4)$$

With the direct proportionality to thickness, a low thickness layer cannot store heat effectively and heat transfer will be only due to the thermal resistive component. Hence low

thickness layers are not able to remove heat vertically, and all the power dissipated stays within the Si layer beneath it, resulting in unacceptable temperature rise. The layer thickness was thus increased in steps, to identify the critical thickness beyond which the peak temperature reduction will saturate. Multiple simulations are run with TC1, 2 and 3 configurations starting at monolayer of graphene and increasing the layer thickness by one graphene monolayer for each run until the peak temperature saturates. Results are shown in Fig 4. Even with the lowest thickness, IL of copper achieves the lowest temperature due to its even thermal conduction property in both, in-plane and cross-plane, directions. Interestingly, all three materials saturate at similar thickness and nearly like peak temperatures.

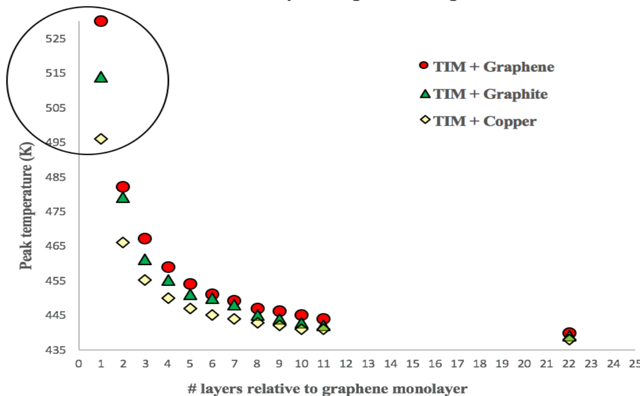

Figure 4: Peak temperature reduction with increasing IL thickness of three different materials in n200 benchmark.

Our final runs include TC5 with graphite based TIM. No IL is inserted in this case. Compared to TC1 with TIM and graphite as IL, TC5 achieved very good peak temperature reduction of 12.84% as shown in Fig 3. This analysis gives us an insight to the minimum thickness required and which material's thermal properties best suit for heat removal in 3D IC at packaging level.

VI. CONCLUSION

The discussion presented in this work aims to understand the impact of graphene or graphite based IL and TIM in 3D IC thermal management at packaging level. While this is achieved merely by the material properties, when implemented in conjunction with other state-of-the art cooling techniques including, micro-channel cooling, thermal aware floorplanning or graphite-based heat spreaders, a further reduction in 3D IC peak temperatures can be achieved. For effective vertical heat conduction, a material with decent thermal conductivity and with good thickness is enough to absorb the heat from the layer beneath it. However, low thickness of a material with a high thermal conductivity will hamper the heat removal process rather than aiding it.

Lastly, we propose to further investigate the use of a very promising graphite-based TIM as an alternative to compensate poor heat dissipation exhibited in 3D ICs. Simulation results show a peak temperature reduction of up to 56°C. It suggests that, for effective thermal management, this might be a potential cost-effective and easy to fabricate method compared to graphene. The simulation results obtained are important for 3D IC designers to take early design decisions and alleviate hotspots even without resorting to other heat removal techniques.

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