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Comparing Past Board Assembly iNEMI Roadmaps to Technology Outcomes

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COMPARING PAST BOARD ASSEMBLY iNEMI ROADMAPS TO TECHNOLOGY OUTCOMES

by

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EXECUTIVE SUMMARY

This project compares past board assembly roadmaps with actual technological outcomes. Its conclusions are mixed: some aspects that the roadmaps covered were very accurate, while others could use improvement. This paper also draws general conclusions on the outline and readability of the board assembly roadmaps. These roadmaps were given to Dr. Lasky and me at no cost from Marc Benowitz, president of iNEMI, for the purpose of this project.

This paper examined the progression of predictions across seven significant aspects of board assembly covered in the 1994, 2002, 2007, 2013 and 2017 roadmaps: 1) Conversion Costs, 2) NPI Cycle Time, 3) Component Trends, 4) Solder Paste, 5) Bar Solder, 6) Wave Solder Flux and 7) Die Attach Adhesives.

Conversion costs were quantified across the 1994, 2002 and 2007 roadmaps and were found to be accurate, if not conservatively estimated (see *Figure 5*). Even the estimate in the 1994 Roadmap for 15 years out was within 0.05 cents of the actual technological outcome per I/O. NPI predictions were found to be extremely accurate quantitatively as well as qualitatively.

The area with the most discrepancy between the roadmaps' predictions and actual technological outcomes is in component trends. Maximum I/O density, minimum pitch for area array packages and chip speed placement were all overestimated markedly, especially in the earlier roadmaps (See *Figures 19 – 21*).

It should be noted that there are discrepancies between these roadmaps, but this project aims to bridge these discrepancies in a comprehensive fashion to better inform iNEMI for future roadmaps.

INTRODUCTION: iNEMI

The iNEMI (International Electronics Manufacturing Initiative) is an industry led research and development consortium of approximately 90 leading electronics manufacturers, suppliers, associations, government agencies and universities. The organization's mission is to forecast and accelerate improvements in the Electronic Manufacturing industry for a sustainable future via collaborative innovation. They accomplish this by road-mapping future technology requirements for the electronics industry globally, identifying and prioritizing technology and infrastructure gaps and helping to eliminate these gaps through high-impact collaborative projects.

The roadmaps have covered 21 unique technology areas or TWGs (Technology Working Groups), spanning fields from Board Assembly, Optoelectronics to Packaging. They not only drive the direction of collaborative internal projects, but electronics manufacturing design and electronics supply chains globally.

Since 1994, iNEMI has produced a roadmap every other year, explaining in detail the anticipated technological advancements needed by large technology companies. These advancements are determined from companies higher on the supply chain regarding the technology they anticipate needing in the next 5 to 10 years. These companies work with iNEMI to congregate ideas on necessary technological advancements at the lower supply chain level for the future by publishing these biannual comprehensive roadmaps. These lower supply chain microelectronics manufacturers rely on this iNEMI roadmap to direct allocation of money to research and development.

However, many leaders in the microelectronics industry have voiced their concern that predictions in these roadmaps have not been accurate of actual technology advancements.

This independent project examines the progression of these roadmaps in the board assembly technology area by qualitatively and quantitatively analyzing predictions from the 1994, 2002, 2007, 2013 and 2017 roadmaps. It should be noted that there are discrepancies between these roadmaps—from general outline to the many aspects of board assembly that are investigated. This project aims to bridge these discrepancies in a comprehensive fashion to better inform iNEMI and identify possible areas for improvement.

INTRODUCTION: BOARD ASSEMBLY

The board assembly technology area includes the materials, equipment, processes, tools and activities necessary to compile and connect integrated circuits, transistors, resistors, displays, printed circuit cards, capacitors and other passive devices into an electrical circuit.

Modern electronics are built on printed circuit boards (PCBs) which are made of composite materials, for example the fiberglass and copper, on the top and bottom of the board that will connect the various electronic components that will be placed onto the board. The board assembly technology area is the process of placing electronic components into their correct places on the PCB and create the solder electrical connections. The first step in this process is applying the solder; a template is used, and solder is then uniformly distributed along the PCB. The resulting solder blocks on the PCB connect components electrically and physically to the PCB. A machine then holds the PCB steady and places the components in their correct locations (Peck). As component sizes get progressively smaller, precision of placement becomes increasingly important. Finally, the board is heated and cooled to solidify the connections. Rigorous inspections ensure that each board functions properly (Peck).

INTRODUCTION: ROADMAPS

This project bases its conclusions off of the examination of the 1994, 2002, 2007, 2013 and 2017 board assembly roadmaps. According to these roadmaps, the main drivers of the board assembly process are reduction in conversion costs and New Product Introduction (NPI) time, increased component I/O density and transition to environmental and regulatory requirements. The iNEMI Board Assembly Technical Working Group (TWG) formed sub-teams to focus on different areas within board assembly. This paper examines the evolution of predictions across: 1) Conversion Costs, 2) NPI Cycle Time, 3) Component Trends, 4) Solder Paste, 5) Bar Solder, 6) Wave Solder Flux and 7) Die Attach Adhesives.

1. CONVERSION COSTS

Conversion cost is the cost to take a group of parts and convert them into a functional electronic assembly, including testing, material and procurement costs less the initial material cost. This is the expected cost by Original Equipment Manufacturers (OEMs), not the actual cost paid by Electronics Manufacturing Services (EMSs).[1] All costs associated with manufacturing and testing the assembly are considered.

With respect to conversion costs, the 1994 roadmap expresses units differently than the rest of the roadmaps (¢/pin). This roadmap also breaks conversion costs into three different categories: commodity, portable and PCMCIA (Personal Computer Memory Card International Association). These predictions are expressed in *Figure 1*. The 1994 Roadmap adds that the United States is 1 to 2 years behind Japan with respect to cost as it does not have enough product volume to generate cycles of learning needed to re-establish infrastructure.

[1] These costs usually align but is slightly more ambiguous during the lead-free transition.

Figure 1

	Current	3 – 5 Years	5 – 15 Years
Conversion cost, commodity ¢/pin	0.45	0.4	0.35 – 0.2
Conversion cost, portable ¢/pin	2	1.5	1 – 0.4
Conversion cost, PCMCIA ¢/pin	2	1.5	0.5 – 0.35

The 2002 Roadmap highlights a swift reduction in conversion costs among all product sectors relative to previous forecasts due to increased productivity and migration of manufacturing activities to low cost countries.[2] The roadmap is pessimistic of this trend, predicting that migrating manufacturing activities to low cost countries will "strip North America of manufacturing capabilities and eventually research and development activities." The roadmap suggests aggressive investment in optoelectronics and high frequency electronics to combat this.

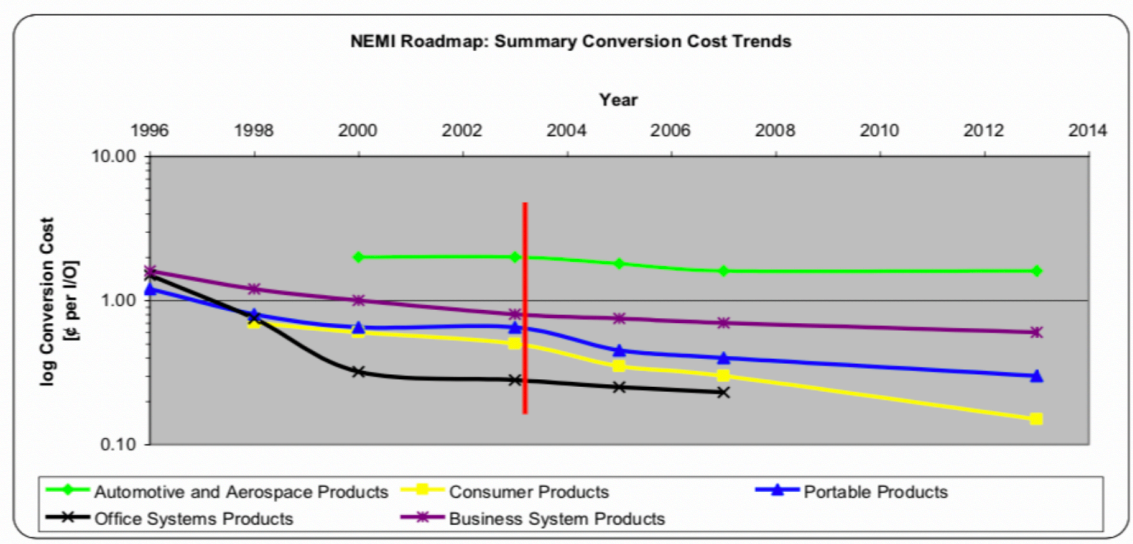
While the microelectronics industry has seen decreased conversion costs across all sectors, the greatest reduction has been in the office systems product sector. This has offered lower costs with the same capabilities to the consumer. *Figures 2* and *3* show 2002 Roadmap projections for conversion costs. Units for conversion costs for the 2002 Roadmap and onwards are expressed in ¢ ÷ I/O (Input/Output).

Figure 2

First Year of Significant Production			2001	2003	2005	2007	2010	2013	2016
Parameter	Metric		Cost						
Automotive and Aerospace Products	¢÷I/O	2000	2.00	1.80	1.60		1.50		
		2002		2.00	1.80	1.60		1.60	
Consumer Products	¢÷I/O	2000	0.60	0.50	0.40		0.22		
		2002		0.4	0.35	0.30	0.20	0.15	
Portable Products	¢÷I/O	2000	0.65	0.50	0.45		0.30		
		2002		0.50	0.45	0.40	0.30	0.30	
Office Systems Products	¢÷I/O	2000	0.32	0.29	0.26		0.19		
		2002		0.28	0.25	0.23			
Business System Products	¢÷I/O	2000	1.00	0.80	0.75			0.65	
		2002		0.80	0.75	0.70	0.65	0.60	0.55

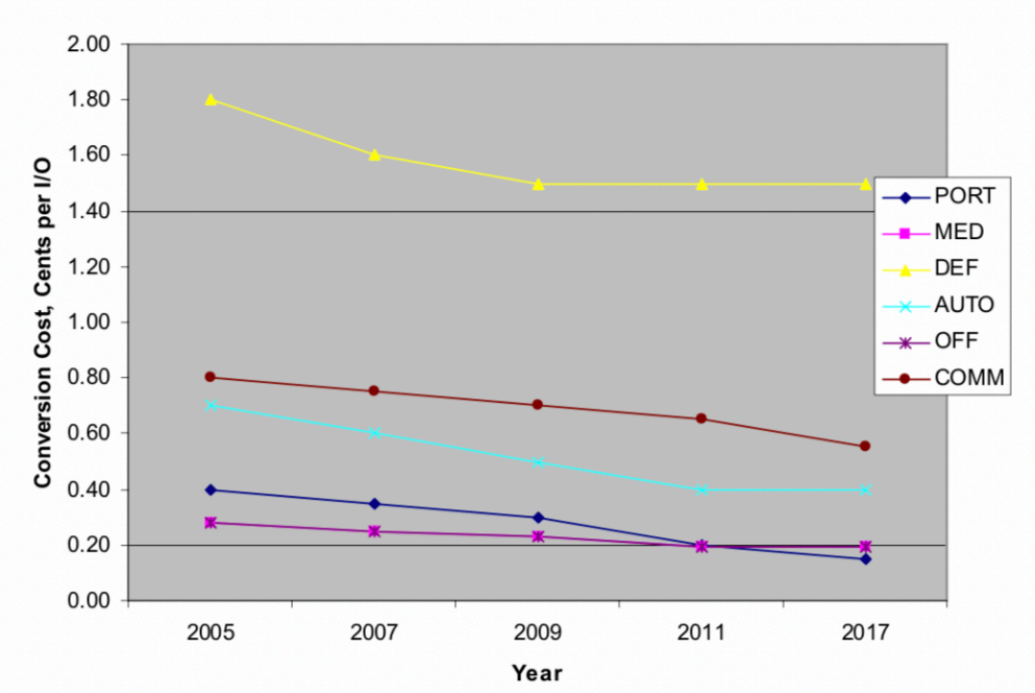
[2] This decrease in conversion costs is said to have no correlation to increased SMT (Surface Mount Technology) utilization.

Figure 3



With respect to conversion costs, the 2007 Roadmap predicts the necessity for significant decreases in conversion costs by 2017, with portable electronics estimating the steepest decline. The defense sector lags other sectors because of its prudent focus on reliability as opposed to cost. The roadmap approximates that conversion costs will be the electronics industry driver after 2011. Conversely to the 2002 Roadmap, the 2007 Roadmap states that the adoption of Surface Mount Technology (SMT) to product designs has enabled conversion cost reductions. There is also a shift in perspective on the continued trend of migration to low cost counties—there is continued optimism in this trend from the 2007 Roadmap and onwards. See *Figure 4* for 2007 Roadmap predictions for conversion costs.

Figure 4

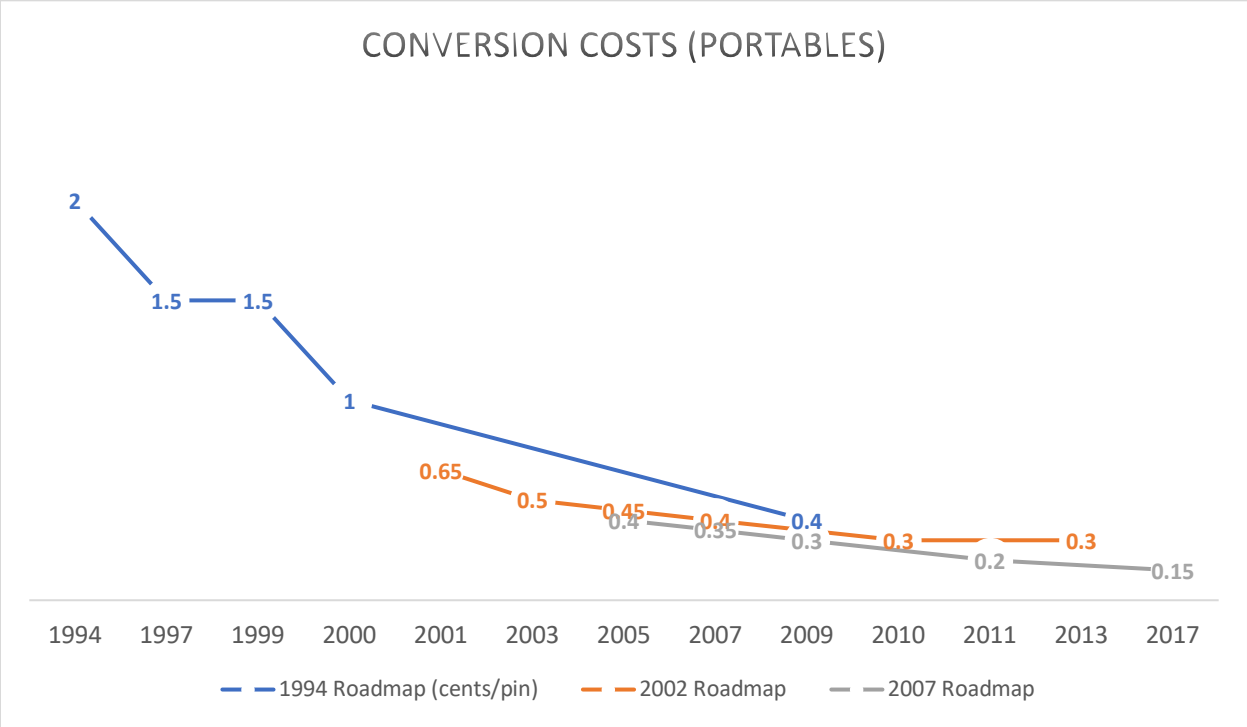


The 2013 and 2017 Roadmaps do not quantify conversion cost predictions, but states that "All costs associated with manufacturing and testing the assembly are considered" and that conversion costs are very closely tied to the escape rate and migration to low cost geographies.

It appears that conversion costs have been estimated appropriately, if not conservatively. *Figure 5* shows predictions for conversion costs across the portables sector,[3] however it should be noted that units differ slightly in 1994 from the 2002 and 2007 roadmaps, from cents per part to cents per I/O, respectively.

[3] The portables sector is the only common sector across all years and seems to be of particular significance.

Figure 5



2. NEW PRODUCT INTRODUCTION CYCLE TIME

New Product Introduction (NPI) cycle time is the time between a design released for alpha prototyping[4] to its release for production. The metric was developed in the 2002 Roadmap and was measured in two categories: 1) Product re-engineering and 2) New products. The time for both of these categories is between the first prototype bill release and the first manufacturing production bill release. *Figure 6* shows projections for both categories.

Figure 6

First Year of Significant Production			*2001*	*2003*	*2005*	*2007*	*2010*	*2013*	*2016*
Parameter	*Metric*	*Cost*							
New Product Introductions	Days	2002		266	200	150		100	
Product Re-spins	Days	2002		50	35	25		15	

(a) Time to Market = Product Documentation released to Manufacturing - First Documentation released to Manufacturing
(b) Based on an average of Business and Office System products

[4] The alpha prototype is used to assess whether the product functions as it is intended to.

The 2002 Roadmap also states that the NPI cycle time is heavily dependent on qualification process time, or the time to confirm that a manufacturer is able to operate at a certain standard during sustained commercial manufacturing.[5] Predicted qualification cycle times in the 2002 Roadmap can be seen in *Figure 7.*

Figure 7

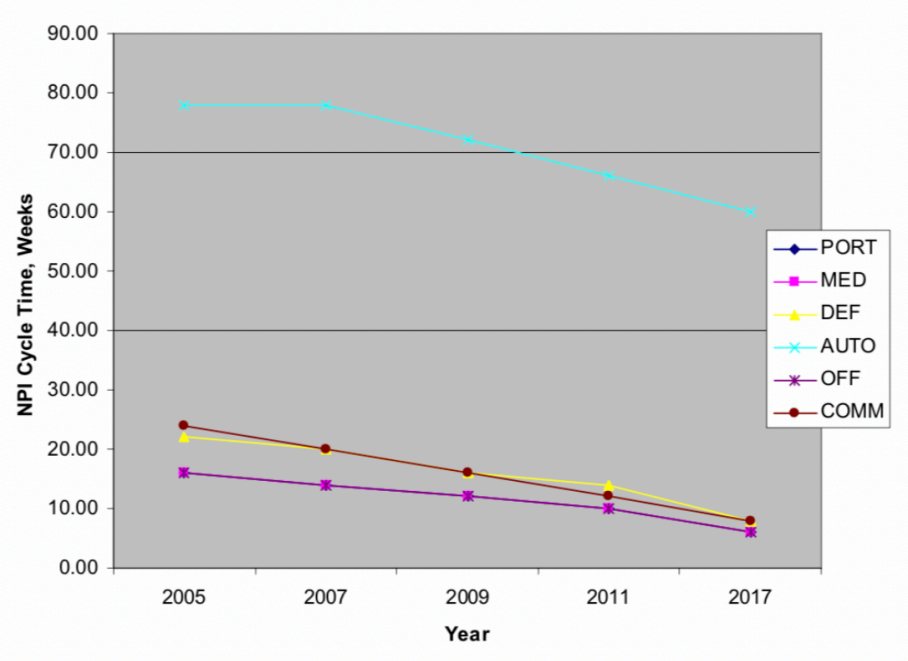
			2001	2003	2005	2007	2010	2013	2016
	Parameter	**Metric**							
	Component Qualification Cycle Time*	Month	2002		3-6	3-6	2-3		1-2	
	Assembly Qualification Cycle Time*	Month	2002		2-4	2-4	2-3		1-3	
	System Qualification Cycle Time*	Month	2002		3-12	3-10	2-8		1-6	
	Customer Qualification Cycle Time**	Month	2002		3-4	3-4	2-3		1-2	

*(a) *Cycle times are measured from the start of the testing cycle in a qualified lab until the release of the product. Any pre-qualification test is not included.*
*(b) ** Cycle times are measured from the receipt of initial product until the customer has verified the functionality and performance stability of the product in the end use environment.*
(c) By 2013 it is assumed that pre-qualification testing will not be necessary.

In the context of NPI Cycle Time, the 2007 Roadmap focuses purely on the second category—new products—but breaks predictions down according to sectors. The roadmap projects a reduction of over 60% in NPI cycle time by 2017, with automobiles, communications and defense having the longest projected NPI and portables, office equipment and medical sectors having shorter NPI times. *Figure 8* shows predicted NPI cycle times from the 2007 Roadmap.

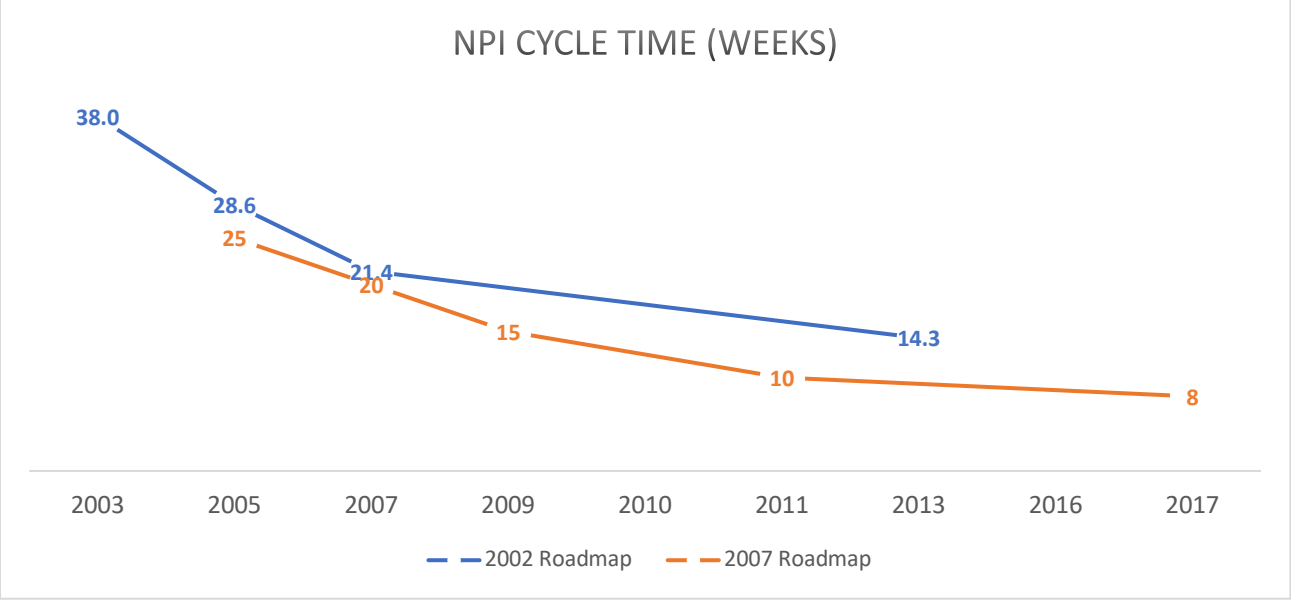
[5] Qualification process time is heavily sector dependent; there are very stringent qualification cycles for harsh environment, medical or large business applications

Figure 8



The 2007 Roadmap was the last roadmap to quantify expectations for NPI cycle time, and a comparison can be seen in *Figure 9*.[6] It appears that estimates in this timeframe were reasonable, if not conservative.

Figure 9



[6] Note that 2002 Roadmap predictions were converted to weeks to match units with the 2007 Roadmap.

The 2013 Roadmap projects that NPI services will follow the demands of the industry and are not going to be a gate for future developments. The roadmap also breaks NPI into four phases: Functional Verification and Testing, Proof of Concept, Manufacturing Readiness and Ramp to Volume. In 2013, some OEMs also started to outsource NPI, although there has been virtually no development of material sets aimed specifically at NPI needs. The 2013 Roadmap does not cover key product sectors, because these expectations are well established in their respective sectors.

The 2013 Roadmap gives keys recommendations for NPI cycle time reduction, including having design rules applied as early as possible, having design rules include commonalities, minimizing hard tooling or other set-up functions (which add cost and increase cycle time) and adding more time to test strategy at NPI stage. *Figure 10* shows a table of attributes of NPI. The roadmap also suggests increased investment in modeling and simulation.

Figure 10

	Unit	Functional Verification	Proof of Concept	Mfg Readiness	Ramp to Volume
Quantiites		< 10	< 10	< 100	100-1000+
DfM	Percentage of total design checks available	< 20%	< 40%	60 - 100%	100%
Reliability	Various	None	HALT	HALT, ESS, ALT, etc	Burn-in, HASA, ORT, etc
Mfg Cycle Time	Days in Mfg	< 5	< 10	Standard	Standard
Test	Various	Function with other assy	Flying Probe, Xray	Production Level	Production Level

The roadmap breaks future priorities with respect to NPI into short, medium and long-term priorities.[7] Short term priorities include the elimination of hard tooling and counterfeit parts from the supply chain. Medium term priorities include the use of modeling simulation tools and

[7] Short term, medium term and long term are defined as 1 to 3 years, 3 to 7 years and 8 or more years respectively.

the consolidation of DfX rule systems to accommodate new technologies. Long term priorities include a transition to deposited materials as a replacement for discrete components, different delivery methods, material developments to help qualify high reliability applications and new interconnect technologies to provide more flexible routing options, reducing or eliminating PCB fabrication cycle time.

The 2017 Roadmap breaks NPI into the same four phases (Functional Verification and Testing, Proof of Concept, Manufacturing Readiness and Ramp to Volume). Additionally, the *exact same* key recommendations are given (having design rules applied as early as possible, having design rules include commonalities, minimizing hard tooling or other set-up functions and adding more time to test strategy at NPI stage). Likewise, the 2017 Roadmap gives the same recommendation for investment in modeling and simulation. *Figure 10* is also presented in the 2017 Roadmap. This latest roadmap also breaks priorities into short, medium and long-term. To contextualize these priorities, it is useful to examine how they compare and contrast to the 2013 Roadmap. It is reasonable to assume that short-term priorities should have been accomplished by the publication of the 2017 Roadmap. It is also reasonable to assume that medium-term priorities would have shifted to short-term priorities, however because long-term is defined as 8 or more years, it seems presumptuous to assume that all long-term priorities would move to the medium-term.

In some cases, the 2013 Roadmap gave an accurate time horizon for priorities. For example, the consolidation of DfX systems moved from medium-term to short-term. However, other priorities seem to have been classified too ambitiously: for example, the elimination of counterfeit parts from the supply chain remains a short-term priority. Likewise, the use of modeling and simulation tools remains a medium-term priority in the 2017 Roadmap. It should

be noted that all long-term priorities in the 2013 Roadmap remain in the long-term horizon in the 2017 Roadmap.

3. COMPONENT TRENDS

This section examines component trends, scrutinizing maximum component I/O density, the maximum I/O per package divided by the package area (max I/O per area), component and substrate sizes and component placement rates. Similar to the discrepancy of units in the conversion cost section of this paper, the 1994 Roadmap expresses packaging density in parts per square inch rather than I/O per square centimeters. The earliest roadmap also highlights the transition from packaged ICs to packageless direct chip attach. See *Figure 11* for 1994 Roadmap predictions for component trends.

Figure 11

	Current	3 – 5 Years	5 – 15 Years
Parts / in^2	105	200	275 – 500
Pins / part	35	52	75 – 270
IC lead pitch (mm)	0.5	0.3	0.2 – 0.07

The 2002 Roadmap indicates that the complexity of components will nearly double by 2013 for all product sectors, which could shape component types, size and pitch. The roadmap forecasts a flattening of the pitch in perimeter, array area packages and die size. Figure 12 shows estimates for Maximum I/O Density by sector. *Figure 13* shows predictions for component and substrate sizes and *Figure 14* shows predictions for component placement rates.

Figure 12

First Year of Significant Production			2001	2003	2005	2007	2010	2013	2016
	Parameter	Metric	Cost						
	Automotive and Aerospace Products	I/O÷cm²	2000	100	180	260		1500		
			2002		180	260	260		1500	
	Consumer Products	I/O÷cm²	2000	208	256	280		470		
			2002		208	256	280	320	360	
	Portable Products	I/O÷cm²	2000	175	240	290		400		
			2002		280	320	350	400	450	
	Office Systems Products	I/O÷cm²	2000	160	240	400		630		
			2002		240	400	630		630	
	Business System Products	I/O÷cm²	2000	156	196	256		400		
			2002		237	256	278	331	400	494

Figure 13

First Year of Significant Production			2001	2003	2005	2007	2010	2013
	Parameter	Metric						
	Passives – Discrete	Mils	2000	10x20	10x20	Deposited		Deposited	
			2002		10x20	10x20	10x20		Deposited
	Passives – Arrays Pitch	Mm	2000	0.5	0.4	0.4		0.4	
			2002		0.4	0.4	0.4		0.4
	Area Array Pitch (Underfilled)	Mm	2000	0.5	0.4	0.25		0.2	
			2002		0.65	0.5	0.5		0.4
	Perimeter Pitch	mm	2000	0.4	0.4	0.4		0.3	
			2002		0.4	0.4	0.4		0.4
	Maximum Component Complexity (Array)	I/O's / Part	2000	700	1000	1200		1500	
			2002		1156	1300	1500		2000
	Large Substrate Products	mm	2000						
			2002		500x585	500x585	500x585		500x585

Figure 14

FIRST YEAR OF SIGNIFICANT				2001	2003	2005	2007	2010	2013
	Parameter	Metric	Chip Placement						
	Chip Placement (multi-Gantry) (Actual measured rate)	cph	2000						
			2003		80,000	110,000	120,000		150,000
	Chip Placement (turret)	Cph	2000						
			2003		27,000	33,000	38,000		45,000
	Chip Placement (Gantry)	m^2/hr	2000						
			2003		14,000	17,000	20,000		25,000
	Chip Placement (not gang) Per IPC 9850 Std.	Cph	2000						
			2003		25,000	37,000	48,000		60,000
	Chip Placement (not gang)	m^2/hr	2000	8,000	9,000	Deposited		Deposited	
			2003		8,000	9,000	12,000		Deposited
	Parameter	Metric	IC Placement						
	IC Placement (BGA / QFP) to 25mm On the fly Vision & (208 QFP / 480 BGA)	Sec/part	2000	0.4	0.3	0.25		0.20	
			2003		0.6	0.4	0.3		0.2
	IC Placement (BGA/QFP) w/vision	Sec/part	2000						
			2003		3.0	2.8	2.2		<2
	IC Placement (CSP) w/vision Low ball count <120 i/o, w/tape	Sec/part	2000	1.5	1.3	1.0		.25	
			2003		1.5	0.3	0.25		0.10
	IC Placement (C4/FCA) W/ Ball Inspect, w/o fluxing, w/tape	Sec/part	2000						
			2003		1.5	1.5	1.0		0.5
	IC Placement (C4/FCA) W/ Ball Inspect W/ball inspect, w/fluxing, w/tray	Sec/part	2000						
			2003		4.0	4.0	3.0		2.0

The 2007 Roadmap predicts a significant increase for maximum component I/O density in the portables sector. In the office equipment and defense sectors predict a plateau after 2009 due to the high cost of fine line routing for PCBs and flattening die size increases. In terms of minimum package pitch for area array packages. See *Figure 15* for component I/O density predictions by sector.

The 2007 Roadmap predicts a 0.4 mm minimum package pitch for area array packages by 2009 and 0.3 mm by 2011. See *Figure 16* for predictions by sector.

Figure 17 shows the part placement technology forecast in the 2007 Roadmap.

Figure 15

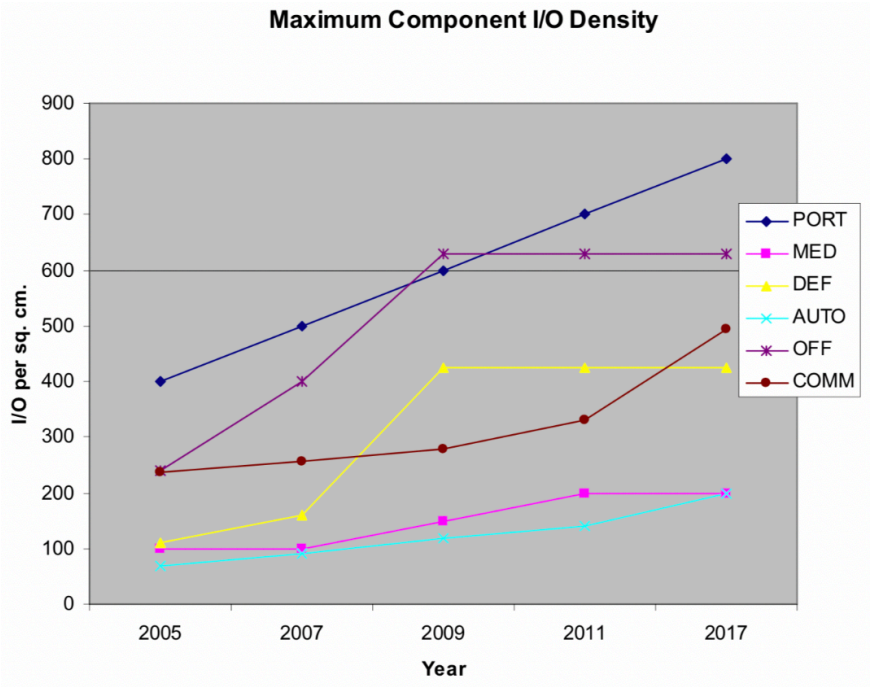


Figure 16

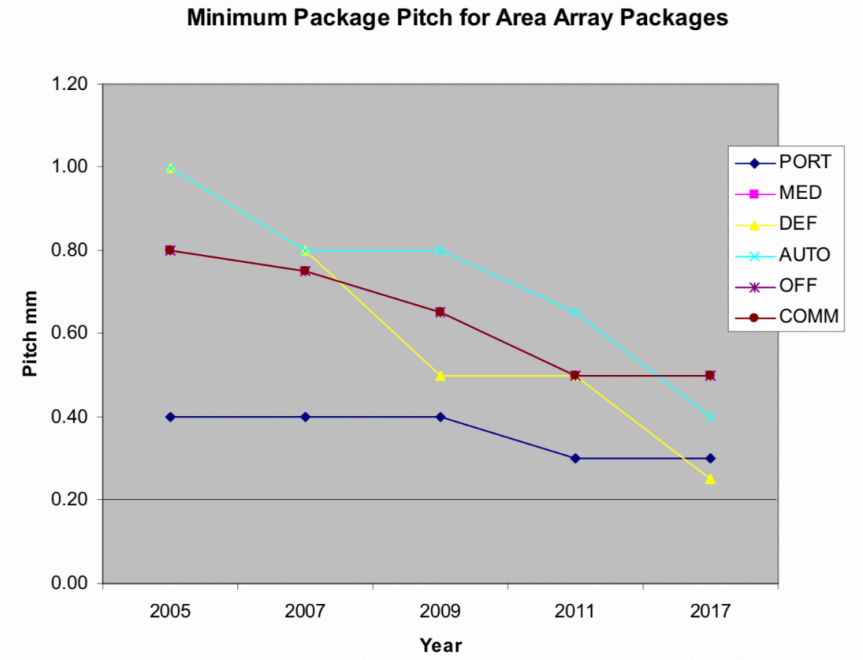


Figure 17

Parameter	Metric	2005	2007	2009	2011	2017
Chip Placement Speed	CPH per square meter using the IPC 9850 standard for 0603 components	12,000	15,000	16,000	17,000	20,000
IC Placement Speed - Large Size IC	CPH per square meter using the IPC 9850 standard for QFP 208	1,200	1,500	1,600	1,700	2,000
IC Placement Speed - Medium Size IC	CPH per square meter using the IPC 9850 standard for SO-16	5,400	6,750	7,200	7,650	8,000
IC Placement Speed - Flip Chip	CPH per square meter	5,000	6,000	7,000	8,000	10,000
Chip Placement Speed	CPH per square meter using the IPC 9850 standard for 0603 components	12,000	15,000	16,000	17,000	20,000
IC Placement Speed - Large Size IC	CPH per square meter using the IPC 9850 standard for QFP 208	1,200	1,500	1,600	1,700	2,000
Placement Accuracy Chips	Microns	70	50	40	30	30
Placement Accuracy Fine Pitch	Microns	60	50	40	30	30
Rotation Accuracy Fine Pitch	Degrees	0.3	0.1	0.1	0.07	0.05
Component Pick reliability	% pick reliability	99.8	99.9	99.95	99.97	99.97
Minimum Placement Force Range	Grams	50	40	30	20	10
Maximum Placement Force Range	Grams					

In the context of component trends, the 2013 Roadmap predicts that increasing maximum I/O density[8] will demand further reduction in device pitch size. The portables sector predicts a 0.4 mm pitch by 2013 and a 0.3 mm pitch by 2015. *Figure 18* shows placement speed estimates from the 2013 Roadmap.

Figure 18

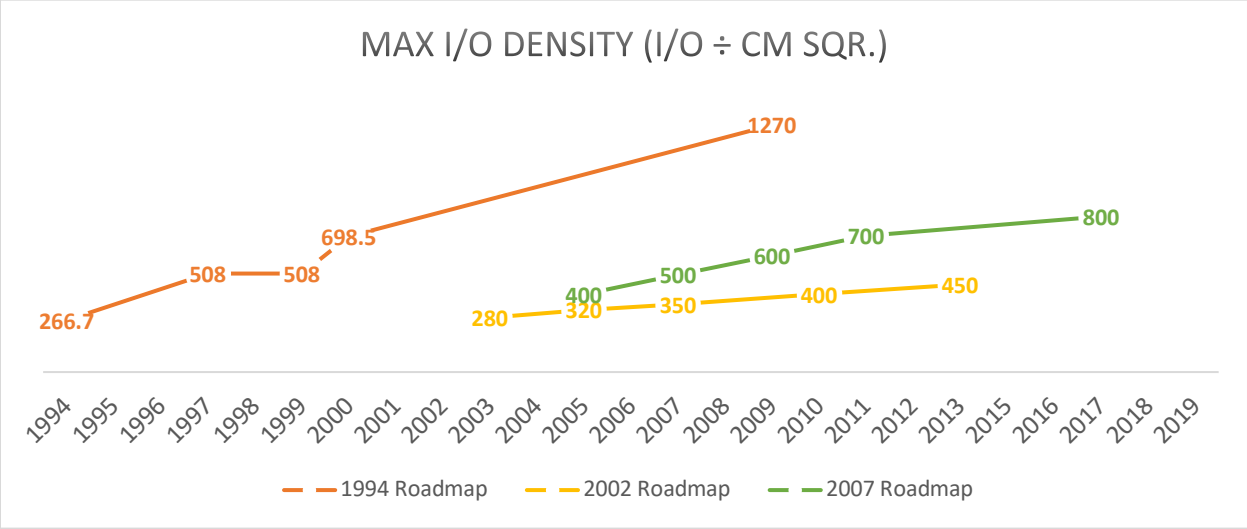
Parameter	Metric	2007	2009	2011	2013	2019
Chip Placement Speed	CPH per square meter using the IPC 9850 standard for 0603 components	15,000	17,000	19,000	22,000	28,000
IC Placement Speed - Large Size IC	CPH per square meter using the IPC 9850 standard for QFP 208	1,600	1,700	2,000	2,300	3,200
IC Placement Speed - Medium Size IC	CPH per square meter using the IPC 9850 standard for SO-16	7,000	7,500	8,500	10,000	15,000
IC Placement Speed - Die Placement	CPH per square meter	6,000	7,000	8,000	9,500	12,000

[8] The 2013 Roadmap does not quantify estimates for maximum I/O density.

The 2017 Roadmap also does not quantify the maximum I/O density but predicts a 0.3 mm pitch by 2019 in the portables sector. The placement speed estimates table in the 2017 Roadmap is identical to that in the 2017 Roadmap (see *Figure 18*).

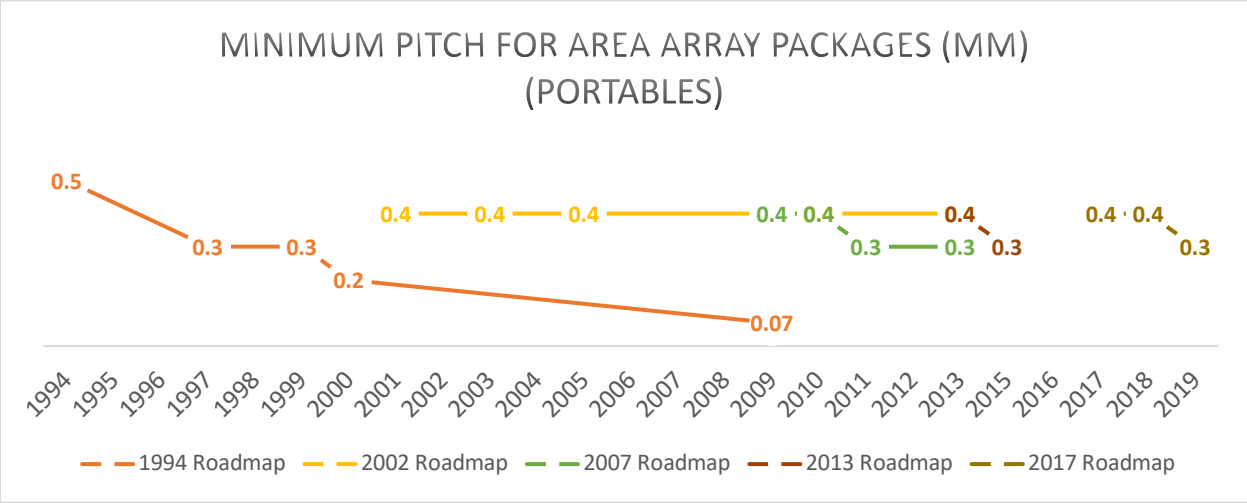
Looking at component trends throughout these roadmaps, we notice substantial over-optimism in earlier roadmaps. However, this seems to be corrected in later roadmaps. See *Figure 19* for a comparison of the 1994, 2002 and 2007 Roadmaps in the context of maximum I/O Density. It appears that the 1994 Roadmap was overambitious, the 2002 Roadmap was under-ambitious, and the 2007 Roadmap met these projections in the middle. Again, note that maximum I/O density was not quantified in later roadmaps.

Figure 19



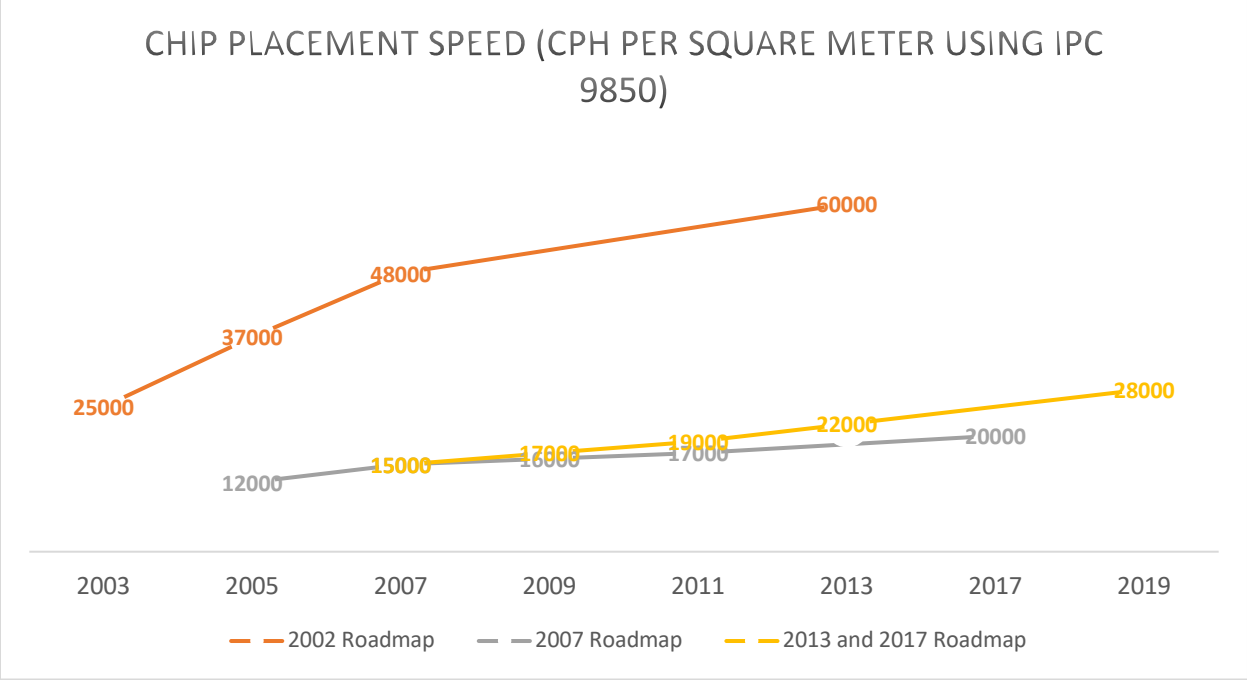
See *Figure 20* for a comparison of all roadmaps in the context of minimum pitch for area array packages in the portables industry. It appears that iNEMI was consistently overambitious, most so in the 1994 Roadmap, but also by consistently predicting and re-predicting the transition from 0.4 mm to 0.3 mm pitch size.

Figure 20



See *Figure 21* for a comparison across the 2002, 2007, 2013 and 2017 Roadmaps in the context of chip placement speed in components per hour (CPH). Note that the exact same tables were given in the 2013 and 2017 Roadmaps (see *Figure 18*). Similar to the maximum I/O density estimates, the 1994 Roadmap was incredibly optimistic while the 2007 Roadmap was under-optimistic, and the 2013 and 2017 Roadmaps met these estimates in the middle.

Figure 21



4. SOLDER PASTE

Solder paste is a powder metal solder that is suspended in a thick flux to act as a temporary adhesive, holding components together until the soldering process fuses parts together. Beginning in 2007, the iNEMI roadmaps provide estimates on the percent of solder pastes that will be lead-free and halogen-free. Since 2007, there has been a prediction of the transition to lower temp lead-free solder alloys in 2011 to 2017 timeframe, but this is still a prediction in the 2017 roadmap. It seems that this has been consistently overestimated. *Figure 22* and *23* show lead-free predictions for North America and Worldwide, respectively.

Figure 22

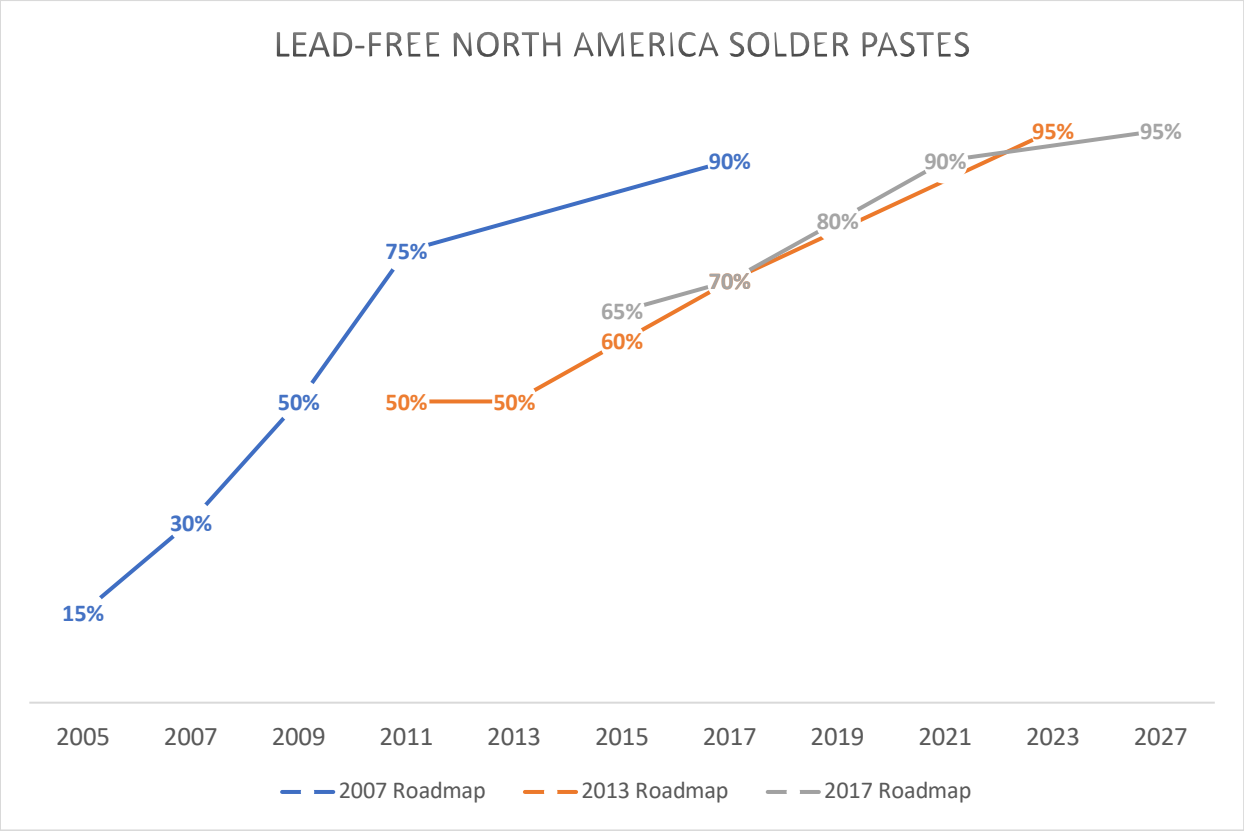
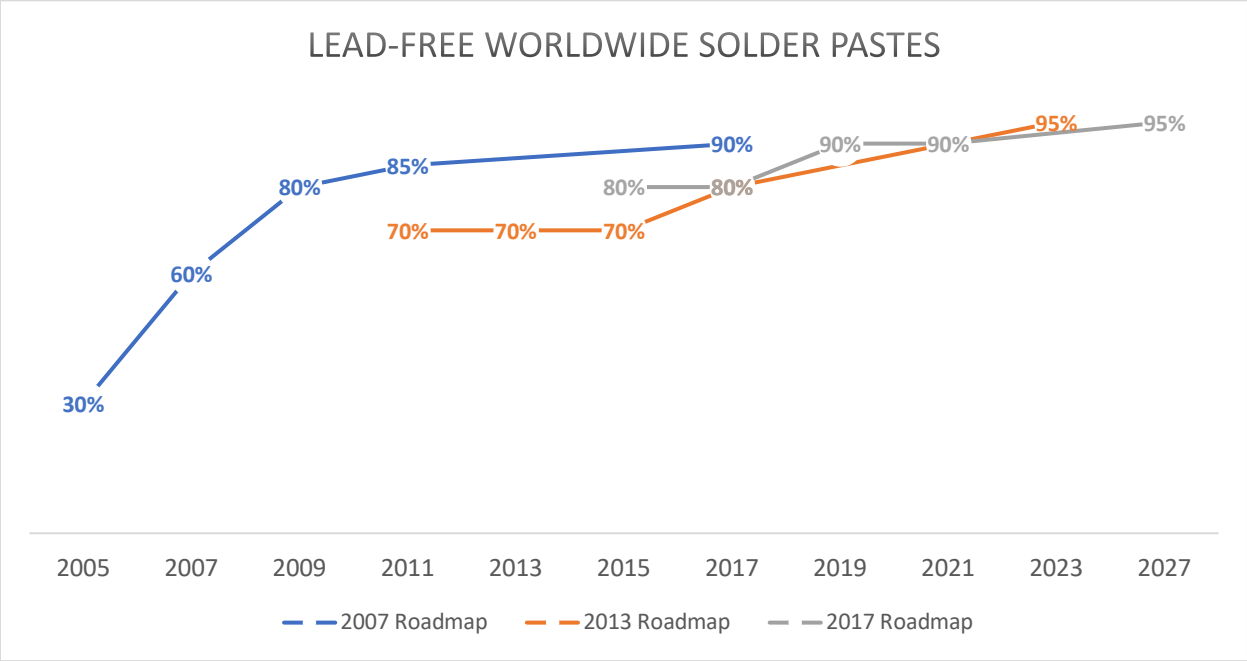


Figure 23



It appears that the percentage of halogen-free solder was overestimated in the 2007 Roadmap, but later corrected in the 2013 and 2017 Roadmap.

5. BAR SOLDER

Beginning in 2007, the iNEMI roadmaps provide estimates on the percent of bar solder that will be lead-free. The 2007 Roadmap highlights the trend towards increased adoption of low silver content wave solder alloys, which have an equal or better performance than high silver alloys at a lower cost.[9] The 2007 Roadmap also highlights the industry need for lower melting point lead-free alloys.

The 2013 Roadmap highlights not only the increased adoption of low silver solder alloys, but also the increased adoption of no silver solder alloys. Again, there is the longer-term goal to develop lower melting point lead-free alloys. Moreover, thicker boards with lower cost pad

[9] Silver pricing is extremely volatile.

finishes and higher layer counts will influence new solder alloy development, especially alloys with superior wetting properties. Additionally, the 2013 Roadmap notes the movement to selective soldering (which will reduce the tonnage of bar solder) and recycling solder dross.

The 2017 Roadmap makes similar comments as the 2013 Roadmap about no silver alloys, lower melting point lead-free alloys and recycling solder dross. However, it also highlights copper dissolution, as it remains an issue on thick, high layer count Telecom boards. See Figures 24 and 25 for a comparison of lead-free bar solder percentages in North America and Worldwide, respectively.

Figure 24

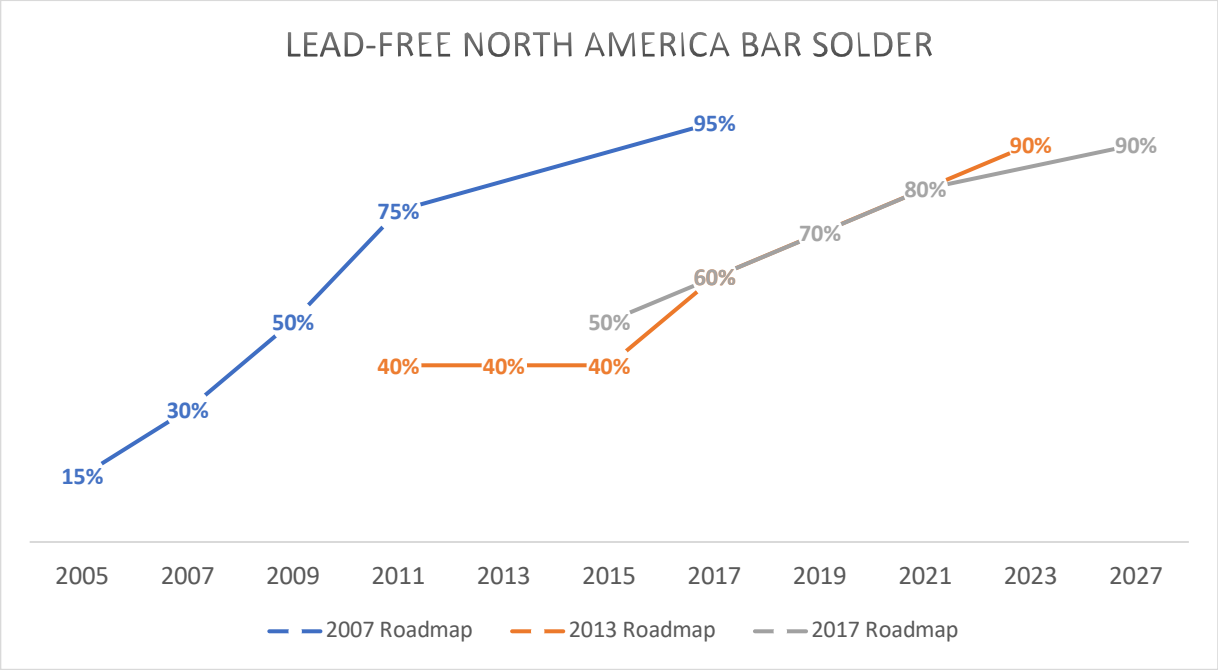
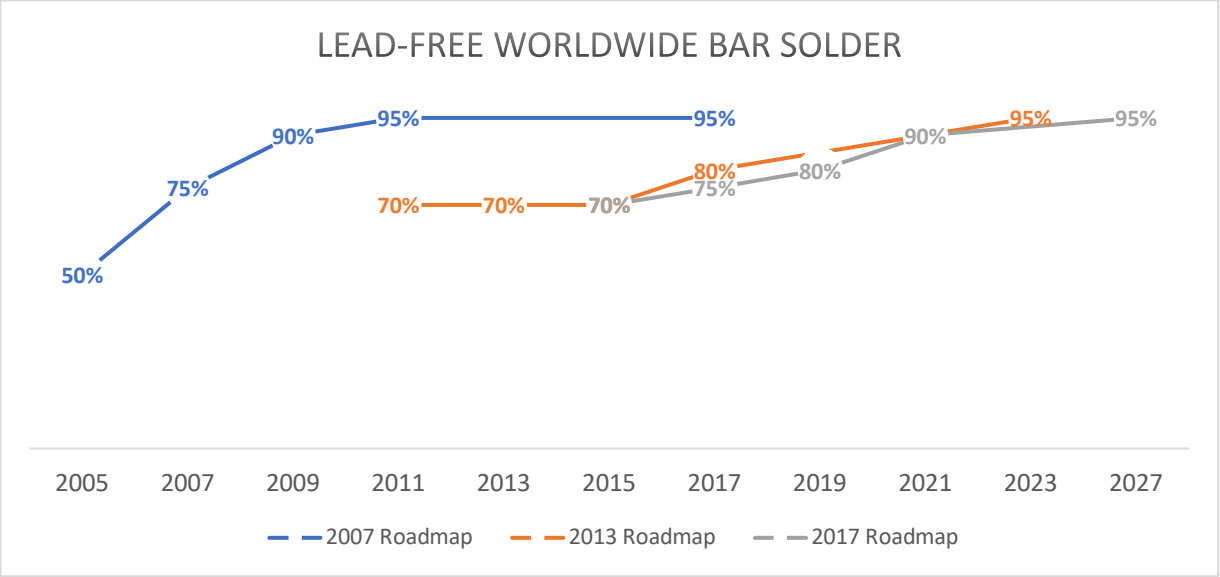


Figure 25



6. WAVE SOLDER FLUX

Wave soldering is used in bulk manufacturing of printed circuit boards. Beginning in 2007, iNEMI began making estimates on what percentage of wave solder flux would be volatile organic compound (VOC) free and halogen free. The 2007 Roadmap highlights the need for dual alloy compatibility because of uncertain schedule for lead free implementation in autos, medical, aerospace and defense. Wave soldering fluxes that have the ability to perform with tin, lead and high temperature lead-free applications were also predicted in to be important through 2011.

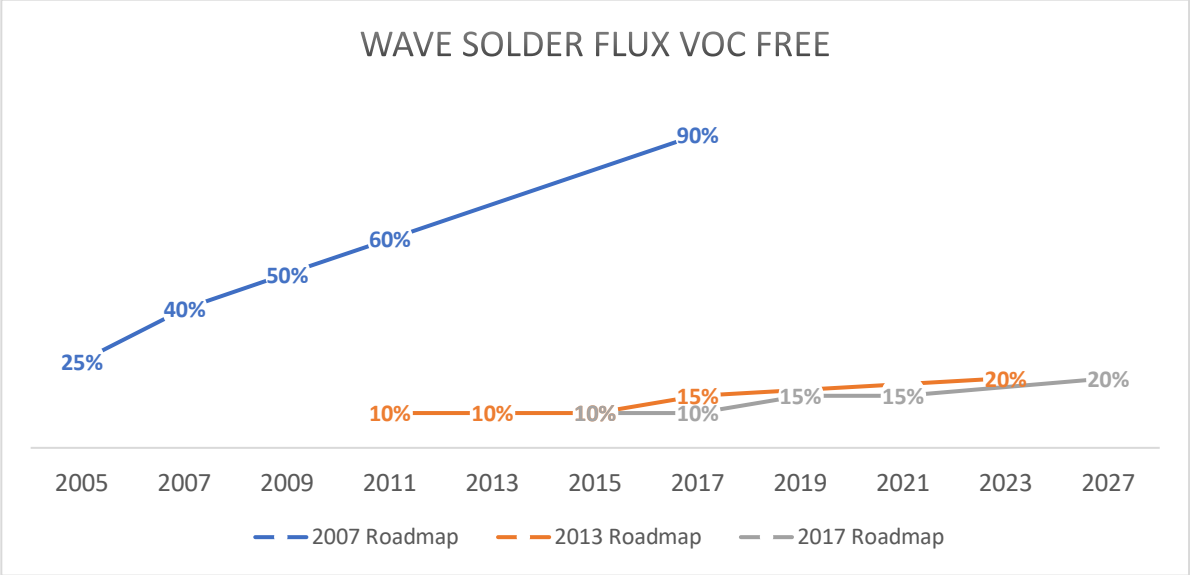
The 2013 Roadmap identifies that thicker boards (greater than 2 mm) with low cost pad finishes and preconditioned by prior SMT reflows as an important market driver as Telecom transitions to lead-free, as higher layer counts require longer dwell times. The Roadmap also predicts that environmental initiatives will drive growth of halogen-free flux. VOC fluxes are also desirable, but the roadmap does not anticipate as much dominance here because of hole-fill difficulties on thicker boards.[10]

[10] This, however, has the capacity to change if legislation changes.

Similarly, the 2017 Roadmap highlights thicker boards as an important market driver as Telecom transitions to lead-free. Identical language is used in the 2017 Roadmap as the 2013 Roadmap in terms of halogen-free and VOC-free fluxes. Rather, in 2017, fluxes were formulated to meet the electro-migration standards set in J-STD-004, as some products have experienced failures do to electro-migration. Pin testability is also said to be important for ICT for longer dwell times.

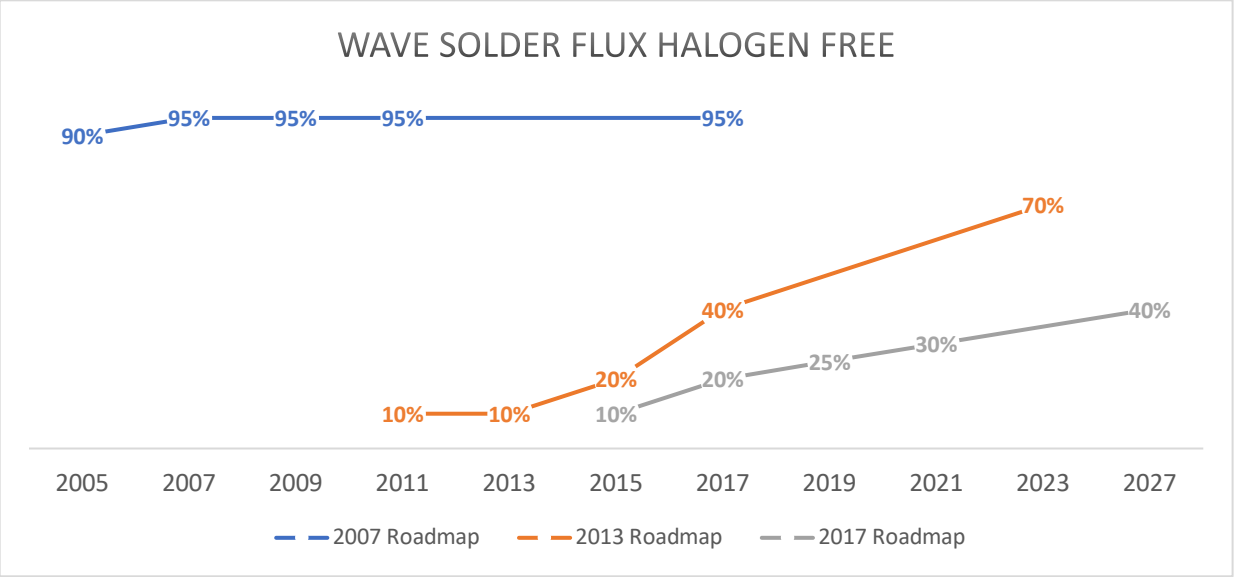
Figure 26 shows the evolution of predictions of VOC-free wave solder flux from 2007 to 2017. It appears that the 2007 Roadmap grossly overestimated the adoption of VOC-free flux, but the 2013 and 2017 roadmaps have comparable predictions.

Figure 26



Like VOC-free flux, it appears that the roadmaps overestimated the adoption of halogen-free flux (see *Figure 27*). Because the 2013 Roadmap still differs drastically from the 2017 Roadmap, it would be worth investigating the likelihood of legislation or environmental issues that could affect this adoption.

Figure 27



7. DIE ATTACH ADHESIVES

Die attach adhesives are used to connect semiconductor chips to packaging substrates as well as control warpage and help mitigate stress during operation. Die attach adhesives are discussed in more depth in the 2007, 2013 and 2017 Roadmaps. However, there is identical language in all three roadmaps: "Polymer based die attach, either paste or pre-applied, capable of meeting the parallel technology challenges of Flip Chip underfills (for heat and moisture resistance) and polymer technology to withstand the higher lead-free reflow temperatures, will be needed."

The 2013 and 2017 roadmaps highlight three key drivers: 1) lead-free, 2) increased power density and the resulting need for thermal management and 3) use of stress sensitive low K silicon. Figures 28, 29 and 30 show die attach adhesives percentages that fit into polymer pre-applied, polymer paste and low K silicon, respectively. All three of these seem to be predicted accurately, however, it appears that the change over time is very minimal.

Figure 28

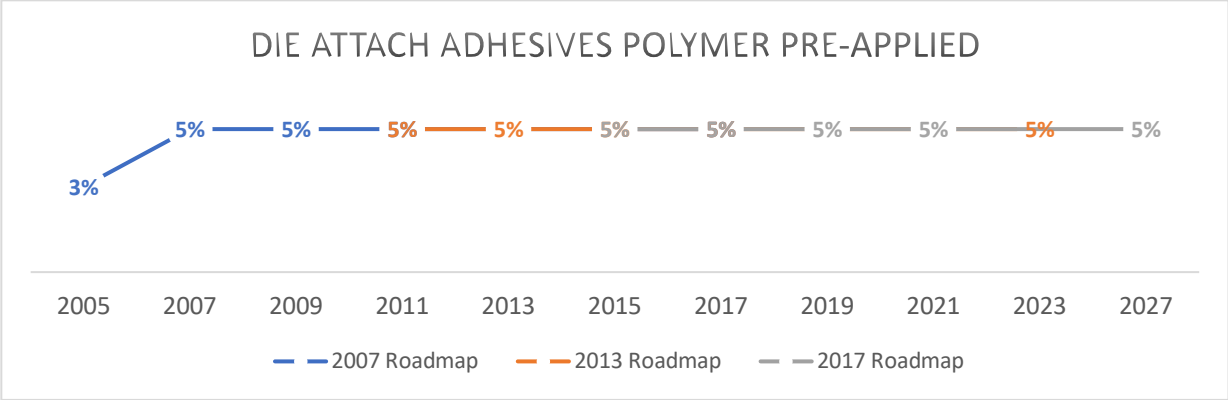


Figure 29

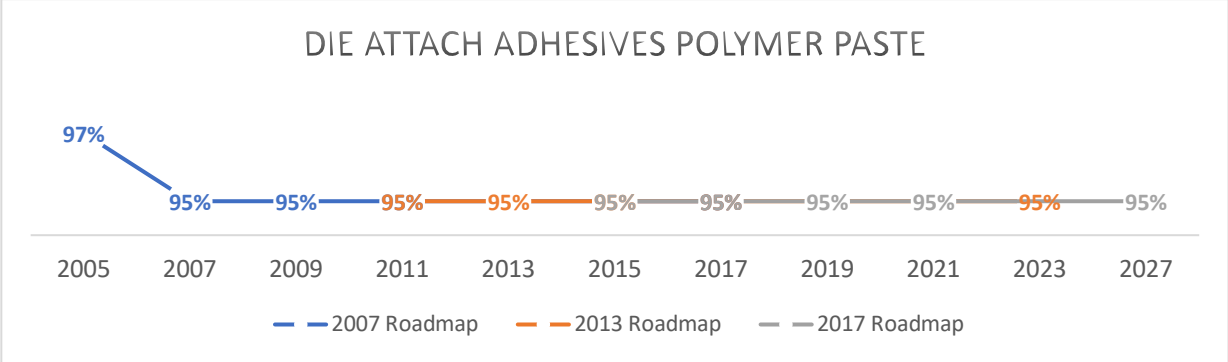
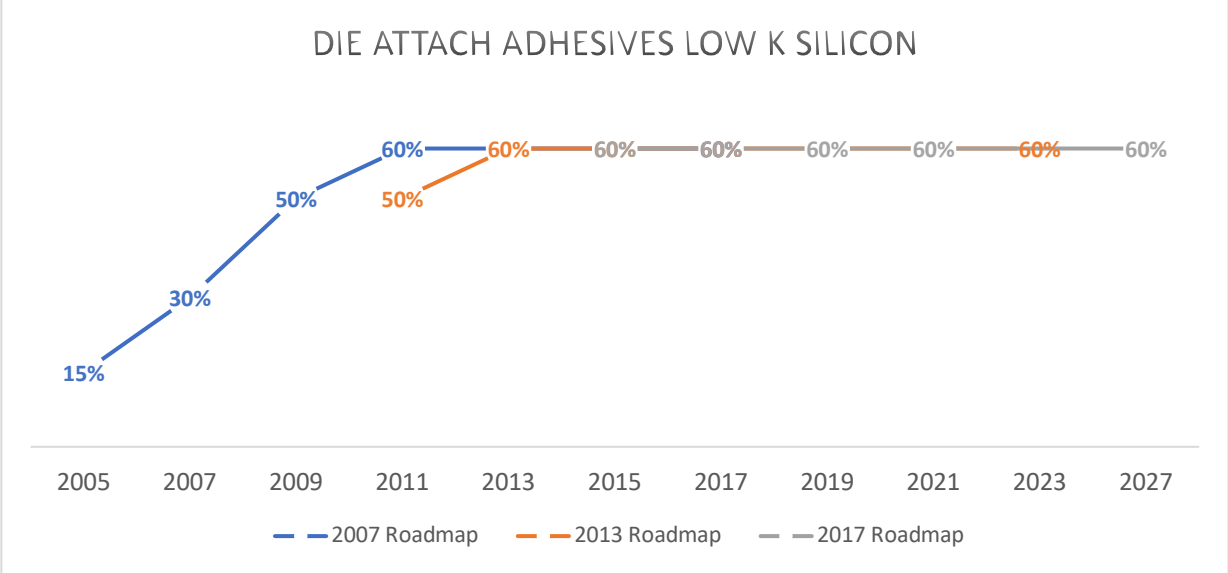


Figure 30



CONCLUSION

iNEMI has made many projections over the last century, a majority of them very accurate. With all the advancements in new legislation, many would expect otherwise. Conversion costs and NPI cycle time were all estimated very accurately, even 15 years out in 1995. The area with the most discrepancies was in component trends, where the 1994 and 2002 roadmaps largely overestimated component density capabilities.

While this project makes conclusions about the evolution of predictions since 1994, it should be noted that many of the metrics were complex to compare. The roadmaps contrast greatly in their general outline and what metrics are used. Some roadmaps discuss metrics qualitatively and some roadmaps discuss metrics quantitatively.

This project aimed to bridge these discrepancies into a comprehensive reflection on the roadmap predictions versus actual technological outcomes.

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