6-2012

# Bridgeless Step/Up Unity Power Factor Rectifier for High Voltage Applications

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جامعة الإمارات العربية المتحدة
United Arab Emirates University

UAEU Faculty of Engineering

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M.Sc. Program in Electrical Engineering

# Bridgeless Step/Up Unity Power Factor Rectifier for High Voltage Applications

By

Aysha Kemadish AL-Kaabi

*A thesis submitted to*
**United Arab Emirates University**
*In partial fulfillment of the requirements*
*For the Degree of M.Sc. in*
**Electrical Engineering**

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# Thesis Title

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DEPARTMENT OF ELECTRICAL ENGINEERING
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June, 2012

# ABSTRACT

Power electronic devices with front- end rectifier are widely used in computer, communication and electric vehicle industries. These rectifiers are nonlinear in nature and generate current harmonics which pollute utility power. International harmonic standards (e.g., IEC 61000-3-2 and EN 61000-3-2) have been put in place to confine power pollution. These standards limit the current harmonics generated by loads to a specified threshold depending on load power and application. In other words, a high power factor is required.

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet the harmonic regulations and standards. However, classical PFC schemes have lower efficiency due to significant losses in the diode bridge. Several bridgeless topologies have been introduced to decrease diode bridge conduction losses. Most of the step-up PFC rectifiers utilize boost converter at their front end due to its natural PFC capability.

In this thesis, a new bridgeless PFC topology based on Cuk converter is presented. Similar to Cuk converter, the proposed topology offers several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, and lower electromagnetic interference (EMI). These advantages make the proposed topology a viable solution for high voltage DC loads such as electric vehicle battery charger.

Chapter III presents steady state analysis for the proposed rectifier. The rectifier is analyzed only during the positive half of the line frequency due to symmetry. Design procedure, simulation and measurements to verify the capability of the rectifier are presented in Chapter IV. Harmonics content and efficiency of the proposed rectifier versus conventional Cuk full bridge PFC rectifier are also presented.

Keywords: Full Bridge Rectifier, Bridgeless Rectifier, Passive and Active Power Factor Correction (PFC), Boost Rectifier, Buck Boost Rectifier, SEPIC Rectifier, CCM, DCM and EMI.

# LIST OF PUBLICATION

1. Aysha Kemadish AL-Kaabi, Abbas A. Fardoun and Esam H. Ismail, Bridgeless Step/Up Unity Power Factor Rectifier for High Voltage applications, *The International Conference on Sustainable Systems and the Environment ISSE'11* , Sharjah, March 23-24, 2011.

2. Aysha Kemadish AL-Kaabi, Abbas A. Fardoun and Esam H. Ismail, Bridgeless Unity Power Factor Rectifier for High Voltage applications, *The International Conference on renewable energy: Applications and Generation ICREGA'12* , Al-Ain, March, 2012.

3. Aysha Kemadish AL-Kaabi, Abbas A. Fardoun and Esam H. Ismail, **Bridgeless High-Voltage Battery-charger PFC Rectifier**, *Submitted to Elsevier Journal on Renewable Energy*.

# UNDERTAKING

I certify that research work titled "*Bridgeless Step/Up Unity Power Factor Rectifier for High Voltage Applications*" is my own work. The work has not been presented elsewhere for assessment. Where material has been used from other sources it has been properly acknowledged / referred.

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# ACKNOWLEDGEMENTS

First of all, I thank Allah who inspired me with health, power and patience to accomplish my thesis.

I would also like to express my deepest appreciation to my advisor, Dr. Abbas Fardoun, for his scientific guidance, wise counsel and sustained encouragement. I am grateful for his support, belief, patience, fairness and constructive feedback. Also, I want to express my sincere gratitude and admiration for Dr. Essam H. Ismail for his support and valuable feedback.

My special thanks go to all lab assistant engineers, whose support enabled me to reach my goal, particularly Eng. Ahmed and Eng. Adel.

Last but not least, my deepest gratitude and greatest admiration go to my friends and lovely family, including my parents, my children, my brothers and sisters, and all my relatives who have always motivated and encouraged me to reach my goal. I sincerely appreciate my special friend Elizabeth for her assistance. I especially want to express my gratitude for the invaluable support of my husband.

The financial support from the Emirates Foundation is deeply appreciated.

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# ABBREVIATIONS

**AC:** Alternating Current

**BJT**: Bipolar Junction Transistors

**CCM:** Continuous Conduction Mode

**DCM**: Discontinuous Conduction Mode

**CENELEC:** European Committee for Electro-technical Standardization

**DC:** Direct current

**IEC**: International Electro-technical Commission

**IGBT:** Insulated Gate Bipolar Transistor

**LC:** Inductive-Capacitive

**MOSFET:** Metal Oxide Semiconductor Field Effect Transistor

**PFC:** Power Factor Correction

**SCRs**: Silicon-Controlled Rectifiers

**RMS**: Root Mean Square

**THD**: Total Harmonics Distortion

**PFP**: Power Factor Pre-regulator

**CM**: Common Mode

# NOMENCLATURE

| | |
|---|---|
| $C_o$ | Output capacitance |
| $D_1$ | Duty cycle of the switch in position 1 |
| $D_2$ | Duty cycle of the switch in position 2 |
| $D_o$ | Output diode |
| $f_L$ | Line frequency |
| $f_r$ | Resonant frequency |
| $f_s$ | Switching frequency |
| $i_c$ | Capacitor current |
| $<i_C(t)>_{Ts}$ | Capacitor charge balance |
| $I_{D.Bridge\_rms}$ | Diode bridge rms current |
| $\Delta I_{in}$ | Input current ripple |
| $i_{in}$ | Rectified input current |
| $i_L$, $I_L$ | Inductance current, peak of the inductance current |
| $l_o$ | Output current |
| $i_Q$ | Switch current |
| $I_{Q.pk}$ | Switch current peak |
| $K$ | Conduction parameter (unit-less) |
| $K_{crit}$ | Critical Conduction Parameter |
| $K$ | Kilo |
| $L_{eq}$ | Equivalent inductance |
| $m$ | Milli |

| | |
|---|---|
| $M$ | Voltage conversion ratio |
| $P_{bridge}$ | Power dissipation in the bridge rectifier |
| $P_{out}$ | Output power |
| $P_{in}$ | Input power |
| $R$ | Resistive load |
| $R_e$ | Emulated input resistance |
| $T_L$ | Line voltage cycle |
| $T_{on}$ | On time duration of the switch |
| $T_{off}$ | Off time duration of the switch |
| $T_s$ | Switching time cycle |
| $v_{ac}$ | Rectified line voltage |
| $V_f$ | Forward voltage |
| $<V_L(t)>_{Ts}$ | Inductor volt-second balance |
| $V_m$ | Peak amplitude of the rectified line voltage |
| $V_o$ | Output voltage |
| $\Delta V_o$ | Output voltage ripple |
| $V_{rms}$ | RMS value of the rectified line voltage |
| $\mu$ | Micro |
| $\omega$ | Line angular frequency |

# CHAPTER 1

## Introduction

The dramatic growth of electronic equipment usage in recent years has resulted in a greater need to ensure that the line current harmonic content of any equipment connected to the AC mains meets regulatory standards .Nowadays, most electronic equipment, including laptops, televisions and cellular phones (nonlinear load), need a rectifier circuit, which produces a non-sinusoidal line current. As illustrated in Fig.1.1 these nonlinear load currents have a lot of harmonics that pollute the AC line voltage by distorting the sinusoidal input voltage. Consequently, thermal stress of the equipment would increase due to greater losses caused by non-sinusoidal waveform. Therefore, the system efficiency and power factor are reduced, and the harmonic content in the AC line current is increased, which has adverse effects like the heating of transformer and induction motors, their life span reduction, the degradation of system voltage wave-form, and the malfunctioning of certain power system protection elements [1-3].

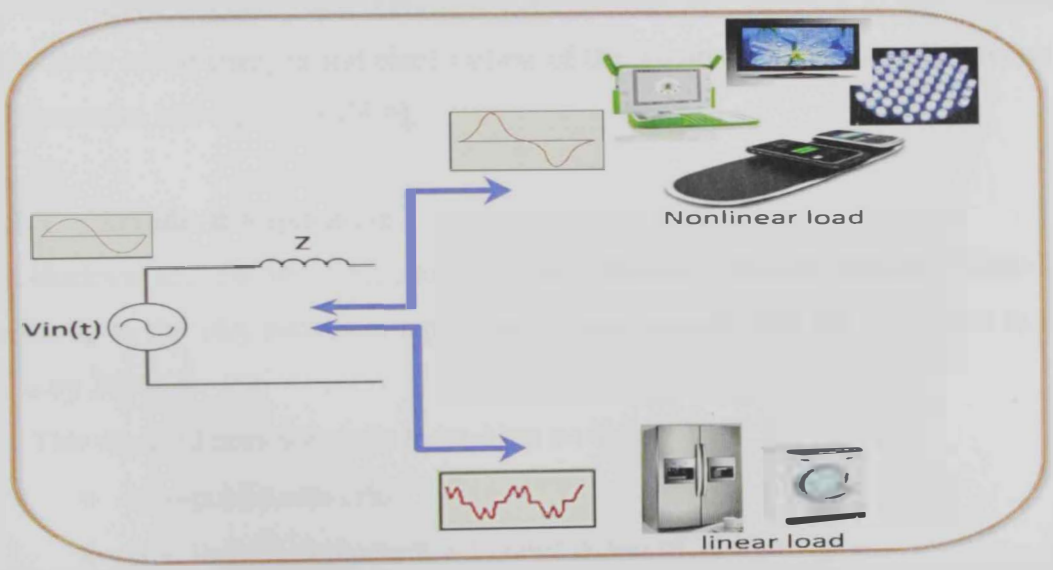



Fig.1.1: The effect of a nonlinear load on the AC line voltage.

To address the above problem a lot of attention is paid to harmonics generated by rectifiers due to the wide spread use of electronic equipment that use front end rectifiers. Therefore, the need for a high efficient, high power factor and low harmonic rectifier is required to minimize harmonic levels. Standards have been put in place to limit input current harmonics. High quality rectifiers should comply with the harmonics' international standard limit for power equipment. Power equipment would include industrial motor drives, electrical vehicle battery chargers, electronic ballasts' fluorescent lamps, and office equipment power supplies.

## 1.1 Harmonic Standard Transitional Periods

The EN 50006 was established in 1975 as the first harmonic standard by the European Committee for Electro-technical Standardization (CENELEC). Due to the decadence of its power quality the EN 50006 was adopted by fourteen European countries. In 1982 the International Electro-technical Commission (IEC) dictated IEC 555-2 as a European standard. Then in1991 CENELEC approved IEC 555-2 to set the levels for harmonic currents injected by loads back on to the network. In April of 1995, the IEC 555-2 was replaced by IEC 1000-3-2 after its revision. The IEC 1000-3-2 has since been adopted as the EN 61000-3-2 European Standard, which defines the practical rules and provides a clearer definition of equipment classes. All older versions have expired since February 2009 besides EN 61000-3-2: 2006, which introduces minor changes and clarifications of the requirements for the measurement of harmonics and their limits[4-6].

### 1.1.1 Standard Application

All electrical and electronic equipment that is connected to the low-voltage AC public mains up to the 16A maximum input current must comply with EN 61000-3-2 as of January 2001.

This standard does not apply to (and has no limits for):

- Non-public networks
- Non lighting equipment with rated power of 75W or less

- Equipment for rated voltages less than 230VAC (limit not yet been considered)
- Arc welding equipment intended for professional use
- Professional equipment (not intended for sale to the general public) with rated power greater than 1 kW
- Heating elements with symmetrical control methods and input power less than or equal to 200W
- Independent dimmer for incandescent lamps with rated power less than or equal to 1 kW. [6]

### 1.1.2 Classification and Limits

There are four different classes in the EN 61000-3-2, which have different limit values:

Table 1.1: Harmonic classes with their respected applications [6].

| Class | application |
|---|---|
| A | • 3-phase balanced equipment,<br>• Household appliances except class D equipment,<br>• Tools except portable tools,<br>• Incandescent lamps dimmers,<br>• Audio equipment,<br>• All other equipment except that stated in class A, B, C or D. |
| B | • Portable tools,<br>• Arc welding equipment. |
| C | • Lighting equipment. |
| D | • PC,<br>• PC monitors,<br>• Radio, |

| | |
|---|---|
| | • TV receivers,<br>• Electrical vehicles battery charger,<br>• Equipment with input power P≤600W. |

The limits for class D equipment are shown in Table 1.3 as a power related current (mA/W) with a maximum permissible value given in Table 1.2.

Table 1.2: Limits for class A equipment [6].

| Harmonic order<br>n | Maximum permissible<br>Harmonic current<br>A |
|---|---|
| Odd harmonics | |
| 3 | 2.30 |
| 5 | 1.14 |
| 7 | 0.77 |
| 9 | 0.40 |
| 11 | 0.33 |
| 13 | 0.21 |
| $15 \leq n \leq 39$ | $0.15.\frac{15}{n}$ |
| Even harmonics | |
| 2 | 1.08 |
| 4 | 0.43 |
| 6 | 0.30 |
| $18 \leq n \leq 40$ | $0.23.\frac{8}{n}$ |

Table 1.3: Limits for class D equipment [6].

| Harmonic order<br><br>N | Maximum permissible harmonic current per watt<br>mA/W | Maximum permissible harmonic current<br>A |
|---|---|---|
| 3 | 3.4 | 2.30 |
| 5 | 1.9 | 1.14 |
| 7 | 1.0 | 0.77 |
| 9 | 0.5 | 0.40 |
| 11 | 0.35 | 0.33 |
| $18 \leq n \leq 40$ | $\frac{3.85}{n}$ | As in Class A |

Among the class D equipment is the electrical vehicles' battery charger, which like other nonlinear equipment, suffers from high harmonics. In order to reduce the harmonics and meet the class D limits, the power factor must be improved. The definition of the power factor and some related facts are explained below. Furthermore, the techniques used to improve the power factor and simultaneously reduce the line current harmonics are discussed in general.

## 1.2 Power Factor Correction

The power factor is defined as the ratio of the real power measured in watts to the apparent power, which is the product of the RMS voltage multiplied by the RMS current as shown in the following relation, [1]

$$powerfactor = \frac{(averagepower)}{(rmsvoltage)(rmscurrent)} (1.1)$$

Ideally, with a linear resistive load, the power factor is unity regardless of the harmonic content of the fundamental voltage. On the other hand, the nonlinear loads draw more RMS current from the source because of their harmonic content, which increases the losses. However, historically it has been defined in terms of a phase-

shift between the voltage and current waveforms, where $I_1$ is the peak of the fundamental current and the denominator is the total RMS value of the current:

$$PF = \frac{P}{S} = \left( \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) \left( cos(\varphi_1 - \theta_1) \right) \quad n = 3, 5, 7 \ldots . \quad (1.2)$$

Furthermore, the difference in phases between the fundamental components of the line voltage and line current is described by $(\varphi_1 - \theta_1)$, assuming that the line voltage is not distorted. As the losses increase, the reactive power increases and the power factor decreases, which increases the total harmonic distortion. The Total Harmonics Distortion (THD) measures the ratio of the total RMS value of the harmonic currents to the RMS value of the line frequency component.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \qquad n = 3, 5, 7 \ldots . \qquad (1.3)$$

The reactive power can be reduced by adding a filter to compensate for the low power factor. In the past a capacitor bank was used, but it cannot work with systems that have high harmonic content because the overheating increases stress that result in premature failure. Two methods can be used to improve the power factor in non-linear loads: passive or active filtering [1].

### 1.2.1 Harmonics Line Current Reduction Techniques

Different techniques can be used to improve the power factor and to conform to the international line harmonics' regulations. The most commonly used techniques are passive and active approach.

#### 1.2.1.1 Passive PFC

Passive Power Factor Correction (PFC) is an expression used for harmonic line current reduction using passive components. It is considered to be a simple way to control the harmonic current where only passive components (inductor and capacitor)

filtering is used. This filter reduces the harmonic current, which means that the non-linear device becomes more linear. Fig. 1.2a shows the input rectifier current without a filter where the input current is only limited by the small input impedance. Fig.1.2b shows that passive technique introduces high impedance for the harmonic, thus smoothing the input current for the electronic equipments. The input current with passive harmonic line current reduction shows a greater reduction in the input current and its harmonic content than the input current without harmonic line current reduction.

The disadvantages of this approach include high current and voltage stresses, high cost and bulky when using large-value, high-current inductors and capacitors. Furthermore, the input current still contains harmonics. [5-8]

#### 1.2.1.2 Active PFC

An active Power Factor Correction (PFC) is a power electronic system that controls the amount of power drawn by a load in order to obtain a power factor as close as possible to unity by using active switching. Bipolar junction transistors (BJT), silicon-controlled rectifiers (SCRs), and Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) are examples of active devices. The active PFC controls the input current of the load such that the current waveform is proportional to the voltage waveform. In order to make the load appear purely resistive, meaning the apparent power equals the real power; the power factor must be as close to unity as possible. In other words, the voltage and current are in phase, and the reactive power consumption is zero as shown in Fig.1.2c. By comparing the three figures (1.2a, 1.2b and 1.2c), active PFC circuitry gives the best performance [6]. In addition, the active power factor correction (PFC) has several advantages. Active switching makes the load behave like a pure resistor or unity power factor, which means it reduces the harmonics in the input line current. The dominant loss in the active approach is the conduction losses of the bridge rectifier. Some types of active PFC include Boost, Buck, Buck-Boost, Single-Ended Primary Inductance Converter (SEPIC), and Cuk. It should be noted that the active power factor correctors can be single-stage or multi-stage [5-11].

Ultimately, the aim of PFC is to shape the input phase currents so that they are in phase with the input phase voltages.

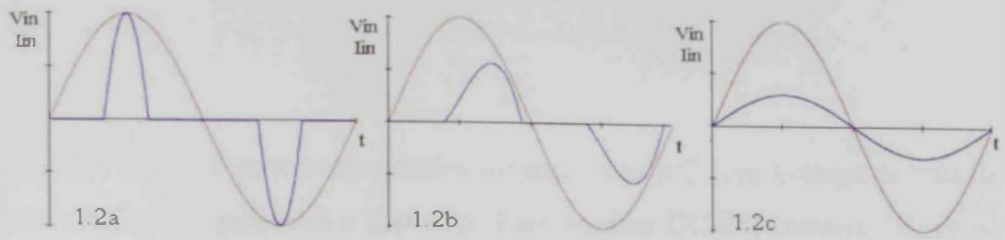



Fig.1.2: PFC effect on the input current: (a)Input current rectifier without filtering, (b)Effect of the passive PFC on the input current rectifier,(c) Effect of the active PFC technique on the input current.

**Aim of this Thesis:**

The main goal of this thesis is to design a step-up high efficiency AC-DC rectifier (high voltage battery charger) with isolation capability for low power application, e.g., Electrical Vehicle. The rectifier is designed to meet EN 61000-3-2requirements. The new rectifier is based on conventional Cuk topology with higher efficiency, a low starting current and low EMI due to it is bridgeless configuration.

This work is intended for high voltage (250-300V) electric cart. The battery will be charged from AC line. The line harmonic must meet EN 61000-3-2. Also this application requires low EMI emission. Typically, a switch is added in between the load and the AC line for safety reasons. Low inherent in-rush current is desired to minimize the switch size.

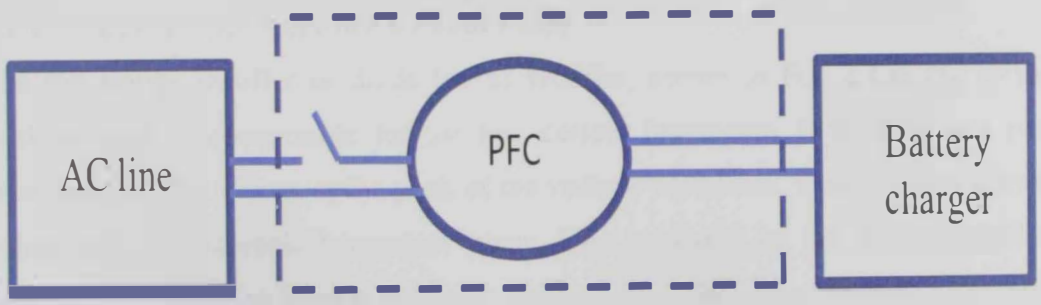



Fig. 1.3: Schematic draw for the battery charger.

# CHAPTER 2

# Literature Review

Generally, in most power electronics systems, the AC line voltage is rectified to convert AC to DC power as a first step. Then another DC-DC converter stage is used to regulate the output voltage in order to meet the load requirements. The major problem with a power rectifier is harmonic pollution. Therefore, PFC converters are used for AC-DC rectifiers to satisfy the International Harmonic Standards, which require the harmonic content of the line current to stay below certain limits, as explained in chapter 1. In this chapter different types of rectifiers are discussed [5-11]. Above, the active PFC and passive PFC are introduced as methods used to improve the power factor, but because of their respective features, they can only improve the power factor with some drawbacks.

## 2.1 AC- DC Passive Rectifier

The passive PFC can achieve a high power factor without losses but places stress on the semiconductor components. Additionally, the volume of the rectification circuitry is greater so the system cost increases [5-8]. Next, the full bridge rectifier without and with a filter are introduced.

### 2.1.1 Full Bridge Rectifier without Filter

The full bridge rectifier or diode bridge rectifier, shown in Fig. 2.1,is the earliest rectifier used to compensate for the line current harmonics. It is used as a peak detection rectifier where, at the peak of the voltage waveform, short duration current pulses with considerable harmonics occur. This is caused by the short conduction interval of the rectifier diodes, as shown in Fig. 2.2(a).The output capacitor value has a considerable effect on the line current harmonics, as displayed in Fig. 2.3(a), which verifies that by reducing the capacity of the capacitor, the harmonic content in the line

current can be reduced without adding additional components. However, the output voltage ripple is increased as shown in Fig. 2.3(b), compared with the output voltage ripple in Fig. 2.2(a), where the diode conduction interval is wider than the Fig. 2.3(b).

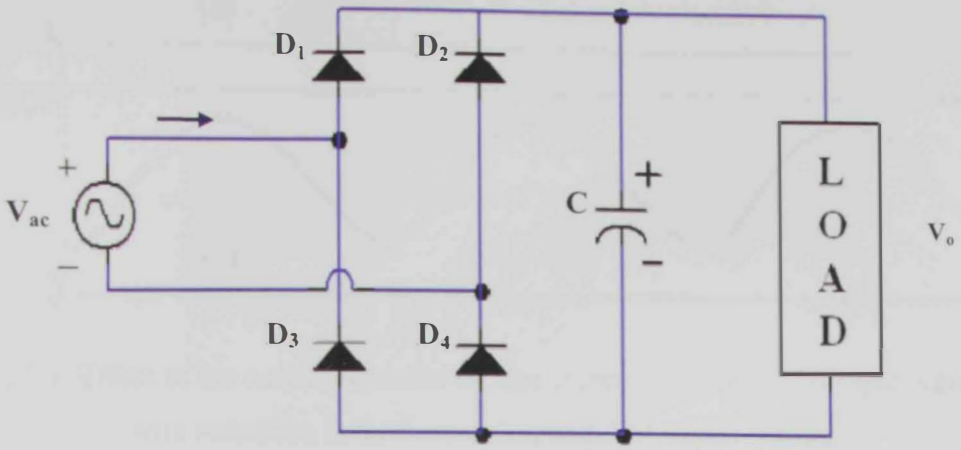



Fig.2.1: Full bridge rectifier.

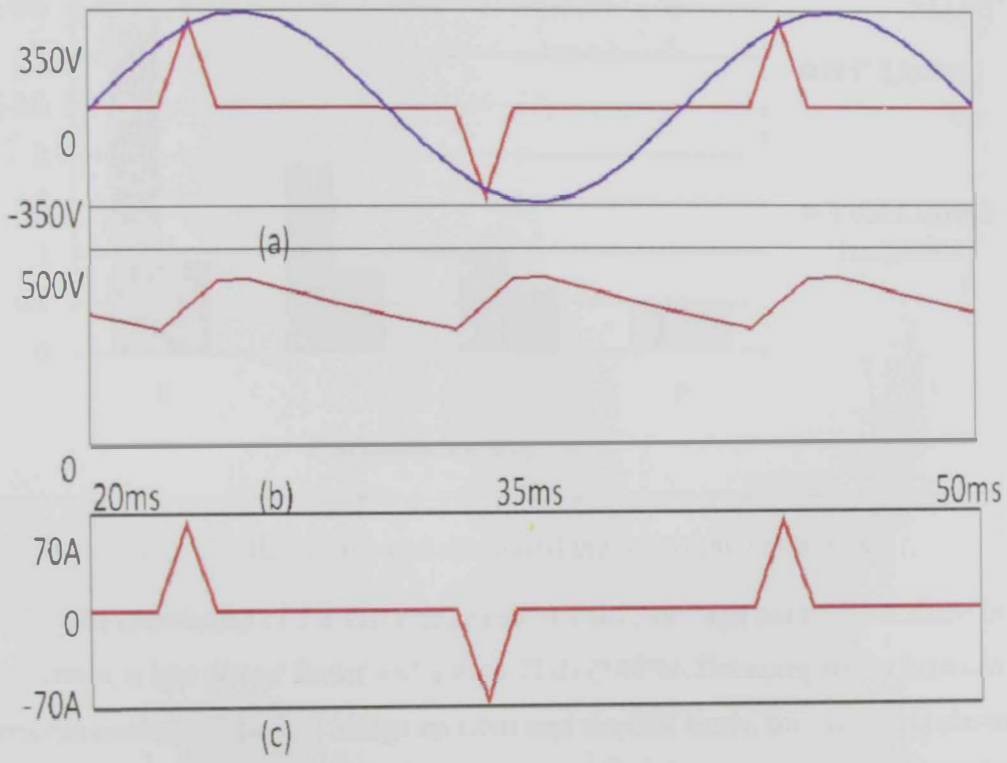



Fig.2.2: Full bridge rectifier simulation results:(a) Input voltage and input current, (b) The output voltage,(c) Zoomed area of input current.

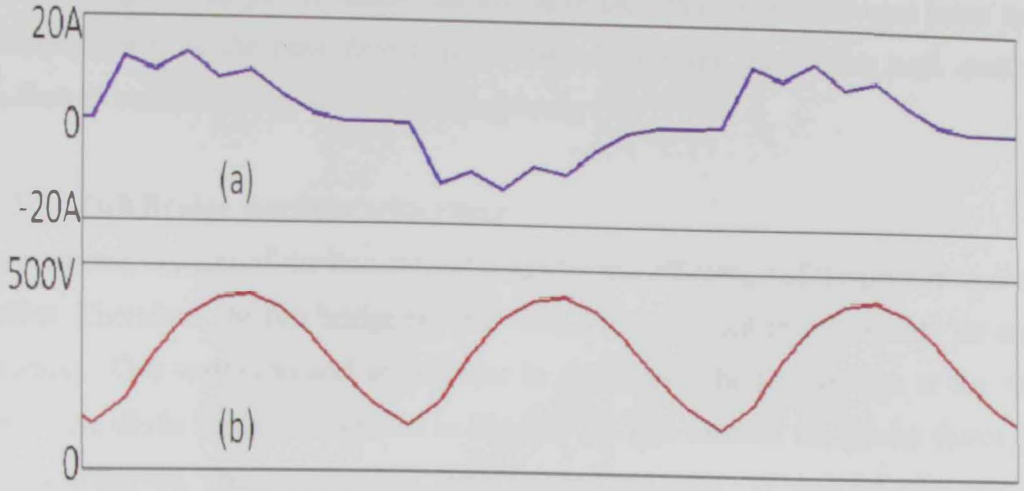



Fig.2.3: Effect of the output capacitor on line current harmonics: (a) Input current with reduction in the harmonics, and (b) Output voltage.

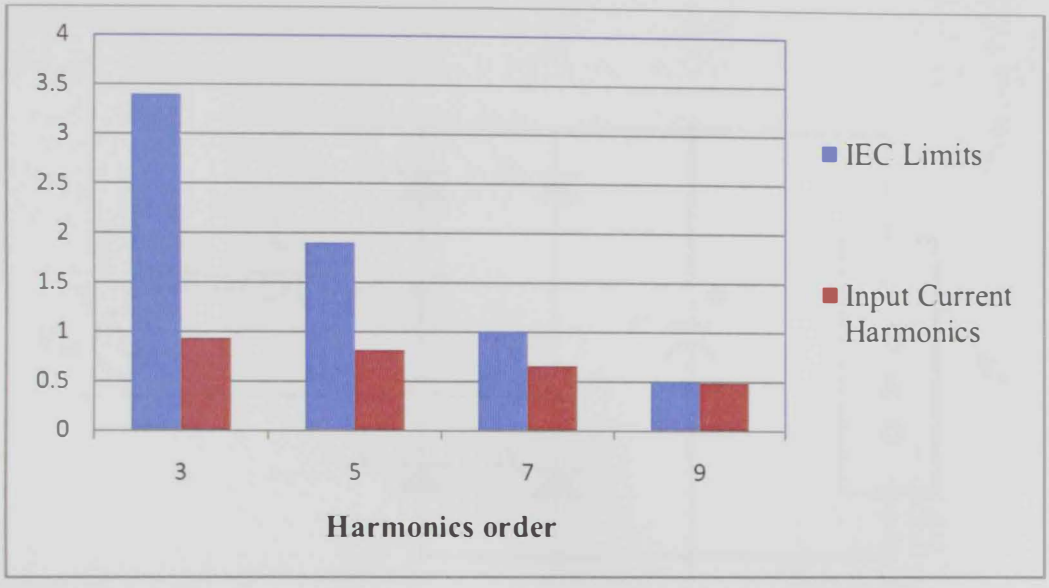



Fig 2.4: IEC limits and simulated input current harmonics.

The drawbacks of the full bridge rectifier include high harmonic content in the line current, a low power factor and a high THD (149%).The comparison between the harmonic content of the full bridge rectifier and the IEC limits for class D is shown in Fig. 2.4. As a consequence of the full bridge rectifiers' low efficiency, the user should install high voltage device, which are both bulky and costly. However, with a rectifier

nearly having a unity power factor, the available DC load power is almost twice the available power of the peak detection rectifier. Nowadays, employing high quality rectifiers in commercial systems has high priority [1].

### 2.1.2 Full Bridge Rectifier with Filter

The harmonic content of the line current degrades the efficiency of the peak detection rectifier. Therefore, the full bridge rectifier with a filter is used to compensate for any distortion. One way is to add an inductor in series with the line voltage at the AC side of the diode bridge, as shown in Fig.2.5. By this method the power factor is slightly improved. The input current, input voltage and output voltage are each shown in Fig.2.6.The harmonics content in the line current is reduced, as shown in Fig.2.6 (b). The harmonic of the line current are slightly reduced, as shown in Fig.2.7, and the THD is 51.7 %. However, the DC output voltage suffers from the ripple, which decreases the rectifier efficiency [1].

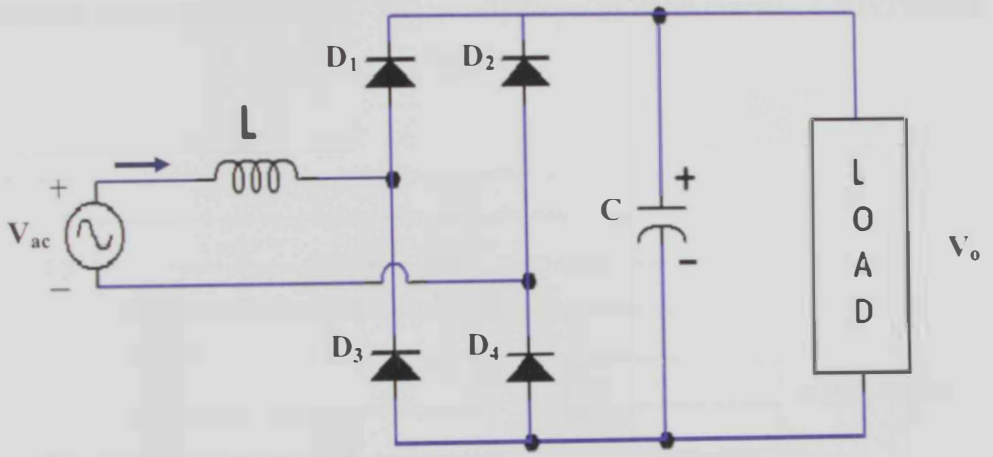



Fig.2.5: Diode bridge rectifier with AC-side inductor.

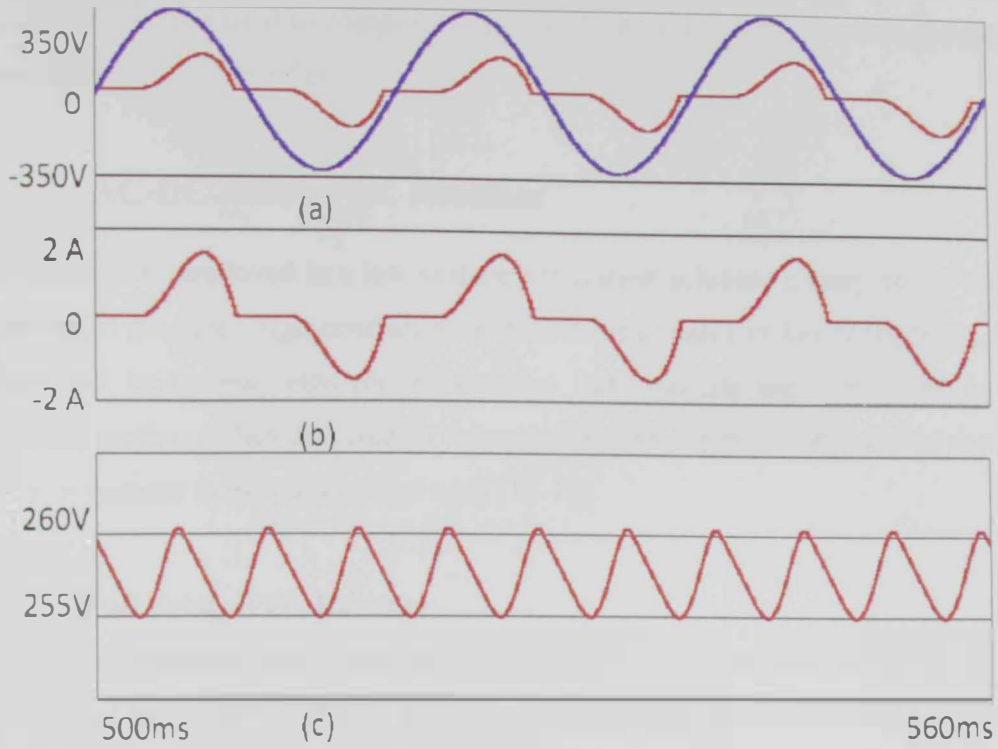



Fig.2.6: Diode bridge rectifier with AC-side inductor simulation results: (a) Input voltage and input current, (b) The zoomed area of input current, and (c) Output voltage.

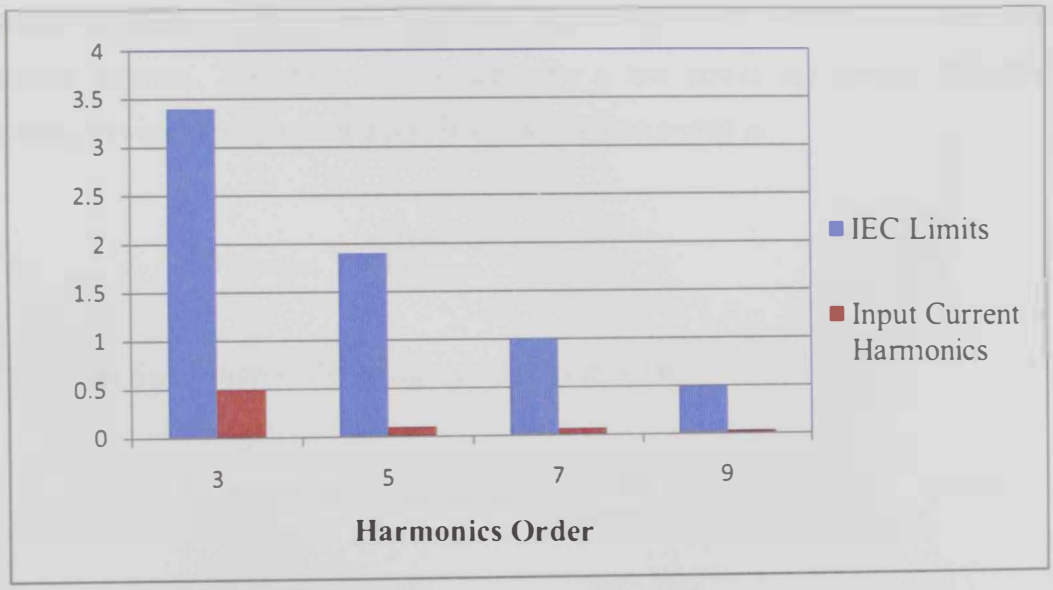



Fig.2.7: Simulated input current harmonics with respect to the IEC limits.

One of the methods used to compensate for the drawbacks of the passive approach is to use an active PFC rectifier.

## 2.2 AC-DC Active PFC Rectifier

The active PFC employed in a low voltage application achieves a unity power factor. However, it produces high conduction and switching losses in heavy loads [8]. The bridge and bridgeless rectifiers with active PFC circuits are introduced in the following sections. They are used to enhance the overall performance of the rectifier circuit in contrast to the passive approach [12-15].

### 2.2.1 Full Bridge PFC Rectifier

Full Bridge rectifiers have relatively low efficiency due to the number of silicon components in the current path of each stage [16-25]. One well known bridge rectifier is the conventional Cuk rectifier, where the current flows through three power semiconductor switches during each switching cycle. During the switch on-time, the current flows through two rectifier bridge diodes and the power switch, as shown in Fig. 2.8(b), while it flows through two rectifier bridge diodes and the output diode ($D_o$) during the switch off-time, as shown in Fig.2.8(c). The forward voltage drop across the bridge diode causes significant conduction losses, resulting in more severe thermal stresses. Therefore, it is suitable for a low power application. The RMS current flowing through each input diode during line period is

$$I_{D_{Bridge\_rms}} = \frac{P_{out}}{\sqrt{2}\eta V_{ac\_rms}} \tag{2.1}$$

The power dissipation in the bridge rectifier is given by

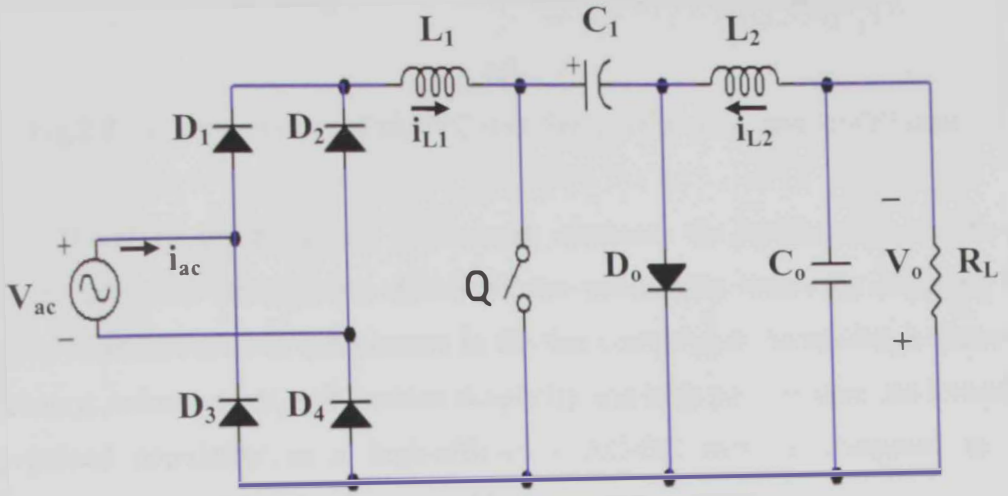
$$P_{bridge} = 4V_f I_{D\_Bridge\_rms} = \frac{4V_f P_{out}}{V_{ac\_rms}}, \tag{2.2}$$

where $V_f$ is the forward voltage.

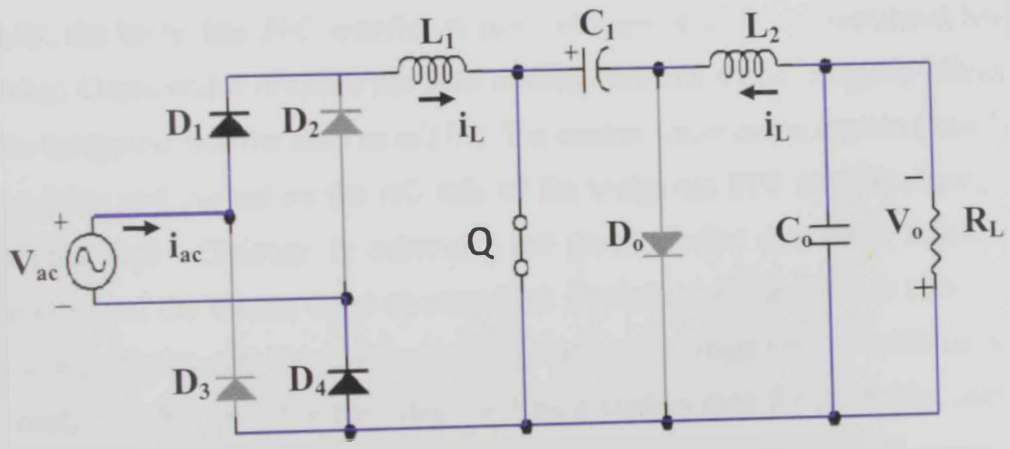
For example, if $V_f$ is 1V and $V_{ac}$ = 80 $V_{rms}$, then the power dissipation in the bridge rectifier is

$$P_{bridge} = 3.5\%P_{in} \tag{2.3}$$

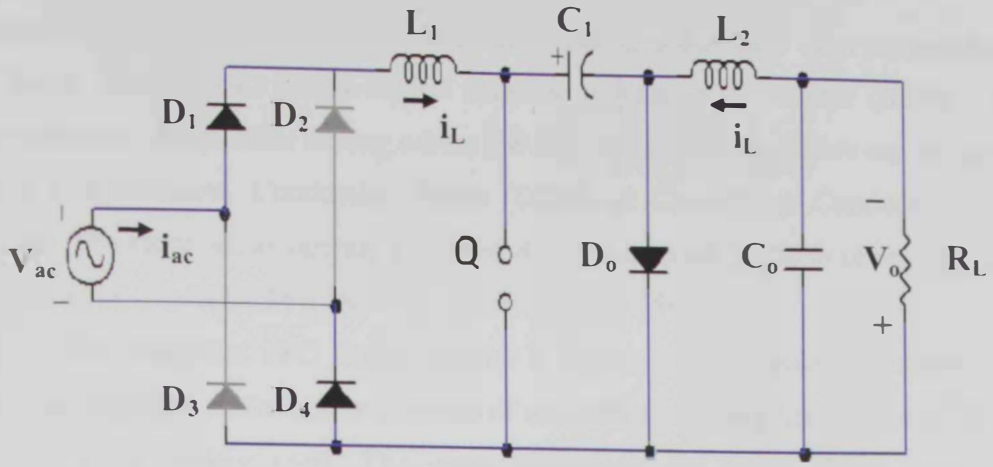
Eq. (2.3) shows that the power dissipation in the bridge rectifier consumes about 3.5% of the total input power.




(a)




(b)




(c)

Fig.2.8: (a) Conventional Cuk PFC rectifier: (b) On state, and (c) Off state.

Therefore, the bridgeless PFC circuit combines the rectifier circuit with the PFC circuit. This combination decreases the conduction losses by reducing the number of semiconductor components in the line current path. Moreover, it increases efficiency, reduces costs, and enables simplicity and high performance. As a result it has gained popularity as a high-efficiency AC-DC rectifier compared to the conventional PFC with either half or full bridge rectifier [26-35].

### 2.2.2 Bridgeless Rectifier

Ideally, the bridgeless PFC rectifier is more efficient than the conventional bridge rectifier. Considerable research has been directed towards maximizing the efficiency of the bridgeless rectifier such as in [32]. The control technique is used to sense both the voltage and current on the AC side of the bridgeless PFC rectifier. Using this technique high efficiency is achieved, the power factor correction function is improved and the circuit noise is controlled. Furthermore, the THD is reduced by eliminating the current harmonics caused by the input voltage [38]. In addition, since the bridgeless PFC rectifier has fewer switching devices than the full bridge rectifier in the current path, it results in lower conduction losses, higher efficiency and cost savings. However, bridgeless rectifier emits high common mode (CM) electromagnetic interference (EMI) noise due to the pulsating of the output voltage in

the ground [35]. There are several bridgeless topologies that have been proposed such as Boost, Buck-Boost, Single-Ended Primary Inductance Converter (SEPIC), and conventional Cuk rectifier among others [36-58]. All of these rectifiers can be used in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM). The rectifier can operate at a fixed duty cycle in the DCM to correct the input power factor, but in CCM it requires a control circuit [56].

The bridgeless PFC Boost rectifier is the dominant topology because of its low cost and high performance in terms of efficiency and simplicity [36-41]. That is why it is so widely used. The input current of the DCM Boost rectifier is discontinuous, which requires an extra passive filter to shape the input current toward a sinusoidal waveform. But in the case of SEPIC and Cuk rectifiers, the input current is continuous due to the existence of two inductors in each rectifier.

The DCM Boost rectifier has shown in Fig. 2.9 has a number of advantages, such as an inherent PFC function, simple controllability, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the major drawbacks of the bridgeless Boost rectifier include a higher DC output voltage than the peak input voltage, a difficult implementation of input-output isolation, a lack of current limitation during the overload conditions, high switching losses and a high start-up in-rush current. The high start-up in-rush current is considered a serious drawback in the Boost rectifier, which requires a huge switch as shown in Fig. 2.10. In addition, a more robust input filter is required to control the high peak ripple currents and voltages. This increases the overall weight and cost of the rectifier. On the other hand, the Cuk rectifier reduces the in-rush current. This is because the input inductor is connected to the energy transfer capacitor instead of directly to the output bulk capacitor as in the boost converter [40]. The in-rush current during start-up for the Cuk rectifier is shown in Fig. 2.11[55].

The bridgeless Boost rectifier with coupled inductor technique and two additional diodes as shown in Fig. 2.12 reduces the conduction losses. It also alleviates the reverse-recovery problem. Furthermore, it achieves zero–current turn-off of the output diode and the reverse-recovery currents of the additional diodes are slowed down to reduce the diode reverse-recovery losses [41].

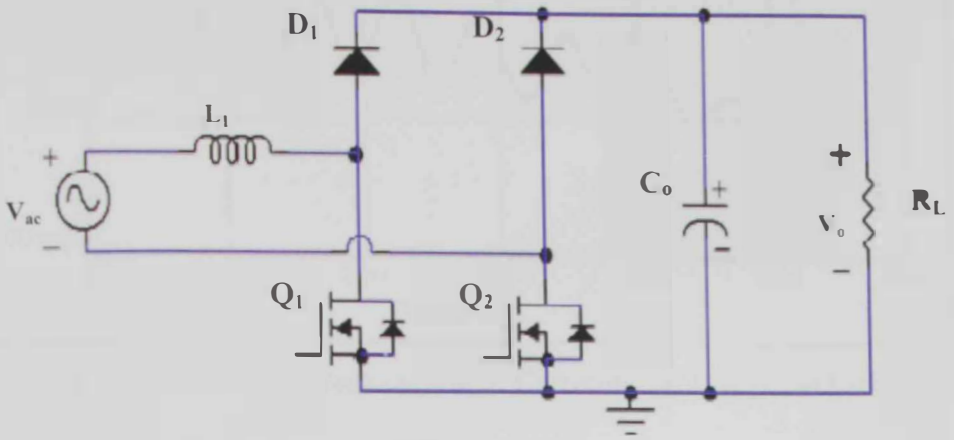



Fig.2.9: Conventional Bridgeless Boost rectifier.

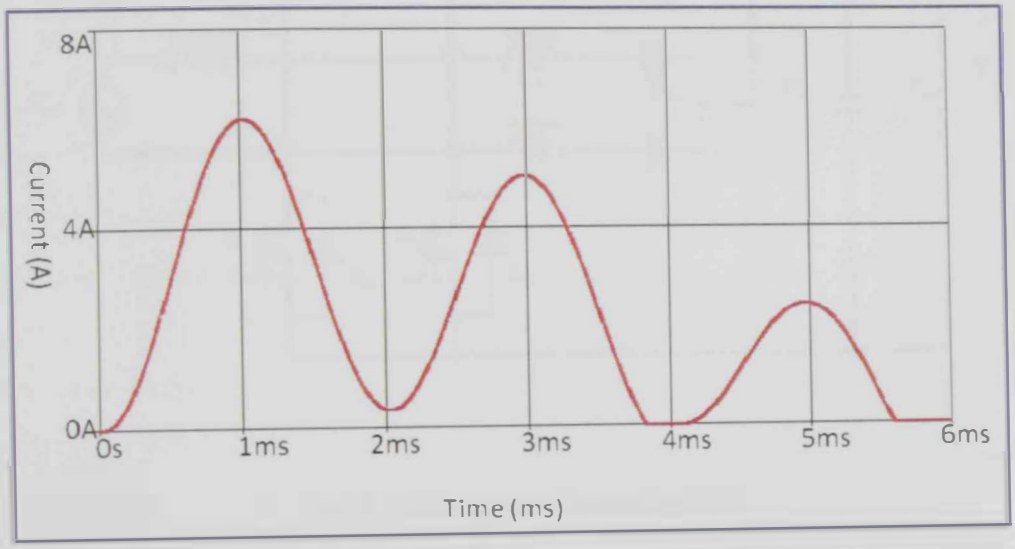



Fig. 2.10: Start-up in-rush current of Conventional Bridgeless Boost rectifier.

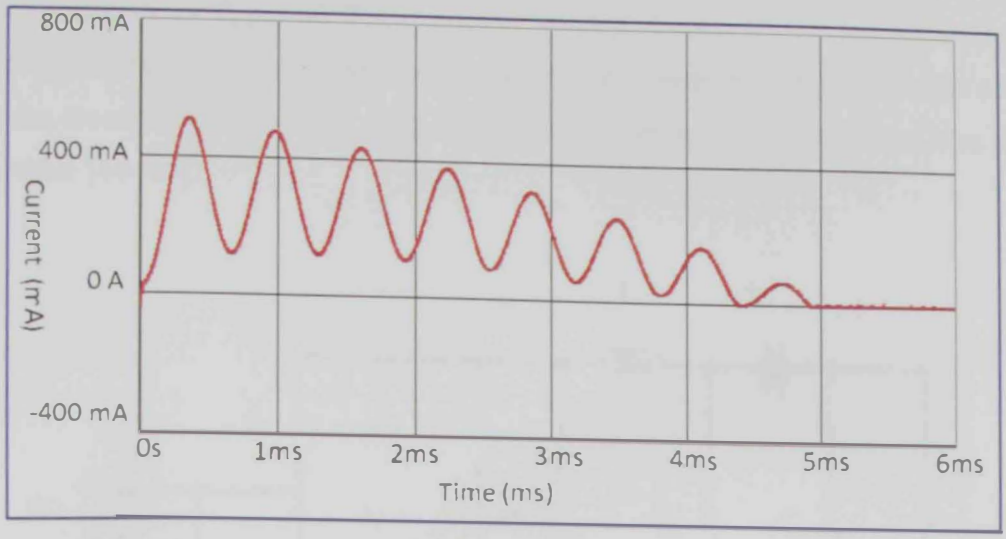



Fig. 2.11: Start-up in-rush current of Conventional Bridgeless Cuk rectifier.

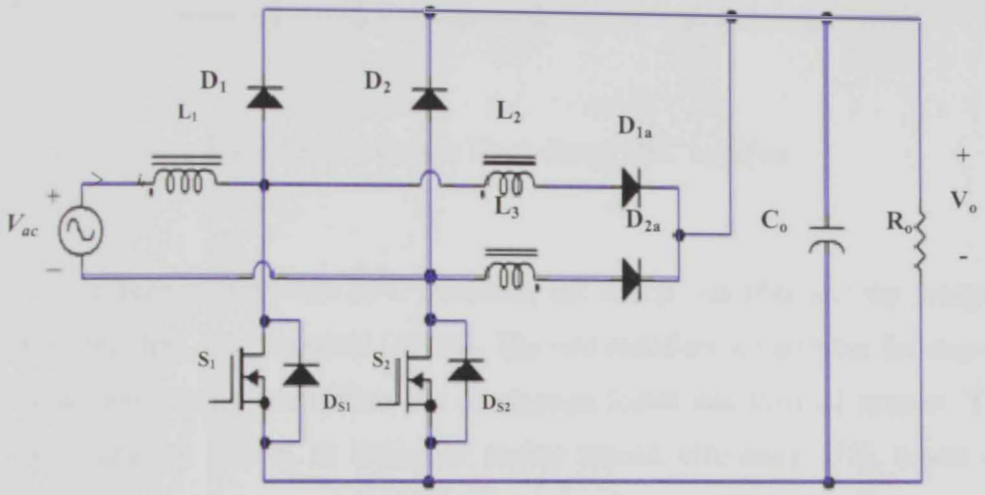



Fig. 2.12: Bridgeless Boost rectifier.

One of the possible solutions used to reduce the conduction losses is the bridgeless Buck-Boost PFC rectifier [42-43]. Bridgeless Buck-Boost PFC rectifier shown in Fig.2.13 improves the efficiency and is suitable for use in the wide input voltage range. Also, the conduction semiconductor components are reduced but still higher than the Cuk rectifier, where there are three switching devices in the current

path during every $T_s$ period. The maximum voltage stress is always lower than that of the Boost PFC rectifier. Furthermore, it avoids the in-rush current problem that occurs in the Boost PFC at start-up [43]. But it requires an isolated gate driver like Buck rectifier [44- 45].

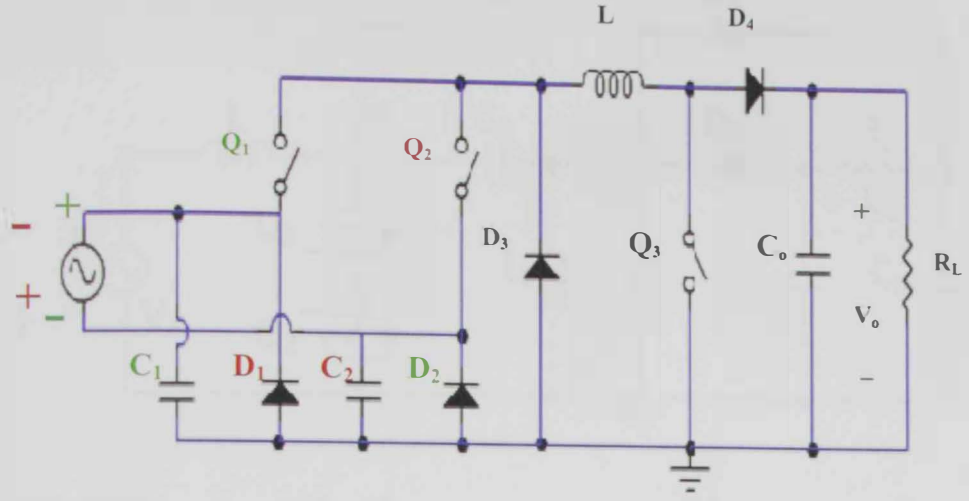



Fig.2.13: Bridgeless Buck-Boost PFC rectifier.

Two recent bridgeless PFC rectifiers, the SEPIC rectifier and the bridgeless PFC Cuk rectifier, are presented [46-58]. The two rectifiers are suitable for step–up / step--down application and reduce the conduction losses and thermal stresses. These improvements are shown in terms of higher circuit efficiency [52], lower cost, considerable size due to coupled inductors, and reduction in the power switch current stress. Furthermore, they offer several advantages unlike the Boost converter in the PFC applications. These advantages include easy implementation of transformer isolation, inherent in-rush current limitations during the startup and overload conditions, lower ripple on the input current and less electromagnetic interference (EMI). However, the SEPIC rectifier shown in Fig. 2.14 suffers from high output ripple because of the discontinuous output current similar to the Boost rectifier [35]. In addition, it requires an additional gate-drive transformer [8] and is intended for low voltage applications but the circuit in this paper is intended for high voltage

applications, so the Bridgeless Cuk step-up rectifier is used. It has a lower conduction loss than the conventional Cuk, which is shown in Fig. 2.8, due to the reduction of silicon switches in the current path. Also, the output current is continuous unlike the SEPIC rectifier due to replacing the diode ($D_1$) with an inductor ($L_{o1}$) [51-57].

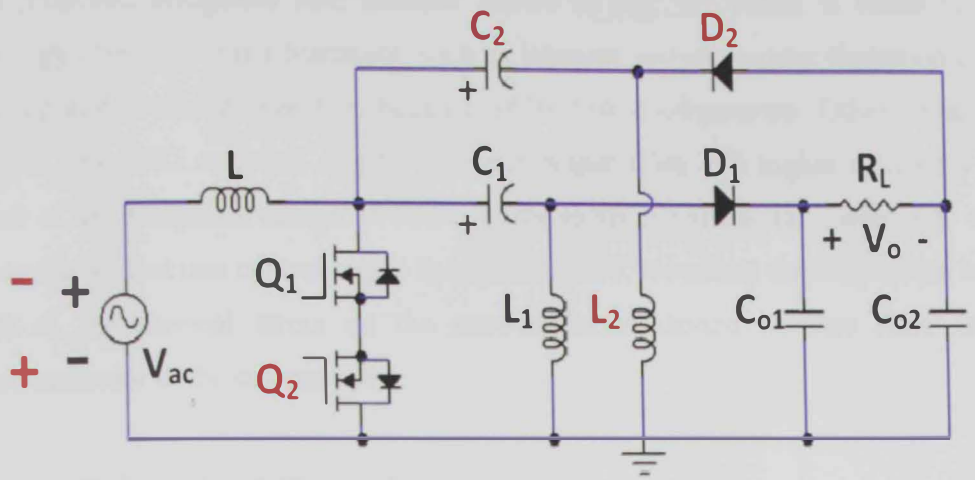



Fig.2.14: Bridgeless SEPIC rectifier.

# CHAPTER 3

# Modeling of Bridgeless DCM Cuk Rectifier

The proposed bridgeless PFC rectifier shown in Fig. 3.1 which is based on Cuk topology offers several advantages, such as inherent in-rush current limitation during start-up and overload condition because of its Cuk configuration. Other advantages include low EMI emission due to its input-output filter and higher efficiency as a result of the bridgeless design. In addition, the rectifier reduces the complexity of the controller so that one control signal is required. Also, it reduces the conduction loss as well as the thermal stress on the semiconductor device because there is one semiconductor in the current path.

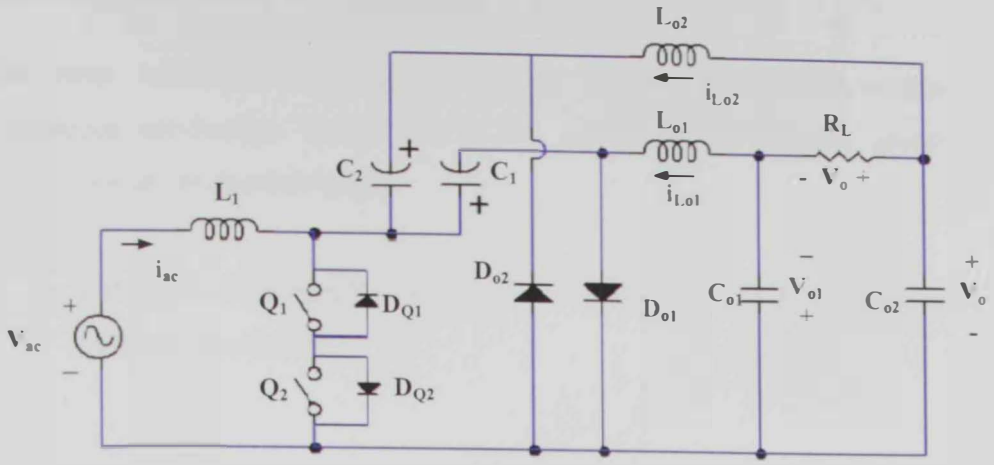
## 3.1 Principle of Operations

The DCM bridgeless PFC Cuk rectifier in Fig. 3.1(a) is formed by connecting two DC-DC Cuk converters, one for each half-line cycle of the input voltage. During the positive half-line cycle, the elements $L_1$, $Q_1$, $C_1$, $C_2$, $L_{o1}$, $L_{o2}$, $C_{o1}$, $C_{o2}$ and $D_{o1}$ are conducting as shown in Fig. 3.1(b). On the other hand, the current flows through $L_1$, $Q_2$, $C_1$, $C_2$, $L_{o1}$, $L_{o2}$, $C_{o1}$, $C_{o2}$ and $D_{o2}$ during the negative half-line cycle as shown in Fig.3.1(c). The capacitor voltages over the positive and negative cycle are shown in Fig.3.1 (b) & (c) and given by:

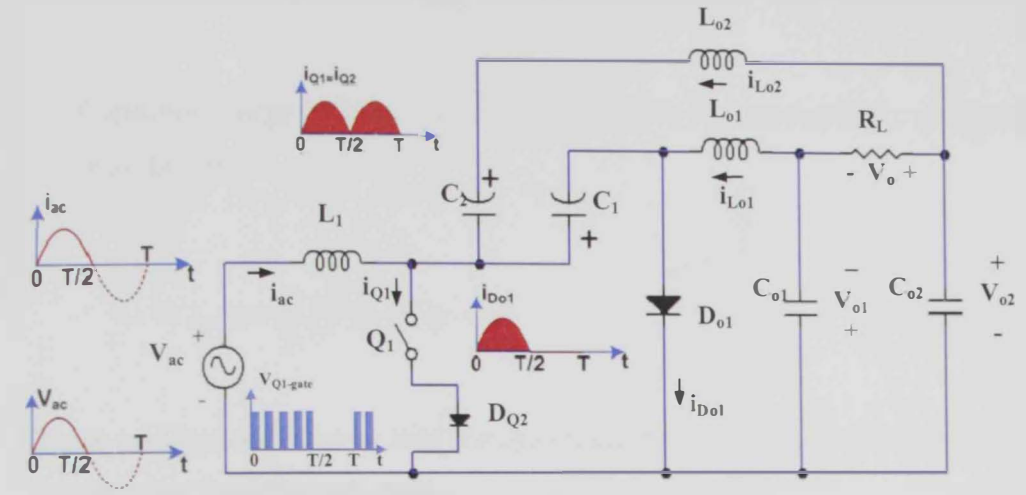
$$V_{C1}(t) = v_{ac} + V_{o1} \rightarrow (0 \le t \le T_L)$$
$$V_{C2}(t) = -v_{ac} + V_{o2} \rightarrow (0 \le t \le T_L) \qquad (3.1)$$

where $T_L$ represents the cycle of the line voltage.

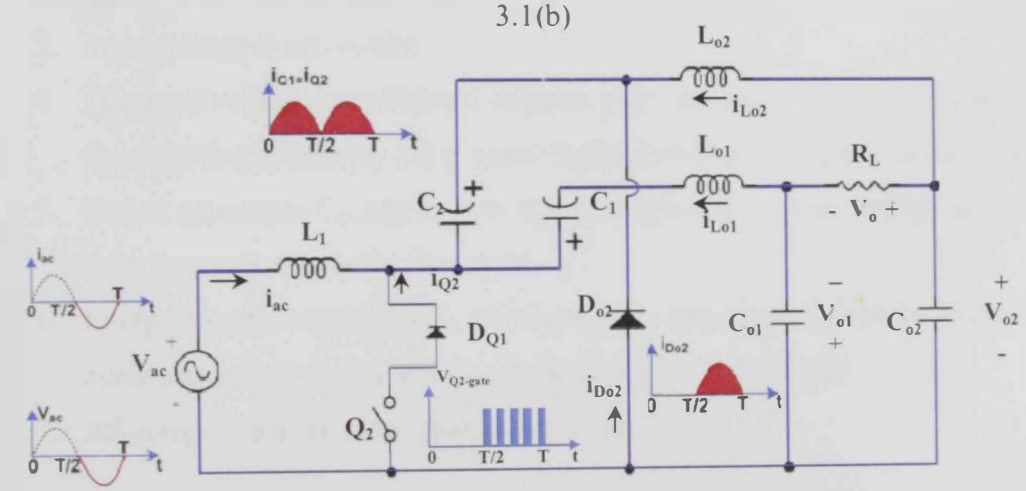
Note that the capacitors are fully charged by input voltage and biased by half the output voltage. (Note: The capacitor voltages are always positive for gain > 2).




3.1(a)




3.1(b)




3.1(c)

Fig.3.1: (a) Proposed bridgeless Cuk rectifier, (b) Positive half-line cycle, and (c) Negative half-line cycle.

## 3.2 Analysis of the Proposed Cuk Converter

The same techniques and approximations for the steady-state analysis of the continuous conduction mode with a few modifications may be applied to the discontinuous conduction mode.

1. Inductor volt-second balance: The DC component of the voltage applied to an inductor must be zero.

$$< v_L >= \frac{1}{T_s}\int_0^{T_s} v_L\,(t)dt = 0 \qquad (3.2)$$

2. Capacitor charge balance: The dc component of current applied to a capacitor must be zero.

$$< i_C >= \frac{1}{T_s}\int_0^{T_s} i_C\,(t)dt = 0 \qquad (3.3)$$

These assumptions must be held for any circuit that operates in steady state, regardless of the operating mode.

3. Input voltage is sinusoidal.
4. The input voltage is considered constant over one switching cycle ($T_s$) since the switching frequency ($f_s$) is much higher than the line frequency ($f_L$).
5. Output capacitors $C_{o1}$ and $C_{o2}$ are large enough such that the voltage across them is constant over the line cycle.
6. Energy transfer capacitors $C_1$ and $C_2$ voltages are constant over the switching cycle and follow the input voltage profile within a line cycle.
7. All components are ideal; thus, there are no losses.

Due to the symmetry of the operations, the positive half-line cycle is analyzed through the three distinct stages as shown in Fig. 3.2 to 3.4. Volt-second balance is applied for each inductor voltage and charge balance for each capacitor current in the

network. The switching ripple in the output capacitor voltages is ignored while the inductor current switching ripple is considered.

### 3.2.1 First Stage: $[t_o, t_1]$

During the first subinterval, the transistor conducts for $0 < t < D_1T_s$, and diode $D_{o1}$ is reversed-biased by the capacitor voltage ($V_{C1}$). The output diode $D_{o2}$ is reversed-biased by capacitor voltage ($V_{C2}$).The converter circuit elements are connected as in Fig. 3.2. The inductor voltages are given by:

$$\begin{aligned} V_{L1} &= v_{ac} \\ V_{Lo1} &= V_{C1} - V_{o1} \\ V_{Lo2} &= V_{o2} - V_{C2} \end{aligned} \tag{3.4}$$

It can be inferred from inductor voltage equation Eq. (3.4) that the inductor voltages are equal to the input voltage by substituting Eq. (3.1) in Eq. (3.4), yielding $V_{Lo1} = v_{ac}$ and $V_{Lo2} = v_{ac}$. The capacitor and inductor currents are related by:

$$\begin{aligned} i_{C1}(t) &= -i_{Lo1}(t) \\ i_{C2}(t) &= i_{Lo2}(t) \end{aligned} \tag{3.5}$$

The capacitors $C_{o1}$ and $C_{o2}$ supply the load current during the first stage, where the output capacitor currents equals the inductor current minus the load current.

$$\begin{aligned} i_{Co1}(t) &= i_{Lo1}(t) - \frac{V_O}{R} \\ i_{Co2}(t) &= -i_{Lo2}(t) - \frac{V_O}{R} \end{aligned} \tag{3.6}$$

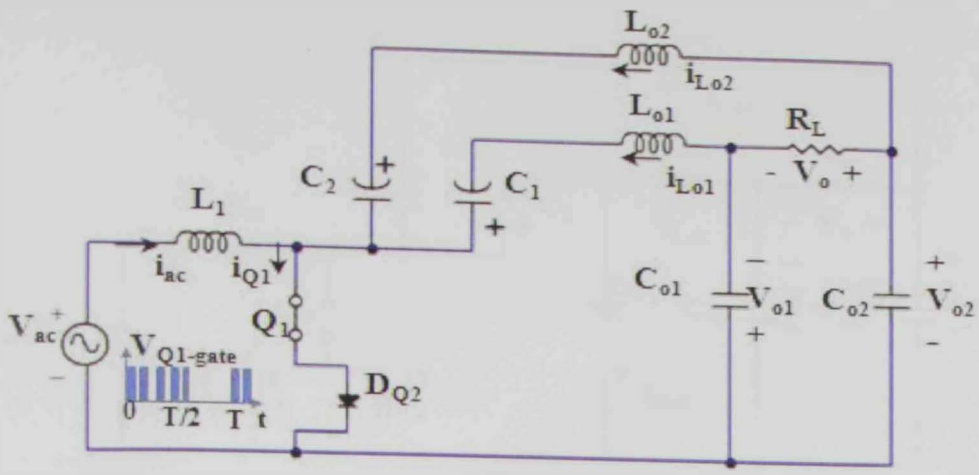



Fig. 3.2: First stage of operation.

The current passing through node $Q_1$ is the summation of the three inductor currents, and the voltage across the diode is the input voltage plus half of the output voltage as shown below.

$$I_{Q1} = I_{Lo1} + I_{Lo2} + I_{L1}$$
$$V_{Do1} = -V_{C1} = -v_{ac} - V_{o1} \qquad (3.7)$$

### 3.2.2 Second Stage: $[t_1, t_2]$

The second stage starts at the instant $t_1$, where switch $Q_1$ turns off and diode $D_{o1}$ conducts to find a path for the inductor currents during $D_1T_s < t < (D_1+D_2)T_s$ simultaneously. The circuit then reduces to Fig.3.3. During this stage the inductor currents supply the load and recharge the capacitors. The diode $D_{o2}$ is reversed-biased by the capacitance voltages ($V_{C1} + V_{C2}$). The stage ends when the summation of the inductors current is zero and $D_{o1}$ becomes reverse biased. Hence, diode $D_{o1}$ is switched off at a zero current.

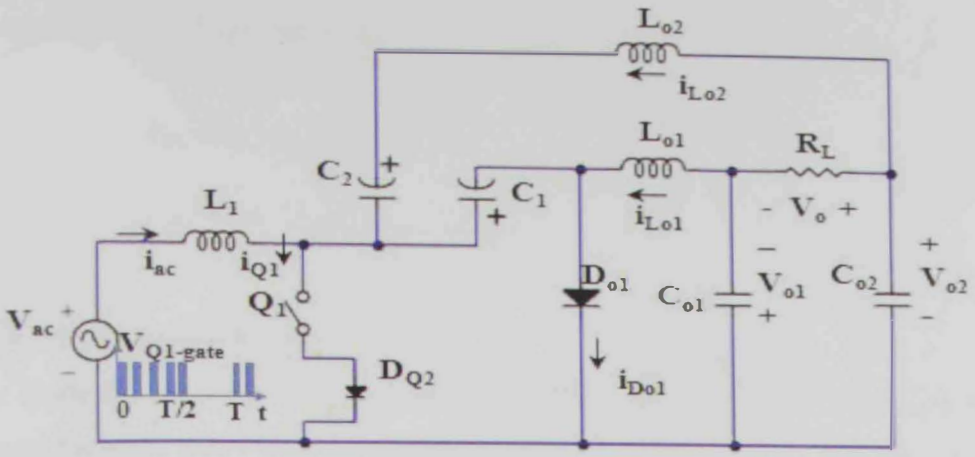



Fig.3.3: Second stage of operation.

The inductor voltages are given by:

$$V_{L1} = v_{ac} - V_{C1}$$
$$V_{Lo1} = -V_{o1} \qquad (3.8)$$
$$V_{Lo2} = V_{o2} - V_{C1} - V_{C2}$$

The energy transfer capacitor currents are given below:

$$i_{C1}(t) = i_{L1}(t) + i_{Lo2}(t)$$
$$i_{C2}(t) = i_{Lo2}(t) \qquad (3.9)$$

The output filter capacitor currents are:

$$i_{Co1}(t) = i_{Lo1}(t) - \frac{V_O}{R}$$
$$i_{Co2}(t) = -i_{Lo2}(t) - \frac{V_O}{R} \qquad (3.10)$$

The current and voltage stress over the switches are given by:

$$V_{Q1} = V_{C1} = v_{ac} + V_{o1}$$

$$I_{Do1} = I_{Lo1} + I_{Lo2} + I_{L1} \qquad (3.11)$$

### 3.2.3 Third Stage: [t2, t3]

The diode $D_{o1}$ becomes reverse-biased at time $t = (D_1 + D_2)\, T_s$, when the diode current becomes zero. Then the circuit is shown in Fig. 3.4 with both transistor and diode in the off state.

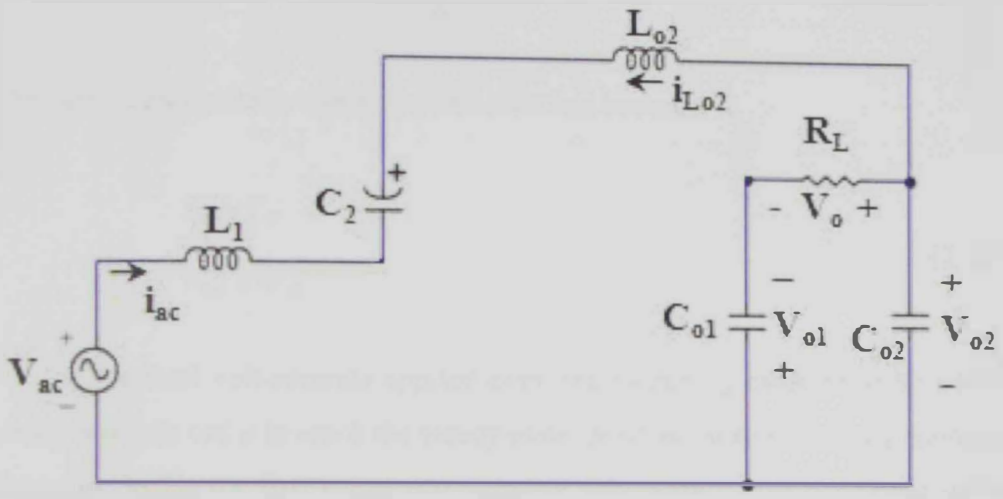



Fig.3.4: Third stage of operation.

The capacitors $C_1$ and $C_2$ are being charged by the inductor currents $i_{Lo1}$ and $i_{Lo2}$. The inductor behaves as a current source, which keeps the current constant during the third subinterval $(D_1 + D_2)\, T_s < t < T_s$, and therefore, the inductor voltage must also be zero in accordance with the relationship $V_L(t) = L di_L(t)/dt$. As a result, the network equations for the third subinterval are:

$$V_{L1} = V_{Lo1} = V_{Lo2} = V_{L2} = 0 \qquad (3.12)$$

The transfer energy capacitor currents are given by:

$$i_{C1}(t) = -i_{Lo1}(t) \Rightarrow i_{C1}(t) = 0$$
$$i_{C2}(t) = i_{Lo2}(t) \tag{3.13}$$

and the output filter capacitor currents are:

$$i_{Co1}(t) = i_{Lo1}(t) - \frac{V_O}{R}$$
$$i_{Co2}(t) = -i_{Lo2}(t) - \frac{V_O}{R} \tag{3.14}$$

The current and voltage stress over the switches become.

$$V_{Q1} = V_{ac}$$
$$V_{Do1} = -V_{o1} \tag{3.15}$$

The total volt-seconds applied over one switching cycle must be zero in the steady-state. In order to reach the steady-state, positive volt-seconds are applied to the inductors during the first stage, and negative volt-second must be applied during the second stage. Therefore, the inductor voltages are equal to the input voltage during the first stage but only equal to half of the output voltage during the second stage, which must be negative as shown in the inductor voltages waveform Fig. 3.5. Hence, $V_o$ is greater than $v_{ac}$, or in other words, the DC output voltage is greater than the input voltage.

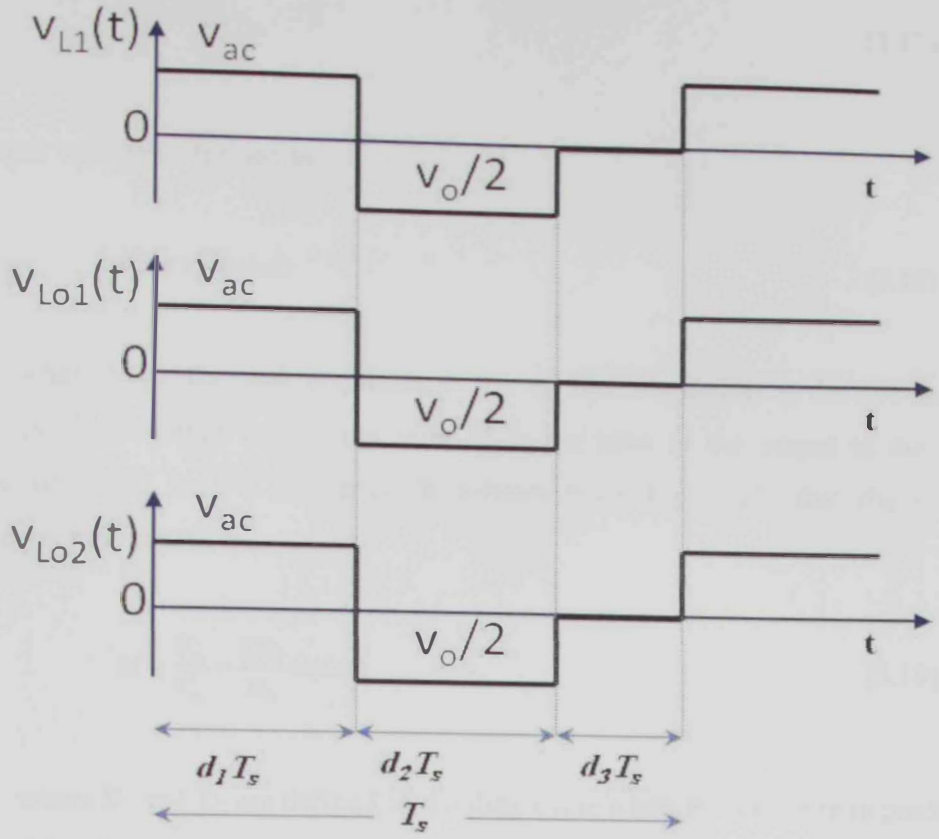



Fig.3.5: Inductor voltages waveform for the proposed DCM Cuk rectifier.

### 3.2.4 Step1: Steady State Analysis

Applying total volt-seconds to the inductors over one switch cycle result in

$$\begin{aligned} &< V_{L1} >_{T_s} = v_{ac} - V_{C1}D_2 = 0 \\ &< V_{Lo1} >_{T_s} = V_{C1}D_1 - V_{o1} = 0 \\ &< V_{Lo2} >_{T_s} = V_{o2} - V_{C1}D_2 - V_{C2} = 0 \end{aligned} \tag{3.16}$$

Assuming $V_o = V_{o1} + V_{o2}$ and $V_{o1} = V_{o2} = \frac{1}{2}V_o$, the three equations are solved by averaging the inductor voltages over one switching cycle. This yields the expression for the output voltage ($V_o$) as function of the duty cycle as shown in the equation:

$$V_o = \frac{2D_1}{D_2} v_{ac} \tag{3.17}$$

The input voltage is defined as,

$$v_{ac} = v_m \sin(\omega t) \tag{3.18}$$

where $V_m$ is the peak amplitude of the $v_{ac}$ function and $\omega$ is the line angular frequency. The voltage conversion ratio M is the ratio of the output to the input voltage of a DC to DC converter. It follows from Eq. (3.17) that the voltage conversion ratio is will be

$$M = \frac{V_o}{V_m} = \frac{2D_1}{D_2} \sin(\omega t) \tag{3.19}$$

where $D_1$ and $D_2$ are defined as the duty cycle when the switch is in position 1 and position 2, respectively, during one switching cycle. The duty cycle when the switch is in position 2 is given by

$$D_2 = \frac{2D_1}{M} \sin(\omega t) \tag{3.20}$$

**3.2.4.1 Control Input Duty Cycle ($D_1$)**

The following inequality is required to operate at DCM

$$D_1 + D_2 < 1 \tag{3.21}$$

The control input duty cycle $D_1$ as a function of M can be found by eliminating the value of $D_2$, which is given in Eq. (3.20).

$$D_1 + \frac{2D_1}{M} \sin(\omega t) < 1 \tag{3.22}$$

Operating in the worst case, the following condition for DCM is

$$D_1 < \frac{M}{M+2} \tag{3.23}$$

### 3.2.4.2 Inductor Currents Waveform

In order to compute the dc component of the inductor currents, the inductor currents' waveform are sketched in Fig. 3.6. During the first stage, the three inductor currents increase linearly at a rate that is proportional to the input voltage $v_{ac}$. The rate of increase of the three inductor currents are given by,

$$\frac{di_{Ln}}{dt} = \frac{v_{ac}}{L_n}, \quad \text{where } L_n = L_1, L_{o1}, L_{o2} \tag{3.24}$$

During the second stage, the equivalent inductor current rate begins decreasing when the diode $D_{o1}$ conducts. The rate of decrease is equal to half of the output voltage as shown in Fig. 3.6 and given below.

$$\frac{di_{Ln}}{dt} = \frac{-\frac{1}{2}v_o}{L_n} \tag{3.25}$$

The inductor current ripple magnitude $\Delta_{iL}$ varies with the applied voltages rather than the applied currents, as shown in Fig. 3.6. The ripple magnitude is the function of the applied voltage ($v_{ac}$) the inductance (L) and the transistor conduction time ($D_1T_s$). but it is not a function of the load resistance (R),

$$\Delta i_{Ln} = \frac{v_{ac}}{2L_n} D_1 T_S \tag{3.26}$$

The equivalent inductor current ripple through the three inductors becomes,

$$\Delta i_{Leq} = \frac{v_{ac}}{2L_{eq}} D_1 T_S \tag{3.27}$$

where $L_{eq} = L_1 // L_{o1} // L_{o2}$ is an equivalent inductance of the three inductors. The converter operates in the discontinuous conduction mode when the sum of the input and output diode current becomes zero. Referring to the waveforms in Fig (3.6), the average input current over one switching cycle is

$$i_{in} = i_{L1} = \frac{v_{ac}}{2L1} D_1 T_S [D_1 + D_2] + I_x \tag{3.28}$$

Furthermore, the average output currents over one switching cycle can be written as:

$$i_{Lo1} = \frac{v_{ac}}{2L_{o1}} D_1 T_S [D_1 + D_2]$$

$$i_{Lo2} = \frac{v_{ac}}{2L_{o2}} D_1 T_S [D_1 + D_2] - I_x \tag{3.29}$$

where $i_{Lo1} + i_{Lo2} = 2\, i_o$

The sum of the three waveforms shown in Fig. 3.6 and expressed by Eqs. (3.28) and (3.29) result in the equivalent waveforms ($i_{Leq}(t)$) shown in Fig. 3.6.

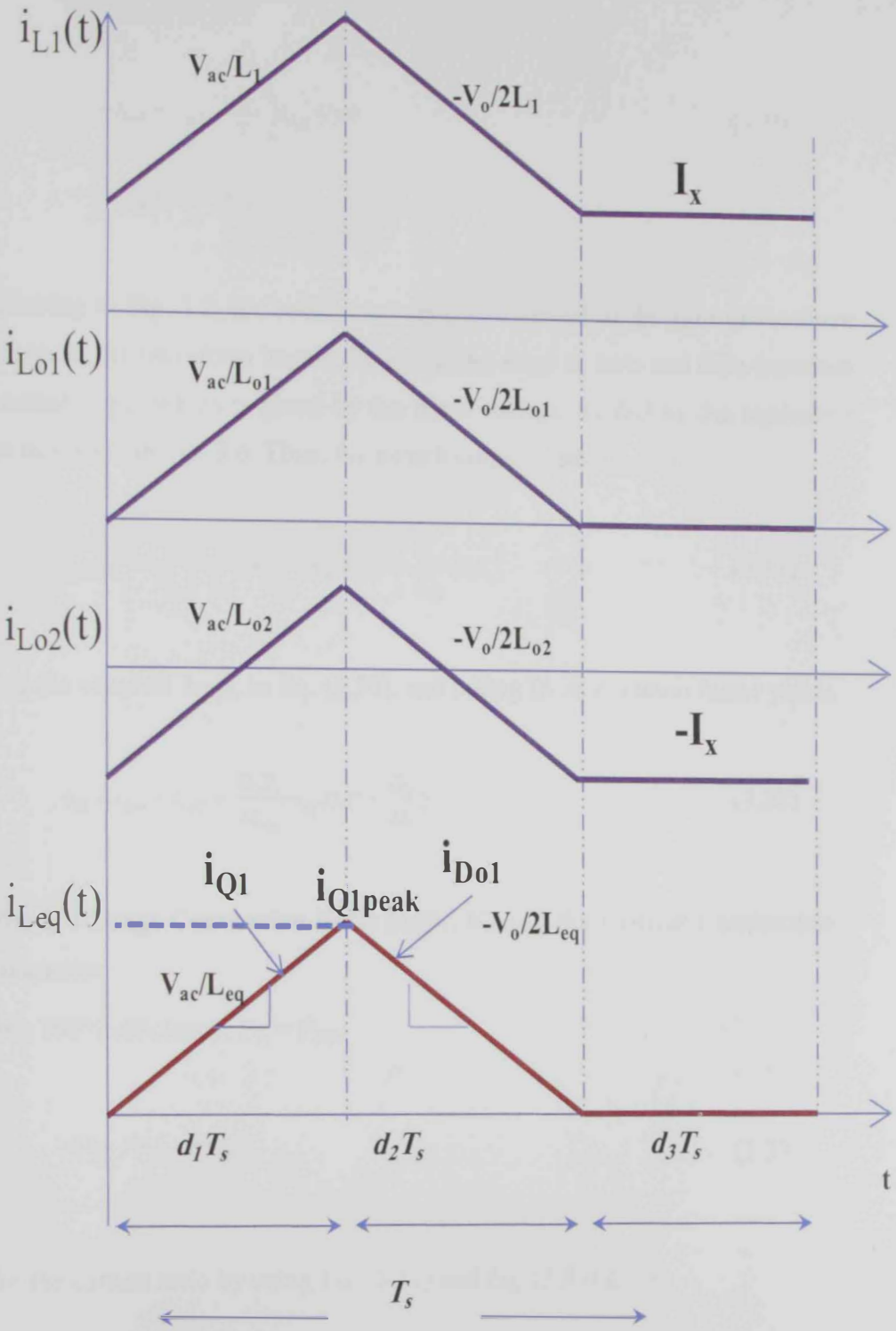



Fig.3.6: Inductor currents' waveform for proposed DCM Cuk rectifier.

The average of the equivalent inductor currents is found by integrating the $i_{Leq}(t)$ waveform over one switching cycle.

$$i_{L1} + i_{Lo1} + i_{Lo2} = \frac{1}{T_s}\int_0^{T_s} i_{Leq}(t)dt \qquad (3.30)$$

$$= \frac{1}{2} i_{Q1pk}(D_1 + D_2)$$

Referring to Fig. 3.2, the switch current ($i_{Q1}$) is equal to the sum of the three inductor currents. Its waveform begins the switching stage at zero and then increases with a constant slope, which is given by the input voltage divided by the equivalent inductance as shown in Fig. 3.6. Thus, the switch current peak $I_{Q1\text{-}pk}$ is

$$I_{Q1,pk} = (\frac{1}{L_1} + \frac{1}{L_{o1}} + \frac{1}{L_{o2}}) v_{ac} D_1 T_s = \frac{v_{ac}}{L_{eq}} D_1 T_s \qquad (3.31)$$

Substituting the value of $I_{Q1pk}$, in Eq. (3.30), and taking $D_1$ as common factor yields

$$i_{L1} + i_{Lo1} + i_{Lo2} = \frac{D_1 T_s}{2L_{eq}} v_{ac} D_1 (1 + \frac{D_2}{D_1}) \qquad (3.32)$$

### 3.2.5 Step 2: Voltage Conversion Ratio M($D_1$, K) and the Critical Conduction Parameter

Considering 100% efficiency, $P_{in} = P_{out}$,

$$< v_{ac} >< i_{in} >= v_o i_o \qquad (3.33)$$

Solving for the current ratio by using Eq. (3.17) and Eq. (3.33) gives

$$\frac{i_o}{< i_{in} >} = \frac{D_2}{2D_1} \tag{3.34}$$

The input line current is defined by finding the value of the output current.

### 3.2.5.1 Output Current

The connection of the output resistor to its adjacent components is detailed in Fig. 3.7 . The node equation of this network is

$$i_{Lo1}(t) = i_{Co1}(t) + \frac{V_O}{R} \tag{3.35}$$

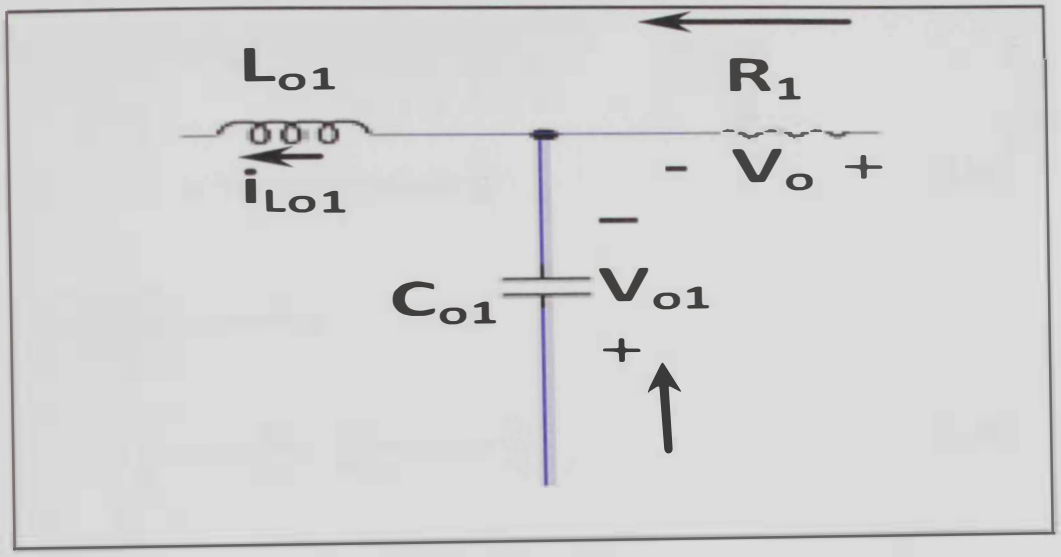



Fig. 3.7: Connection of the output capacitor $C_{o1}$ to adjacent components.

By applying the charge balance on output capacitors $C_{o1}$ and $C_{o2}$, the net change in capacitors charges is found. Therefore, the load current must be supplied by the direct inductors $L_{o1}$ and $L_{o2}$ connected to the load current as shown in Eq. (3.36). In particular, the DC component of the inductor current must equal the load current as given in Eq. (3.37).

$$< i_{C_{o1}}(t) >_{T_S} = i_{Lo1}(t) - \frac{V_O}{R}(D_1 + D_2 + D_3) = 0 \Leftrightarrow I_{Lo1} = \frac{V_O}{R}$$
$$< i_{C_{o2}}(t) >_{T_S} = i_{Lo2}(t) - \frac{V_O}{R}(D_1 + D_2 + D_3) = 0 \Leftrightarrow I_{Lo2} = -\frac{V_O}{R} \quad (3.36)$$

As a result,

$$I_{Lo1} = I_{Lo2} = \left|\frac{V_o}{R_L}\right| \quad (3.37)$$

### 3.2.5.2 Input Current

Substituting Eq. (3.30) in Eq. (3.32) yields

$$i_{in} + 2i_o = \frac{D_1 T_s}{2L_{eq}} v_{ac} D_1 (1 + \frac{D_2}{D_1}) \quad (3.38)$$

Then factoring $i_{in}$ result in

$$i_{in}(1 + \frac{2i_o}{i_{in}}) = \frac{D_1 T_s}{2L_{eq}} v_{ac} D_1 (1 + \frac{D_2}{D_1}) \quad (3.39)$$

Furthermore, substituting Eq. (3.34) in Eq. (3.39) produces,

$$i_{in}(1 + \frac{D_2}{D_1}) = \frac{D_1 T_s}{2L_{eq}} v_{ac} D_1 (1 + \frac{D_2}{D_1}) \quad (3.40)$$

Simplifying Eq. (3.40) gives

$$i_{in} = \frac{D_1 T_s}{2L_{eq}} v_{ac} D_1 \tag{3.41}$$

The input current as a function of the emulated input resistance ($R_e$) of the converter is

$$i_{in} = \frac{v_{ac}}{R_e} \tag{3.42}$$

where input current $i_{in}$ is equal to the inductor current $i_{L1}$, and the emulated input resistance equals

$$R_e = \frac{2L_{eq}}{D_1^2 T_S} \tag{3.43}$$

The input current $i_{in}$ is in-phase with input voltage $v_{ac}$ at any given operating point; thus the input current obeys Ohm's law as shown in Eq. (3.42).

### 3.2.5.3 Voltage Conversion Ratio M($D_1$, K)

The voltage conversion ratio can be found by solving Eq. (3.33), where the input and output power are:

$$< P_{in}(t) >_{T_L} = \frac{1}{T_L} \int_0^{T_L} v_{ac} < i_{in}(t) >_{T_s} dt \tag{3.44}$$

$$< P_{in}(t) >_{T_L} = \frac{1}{T_L} \frac{D_1 T_s}{2L_{eq}} D_1 \int_0^{T_L} v_{ac}^2 dt_1$$

$$< P_{in}(t) >_{T_L} = \frac{D_1 T_s}{2L_{eq}} D_1 \frac{V_m^2}{2}$$

$$P_o = \frac{V_o^2}{R} \tag{3.45}$$

, resulting in

$$\frac{V_o^2}{V_m^2} = \frac{RT_s D_1^2}{2(2L_{eq})} \tag{3.64}$$

The voltage conversion ratio as a function of the conduction parameter K is given by,

$$M(D_1, K) = \frac{D_1}{\sqrt{2K}} \tag{3.47}$$

where K is a unit-less parameter and can be expressed as:

$$K = \frac{2L_{eq}}{RT_S} \tag{3.48}$$

Moreover, solving for $D_1$ yields

$$D_1 = M\sqrt{2K} \tag{3.49}$$

### 3.2.5.4 Critical Conduction Parameter ($K_{crit}$)

Inserting Eq. (3.23) into Eq. (3.49) and simplifying results in the following condition for $K_{crit}$ as a function of M to operate in DCM:

$$K_{crit} < \frac{1}{2(2\sin(\alpha t) + M)^2} \tag{3.50}$$

where $K_{crit}$ is the critical value of K operating at DCM, which is a unit-less parameter.

### 3.2.5.5 Large Signal Model

The switch network input port is designed by Eq. (3.42) shown in Fig. 3.8 and the switch network output port is modeled by Eq. (3.37). Otherwise, it could be designed by finding the output power, which is equal to the input power as shown in Eq. (3.51).

$$\langle i_o(t)\rangle_{Ts}\langle v_o(t)\rangle_{Ts} = \frac{\langle v_{ac}(t)\rangle_{Ts}^2}{R_e} = \langle p(t)\rangle_{T_s} \tag{3.51}$$

In other words, the lossless power states that the input and output powers are equal:

$$P_{out} = \frac{V_{ac}^2}{R_e} = \frac{V_o^2}{R} \tag{3.52}$$

By simplifying Eq. (3.52), the voltage conversion ratio M becomes,

$$M = \sqrt{\frac{R}{2R_e}} \tag{3.53}$$

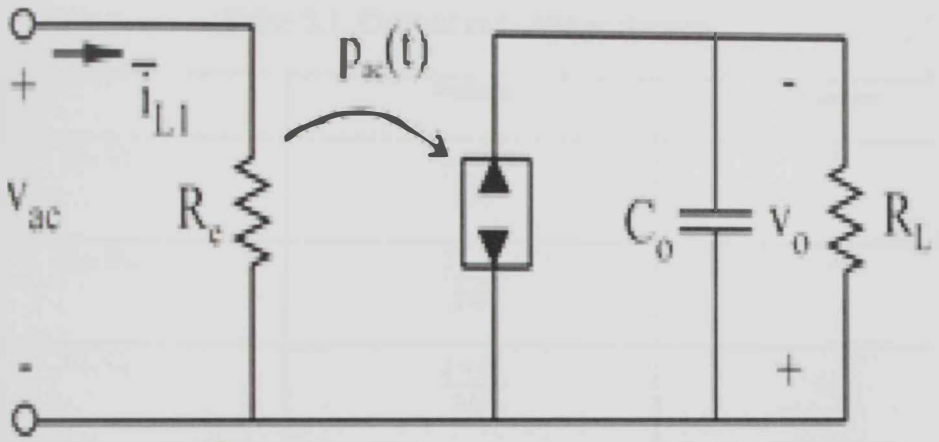



Fig. 3.8: Large signal model of the general averaged Equivalent circuit in a converter operating in DCM.

## 3.3 Stresses

The current stresses on the $Q_1$ and $D_{o1}$ equal the summation of the inductor currents as given in Eq. (3.7) and Eq. (3.11) and displayed in Fig. 3.6.The voltage stresses

over the switching are shown in Fig.3.9. The voltage and current stresses of the converter components are shown in Table 1. All stresses are normalized with respect to the output voltage and load current.

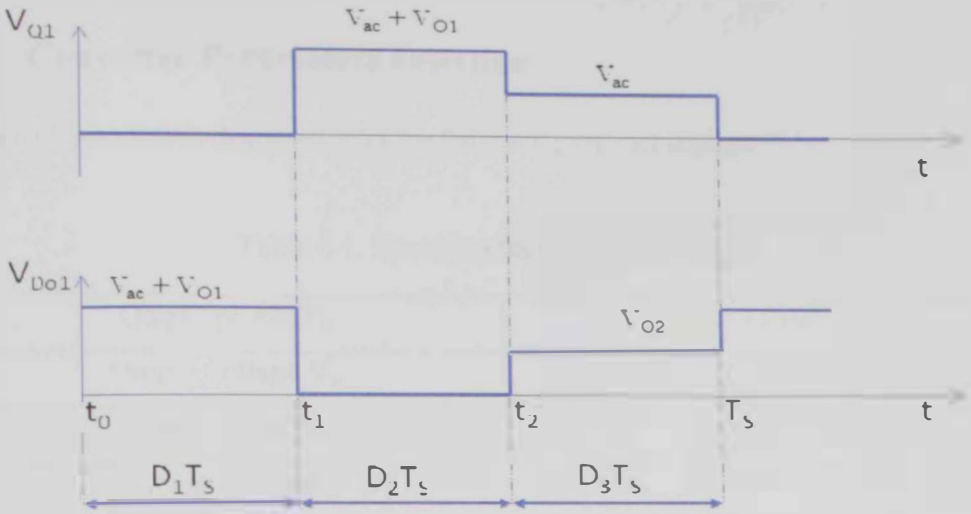



Fig.3.9: The semiconductor switch and the diode voltage stresses.

Table 3.1: Current and voltage stresses.

| | Voltage | Current |
|---|---|---|
| $Q_1$, $Q_2$ | $\frac{2+M}{2M}$ | $M$ |
| $D_{o1}$, $D_{o2}$ | $\frac{2+M}{2M}$ | $M$ |
| $C_1$, $C_2$ | $\frac{2+M}{2M}$ | $\pm 1\frac{1}{2}$ |
| $C_{o1}$, $C_{o2}$ | $\frac{1}{2}$ | $\frac{1}{2}$ |
| $L_1$ | $\frac{1}{2}$ | $M$ |
| $L_{o1}$, $L_{o2}$ | $\frac{1}{2}$ | $\pm 1\frac{1}{2}$ |

# CHAPTER 4

# Design, Simulation and Measurements

## 4.1 Converter Parameters Selection

The Cuk rectifier is designed with the following characteristics:

Table 4.1: Specifications of the prototype.

| | |
|---|---|
| Output power $P_o$ | 125W |
| Output voltage $V_o$ | 250V |
| Input voltage $v_{ac}$ | 100 sin (2π50t)V |
| Switching frequency $f_s$ | 50kHz |
| Output Resistance, R | 500Ω |
| Input Current ripple $\Delta I_{in}$ | 10% $I_{in}$ |
| Output voltage ripple $\Delta V_o$ | 0.6% $V_o$ |

The voltage conversion ratio is:

$$M(D) = \frac{250}{100} = 2.5 \tag{4.1}$$

The critical conduction parameter can be evaluated from Eq. (3.50)

$$K_{crit} = 24.69 \times 10^{-3} \tag{4.2}$$

To assure DCM operation, the $K < K_{crit}$ is chosen to be:

$$K = 4.9 \times 10^{-3} \tag{4.3}$$

The control input duty cycle $D_1$ is found by Eq. (3.49):

$$D_1 = M\sqrt{2K} = 0.248 \tag{4.4}$$

The input current ripple as given in the specification shown in Table 4.1 is:

$$\Delta I_{in} = 10\% \frac{2P}{V_m} = 0.25 \tag{4.5}$$

### 4.1.1 Inductors Design

The design of the input inductor is completed by using the desired ripple value of the input current. Therefore, $L_1$ can be obtained considering the maximum current ripple as given by:

$$L_1 = \frac{V_m D_1 T_s}{\Delta I_{L1}} = 2\,\text{mH} \tag{4.6}$$

where $\Delta I_{L1}$ is the same as $\Delta L_{in}$.

An equivalent inductance $L_{eq}$ is affected by the conduction parameter as shown in Eq. (3.48). Thus, evaluating this equation gives:

$$L_{eq} = \frac{KRT_s}{2} = 24.5\,\mu\text{H} \tag{4.7}$$

The output inductor $L_{o1}$ and $L_{o2}$ are equal and can be found using the following equation:

$$L_{o1} = L_{o2} = \frac{L_1 L_{eq}}{L_1 - L_{eq}} = 50\,\mu\text{H} \tag{4.8}$$

### 4.1.2 Energy Transfer Capacitors Design

The capacitors $C_1$ and $C_2$ are designed under two constraints in order to have the proposed topology operates as a true PFC converter. The voltage across $C_1$ and $C_2$ are

within a switching cycle and to follow the input voltage profile within a line cycle. They are very important elements in the proposed Cuk rectifier because their values have a significant influence on the input current waveform. The resonant frequency of $C_1$, $C_2$, $L_1$, $L_{o1}$ and $L_{o2}$ must be much greater than the line frequency to avoid input current oscillations at every half-line cycle and lower than the switching frequency to assure an almost constant voltage in a switching period. The $C_1$ and $C_2$ designed equation is given by:

$$C_1 = C_2 = \frac{1}{(2\pi f_r)^2 (L_1 + L_{o1})} \qquad (4.9)$$

where $C_1 = C_2$ and $f_L < f_r < f_s$

Different capacitance values are chosen as shown in Table 4.2 to study their effect on the input current and their capacitor voltages. The first capacitance value is selected to be close to line frequency, and the third one is selected to be close to switching frequency, while the second one is selected to be in between. The influence of the three capacitors' values on the input current and their voltages is shown in Fig. 4.1 and Fig.4.2. The input current signal is not in-phase with the input voltage when the resonant frequency is either near to the line frequency or switch frequency as shown in Fig. 4.1(a) and Fig. 4.1(b). Furthermore, the capacitor voltage has higher peak value than that shown in Fig. 4.2(c), which means the capacitor voltages cannot be considered constant in a switching cycle. In other words, the capacitor voltage in Fig. 4.2(a) is charging very quickly, but it is slowly charging in Fig. 4.2(b). As a result, the best value for the energy capacitors $C_1$ and $C_2$ are calculated based on Eq. (4.9) by applying a resonant frequency greater than the line frequency and less than the switching frequency with a value of $1\mu F$ [46, 57].

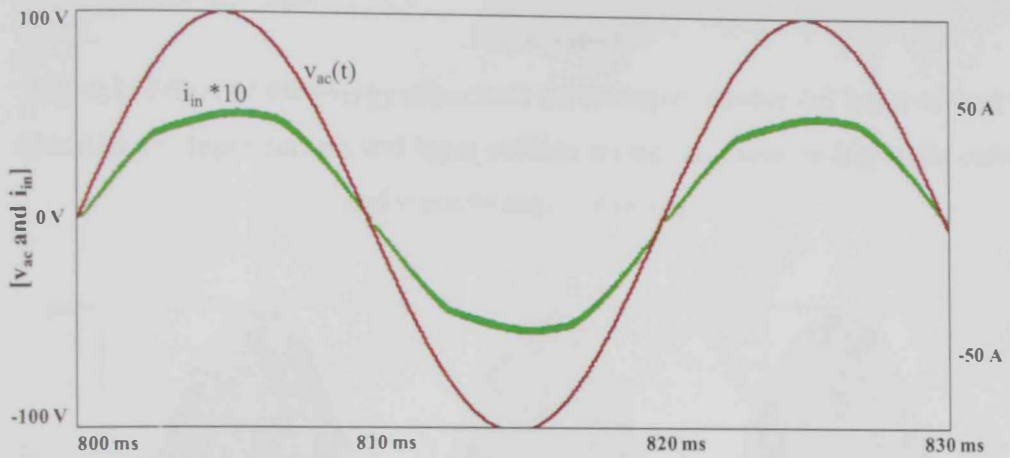
Table 4.2: Effect of the resonant frequency on the energy transfer capacitor values.

| $f_r$ (Hz) | C1= C2 (μF) |
|---|---|
| 1000 | 12 |
| 3515 | 1 |

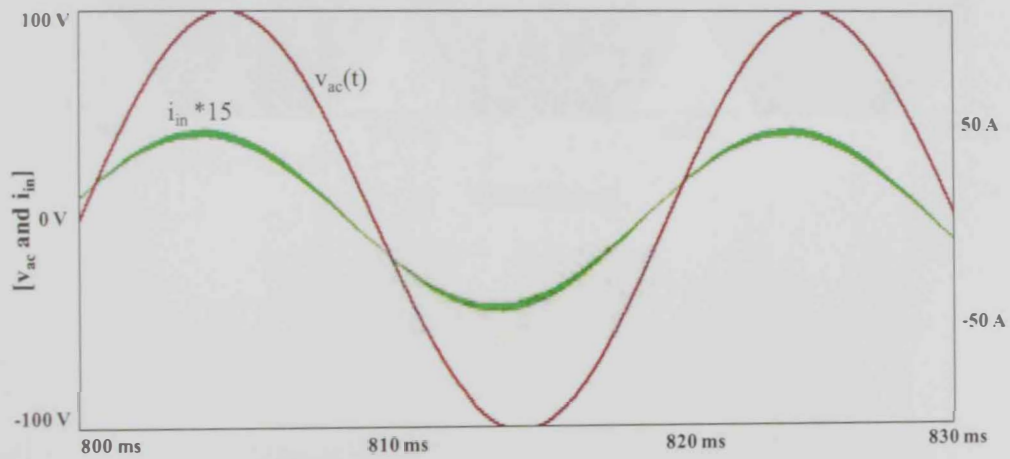
| | |
|---|---|
| 10,000 | 0.12 |

Considering a resonant frequency ($f_r$) of (3515 Hz), the energy transfer capacitors are given by

$$C_1 = C_2 = \frac{1}{(2\pi 3515)^2 (2\times 10^{-3} + 50\times 10^{-6})} = 1\eta \qquad (4.10)$$




(a) $C_1 = C_2 = 0.1\ \mu F$




(b) $C_1 = C_2 = 12.356\ \mu F$

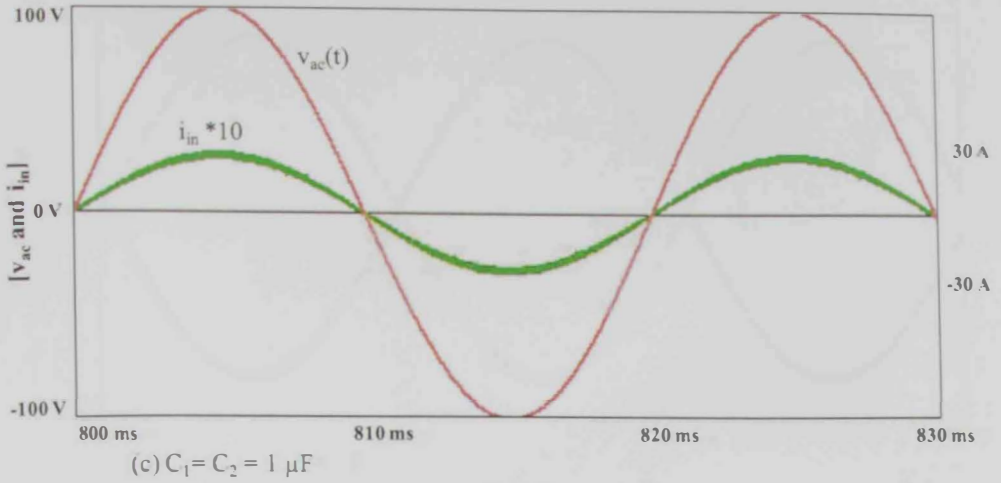
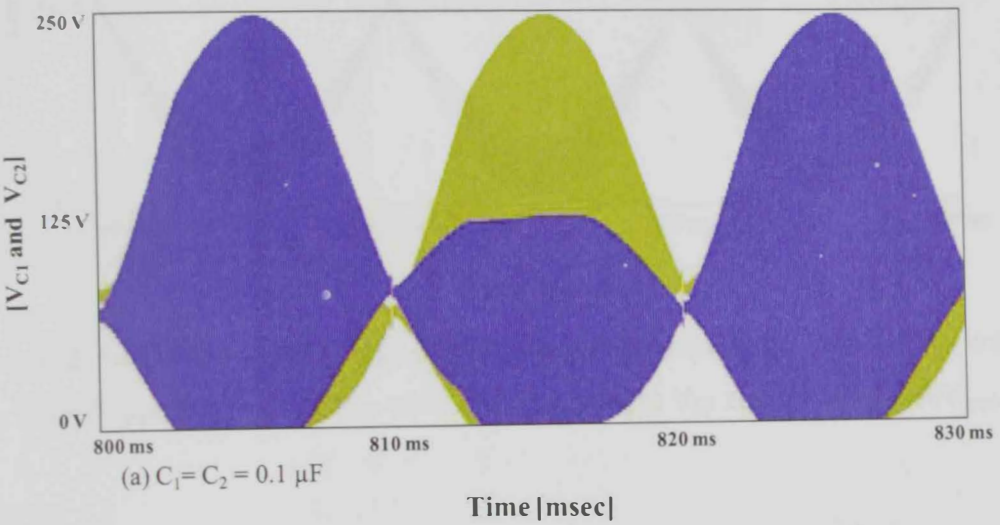



Fig. 4.1: Effect of the energy capacitors on the input current: (a) Input current is distorted, (b) Input current and input voltage are out of phase, and(c) Input current and input voltage are in-phase.



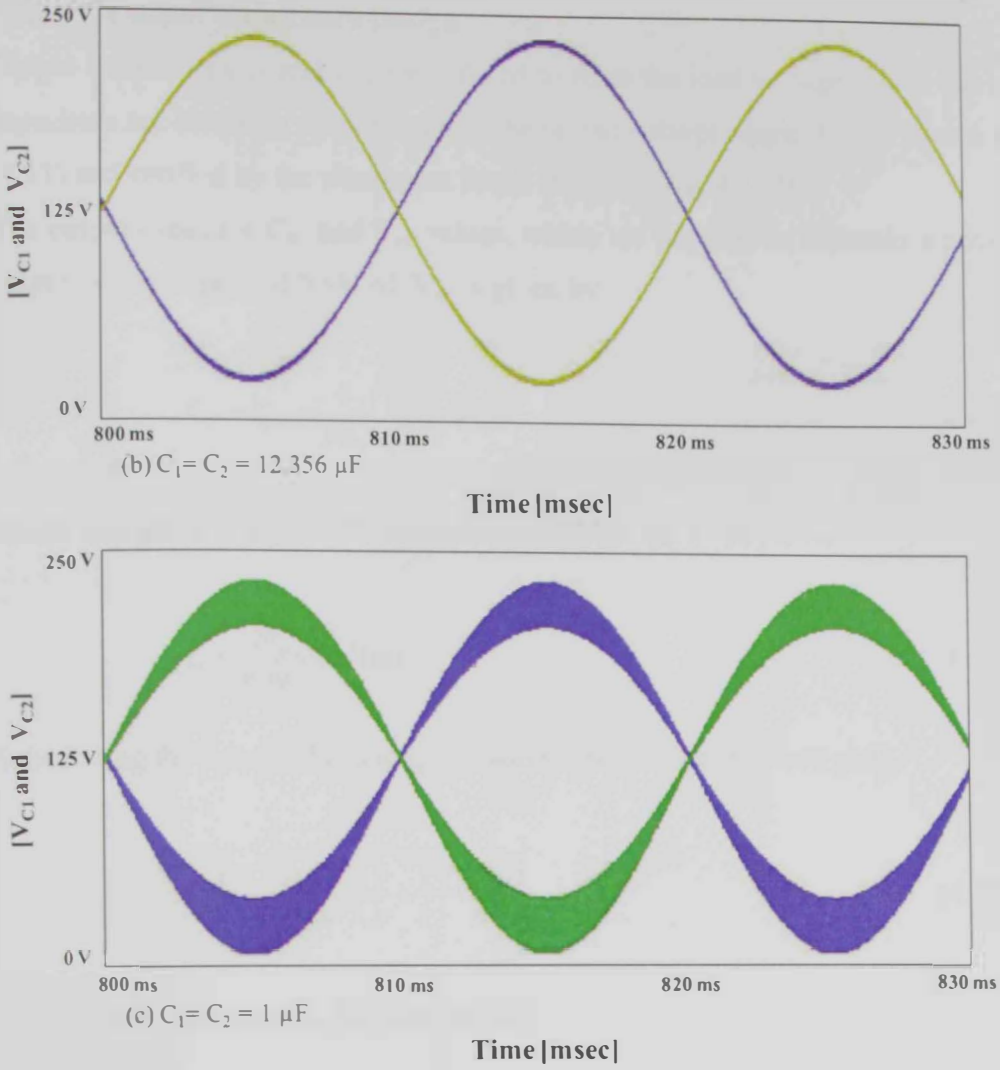



Fig. 4.2: Effect of the energy capacitors on their voltage: (a) $V_{C1}$ and $V_{C2}$ with $600V_{peak}$, (b) $V_{C1}$ and $V_{C2}$ with $230V_{peak}$, and (c) $V_{C1}$ and $V_{C2}$ with $250V_{peak}$.

### 4.1.3 Output Capacitors Design

Output capacitors $C_{o1}$ and $C_{o2}$ are utilized to filter the load voltage. Thus, the output capacitors are inversely proportional to the output voltage ripple $\Delta V_o$ as shown in Eq. (4.11) and verified by the simulation result shown in Fig. 4.3 [46].

The output capacitor $C_{o1}$ and $C_{o2}$ values, which are required to maintain a peak-peak output voltage ripple of 0.6% of $V_o$, is given by

$$C_{o1} = C_{o2} = \frac{1}{\Delta v_o} \int_{T_L/8}^{3T_L/8} (i_o - I_o)\,dt \qquad (4.11)$$

where $I_o$ is given in Eq. (3.37) and $i_o$ is found from Eq. (3.36) to be

$$i_o = \frac{2V_o}{R_e M^2} \sin^2(\omega t) \qquad (4.12)$$

Substituting the values of $I_o$ and $i_o$ and solving the integration will yield,

$$= \frac{T_L V_o}{2\Delta v_o} \left[ \frac{1}{R_e M^2} \left( \frac{1}{\pi} + \frac{1}{2} \right) - \frac{1}{R} \right] \qquad (4.13)$$

By evaluating Eq. (4.13 ), $C_{o1}$ and $C_{o2}$ are:

$$C_{o1} = C_{o2} = 2200\,\mu F \qquad (4.14)$$

Table 4.3: The relationship between the output capacitor and output voltage ripples.

| $C_{o1}$=$C_{o2}$ (uF) | $\Delta v_o$ (V) |
|---|---|
| 220 | 14.46 |
| 636.5 | 5 |
| 2200 | 1.45 |

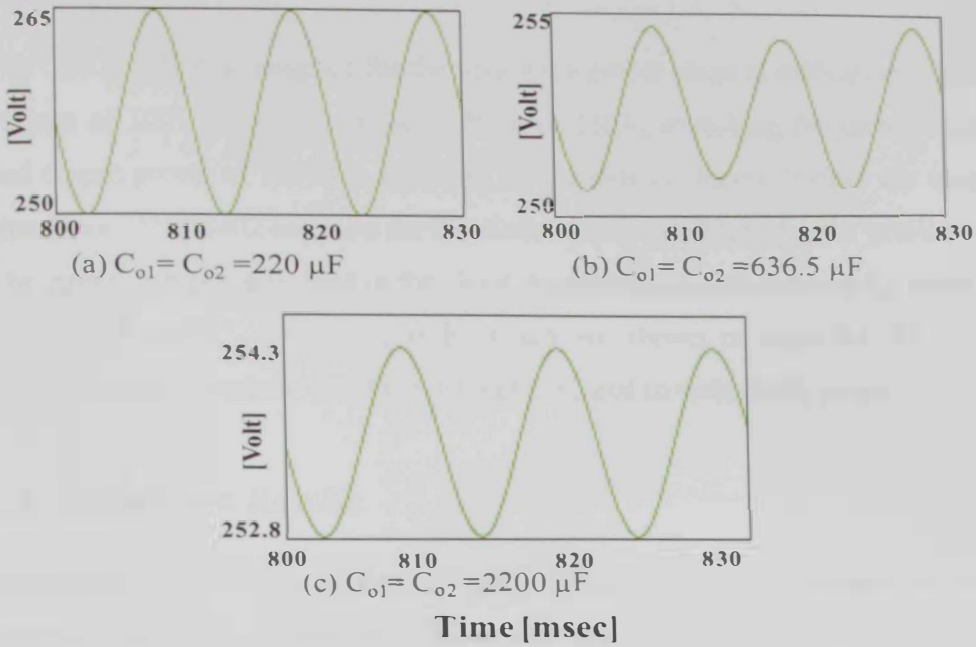



Fig. 4.3: Influence of the output capacitors on the output voltage ripple: (a) $\Delta V_o$ =15V, (b) $\Delta V_o$ = 5V,and (c) $\Delta V_o$ = 1.5V.

### 4.1.4 Proposed Rectifier Components

Table 4.4: List of the components used in the proposed rectifier.

| Component | Value/Model |
|---|---|
| $L_1$ | 2 mH |
| $L_{o1}$ | 50 μH |
| $L_{o2}$ | 50 μH |
| $C_1$ | 1μF |
| $C_2$ | 1μF |
| $C_{o1}$ | 2200 μF |
| $C_{o2}$ | 2200 μF |
| $Q_1$ | irfb4332pbf |
| $Q_2$ | irfb4332pbf |
| $D_{o1}$ | D1N5402 |
| $D_{o2}$ | D1N5402 |

The Cuk rectifier is designed for the following power stage specifications: peak input voltage of 100V at 50 Hz, output voltage of 250V, switching frequency of 50 kHz, and output power of 125W.In addition, actual semiconductor devices are used in the simulation; D1N5402 are used for the diodes and irfb4332pbf for the power switches. The circuit components used in the simulation are chosen as follows: $L_1$ =2mH, $L_{o1}$ = $L_{o2}$= 50μH and $C_{o1}$ =$C_{o2}$= 2200μF, which are shown in table 4.4. Moreover, an equivalent series resistor (ESR) of 10 mΩ is placed in series with all the inductors.

## 4.2 Simulation Results

Simulation studies were performed using ORCAD software package, to verify the analysis results. As mentioned previously, the $C_1$ and $C_2$ values affect the input current. Thus through simulation, $C_1$ and $C_2$ are chosen to be (1μF), which is well-matched with the designing value. The input voltage and current are in-phase as shown in Fig. 4.4(a).The total harmonic distortion in the line current is 0.17% and the efficiency is 94%. The output voltage and the output current are shown in Fig. 4.4(b) and 4.4(c). The $Q_1$ is conducting over the positive half-line cycle, while the $Q_2$ conducts over the negative half-line cycle, as shown in Fig. 4.5(a) and (b). Also, it shows the voltages of $D_{o1}$ and $D_{o2}$ over the line cycle.

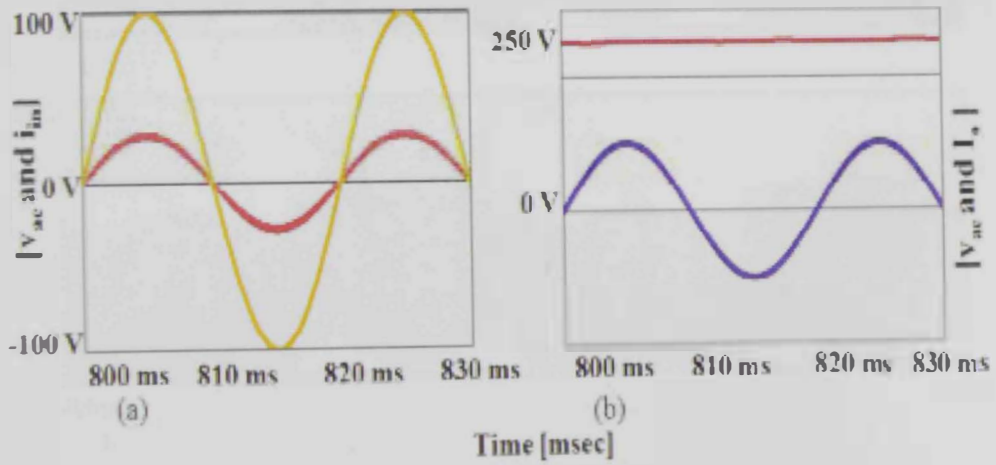



Fig. 4.4: Simulation results for the proposed rectifier: (a) Input current and voltage, (b) Output current, and (c) Output voltage.

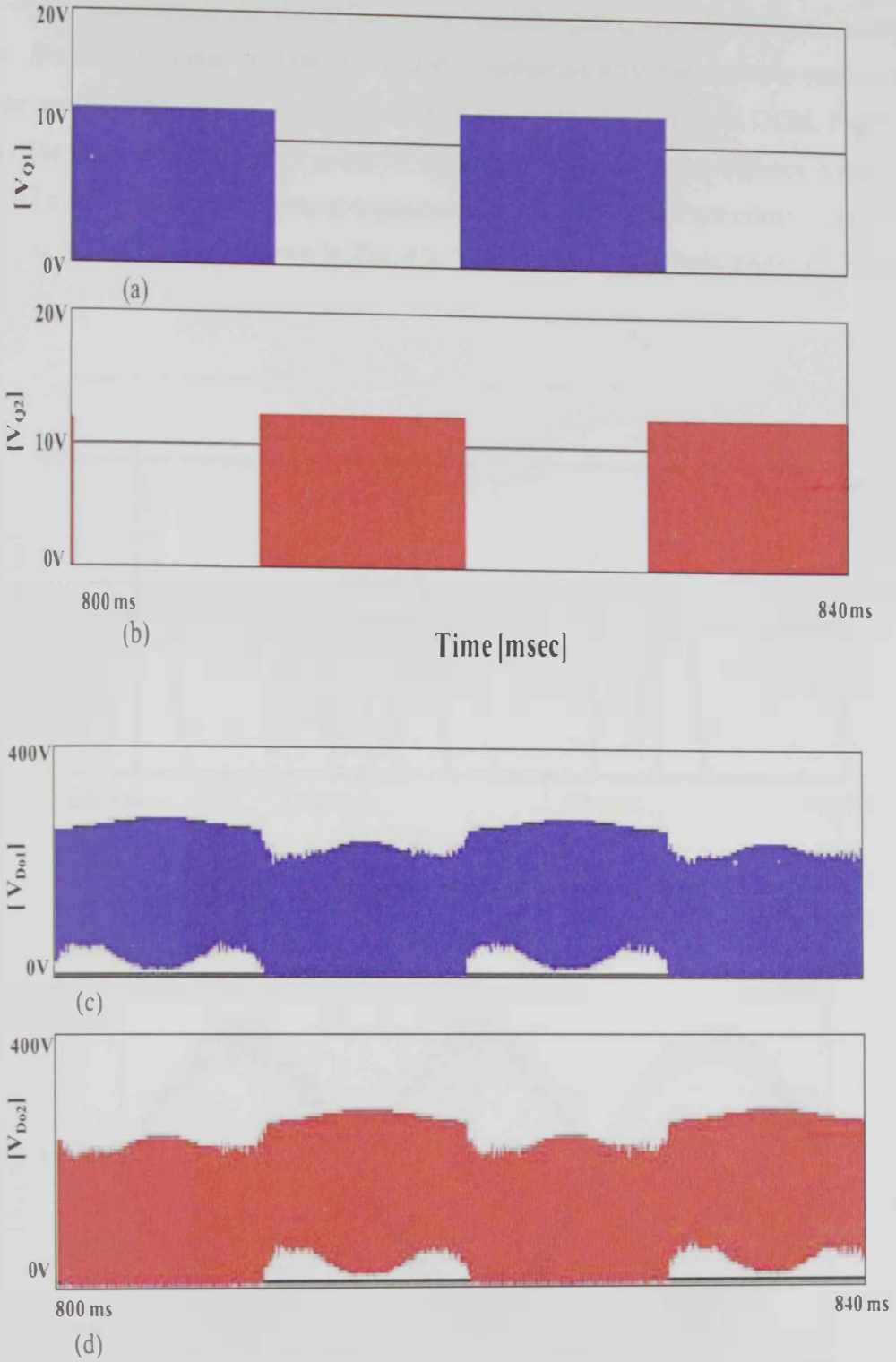



Fig. 4.5: Switching signals over the line cycle: (a)$Q_1$, (b) $Q_2$, (c) $D_{o1}$,and (d) $D_{o2}$.

Fig. 4.6 presents the diode $D_{o1}$ current and the gating signals over a switching cycle. It should be noted that the diode starts conducting after the switch is turned off and the current goes to zero before the end of the cycle which ensures DCM. Fig. 4.7 shows the capacitor voltages $V_{C1}$ and $V_{C2}$. Both voltages are in accordance with Eq. (3.1). The voltages over the output capacitors $C_{o1}$ and $C_{o2}$, which are equal to the half of the output voltage, are shown in Fig. 4.8. This proves the analysis given in Chapter 3.

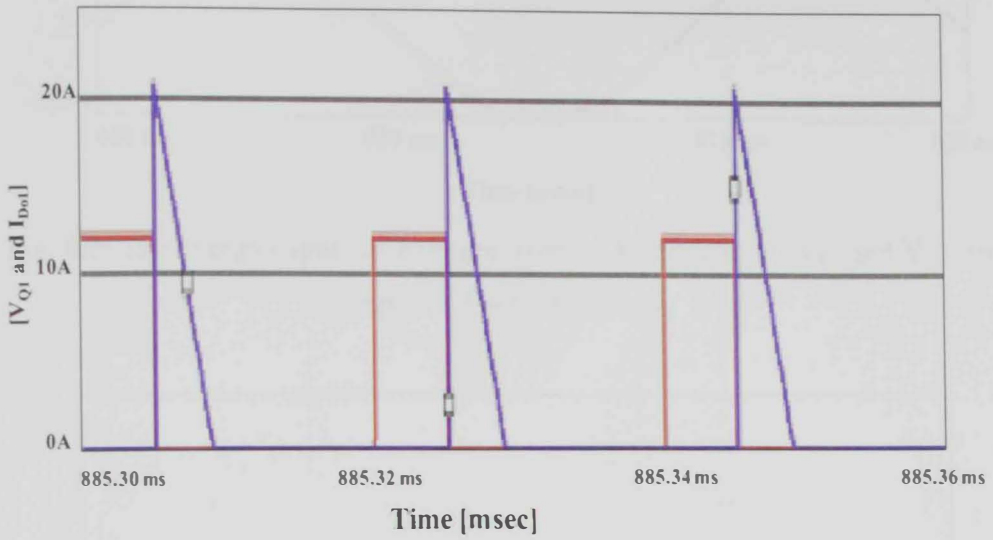
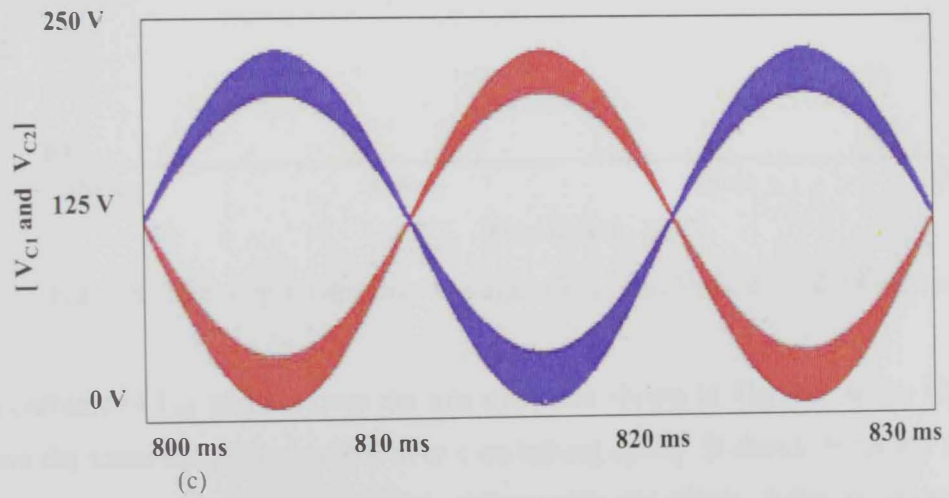



Fig. 4.6: $Q_1$ and $Do_1$ over the switching cycle.




(c)

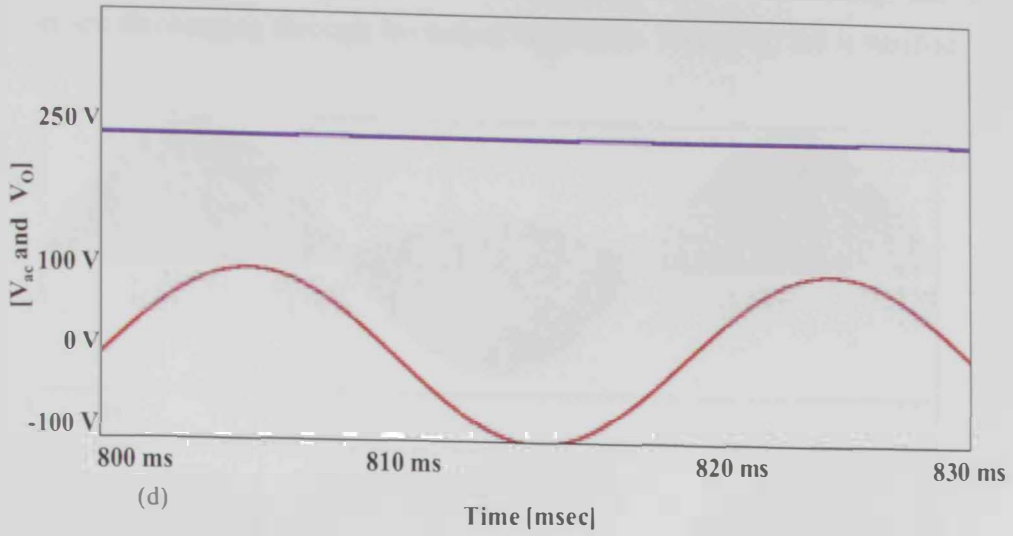



Fig. 4.7: The energy capacitor voltages over the line cycle: (a) $V_{C1}$ and $V_{C2}$, and (b) Input and output voltage.

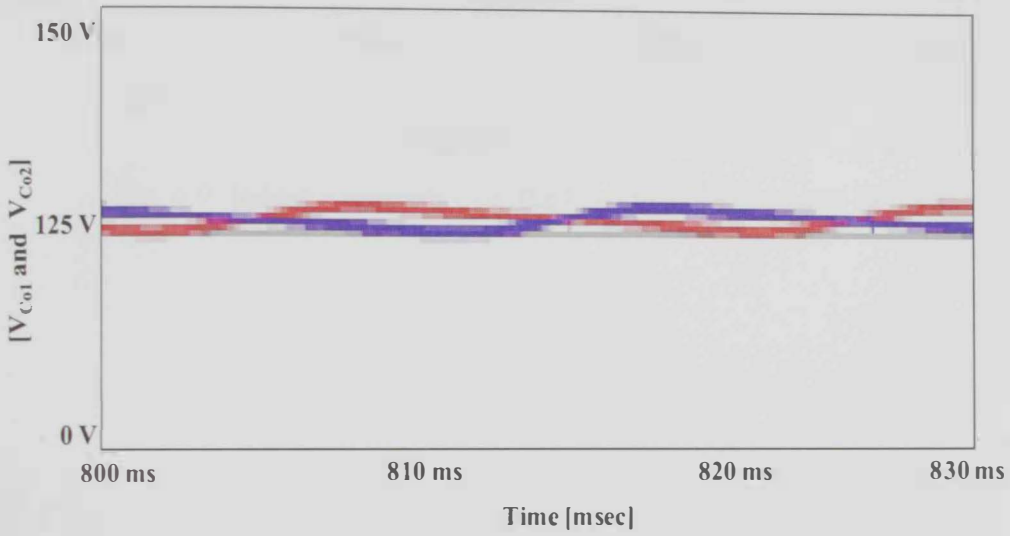



Fig. 4.8: The output capacitor voltages ($V_{Co1}$ and $V_{Co2}$) over the line cycle.

The currents of $L_{o1}$ and $L_{o2}$ over the line cycle are shown in Fig. 4.9, while Fig. 4.10 shows the three inductor currents over a switching cycle. It should be noted that the inductor currents have proportional slopes over the three different stages of a switching cycle. Thus, the three inductors can be coupled which leads to lower costs

and smaller size. In addition, the three inductors are being charged by the input voltage when $Q_1$ is conducting, but when the diode $D_{o1}$ is conducting; the three inductors are discharging through the output capacitors. Thus, Fig. 3.6 is verified.

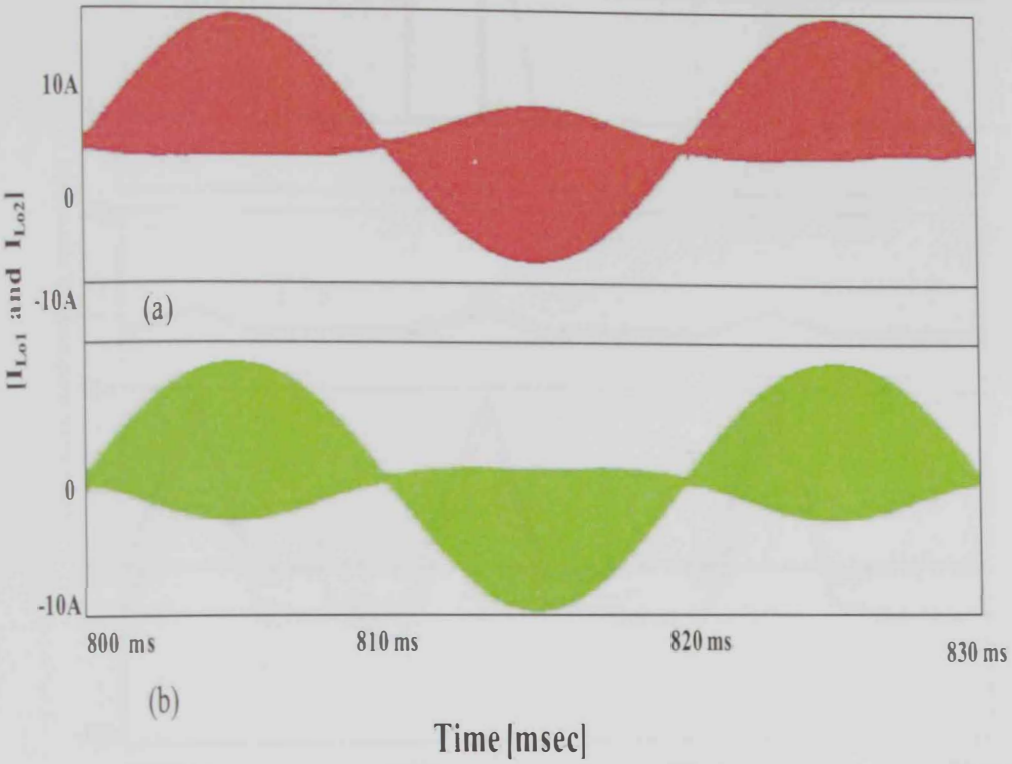



Fig. 4.9: Inductor currents over the line cycle: (a) $I_{Lo1}$, and (b) $I_{Lo2}$.

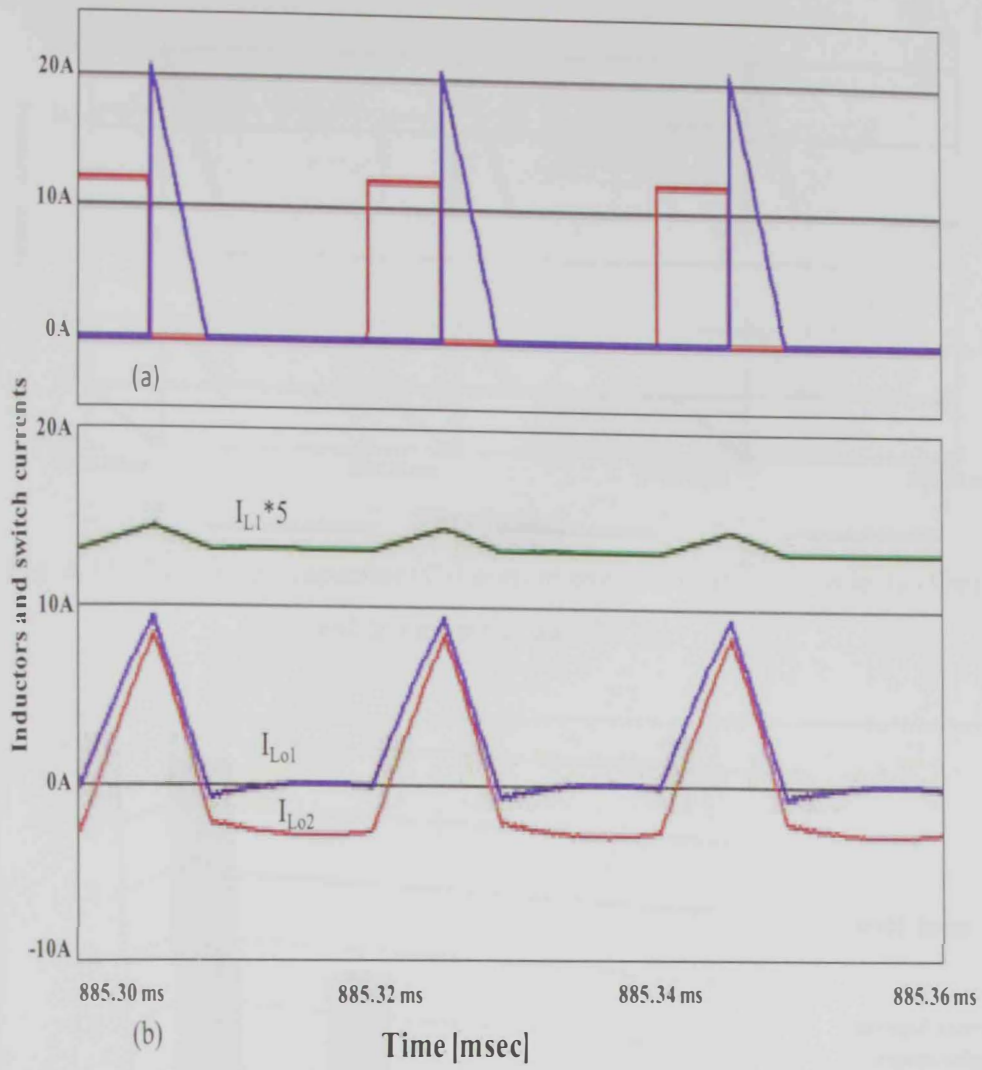



Fig. 4.10: Three inductor currents over the switching cycle.

Fig. 4.11 shows that the capacitor $C_2$ is discharging through the inductor $L_{o2}$ over the first stage when $Q_1$ is conducting. However, it is charged by the inductor $L_{o2}$ during the second stage and equals to zero over third stage which is compatible with analysis presented earlier in the chapter3. The proposed rectifier satisfies the EN 61000-3-2 regulations as shown in Fig. 4.12.

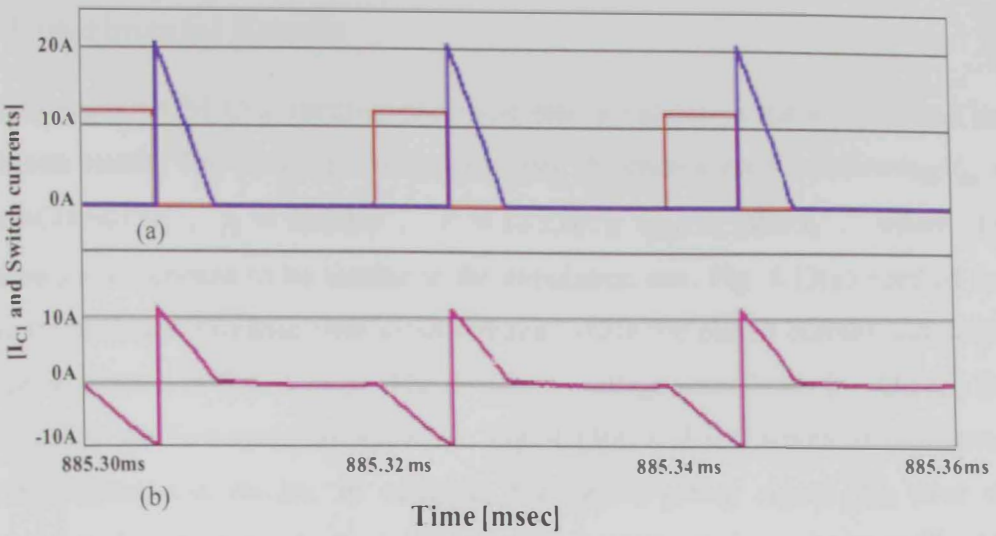



Fig. 4.11: The energy capacitor ($C_2$) current over the switching cycle: (a) Gating and diode signal, and (b) $I_{C2}$.

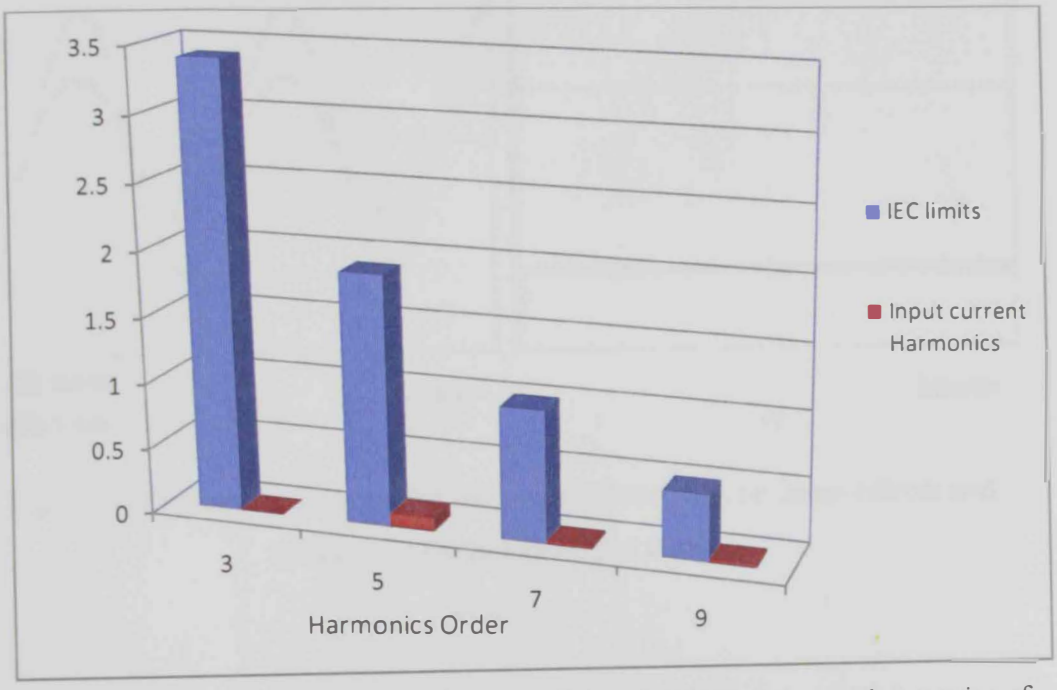



Fig.4.12: Comparison between IEC limits and simulated input current harmonics of the proposed rectifier.

## 4.3 Experimental Results

The bridgeless DCM Cuk rectifier prototype test is validating the analysis and the simulation result. The prototype is implemented depending on the following:$V_{ac} = 100\sin(2\pi 50t)\,V$ , $f_s = 50\,kHz$ , $P = 125\,W$ , $I_{ripl} \leq 10\%\, I_1$ , where the components are chosen to be similar to the simulation one. Fig. 4.13(a) verified that the input current is in-phase with input voltage, where the output current and output voltage are shown in Fig. 4.13(b). The switching voltage waveforms for: $Q_1$, $Q_2$, $D_{o1}$ and $D_{o2}$ over the line cycle are shown in Fig. 4.14(a) and (b), which are consistent with the simulation results. In addition, the switch-gating signal $V_{Q1}$ over the switching cycle, which conducts over the positive half line cycle, is shown in Fig. 15.

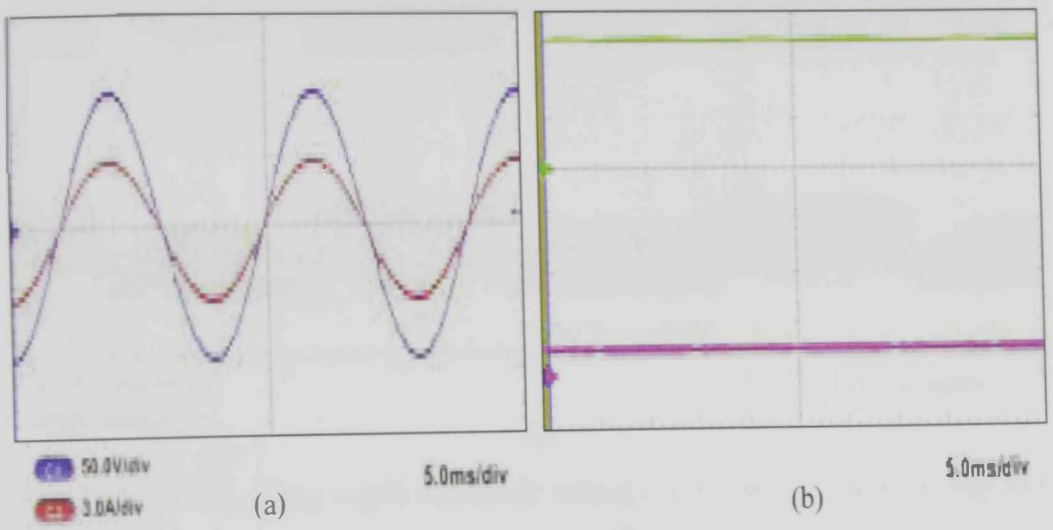
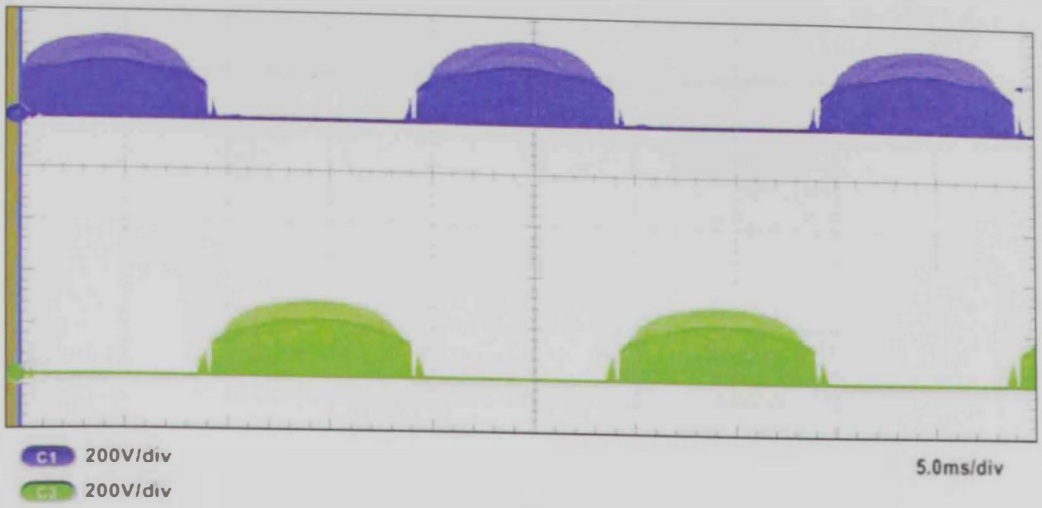
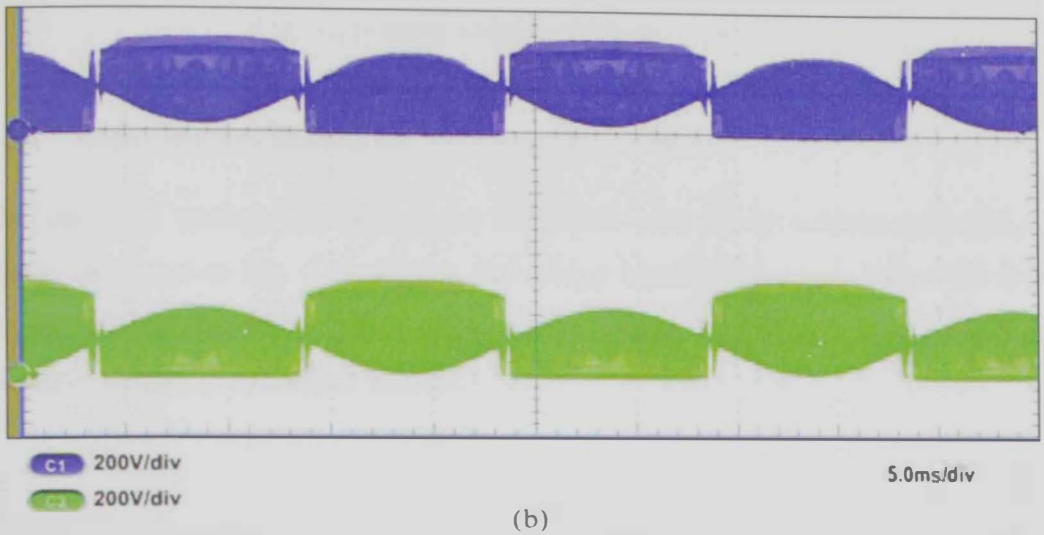



Fig. 4.13: Experimental results for the proposed rectifier: (a) Input current and voltage, (b) Output and input voltage.




(a)




(b)

Fig. 4.14: Switch-gating signal and diode voltages over the line cycle: (a) $V_{Q1}$ and $V_{Q2}$, (b) $V_{Do1}$ and $V_{Do2}$.

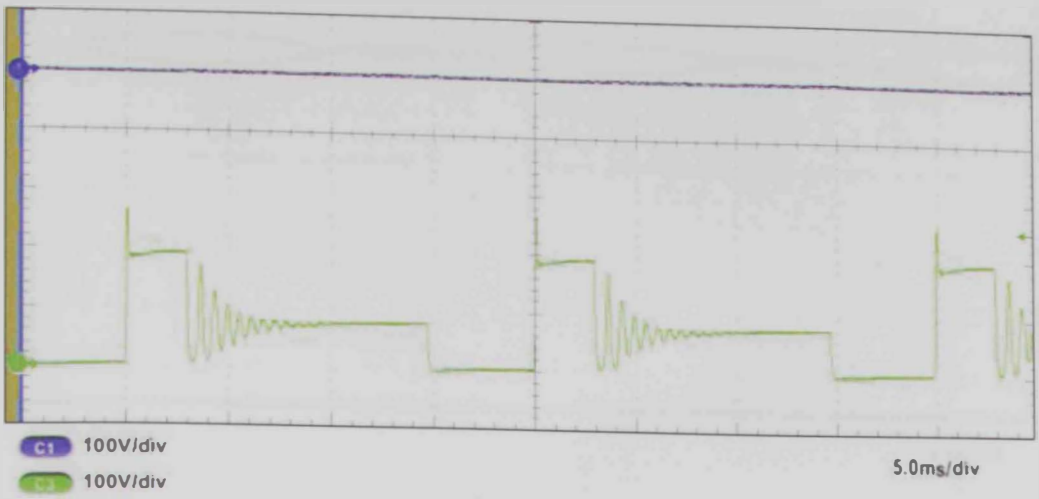
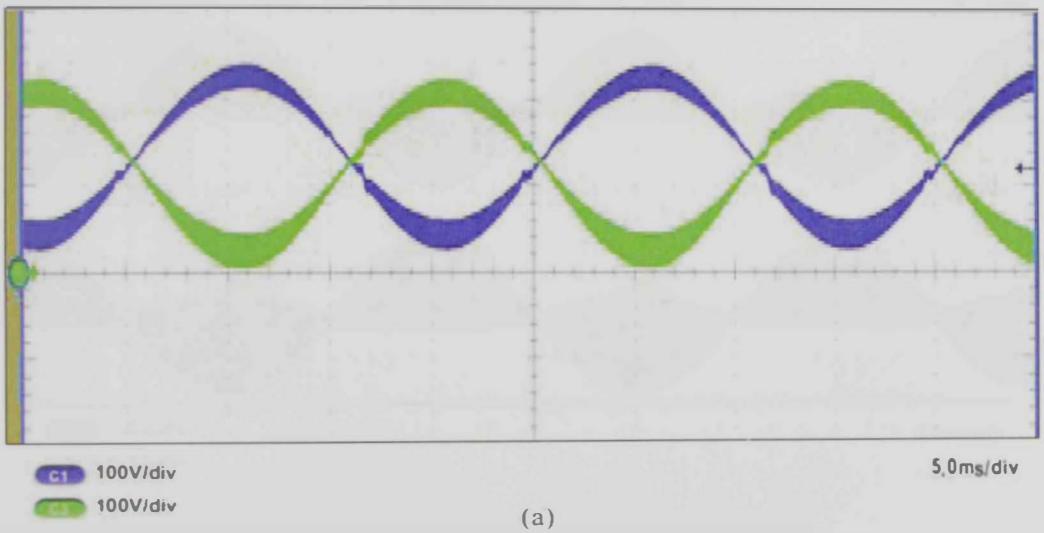


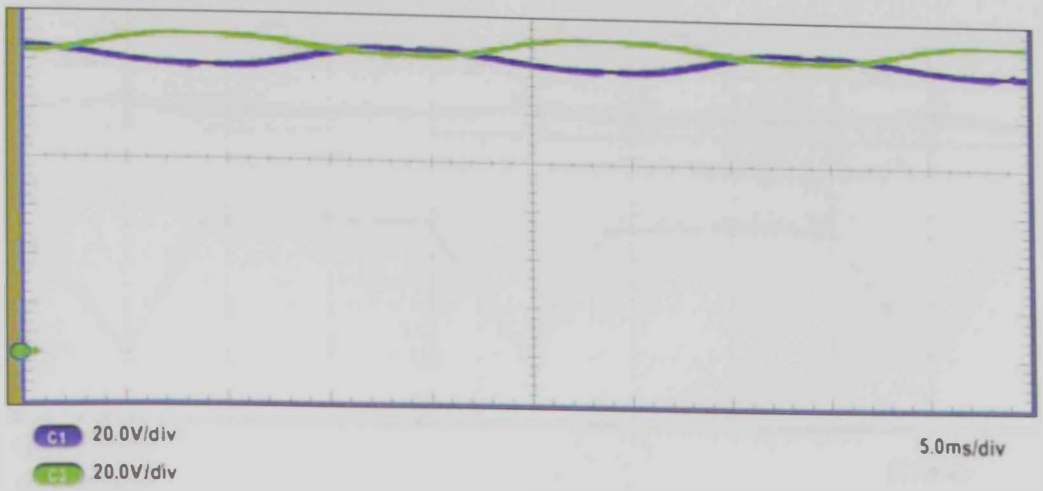

Fig. 4.15: Input voltage and Gating signal $V_{Q1}$.

### 4.3.1 Experimental Results for the Capacitor Voltages

The capacitor voltage waveforms are consistent with the simulation and analysis results as shown in Fig. 4.16. Hence, the energy capacitor voltages follow the input voltage and are shifted up by half of the output voltage. The output capacitor voltages are equal to half of the output voltage.




(a)

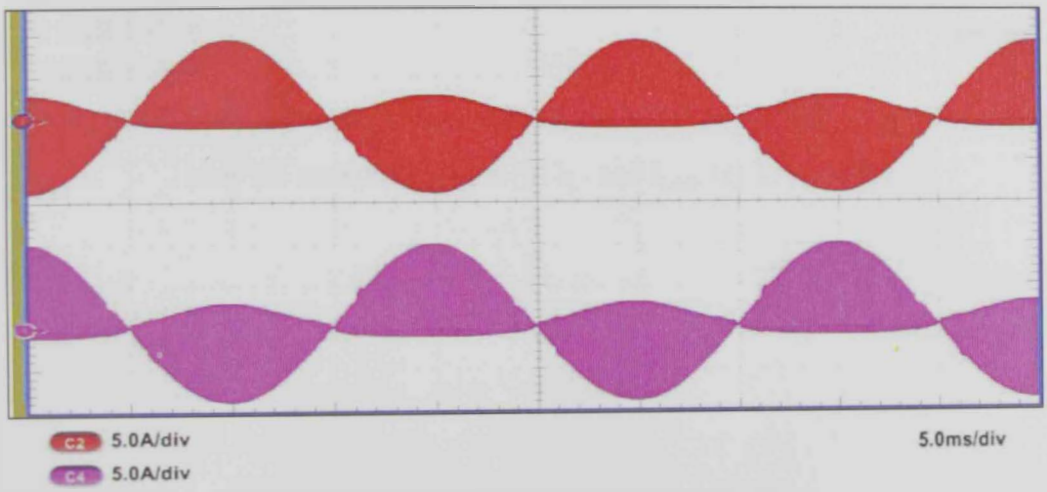



(b)

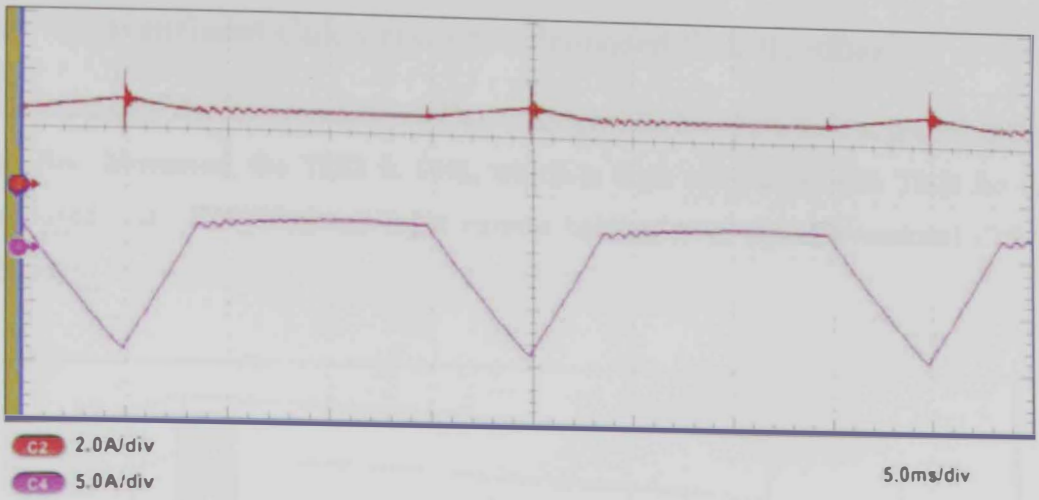
Fig. 4.16: The energy capacitor voltages and output capacitor voltages over the line cycle: (a) $V_{C1}$ and $V_{C2}$, (b) $V_{Co1}$ and $V_{Co2}$

### 4.3.2 Experimental Results for the Inductor Currents

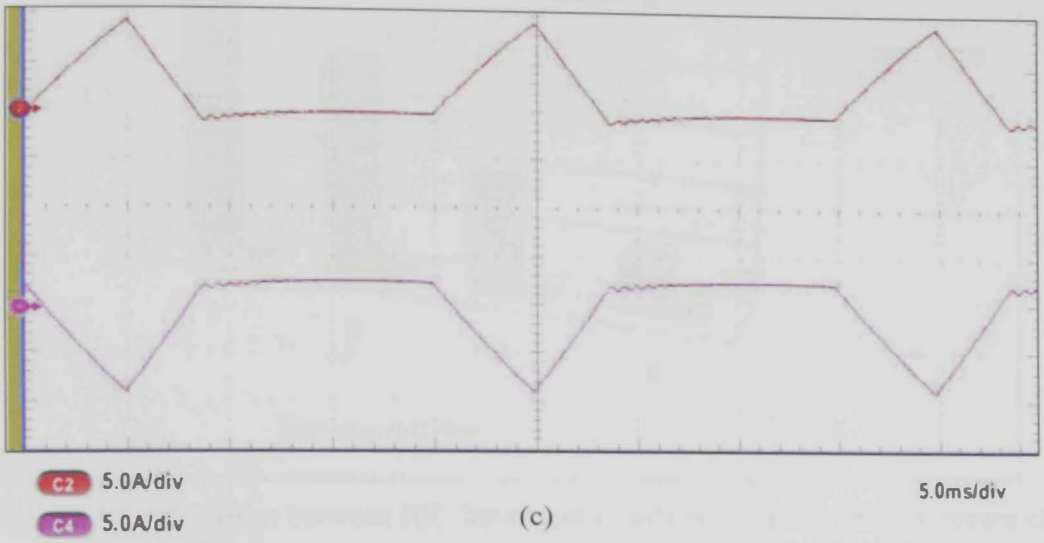
The inductor current$I_{Lo1}$ and $I_{Lo2}$ waveforms over the line cycle are shown in Fig. 4.17(a). The inductor currents $I_{L1}$ and $I_{Lo2}$ over as witching cycle are shown in Fig. 4.17(b), while Fig. 4.17(c) shows $I_{Lo1}$ and $I_{Lo2}$ waveforms.




(a)




(b)




(c)

Fig. 4.17: Inductor currents over the line cycle: (a) $I_{Lo1}$ and $I_{Lo2}$, Inductor currents over the switching cycle: (b) $I_{L1}$ and $I_{Lo2}$, (c) $I_{Lo1}$ and $I_{Lo2}$.

## 4.4 Conventional Cuk Versus the Proposed Cuk Rectifier

The efficiency for the conventional Cuk is 88% while it is 94% for the proposed Cuk rectifier. Moreover, the THD is 10%, which is high comparing with THD for the proposed Cuk. The simulated input current harmonics of the Conventional Cuk is shown in Fig. 4.18.


Fig. 4.18: Comparison between IEC limits and simulated input current harmonics of the conventional Cuk rectifier.

The comparison between the conventional Cuk and the proposed Cuk rectifier is shown in Table 4.5. The proposed bridgeless topology has fewer semiconductors in the current conduction path. However, it has one additional switch compared with the conventional Cuk. Nonetheless, the switching losses are the same because only one switch is active over a switching cycle. Also, the proposed rectifier has a floating switch which requires additional gating circuitry.

Table 4.5: Comparison between conventional and bridgeless Cuk rectifier in DCM mode.

| | Conventional Cuk | Proposed Cuk Rectifier |
|---|---|---|
| Diodes | 4 slow and 1 fast | 2 fast |
| Switch | 1 | 2 |
| Current conduction path in stage 1 | 2 slow diodes and 1 switch | 1 body diode and 1 switch |
| Current conduction path in stage 2 | 3 diodes(2 slow and 1fast) | 1 fast diode |
| Current conduction path in stage 3 | 2 slow diodes | ---------- |
| # of components | 10 | 11 |
| Integrated magnetic | One core for 2 inductors | One core for 3 inductors |
| Deriver circuit complexity | 1 non-floating | 1 floating and 1 non-floating |
| Ground | Non-floating | Floating |

# CONCLUSION AND FUTURE WORK

In this thesis, a brief PFC correction review has been presented. The advantages and disadvantages of several bridgeless topologies have been discussed. The case for a low inrush current and a continuous input/output current AC-DC rectifier has been made.

A high step-up Cuk bridgeless AC-DC rectifier has been detailed. The proposed step-up DCM bridgeless Cuk rectifier has been analyzed in DCM mode. The current and voltage stresses of the proposed topology are presented. The gain of the converter as a function of the control signal has been derived. An example of the design procedure for the converter is shown step by step. A comparison study between the full-bridge PFC Cuk rectifier and the proposed bridgeless rectifier is presented. It has been verified that the studied rectifier has fewer silicon components in the current path versus the full bridge rectifier. Hence, there are less conduction losses as well as a higher efficiency. The proposed rectifier has an efficiency of 94% versus an efficiency of 88% for the conventional rectifier.

The converter has been simulated using an ORCAD software package. The simulation results matched the analysis. Real component models have been used in the simulation. The capability of the proposed topology has been built and tested in the lab for a 125 W output power. The experimental results supported the simulation results. The input current harmonics has been compared to the EN 61000-3-2 standard requirements. The efficiency of the proposed rectifier at 125W and full load is 94% with THD being 0.17%. The input current THD is lower than the EN 61000-3-2. In addition, the rectifier is controlled by one signal. The proposed rectifier meets the requirements presented at the beginning of chapter 3.

## Future work

The proposed objectives of this research were successfully accomplished. Design a feedback controller for load voltage regulation and confirm power factor under load conditions is recommended for future work.

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# APPENDIX A

## ORCAD PROGRAM

```
Vac     1 0          sin(0 100 50)
L1      1 2          2m
RL1     2 3          0.01
C1      3 4          1u
XS1     3  10 11     irfb4332pbf
Vph     15 0         PULSE (0 12 0 1n 1n 5.u 20u)
vpl     16  0        pulse(0 1 0 1n 1n 10m 20m)
vpn     17 0         pulse(0 1 10m 1n 1n 10m 20m)
Evsp    10 11        VALUE { V(15,0)*V(16,0)}
XS2     0  12 11     irfb4332pbf
Evs2    12  11       VALUE {V(15,0)*V(17,0)}
C2      3 5          1u
Do1     0 4          D1N5402
Do2     5 0          D1N5402
L2      4 8          50u
RL2     8 9          0.01
L3      5 6          50u
RL3     6 7          0.01
Co1      7 0         2200u
R       7 9          500
Co2     9 0          2200u

**********simulation**********
*Analysis directives:
.PRObe
.TRAN 0.1u 900m 500m 0.1u UIC
******************************
.MODEL DI_PDS3200 D  ( IS=51.7u RS=11.3m BV=200 IBV=10.0u
+ CJO=630p  M=0.333 N=2.21 TT=14.4n )

.MODEL  Dmod  D  (IS=3.44523e-06  RS=0.01  N=1.99899  EG=0.965769
XTI=4 BV=200 IBV=1e-05
+  CJO=1.12334e-10  VJ=0.4  M=0.291003  FC=0.5  TT=4.54449e-08  KF=0
AF=1)
```

```
.MODEL DSTTH5L06 D (IS=494.98E-9 N=2.2603 RS=14.292E-3
IKF=.30782 CJO=127.22E-12 M=.42266
+ VJ=.3905 ISR=10.010E-21 NR=4.9950 FC=0.5 TT=24.000E-9)

.MODEL D1N5402 D(IS=2.68E-12 )
*.MODEL D1N5402 D(IS=2.68E-12 RS=0.00731 N=1.17 TT=1.44E-5
CJO=1.24E-10
*+ VJ=0.6 M=0.333 BV=266 IBV=1E-5 )

*IXKK85N60C NMOS model 600V, 85A, 35mohm, Rg=2.2 Ohm
.MODEL IXKK85N60C NMOS ( LEVEL=3 L=2.0000E-6 W=860
KP=1.0387E-6 RS=10.000E-3
+ RD=19.626E-3 VTO=3.4544 RDS=12.000E6 TOX=2.0000E-6
CGSO=11.628E-18 CGDO=729.90E-15 CBD=80.669E-9
+ MJ=1.1673 PB=3 RG=10.000E-3 IS=21.329E-6 N=2.3569 RB=1.0000E-9
GAMMA=0 KAPPA=0)


****************** IRFB4332PBF ************************
.SUBCKT irfb4332pbf 1 2 3
* SPICE3 MODEL WITH THERMAL RC NETWORK
**************************************
*       Model Generated by MODPEX     *
*       Copyright(c) Symmetry Design Systems*
*       All Rights Reserved       *
*       UNPUBLISHED LICENSED SOFTWARE   *
*       Contains Proprietary Information *
*        Which is The Property of     *
*       SYMMETRY OR ITS LICENSORS      *
*       Commercial Use or Resale Restricted *
*       by Symmetry License Agreement    *
**************************************
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
```

```
+VTO=5.2452 LAMBDA=1.44034 KP=495.593
+CGSO=5.57997e-05 CGDO=3.6051e-07
RS 8 3 0.0118129
D1 3 1 MD
.MODEL MD D IS=1.06456e-08 RS=0.00128288 N=1.36378 BV=250
+IBV=0.00025 EG=1 XTI=2.31736 TT=1e-07
+CJO=7.7726e-09 VJ=0.5 M=0.776144 FC=0.1
RDS 3 1 1e+07
RD 9 1 0.017856
RG 2 7 4.09017
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=3.36828e-09 VJ=0.5 M=0.9 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.400101 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 3.36828e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 1 0 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.400101
.ENDS irfb4332pbf

**********************************************************

.OPTIONS ITL2=200
.OPTIONS CHGTOL=10N
```

```
.OPTIONS ITL5=0 ;*TOTAL ITERATION LIMIT
.OPTIONS LIMPTS=0 ;*MAXIMUM POINT ALLOWED
.OPTIONS ITL4=100 ;*ITERATION LIMIT PER POINT
**** Real Tolerance ****
.OPTIONS RELTOL=0.001
.OPTIONS VNTOL=1E-6
.OPTIONS NUMDGT=6
.OPTIONS ABSTOL=1E-6
.four 50 I(Vac)
.END
```

# الاطروحه في سطور

الاجهزه الالكترونيه بخاصية التقويم الذاتي تستخدم على نطاق واسع في صناعة السيارات الكهربائيه، الكمبيوترات والاتصالات. ونتيجه لتلوث هذه المقومات اللاخطيه بالتوافقيات فقد وضعت معايير دوليه لحصر هذا التلوث. لذلك اصبح استخدام تقنيات معامل القدره المصححه امراً ضرورياً، لانواع كثيره من الاجهزه الالكترونيه لتلبية اللوائح والمعايير الدوليه.

هذه الاطروحه تكشف الستار عن محول كهربائي جديد بتقنية معامل القدره المصححه وبخصائص مميزه اهمها: انخفاض التداخل الكهرومغناطيسي، استخدام وحدة تحكم غير معقده والحد من سحب التيار عند التشغيل وفي حالات الحموله الزائده. هذه المزايا تجعل من البنية المقترحه حلاً مثاليا قابلاً للتطبيق في صناعة شاحن البطارية للسيارات الكهربائيه.

حيث ان الهدف الرئيسي من هذه الاطروحه الا وهو تصميم محول كهربائي ذو كفاءه عاليه يلبي المعايير الدوليه و يستخدم كشاحن بطاريه ذو جهد عالي قد اثبت بثلاث طرق مختلفة. اولاً: بالتحليل الرياضي المنطقي للدائره الكهربائيه. ثانياً: باستخدام برنامج المحاكاه ORCAD. ثالثاً: عملياً وذلك بصنع المحول الكهربائي واختبار فعاليته داخل المختبر. وقد كانت النتائج متطابقه تماماً. وقد اثبتت المقارنه بين المحول المقترح والمحول الموجود، ان المحول المقترح يتميز بكفاءه أعلى وخصائص أفضل.

وفي الختام، اسأل المولى عز وجل التوفيق والسداد ، وان يجعل من هذا العمل بداية لمستقبل افضل ويعم نفعه على المجتمع.

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كلية الهندسة
برنامج ماجستير الهندسة الكهربائية

# محول كهربائي لرفع الجهد بكفاءه عاليه لتطبيقات الجهد العالي

رسالة مقدمة من الطالبة
عائشة كميدش الكعبي

إلى
جامعة الامارات العربية المتحدة
استكمالا لمتطلبات الحصول على درجة الماجستير
في الهندسة الكهربائية

أشراف
الدكتور عباس فردون



يونيو ٢٠١٢