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Wide-Gain Range Bridgeless PFC Modified SEPIC Rectifier

Ahmed Mohammed Ahmed Al Gabri

United Arab Emirates University

College of Engineering

Department of Electrical Engineering

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Ahmed Mohammed Ahmed Al Gabri

This thesis is submitted in partial fulfillment of the requirements for the Master of Science in Electrical Engineering degree

Under the direction of Dr. Abbas Fardoun

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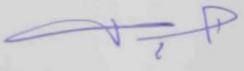
DECLARATION OF ORIGINAL WORK

I, Ahmed Al Gabri, the undersigned, a graduate student at UAE University and the author of the thesis titled "Wide-Gain Range Bridgeless PFC Modified SEPIC Rectifier" hereby solemnly declare that this thesis is an original work done and prepared by me under the guidance of Dr. Abbas Fardoun, in the college of Engineering at UAEU. This work has not been previously formed as the basis of the award of any degree, diploma or similar title at this or other university. The materials included in my thesis have been referenced and acknowledged.

Student's signature



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Thesis Examination Committee:

1) Advisor: Dr. Abbas Fardoun

   Title: Associate Professor

   Department: Electrical Engineering

   Institution: College of Engineering, UAE University

   Signature _____ Date 30/1/2014

2) Co-advisor: Prof. Esam Ismail

   Title: Professor

   Department: Electrical Engineering

   Institution: College of Technological Studies, Kuwait

   Signature E. Ismail Date 30/1/2014

3) Member: Dr. Ala Hussein

   Title: Assistant Professor

   Department: Electrical Engineering

   Institution: UAE University

   Signature _____ Date 30/1/2014

4) External Examiner: Prof. Francisco Javier Sebastian Zuñiga

   Title: Professor

   Department: Electrical Engineering, Electronic Computers and Systems Engineering

   Institution: University of Oviedo, Spain

   Signature _____ Date 30/1/2014

Accepted by

Master's Program Director Dr. Abbas Fardoun .....

Signature: _____ Date: 30/1/2014

Prof. Amr El - Dieb

Dean of the College.....

Signature: _____ Date: 9/3/2014

9/3/2014

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ABSTRACT

With the increasing demand for power from the ac line and more strict limits for power quality, power factor correction has gained great attention in recent years. All basic power converter topologies, such as Boost, Buck, Buck-Boost, and their variations, can be used to realize active PFC techniques.

In this research, a new bridgeless rectifier that operates with high power factor and high efficiency is investigated targeting LED and battery charging applications. The new topology is a high-power-factor rectifier, which is suitable for universal line base on a modified version of the single-ended primary inductance converter (SEPIC) operating in Discontinuous Conduction Mode (DCM). The new configuration also allows the reduction of the losses associated to the diode reverse recovery current. Furthermore, the proposed topology has wider gain than classical full bridge SEPIC converter, higher efficiency and lower current harmonics.

Small signal analysis is used to model the variation affecting the rectifier circuit. Current Injected Equivalent Circuit Approach (CIECA) is utilized in modeling the small signal transfer function of the converter. Feedback control is applied to regulate output voltage around the desired reference and to reduce the effect of disturbances. Simulated results of the output voltage as function of input voltage disturbance and load change are presented.

The proposed topology is simulated using PLECS, PSPICE and MATLAB. In addition, a 200W prototype is built and tested to validate analysis and simulation. Comparison between simulation and experimental results is also presented.

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ABBREVIATIONS

PFC: Power Factor Correction

CCM: Continuous Current Mode

DCM: Discontinuous Current Mode

DC: Direct Current

AC: Alternate Current

IEC: International Electro-technical Commission

THD: Total Harmonic Distortion

PF: Power Factor

RMS: Root Mean Square

EMI: Electromagnetic Interference

PWM: Pulse Width Modulation

NOMENCLATURE

I_1	RMS value of the fundamental component of the input current
I_o	DC component of the input current
I_n	nth component of the input current
θ_i	The phase angle of the fundamental component of the current.
φ_v	The phase angle of the AC input voltage.
$d_1(t)$	Duty cycle at stage 1 of the switching cycle
$d_2(t)$	Duty cycle at stage 2 of the switching cycle
$d_3(t)$	Duty cycle at stage 3 of the switching cycle
$v_{ac}(t)$	Input voltage
V_M	Peak amplitude of input voltage
f_s	Switching frequency
T_s	Switching cycle
$v_{C1}(t)$	Capacitor C_1 voltage
$v_{C2}(t)$	Capacitor C_2 voltage
$v_{C3}(t)$	Capacitor C_3 voltage
$v_{Co}(t)$	Output capacitor voltage
$i_{C1}(t)$	Capacitor C_1 current
$i_{C2}(t)$	Capacitor C_2 current
$i_{C3}(t)$	Capacitor C_3 current
$i_{Co}(t)$	Output capacitor current
$v_{L1}(t)$	Inductor L_1 voltage
$v_{L2}(t)$	Inductor L_2 voltage
$v_{Lo}(t)$	Output inductor voltage
$i_{L1}(t)$	Inductor L_1 current
$i_{L2}(t)$	Inductor L_2 current
$i_{Lo}(t)$	Output inductor L_o current
$v_{D1}(t)$	Diode D_1 voltage
$v_{D2}(t)$	Diode D_2 voltage

$v_{Do}(t)$	Output diode D_o voltage
$i_{D1}(t)$	Diode D_1 current
$i_{D2}(t)$	Diode D_2 current
$i_{Do}(t)$	Output diode D_o current
$v_{Q1}(t)$	Switch Q_1 voltage
$v_{Q2}(t)$	Switch Q_2 voltage
$i_{Q1}(t)$	Switch Q_1 current
$i_{Q2}(t)$	Switch Q_2 current
M	Conversion ratio
I_x	Inductor L_1 current during stage three
I_y	Inductor L_2 current during stage three
I_z	Inductor L_o current during stage three
I_{Do}	Average diode current over half-line cycle
$\overline{i_{Do}}$	Average output diode D_o current over a switching cycle
$i_{in}(t)$	Input current
$i_o(t)$	Output current
K	Dimensionless coefficient
$K_{critical}$	Critical coefficient at the boundary between DCM and CCM.
R_e	Emulated resistance
$M(d_1, K)$	Conversion ratio in terms of duty cycle and coefficient K
$\langle v_{Q1}(t) \rangle_{Ts}$	Average switch Q_1 voltage over a switching cycle
$\langle v_{in}(t) \rangle_{Ts}$	Average input voltage over a switching cycle
$\langle v_{Do}(t) \rangle_{Ts}$	Average output diode D_o voltage over a switching cycle
$\langle v_{C1}(t) \rangle_{Ts}$	Average capacitor C_1 voltage over a switching cycle
$\langle i_{Q1}(t) \rangle_{Ts}$	Average switch Q_1 current over a switching cycle.
$\langle i_{Do}(t) \rangle_{Ts}$	Average output diode D_o current over a switching cycle.
T_{OLo}	Uncompensated loop gain DC gain
ω_o	System pole

CHAPTER 1

Introduction

In recent times, the increase use of rectifiers in electrical equipment such as computers, laptops, uninterruptable power supplies, telecommunications and bio-medical equipment has become uncontrollable as its growth is rising exponentially. Unwanted produced harmonics by these rectifier circuits are injected into the power grid which results in many undesirable effects [1]. To overcome this problem, some international standards like IEC 61000-3-2 are introduced to control design of these rectifiers to meet specific harmonics percentage [2]. Most of the power supplies use conventional rectifier with a large filter capacitor at the end of rectification. This causes excessive peak current, high harmonic distortion and low power factor [1-12]. With this increasing demand for power from the ac line and more strict limits for power quality, power factor correction has gained great attention. A variety of circuit topologies and control methods have been developed for the PFC application [3-10]. All these converters can be used in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM).

1.1 Motivation

In general, off-line switching-mode power supply shown in Figure. 1.1 consists of the utility power source and a switched-mode power supply, which provides a regulated DC power for the electric appliances and equipment by using a rectifier that convert AC input voltage into DC voltage. In addition, a harmonics filter capacitor and a switching power converter are used to improve the rectified DC voltage [26-

30]. However the conventional AC/DC power supply will generate impulsive current with high harmonics distortion due to the interaction between diode rectifier and capacitor filter [3-10] [26-30].

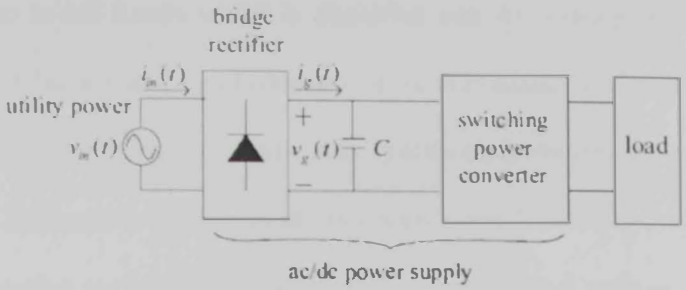

Figure 1.1: Off-line switching-mode power supply.

This causes the power factor to degrade, and thus leads to the increase of the current flowing to the load. Energy losses on the power transmission lines thus increase. Hence, the power company requires customers to maintain the high power factor of their respective loads. Moreover, engineers often consider power factor as a figure of merit to measure the efficiency of the power transmission [20]. As a result, the need to eliminate high harmonics distortion to increase the power factor of a power supply system becomes a significant issue of energy savings and electricity quality promotion. On the other hand, the switched-mode power supply, operating at higher frequency for power conditioning, can reduce its size and keep cost down [3-11]. However, higher switching frequencies result in more switching losses and thus lower the power efficiency. To overcome these drawbacks, the soft switching technique is thus applied to reduce the switching losses [9-10]. The main aim of this thesis is to design PFC rectifier with high power factor and high power efficiency that will reduce pollution on AC lines.

1.2 Electrical loads classifications

In general, electrical loads could be classified according to different criteria. They can be dived into two main sub-groups according to current or voltage fed to them. The first group is AC Loads which is classified into AC voltage loads such as (ac voltage BUS, induction and synchronous motors in constant speed applications) and AC current loads such as (induction and synchronous motors in constant torque applications). AC loads are fed from utility mains using AC-AC cycloconversion that involves converting an AC input voltage to a desired output voltage of controllable magnitude and frequency or using DC-AC inverter if the source is DC such as batteries or solar cells. On the other hand, DC Loads are the second group such as (LED-based lighting, computers and radio). DC loads are classified into DC voltage loads such as (DC motor in constant speed applications, batteries during charging) and DC current loads such as (DC motor in constant torque applications) [27-28]. DC loads are fed from the utility mains using AC-DC rectifiers that convert the AC voltage into a desired DC voltage or they could be fed from DC sources using voltage regulators (DC-DC) converters which convert the source DC voltage to the desired load DC voltage. The main concern in this thesis is the AC-DC rectifiers that are used to supply DC electronic appliances with DC voltage. From an energy saving point of view, a switching power rectifier is required to exhibit high power factor and high power efficiency. Accordingly, many researches have been focusing on designing and developing power rectifiers that can deliver the required power with higher power factor, higher efficiency, lower cost, lower harmonic distortion and lower losses [3-26]. Furthermore loads could be divided into linear loads such as (Resistive,

Capacitive and Inductive) and non-linear loads (such as computers, laser printers, rectifiers, PLC, electronic ballast, refrigerator, TV etc). In linear loads, the voltage and current waveforms are sinusoidal and the current at any time is proportional to the voltage. Circuits containing purely resistive heating elements (filament lamps, cooking stoves, etc.) have a power factor of 1.0 which means that the current is following the voltage without any phase shift as shown in Figure 1.2. Circuits containing inductive or capacitive elements (electric motors, solenoid valves, lamp ballasts and others) often have a power factor below 1.0 [24-27].

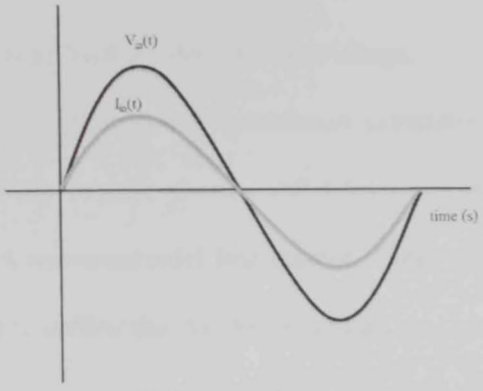

Figure 1.2: Purely resistive linear load.

With the development of high-tech industry, most of the electric appliances are nonlinear. The nature of non-linear loads is to generate harmonics in the current waveform as illustrated in Figure 1.3. This distortion of the current waveform leads to distortion of the voltage waveform. Under these conditions, the voltage waveform is no longer proportional to the current. A detailed discussion on the influence of the nonlinear loads is explained in the following section.

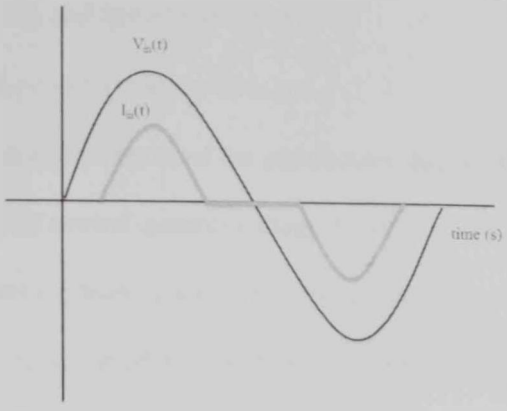

Figure 1.3 Non-linear load

1.3 The effect of a nonlinear load on the AC line voltage.

Electronic equipment such as communication, computers and its accessories (printers and fax machines), mobile phones and televisions which are considered nonlinear load produces a non-sinusoidal line current. These nonlinear load currents have a high harmonics that pollute the AC mains and affect surrounding linear loads [1-30]. Most of the electronic equipment connected to the electricity power grid draws high peak discontinuous non-sinusoidal line current rather than smooth sine wave current. This current is composed of number of harmonic currents, which flow through electricity power grid as well as in the equipment itself. Therefore, the system efficiency and power factor are reduced, and the harmonic content in the AC line current is increased, which has negative impacts such as [24-30]:

- Interference with other equipment.
- Overheating of distribution system equipment.
- Distortion of system voltage wave-form.
- Electromagnetic interference (EMI) problems.

- Overheating and fail of transformer.
- Affecting power system protection.
- Increase the resistances of the conductors due to skin effect and cause an abnormal neutral-ground voltage difference.

To avoid harmonics effects, a lot of researches were conducted on harmonics generated by rectifier circuits used for electronic equipment. To minimize current harmonic levels power factor correction techniques is used and developed [3-30]. In addition, International Standards such as EN 61000-3-2 have been placed to limit input current harmonics. There are four different classes in this standard, which have different limit values. Table 1.1 shows a summary of these classes. Therefore, the design of PFC rectifier circuits depends on the applications classes where each class has a percentage of harmonics limitation that can't be exceeded.

Table 1.1: Classification of EN-6100-3-2 standard [2]

Class	Applications
Class A	Balanced three-phase equipment Single-phase equipment not in other classes
Class B	Portable power tools
Class C	All lighting equipment
Class D	Single-phase, below 600 Watts

1.4 Power factor correction techniques

Due to the spread of non-linear loads in the power systems, current and voltage harmonics are produced and affect the power grid. Therefore, the undesired distortions should be compensated to minimize their effects on the distribution system and as a result the efficiency will be improved. Several methods and approaches are

used nowadays to improve the power factor and to meet the international line harmonics' regulations. The most commonly used methods are passive and active approach [28].

In passive PFC approach, an L-C filter is introduced between the AC line and the input port of the diode rectifier of AC-DC converter. This filter causes the harmonic current to be decreased, which means that the nonlinear device becomes more linear [21-26] [28-32]. However, the line current will be drawn from the input at only the peak of the sinusoidal line voltage, resulting in the "peaky" input line current that causes line harmonics On the other hand, in active PFC converter techniques, power electronics DC-DC converter is used and operated at high frequency to shape the input line current and make it follow the input voltage waveform. The most common used topologies as DC-DC converter in active PFC converter are Boost, Buck-Boost, Flyback, Cuk, ZETA or SEPIC topologies presented in [31]-[33], [45], [30] and [61]. Buck and Buck derived converters, such as Forward, Half-Bridge, Full-Bridge and Push-Pull can be used to comply with some standards regarding low-frequency harmonics in the line, but they cannot be used as ideal PFC, because sinusoidal line current cannot be achieved using these converters. Furthermore, in active PFC approach, the input power factor can reach approximately unity and the rectifier input interface of power converter emulates a pure resistor which means that input current follows input voltage [15-23]. The active PFC methods have many advantages over the passive PFC techniques such as almost unity power factor, harmonics reduction and size and weight reduction. Hence this research is focused on

the area of active PFC converter to achieve near unity input power factor and hence to decrease harmonic distortion.

The PFC control methods are classified into two groups: Active control and Automatic control of line current. Active control method is associated with CCM of the inductor current, so it is referred as CCM shaping technique. On the other hand, the automatic control is used when converter operates in DCM [24-30]. For medium and high power applications, CCM is suitable because of low EMI and better input current waveform. The DCM method is employed for low power applications, i.e. 300 W or less [3-8].

1.5 Thesis objectives:

The main goal of this thesis is to design a New Bridgeless power factor rectifier topology that can:

- Minimizes the switching losses.
- Achieves nearly unity power factor.
- Maximizes the efficiency.
- Produces high gain at moderate Duty Cycle.
- Operates at universal-line voltage ranges (90-260V_{rms}).
- Minimize input/output current ripple (reduce EMI effects)

1.6 Thesis structure

This thesis is divided into eight chapters. Chapter 1 presents an introduction to the main objectives of the thesis and shows the motivation behind developing existence rectifiers in order to reduce Ac pollution. An extended literature review on several fundamental factors has been considered for the improvement of rectifiers operation. Chapter 3 focused on the steady state analysis of the proposed rectifier and the DCM

operation of the rectifier and its advantages over CCM. After that, in chapter 4, the components of the proposed rectifier circuit will be designed according to the analysis of chapter 3; these components will be designed to ensure that circuit on operating in DCM. Moving to chapter 5, a small signal model of the rectifier will be built using current injected approach since the circuit is operating in DCM, then according to the model a feedback control will be designed to regulate the output voltage around a set point. Next, a comparison between simulation and experimental result at specified operating point are conducted in chapter 6. A comparison between the proposed circuit and a full-bridge topology are presented in chapter 7. Finally, a summary of the work done is presented in chapter 8.

CHAPTER 2

Literature Review

2.1 Power factor and harmonic distortion

Presently, there is increasing demands of unity power factor and low total harmonic distortion of the current drawn from the power utility. Significant efforts have been made for the improvements of the PFC converters. Power factor correction rectifiers' main objective is to shape the input current of power supplies in order to maximize the real power available from the mains [3-9]. Ideally, the electrical appliance should present a load that emulates a pure resistor; therefore the reactive power drawn by the device will be zero. The input current harmonics will be reduced because the current is following the input voltage profile and is exactly in phase with it. Furthermore, the current drawn from the mains to meet the load requirement will be reduced; as a result the losses (I^2R) and costs associated will be minimized. The reduction of harmonics will also reduce the interference with other devices that are being powered by the same source [24-30]. Power factor correction is simply defined as the ratio of real power to apparent power:

$$PF = \frac{\text{Real Power (Watts)}}{\text{Apparent Power (VA)}} \tag{2.1}$$

Where the real power is the average value (averaged in a line period) of the instantaneous product of current and voltage and the apparent power is the product of the rms value of current and the rms value of voltage [28].

For linear load (resistive, inductive and capacitive) the power factor is one, if both current and voltage are sinusoidal and in phase which is the ideal case. The power factor is the cosine of the phase angle between voltage and current if both of them are sinusoidal and not in phase [26-28]. A unity power factor implies that 100% of the current is contributing to power in the load while a power factor of zero indicates that no current is feeding the load. On the other hand, the general equation governing power factor relation in switched-mode power supplies which present non-linear impedances as a result of the input circuit which consists of half wave or full wave bridge rectifier [26-28]:

$$power\ factor = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{\left(I_o^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2} \right)}} \right) \left(\cos(\varphi_v - \theta_i) \right) \qquad (2.2)$$
$$= (Distortion\ factor)(Displacement\ factor)$$

Where:

I_1: RMS value of the fundamental component of the input current.

I_o: DC component of the input current.

I_n: nth component of the input current.

θ_i: The phase angle of the fundamental component of the current.

φ_v: The phase angle of the AC input voltage.

Distortion factor is defined as the ratio of the rms fundamental component of the current and the total rms value of the current, while displacement factor is defined as the cosine of the angle between the fundamental components of the voltage and current waveforms [28]. It is known that higher power factor leads to lower

harmonics. In the case of switch-mode power supplies the displacement factor is almost unity, so the relationship between harmonic distortion and power factor is:

$$THD(\%) = \frac{\sqrt{\sum_{p=2}^{\infty} I_p^2}}{I_1} \qquad (2.3)$$

$$PF = \frac{1}{\sqrt{1 + (THD)^2}} \qquad (2.4)$$

Where THD represents the total Harmonic Distortion which is the ratio of the rms value of the waveform not including the fundamental, to the rms fundamental magnitude.

2.2 Circuit operation modes

Since the 80's, several power factor correction topologies have been proposed such as Boost, flyback, Buck, SEPIC, Cuk and ZETA converters. These topologies could be used in either DCM or CCM according to the application. It is known that a DC-DC converter operates in CCM, if inductor current never reaches to zero or kept constant within part of the switching cycle, while it operates in DCM, if inductor current reaches zero or remains constant for part of the switching period. For higher power level applications, CCM operation mode is preferred while the DCM operation mode is used in applications of less than 300 watts [34-38]. The proposed topology is designed to work in DCM to achieve almost unity power factor and low THD of input current. Furthermore, the DCM operation gives additional advantages such as: zero current turn-on in the power switches, zero-current turn-off in the output diode, and reduces the complexity of the control circuitry [7-8]. Furthermore, the Boost, Buck-Boost, Cuk and SEPIC converters operating in DCM have the automatic "voltage

follower" property which means that the input current naturally follow the input voltage profile and thus achieve a sinusoidal input current [38-40]. Therefore, it is possible for these circuits to use one control loop at the output (voltage or current) to achieve a unity power factor.

2.3 PFC rectifiers' topologies

As mentioned before many PFC rectifier topologies have been proposed. In this section several topologies will be discussed and the advantages and disadvantages of them will be shown.

2.3.1 Boost PFC rectifier

The PFC Boost rectifier is the most well-known topology because of its low cost and high performance in terms of efficiency and simplicity. Boost rectifier is shown in Figure 2.1. The Boost converter is the common power conditioning interface [36-38] [42-44]. Conventional Boost PFC converters are composed of a full bridge AC to DC diode rectifier followed by a Boost converter. It's a nonlinear load because two diodes of the bridge rectifier lie in the direct power path for either the positive or negative half-cycle of the input ac line voltage. The Boost converter contains basically a diode, a transistor as switch and at least one energy storage element. Capacitors are generally added to output so as to perform the function of reducing output voltage ripple and sometimes inductors are also combined with. Full bridge Boost rectifier has many advantages such as: continuous input current due to the existence of input inductor, low voltage- and current-stress, high performance in terms of efficiency, voltage step-up capability and simple structure [7-9][24-28][36-

38]. Although Boost PFC rectifiers has many advantage, several disadvantages are affecting the extent of Boost rectifiers such as: production of high gain at narrow duty cycle, high losses due to diode bridge, higher DC output voltage than the peak input voltage which limits Boost usage in high voltages (above input line voltage), difficult implementation of input-output isolation and high start-up in-rush current [3-9].

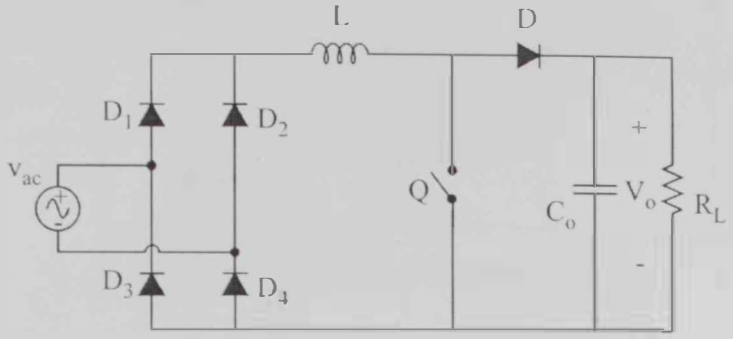

Figure 2.1: Conventional Boost rectifier.

2.3.2 SEPIC PFC rectifier

Several topologies have been proposed to compensate for the disadvantages of PFC Boost. SEPIC rectifier displayed in Figure 2.2 is one of the famous rectifiers that can replace Boost rectifiers due to their advantages such as: the output voltage of SEPIC converter can be either higher or lower than the input voltage so SEPIC offer voltage step up and step down properties which makes it suitable in wide output voltage range applications. Moreover, SEPIC offers easy implementation of transformer isolation and inherent in-rush current limitations during the startup and overload conditions [7-8] [17] [45-47]. Furthermore, by observing Figure 2.2 the two inductors can be coupled in the same magnetic core, therefore the input current ripple can be reduced theoretically to zero which will leads to reduction in the input filter (theoretically eliminated) [9-10, 47]. However, SEPIC topology compared to Boost

topology, has the following disadvantages: High losses due to diode bridge, high output ripple because of the discontinuous output current and the voltage and current stresses on the active and passive switches are high.

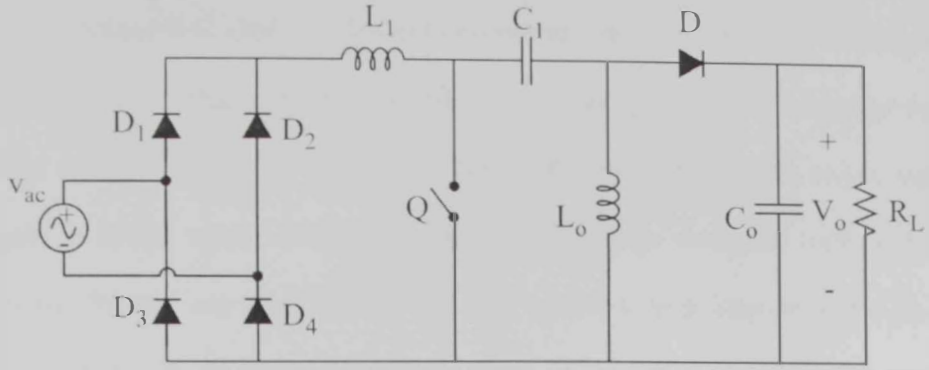

Figure 2.2: Conventional SEPIC rectifier.

2.3.3 Modified SEPIC rectifier

Since SEPIC PFC rectifier has plenty of advantages, a lot of researches have been conducted on SEPIC topology to come up with a rectifier that has high efficiency, lower harmonic distortion and almost unity power factor. A high-power-factor rectifier suitable for universal line based on a modified version of SEPIC is shown in Figure 2.3 [8].

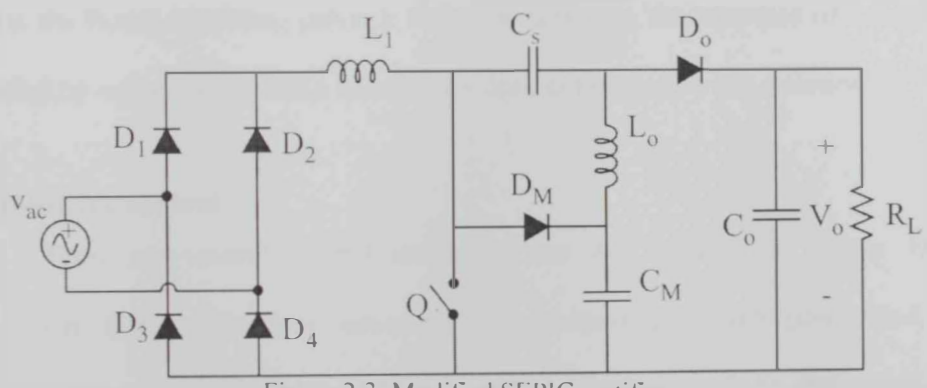

Figure 2.3: Modified SEPIC rectifier.

In this topology, the voltage multiplier technique is applied to the conventional SEPIC circuit, obtaining new operation characteristics. The voltage multiplier technique was used for a Boost converter in order to increase the static gain with reduced switch voltage [8, 48]. Furthermore, the multiphase Boost was improved by voltage doubler in [49] for a universal input HPF rectifier, in order to get high static gain at lower input voltage. Integrating the voltage multiplier cell with a conventional SEPIC was used [8] in order to obtain a high step-up static gain operating with low input voltage and a low step-up static gain for the high input voltage operation. The modified SEPIC could be considered as an motivating substitute for the universal input high power factor rectifier or wide input voltage range applications, operating with high efficiency. However, this topology shown in Figure 2.3 has some disadvantages such as higher losses due to diode bridge and higher circuit complexity than the classical Boost converter. Also, Modified SEPIC converter doesn't have the possibility of avoiding large current passing through the inductors and the diodes if an overload takes place (as in the case of the Boost converter). Moreover, it has the same start-up problems as the Boost converter and, also as the Boost converter, galvanic isolation cannot be implemented (the converter obtained by replacing L_0 with a transformer does not have galvanic isolation).

2.4 Feedback control

There are several control strategies that can be used in Power Factor Correction (PFC) rectifiers operating in Continuous Conduction Mode or Discontinuous Conduction Mode. After components design of the PFC rectifier a

feedback control must be used to ensure that the rectifier is correctly regulating the output voltage. Mainly, there are two parameters that should be taken care by feedback control. The input current should follow the input voltage to emulate a resistor and the output voltage should be regulated around the desired set point. As mentioned previously in this chapter, an ideal PFC should emulate a resistor on the input side while maintaining a properly regulated output voltage. In the case of sinusoidal line voltage, the converter must draw a sinusoidal current from the utility; for the sake of that, an appropriate sinusoidal reference is generally needed and the control objective is to force the input current to follow this current reference [28]. The input current in PFC rectifiers operating in CCM doesn't follow the input voltage, so the current loop must be used to control switches in a way that let the input current follow the input voltage. While in PFC rectifiers operating in DCM, the input current follows the input voltage naturally [50]. Therefore, the control system is simplified since the current loop could be avoided.

The controller could be designed using one of the well-known controllers such as lead compensator, lag compensator, PID, neural network, LQR method or sliding mode [28, 50, 61-69]. Using one of the mentioned control method, the output voltage of an AC/DC converter is regulated to the desired DC voltage. In a closed-loop power converter, to regulate the output voltage the main objective of the controller is adjusting the converter's duty-cycle in order to control the converter switches [28]. The term "duty-cycle" (D) refers to the proportion of on-time to the period T of the switch and is expressed in percent, with 100% as being fully on [28]. The output voltage is regulated by controlling the width of the on-time gating pulse relative to the

switching cycle. This method is generally referred to as Pulse-Width Modulation (PWM).

2.4.1 Small signal analysis

To make the design of the control loop of a switching converter it is required to have the system transfer functions with good approximation representing the dynamic behavior of the rectifier. Among the various techniques existing for obtaining suitable model, small signal modeling is normally used [28, 61-68]. The small signal modeling is linearizing the nonlinear behavior of the rectifier around an operating point, obtaining representative models to small perturbations [28, 51-58]. There are many known methods to build small signal models for example, the method of the state space averaging developed by Middlebrook [51, 53] and the method of the equivalent circuit of the injected current developed by Chetty [52, 54-56]. The equivalent circuit method of the injected current applied to rectifiers operating in continuous conduction mode has proven to be the most suitable to modeling rectifiers operating in discontinuous conduction mode [57].

A comparison between averaging method and the current injected equivalent circuit approach was done in [59]. The small signal model of the novel HPFC converter operating in DCM was built using both approaches and the transfer functions (control to input and output to input) derived by the averaging method coincide with those derived by the current injected equivalent circuit approach. Based on the model which was built using Current injected equivalent circuit approach, a PI controller was designed to regulate only the output voltage in the presence of the line

voltage and load variations since the rectifier was operating in DCM which means that the input current naturally follows the input voltage.

2.4.2 Method of the equivalent circuit of the injected current

The equivalent circuit method of the injected current applies in both converters operating in continuous conduction mode and discontinuous conduction mode. It has great advantage when it is used to model converters operating in discontinuous conduction mode over other methods of small-signal modeling. CIECA modeling applied to PWM DC-DC converters operating in discontinuous conduction has been presented by Chetty [56]. A summary of the steps used to obtain the mathematical model of PFC rectifier is discussed below.

Step 1: Identification of linear and nonlinear elements in PFC rectifier

Step 2: Identification of the equations of the rectifier.

Step 3: Averaging rectifier equations over a half-line cycle.

Step 4: Small signal perturbation and linearization.

Step 5: Obtaining dynamic properties (Transfer Function) and equivalent circuit.

CHAPTER 3

Proposed circuit

3.1 Circuit description

As mentioned in the previous chapter, many researches have been conducted in developing PFC rectifier in such a way that it can operate with high efficiency, unity power factor and reduced level of harmonic distortion. A group of authors focused on improving PFC rectifier by introducing bridgeless PFC rectifier instead of conventional full bridge rectifier that has conduction losses problem. In the conventional PFC circuit, the front stage is normally a full bridge AC-to-DC diode rectifier circuit followed by a PFC circuit of variable characteristics such as (Boost, Buck, SEPIC, Flyback and Cuk) [3-8, 28]. Therefore, the power flows through at least three power semiconductor devices, including two rectifier diodes and at least one active switch. Recently, a PFC circuit has been developed which combines the rectifier diode bridge and the main PFC circuit into a so-called bridgeless PFC circuit in which the power flows through only two power semiconductor devices and therefore reduces converter conduction loss [3-8, 24-30]. Several bridgeless Boost topologies were presented and the overall performance of the rectifier was improved since conduction losses due to diode bridge is reduced [8, 17, 45-47, 58]. Furthermore, since conventional rectifier based on SEPIC PFC circuit has many advantages compared to conventional Boost, many authors had developed new bridgeless topologies based on SEPIC circuit [17, 47].The bridgeless PFC rectifier decreases the conduction losses by reducing the number of semiconductor

components in the line current path. Furthermore, it increases efficiency and improve the overall performance. Therefore, it has gained popularity as a high-efficiency AC-DC rectifier compared to the conventional PFC bridge rectifier.

Lately, some researches are focused on applying voltage multiplier in PFC rectifier to improve its operation [8].The use of voltage multiplier will offer the following advantages: the higher static gain for the operation with the lower input voltage range, lower switch voltage operation, higher efficiency operation with the lowest input voltage, lower input current ripple and easy integration with a regenerative snubber.

In this thesis a combination of the previous studies were gathered and applied on conventional bridge SEPIC PFC rectifier to come up with a new circuit that has better specifications. The new topology is a bridgeless SEPIC PFC rectifier with voltage multiplier as illustrated on Figure 3.1. SEPIC PFC circuit was selected due its advantages such as easy implementation of magnetic coupling that will reduce input current ripple. The bridgeless configuration will reduce the conduction losses since the diode bridge is removed, as a result the overall efficiency will increase. The voltage multiplier will add higher static gain for the operation with the lower input voltage range, lower switch voltage operation and higher efficiency.

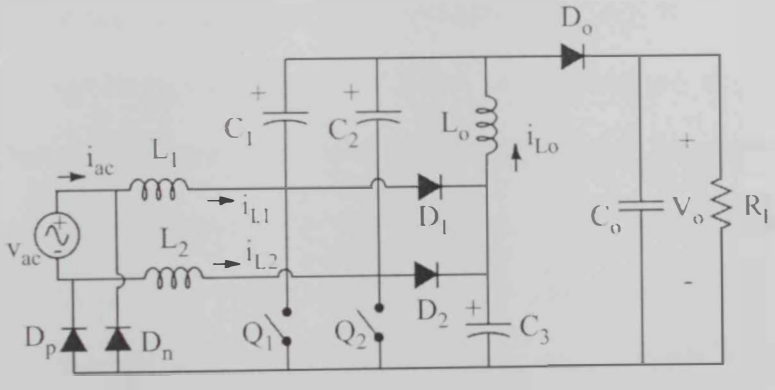

Figure 3.1: The proposed rectifier circuit

The proposed circuit consists of two SEPIC PFC circuits with multiplier D_1 or D_2 with C_3 connected in a symmetrical configuration. Each configuration will operate in a half-line cycle, as depicted on Figures 3.2 and 3.3. By implementing two line frequency diodes D_p and D_n, the output ground is connected to the terminals of AC mains directly in the whole AC line cycle, which stabilizes voltage potential of output ground and reduces Common Mode EMI generation. Furthermore, the efficiency is improved by using line frequency diodes instead of using the relatively high forward voltage MOS's body diodes as a part of the current following path. Furthermore the inductors can be magnetically coupled into a single magnetic core to attain an input current having very low current ripples. Moreover, the symmetrical operation of the proposed simplifies the switches Q_1 and Q_2 drive circuits. In the positive half-line cycle, Q_1 will be derived by a logic circuit and Q_2 will be off. While on the negative half-line cycle Q_2 will be derived with the same logic circuit since Q_1 is off. Note that, by referring to Fig. 3.1, there are maximum three semiconductors in the current flowing path compared to the modified SEPIC rectifier illustrated in Figure 2.3 where four diodes are on at maximum condition; hence, the conduction losses, as well as the thermal stresses on the semiconductor devices, are further reduced, and the circuit efficiency is improved compared to the conventional modified SEPIC rectifier. The proposed topology is designed to work in DCM to achieve almost unity power factor and low THD of input current. Furthermore, the DCM operation gives additional advantages such as: zero current turn-on in the power switches and zero-current turn-off in the output diode. In SEPIC PFC circuit the input current follow the input voltage naturally and thus achieve a sinusoidal input current. Therefore, the

complexity of the control circuitry is reduced since only output voltage control loop will be built to achieve a unity power factor results.

3.2 Operation of the proposed bridgeless PFC circuit

The same techniques and approximations for the steady-state analysis of the continuous conduction mode with a few modifications could be applied to the discontinuous conduction mode [4-9, 28]. This is due to the source is to be considered as constant through switching cycle (switching cycle is less than line cycle) so the changes in AC source in line cycle appears like constant in the switching cycle.

1. Inductor volt-second balance: The DC component of the voltage applied to an inductor must be zero.

$$< v_L >_{Ts} = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = 0 \qquad (3.1)$$

2. Capacitor charge balance: The DC component of current applied to a capacitor must be zero.

$$< i_C >_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_C(t)dt = 0 \qquad (3.2)$$

These assumptions must be held for any circuit that operates in steady state, regardless of the operating mode.

3. The input voltage v_{ac} is considered to be an ideal rectified sine wave, $v_{ac}(t) = V_M \sin(\omega t)$, where V_M is the peak amplitude and ω is the line angular frequency.

4. The switching frequency (f_s) is much higher than the ac line frequency (f_L), so that the input voltage can be considered constant during one switching period (T_s).

5. All components are ideal; thus, there are no losses. The efficiency is 100%.

6. All the capacitors are big enough such that their switching voltage ripples are negligible during the switching period T_s.

Due to the symmetry of the operations, the positive half-line cycle is analyzed through the three distinct stages of DCM operation. Volt-second balance is applied for each inductor voltage and charge balance for each capacitor current in the network. The switching ripple in the output capacitor voltages is ignored while the inductor current switching ripple is considered.

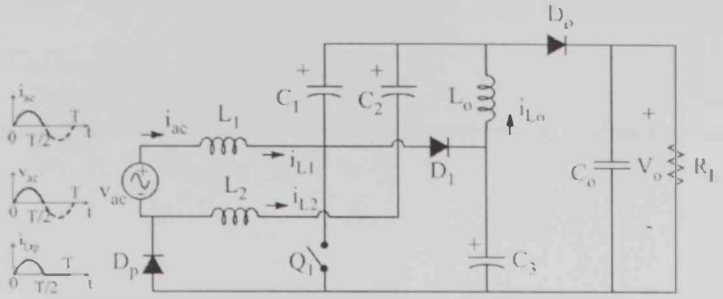

Figure 3.2: Equivalent rectifier circuit during positive half-line period.

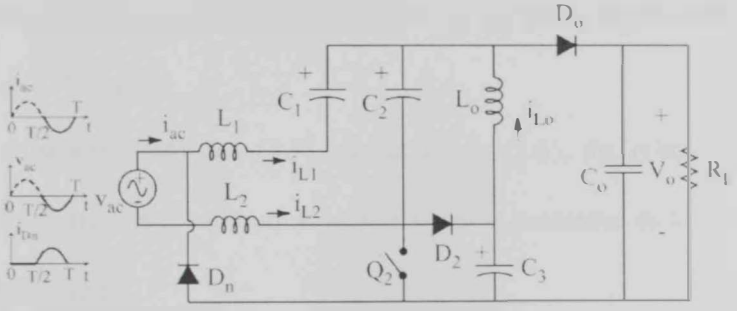

Figure 3.3: Equivalent rectifier circuit during negative half-line period.

3.3 Principle of operation

Before going through the analysis of the discontinuous current mode three stages of the proposed circuit, additional assumptions should be used to simplify the analysis. The assumptions of V_{C1} and V_{C2} are necessary since they are used in figuring out the output-input gain ratio relationship. These assumptions can be

justified by considering the following three loops at positive half line cycle ($0 < t < T_1/2$) shown in Figure 3.2.

Loop 1 (V_{ac}, L_1, C_1, L_o, C_3)

By applying KVL on Loop 1 and it is known that within a switching period inductor voltage is zero [28]:

$$< v_{L1}(t) >_{Ts} = < v_{L2}(t) >_{Ts} = < v_{LO}(t) >_{Ts} = 0 \quad (3.3)$$

The following equation can be extracted

$$v_{C1}(t) = v_{C3}(t) - v_{ac}(t) \quad (3.4)$$

Loop 2: (L_2, C_2, L_o, C_3):

The same procedure is repeated to loop 2, therefore the following relation can be figured:

$$v_{C2}(t) = v_{C3}(t) \quad (3.5)$$

Loop3: (C_1, C_o, C_3)

Finally, by applying KVL on Loop 3, the following equation can be extracted:

$$v_O(t) = v_{C3}(t) + v_{C1}(t) \quad (3.6)$$

By placing equations (3.4) and (3.5) into equation (3.6), the relationship between capacitor voltage and input and output voltages can be presented as follow:

$$v_{C1}(t) = \left(\frac{v_O(t) - v_{ac}(t)}{2}\right) \quad (3.7)$$

$$v_{C3}(t) = \left(\frac{v_{ac}(t) + v_O(t)}{2}\right) \quad (3.8)$$

The same steps can be applied at the negative half line cycle to get relation between capacitors voltage and voltages of input and output. Since the proposed circuit is symmetric the analysis at the positive half line cycle will be considered only. Figure 3.2 show the equivalent circuit at the positive half line cycle that will be analyzed in

the following sections. The proposed circuit was designed to operate in DCM which has a lot of advantages as mentioned previously. Analysis of this mode consists of three stages during switching period. On the first stage, switch Q_1 will be on while diodes D_1 and D_o are off. On the second stage, diodes D_1 and D_o are on while switch Q_1 is off. Diodes D_1 and D_o and switches are off on the last stage. Finally, diode D_p is always on during the three stages. A detailed analysis of each stage is shown in the following sections.

3.3.1 The first stage

During this subinterval, switch Q_1 is turned on by the control signal and both diodes D_1 and D_o are off. Multiplier diode D_1 is reversed biased due to capacitor C_3 voltage, while output diode D_o is reversed biased due to the subtraction of capacitors C_1 and C_o voltages (V_{Co}-V_{C1}). Diode D_p will be forward biased by the sum of inductors current ($i_{L1}(t)$ and $i_{L2}(t)$) and diode D_n will be reversed biased by input voltage. The equivalent circuit representing the first stage is shown in Figure 3.4.

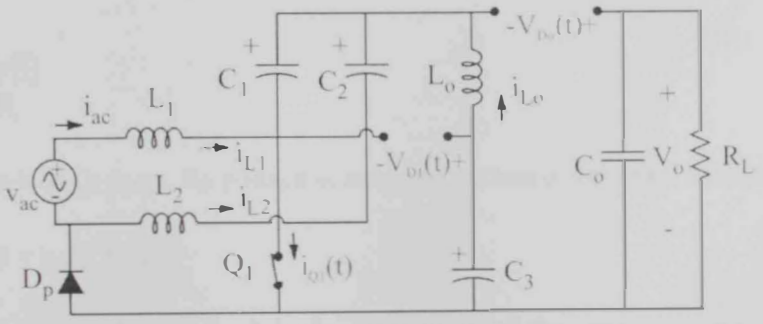

Figure 3.4: Topological stage during switch Q_1 on time over switching cycle.

Using Figure 3.4 and equations (3.4), (3.5), (3.6) (3.7) and (3.8), the Inductor voltages can be expressed as follow:

$$v_{L1}(t) = v_{L2}(t) = v_{Lo}(t) = v_{ac}(t) \tag{3.9}$$

In this stage, the three-inductor currents increase linearly at a rate that is proportional to the input voltage v_{ac}. The rate of increase of the three inductors current is given by:

$$\frac{di_{Ln}(t)}{dt} = \frac{v_{ac}(t)}{L_n}, \qquad n = 1, 2, 3 \tag{3.10}$$

In addition the current through each capacitor can be written in terms of inductor current using Figure 3.4.

- Capacitor C_1

$$i_{C1}(t) = i_{L2}(t) + i_{LO}(t) \tag{3.11}$$

- Capacitor C_2

$$i_{C2}(t) = -i_{L2}(t) \tag{3.12}$$

- Capacitor C_3

$$i_{C3}(t) = -i_{LO}(t) \tag{3.13}$$

- Capacitor C_o

$$i_{C_o}(t) = -\frac{v_O(t)}{R_L} \tag{3.14}$$

Since the switch Q_1 is on, its voltage is zero and current during first subinterval is:

$$i_{Q1}(t) = i_{L1}(t) + i_{L2}(t) + i_{LO}(t) \tag{3.15}$$

Referring to Figure 3.4, the switch current is equal to the sum of the three inductors' currents. Thus, the rate of change of switch current is given by:

$$\frac{di_{Q1}(t)}{dt} = \frac{v_{ac}(t)}{L_e} \tag{3.16}$$

The peak current of the switch within this interval is:

$$I_{Q1\_peak} = \frac{V_M}{L_e} d_1 T_s \tag{3.17}$$

Where V_M is the peak amplitude of the input voltage v_{ac}, d_1 is the switch duty cycle at the fist stage, and L_e is the parallel combination of inductors L_1, L_2 and L_o. Multiplier diode D_1 current is zero, while the voltage can be expressed at this interval. Furthermore, the output diode Do has similar voltage shown in equation (3.18)

$$v_{D1}(t) = v_{Do}(t) = \frac{v_{ac}(t) + v_o(t)}{2} \tag{3.18}$$

3.3.2 The second stage

During this subinterval, switch Q_1 will be off by the control signal and both diodes D_1 and D_o will conduct simultaneously providing a path for the three inductor currents. The equivalent circuit representing the second stage is shown in Figure 3.5. Using Figure 3.5 the three inductors voltages can be written as follow.

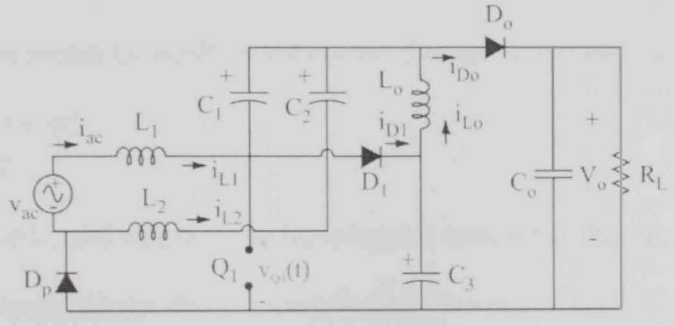

Figure 3.5: Topological stage during switch Q_1 off time over switching cycle.

$$v_{L1}(t) = v_{L2}(t) = v_{Lo}(t) = -v_{C1}(t) \tag{3.19}$$

In this stage, the three inductor currents decrease linearly at a rate that is proportional to the capacitor voltage V_{C1}. The rate of decrease of three inductors' currents are given by

$$\frac{di_{Ln}(t)}{dt} = -\frac{v_{C1}(t)}{L_n}, \qquad n = 1, 2, 3 \tag{3.20}$$

Then the current through each capacitor is written in terms of inductor current using Figure 3.5.

- Capacitor C_1

$$i_{C1}(t) = i_{L2}(t) + i_{LO}(t) - i_{Do}(t) \tag{3.21}$$

- Capacitor C_2

$$i_{C2}(t) = -i_{L2}(t) \tag{3.22}$$

- Capacitor C_3

$$i_{C3}(t) = i_{L1}(t) + i_{L2}(t) - i_{Do}(t) \tag{3.23}$$

- Capacitor C_o

$$i_{Co}(t) = i_{Do}(t) - \frac{v_O(t)}{R_L} \tag{3.24}$$

At this stage the switch Q_1 is off, so the current through it zero and its voltage is:

$$v_{Q1}(t) = \frac{v_{ac}(t) + v_o(t)}{2} \tag{3.25}$$

Multiplier diode D_1 and output diode D_o voltage is zero, while the current was gotten by capacitor charge balance that is shown in the following section.

$$i_{D1}(t) = i_{Do}(t) = \frac{1}{2}\left(i_{L1}(t) + i_{L2}(t) + i_{Lo}(t)\right) \tag{3.26}$$

The diodes D_1 and D_o current is equal to half the sum of the three inductors' currents. Thus, the rate of change of diodes current is given by:

$$\frac{di_{Do}(t)}{dt} = \frac{di_{D1}(t)}{dt} = -\frac{v_{C1}(t)}{2L_e} \tag{3.27}$$

The peak current of the two diodes within this interval is:

$$I_{D1} = I_{Do} = -\frac{V_{C1}}{2L_e} d_2 T_s \tag{3.28}$$

Where V_{C1} is the peak voltage of capacitor C_1 and d_2 is the diodes duty cycle (diodes D_1 and D_o during the positive half-line cycle and diodes D_2 and D_o during the negative half-line cycle). The second stage ends when both diodes are reversed biased and the third stage begins.

3.3.3 The third stage

During this subinterval, switch Q_1 remains off while both diodes D_1 and D_o reverse biased and turned off. The equivalent circuit representing the first stage is shown in Figure 3.6. The three inductors behave as current sources, which keep the currents constant. The voltage across the three inductors is zero. During this interval, only the diode D_p conducts to provide a path for i_{L1} and i_{L2}. Capacitor C_1 is being charged by the inductor current i_{L1}, Capacitor C_2 is being charged by the inductor current i_{L2} and capacitor C_3 is being charged by the inductor current i_{Lo}. Using Figure 3.6 the inductors voltage can be written as follow.

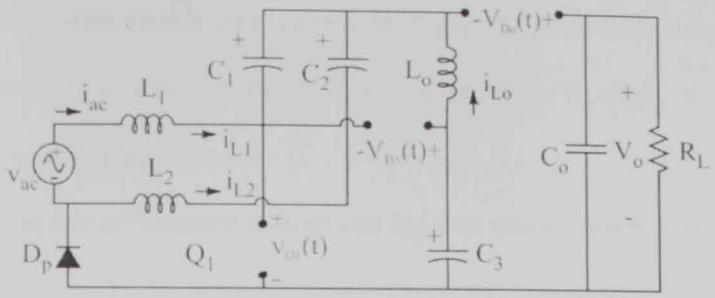

Figure 3.6: Topological stage during DCM over switching cycle.

$$v_{L1}(t) = v_{L2}(t) = v_{LO}(t) = 0 \tag{3.29}$$

The capacitors current are written in terms of inductor current

- Capacitor C_1

$$i_{C1}(t) = -i_{L1}(t) = -I_x \tag{3.30}$$

- Capacitor C_2

$$i_{C2}(t) = -i_{L2}(t) = -I_y \tag{3.31}$$

- Capacitor C_3

$$i_{C3}(t) = -i_{LO}(t) = -I_z \tag{3.32}$$

- Capacitor C_o

$$i_{C_o}(t) = -\frac{v_O(t)}{R_L} \tag{3.33}$$

Voltage stresses on the switch during the third stage are:

$$v_{Q1}(t) = v_{ac}(t) \tag{3.34}$$

Finally, Voltage stresses on both diodes D_1 and D_o during the third stage are:

$$v_{D1}(t) = v_{Do}(t) = v_{C1}(t) \tag{3.35}$$

This period ends when switch Q_1 is turned on. Figure 3.7 shows the theoretical DCM waveforms during one switching period *Ts* for the proposed rectifier.

3.4 Inductor volt-second balance

The principle of inductor volt-second balance allows determination of the DC voltage components in any switching converter [28]. In steady state, the average voltage applied to an inductor must be zero. In this section, inductor volt-second balance will be applied to three inductors L_1, L_2 and L_o to get a relation between the switch duty cycle at the first stage d_1 and the switch duty cycle at the second stage d_2 that will be used to get the voltage conversion ratio in terms of circuit parameters. The average voltage of each inductor during a switching period is zero. Since the voltage of the three inductors are the same, inductor L_1 will be used:

$$< v_{L1}(t) >_{Ts} = 0 \tag{3.36}$$

Where $<v_{L1}(t)>_{Ts}$ is the average voltage of L_1 during a switching period. Substituting equations (3.9), (3.19) and (3.29) that represent (v_{L1}) at each subinterval:

$$d_2 = \frac{2\sin(\omega t)}{M - \sin(\omega t)} d_1 \tag{3.37}$$

Where conversion ratio M is defined by:

$$M = \frac{v_o}{V_M} \tag{3.38}$$

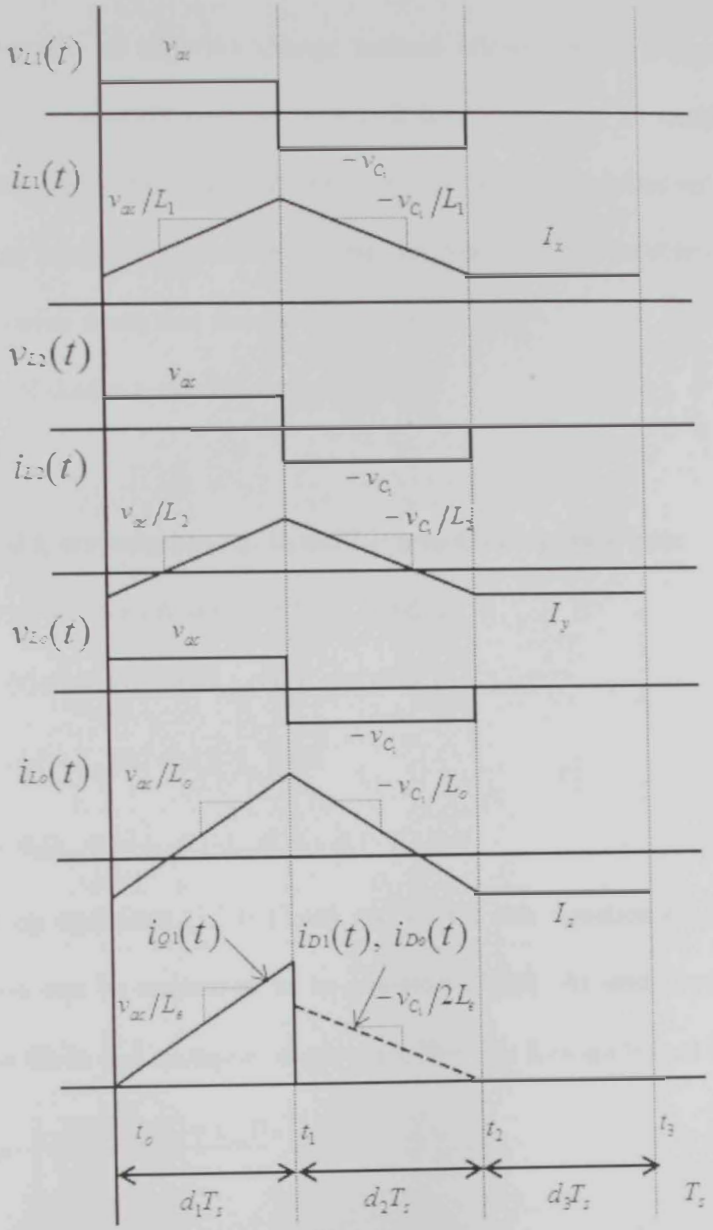

Figure 3.7: Theoretical DCM waveforms during switching period for the proposed rectifier

3.5 Capacitor charge balance

The principle of capacitor charge balance allows determination of the D_C components of the inductor currents in a switching converter. In steady state, the average current applied to a capacitor must be zero [28]. As mentioned before, the capacitor charge balance is used mainly in this section to get current relation of output diode and multiplier diode that was used in section 3.3.2.

The derivation of diodes current is shown below:

$$I_z = -(I_x + I_y) \tag{3.39}$$

Where I_x, I_y and I_z are inductors L_1, L_2 and L_3 current during stage three.

Applying charge balance on capacitor C_1, C_2 and C_3

$$d_1(i_{L2}(t) + i_{LO}(t)) + d_2(i_{L2}(t) + i_{LO}(t) - i_{Do}(t)) + d_3(-I_x) = 0 \tag{3.40}$$

$$d_1(-i_{L2}(t)) + d_2(-i_{L2}(t)) + d_3(-I_y) = 0 \tag{3.41}$$

$$d_1(-i_{LO}(t)) + d_2(i_{L1}(t) + i_{L2}(t) - i_{Do}(t)) + d_3(-I_z) = 0 \tag{3.42}$$

Then by placing equations (3.39) (3.40) and (3.41) into equation (3.2), the diodes current relation can be expressed as in equation (3.43). At stage two the current through output diode and multiplier diode when they are forward biased is:

$$i_{Do}(t) = i_{D1}(t) = \frac{i_{L1}(t) + i_{L2}(t) + i_{LO}(t)}{2} \tag{3.43}$$

3.6 Voltage conversion ratio

The voltage conversion ratio $M = V_o / V_M$ in terms of circuit parameters can be found by using several techniques such as applying power balance principle by assuming 100% efficiency and equating input power and output power [5-8, 28]. This

method is hard to be applied here so another technique is used to obtain voltage conversion ratio by evaluating the average diode D_o current I_{Do} during half line cycle of the ac input voltage.

From Figure 3.1, the average current of output diode is

$$[I_{D_o}(t)]_{avg} = [I_{C_o}(t)]_{avg} + [I_{R_L}(t)]_{avg} \tag{3.44}$$

It is known the average current (DC) passing through the capacitor is zero, which means that output diode average current is equal to average load current

$$[I_{D_o}(t)]_{avg} = [I_{R_L}(t)]_{avg} = \frac{v_o(t)}{R_L} \tag{3.45}$$

Average diode current over half-line cycle is:

$$I_{D_o} = \frac{1}{T_L/2} \int_0^{T_L/2} \overline{i_{D_o}}\, dt \tag{3.46}$$

Where T_L is the period of the line voltage. The symbol "$\overline{\ }$" denotes the average value during one switching cycle T_s. From Figure 3.8 the average output diode current over a switching cycle is given by:

$$\overline{i_{D_o}} = \frac{1}{T_s} \int_0^{T_s} i_{D_o}(t)\, dt \tag{3.47}$$

This integration can be expressed in another form (the area under the curve) which is the triangle area:

$$\overline{i_{D_o}} = \frac{1}{T_s} \left[\frac{1}{2} (base)(height) \right] \tag{3.48}$$

The base represents the second stage of the switching cycle (d_2T_s) and the height of the triangle represents the peak output diode current:

$$i_{D_o-pk} = \frac{v_{C1}}{2L_e} d_2 T_s \tag{3.49}$$

Substituting equation (3.49) into equation (3.48) to get average output diode current over a switching cycle:

$$\overline{i_{D_o}} = \frac{1}{4} \frac{d_1^2 T_s v_{ac}^2}{L_e v_{C1}} \tag{3.50}$$

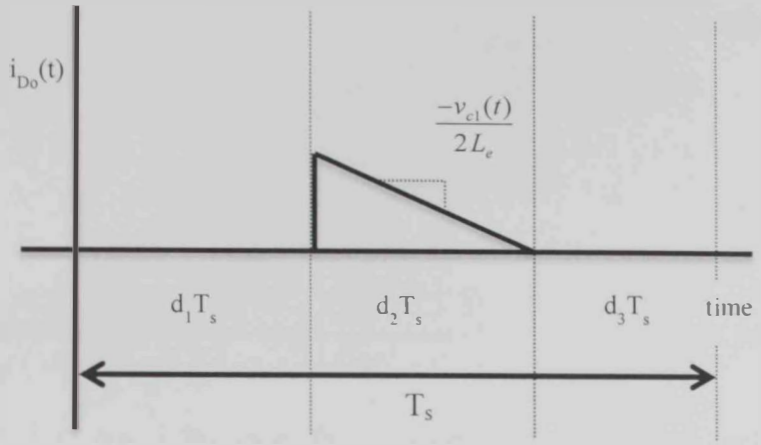

Figure 3.8: Output diode current over a switching cycle.

Subsequently, the average output diode current over a half line cycle can be obtained by substituting equation (3.50) into equation (3.47).

$$I_{D_o} = \frac{d_1^2 T_s V_M}{T_L L_e} \int_0^{T_L/2} \frac{\sin^2(\omega t)}{M - \sin(\omega t)} dt \tag{3.51}$$

The integration shown in equation (3.78) is difficult to be solved; so long division is used to simplify it:

$$\int_0^{T_L/2} \frac{\sin^2(\omega t)}{M - \sin(\omega t)} dt = \int_0^{T_L/2} \left(-\sin(\omega t) - M + \frac{M^2}{M - \sin(\omega t)} \right) dt \tag{3.52}$$

Using CRC Book (Standard Mathematical Tables) [60], the average output diode current over a half line cycle is given by:

$$I_{D_O} = \frac{d_1^2 T_s V_M}{L_e} \left(\frac{-M}{2} - \frac{1}{\pi} + \frac{M^2}{\pi\sqrt{M^2 - 1}} \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{M^2 - 1}} \right) \right] \right) \tag{3.53}$$

As mentioned previously the integral of the steady-state capacitor C_o current over one line-cycle integration period is zero, the average value of the diode D_o current during one line cycle is equal to the average current through the load R_L. Thus, by equating (3.45) and (3.53), the relationship between duty cycle d_1 and conversion ratio is.

$$d_1 = \sqrt{\frac{K M}{\alpha}} \tag{3.54}$$

Where:

$$K = \frac{2L_e}{T_s R_L} \tag{3.55}$$

$$\alpha(M) = -\frac{2}{\pi} - M + \frac{2M^2}{\pi\sqrt{M^2 - 1^2}}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{M^2 - 1^2}}\right)\right] \tag{3.56}$$

Equations (3.54, 3.55 and 3.56) show that relationship between duty cycle and conversion ratio is nonlinear and it is difficult to get conversion ratio explicitly. Two techniques were used to simplify the relationship around operating point. The first method is curve fitting using Microsoft Excel in which equation (3.56) which is representing non linearity replaced by a second order equation:

$$\alpha(M) = 0.301M^2 - 1.751M + 2.761 \tag{3.57}$$

Figure 3.9 shows both curves that represent the actual values equation (3.56) and the approximated values equation (3.57). The second approximation was done by using curve fitting tool box in Matlab to approximate equation (3.56) in the following simple form:

$$F(x) = \frac{a}{x - b} \tag{3.58}$$

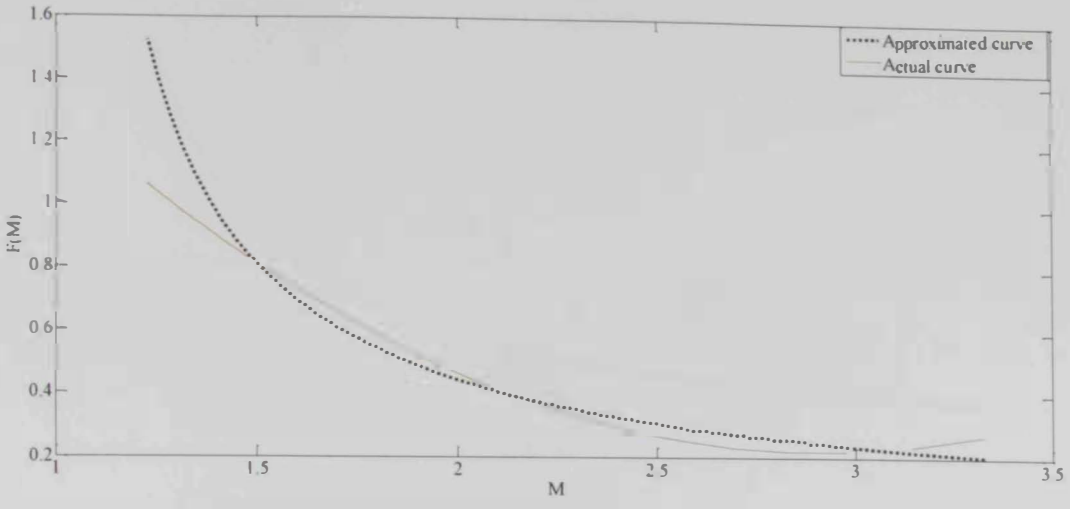

Figure 3.9: The first approximation curve

Different values of (a and b) were tested and the best approximation was shown in equation (3.59) which was used in [57].

$$F(M) = \frac{0.48}{M - 0.92} \tag{3.59}$$

A comparison between the two methods was done around the same operating point where M ranges from 1 to 3. The second method was selected because the error was below 2% while the error in the first method was higher. In addition, this form is easier to be used in output diode current to get the relation $M(d_1,K)$. Table 3.1 shows the comparison between these techniques. So, the average output diode current can be rewritten in the following form that will be used in the following sections:

$$I_{D_O} = \frac{d_1^2 T_s V_M}{2L_e}\left(\frac{0.48}{M - 0.92}\right) \tag{3.60}$$

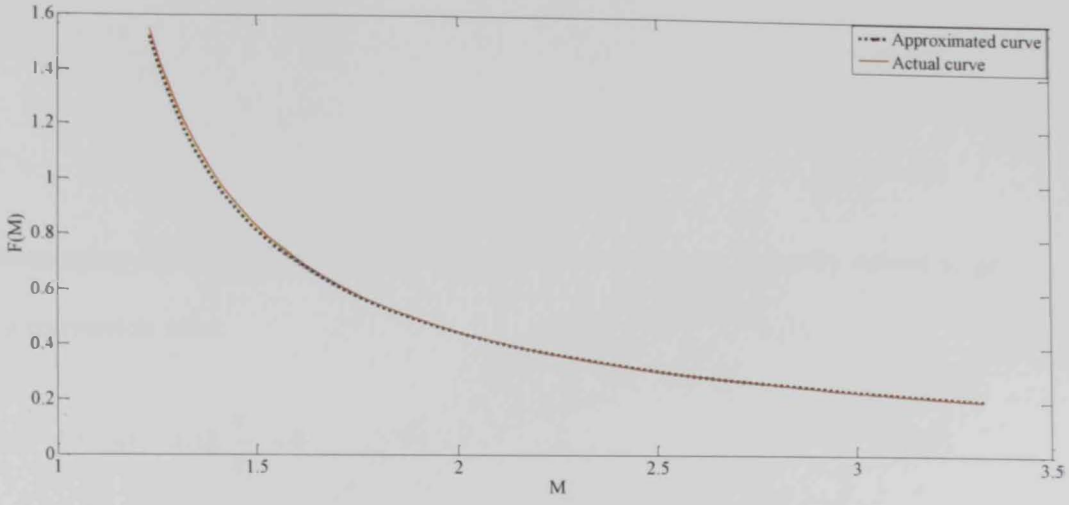

Figure 3.10: The second approximation curve

Table 3.1: Comparison between approximation methods

M	α(M)	Method 1	Error %	Method 2	Error %
1.2	1.696	1.093	35.529	1.714	-1.095
1.4	0.977	0.900	7.926	1.000	-2.354
1.6	0.694	0.730	-5.188	0.706	-1.718
1.8	0.540	0.584	-8.234	0.545	-1.014
2	0.443	0.463	-4.613	0.444	-0.421
2.2	0.375	0.366	2.556	0.375	0.062
2.4	0.326	0.292	10.267	0.324	0.456
2.6	0.288	0.243	15.559	0.286	0.782
2.8	0.258	0.218	15.501	0.255	1.054
3	0.234	0.217	7.175	0.231	1.285

Rewriting the average output diode current formula (3.60) and equating it with the average output current v_o/R_L , to get the voltage conversion ratio, the duty cycle can be rewritten in the following form

$$d_1 = \sqrt{\frac{K M}{\beta}} \tag{3.61}$$

Where the following coefficients (β and k) represent:

$$\beta = \frac{0.48}{(M - 0.92)} \tag{3.62}$$

$$K = \frac{2L_e}{R_L T_s} \tag{3.63}$$

Rearranging equation (3.60) to be in quadratic form that can be easily solved to get the conversion ratio:

$$M^2 - 0.92M - 0.48\frac{R_L}{R_e} = 0 \tag{3.64}$$

Where the emulated resistance (R_e) is

$$R_e = \frac{2L_e}{d_1^2 T_s} \tag{3.65}$$

Then, by solving equation (3.64), the conversion ratio (M) can be expressed as a function of the duty cycle and the coefficient (k):

$$M(d_1, K) = 0.46 + \sqrt{0.212 + 0.48\frac{d_1^2}{K}} \tag{3.66}$$

Since equation (3.64) is quadratic, there were two solutions, but the negative solution is neglected because output voltage in SEPIC topology is always positive. The conversion ratio is defined according to the specific application, while the load resistance R_L is dependent on the output power level. With the specified power and voltage demands, the inductance is designed according to the desired range of duty cycle and switching frequency. Moreover, the larger the switching frequency is, the smaller the inductance. In order to design a smaller inductor with purpose of

obtaining smaller size and weight, a higher switching frequency is preferred. However, the higher the switching frequency is, the higher the switching loss would be. As a result, a tradeoff between the size of inductor and the switching loss should be taken into account in the design process [3-9].

3.7 Boundaries between CCM and DCM

As mentioned in the previous chapter, the PFC rectifier circuit can operate in CCM or DCM. Since the proposed topology was designed to operate in DCM, the dimensionless coefficient (K) that was mentioned in equation (3.55) must be designed in such a way that ensures DCM operation of the proposed circuit. Referring to the diode D_o current waveform in Figure 3.8, the DCM operation mode requires that the sum of the switch duty cycle and the normalized switch-OFF time length be less than one:

$$d_2 < 1 - d_1 \tag{3.67}$$

Then, by replacing d_2 by its value shown in equation (3.37), duty cycle d_1 can be represented by:

$$d_1 < \frac{M - \sin(\omega t)}{M + \sin(\omega t)} \tag{3.68}$$

After that, substituting duty cycle equation found previously using second approximation (3.61) in equation (3.68) to get the following relation:

$$K < K_{critical} \tag{3.69}$$

$$K_{critical} = \left(\frac{M - \sin(\omega t)}{M + \sin(\omega t)}\right)^2 \left(\frac{\beta}{M}\right) \tag{3.70}$$

Where the dimensionless conduction parameter K was defined in equation (3.55) and K_{crit} is the critical value of K operating at DCM that has maximum value and minimum value depending on the input line angle.

- When ωt = 0 or 180

$$K_{critical-Max} = \frac{\beta}{M} \tag{3.71}$$

- When ωt = 90 or 270

$$K_{critical-Min} = \left(\frac{\beta}{M}\right)\left(\frac{M-1}{M+1}\right)^2 \tag{3.72}$$

For values of $K < K_{critical-Min}$, the proposed rectifier operates in DCM and it operates in CCM for values of $K > K_{critical-Max}$. However, for values $K_{critical-Min} < K < K_{critical-Max}$ the converter operates in both modes, i.e., in CCM near the peak value of the input line voltage and in DCM near the zero crossing of the input line voltage. These relations will be used in circuit design section to ensure that rectifier elements and duty cycle are selected in a proper way.

3.8 Large signal model

As mentioned in section 2, one of the advantages of designing the rectifier to operate in DCM is that input current follows input voltage profile which means that the rectifier appears as an emulated resistor and the power factor is almost unity. The following analysis will proof that the low frequency components of the switch network input port obey Ohm's law. The waveform of the switch network terminal voltage and current over a switching cycle is drawn in Figure 3.11.

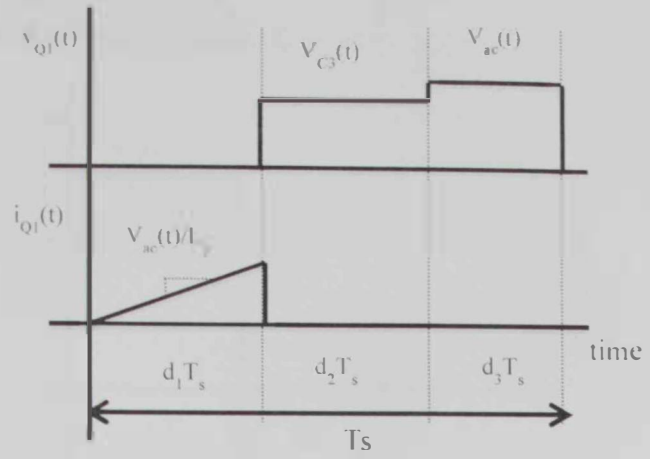

Figure 3.11: Switch Q_1 terminal voltage and current.

According to Figures 3.2 and 3.11, during the second operation stage (d_2T_s), the average switch voltage over a switching cycle can be expressed as

$$\langle v_{Q1}(t)\rangle_{Ts} = \langle v_{ac}(t)\rangle_{Ts} \tag{3.73}$$

The average switch current over a first stage of switching cycle (d_1T_s), is derived by integrating the switch current waveform as depicted in Figure 3.11 during the whole switching cycle

$$\langle i_{Q1}(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_{Q1}(t)dt = \frac{d_1^2 T_s}{2L_e}\langle v_{ac}(t)\rangle_{Ts} \tag{3.74}$$

Then, by dividing equation (3.73) and equation (3.74):

$$\frac{\langle v_{Q1}(t)\rangle_{Ts}}{\langle i_{Q1}(t)\rangle_{Ts}} = \frac{\langle v_{ac}(t)\rangle_{Ts}}{\frac{d_1^2 T_s}{2L_e}\langle v_{ac}(t)\rangle_{Ts}} = \frac{2L_e}{d_1^2 T_s} = R_e \tag{3.75}$$

According to equation (3.74), over a switching cycle switch Q_1 average voltage is proportional to average current. In other words, switch Q_1 emulates a resistor with

resistance R_e. The waveform of switch Q_1 network terminal voltage during a switching cycle is drawn in Figure 3.11.

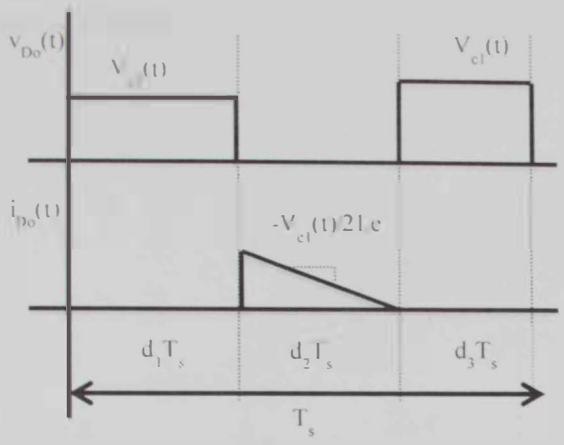

Figure 3.12: Output Diode terminal voltage and current

Similar procedures are applied to output diode D_o terminal voltage and current to find the average voltage and the average current of output diode D_o over a switching cycle. Using Figure 3.12, average diode voltage and current can be expressed, respectively, as

$$\langle v_{Do}(t)\rangle_{Ts} = \langle v_{C1}(t)\rangle_{Ts} \tag{3.76}$$

$$\langle i_{Do}(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{Ts} i_{Do}(t)dt = \frac{d_1^2 T_s}{4L_e}\frac{\langle v_{ac}(t)\rangle_{Ts}^2}{\langle v_{C1}(t)\rangle_{Ts}} \tag{3.77}$$

Then, by multiplying equations [(3.76) and (3.77)] and plugging R_e value from equation (3.75), the equivalent power out of the diode can be expressed as:

$$\langle v_{Do}(t)\rangle_{Ts}\langle i_{Do}(t)\rangle_{Ts} = \frac{\langle v_{ac}(t)\rangle_{Ts}^2}{2R_e} = \frac{\langle P(t)\rangle_{Ts}}{2} \tag{3.78}$$

According to equation (3.78), The output diode D_o behaves like a controlled power source, the power of which is equals to half of power consumption of the equivalent

resistor $R_e(d_1)$. Thus, the switch network could be modeled by a loss-free resistor and a dependent power source as shown in Figure 3.13. Since D_1 and D_o have similar voltage and current waveform

$$\langle v_{D1}(t)\rangle_{Ts}\langle i_{D1}(t)\rangle_{Ts} = \frac{\langle v_{ac}(t)\rangle_{Ts}^2}{2R_e} = \frac{\langle P(t)\rangle_{Ts}}{2} \tag{3.79}$$

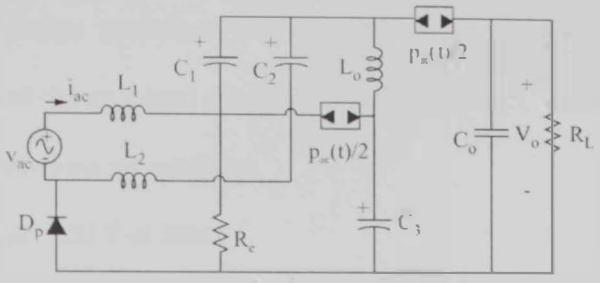

Figure 3.13: loss-free resistor model

In addition, the multiplier diode D_1 behaves like a controlled power source, the power of which is equals to half of power consumption of the equivalent resistor R_e. The equivalent circuit of the topology in the steady state can be modeled by replacing the switch network with its averaged model. In steady-state condition, in which the inductor and capacitor can be, respectively, replaced with short circuit and open circuit as shown in Figure 3.14.

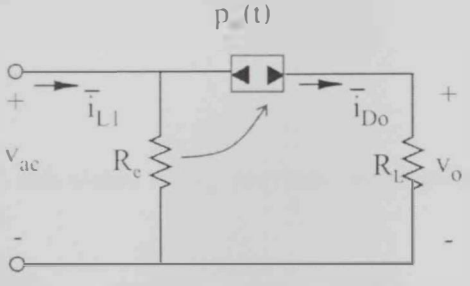

Figure 3.14: loss-free resistor model at steady state (L is shorted and C is opened)

CHAPTER 4

Design procedure

4.1 Power stage specification

A simplified design procedure is presented in this section to determine the component values of the proposed rectifier. To design the PFC rectifier, the following power stage specifications are assumed:

1. Input voltage: 120 V at 50Hz
2. Output voltage: 400 V
3. Output power: 200 W.
4. Switching frequency f_s = 50 kHz
5. Maximum input current ripple Δi_{l1} =10% of fundamental input current.
6. Output voltage ripple Δv_o =2% V_o

From the aforementioned data and assuming that the efficiency is 100%, the values of the circuit components are calculated as follows.

The load is resistive and its value is given by:

$$R_L = \frac{(400)^2}{200} = 800\Omega \qquad (4.1)$$

The conversion ratio is calculated using previous assumption of input voltage and output voltage:

$$M = \frac{400}{\sqrt{2}(120)} = 2.36 \qquad (4.2)$$

The constant β is required to calculate ($K_{critical}$) that is needed to define the mode of operation:

$$\beta = \frac{0.48}{2.36 - 0.92} = 0.333 \tag{4.3}$$

$$K_{critical-Min} = \left(\frac{0.333}{2.36}\right)\left(\frac{2.36-1}{2.36+1}\right)^2 = 23.11\times10^{-3} \tag{4.4}$$

To ensure that proposed rectifier is operating in DCM the dimensionless coefficient K should be less than $K_{critcal\ Min}$

$$K = 0.85 * K_{critical-Min} = 19.65\times10^{-3} \tag{4.5}$$

The duty cycle that ensures DCM operation is:

$$d_1 = \sqrt{\frac{KM}{\alpha}} = 0.37 \tag{4.6}$$

From this result, the constant L_e can be calculated

$$L_e = 388.4\mu H \tag{4.7}$$

4.2 Inductors design

The inductor values are calculated using inductor current ripple equation shown below:

$$\Delta i_{L1} = \frac{v_{ac}(t)}{2L_1} d_1 T_s \tag{4.8}$$

The maximum inductor current ripple can be calculated from the peak input current:

$$\Delta i_{L1-Max} = 10\% i_{ac\_peak} = 0.236 \tag{4.9}$$

Then, inductors L_1 and L_2 are equal and given by inductor ripple equation considering maximum condition:

$$L_1 = L_2 = 2.66mH \tag{4.10}$$

$$L_o = \frac{1}{\frac{1}{L_e} - \left(\frac{1}{L_1} + \frac{1}{L_2}\right)} = 180\mu H \tag{4.11}$$

4.3 Capacitors design

Capacitors C_1 and C_2 are designed under the following constraints:

1) These capacitors are designed to present nearly constant voltage value during switching cycle.
2) Capacitors voltage should follow the input voltage profile during line cycle.

The resonant frequency between (L_1, C_1, L_o, and C_3) during stage 1 of the switching cycle shown in Figure 3.4 must be much greater than the line frequency to avoid input current oscillations at every line half cycle:

$$\omega_{r1} = \frac{1}{\sqrt{((L_1+L_o)(C_1+C_3))}} \qquad \omega_{r1} > \omega_L \tag{4.12}$$

The resonant frequency between capacitor C_1 and inductor L_o must be lower than switching frequency to assure constant voltage in a switching period.

$$\omega_{r2} = \frac{1}{\sqrt{(C_1)(L_o)}} \qquad \omega_{r2} > \omega_L \tag{4.13}$$

Several values for resonant frequency were tried to match these constraint and the best result was by selecting:

$$C_1 = C_2 = C_3 = 1.2\mu F \tag{4.15}$$

$$f_L = 50\ Hz \tag{4.16}$$

$$f_{r1} = \frac{1}{2\pi\sqrt{((L_1+L_o)(C_1+C_3))}} = 2000\ Hz \tag{4.17}$$

$f_L < f_{r1} < f_s$ constraint (1) is acheived

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_o C_1)}} = 11KHz \tag{4.18}$$

$f_L < f_{r2} < f_s$ constraint (2) is acheived

Output capacitor C_o is calculated by using power balance equation ($P_{in} = P_o$) to get output diode current equation:

$$v_{ac}(t) i_{in}(t) = v_o(t) i_o(t) \tag{4.19}$$

Using equation (4.19), the output current can be expressed as:

$$i_o(t) = \frac{P_{in}(1 - \cos(2\omega t))}{2V_o} \tag{4.20}$$

Where P_{in} represent the peak power ($P_{in} = I_M \cdot V_M$). Using Figure 4.1 and applying nodal analysis on the output node, the relation between output capacitor current and output diode current is as follows:

$$i_{Co}(t) = i_o(t) - I_o \tag{4.21}$$

Substituting equation (4.20) into equation (4.21), output capacitor current can be expressed by:

$$i_{Co}(t) = \frac{P_{in}(1 - \cos(2\omega t))}{V_o} - I_o \tag{4.22}$$

All AC current goes through capacitance and the DC current are blocked.

$$i_{Co}(t) = C_o \frac{dv_o(t)}{dt} = -I_o \cos(2\omega t) \tag{4.23}$$

At switching cycle level:

$$\Delta v_{Co}(t) = \frac{1}{C_o}\int_{T_1/8}^{3T_1/8}\left(i_o(t) - I_o\right)dt \qquad (4.24)$$

Where the output diode current at switching frequency level is given by

$$i_o(t) = \frac{1}{4}\frac{D_1^2 T_s}{L_e V_{C1}} v_{in}^2(t) \qquad (4.25)$$

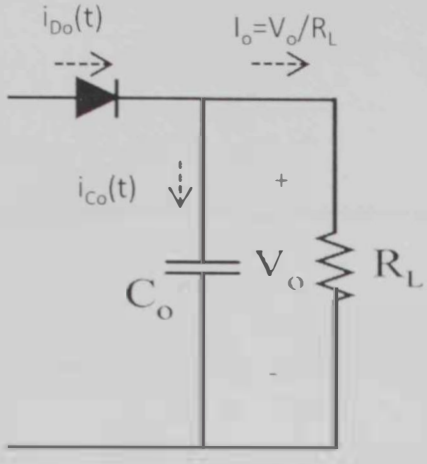

Figure 4.1: Nodal analysis at output side.

The limits of integration in equation (4.24) was selected integrating equation (4.23) to get output capacitor voltage ripple, then the limits was defined according to the maximum and minimum values of the ripple:

$$\Delta v_{Co}(t) = -\frac{I_o}{2\omega C_o}\sin(2\omega t) \qquad (4.26)$$

Output capacitor voltage ripple (Δv_{Co}) will be maximum at zero crossing of $i_{Co}(t)$ shown in Figure 4.2 and that is when $2\omega t = \pi/2$. The upper limit of the integration can be defined as $t_2=3T_1/8$. On the other hand, the minimum value of output capacitor voltage ripple (Δv_{Co}) will be at the second zero crossing of $i_{Co}(t)$ as shown in Figure

4.2 and that is when $2\omega t = 3\pi/2$. The lower limit of the integration can be defined as $t_1=T_L/8$.

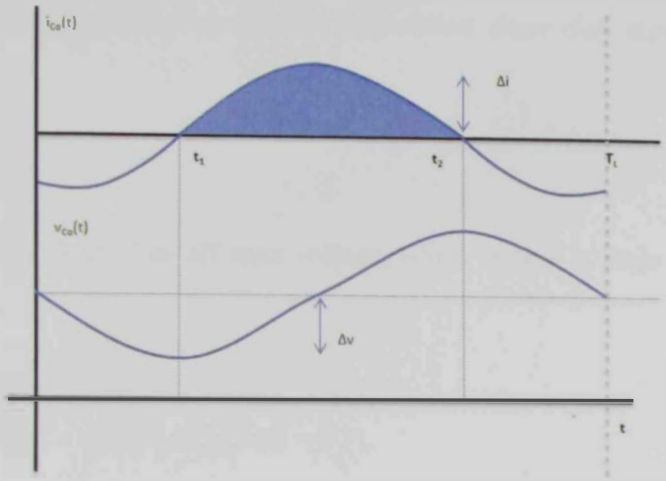

Figure 4.2: Integration limit identification

By solving equation (4.24), the capacitor output voltage ripple is shown as below

$$\Delta v_{Co}(t) = \frac{1}{C_o}\left(\frac{1}{4}\frac{d_1^2 T_s V_M^2}{L_e V_{C1}}\left(\frac{T_L}{8}+\frac{T_L}{4\pi}\right)-\frac{V_o}{R_L}\left(\frac{T_L}{4}\right)\right) \tag{4.27}$$

Using power stage specification to calculate output capacitor voltage ripple, and using equation (3.7) to calculate the pack value of the capacitor C_1 voltage then plug both values in equation (4.29) to get output capacitor value

$$\Delta v_{Co}(t) = 2\% \;\; V_o = 8V \tag{4.28}$$

$$C_o = \frac{1}{\Delta v_{Co}}\left(\frac{1}{4}\frac{d_1^2 T_s V_M^2}{L_e V_{C1}}\left(\frac{T_L}{8}+\frac{T_L}{4\pi}\right)-\frac{V_o}{R_L}\left(\frac{T_L}{4}\right)\right) \approx 250\mu F \tag{4.29}$$

4.4 Semiconductor stresses

The semiconductors' voltage and current stresses for the proposed rectifier are calculated using on-state and off-state equations discussed in section 3. The peak voltages and currents are considered in the calculation since they represent worst condition.

- Switch Q_1

The voltage stress is defined as off state voltage, which occurs at stage 2 (switch is off)

$$v_{Q1-Max} = \frac{V_M + V_o}{2} \tag{4.30}$$

The current stress is the summation of current passing through all inductors as shown in stage 1 mentioned in section 3.

$$i_{Q1}(t) = i_{L1}(t) + i_{L2}(t) + i_{Lo}(t) \tag{4.31}$$

$$I_{Q1-Max} = \int_0^{d_1 T_s} \frac{V_M}{L_e} dt = \frac{d_1 T_s}{L_e} V_M \tag{4.32}$$

- Diodes D_1 and D_o

The voltage stress of both diodes are the same and it is calculated at stage 1 (diode is off)

$$v_{D1-Max} = v_{Do-Max} = \frac{V_M + V_o}{2} \tag{4.33}$$

Diodes peak current stress is half inductors current summation:

$$i_{Do}(t) = \frac{1}{2}((i_{L1}(t) + i_{L2}(t) + i_{Lo}(t)) \tag{4.34}$$

Then, using output diode current waveform shown in Figure 3.8

$$slope = \frac{0 - I_{Do\_Max}}{D_2 T_s} = \frac{-v_{C1}}{2L_e} \tag{4.35}$$

Finally, diodes current stress is

$$I_{Do\_Max} = I_{D1\_Max} = \frac{d_1 T_s}{2L_e} V_M \tag{4.36}$$

- Line frequency diodes D_p and D_n

At positive line cycle, D_p is conducting while D_n is not conducting. On the other hand, D_p will be turned off and D_n will start conducting at negative line cycle. So voltage stress will be the same in magnitude

$$v_{Dn-Max} = v_{Dp-Max} = v_{ac} = V_M \tag{4.37}$$

The current stress is calculated using output power and assuming 100% efficiency

$$I_{Dn-Max} = I_{Dp-Max}(t) = i_{ac} = \frac{2P_o}{V_M} \tag{4.38}$$

CHAPTER 5

Feedback control

5.1 Small signal modelling

To make the design of the control loop of a switching rectifier, it is required to have a transfer function with good approximation representing the dynamic behavior of the converter. The small signal modeling method was used to build a rectifier mathematical model. Since the proposed circuit was designed to operate in DCM, method of the equivalent circuit of the injected current "CIECA" was used to construct the system model [36] and [52]-[56]. The equivalent circuit method of the injected current steps mentioned in chapter 2 were applied on the proposed circuit to obtain the mathematical model

Step 1: Identification of linear and nonlinear elements in PFC rectifier.

In the first stage of modeling, the linear parts are inductors and capacitors, while nonlinear part is represented by switches and diodes.

Step 2: Identification of the equations of the rectifier.

The second step of the modeling is to write the equations of the rectifier which was done in chapter 3. The main equation that is needed in this section is the average output diode current equation over a half-line cycle which is rewritten again in this section:

$$i_o = \frac{d_1^2 T_s}{2L_e} V_M \left(\frac{0.48}{M - 0.92} \right) \qquad (5.1)$$

Using power balance principle and assuming 100% efficiency the average input current over a half-line cycle can be represented by the following relation

$$i_{ac} = \frac{d_1^2 T_s}{L_e} V_o \left(\frac{0.48}{M - 0.92} \right) \tag{5.2}$$

Input current and output current were averaged over half ac line cycle to get rid of the second and higher harmonic components.

Step 3: Small signal perturbation and linearization.

To construct a small signal ac model at a quiescent operating point, some assumptions must be considered such as the input voltage, output voltage, duty cycle and output current are equal to a given quiescent value plus some superimposed small ac variation:

$$v_{ac} = V_M + \hat{v}_{ac},\ v_o = V_o + \hat{v}_o,\ d_1 = D + \hat{d}_1,\ i_o = I_o + \hat{i}_o \ and\ i_{ac} = I_M + \hat{i}_{ac} \tag{5.3}$$

For the previous assumptions, the ac variations are small in magnitude compared to the DC quiescent values

$$\hat{v}_{ac} << V_M,\ \hat{v}_o << V_o,\ \hat{d}_1 << D,\ \hat{i}_o << I_o \ and\ I_M << \hat{i}_{ac} \tag{5.4}$$

The linear result of the input current after perturbation and neglecting DC terms and the non-linear terms resulting from the product of small signal perturbations is a function of the three variables (v_{ac}, v_o and d_1):

$$i_{ac} = f_1(v_{ac}, v_o, d_1) \tag{5.5}$$

Linear equation of input current can be written in a canonical form by using three-dimensional Taylor series expansion about the quiescent point (V_M, V_o, d_1) [28]

$$\hat{i}_{ac} = j_1 \hat{d}_1 + g_1 \hat{v}_o + \frac{1}{r_1} \hat{v}_{ac} \tag{5.6}$$

Where the coefficients (j_1, g_1, r_1) can be calculated by

$$j_1 = \frac{\partial f_1(v_{ac}, v_o, d_1)}{\partial d_1}\Big|_{d_1=\bar{d}_1} = \frac{2d_1T_s}{L_e}V_oV_M\left(\frac{0.48}{V_o - 0.92V_M}\right) \tag{5.7}$$

$$g_1 = \frac{\partial f_1(v_{ac}, v_o, d_1)}{\partial v_o}\Big|_{v_o=V_o} = \left[\frac{(V_o - 0.92V_M)\left(\frac{0.48d_1^2T_s}{L_e}V_M\right) - \left(\frac{0.48d_1^2T_s}{L_e}V_MV_o\right)}{(V_o - 0.92V_M)^2}\right] \tag{5.8}$$

$$\frac{1}{r_1} = \frac{\partial f_1(v_{ac}, v_o, d_1)}{\partial v_{ac}}\Big|_{v_{ac}=V_M} = \left[\frac{(V_o - 0.92V_M)\left(\frac{0.48d_1^2T_s}{L_e}V_o\right) - \left(\frac{(0.44)d_1^2T_s}{L_e}V_MV_o\right)}{(V_o - 0.92V_M)^2}\right] \tag{5.9}$$

Also, the linear result of the output current after perturbation is a function of the three variables (v_{ac}, v_o and d_1):

$$i_o = f_2(v_{ac}, v_o, d_1) \tag{5.10}$$

Using the three-dimensional Taylor series expansion about the same quiescent point (V_M, V_o, D_1), the linear equation of input current can be written as follow:

$$\hat{i}_o = j_2\hat{d}_1 + g_2\hat{v}_{ac} + \frac{1}{r_2}\hat{v}_o \tag{5.11}$$

Where the coefficients (j_2, g_2, r_2) can be calculated by:

$$j_2 = \frac{\partial f_2(v_{ac}, v_o, d_1)}{\partial d_1}\Big|_{d_1=\bar{d}_1} = \frac{d_1 T_s}{L_e} V_M^2 \left(\frac{0.48}{V_o - 0.92V_M} \right) \tag{5.12}$$

$$g_2 = \frac{\partial f_2(v_{ac}, v_o, d_1)}{\partial v_{ac}}\Big|_{v_{ac}=V_M} = \left[\frac{(V_o - 0.92V_M)\left(\frac{0.48 d_1^2 T_s V_M}{L_e} \right) + \left(\frac{(0.22) d_1^2 T_s V_M^2}{L_e} \right)}{(V_o - 0.92V_M)^2} \right] \tag{5.13}$$

$$\frac{1}{r_2} = \frac{\partial f_2(v_{ac}, v_o, d_1)}{\partial v_o}\Big|_{v_o=V_o} = \frac{0.48 d_1^2 T_s V_M^2}{2L_e(V_o - 0.92V_M)} \tag{5.14}$$

Step 4: Obtaining dynamic properties (Transfer Function) and equivalent circuit

At this stage it is possible to obtain from the set of equations described above the transfer functions output-input and output-control. Furthermore, using theses equations the equivalent linear circuit of the proposed circuit can be drawn as illustrated in Figure 5.1 which represents the small-signal properties of the input and output stages for low frequencies.

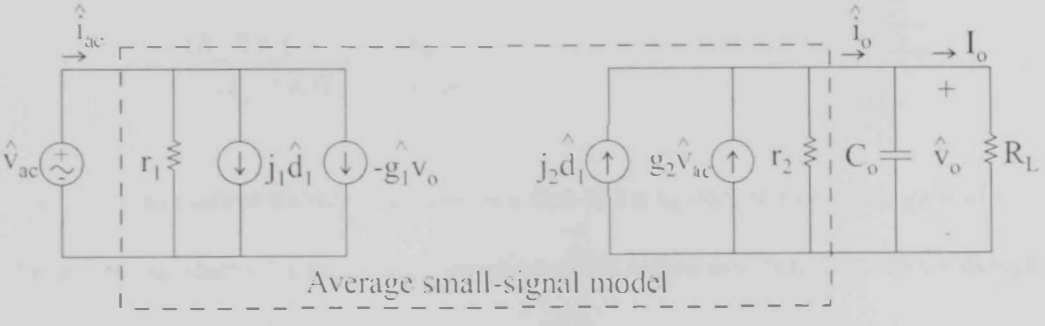

Figure 5.1: Small-signal equivalent circuit for the proposed rectifier.

Mainly the system is modeled using Figure 5.1; the mathematical model consists of three transfer functions (Output-to- Control, Output -to-Input and Output impedance). Each transfer function is constructed as follows:

a) Output-to-Control transfer function:

The transfer function is in the form show in equation (5.15) by ignoring input voltage variations

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big|_{\substack{\hat{v}_{ac}(s)=0 \\ \hat{i}_{Load}(s)=0}} \tag{5.15}$$

Using Figure 5.1, by shorting voltage sources and opening current sources and then applying KCL on the equivalent circuit shown in Figure 5.2, the transfer function can be shown as following:

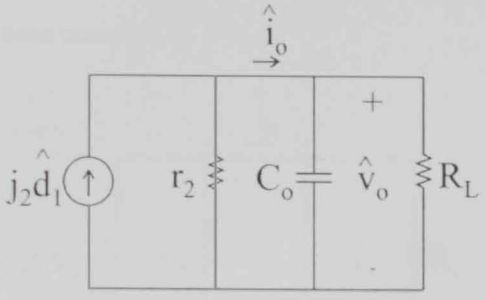

Figure 5.2: Equivalent circuit to get Output-to-control transfer function

$$G_{vd}(s) = \frac{j_2(R_L \,//\, r_2)}{1 + s(C_o(R_L \,//\, r_2))} = \frac{G_{d_0}}{1 + s/\omega_p} \tag{5.16}$$

The output to control transfer function is a first order system with a static gain of G_{do} and a time constant of $1/w_p$. Using operating point mentioned before in circuit design in chapter 4, the transfer function is

$$G_{vd}(s) = \frac{815.15}{1 + s/15} \tag{5.17}$$

b) Output-to-Input transfer function

The transfer function is in the form show in equation (5.24) by ignoring duty cycle variations

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{ac}(s)}\Big|_{\substack{\hat{d}_1(s)=0 \\ \hat{i}_{Load}(s)=0}} \tag{5.18}$$

Same procedures are repeated in Figure 5.1, by shorting voltage sources and opening current sources and then applying KCL on the equivalent circuit shown in Figure 5.3, the transfer function can be shown as following:

$$G_{vg}(s) = \frac{g_2(R_L // r_2)}{1 + s(C_o(R_L // r_2))} = \frac{G_{go}}{1 + s/\omega_p} \tag{5.19}$$

The output to input transfer function is also a first order system with a static gain of G_{go} and with a similar time constant of $1/w_p$.

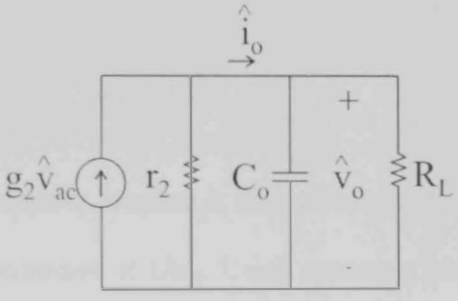

Figure 5.3: Equivalent circuit to get output-to-input transfer function

Using the same operating point mentioned before in circuit design in chapter 4, the transfer function is

$$G_{vg}(s) = \frac{2.35}{1 + s/15} \tag{5.20}$$

c) Output impedance transfer function

Finally, Output impedance transfer function is also required to perfectly model the proposed circuit.

$$Z_{out}(s) = -\frac{\hat{v}_o(s)}{\hat{i}_{Load}(s)}\Big|_{\substack{\hat{d}_1(s)=0 \\ \hat{v}_{ac}(s)=0}} \tag{5.21}$$

Same procedures are repeated in figure 5.1, by shorting voltage sources and opening current sources and then applying KCL on the equivalent circuit shown in Figure 5.4, the transfer function can be shown as following:

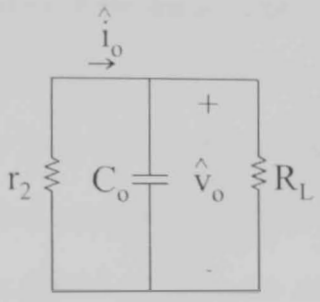

Figure 5.4: Equivalent circuit to get output impedance transfer function

$$Z_{out}(s) = \frac{r_2 // R_L}{1 + sC_o(r_2 // R_L)} = -\frac{G_{zo}}{1 + s/\omega_p} \tag{5.22}$$

The Output impedance transfer function is also a first order system with a static gain of G_{zo} and with a time constant of $1/w_p$. Using operating point mentioned before in circuit design in chapter 4, the transfer function is

$$Z_{out}(s) = \frac{305.3}{1 + s/15} \tag{5.23}$$

It is clear that the three transfer functions are consisting of one stable pole with no right half plane zeros or poles. The three transfer functions were simulated in Matlab using steady state operating point and compared with switch model result to ensure that the approximated mathematical modeling of the rectifier is accurate. Firstly, a small variation step was applied to the duty cycle and the output voltage waveform was plotted in Figure 5.5 for both mathematical model shown in equation 5.17 and switch model. It is obvious that both curves have the same specification

which means that output to duty cycle transfer function shown in equation 5.17 is accurate approximation for switch model response to duty cycle variation. Secondly, a small step variation was applied at the input voltage and system response of the mathematical model shown in equation (5.20) and the switch model was plotted in Figure 5.6. This figure clearly shows that both curves are almost identical which ensures that approximated mathematical model shown in equation (5.20) is correct. Finally, a small disturbance was applied at the load to check the validity of the output impedance mathematical model shown in equation (5.23). By observing Figure 5.7, the estimated output impedance small-signal model results and switch model simulation results are consistent. Therefore, simulation results have shown the validity of the design approach and small-signal model presented.

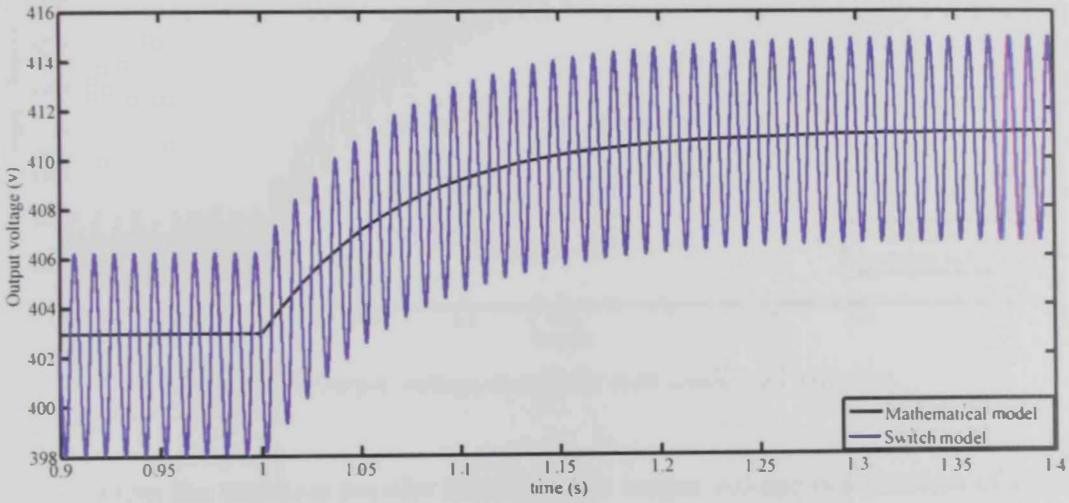

Figure 5.5: Output voltage waveform with small duty cycle variation.

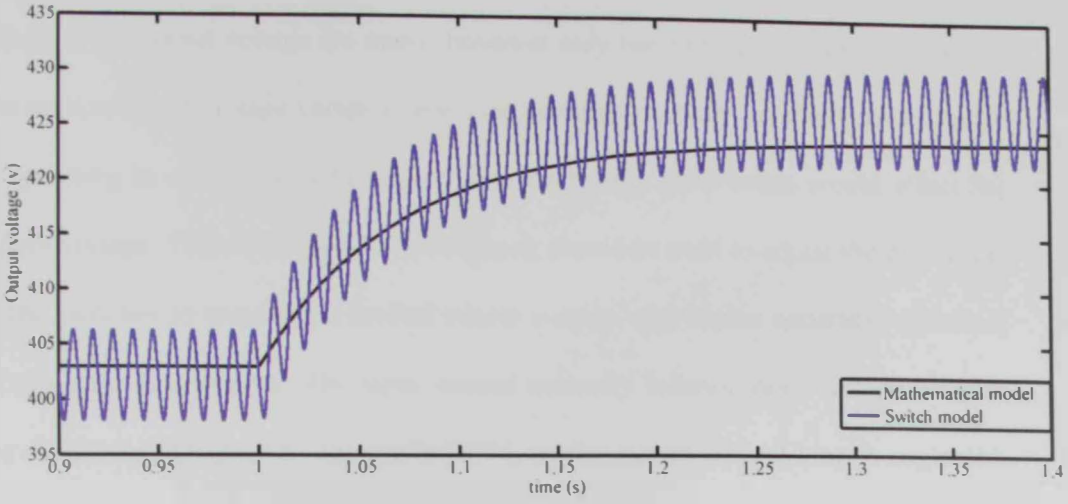

Figure 5.6: Output voltage waveform with small input voltage variation.

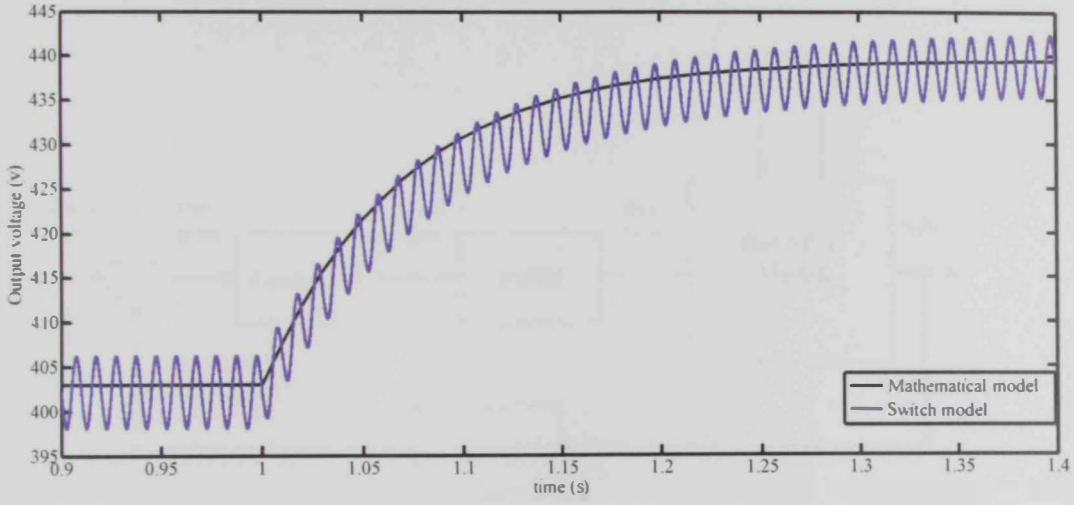

Figure 5.7: Output voltage waveform with small load variation.

From the previous transfer functions, the output voltage is a function of input voltage, duty cycle and load current as illustrated in Figure 5.8. In AC-to-DC rectifiers it is desired to produce a regulated output voltage and an input current that follows input voltage profile, so that it appears as an emulated resistor from the input side to ensure almost unity power factor. The output voltage must be constant with small accepted fluctuations around the steady state value in spite of the disturbances

in input line voltage or load current. The source of disturbances and variations affecting the output voltage are many, however only two of them will be discussed in this section: input voltage variation and load variation. Actually, if the rectifier circuit is operating in open loop with a fixed duty cycle, any disturbance would affect the output voltage. Therefore, a negative feedback should be used to adjust the duty cycle of the switches to acquire the desired output voltage with higher accuracy regardless of available disturbances. The input current naturally follows input voltage because the circuit was designed to operate in DCM, so the current control loop is neglected. Figure 5.8 depicts the functional block diagram of feedback system for regulation of the output voltage.

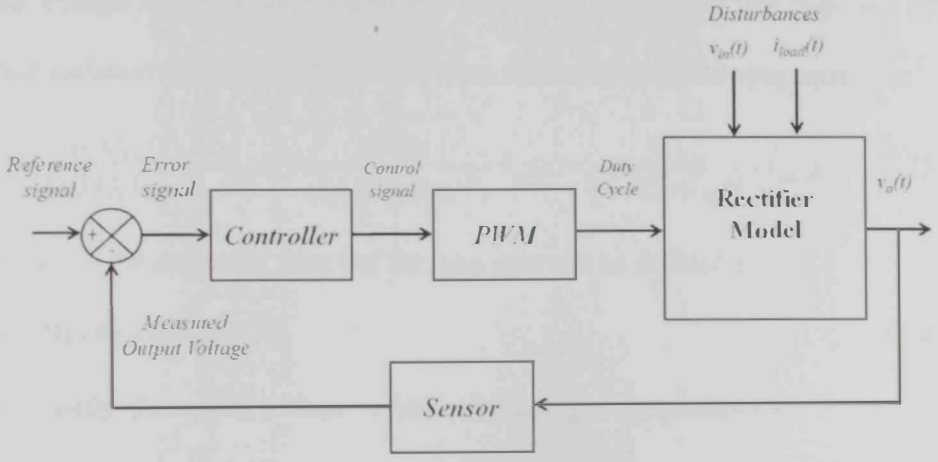

Figure 5.8: The block diagram representing the feedback system.

The output voltage is measured using a sensor (H) which is practically a voltage divider. The sensor is represented by a gain of (3/80) that ensures getting 15 volts to be compared with a reference of 15 volts. V_P represents the peak value of the modulating signal used in PWM and it was selected to be 15. Therefore the main objective is to make output voltage of the sensor equal reference signal regardless of

disturbances which means reducing error signal. The small signal model of the proposed circuit mentioned previously is used to design the feedback system and to study its effects with existing of disturbances. The loop gain T(s) is defined as the product of the small signal gains in the forward and feedback paths of the feedback loop [28]. The output voltage variation can be expressed as a linear combination of the three independent inputs: the input voltage variation, control input variation and the load current variation as follows:

$$\hat{v}_o(s) = G_{vd}(s)\hat{d}_1(s) + G_{vg}(s)\hat{v}_{ac}(s) - Z_{out}(s)\hat{i}_{Load}(s) \tag{5.24}$$

Adding a feedback controller will increase the value of the loop gain that will cause reduction in the disturbance effect. The transfer function from disturbance to the output voltage will be multiplied by the factor (1/ (1+T(s)). In this case, the output voltage variation can be rewritten in the form shown by the following equations:

$$\hat{v}_o(s) = \frac{G_c G_{Vd}/V_p}{1 + HG_c G_{vd}/V_p}\hat{v}_{ref}(s) + \frac{G_{vg}}{1 + HG_c G_{vd}/V_p}\hat{v}_{ac}(s) - \frac{Z_{out}}{1 + HG_c G_{vd}/V_p}\hat{i}_{Load}(s) \tag{5.25}$$

Where G_C is the controller gain and the loop gain can be defined as:

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_p \tag{5.26}$$

Consequently, the output voltage variation including a compensator is:

$$\hat{v}_o(s) = \frac{1}{H}\frac{T}{1+T}\hat{v}_{ref}(s) + \frac{G_{vg}}{1+T}\hat{v}_{ac}(s) - \frac{Z_{out}}{1+T}\hat{i}_{Load}(s) \tag{5.27}$$

Therefore, when the loop gain T is large in magnitude, the effect of the disturbance on the output voltage will be reduced. In addition, a large loop gain will cause the output voltage to be close to the reference input. In the following section the controller will be designed using loop gain and bode plot.

5.2 Close loop analysis

Adding a feedback loop could affect the system stability. A method given by the Nyquist stability theorem called the phase margin criterion is used for stability checking [28]. When the phase margin of the loop gain T is positive, the system is stable. From equation (5.27) it is clear that if the loop gain is large the disturbance effect will be small.

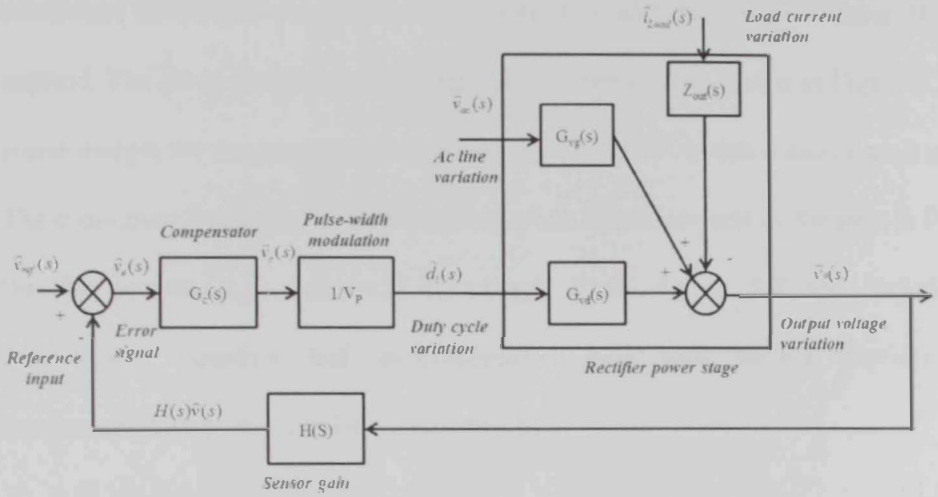

Figure 5.9: Complete block diagram of voltage regulator system using small signal model

5.2.1 Controller design

The Lag compensator was selected to be used to close the loop of the proposed circuit such that the output voltage is better regulated in the presence of the variations in line voltage and load resistance. The transfer function of the lag compensator is:

$$G_C(s) = G_{C\infty}\left(1+\frac{\omega_L}{s}\right) \tag{5.28}$$

Where $G_{C\infty}$ is the high frequency gain of the compensator and ω_L is the corner frequency. Using Figure 5.9 and assuming G_C=1, the uncompensated loop gain (T_{OL}) can be represented as following:

$$T_{OL} = \frac{H}{V_p} G_{Vd} = \frac{2.04}{1 + s/15} = \frac{T_{OLo}}{1 + s/\omega_o} \tag{5.29}$$

Where T_{OLo} is uncompensated loop gain DC gain and ω_o is the system pole. As mentioned in the previous section the controller will be designed using Bode plot method. The Bode plot for the uncompensated loop gain is shown in Figure 5.10. The phase margin for the uncompensated loop gain is +119° which means that it is stable. The cross over frequency is the frequency when the magnitude of the gain is 0 dB and for this system it is (ω_c = 25.4 rad/sec). From Figure 5.8 and including lag compensator equation and uncompensated loop gain shown previously, the compensated loop gain can be represented by:

$$T_{CL} = T_{OL} G_C(s) \tag{5.30}$$

Compensated loop gain asymptotes can be approximated at high frequencies:

$$\|T_{CL}\| = \frac{T_{OLo} G_{C\infty}}{\omega / \omega_o} \tag{5.31}$$

Crossover frequency is selected to be well below twice the line frequency, to avoid excessive second-harmonic injection from the output voltage into the input current (resulting in third-order harmonic current) [35, 45].

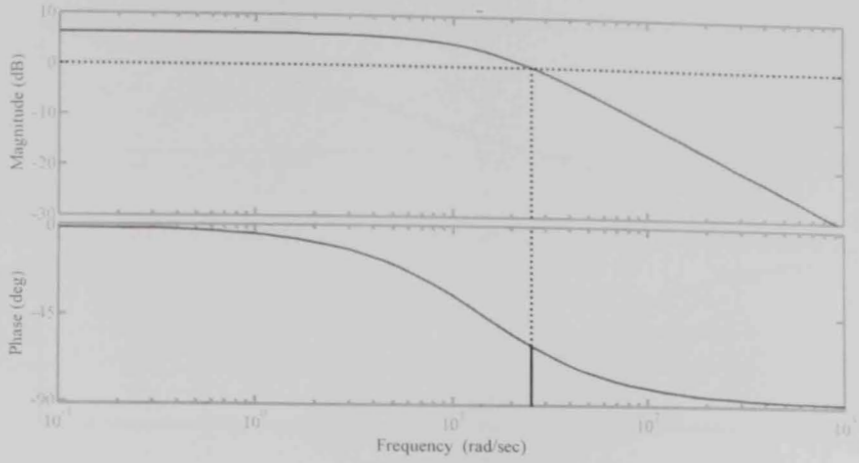

Figure 5.10: Magnitude and phase of uncompensated loop gain.

It is known that at cross over frequency the gain is unity (0 dB), therefore the compensator gain $G_{c\infty}$ can be calculated from equation (5.31):

$$G_{C\infty} = \frac{T_{OLo}\omega_o}{\omega_c} \tag{5.32}$$

Using equation (5.32) and selecting crossover over frequency around 10 Hz, the lag compensator is represented by:

$$G_C(s) = 2\left(1 + \frac{100}{s}\right) \tag{5.33}$$

As mentioned in the previous sections, stability is affected by adding a feedback control. The phase margin criterion is used for stability check including the lag compensator.

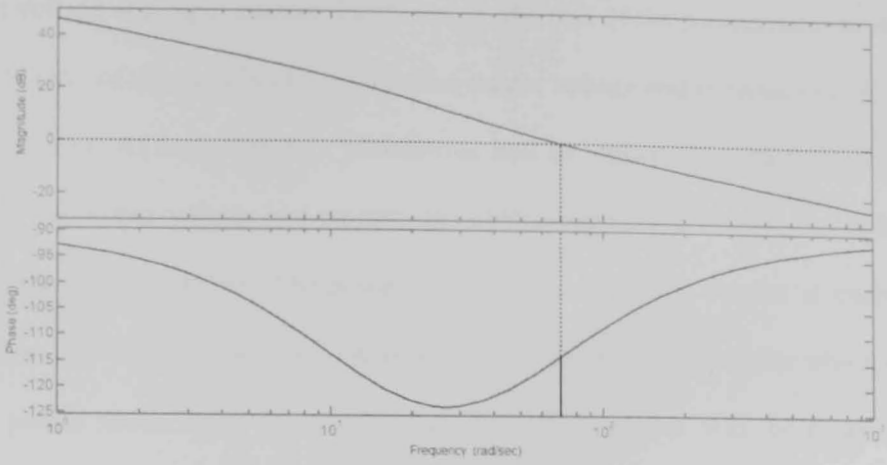

Figure 5.11: Magnitude and phase of compensated loop gain.

It is clear that the system is still stable due to positive phase margin at the crossover frequency, despite the drop in phase margin compared with the uncompensated loop gain in Figure 5.10.

5.3 Feedback control for the switch model

The proposed circuit was built using PLECS 3.4.1 software to test its operation with feedback control loop. As mentioned in the previous sections that controller is used to regulate the output voltage around the desired set point and to remove disturbances caused by load variations and input voltage variations. In this section four cases of variations will be discussed to test the controller performance on the switch model of the proposed circuit displayed in Figure 5.12. The first case is dropping the load by 50%, the second case is load increase by 25%, the third case is input voltage increase by 20% and the last case is voltage decrease by 15%. Several issues are discussed in each case, mainly the effect of each variation condition on the

output voltage and input current. Furthermore, the role of the compensator to modify the duty ratio of the switches to regulate the output voltage and to reduce the effect of the variations. At each case four waveforms will be shown (The input voltage and current, the output voltage and current, the control signal and finally, the switching signal fed to the switches. The power balance ($P_{in} = P_{out}$) is proven at each case. Moreover, the input current was kept following the input voltage profile which means unity power factor and Harmonics reduction. The circuit was built using the following operating point:

1. Input voltage: 120 V at 50Hz
2. Output voltage: 400 V
3. Output power: 200 W.
4. Switching frequency f_s = 50 kHz

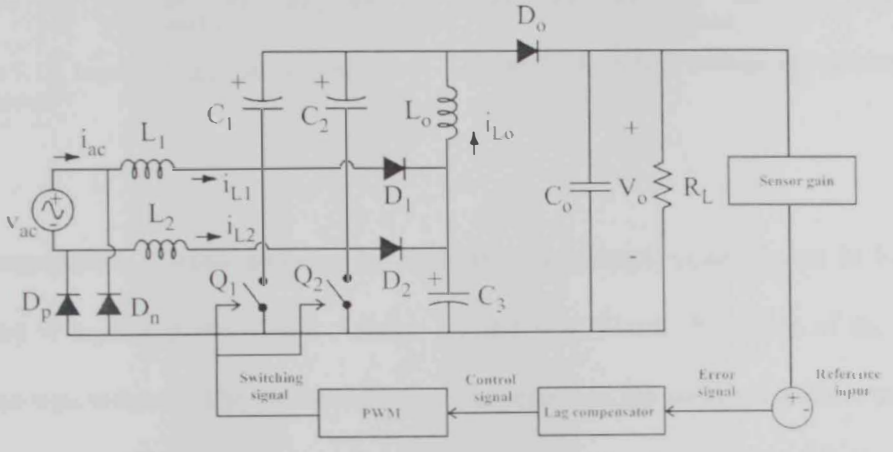

Figure 5.12: Switch model with feedback control.

5.3.1 Case 1: Power drop

The power was changed from 200 watt to 100 watt and the effect of this variation was illustrated in the following figures. From Figure 5.13, it is clear that the input current follows the input voltage profile even when it was dropped. Comparing

the effect of load drop on the input side at Figure 5.13 and on the output side at Figure 5.14, the power balance is attained since the input current reduced due to output current reduction.

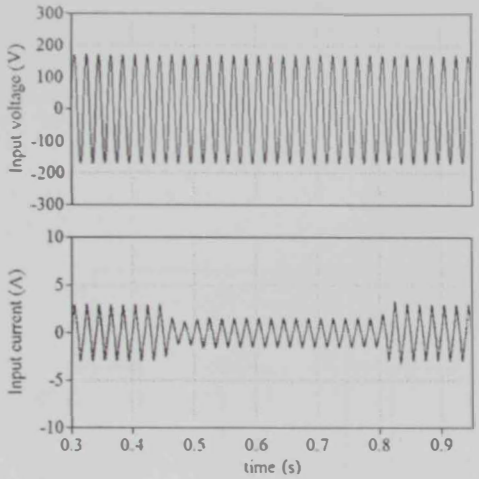

Figure 5.13: Input voltage and current waveforms

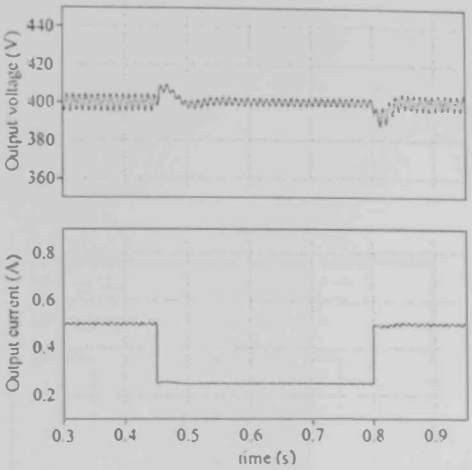

Figure 5.14: Output voltage and current

The compensator worked properly by changing the control signal shown in Figure 5.15 and it regulated the output voltage around 400 V and the effect of the load variation was reduced. The switching signal that controls the switches is illustrated in Figure 5.16 at normal operation while the switching during load variation is depicted in Figure 5.17. It is obvious that the duty cycle was reduced from 0.37 to 0.28 to compensate for the applied variation.

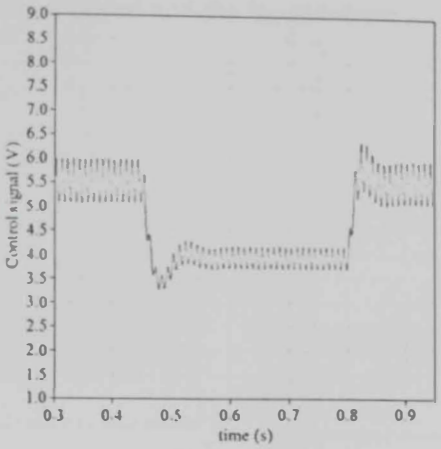

Figure 5.15: Control signal

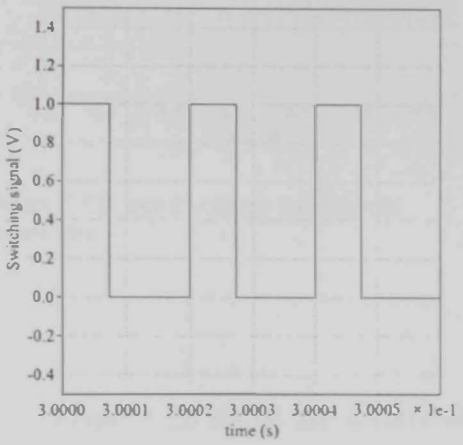

Figure 5.16: Duty cycle before applying variation

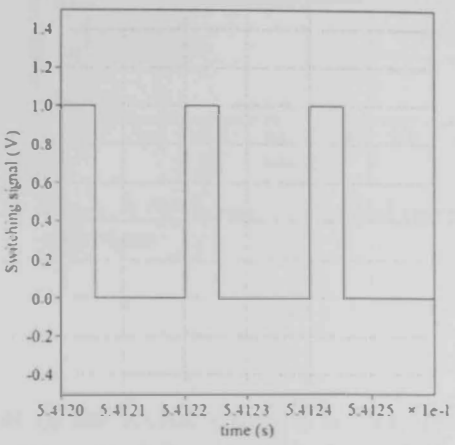

Figure 5.17: Duty cycle during variation

5.3.2 Case 2: Load rise

The load was increased by 25% since the proposed circuit was designed to operate in DCM which means it is applicable at low power load less than 300 watts, therefore the load was increased to 250 watt and the effect of this increase is the opposite of load drop is shown in the following figures. The load current increased

because load resistance has dropped and the input current increased to achieve power balance.

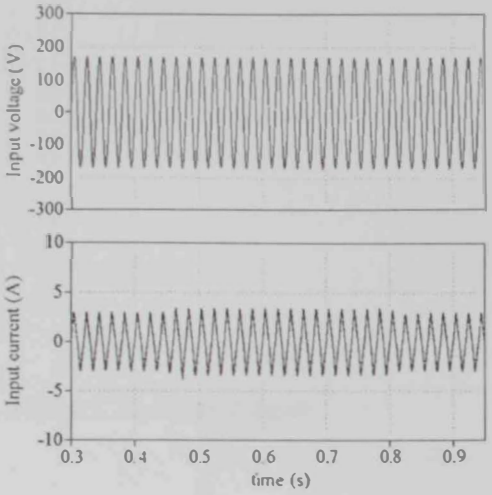

Figure 5.18: Input voltage and current waveform

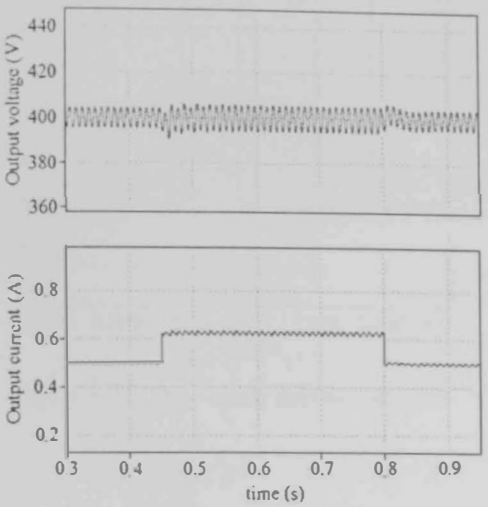

Figure 5.19: Output voltage and current waveform

Figure 5.20 shows the control effort of the compensator, it is clear that the control signal increase to compensate for the load rise and this causes the duty cycle to increase to about 0.41 to increase current drawn from the source as presented in Figure 5.21.

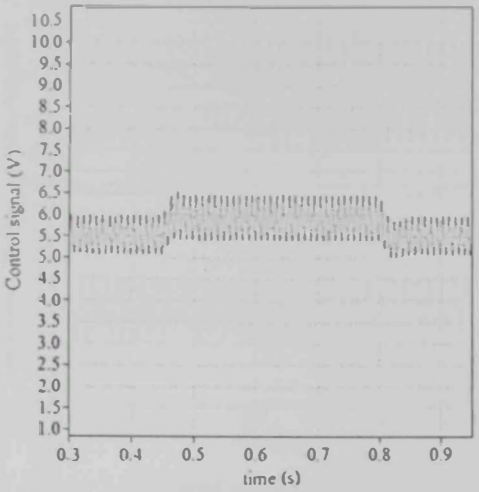

Figure 5.20: Control signal

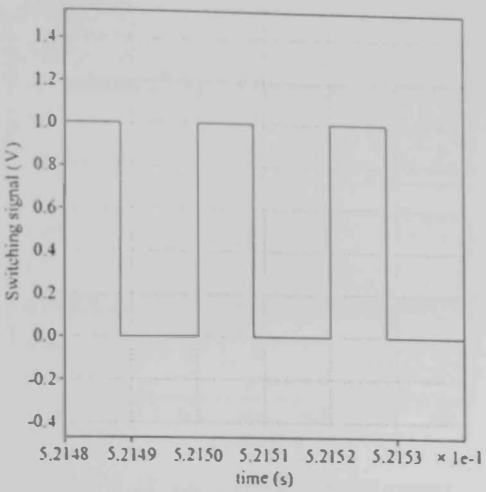

Figure 5.21: Duty cycle during variation

5.3.3: Case 3: Input voltage increase

To simulate the input voltage variation, the voltage peak value increased by 20% from 170 V to 200 V, then the effect of this variation was depicted as follow. Figure 5.22 shows that input current was reduced as a result of the input voltage variation. The compensator reduced the control signal as shown in Figure 5.24 to compensate for voltage variation and as a result the duty cycle is reduced to about 0.27 as illustrated in figure 5.25.

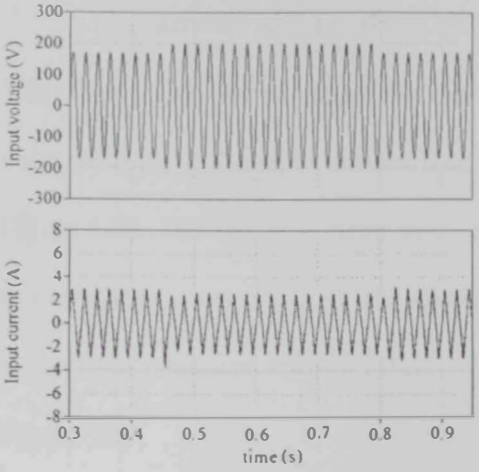

Figure 5.22: Input voltage and current waveform

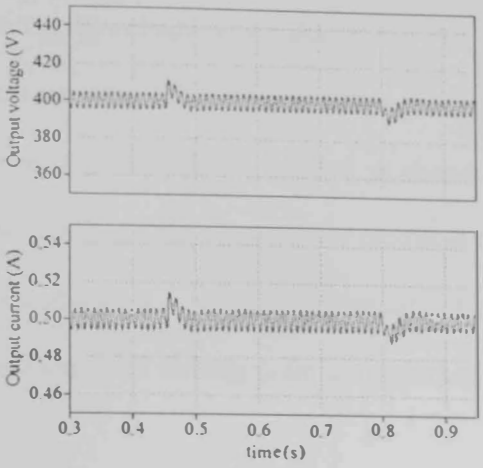

Figure 5.23: Output voltage and current waveform

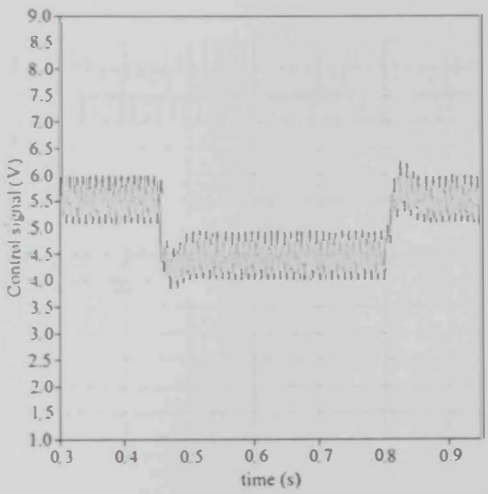

Figure 5.24: Control signal

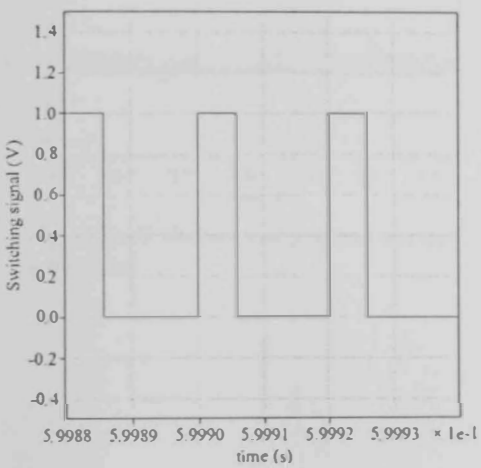

Figure 5.25: Duty cycle during variation

5.3.4 Case 4: Input voltage drop

The last case was simulated by reducing the voltage peak value from 170 V to 150 V and then the effect of this variation was shown as follow. Since the input voltage dropped the input current was increased to keep power balance as shown in Figure 5.26. The output voltage was dropped and then the compensator modified the duty cycle to compensate for the applied disturbance and regulate the output voltage around the reference voltage (400 V) with about 0.05 settling point as presented in Figure 5.27.

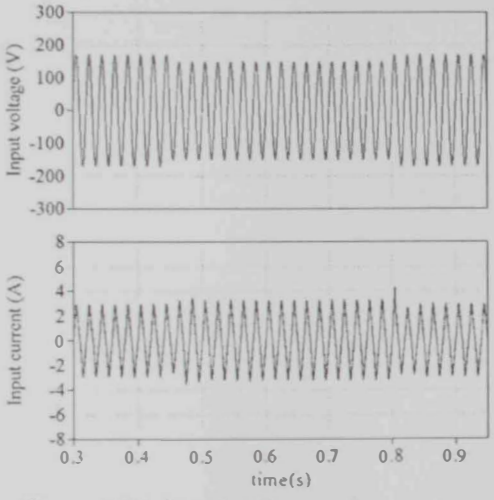

Figure 5.26: Input voltage and current waveform

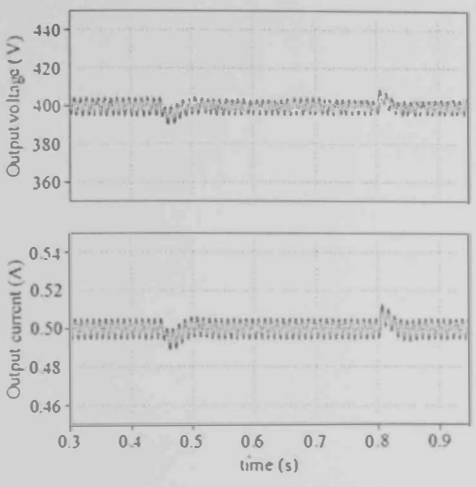

Figure 5.27: Output voltage and current waveform

In this case the controller increase the control signal in order to increase the duty cycle to (0.46) that control the switches to allow the circuit to draw more current from the input source to preserve power balance as shown in Figure 5.28 and Figure 5.29.

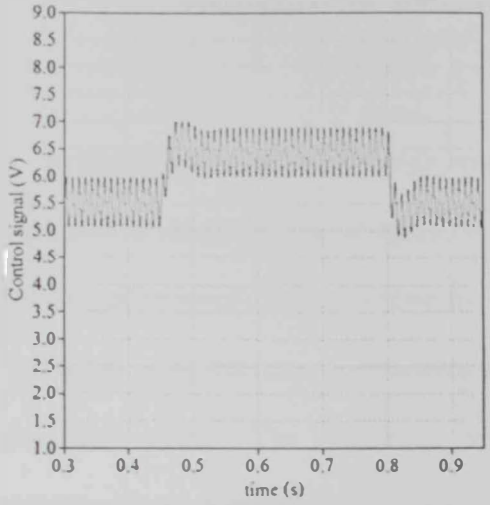

Figure 5.28: Control signal

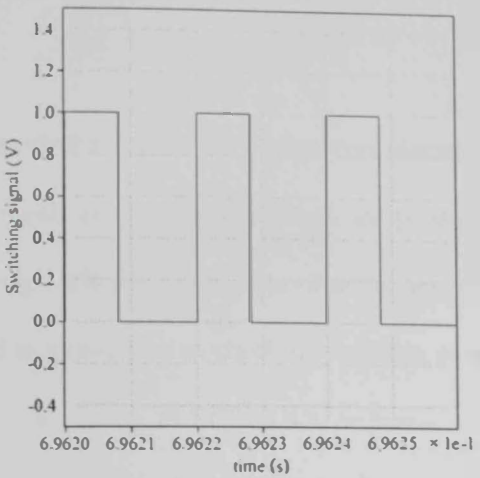

Figure 5.29: Duty cycle during variation

CHAPTER 6

Simulation and experimental results

In this chapter, the rectifier was implemented based on the design considerations explained in chapter 4. The designed components are simulated to check the proposed circuit performance and to validate the design criteria. Then, experimental test was conducted using the same components used in simulation to check the validity of the simulation results. The simulation was done using PLECS 3.4.1 software. All components were modeled with losses, to make the simulation close to the practical. Typical rectifier waveforms are presented for both simulation and experimental. As mentioned in chapter 3, the circuit consists of two parallel configurations that are symmetrical, one configuration operates in positive cycle and the other operates in negative cycle. As a result, the simulated and experimental result of some components will not be shown due to the similarity.

6.1 Input voltage and current

One of the main objectives of the proposed circuit was to make the input current follow the input voltage profile to ensure unity power factor. The simulated waveform of input current and voltage are shown in figure 6.1 and it is clear that the input current follows the input voltage. A validation of the simulation result is illustrated in Figure 6.2. The experimental result is so close to the simulated result.

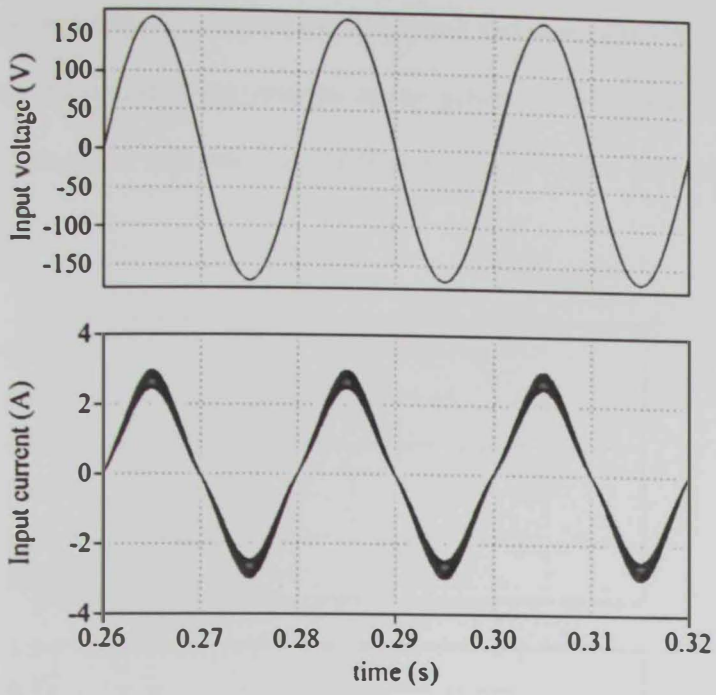

Figure 6.1: Simulation results: Input voltage and input current.

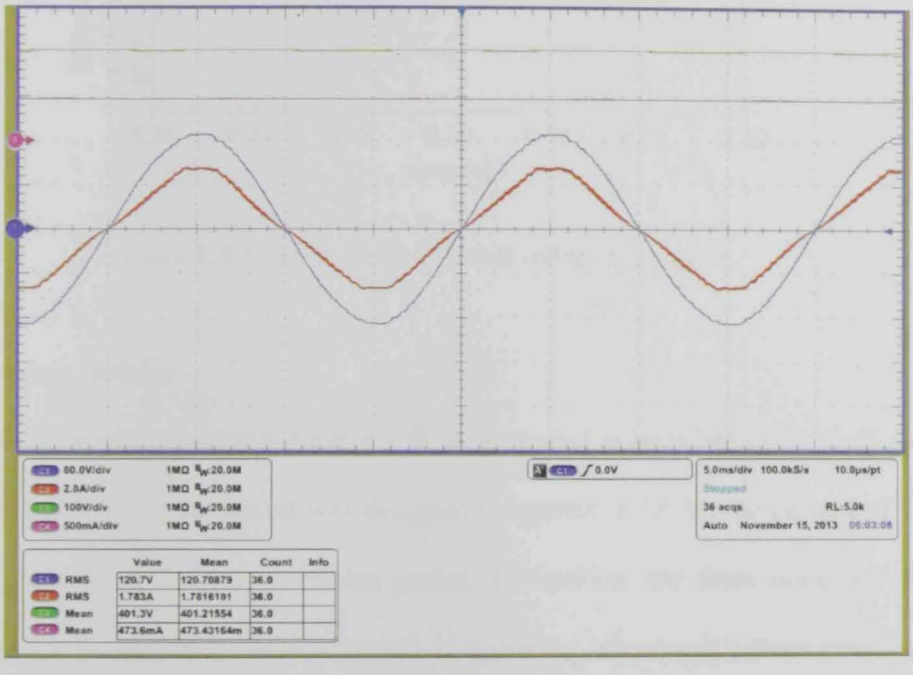

Figure 6.2: Experimental results: Input (voltage in blue and current in red) and output (voltage in green and current in purple).

6.2 Output voltage and current

The circuit was designed to produce 400 V and a current of 0.5 A. Figure 6.3 clearly shows that the designed components assure achieving the operating point in simulation. furthermore the experimental result presented in Figure 6.2 validated the simulated results.

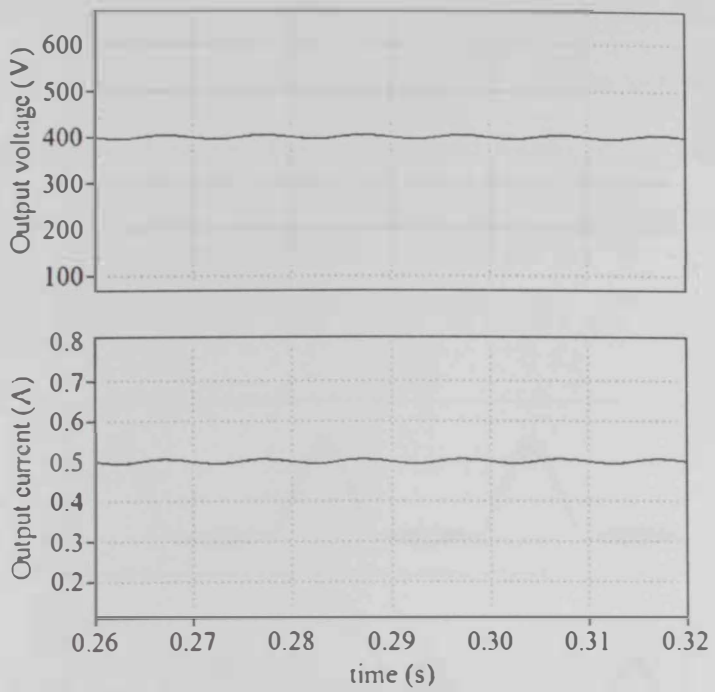

Figure 6.3: Simulation results: Output voltage and current.

6.3 Inductors current

In this section inductors current will be presented at both line cycle level and switching level. Since the circuit was designed to operate in DCM, the current of all inductors should be fixed at switching period. In addition, the three inductors are being charged by the input when switch Q_1 is operating, however the three inductors

are discharging through the output capacitors when the switch is turned off and diodes D_1, D_2 and D_o are conducting.

6.3.1 Current passing through inductors at line scale

Figure 6.4 represent the simulation result of inductors L_1, L_2 and L_o. It is clear that inductors L_1 and L_2 operate within half line cycle inductor L_1 operates at positive half line cycle while inductor L_2 operates at negative half line cycle. However, inductor L_3 operates in the whole line cycle since it is common in both symmetrical configurations mentioned above. The experimental results of the three inductors current are shown in Figures 6.5 and 6.6. Both experimental results and simulation results are identical.

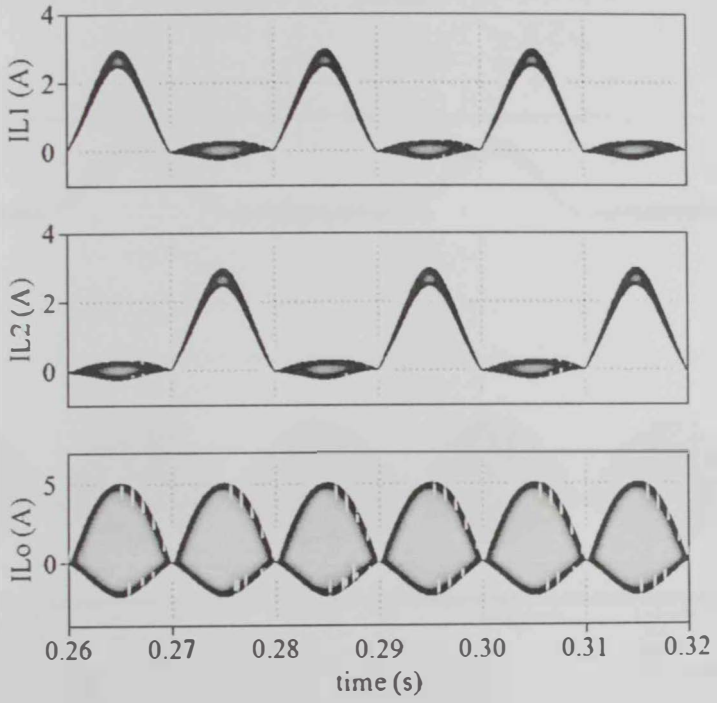

Figure 6.4: Simulation results: Inductor line-cycle level current.

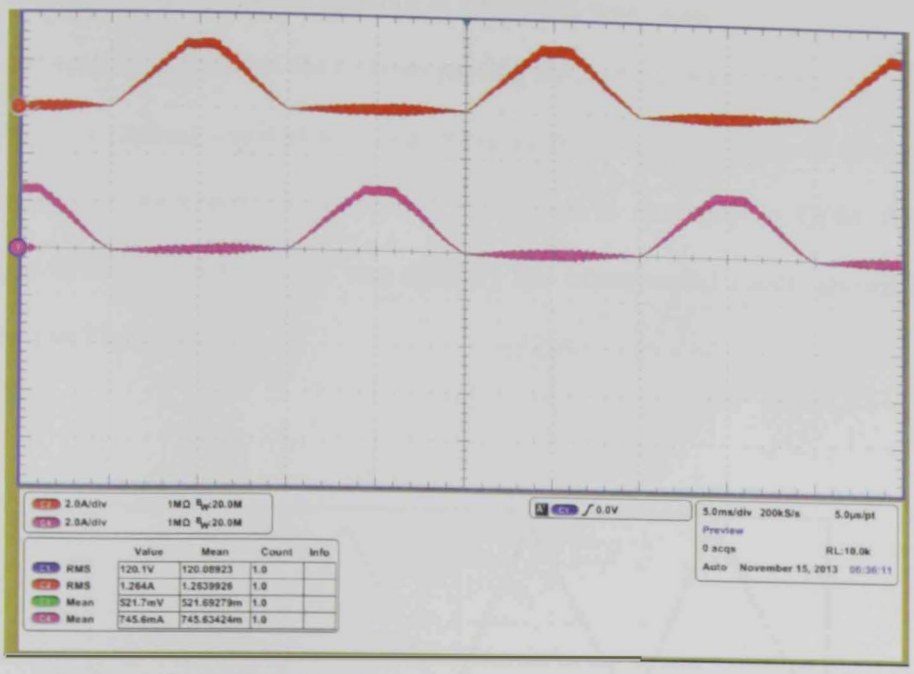

Figure 6.5: Experimental results: Inductors line-cycle level current (L_1 in red and L_2 in purple).

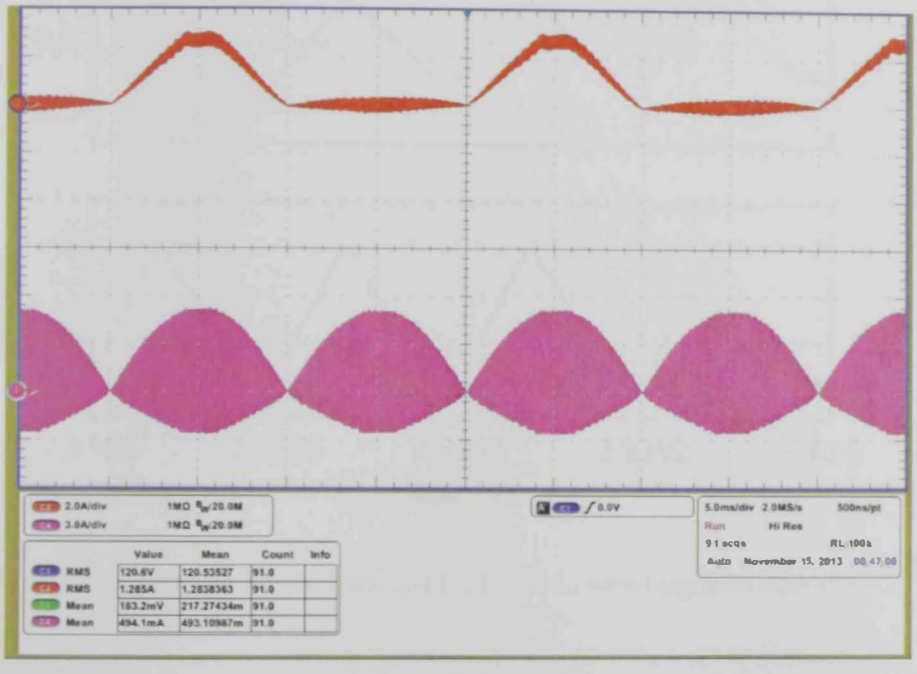

Figure 6.6: Experimental results: Inductors line-cycle level current (L_1 in red and L_o in purple).

6.3.2 Current passing through inductors at switching-time scale

The simulation result of the currents passing through the three inductors L_1, L_2 and L_o during switching cycle is depicted in Figure 6.7. This figure proves that the used components were well designed and the circuit is operating in DCM. The verification of the simulated result was done by the experimental results shown in Figure 6.8 and Figure 6.9.

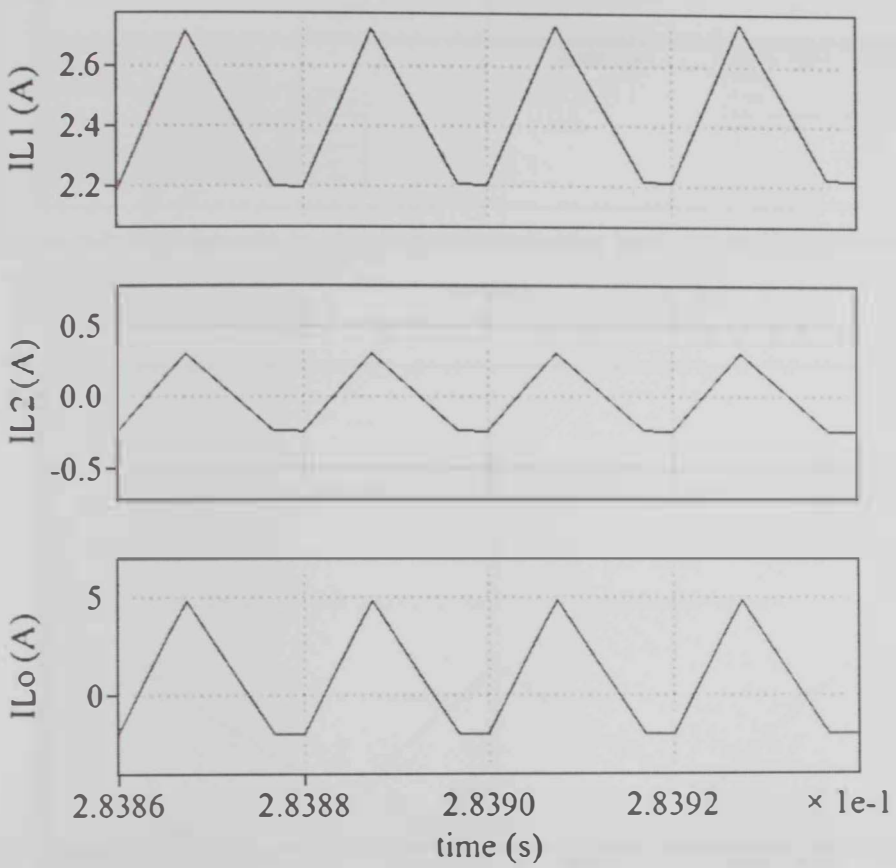

Figure 6.7: Simulation results: Inductors L_1, L_2 and L_o switching level current.

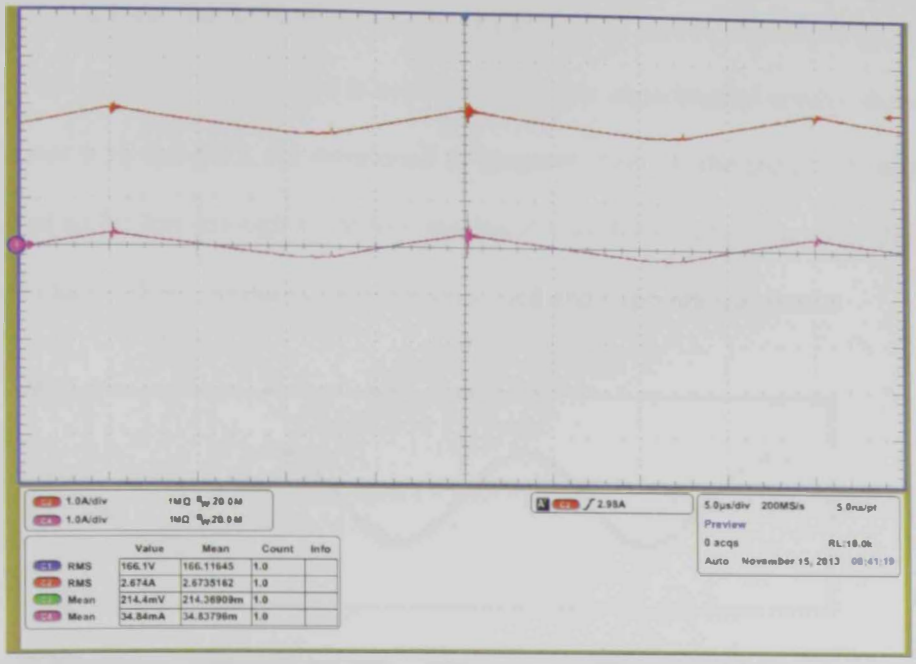

Figure 6.8: Experimental results: Inductors switching level current (L_1 in red and L_2 in purple).

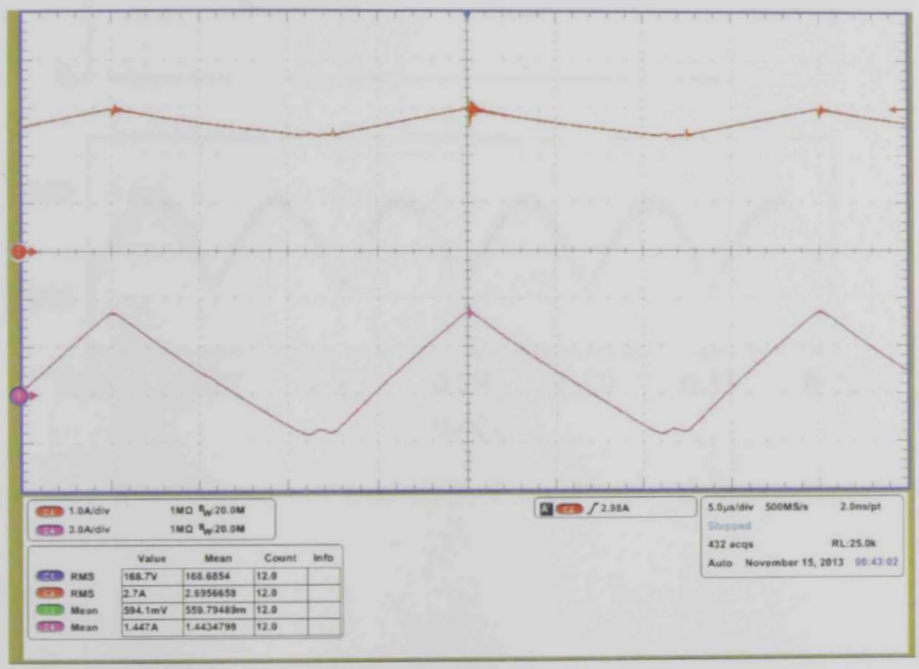

Figure 6.9: Experimental results: Inductors switching level current (L_1 in red and L_o in purple).

6.4 Voltage across capacitors

In this section, the simulation results of the voltage across capacitors C_1, C_2 and C_3 are shown in Figure 6.10 is compared with the experimental results shown in Figures 6.11 and 6.12. As mentioned in chapters 3 and 4, the capacitors were designed to be low enough to follow the input waveform. The following three figures clearly show similarity between simulated and experimental results

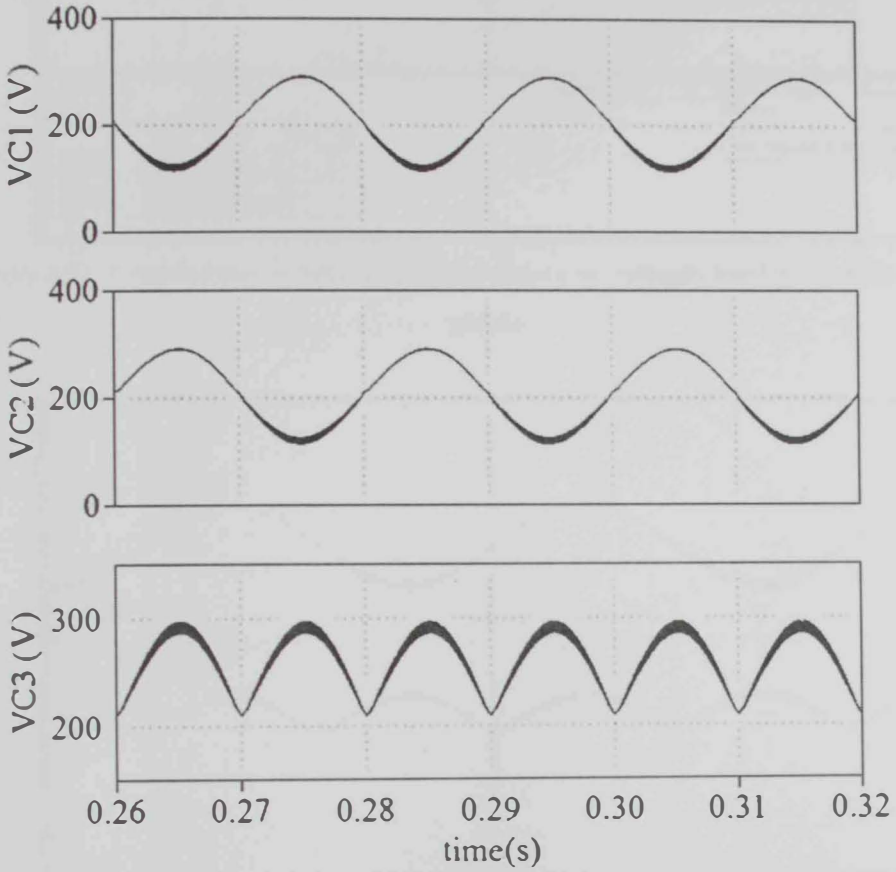

Figure 6.10: Simulation results: Capacitors C_1, C_2 and C_3 line-cycle level voltages.

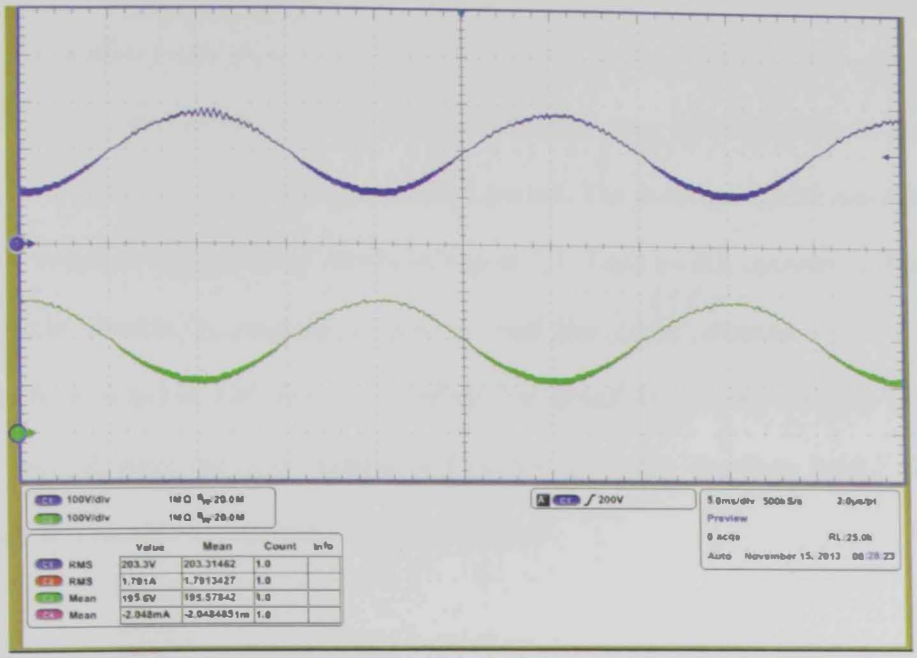

Figure 6.11: Experimental results: Capacitors line-cycle voltages level (C_1 in blue and C_2 in green).

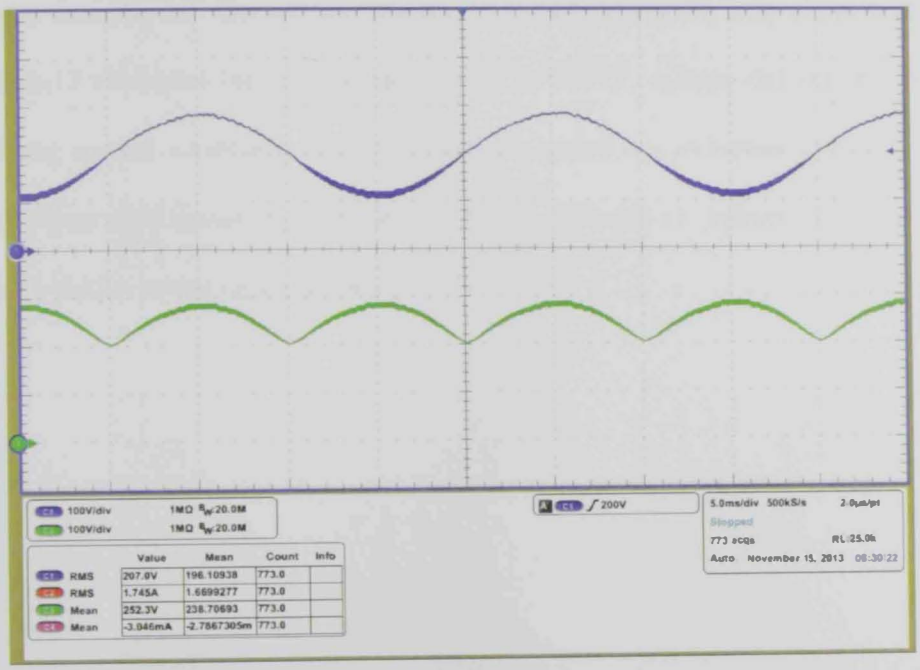

Figure 6.12: Experimental results: Capacitors line-cycle voltages level (C_1 in blue and C_o in green).

6.5 Switch Q_1 voltage and current

This section is divided into two subsections. The first subsection is about switch voltage and current during line cycle while the other subsection focuses on switch voltage and current during switching period. The proposed circuit consists of two switches Q_1 and Q_2 as shown in Figure 3.1. Each switch operates in half line cycle. Switch Q_1 conducts at positive half line cycle, whereas switch Q_1 conducts at negative half line cycle. Since the circuit is symmetrical, the two switches will have the same voltage and current stresses. Therefore, switch Q_1 voltage and current waveforms will be mentioned.

6.5.1 Switch Q_1 line-cycle level voltage and current

At positive half line cycle, switch Q_1 will turn on by input duty cycle (0.37) causing charging of the energy storage elements (inductors and capacitors). Figure 6.13 illustrates the simulation result of switch Q_1 voltage and current. By observing current waveform, it is clear that the switch is conducting in half line cycle. Figure 6.14 shows the experimental result of switch Q_1 voltage and current which is similar to the simulated result.

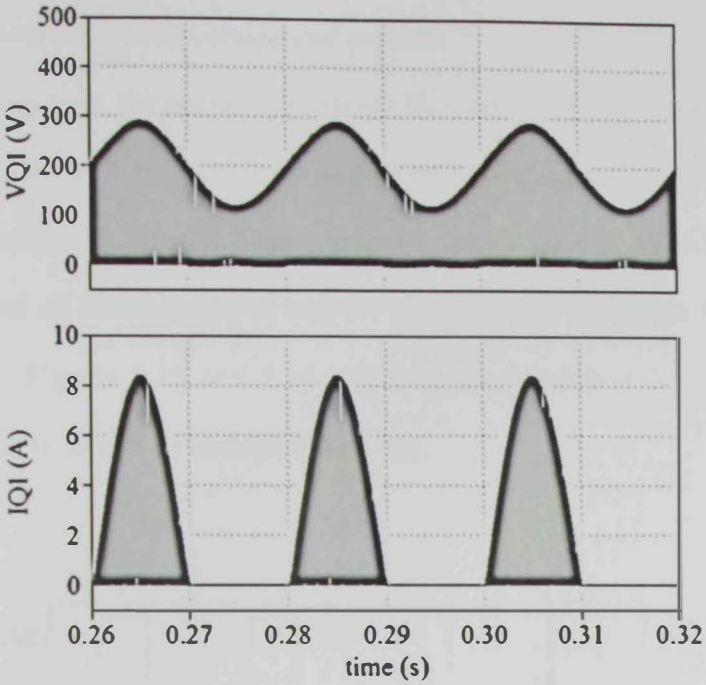

Figure 6.13: Simulation results: Switch Q_1 line-cycle level voltage and current.

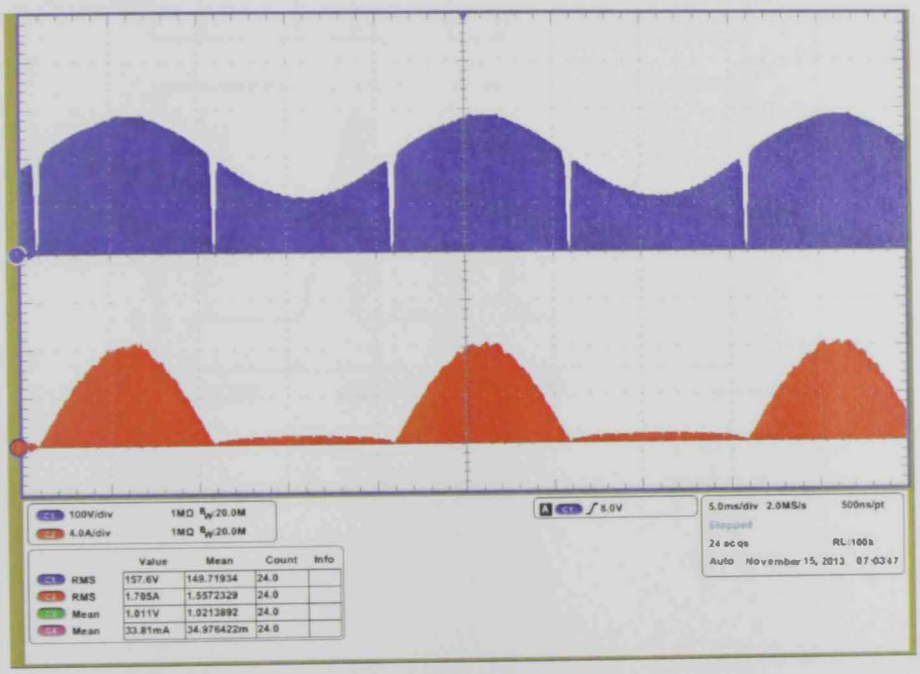

Figure 6.14: Experimental results: Switch Q_1 line-cycle level voltage in blue and current in red.

6.5.2 Switch Q_1 switching level voltage and current

At switching level, the operation of switch Q_1 consists of three stages. Firstly, at stage one (d_1T_s) the switch Q_1 is turned on causing its voltage to be zero while the current is increasing with positive slope. Secondly, at the second stage (d_2T_s) the switch Q_1 is turned off resulting in zero current. Finally, at the third stage the switch will remains off. Figures 6.15 and 6.16 represent the simulation result and the experimental result of switch Q_1 voltage and current.

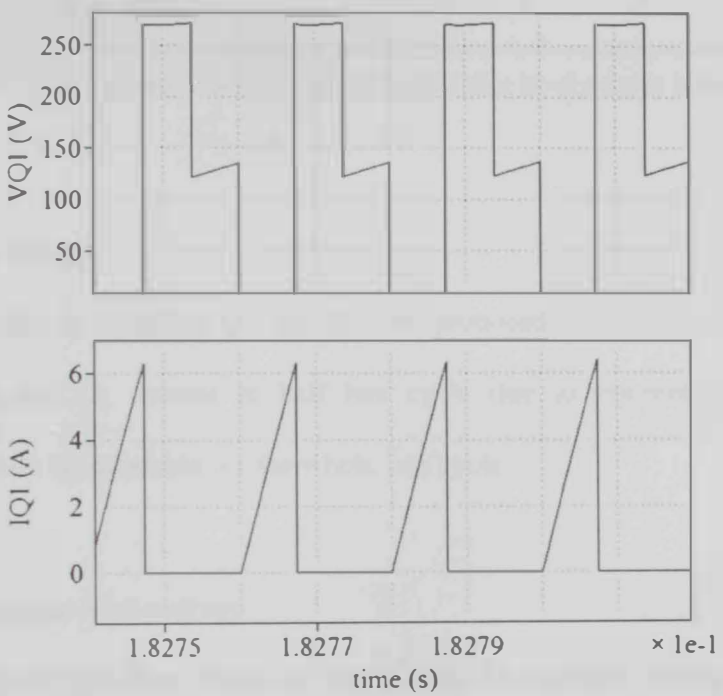

Figure 6.15: Simulation results: Switch Q_1 switching level voltage and current.

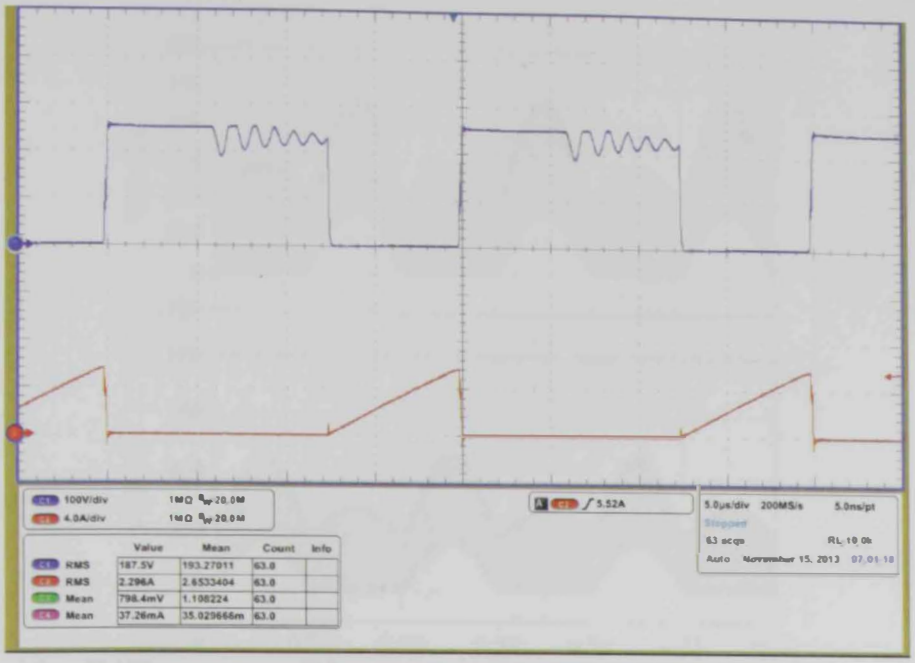

Figure 6.16: Experimental results: Switch Q_1 switching level voltage in blue and current in red.

6.7 Diodes voltage

Similar to switches Q_1 and Q_2, the proposed circuit contains three diodes. Diodes D_1 and D_2 operate at half line cycle due to symmetrical configuration, whereas diode D_o conducts for the whole line cycle.

6.7.1 Line-cycle level voltage

It is obvious from Figure 6.17 that diode D_1 conducts during the positive half line cycle, while D_2 conducts during the negative half line cycle. The simulation result was verified by experimental result show in Figure 6.18.

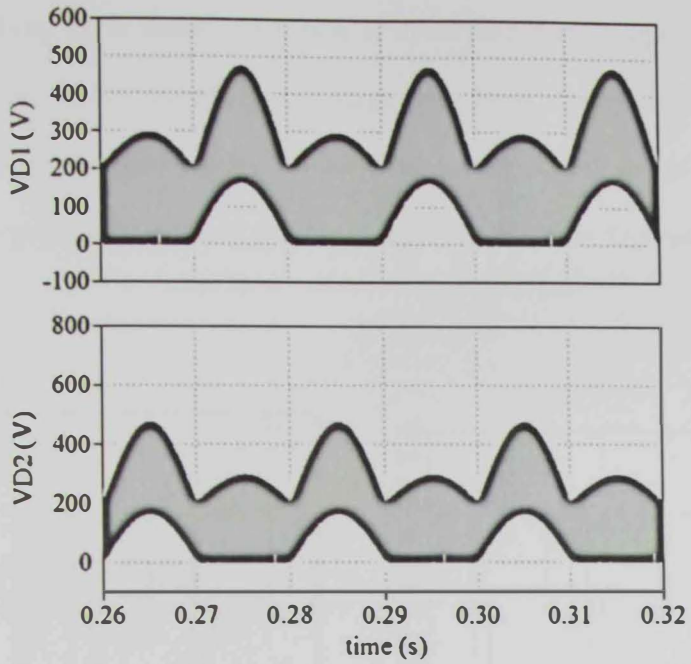

Figure 6.17: Simulation results: Diodes D_1 and D_2 line-cycle level voltage.

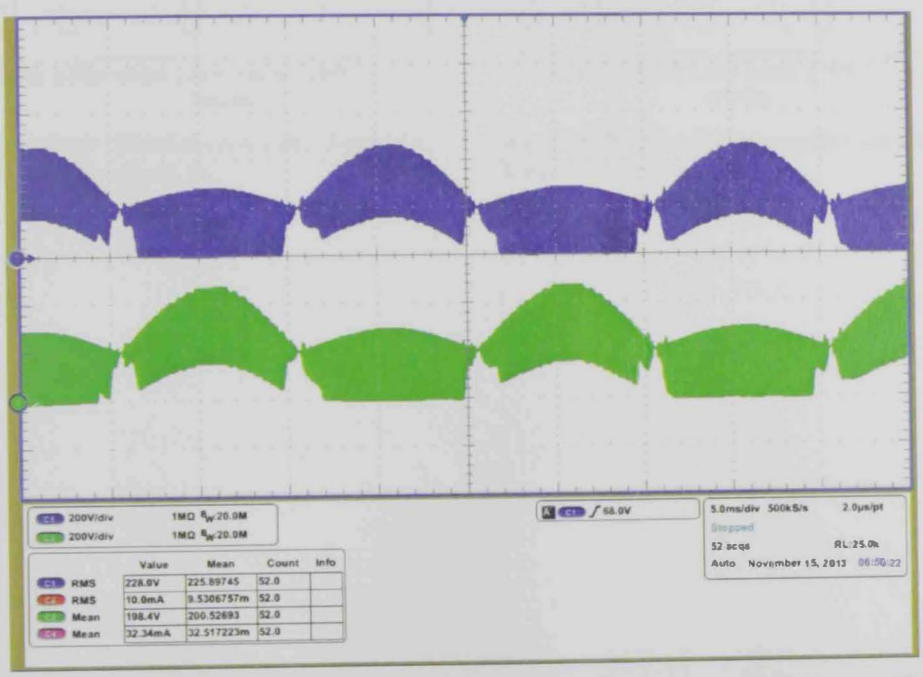

Figure 6.18: Experimental results: Diodes line-cycle level voltage (D_1 in blue and D_2 in green).

6.7.2 Switching level voltage

During switching level, diodes operation is dived into three stages. When the switch Q_1 is on the diodes are off during stage one. Then, diodes conduct at the second stage resulting in zero voltage. Finally, diodes turned off at the last stage. Simulation and experimental result of the three stages are shown in Figures 6.19, 6.20 and 6.21.

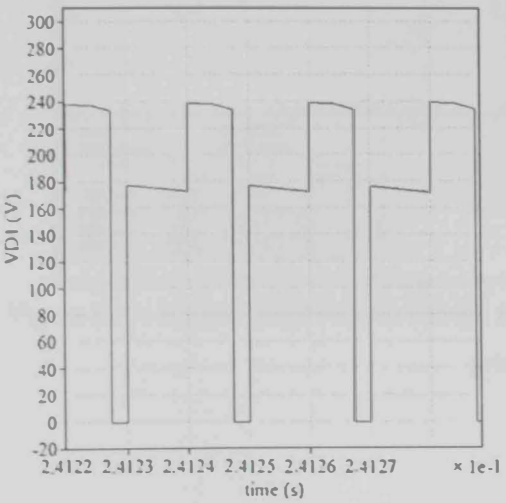

Figure 6.19: Simulation results: Switching level voltage diode D_1.

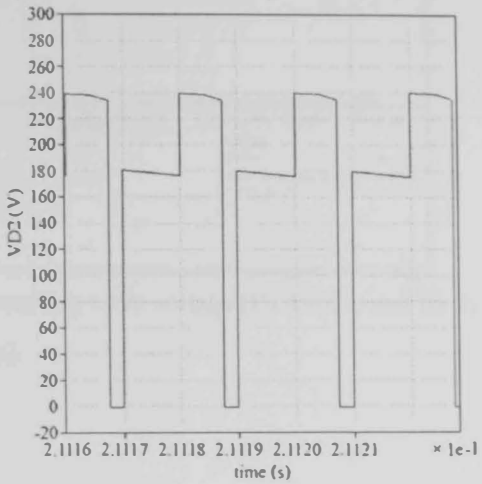

Figure 6.20: Simulation results: Switching level voltage diode Do.

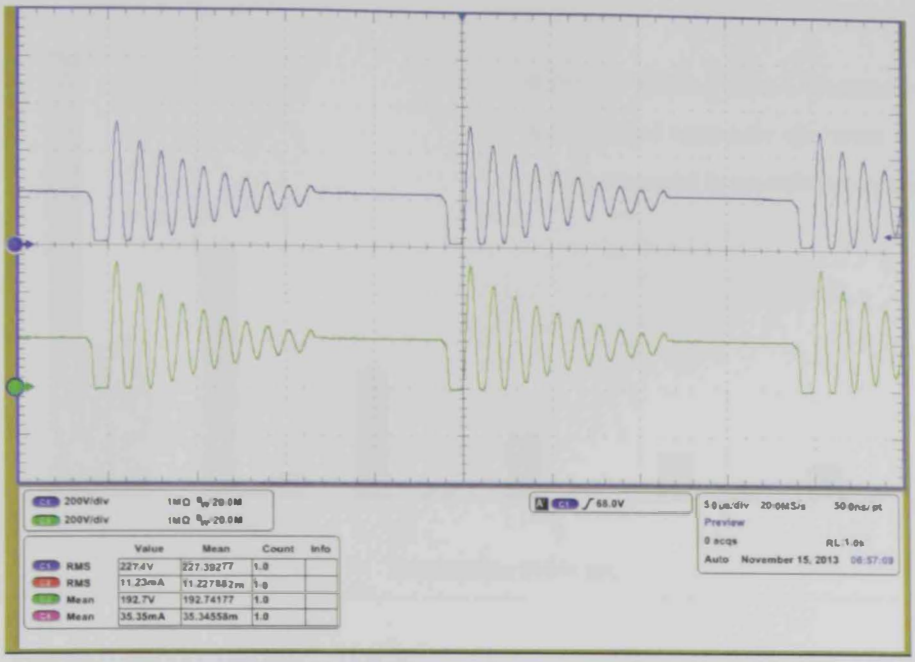

Figure 6.21: Experimental results: Diodes switching level voltage (D_1 in blue and D_2 in green).

Finally, simulated and experimental harmonic spectrum for the input line current is also presented in Figure 6.22 and compared with IEC 61000-3-2 Class D standard. The Fourier components of the input current at odd harmonic order were plotted and compared with IEC standards as shown in Figure 6.22. Clearly, the proposed circuit reduced the harmonics well below the IEC standards.

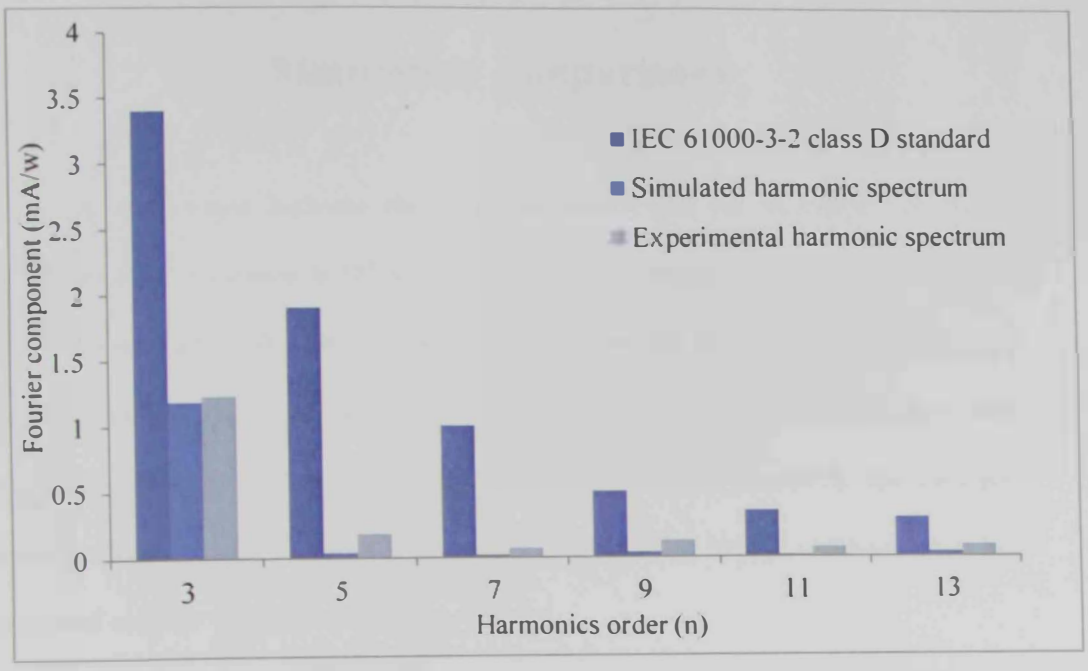

Figure 6.22: Simulated and experimental harmonic spectrum for input line current of the proposed circuit compared to IEC 61000-3-2 class D standard.

CHAPTER 7

Simulation comparisons

A comparison between the proposed circuit and the modified full bridge SEPIC rectifier presented in [8] have been done at different output power levels (50 watt, 100 watt and 200 watt) to study the improvements of the proposed circuit. At each power level a range of input voltage was used to compare efficiency, total harmonic distortion and power factor. Both circuits were drawn in the previous sections. In section 2, Figure 2.3 illustrates modified full bridge rectifier, while the proposed rectifier was shown in Figure 3.1.

Each circuit was designed at the same operating point used in designing the proposed circuit which is:

- $V_{in}=170 \sin(\omega t)$ where line frequency is ($f_l=50$ Hz)
- $P_o=200$ watt
- $V_o=400$ V
- $f_s=50$ kHz

The modified SEPIC was designed properly to ensure working at discontinuous current mode. So, at each power level, the equivalent inductor L_e was calculated for operation in DCM, as given in subsection 3.7.

Where L_e for each circuit is:

Proposed circuit: $1/L_e = (1/L_1) + (1/L_2) + (1/L_o)$ (7.1)

Modified SEPIC: $1/L_e = (1/L_1) + (1/L_2)$ (7.2)

Both circuits (the proposed rectifier and modified SEPIC) were designed properly and ensured operation under DCM. Then, using the selected components several simulations were done for each circuit using ORCAD PSPICE under a range of input voltage (100, 120, 140, 160, 180 and 200) volts at different power level (50, 100 and 200) watts. The THD, PF and efficiency were calculated for each circuit then the results were plotted to show the improvement that the proposed rectifier had.

7.1 Total current harmonic distortion as a function of the input voltage variation.

The THD variation as a function of the input voltage of both circuits was calculated at a three power level. For each input voltage level, the THD% was gotten from the simulation result for each circuit and then plotted using Microsoft Excel as shown in Figures 7.1, 7.2 and 7.3.

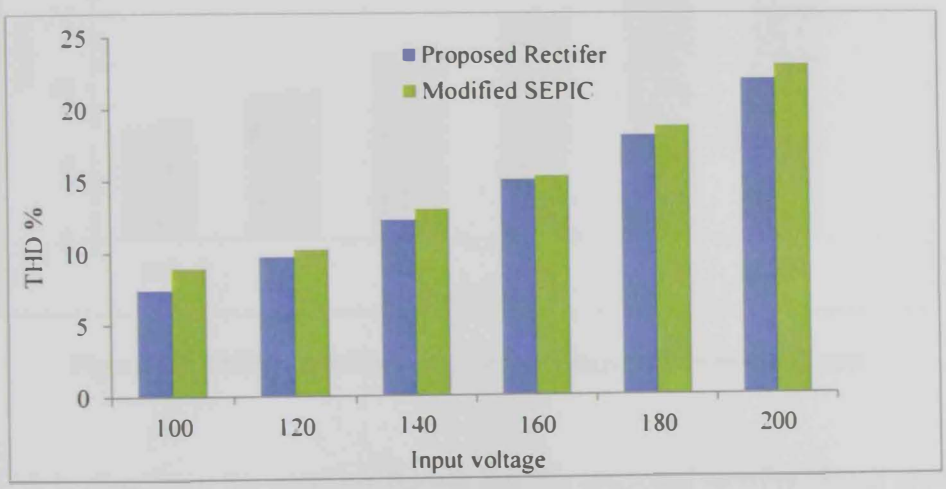

Figure 7.1: THD% as a function of input voltage at Power = 50 watt

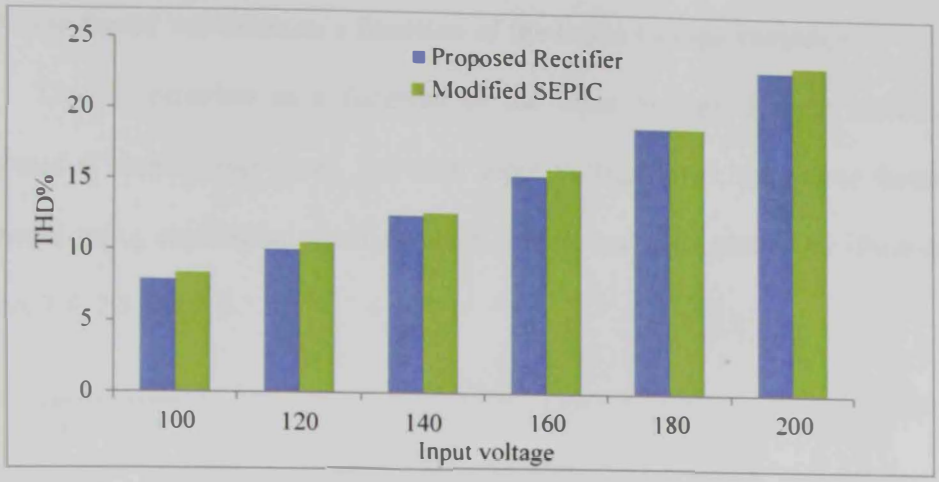

Figure 7.2: THD% as a function of input voltage at Power = 100 watt

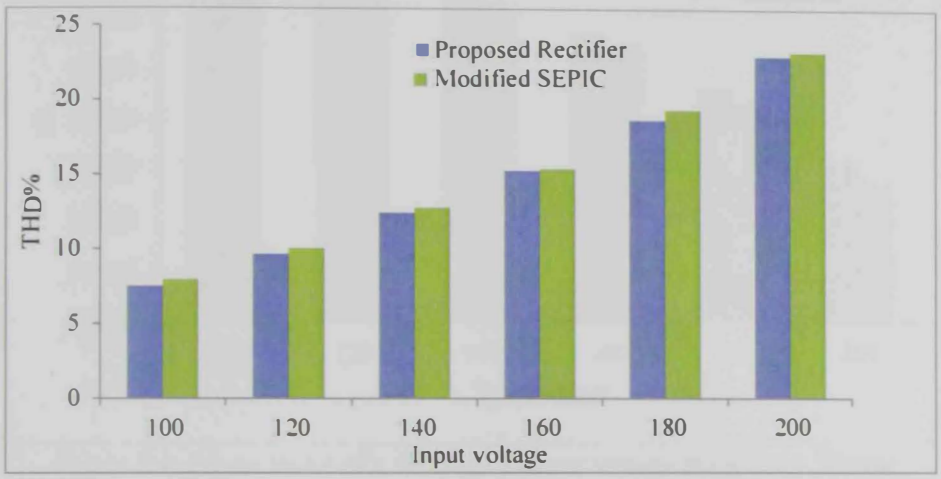

Figure 7.3: THD% as a function of input voltage at Power = 200 watt.

It is clear from the previous figures that the proposed rectifier circuit produces the least amount of THD and this is mainly due to bridgeless configuration of the proposed circuit. Furthermore, the circuit was designed to operate in DCM in which the current naturally follows the input voltage, so the input current is almost sinusoidal.

7.2 Power-factor variation as a function of the input voltage variation

The PF variation as a function of the input voltage of both circuits was calculated at three power level. For each input voltage level, the power factor was calculated using simulation result for each circuit and then plotted as illustrated in Figures 7.4, 7.5 and 7.6.

$$PF = \frac{1}{\sqrt{1+(THD)^2}} \tag{7.3}$$

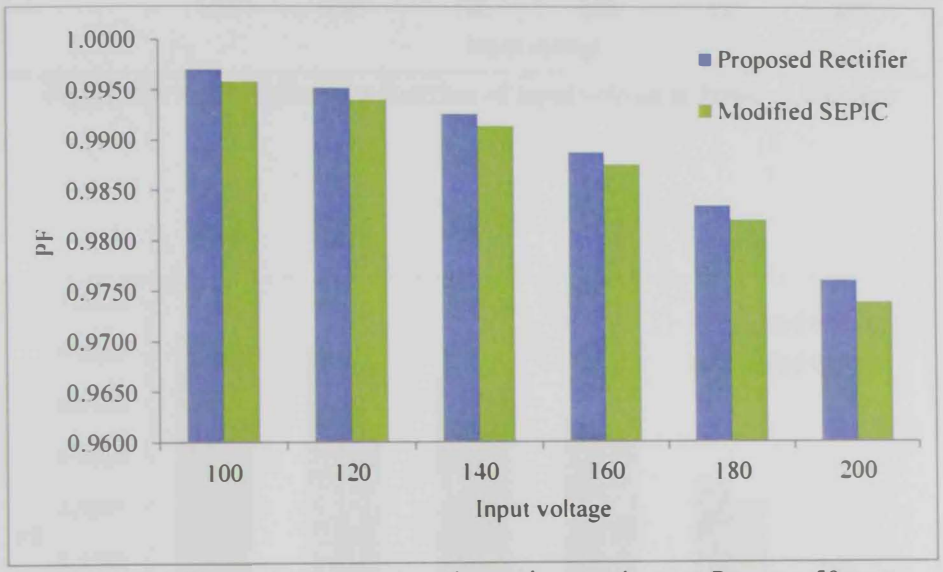

Figure 7.4: Power factor as a function of input voltage at Power = 50 watt

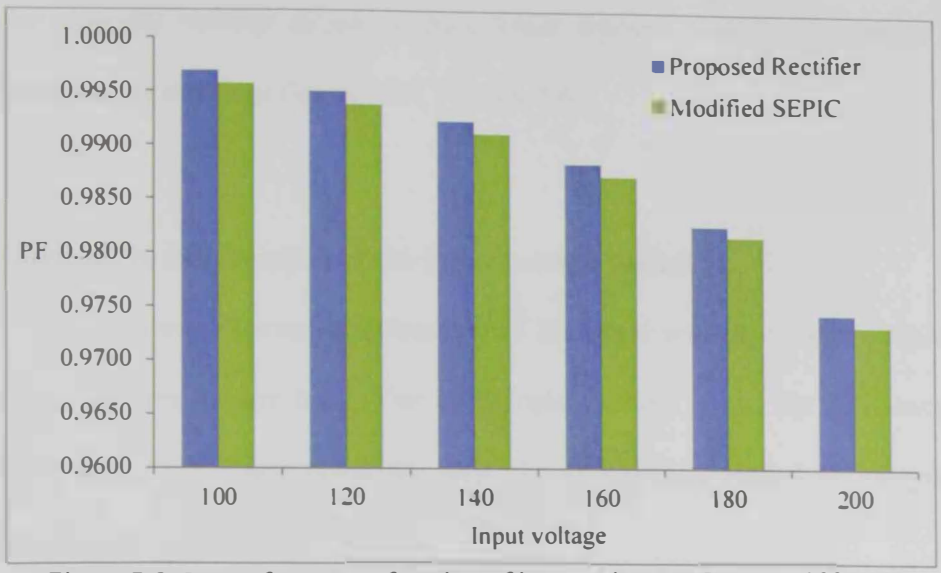

Figure 7.5: Power factor as a function of input voltage at Power = 100 watt

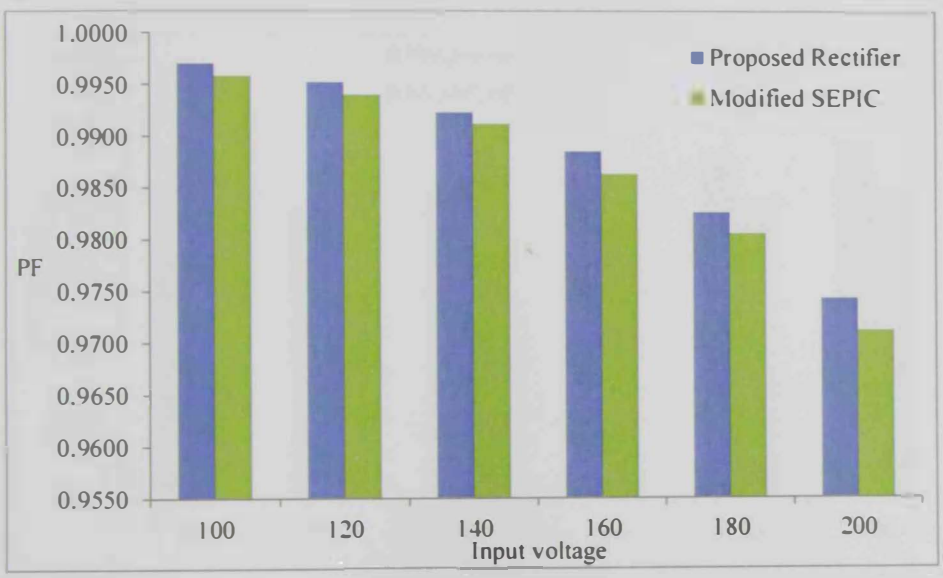

Figure 7.6: Power factor as a function of input voltage at Power = 200 watt

Since the power factor is inversely proportional with THD from equation (7.2) and the proposed rectifier circuit produce lower amount of THD, the power factor will be higher as shown in Figures 7.4, 7.5 and 7.6.

7.3 Efficiency% as a function of the input voltage variation:

The efficiency curves as a function of the input voltage of both circuits was calculated at three power level. For each input voltage level, the efficiency was calculated using simulation result for each circuit and then plotted as illustrated in Figures 7.7, 7.8 and 7.9.

$$\text{Efficiency} = \frac{P_{out}}{P_{in}} \tag{7.5}$$

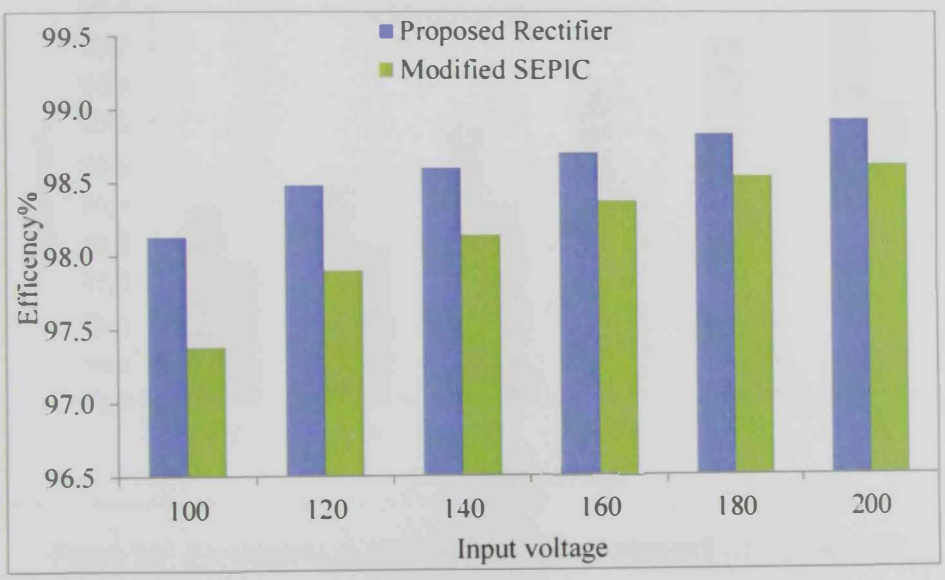

Figure 7.7: Efficiency% as a function of input voltage at Power = 50 watt

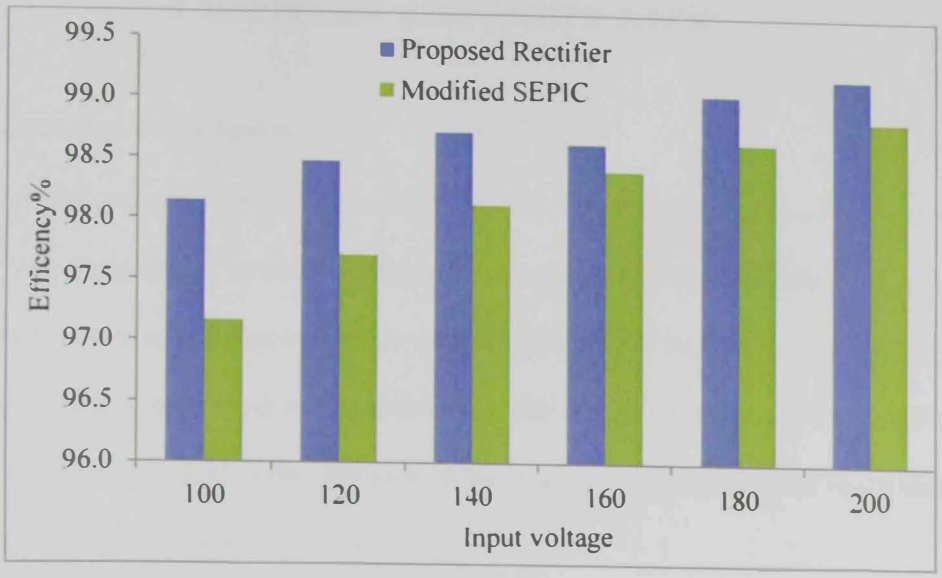

Figure 7.8: Efficiency% as a function of input voltage at Power = 100 watt

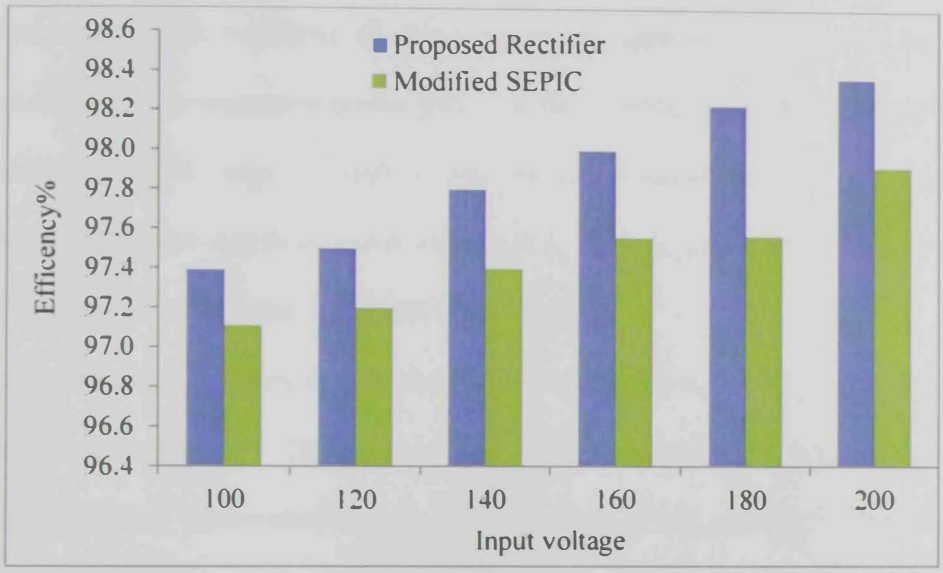

Figure 7.9: Efficiency% as a function of input voltage at Power = 200 watt

By observing the Figures 7.7, 7.8 and 7.9, it is obvious that the efficiency has been improved for the proposed rectifier compared with the bridge circuit.

CHAPTER 8

Conclusion and future work

8.1 Summary and conclusion

A new topology based on modified SEPIC was presented in this thesis. The circuit was designed to operate in discontinuous inductor current mode due to its advantages, such as unity power factor and simple control. Furthermore, the circuit configuration is symmetrical which means that the circuit operation in the positive half line cycle is identical to the operation in the negative half line cycle as mentioned in chapter 3 which simplifies the analysis.

The power factor was proven in chapter 3 that it is almost unity since the input current follows input voltage profile and the switch network behaves like an equivalent resistor with resistance R_e. Also, the switch network was modeled by a loss-free resistor and a dependent power source as shown in Figure 3.13. In chapter 4, the circuit components were designed properly to ensure operation in DCM. After that a lag compensator was designed in chapter 5 to regulate the output voltage and reduce the effect of input voltage and load disturbances.

A comparison between simulation results done by PLECS and experimental results was done in chapter 6. The comparison showed that both results are almost the same. In addition, a comparison between the proposed circuit and IEC 61000-3-2 standard was done to show the reduction in total harmonics distortion. Finally, the proposed circuit was compared with the full bridge modified SEPIC considering three power level and a range of input voltage at each power level. Both circuits were

compared according to the total harmonics distortion, power factor and efficiency. In chapter 7, it was showed that the proposed circuit had a higher power factor and efficiency and a lower total harmonics distortion.

8.2 Future work

Stress analysis of the converter components and switches is also required. Experimental results of the closed loop system with the derived controller are needed. Comparison between the simulated and the experimental results to evaluate the designed controller would improve the presented work. Finally, design several controllers with different control methodologies such as sliding mode control, fuzzy logic and optimal control.

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الخلاصة

اكتسب تصحيح معامل القدرة اهتماما كبيرا في السنوات الاخيرة نتيجة الطلب المتزايد على الطاقة من خطوط الكهرباء الموفرة من قبل شركات الكهرباء و نتيجة لصرامة الشروط الموضوعة من قبل المنظمات العالمية مثل (اللجنة الكهروتقنية الدولية) للحصول على جودة عالية. جميع التصاميم الأولية للمحولات الكهربائية مثل (البوست، الباك، الباك-بوست و الاشكال الاخرى المعدلة منها) قد تستخدم كمحول نشط ذو معامل قدره مصحح.

في هذا البحث، سيتم مناقشة محول لا مقنطر جديد يعمل بمعامل قدرة عالي و كفاءة عالية، الذي قد يستخدم في تطبيقات ال اي دي و شحن البطاريات. المحول الجديد مناسب للعمل على نطاق واسع من الجهد الكهربائي وهو مصمم اعتمادا على نسخة سبيك معدلة. بالاضافة الى ذلك، فإنه تم تصميم المحول ليعمل بطريقة توصيل التيار المتقطع. التصميم الجديد للمحول يؤدي الى تقليل الخسارة في الطاقة الناتجة من اشباه الموصلات (الدايود) في المحولات المقنطرة. كما ان نطاق الجهد للمحول الجديد اوسع من نطاق الجهد في محول سبيك المقنطر والكفاءة ايضا اعلى والتلوث في خطوط نقل الطاقة (الهارمونيك) اقل.

سيتم تصميم متحكم يقوم بالحفاظ على جهد الحمل الخارجي في حالة مستقرة و تقليل تأثير المؤثرات الخارجية الناجمة عن تغير في جهد المصدر او تغير في مقدار الحمل الخارجي. المتحكم سيصمم عن طريق تقنية سيكا المستخدمة لبناء النموذج الرياضي للمحول المقترح ومن خلال هذ النموذج سيتم تصميم المتحكم.

واخيرا، سيتم عرض نتائج محاكاة للمحول المقترح باستخدام ثلاث برامج (ماتلاب، اوركاد و بليكس). كما انه سيتم بناء نموذج للمحول في المختبر ذو قدرة 200 وات لتتم مقارنتهه مع نتائج المحاكاة.

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