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Advancements Towards Single Site Information Storage and Processing Using HfO2 Resistive Random Access Memory (ReRAM)

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Advancements towards single site information storage and processing using HfO_2 Resistive Random Access Memory (ReRAM)

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Abstract

Resistive Random Access Memory (ReRAM) has attracted much attention among researchers due to its fast switching speeds, lower switching voltages, and feasible integration into industry compatible CMOS processing. These characteristics make ReRAM a viable candidate for next-generation Non-Volatile Memory. Transition-Metal-Oxides have been proven to be excellent materials for ReRAM applications.

This work investigates the effect of various, post-deposition anneals (PDA) on the switching parameters of Ni/Cu/HfO_2/TiN Resistive Memory Devices (RMD). Results are presented in the form of a Small Business Innovation Research (SBIR) grant proposal. The use of the SBIR format emphasizes understanding of the experimental design, commercial viability, and broader impacts of ReRAM technology.

Acknowledgements

I would like to thank Dr. Nathaniel Cady for allowing me the opportunity to conduct research with his lab over the previous two years. Working in the Cady lab has proven to be enriching, enlightening, and enjoyable. I wish to express thanks towards Benjamin Briggs for an enormous amount of help and guidance. I will forever wonder “What would Ben do?” Jihan Capulong was particularly helpful in analyzing the data relevant to the project.

No one has put up with my antics more than my two roommates Ian Lepkowsky and Adam Abdelaziz. Thank you for distracting me during those times I wasn’t writing this thesis. You have kept me sane.

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II. Project Summary

Technical Abstract

The driving force behind the semiconductor industry is twofold:

(1) Develop new material systems which exhibit novel or superior properties which can be exploited in various applications and devices.

(2) Decrease the size of constituent devices in order to make them more powerful and accessible to society.

The industry is currently facing barriers which will stall the scaling of memory and storage. In order to overcome these barriers, new materials and methods must be considered. Modern computers allocate separate space for information storage and information processing, the hard-drive and RAM respectively. Computer quality is directly related to the performance of these elements.

Resistive Random Access Memory, or ReRAM, shows superior switching speeds, requires less power, exhibits high endurance, and is compatible with current CMOS manufacturing processes. This proposal describes a method for the fabrication of ReRAM cells for use within single-site information storage and processing elements. By taking advantage of indefinite retention times, ReRAM can be used to store information. A read mechanism which does not alter the logic state of the ReRAM cell allows for information processing. The Phase I research program details the fabrication of hafnium oxide based ReRAM which will enable Single-Site Storage and Processing (S3P) technology.

Anticipated Results/Potential Commercial Applications

The scaling of both memory and storage elements has facilitated advances within aerospace, medicine, defense, and consumer electronics for several decades. These advances can be attributed to augmented processing power and product mobility as well as decreased power consumption. Companies are currently redirecting research efforts toward ReRAM for next generation Non-Volatile Memory (NVM) due to superior switching speed, lower power requirements, indefinite retention, and CMOS processing compatibility. The technology described in this proposal exploits these same characteristics in order to achieve Single-Site Storage and Processing (S3P). S3P technology as enabled by ReRAM will result in a drastic increase in electronic performance. Consolidation of the hard-drive and RAM eliminates the need for load times (programs will be executed at the site of storage), removes parasitic power losses associated with transferring information between the two elements, and decreases the amount of packaging required to house a chip. This translates as high speed, low power, and high mobility. S3P technology will be geared towards highly mobile and performance dependent tasks, such as those present in on-site medical treatment, military expeditions, and remote information processing. Applications will also be found in consumer electronics, particularly those centered on gaming and telecommunications. The proposed research program will focus on component development. The final product of Phase I will be a Process of Record (POR) which will be incorporated into the design of the S3P proof-of-concept to be developed in Phase II.

IV. Project Description

Identification and Significance of Opportunity

Semiconductor technology is ubiquitous in society. Every person and professional is in continual contact with both computers and mobile devices. Several sectors including telecommunications, government, military, finance, and aerospace provide constant demand for high integrity, high performance, and low power electronics. This demand drives research designed to produce both superior performing electronics and new ways of storing and processing information.

The two major forms of memory currently relevant are Flash and DRAM technologies. Flash is a portable solid state form of memory, capable of over 10,000 writes. Currently available Flash memory elements work through the manipulation of only several electrons. However, such a storage mechanism is susceptible to thermal scattering and charge loss. Further scaling of Flash technology is decreasingly feasible. DRAM offers extremely fast speeds, but is nearly 20 times as expensive as Flash. Thus, there is a need for a new form of memory which can combine the storage capability and non-volatility of Flash with the speed and performance of DRAM.

The goal of this research program is to produce ReRAM which operates at a competitive level with current projections by the International Technology Roadmap for Semiconductors (ITRS) [1]. Phase I research will focus on manipulating the grain structure of ReRAM active layers through precise heating and cooling treatments. Phase II research efforts will demonstrate simple architectures capable of S3P. Once the proof-of-concept is established, efforts with Phase III partners will focus on scaling the technology to a manufactureable level. ReRAM has already been established as a CMOS compatible technology and will therefore be viable on a High Volume Manufacturing (HVM) scale [4].

Background

Flash Memory

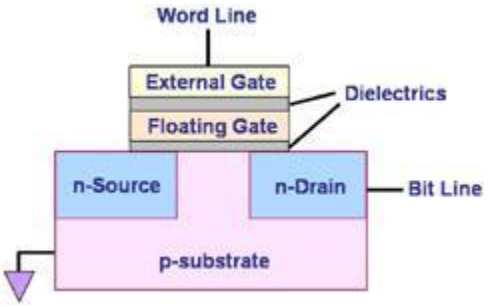

Figure 1: Flash memory cell [14]

Flash memory is a form of non-volatile Electronically Erasable Programmable Read Only Memory (EEPROM). Flash memory arrays consist of a grid of columns and rows, with two transistors at each intersection. A thin oxide layer separates the two transistors, known as the floating gate and control (external) gate (Fig 1). Flash memory cells work via the application of an electric field to the control gate. The field causes electrons to become trapped at the oxide-floating gate interface. A value of 0 or 1 is assigned to the memory cell based off of the shift in threshold voltage caused by the presence of electrons. However, current models of flash store a

limited number of electrons within the thin oxide layer. Because the system is sensitive to fluctuations in charge density, the loss of a single electron from thermal contributions can lead to loss of retention. Further scaling of Flash technology will only exacerbate losses.

Dynamic Random Access Memory (DRAM)

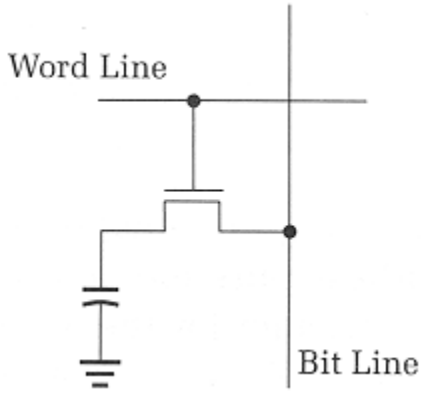

Figure 2: DRAM memory cell [15]

DRAM memory cells work by coupling a transistor with a capacitor (Fig 2). The capacitor stores charge, and is what is read when determining the logic state of a cell. The transistor acts as a control for storing charge within the capacitor. However, DRAM cells must be refreshed frequently as the charge continuously leaks from the capacitor. This refresh function is constantly occurring and impedes the performance of DRAM. While capable of fast switching speeds, DRAM is volatile and expensive.

Resistive Random Access Memory (ReRAM)

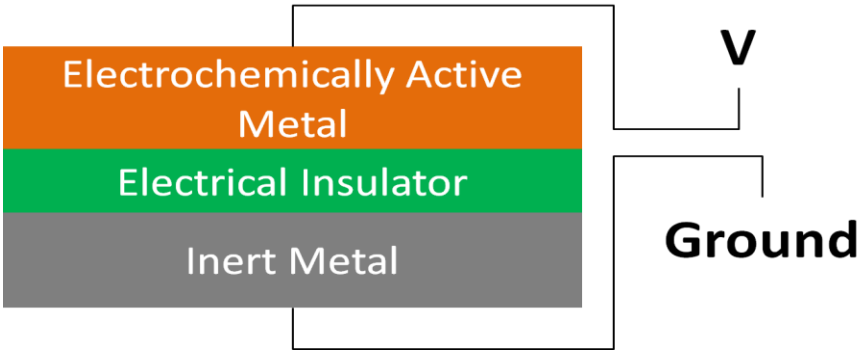

Figure 3: Metal-Insulator-Metal structure of a ReRAM cell. The top electrode is biased and the bottom electrode is grounded during electrical testing.

ReRAM memory cells are constructed as simple metal-insulator-metal structures, similar to that of a parallel plate capacitor (Fig 3). However, the function of a ReRAM cell is not to store charge, but to exhibit a specific magnitude of resistance. Applying a large electric field to the device will change the device's resistance state. The High Resistance State (HRS) correlates to a value of 0 while the Low Resistance State (LRS) corresponds to a value of 1. Current will pass through a device in the LRS while being blocked by a device in the HRS. The resistance state of a cell can be maintained indefinitely.

ReRAM has attracted much attention among researchers due to its fast switching speeds [2], lower switching voltages [3], and feasible integration into industry compatible CMOS processing [4]. Current challenges facing the development of manufactureable ReRAM elements include variability of devices and control over the switching mechanism. Nevertheless, recent progress has been made in both controlling device switching and limiting performance variability.

Rationale and Technical Approach

ReRAM likely switch via a combination of both vacancy and cation motion. Both oxygen vacancy and electrochemical migration are enhanced at grain boundaries, and therefore microstructure engineering offers a solution which addresses both switching mechanisms [5-9]. Phase I research is inspired by this principle. We hypothesize that employing a post-deposition anneal (PDA) on the HfO_2 active layer will result in improved switching. PDA allows us a mechanism for adjusting the microstructure, i.e. the grain boundaries and texture of the active layer.

Rapid Thermal Anneal (RTA) will be employed to limit diffusion of the bottom electrode into the active layer. RTA uses quartz lamps to achieve extremely sharp temperature spikes and gas transport to enhance sample cooling. The sharp influx of energy during RTA maintains any microstructure change.

Enhanced Motion along Grain Boundaries

The diffusion of a species within a solid can occur via lattice and grain boundary diffusion. It has been long established that diffusion through polycrystalline material is several orders of magnitude greater than in single crystal material. This is attributed to the presence of grain boundaries and was first addressed in a qualitative manor by Fisher in 1951 [10]. Grain boundary diffusion is dependent on the angle or misorientation between grains. Intuitively, grain boundaries can act as a highway for the diffusion of mobile species (FIG 4). Invoking this image, it should be possible to control atomic diffusion by modifying the grain boundaries. Preliminary work which suggests it is possible to control the diffusion process is discussed in Related Research. Analysis of grain size and texture of the HfO_2 film will play a critical role in determining microstructural differences arising from different annealing conditions.

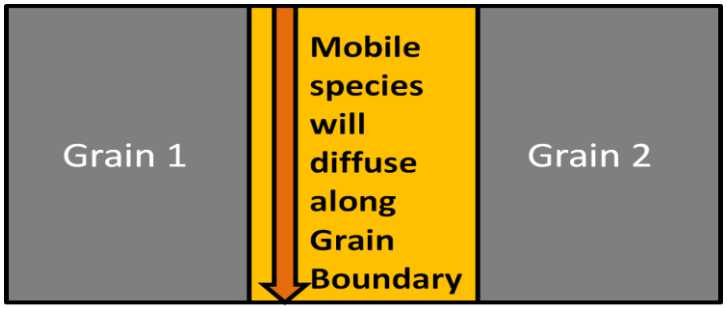

Figure 4: Schematic of a grain boundary. Grains 1 and 2 do not perfectly align. The space between (yellow) is called a grain boundary. Mobile species move through this yellow region at significantly higher rates than through the gray regions.

Anticipated Benefits

The Phase I research program aims to demonstrate competitive ReRAM performance with respect to the ITRS roadmap. Competitive performance translates into sub-10ns switching

speeds, low power switching (<1.3V), and data retention of 10 years. This will be accomplished through the engineering of grain boundaries within the HfO_2 layer of ReRAM cells. Grain boundary control offers a way in which we can enhance the electrochemical migration of copper during device switching. Enhanced switching properties can be employed in both Non-Volatile Memory (NVM) applications as well as S3P. ReRAM based NVM offers substantial improvements in switching speeds, data retention, and costs associated with power usage over currently available Flash or DRAM technologies. The development of competitive ReRAM will also enable S3P, resulting in a drastic increase in electronic performance. S3P eliminates the need for load times, removes parasitic power losses associated with transferring information between the hard-drive and RAM, and decreases the amount of packaging required. S3P technology developed by ReRAM Solutions will provide significant increases in processing capabilities for consumers. The primary goal of the SBIR research program is to generate intellectual property. Intellectual property will provide ReRAM Solutions with the opportunity to contract and license the technology to potential Phase III partners.

V. Phase I Research Plan

Introduction

The main objective of Phase I research is to demonstrate that competitive ReRAM may be fabricated through grain-boundary engineering. Phase I will advance the development of Single-Site Storage and Processing proof-of-concept. Phase I is divided into three major task areas. Figure 5(a) illustrates the flow and dependence of major task areas. Figure 5(b) is a Gantt chart which highlights technical milestones for Phase I.

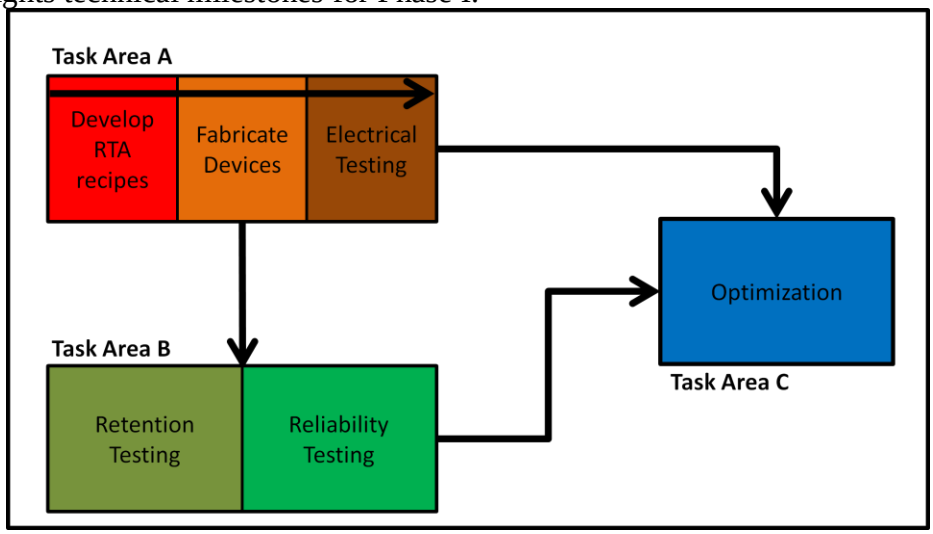

Figure 5 (a): Flow chart of Phase I research. Large blocks indicate task areas, while sub-sections of each block indicate task objectives. Arrows indicate the flow of objectives and their dependency on each other.

Technical Milestones		Year 1				Year 2			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1. Device Fabrication and Characterization									
	1.1 RTA Recipe								
	1.2 Device Fabrication								
	1.3 Current-Voltage Measurements								
2. Device Retention and Reliability									
	2.1 Retention Studies								
	2.2 Reliability Studies								
3. Device Optimization									
	3.1 Comparison to ITRS projections								

Figure 5 (b): Gantt chart illustrating technical milestones for Phase I research.

Task Area A: Device Fabrication and Characterization

Objective 1

The aim of this objective is to develop RTA tool recipes which will deposit different amounts of energy into amorphous HfO_2 films. A sound indicator of deposited energy is thermal budget; defined as the total amount of thermal energy transferred to a wafer during an elevated temperature process. Thermal budget is therefore proportional to the temperature and duration of a given process. Figure 6 illustrates a basic temperature profile which can be achieved on an RTA. Integrating the area under the temperature profile will give a relative measure for thermal budget between recipes.

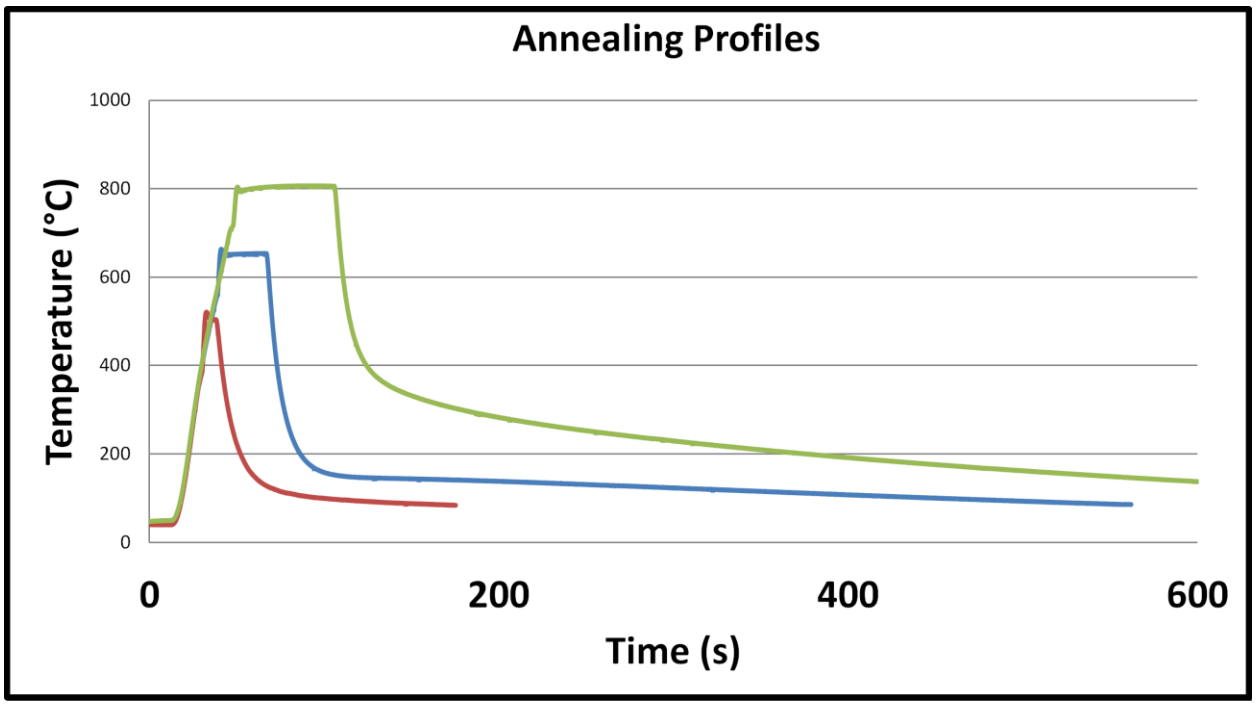

Figure 6: Basic temperature profiles which can be achieved using Rapid Thermal Anneal

The RTA has the ability to improve the stability of ramp rates based off of information from previous anneals. The system monitors both temperature overshoot and lamp power during ramping. The system can then use this information to decrease lamp power at the appropriate time and mitigate temperature overshoot on future anneals.

Objective 2

The aim of this objective is to execute anneals developed in objective 1. We currently contract HfO_2 deposition to Canon Anelva ™, and plan on maintaining this relationship for the duration of the Phase I and Phase II programs. Canon Anelva™ deposits films of amorphous and stoichiometric HfO_2, of variable thickness.

RTA treatments will be conducted within a Class 1000 cleanroom. X-Ray Diffraction will be used in order to determine both grain growth and texture of the annealed films. Following the annealing process, top electrodes will be deposited using electron beam evaporation. Only active metals will be considered as top electrode materials. All active electrodes will be capped by a thin layer of Nickel in order to prevent oxidation. Device cross-sections will be examined under a Scanning Electron Microscope (SEM) in order to dial in deposition rates. Before devices can undergo electrical testing, a portion of the wafer must be etched down in order to gain access to the bottom electrode. Secondary Ion Mass Spectrometry (SIMS) will be employed to sputter to the bottom electrode. SIMS has the added benefit of providing chemical information as a function of depth.

Objective 3

An Agilent B1500A Semiconductor Parameter Analyzer will be used to conduct electrical testing. Devices will be tested in both sweep and pulse mode. Related research indicates that the

proposed resistive memory devices will operate in a unipolar fashion. In unipolar switching, the transition from HRS to LRS, and vice versa, occurs under the same bias polarity. Switching metrics to be measured include V_{Form}, V_{On}, V_{Off}, R_{On}, R_{Off}, device endurance, and switching power.

Sweep mode measurements will be taken by biasing the top electrode to positive and the bottom electrode to ground. A forming step which correlates to the initial formation of the filament is typically required. During the forming step, a current compliance must be placed on the system in order to prevent the device from catastrophically failing. Once formed, devices will be in the LRS. Another bias is applied which will switch the device from LRS to HRS. During the subsequent transition into the LRS a current compliance is used. This cycling is repeated many times in order to characterize the device. Figure 7 highlights a typical unipolar switch.

The forming process complicates ReRAM fabrication, costing time, money, and tool space for the manufacturers. Related research conducted by ReRAM Solutions has shown that the forming process can be eliminated via RTA treatments of the HfO_2 layer. Thusly, ReRAM Solutions can both mitigate the cost of the forming process while simultaneously manipulating grain structure to achieve enhanced electrochemical migration.

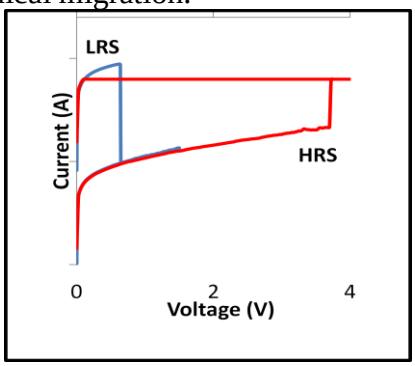

Figure 7: Unipolar switching. Applying a positive bias to a device in the Low Resistance State (LRS) causes a transition (blue) to the High Resistance State (HRS). An even larger positive bias will return the device from the HRS to the LRS (red).

Pulse mode measurements require that a transistor is placed in series with the ReRAM cell. The transistor functions analogously to the current compliance used in sweep mode measurements, but has more practical relevance to CMOS integration. Adjustments to pulse height and width will be made in order to characterize switching under pulse mode.

Task Area B: Device Retention and Reliability

Objective 1

Data retention is defined as the ability of a memory cell to maintain its data state over long periods of time, regardless of whether power is on or off. The International Technology Roadmap for Semiconductors (ITRS) projects 10 year retention for memory arrays. For ReRAM, this means an individual memory cell must be capable of maintaining either a LRS or HRS for 10 years. In order to measure logic retention, devices must undergo accelerated testing in which memory arrays are placed at elevated temperatures and stresses. Inducing failure mechanisms through extreme conditions allows for extrapolation of retention under room temperature

conditions. Retention tests will be conducted in-house with the aid of Dr. James Lloyd's accelerated testing laboratory.

Objective 2

Reliability measures the probability of correct functioning without failure until some time, t. In general, the probability of correct function approaches 0 over time [11]. Reliability studies are useful because they give a good picture of product lifetime. Having reliability data that shows correct functioning over an extended period of time helps validate a product in the competitive environment of the semiconductor industry.

Reliability lifetime follows an Arrhenius behavior. An energy barrier exists which must be overcome when transferring from correctly functioning state to a deteriorated state. This energy is the activation energy E_a .Thermal energy supplies the necessary push to overcome this energy barrier. Taking advantage of this Arrhenius behavior, it is possible to conduct accelerated testing at elevated temperatures. Furnaces outfitted for electrical testing will be used to conduct the tests. These tools are courtesy of Dr. James Lloyd.

Task Area C: Device Optimization

The objectives are concomitant. The final RTA treatment will be chosen based off of electrical testing, retention, and reliability. Direct comparisons will be made to the ITRS. The device build and anneal which shows the most commercial viability will be chosen. Task Area 3 is primarily concerned with the analysis of information obtained in Task Areas 1 and 2. Devices showing performance at a competitive level with ITRS projections will be incorporated into the proof-of-concept developed in Phase II.

However, if analysis indicates that devices will not perform at a competitive level with ITRS projections, there is a contingency plan. Poorly performing devices will undergo a complete metrological analysis including high resolution imaging (SEM and TEM) and chemically sensitive depth profiles (SIMS and XPS). Metrological analysis will help visualize and isolate issues within the fabrication process which lead to device failure.

Significance to future research and commercial applications

Phase I focuses on component development. The process of record for ReRAM fabrication produced during Phase I will be used during Phase II. Phase II is motivated by the construction of a proof-of-concept memory array, with the potential for an early-entry device. Phase III partners will provide the necessary momentum to carry S3P proof-of-concept to high volume manufacturing.

VI. Related Research

Early experimental efforts have been made which support the ideas and concepts on which the proposed research is based. Previously we have shown that the on-state conducting mechanism varies between amorphous and crystalline HfO_x based ReRAM [12, 13]. More recently, we have shown that RTA can be effectively used to manipulate the microstructure of HfO_2 in such a way as to produce film of different textures.

Thin films may exhibit short range or long range order. Films which show short range order are known as amorphous while films which show long range order are dubbed crystalline. Between these two extremes lies a regime known as polycrystalline. Polycrystalline refers to the presence of multiple crystallites which make up the film. Because these crystallites exhibit different atomic orientations from each other, they do not align. It is due to this misalignment that grain boundaries arise.

It is well established that the addition of thermal energy will lead to phase transformation in thin films. During film transformation, certain crystallites may dominate the composition of the film. The dominance of one crystallite over other another is known as texture. The texture of a film will affect the orientation of grain boundaries and thus percolation pathways for diffusing species. XRD was performed on annealed samples (Table 1) in order to understand grain and texture evolution.

Temperature (°C)	Time (s)		
500	10	30	60
650	10	30	60
800	10	30	60

Table 1: RTA annealing parameters.

Grazing Incidence X-Ray Diffraction was performed on as-deposited and annealed samples. Cu-Kα radiation ($\lambda = 1.53$ nm) was used to expose the samples using a Bruker D8 Diffractometer. Figure 8 shows a normalized plot of intensity versus 2θ. The normalized intensity of a peak signifies a grain's dominance in the film. If one peak dominates the spectrum, this indicates the film is textured with this crystal orientation. The data presented justifies the basis behind our hypothesis. Using simple RTA processes, amorphous HfO_2 can be transformed into varying textures of monoclinic HfO_2.

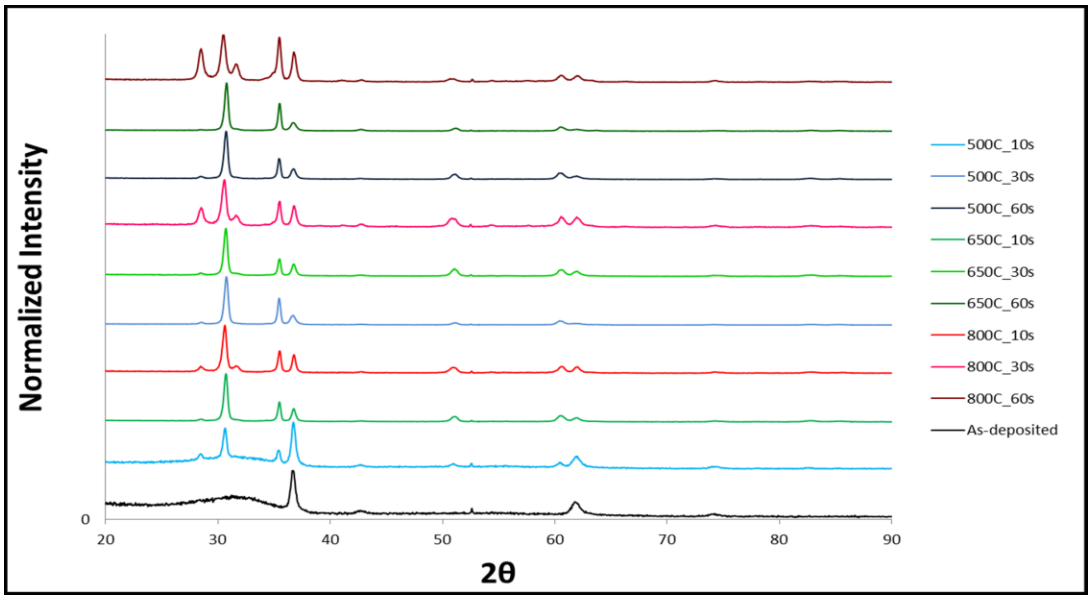

Figure 8: XRD patterns of the as-deposited and annealed films. The as-deposited (black) is consistent with amorphous HfO_2. The offset is organized such that the anneal with the highest thermal budget is on the top, lowest on the bottom.

Furthermore, ReRAM Solutions has conducted experiments which show the forming process may be eliminated by conducting anneals with high thermal budgets. This data is presented in Figure 9 below. The as-deposited sample shows forming voltages in excess of 15 volts. As the temperature and time of the annealing process increases, we see a decrease in the forming voltage until the initial switch occurs on the same order of magnitude as normal switching. This trend suggests that crystallization and the growth of grains lowers the energy barrier for the electrochemical migration of copper. It is this trend which ReRAM Solutions wishes to exploit.

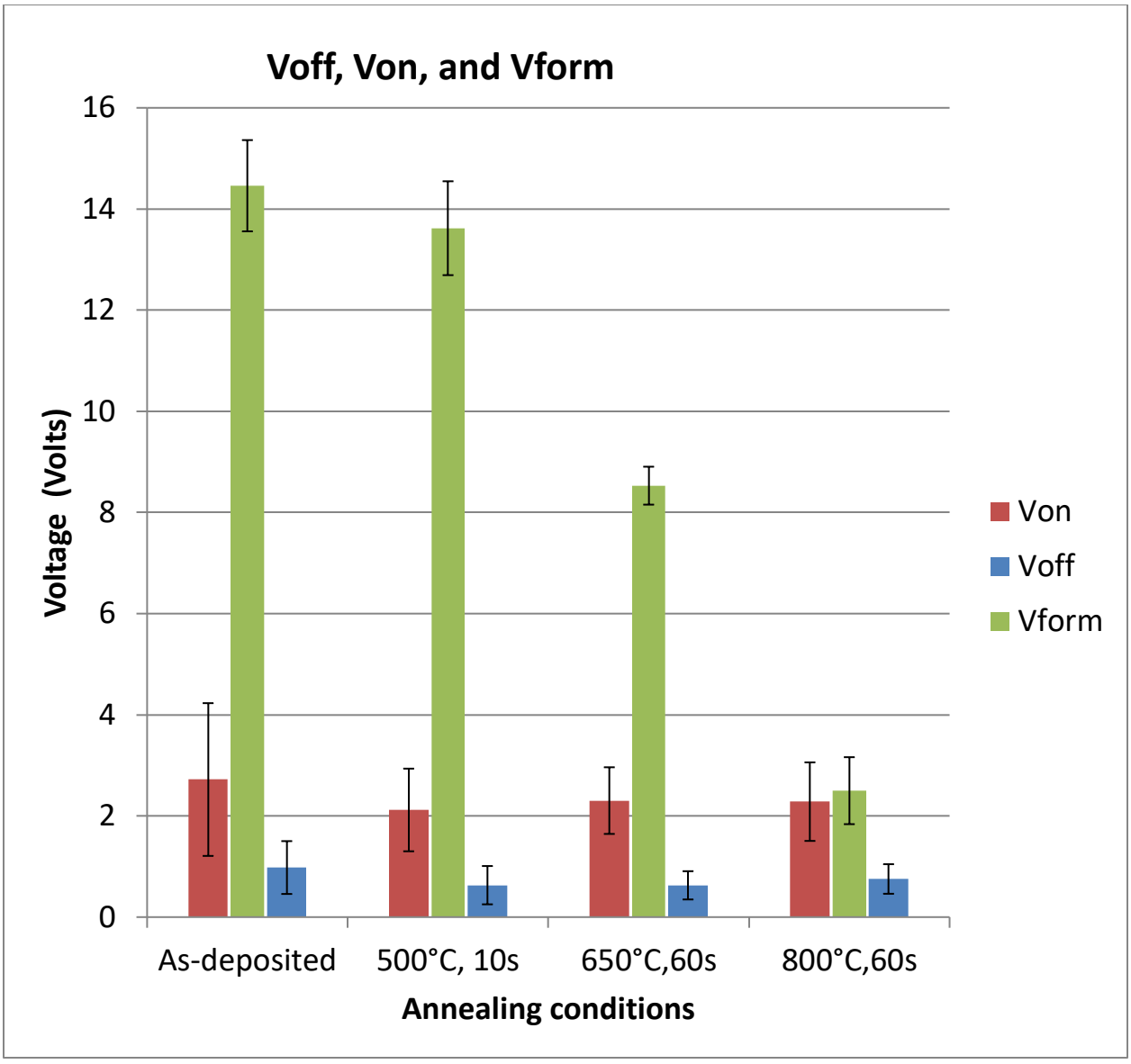

Figure 9: Forming process mitigation. Green curve represents Forming voltage, blue and red curves represent typical switching events.

VII. Commercialization and Budget Justification

Company Information

ReRAM Solutions is an early stage business which seeks to specialize in the fabrication of new electronic structures using Resistive Random Access Memory. Existing upstream from computer chip manufacturers, ReRAM Solutions' niche is to provide an alternative route to Moore's Law through ReRAM systems engineering. The company currently staffs a total of 4 employees, two of which are Ph.D. level with a third expected to join within the next few months. A strategic partner of and located at the College of Nanoscale Science and Engineering (CNSE), the company is able to leverage high quality research and development facilities which allow for in-house development of technology. The CNSE operates as a consortium, bringing together over 250 corporations involved in semiconductor manufacturing. Under the consortia model, competing companies establish working relationships to lower the overall costs of manufacturing. As aforementioned, semiconductor research and manufacturing is extremely expensive, and therefore it is advantageous for firms to work together to lower costs. This is achieved by pooling money and sharing research equipment. Over $14 billion has been invested in CNSEs facilities, creating a world class research environment. The environment fosters a sense of collaboration between competitors. Such readiness to work with competitors will prove advantageous during ReRAM Solutions' search for Phase III investors.

As a strategic partner of the CNSE, we have access to exclusive avenues of commercialization. Invention disclosures will be processed by CNSE's Office for Technology Innovation and Commercialization. The CNSE retains full rights to any proprietary materials, processes, etc. When appropriate, a licensing agreement with the CNSE will be reached which will transfer intellectual property over to ReRAM Solutions. Intellectual property will be leveraged to reach contractual and licensure agreements with companies within the memory market.

Market Opportunity

Ultimately S3P technology aims to disrupt current forms of Non-Volatile Memory (NVM) and thus is a good indicator of future markets. The market size for NVM is assessed in Figure 9. Currently, market consumption can be broken down into several categories, including cache memory storage, industrial and transportation uses, mass storage, mobile phones, and smart cards. By the end of 2013, it is estimated that the NVM market will have reached nearly $400 million. Our commercialization strategy, outlined in Figure 10, estimates ReRAM Solutions will enter the market in late 2016. At the point of entry, the market will be valued at $1 billion. Although other forms of memory will continue to exist, it is anticipated that ReRAM will head the market once S3P technology is adopted by major manufacturers. Other markets that will be targeted by S3P technology include the medical and defense industries. In 2012, the U.S. medical devices market was estimated at $120 billion. Even conservatively estimating the market share at 1%, this represents $1 billion. In 2013, the Department of Defense is expected to invest $69 billion in R&D for new technologies. Again, conservative estimates indicate S3P technology could encapsulate millions of dollars in defense contracts.

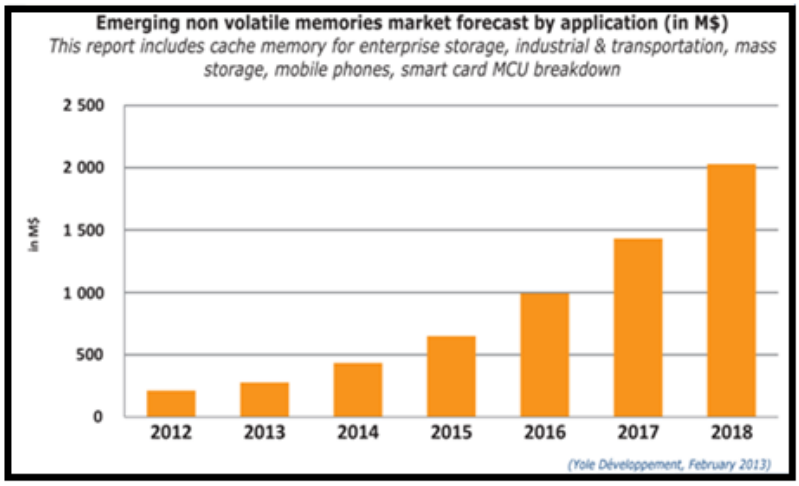

Figure 10: Market for Non-Volatile Memory through 2018. Graph indicates the market will grow in excess of $2 billion.

The nature of semiconductor research and manufacturing is extremely expensive. Deposition, lithography, metallization, and other processing tools can cost upwards of $1 million per tool. These large upfront costs create large barriers to entering the NVM market, only allowing for large corporations to maintain market space. In fact, the NVM market is largely controlled by only 5 players, namely Samsung, Micron, Sk Hynix, Toshiba and Sandisk. These companies represent yet another barrier to entry, i.e. competition. If ReRAM Solutions is to successfully and sustainably enter the market, alliances must be made with these competitors. Intellectual property which procures the market space encapsulated by S3P technology must be obtained and leveraged against the competition. ReRAM Solutions will use its membership as a strategic partner of the CNSE to gain access to Samsung, Micron, and Toshiba. The consortia model employed by the CNSE means all three of these companies are conducting R&D on-site, occupying the same space and using the same tools as ReRAM Solutions. Within the consortia model, competing companies develop licensing agreements which will allow members to share both intellectual property and the cost of tools. Under this atmosphere, ReRAM Solutions will be able to readily create an alliance within the NVM market, thus lowering the barriers to entry.

The technology described in this proposal will consolidate storage and memory elements employing ReRAM technology. S3P eliminates the need for load times, decreases parasitic power losses, and minimizes the amount of chip packaging required. These characteristics form the basis of proprietary claims. The end goal of this research program is to obtain intellectual property which may be licensed to companies such as Samsung, Micron, and Toshiba.

Commercialization Activities

Commercial Milestones		Year 2				Year 3				Year 4			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1. Demonstration of competitive ReRAM													
2. Proof-of-Concept													
3. Commercialization assistance through CNSE consortia													
	3.1 Scaling to HVM												
	3.2 Establishing either Supply chains or Licensing agreement												

Figure 11: Commercialization Milestones

Major commercialization milestones are outlined in Figure 11. Phase I research is geared towards component development, and is expected to be completed by the second quarter of year 2. Following the demonstration of competitively performing ReRAM, efforts to produce a S3P proof-of-concept will begin. It is expected that prototype development will take one year at most. Commercialization activities will largely take place during Phase II. ReRAM Solutions will fully capitalize on the consortia present at the CNSE during this period. Samsung, Micron, and Toshiba are targeted Phase III investors. Once an alliance is made, Phase III partners will catalyze the scaling S3P technology.

S3P is projected to be rapidly scaled to High Volume Manufacturing (HVM). ReRAM has been shown to be compatible with CMOS fabrication processes and is expected to hit the market as NVM in 2013. Processes involved in ReRAM fabrication include Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Photolithography, and Rapid Thermal Anneal. Metrological analysis is also found in-line, offering easy avenues for failure analysis. Both the fabrication and the metrological equipment listed above are readily found in an industrial scale cleanroom. S3P technology requires no change in the cleanroom infrastructure and therefore is economically viable for memory manufacturers. Due to impending integration into CMOS processing, there is no anticipated obstacles to manufacturing.

Intellectual property will provide the necessary revenue. During negotiations with Phase III investors, it will be imperative to establish a licensing agreement which provides a sustainable source of revenue for ReRAM Solutions. An agreement which provides royalties per unit sold is noted as the most profitable route. This is seen as advantageous over an agreement which involves a single, up-front transaction. ReRAM Solutions believes S3P to be a disruptive technology with a long future. Capitalizing over a long period of time is therefore advantageous, providing a constant supply of revenue.

Budget Justification

The table below outlines the budget for the Phase I research program. In total, we are requesting $150,000 from the SBIR program.

Sponsor: NSF SBIR	Title: Advancements towards single site information storage and execution using HfO2 Resistive Memory Devices (RERAM)
Project Investigator: Nathaniel Cady	Co- Project Investigator :

Period of Time: 1 YRS					
YEAR 1					
Salaries	**% Effort**	**Annual Salary**	**Total Cost**	**Requested Funding**	**Cost Share**
Faculty					
Nathaniel Cady	20%	$105,000	$20,900	$20,900	$0
			$0	$0	$0
			$0	$0	$0
Total State Paid employees			**$20,900**	**$20,900**	**$0**
RF Paid Employess					
Michael Hovish	50%	$15,000.00	$7,500	$7,500	$0
			$0	$0	$0
Total RF Paid Employees			**$7,500**	**$7,500**	**$0**
Graduate Students	**FTE**				
Benjamin Briggs	**50%**	**$21,840.00**	$10,920.00	$10,920	$0
Name: TBD			$0.00	$0	$0
Total Graduate Students	50%		**$10,920**	**$10,920**	**$0**
Summer					
N/A			$0	$0	$0
N/A			$0	$0	$0
Total Summer Salaries	0%		**$0**	**$0**	**$0**
Total Salaries			$39,320	$39,320	$0
Fringe Benefits	**Rate %**	**$ Base**			
State Employees	50.81%	$20,900	$10,619	$10,619	$0
RF Employees *	45.00%	$7,500	$3,375	$3,375	$0
Graduate Students *	16.00%	$10,920	$1,747	$1,747	$0
Summer	17.00%	$0	$0	$0	$0
Total Fringe Benefits			**$15,742**	**$15,742**	**$0**
Total Salaries and Fringe Benefits			**$55,062**	**$55,062**	**$0**
Other Direct Costs - Attach Details for any item listed below					
Equipment: Cleanroom access RPI (Cu depositions)			$20,000	$20,000	$0
*Tuition			$27,800	$27,800	$0
Travel			$2,000	$2,000	$0
Materials & Supplies: Shadow Mask set, Metal Targets			$5,300	$5,300	$0
Publications			$4,000	$4,000	$0
				$0	$0
				$0	$0
Total Other Direct Costs			**$59,100**	**$59,100**	**$0**

TOTAL DIRECT COSTS			**$114,162**	**$114,162**	**$0**
Facilities and Administrative Expense	Rate %	Base MTDC			
Does not incl:equip, install,tuit	53.00%	$66,362	**$35,172**	**$35,172**	**$0.00**
Total Estimated Project Cost			**$149,334**	**$149,334**	**$0**

A. Personnel

Dr. Nathaniel Cady will spend 20% of his time on ReRAM Solutions. This corresponds to a total of 2.4 person-months for a total of $21,000.00

Michael Hovish will spend 50% of his time on ReRAM Solutions. This corresponds to a total of 6 person months for a total of $7,500.00

Benjamin Briggs will spend 50% of his time on ReRAM Solutions. This corresponds to a total of 6 person months for a total of $10,920.00

B. Fringe benefits

Fringe benefits total $15,742.00, or $5247.33 per person. This accounts for dental, vision, and medical benefits.

C. Equipment

A new shadow mask set is needed to deposit electrode material during device fabrication. Metal targets are also required for the fabrication of devices.

The shadow mask set is estimated at $300.00
Metal targets average $300/target. In order to fabricate a large number of devices, several targets must be purchased per material for a total of $5000.00

D. Travel and Publications

Travel money is estimated at $666.66 per person for three of the four employees during year 1. This creates a total travel cost of $2000.00

Publications range from $1500.00 in smaller journals to upwards of $5000.00 in a journal like Nature. There is no expectation that work done would contribute towards a highly visible journal. Thus publication costs are estimated at $4000.00 which would give us the ability to submit two lower profile papers.

VIII. Key Personnel and Bibliography

It is anticipated that Dr. Nathaniel Cady will serve as principle investigator for the proposed program, with key contributions for Phase II research made by Dr. Dhireesha Kudithipudi. Abbreviated resumes for contributing members follow.

Dr. Nathniel Cady

Education:

- Post Doctoral Associate, Microbiology, Cornell University, Ithaca, NY, 2006
- Ph.D., Microbiology, Cornell University, Ithaca, NY, 2005
- B.A., Biology, Cornell University, Ithaca, NY, 1999

Employment:

- Associate Professor of Nanobioscience, College of Nanoscale Science and Engineering SUNY Albany
- Co-Founder of Illuminaria, LLC

Relevant Publications:

- N.R. McDonald, S.M. Bishop, B.D. Briggs, J.E. Van Nostrand, **N.C. Cady**. Influence of the plasma oxidation power on the switching properties of Al/CuxO/Cu memristive devices. (2012) *Solid-State Electronics. Online publication: http://dx.doi.org/10.1016/j.sse.2012.06.007*
- S.M. Bishop, B.D. Briggs, P.Z. Rice, J.O. Capulong, H. Bakhru, **N.C. Cady**. Ion implantation synthesis and conduction of tantalum oxide resistive memory layers. (2012) *Journal of Vacuum Science & Technology B.* 31(1): 012203.
- P.Z. Rice, B.D. Briggs, S.M. Bishop, **N.C. Cady**. Development of a silicon oxide based resistive memory device using a spin-on hydrogen silsesquioxane precursor. (2012) *Journal of Materials Research. Online Publication - DOI: 10.1557/jmr.2012.390*S.M. Bishop, H. Bakhru, J.O. Capulong, **N.C. Cady**. Influence of the SET current on the resistive switching properties of tantalum oxide created by oxygen implantation. (2012) *Applied Physics Letters. 100, 142111.*

Dr. Dhireesha Kudithipudi

Education:

- Ph.D., Electrical & Computer Engineering University of Texas, San Antonio (2006)
- M.S., Computer Engineering Wright State University, Ohio
- B.S., Electrical & Electronics Engineering Nagarjuna University, India

Employment:

- Assistant Professor, Department of Computer Engineering, Rochester Institute of Technology

Relevant Publications:

- C. Merkel, D. Kudithipudi, "A Temperature Sensing RRAM Architecture for 3D-ICs", IEEE Transactions on VLSI, 2013 (to appear).
- M.Soltiz, D.Kudithipudi, C.Merkel, G. Rose, and R.Pino, "Memristor-based Neural Logic Blocks for Non-linearly Separable Functions", IEEE Transactions on Computers, 2013 (to appear)
- C. Merkel, D. Kudithipudi, "Towards Thermal Profiling in CMOS/Memristor Hybrid RRAM Architectures," *International Conference on VLSI Design* (VLSID '12), Hyderabad, India, 2012.
- C. Merkel, D. Kudithipudi, "Reconfigurable N-Level Memristor Memory Design," *International Joint Conference on Neural Networks* (IJCNN '11), San Jose, CA, 2011.

Benjamin Briggs

Education:

- Ph.D. Candidate, Nanoscale Engineering, College of Nanoscale Science and Engineering, SUNY Albany (Expected Fall 2013)
- M.S. Nanoscale Engineering, College of Nanoscale Science and Engineering, SUNY Albany (2011)
- B.S. Electrical Engineering, SUNY New Paltz

Relevant Publications:

- N.R. McDonald, S.M. Bishop, B.D. Briggs, J.E. Van Nostrand, **N.C. Cady.** Influence of the plasma oxidation power on the switching properties of Al/CuxO/Cu memristive devices. (2012) *Solid-State Electronics. Online publication:* http://dx.doi.org/10.1016/j.sse.2012.06.007

- S.M. Bishop, B.D. Briggs, P.Z. Rice, J.O. Capulong, H. Bakhru, **N.C. Cady.** Ion implantation synthesis and conduction of tantalum oxide resistive memory layers. (2012) *Journal of Vacuum Science & Technology B.* 31(1): 012203.
- P.Z. Rice, B.D. Briggs, S.M. Bishop, **N.C. Cady.** Development of a silicon oxide based resistive memory device using a spin-on hydrogen silsesquioxane precursor. (2012) *Journal of Materials Research. Online Publication - DOI: 10.1557/jmr.2012.390*
- S.M. Bishop, H. Bakhru, S.W. Novak, B.D. Briggs, R.J. Matyi, and **N.C. Cady**. Ion Implantation Synthesized Copper Oxide-based Resistive Memory Devices. (2011) *Applied Physics Letters*. 99, 202102.

Michael Hovish

Education:

- B.S. Nanoscale Science, College of Nanoscale Science and Engineering, SUNY Albany

Employment:

- Research Assistant, Cady Lab, College of Nanoscale Science and Engineering, SUNY Albany

Relevant Work:

- B.D. Briggs, S.M. Bishop, J.O. Capulong, **M.Q. Hovish**, R.J. Matyi, and N.C. Cady, "Comparison of HfO_x-Based Resistive Memory Devices with Crystalline and Amorphous Active Layers", International Semiconductor Device Research Symposium, Baltimore, MD, Dec. 2011.

- J.O. Capulong, B.D. Briggs, S.M. Bishop, **M.Q. Hovish**, R.J. Matyi, and N.C. Cady, "Effect of Crystallinity on Endurance and Switching Behavior of HfOx-based Resistive Memory Devices", International Integrated Reliability Workshop, S. Lake Tahoe, CA, Oct. 2012.

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IX. Facilities and Equipment

The College of Nanoscale Science and Engineering (CNSE) is a fully-integrated research, development, prototyping, and educational facility that provides support through outreach, technology acceleration, business incubation, pilot prototyping, and test-based integration. 85,000 ft^2 of class 1 and class 1000 clean room space contribute to the research capabilities of the Albany NanoComplex, which hosts over 250 corporate partners on site. Location at the CNSE gives access to both advanced laboratory space and potential Phase III research partners. The location of the proposed SBIR research provides strategic leverage for bringing semiconductor technology to market.

The majority of Phase I research will be conducted in-house at the CNSE, utilizing the available class 1000 clean room space. Phase III research objectives will be aimed at scaling the technology, requiring the use of the Class 1 clean room. Facilities maintain a staff of technicians, as well as maintain service contracts with tool suppliers. In-house equipment relevant to Phase I research includes:

Deposition

- Kurt J. Lesker PVD75 DC/RF reactive sputtering tool
- Rapid Thermal Anneal furnace
- Electron Beam Evaporator

Device Characterization and Metrology

- Agilent Probe Analyzer
- Scanning Electron Microscope
- Secondary Ion Mass Spectrometry
- Transmission Electron Microscope
- X-Ray Diffractometer
- Accelerated Testing Laboratory

Deposition equipment is located in the Class 1000 cleanroom. The cleanroom is a common area, accessible to a number of employees, students and facility present on site. The facility is available for use by other universities and industrial partners. The deposition chamber is newly purchased and characterized. Capable of both DC and RF sputtering, the system is versatile and can be used to fabricate a large number of films. During Phase I research, however, the tool will be designated for HfO_2 depositions only, in order to limit contamination from the chamber walls. A more complete description of the deposition chamber follows.

Physical Vapor Deposition

A Kurt J. Lesker PVD75 sputter tool owned by Dr. Nathaniel Cady will be used for the deposition of hafnium oxide films. The chamber pressure is controlled by a turbo pump, and within the chamber there is a single two inch magnetron sputter cathode capable of both DC and RF biasing. A quartz lamp controls the chamber's temperature, ranging between 25°C and 350°C. The sample plate can rotate, aiding in uniform deposition. Preliminary research has produced a variety of hafnium oxide films, ranging from stoichiometric HfO_2 to severely sub-stoichiometric HfO.

Rapid Thermal Anneal

The Rapid Thermal Anneal furnace is run with a fully automated computer system which is capable of creating, sustaining, and repeating complex heating and cooling cycles. A thermocouple is located near the sample holder and monitors the temperature of the chamber during annealing. Quartz heating lamps located in the chamber are turned on to create intense temperature spikes, reaching rise rates of 20°C/s. Nitrogen can be flowed into the chamber at variable rates. Adjusting nitrogen flow rate gives a direct way to control the cooling rate. The system has the ability to "learn" from previous runs, whereby the computer uses thermocouple measurements to adjust the power output of the lamps. This function helps avoid overshoot during temperature rises.

Agilent Probe Analyzer

The Agilent B1500A Semiconductor Parameter Analyzer is capable of performing all of the required electrical characterization, including sweep and pulse mode measurements. Four independent tungsten SMU probes are available, each of which can be assigned a unique biasing function. During sweep mode testing, SMU1 supplies current to the top electrode of resistive memory devices; SMU2 grounds the bottom electrode. During pulse mode, a 1T1R test structure is used in which a transistor and resistive memory device are connected in series. SMU 3 is used to apply a voltage to the transistor's gate, which functions as current compliance during set. The analyzer can be programmed to monitor voltage, current, and resistance of the resistive memory devices.

Other Equipment

The other equipment listed is located within a metrology facility on site. The metrology suite is a common use area. Each tool is assigned a dedicated technician for maintenance purposes. Also available are various wafer related tools such as the diamond saw dicer.

X. Equivalent/Overlapping Proposals

NONE