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Phase Shift Controlled PWM Technique for Interleaved remote Boost Converter Based on Semiactive Quadrupler Rectifier for High Step up Applications

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Abstract

Semiactive quadrupler rectifiers (SAQRs) are proposed on this paper to serve as the seconda ry rectification circuits, which make the secondary facet voltages to be controllable and assist reduce current stress and conduction losses. An interleaved isolated raise converter is developed based totally at the proposed SAQRs. By way of utilizing the heart beat width modulation (PWM) plus section shift (PPS) control strategy, the number one and secondary facet voltages are well matched to lessen the cutting edge values and circulating conduction losses. With the proposed SAQRs, the volt age gain is extended and the voltage load on electricity devices and passive additives used in rectification circuits are decreased to the half of the excessive output voltage. consequently, the performance is progressed by the use of a transformer with a smaller turns ratio and reduced parasitic parameters, and by using low voltage score gadgets with better switching and conduction performance. With optimal design, decrease voltage, and present day stresses on the primary side switches, minimized input present day ripple may be found out. Moreover, the zero voltage switches on switching of the lively switches and the zero modern turn off switching of the diodes can be performed over a wide load and voltage range by way of the proposed SAQR based converter and the control method. In the meantime, the better voltage advantage, the lower voltage, and the current stresses on electricity devices may be obtained with the proposed SAQR based totally converter compared with passive quadrupler rectifier primarily based converter. The feasibility and effectiveness of the proposed SAQRs and the derived converter are established by a 380 V output prototype.

Keywords*—DC–DC converter, highstep up, inter leaved isolated boost converter, semiactive quadrupler rectifier, soft switching.*

INTRODUCTION

POWER systems sourced via renewable power resources and batteries had been turning into the powerful answers to compensate the worldwide energy scarcity and environmental problems [1]–[4].
Usually the 2 level configuration construct ed by a front give up dc–dc converter and a grid connected inverter is widely used, because of the low output voltages of those renewable strength resources and batteries [5]. consequently, the high step up voltage conversion ratio is needed for the dc–dc level to convert the low voltages into a sufficiently excessive voltage for the invert er. In the meantime, the galvanic isolation is anticipated to be implemented within the dc–dc level in place of within the inverter degree to reduce the dimensions of the isolation transformer and to increase the general device performance [6]. except,

the low voltage stresses on electricity gadg

ets are preferred now not handiest for cost

discount but additionally for performance development by using the low voltage score gadgets with higher conduction/swit ching performance [7], [8].The current fed converters are good candidates for these applications due to their excellent step up ability, low voltage stresses on the rectifying devices, and low input current ripple [9], [10]. However, the voltage stresses on the rectifying diodes are still high and are usually equal to the output voltage. To further reduce the voltage stresses on secondary side components, the voltage multiplier (VM) technique [11]–[13] and the series connected voltage doubler rectifiers [14] have been presented . Moreover, the transformer with the reduc ed turns ratio and small parasitic parameter s can be used to improve the efficiency, by adopting these rectification circuits. Howe ver, the input/primary side switches of these current fed converters are subjected to increased voltage stresses, which are much higher than the input voltage [15], [16]. Moreover, since only the passive components are used in the secondary side rectification circuits, the currents passing through the transformer and the rectificatio n circuits are typically in triangular form and are discontinuous [3], [9], [13]–[16]. Hence, the large peak and root–mean squared (rms) currents are induced. Furthe rmore, the high current stresses and large conduction losses, which caused by the large peak and rms currents, will hurt the efficiency of these converters. In addition, due to the passive structure of these rectification circuits, the primary side voltages are always larger than 1/*n* of the secondary side voltages during the power transferring state (*n* represents the turns ratio of transformer). Large turns ratio of transformer or large primary side duty cycle is required for high step up

applications, due to the inherent step down characteristics of the secondary side rectification circuits. Hence, the leakage inductance and turns ratio of the transformer or the voltage stresses on primary side switches are increased.

Referring to some isolated bidirectional converters [19], [20] and the semi dual active bridge converter (SDAB) [21][23], small peak/rms currents passing through transformer and rectifiers can be obtained owing to the used active switches,especial y when operated with the unity normalized voltage gain. Furthermore, since the secon dary side voltages are controllable, the higher voltage gain can be realized. Hence, the reduced turnsratio and the smaller primary side duty cycle are obtained to reduce the parasitic parameters of transformer and the voltage stresses on primary side switches. These converters in [21]–[23] can be derived by replacing two active switches with two diodes [22]. However, these converters still have some limitations that the output power cannot be regulated to zero in buck mode, hard switching in continuous conduction mode 2 (CCM2), and the large peak and rms currents of i_{LE} when operated away from the unity normalized voltage gain.

In this paper, the concept of semiactive quadrupler rectifiers (SAQRs) is proposed to alleviate the limitations of the current fed converter discussed above. These SAQRs are derived by replacing the diodes in rectification circuits by active switches or by adding the extra bidirection al switch. The major contribution of this p- aper is to propose the novel interleaved isolated boost converter by employing the SAQRs . decrease voltage stresses on the primary side switches and decreases

modern day stresses at the secondary aspect rectification circuit were accomplis hed for the proposed SAQR primarily based converter as compared with those with passive rectifiers. the pulse width modulation (PWM) plus phase shift (PPS) control approach is followed due to its benefits in bi directional converter [19], and the unmarried stage energy conversion, gentle switching overall performance, and low input modern ripples can be executed with the proposed converter.

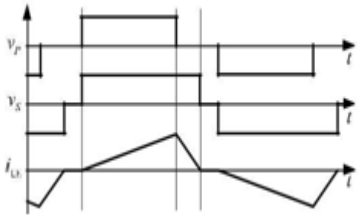


Fig. 1. Typical waveforms of the converter with passive rectifiers.

DERIVATION AND OPERATIONAL PRINCIPLES OF THE PROPOSED INTE RLEAVED ISOLATED BOOST CONVERTER WITH SAQR

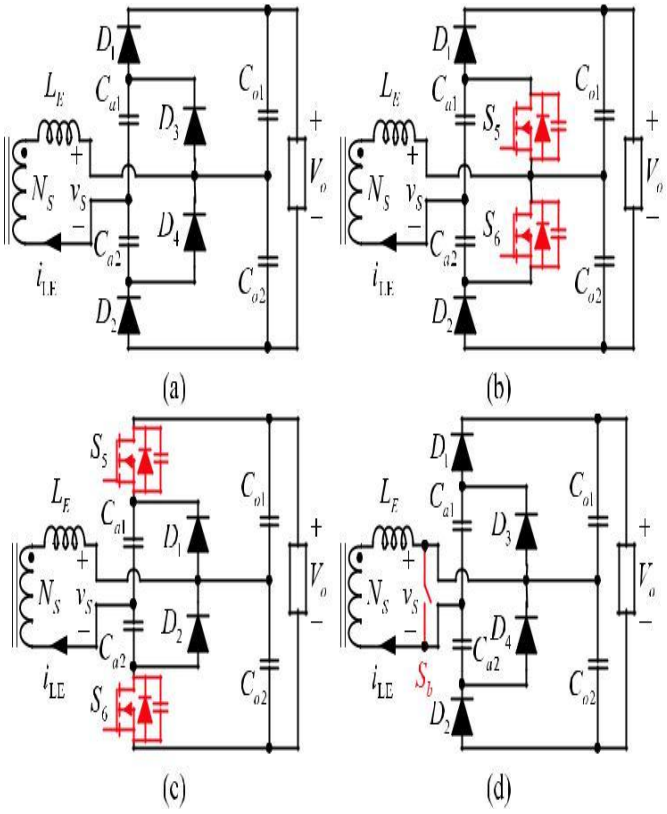
Derivation of the Proposed Converter With SAQR

The passive VM with reduced voltage stresses and the soft switching performanc e for the secondary side rectifying diodes is given in Fig. 1(a). However, since only the passive devices are used in the secondary side rectification circuit, the primary side and secondary side voltages v_P and v_S would have the following relationship:

$$n \cdot v_P > v_S \qquad (1)$$

where n is the turns ratio of the transformer defined as $n = N_S : N_P$, and N_P and N_S are the primary and secondary windings of the transformer. As a result, due to this step down characteristic of the converter with passive secondary side circuits, the current passing through the secondary winding of transformer/inductor is typically in triangular form and is discontinuous (the typical waveforms are shown in Fig. 2). Hence,

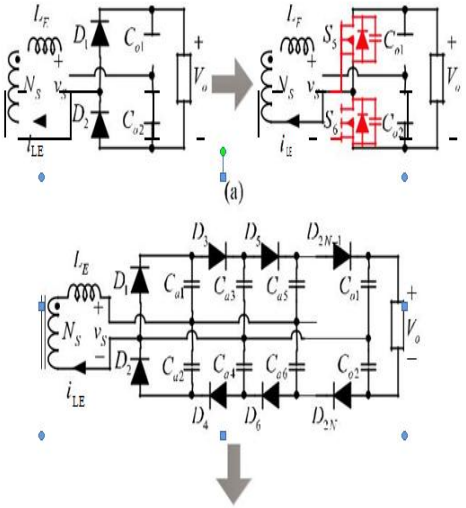
.Fig.2. (a) Passive voltage multiplier. (b)–(d) Proposed SAQRs.



the large peak and rms currents flowing through rectification circuit are induced, which results in the high current stresses and large conduction losses. Meanwhile, since the voltage gain can only be regulated by the primary side circuit and the transformer, the large duty cycle or transformer turns ratio is required, which results in the high voltage stresses on primary side switches or large parasitic parameters of transformer, and thus, the efficiency would be hurt.

Referring to some isolated bidirectional converters and the SDAB converters, the current flowing through transformer windings and rectifiers can be regulated with trapezoidal shape, by adopting active switches in the rectification circuits. Furthermore, with secondary side phase shift control, reduced duty cycle of primary side main switches and smaller turns ratio of transformer can be obtained although the number of active switches is increased and the control will become a little complicated. However, with the active switches used in the rectification circuit, the secondary side voltage v_S is control lable. Thus, the small peak and rms currents passing through transformer/induc tor, the low voltage rating switches, and the transformer with reduced parasitic parameters can be obtained to improve the efficiency.

As shown in Fig. 1, the SAQRs are developed by replacing the diodes in rectification circuit by active switches or developed by adding extra bidirectional switch S_b. From the perspective of the switches number, the SAQRs shown in Fig. 1(b) and (c) are promising approaches . As an example, the SAQR shown in Fig. 1(b) is analyzed in detail to verify the advantages of the proposed SAQR based converter compared with the converter with passive VM given in Fig. 1(a). The topology derivation idea can be further applied to other.



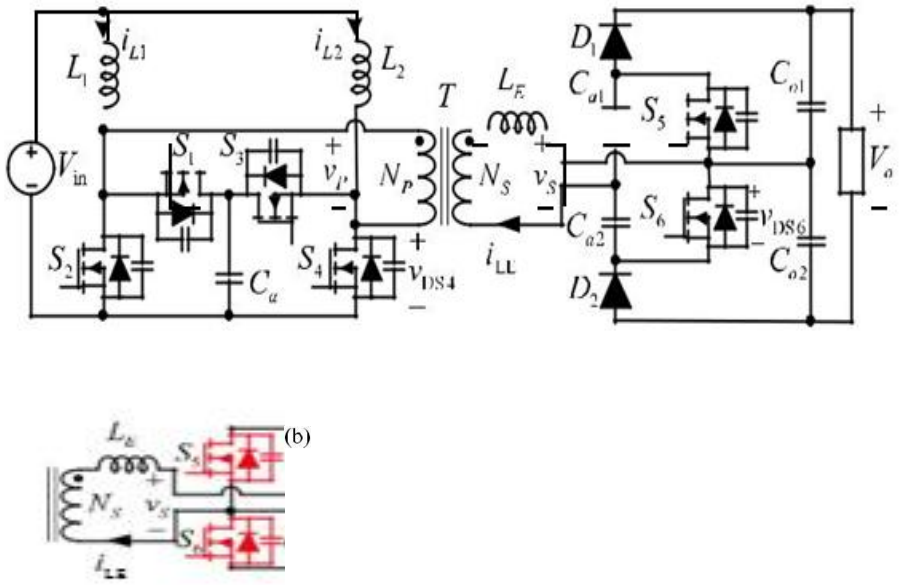
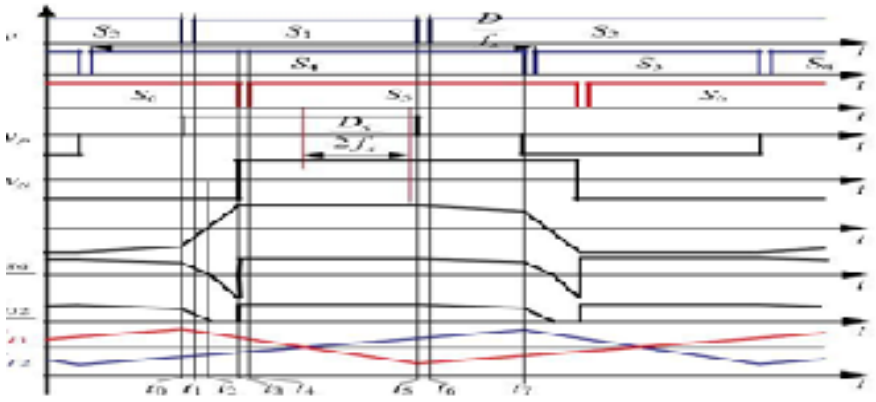


Fig.3. Topology derivations based on other passive rectifiers.
(a) Voltage doubler. (b) *n* stage voltage multiplier.

passive rectifiers, as shown in Fig. 3 as an example, and only two active switches are needed. Compared with the method by replacing all the diodes with the active switches, which is used to derive the converter in [19] from the one in [24], less active switches are required and the cost will be reduced.



(a)

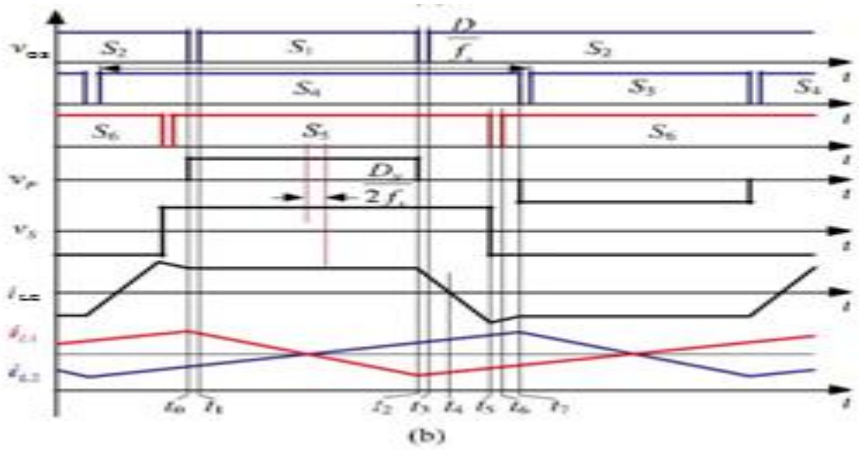


Fig. 5. Switching waveforms of the proposed converter.
(a) $D > 0.5$ and $D_S > D - 0.5$. (b) $D > 0.5$ and $0 < D_S < D - 0.5$.

Operational Principles of Proposed Converter with SAQR

The topology of the proposed interleaved isolated boost converter with SAQR is drawn in Fig. 4. The primary side of the converter is an interleaved isolated boost circuit, and the secondary side is a semiact ive rectifier composed of two active switch es and two diodes. As illustrated in Fig. 4, L_1 and L_2 are input inductors. It should be noted that, in practice, the inductor L_E can be implemented either only with the leakage inductance of the transformer or with an external inductor to achieve the de sired value. Compared with the equivalent input stage given in [19] with using two coupled inductors, the small contemporary stresses of the input inductors and transfor mer are provided with the interleaved isolated enhance circuit, and it'll be easy to optimal design of these magnetic additives one at a time. The best consistency of pressure circuits has been realized, or even without the dc blocking off capacitor, the dc component of the transformer could be very small and the middle saturation problem is prevented.

To achieve small input current ripple and good soft switching performance, the PWM PPS control strategy is applied to the proposed converter. The primary side switches S_2 and S_4 are operated under the same duty cycle D and the driving signals for S_2 and S_4 have the 180° phase shifted angle between each other. The switches S_1 and S_2 (or S_3 and S_4) are operated complementarily with reasonable dead time. The secondary side switches S_5 and S_6 have a constant duty cycle of 0.5 and are under complementary operation. By PWM control, the

Amplitude of voltage v_P and v_S illustrated in Fig. 5 are well matched, which can reduce circulating conduction loss and peak/rms values of inductor currents of L_E. Therefore, the volt age V_C on the capacitor

C_a and the output voltage V_o will have the following relationship:

$$V_C = V_o/4n \ldots\ldots\ldots\ldots \quad (2)$$

and v_S, and the secondary side phase shift ratio is defined as

$$D_S = \phi_S/\pi. \quad (3)$$

The power flow of the proposed converter is controlled by changing the secondary side phase shift ratio D_S. The detailed operational principles of the proposed converter when $D > 0.5$ and $D_S > D - 0.5$ will be presented as follows.

Fig. 5(a) shows the operational waveforms of the proposed converter when $D > 0.5$ and $D_S > D - 0.5$, where f_s is the switching frequency. The input inductors L_1 and L_2 are designed to ensure the current i_{L1} and i_{L2} are continuous in one switching cycle and $L_1 = L_2$. For simplification, the parasitic capacitances of MOSFET are ignored and the transformer is assumed to be ideal. There are 14 switching states in one switching period. Due to the symmetry of the circuit, only seven states are analyzed here and corresponding equivalent circuits for each switching state are shown in Fig. 6.

The secondary side phase shift angle ϕ_S is defined as the phase difference between the fundamental components of v_P

State 1 [t_0, t_1] [see Fig. 6(a)]: Before t_0, S_2, S_4, S_6, and D_1 are on, and the inductor current $i_{LE} < 0$. The energy stored in the inductor L_E is delivered to the load. Inductor L_1 and L_2 are charged by the input voltage source and capacitors C_{o1} and C_{a2} are charged, whereas C_{o2} and C_{a1} are discharged. At t_0, S_2 is turned off and the body diode of S_1 begins to conduct due to the energy stored in the L_1 and L_E. In this state, the inductor current i_{LE}, i_{L1}, and i_{L2} can be calculated by

$$\begin{aligned} i_{LE}(t) &= (nV_C + V_o/4)\,(t - t_0)/L_E + i_{LE}(t_0) \\ i_{L1}(t) &= (V_{in} - V_C)\,(t - t_0)/L_1 + i_{L1}(t_0) \quad (4) \\ i_{L2}(t) &= V_{in}\,(t - t_0)/L_2 + i_{L2}(t_0). \end{aligned}$$

State 2 [t_1, t_2] [see Fig. 6(b)]: At t_1, S_1 is turned on with zero voltage switching (ZVS). This state ends when the inductor current i_{LE} recovers to zero, and D_1 is turned off naturally with zero current and without reverse recovery loss.

State 3 [t_2, t_3] [see Fig. 6(c)]: At t_2, the inductor current i_{LE} recovers to zero, and during this state, L_E is charged by the voltage V_C and the voltage on the capacitor C_{a2}.

State 4 [t_3, t_4] [see Fig. 6(d)]: At t_3, S_6 turns off, and the body diode of S_5 and the diode D_2 begin to conduct due to the energy stored in the inductor L_E. In this state, capacitors C_{o2} and C_{a1} are charged, while C_{o1} and C_{a2} are discharged. Due to the PWM control, the voltage v_P and v_S are well matched,and therefore, the voltage on the L_E is zero and inductor current i_{LE} remains the same during this state.

State 5 [t_4, t_5] [see Fig. 6(e)]: At t_4, S_5 turns on with ZVS. The energy is transferred to the output from the source

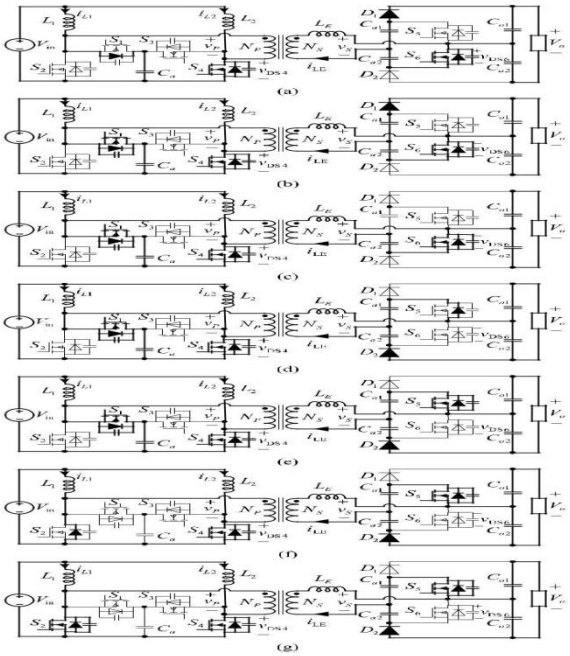
Fig.6. Equivalent circuits for each operation continuously in this state and it end when S_1 turns off at t_5.

State 6 [t_5, t_6] [see Fig. 6(f)]: At t_5, S_1 is turned off and the body diode of S_2 begins to conduct due to the energy stored in the L_1 and L_E. In this state, only the energy stored in the L_E is transferred to load while L_1 is charged by input voltage source. The inductor current i_{LE} and i_{L1} can be calculated by

$$i_{LE}(t) = -V_o\,(t - t_5)\,/4L_E + i_{LE}(5)\,(t_5)$$

$$i_{L1}(t) = V_{in}\,(t - t_5)\,/L_1 + i_{L1}\,(t_5)\,.$$

State 7 [t_6, t_7] [see Fig. 6(g)]: At t_6, S_2 turns on with ZVS and this state ends when S_4 turns off at t_7.



state when D >0.5 and $D_S > D - 0.5$. (a) State 1 [t_0, t_1]. (b) State 2 [t_1, t_2]. (c) State 3 [t_2, t_3]. (d) State 4 [t_3, t_4]. (e) State 5 [t_4, t_5]. (f) State 6 [t_5, t_6]. (g) State 7 [t_6, t_7].

similar operation works in the rest states of the switching period. The detailed operatio nal waveforms of the proposed converter under D > 0.5 and 0 < D_S < D

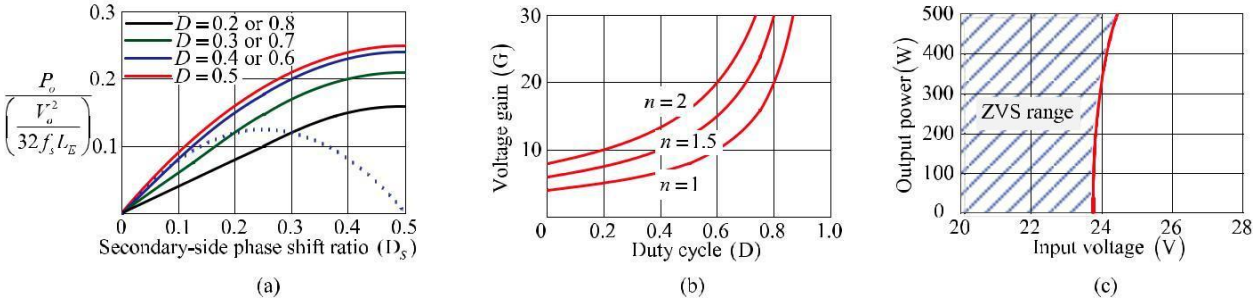


Fig. 7. Performance of the proposed converter. (a) Output power curves. (b) Voltage gain. (c) ZVS range of S_2 and S_4.

Fig. 5(b). The steady state switching waveforms when $D < 0.5$ and the detailed analysis are omitted here considering the length of this paper.

III. PERFORMANCE ANALYSIS AND DISCUSSION

A. *Output Power*

According to the operational principles of the proposed converter when $D > 0.5$ and $D_S > D - 0.5$ and the waveforms shown in Fig. 5(a), we have $i_{LE}(t_0) + i_{LE}(t_7) = 0$, $i_{LE}(t_3) = i_{LE}(t_5)$, and $i_{LE}(t_2) = 0$. Then based on (2), (4), and (5), the value of $i_{LE}(t_0)$, $i_{LE}(t_3)$, and T_2 can be obtained as

$$iLE\,(t0) = -(DS - 2D + 1)\,Vo/8fsLE$$
$$i_{LE}\,(t_3) = D_S V_o/8f_s L_E \qquad (6)$$
$$T_2 = t_2 - t_0 = (D_S - 2D + 1)/4f_s.$$

Ignoring the power loss during the power conversion, the output power can be given by

$$P_o = D_S\,(1 - D_S) - 0.25(1 - 2D)^2\; V_o^2 / 32 f_s L_E. \qquad (7)$$

B. *Voltage Gain*

According to the operation analysis of the proposed converter with SAQR, the relationship between the input voltage and voltage on capacitor C_a can be obtained as

$$V_C = V_{in}/(1 - D). \qquad (10)$$

The voltage gain G is defined as

$$G = V_o/V_{in}. \qquad (11)$$

By substituting (2) and (10) into (11), G is obtained as

$$G = 4n/(1 - D). \qquad (12)$$

The voltage gain curves versus the duty cycle D with different values of turns ratio n are plotted in Fig. 7(b). It can be seen high voltage gain can be achieved with the proposed SAQR based interleaved isolated

boost converter even with the turns ratio $n = 1$ and a small duty cycle.

Similarly, the output power of the proposed interleaved isolated boost converter with SAQR when $D > 0.5$ and $0 < D_S < D - 0.5$ can be given by

$$P_o = D_S(1 - D)V_o^2\ 16f_sL_E. \quad (8)$$

The output power of the proposed converter when duty cycle $D < 0.5$ can be given by

$$P_o = \begin{cases} \dfrac{[D_S(1-D_S) - 0.25(2D-1)^2]V_o^2}{32f_sL_E}, & D_S \geq 0.5 - D \\ D_SDV_o^2\ 16f_sL_E, & 0 < D_S < 0.5 - D. \end{cases} \quad (9)$$

According to (7)–(9), the output power curves versus the secondary side phase shift ratio D_S with different duty cycle D are shown in Fig. 7(a). From the output power equations and the curves given in Fig. 7(a), it can be seen that the maximum output power occurs when D_S is equal to 0.5, and with the secondary side phase shift control, the output power can be under control within the entire operation range. On the other hand, when operated with duty cycle $D = 0.5$, the proposed converter has the strongest power transmission capability. Meanwhile, with larger or smaller duty cycle than 0.5, the

Power transmission capability will be wea kened.

C. *Soft Switching*

1) *Secondary Side Switches:* Due to the energy stored in inductor L_E, the inductor current i_{LE} would flow through the body diode of MOSFET during dead time before turning on the MOSFET, and ZVS is achieved. Therefore, the ZVS conditions of secondary side active switches when duty cycle $D > 0.5$ can be obtained as

$$\begin{aligned} &i_{LE}(t_3) > 0, \text{ when } D_S \geq D - 0.5 \\ &i_{LE}(t_5) < 0, \text{ when } 0 < D_S < D - 0.5. \end{aligned} \quad (13)$$

By substituting (6) into (13), the ZVS conditions of the secondary side active switches are given as

$$\begin{aligned} &D_S > 0, \text{ when } D_S \geq D - 0.5 \\ &D > 0.5, \text{when } 0 < D_S < D - 0.5. \end{aligned} \quad (14)$$

Thus, ZVS can be always achieved for secondary side switches S_5 and S_6, and by using the same analysis method, it can be derived that the ZVS for S_5 and S_6 can also be realized within full range when duty cycle $D < 0.5$. Thanks to the phase shift control strategy, zero current switching (ZCS) can be achieved for all of the secondary side diodes within full range.

2)Primary Side Switches: For the primary side switches, the current through switches when they are turned

on/off is related to both the input inductor current and the current i_{LE}. As a result, the ZVS conditions of primary side switches are determined by various factors such as the inductor L_E, the input inductor L, and the input/output power. To simplify the analysis, the parasitic capacitances of MOSFET are ignored and the inductor L_1 and L_2 have good current sharing performance. Once the body diode of MOSFET is on before turning on the

MOSFET, ZVS can be achieved. Therefore, the

ZVS conditions of the primary side switches when $D > 0.5$ and $D_S > D - 0.5$ can be obtained as

$$i_{LH} - ni_{LE}(t_0) > 0, \text{ for } S_1\&S_3 \quad (15)$$
$$i_{LL} - ni_{LE}(t_5) < 0, \text{ for } S_2\&S_4$$

where i_{LH} and i_{LL} are the peak and valley values of the input inductor current and based on the operation analysis, the value of i_{LH} and i_{LL} can be derived as

$$^{i}\text{L} = P_o/2V_{in} + DV_{in}/2f_sL \quad (16)$$
$$\text{H}$$
$$i_{L1L} = P_o/2V_{in} - DV_{in}/2f_sL.$$

By substituting (6), (16) and $i_{LE}(t_5) = i_{LE}(t_3)$ into (15), the detailed constraints of ZVS performance for the primary side switches can be obtained as

S_1 & S_3 : $P_o/2V_{in} + DV_{in}/2f_sL + n^{(DS-2D+1)Vo} > 0$

$8f_sL_E$

S_2 & S_4 : $P_o/2V_{in} - DV_{in}/2f_sL - nD_SV_o/8f_sL_E < 0.$
(17)

Similarly, the ZVS conditions of primary side switches when $D > 0.5$ and $0 < D_S < D - 0.5$ can be obtained as

S_1 & S_3 : $P_o/2V_{in} + DV_{in}/2f_sL - nD_SV_o/8f_sL_E > 0$

$-nD_SV_o/8f_sL_E < 0.$ (18)

Substituting (7)–(9) into (17) and (18), the ZVS conditions of primary side switches can be obtained with the help of Calculation Software Math cad under the following conditions of the proposed converter: $V_{in} = 20 - 28\ V$, $V_o = 380\ V$, $V_C = 47.5\ V$, $n = 2$, $L = 50\ \mu$H, $L_E = 8.5\ \mu$H, and $f_s =$ 100 kHz. The expressions for ZVS boundary of the primary side switches are very complex and are omitted here. By

Math cad, it is derived that the ZVS soft switching for switches S_1 and S_3 can be achieved within full voltage and load range, while that of switches S_2 and S_4 will be realized in a wide operation range depending on the voltage and power and the ZVS range of S_2 and S_4 is plotted in Fig. 7(c).

According to the operational analysis, it can be found that the main dc component of input inductor current is opposite to

The direction of the current that can flow through the body diode of S_2 and S_4. This is the reason why the ZVS range of S_2 and S_4 is narrow. Furthermore, if the output capacitances of S_2 and S_4 are taken into considerations, the small current $ni_{LE} - i_L$ will be hard to fully discharge the output capacitance during the dead time, which makes the ZVS turn on hard to realize. To further ensure the ZVS turn on of S_2 and S_4, the large current ripple of i_L is required. However, higher current stress and larger conduction losses are induced due to the increased peak and rms current values, which will do harm to the efficiency.

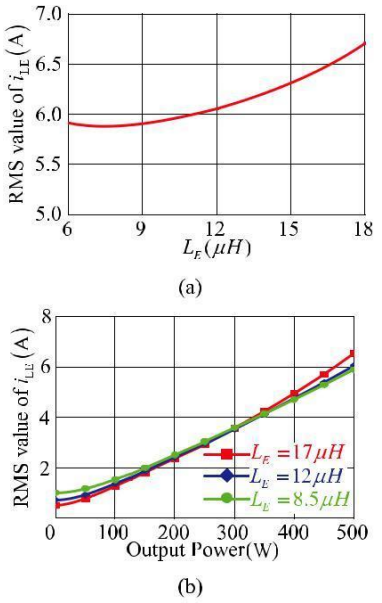


Fig. 8. RMS current curves of i_{LE}: (a) versus L_E at output power of 500W and (b) versus output power.

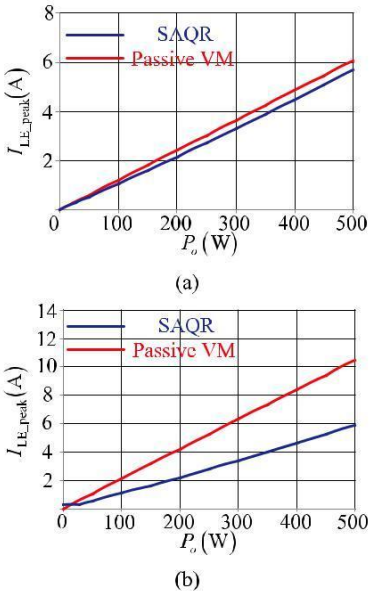


Fig. 9. Inductor current comparisons. (a) RMS value. (b) Peak value.

D. Design Considerations

A 500 W prototype is built as the example of parameter design procedure. The converter is designed for high step up applications with the input voltage of 20–28 V, the output voltage of 380 V, and the switching frequency of 100 kHz.

1) *Turns Ratio of Transformer:* According to the anal

ysis mentioned above, the large input inductor current value and the output capacitances of S_2 and S_4 will make the ZVS turn on hard to realize. Furthermore, if converter operated with D > 0.5 over full input voltage range, the voltage V_C on the capacitor C_a will be larger compared with that when operated with D around 0.5. Therefore, with D around 0.5, the primary side switches suffer lower voltage stresses, and the low voltage

TABLE I
PERFORMANCE COMPARISONS

Components	The proposed converter	Converter with passive VM	Converter in [14]
Secondary-side active switches	2	0	0
Secondary-side diodes	2	4	4
Voltage stresses on the secondary-side components	$V_o/2$	$V_o/2$	$V_o/2$
Voltage stresses on the primary-side components	Low	High	High
Voltage gain	High	Low	Low
Peak/RMS currents of L_E	Low	High	High
Current stresses and conduction losses	Low	High	High
Soft-switching of secondary-side switches	S_5&S_6: ZVS turn-on D_1&D_2: ZCS turn-off	D_1–D_4: ZCS turn-off	D_1–D_4: ZCS turn-off
Number of transformers	1	1	2
Power rating of transformer	P_o	P_o	$P_o/2$

Fig. 10. Photograph of the tested prototype.

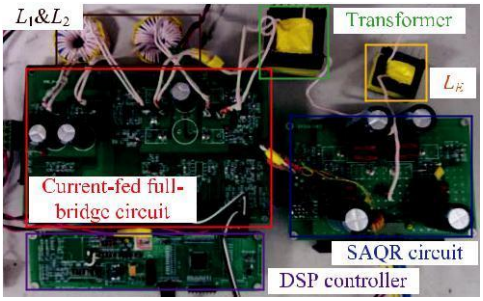


TABLE II-COMPONENTS AND PARAMETERS OF THE PROTOTYPES

Components	Parameters
Input voltage (V_{in})	20–28 V
Output voltage (V_o)	380 V
Maximum output power (P_o)	500 W
Switching frequency	100 kHz
Turns ratio of transformer	1:2
Inductor L_E	8.5 μH
Primary-side MOSFETs	IPP037N08N
Secondary-side MOSFETs	IRF4229
Secondary-side diodes	DPG20C300PB

Rating devices with better switching/conduction performance can be used to reduce the switching and conduction losses. Meanwhile, the input current ripple can be minimized with D around 0.5 and the peak/rms values of input inductor currents can be reduced compared with operated under $D > 0.5$ within full range. As a result, the turn's ratio of the transformer is designed to ensure the converter operated with D around 0.5 and can be designed as

$n = 380 \quad = 1.98.$ (19)

$4 \times 24/ (1 - 0.5)$

Thus, in practical implementation, the turn s ratio of trans former is selected at 2 and V_C is set to 47.5 V. Compared with the design method presented in [19] with $D >$ 0.5 within full range, although the ZVS range of S_2 and S_4 will be narrowed, the use of low voltage rating devices and reduced input inductor current ripples and rms values will improve the efficiency.

2) *Inductor L_E:* The inductor L_E not only determines the power transmission capabil ity of the proposed converter but also will have great influence on the rms values of i_{LE}, which will affect the conduction losses of the proposed converter. The rms current curves with different values of inductor L_E and output power are shown in Fig. 8, which are plotted under the following conditions with V_{in} = 20 V , V_o = 380 V , and f_s = 100 kHz. According to Fig. 8(a), it can be seen that with the decrease of inductor L_E, the rms value of i_{LE} will decrease at first, and when L_E is smaller than 7.5 μH, the rms value will increase. On the other hand, with the decrease of inductor value [see Fig. 8(b)], the rms values of i_{LE} are increased when $D_S < D - 0.5$ while decreased when $D_S > D - 0.5$. Therefore, with the decrease of L_E, the conduction losses of switches with large output power are reduced while those at light load are increased. Meanwhile, if operated with D close to 0.5, the proposed converter will mainly be operated with $D_S > D - 0.5$ and the decrease of L_E will bring benefits within full load range. Therefore, a tradeoff has been made and the inductor L_E is designed as 8.5 μH.

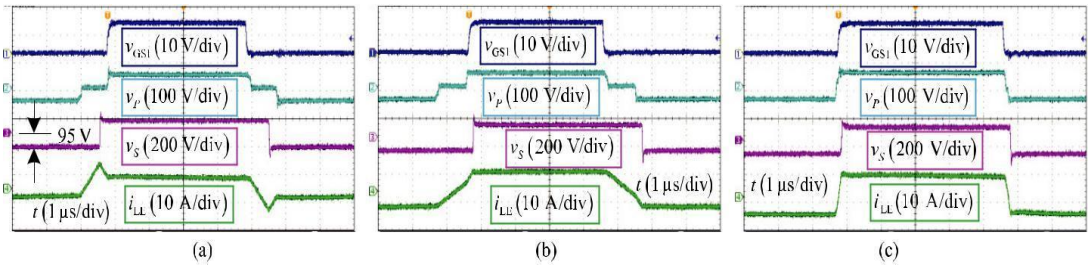
E. Performance Comparison between the Proposed Converter and the Converter with Passive VM

1) *Voltage Gain Comparison:* For the interleaved isolated boost converter with passive VM given in Fig. 1(a), the voltage v_P will be always larger than v_S/n, then the following equation is obtained:

$$V_C > V_o/ 4n. \quad (20)$$

The voltage gain of the converter with passive VM can be given by

Fig. 11. Steady state waveforms of the proposed converter when duty cycle $D \geq 0.5$, driving voltages of S_1 (v_{GS1}), square wave voltages on primary and secondary side (v_p, v_s), and current through the inductor L_E (i_{LE}). (a) $D > 0.5$ and $D_S < D - 0.5$. (b) $D > 0.5$ and $D_S > D - 0.5$. (c) $D = 0.5$.



$G = V_o/ V_{in} < 4nV_C / V_{in} = 4n/ (1 - D)$. (21)

By comparing (12) and (21), it can be seen that the voltage gain of the converter with passive VM is always smaller than that of the proposed SAQR based converter. To obtain the same voltage gain with the same turnsratio n, the duty cycle of the proposed converter is smaller, and smaller voltage stresses on primary side switches have been obtained.

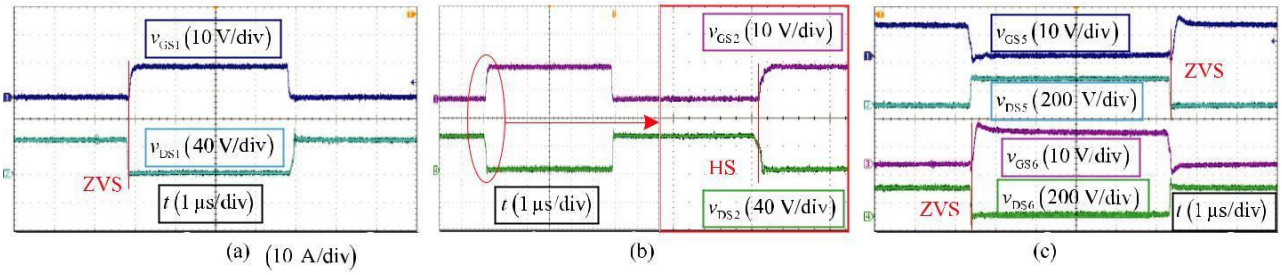


Fig. 12. Zero voltage switching waveforms of the proposed converter with $D \geq 0.5$: (a) driving and drain source voltages of S_1 (v_{GS1} and v_{DS1}), (b) driving and drain source voltages of S_2 (v_{GS2} and v_{DS2}), and (c) driving and drain source voltages of S_5 and S_6 (v_{GS5}, v_{DS5},v_{GS6}, and v_{DS6}).

2) *Inductor Current i_{LE} Comparison:* The inductor L_E has a great influence on the peak and rms values of current i_{LE}. Therefore, it will have great effects on both conduction losses and current stresses of switches and transformer/inductor. The inductor current comparison results between the proposed converter and the converter with pas

sive VM are shown in Fig. 9. These curves are plotted under the following conditions: V_{in} = 24 V, V_o = 380 V, V_C = 47.5 V, f_s = 100 kHz, n = 2, and L_E = 8.5 μH.

From the comparison results shown in Fig. 9, it can be seen that both the rms and peak values of the inductor current i_{LE} in the proposed converter are smaller than that of the converter with passive VM, especially for the peak values. Thus, the proposed converter offers the better performances with smaller conduction losses and lower current stresses compared with the convert

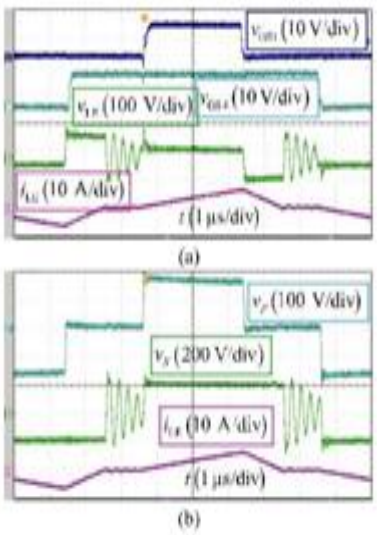
er with passive rectifiers. Moreover, less winding turns and smaller air gap are required to prevent saturation of the inductors in the proposed converter.

The performance comparisons between the proposed SAQR based converter, the converter with passive VM, and the con

verter presented in [14] are summarized in Table I. It should be noted that single transformer or the inductor L_E suffers low current stress in [14], but two transformers and inductors are used and the total current stresses are still high. Meanwhile, the mismatch of two transformers and inductors may cause the voltage and the power unbalance problem. Although two active switches are required in the proposed SAQR based converter and control implementation becomes a little complicated. The proposed SAQR based converter offers better performances with smaller voltage stresses on the primary side switches, lower peak/rms currents of

L_E, lower current stress and conduction losses, and higher voltage conversion gain.

Fig. 13. Steady state waveforms of the interleaved isolated boost con verter with passive VM under $V_{in} = 20\ V$. (a) v_{GS1} and v_{GS4}, voltage applied on the inductor L_E (v_{LE}) and i_{LE}. (b) v_p, v_s, and i_{LE}.



IV. EXPERIMENTAL VERIFICATION AND ANALYSIS

A 500 W prototype of the proposed interleaved isolated boost converter with SAQR (as shown in Fig. 4) is built to verify the feasibility of the proposed SAQRs and the derived converter. The photograph of the tested prototype is shown in Fig. 10 with the detailed descriptions. The specifications are listed in Table II. As well, a prototype of the converter with passive rectifiers given in Fig. 1(a) is built with the same specificatio ns. Both the two prototypes are implement ed with the same printed circuit board (PCB), switches, and core materials for transformer/inductors, which ensure that the experimental comparisons are conduct ed under the same conditions.

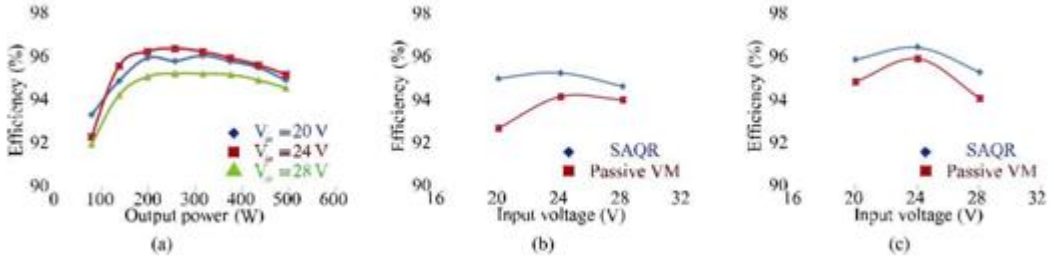


Fig. 14. Measured efficiency curves. (a) Proposed converter. (b) Comparisons at full load with the converter with passive VM. (c) Comparisons at half load.

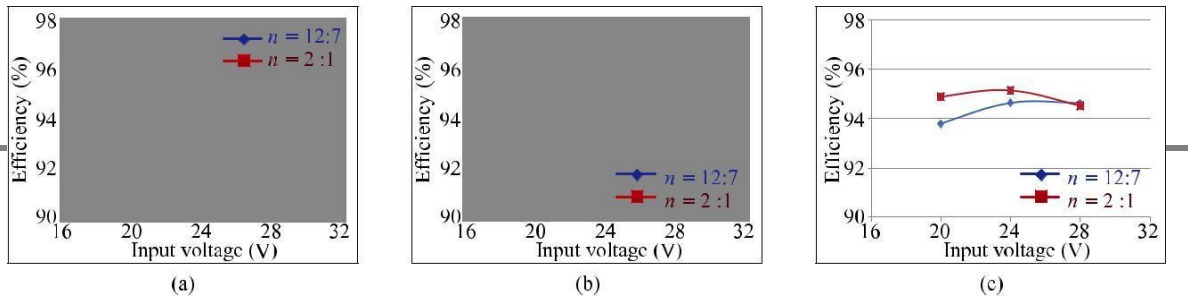


Fig. 15. Efficiency comparisons with n = 12 : 7. (a) Light load. (b) Half load. (c) Full load.

The steady state waveforms of the proposed converter under $D \geq 0.5$ are shown Fig. 11. The waveforms in Fig. 11(a) and

(b) Are tested under 20 V input voltage with $D > 0.5$ while that in Fig. 11(c) are tested under $D = 0.5$. From the wave forms shown Fig. 11, it can be seen that the inductor current i_{LE} maintains constant during the power transferring state, because the primary and secondary side voltage v_P and v_S are well matched due to the PWM PPS control. The amplitude of v_S is only 95 V which is a quarter of the output voltage. Thus, the voltage can be stepped up to 380 V from 20 V using a transformer with a small turns ratio n = 2. As shown in Fig. 11(c), the equivalent duty cycle of v_P reaches maximum value when operated with D = 0.5. The experimental waveforms match the theoretical analysis pretty well.

The switching waveforms of the proposed converter with $D \geq 0.5$ are shown in Fig. 12. It can be seen that the ZVS soft switching performance of primary side upper switches (S_1 and S_3) and secondary side switches (S_5 and S_6) can be achieved. However, the ZVS performance is lost for primary side lower switches (S_2 and S_4), which is because only a small current is used to discharge the output capacitances of S_2 and S_4. From Fig. 12(b), it can be seen that the drain to source voltage of S_2, v_{DS2}, has already decreased before S_2 is turned on but it did not decrease to zero, which satisfied the theoretical analysis.

Fig. 13 shows the experimental waveforms of the converter with passive VM, which are tested under 20 V input voltage. It can be seen that, the inductor current i_{LE} increases during the power transferring state. Moreover, the voltage applied to the inductor L_E is positive, which means the v_P is larger than v_S/n and it is satisfied with the theoretical analysis. Comparing the experimental waveforms shown in Figs. 11 and 13, which are tested under the output power of 500 W, the peak value of i_{LE} is about 6.5 A in the proposed converter and is about 13 A in the converter with passive VM, which match the previous Analysis and indicate that the proposed converter suffers lower current stresses.

The efficiency curves of the proposed converter are plotted in Fig. 14(a). These tested results indicate that high conversion efficiency is achieved over wide input voltage and load range owing to the soft switching operation, the utilization of low voltage rating power devices, and small peak/rms currents. The highest efficiency is reached when the input voltage is 24 V and the duty cycle D is equal to 0.5. The maximum value is about 96.33%, and the efficiencies higher than 95% have been achieved over a wide load and voltage range.

The comparisons between the proposed converter and the converter with passive VM are shown in Fig. 14(b) and (c). It can be seen that, the measured efficiencies of the proposed converter are higher within full voltage range with different output loads, which satisfied the theoretical analysis well. The measured and comparison results indicate that the proposed SAQRs and the derived

converter are good candidates for high step up dc–dc conversion applications.

To accurately verify the effectiveness of the proposed design methods, a prototype, with the same PCB, switches, and core materials for transformer/inductors with the turns ratio of trans former n = 12 : 7 to maintain D > 0.5 within the full input voltage range, has been built. The inductor L_1 and L_2 are the same and the inductor L_E is redesigned as 12.95 μH following the same design ideal given in Section III E. The measured efficiency comparison results with different output powers are given in Fig. 15. It can be seen that the efficiency results will be higher with n = 2 : 1 compared with those with n = 12 : 7 especially at the full load. Furthermore, the same primary side switches are used in these two prototypes and since the lower voltage rating devices with better switching and conduction performance can be used when n = 2 : 1, the efficiency results can be further improved.

CONCLUSION

The SAQRs and the derived interleaved isolated boost converter have been propose d to fulfill the requirements of high step up conversions. The secondary side voltages are controlled to match the primary side voltages, and to reduce current stress and conduction losses, using the PWM PPS modulation. The voltage stresses on the components in SAQRs are reduced to half of the output voltage which extends the voltage conversion ratio. Hence, low voltage rating switching devices with bette r conduction and switching performance have been used to improve efficiency. Moreover, the ZVS turn on of the active switches and the ZCS turn off have been achieved by the proposed PWM PPS modulation. With optimal design, low voltage stresses on the primary side switches together with the reduced input current ripple and peak/rms values have been obtained to improve the conversion efficiency. The operating principles, the output characteristics, and the soft switching performance of the proposed SAQR based interleaved isolated boost converter are presented in detail. Meanwhi le, the advantages of the proposed converte r with SAQR compared with the passive rectifier based converter are analyzed and verified by experimental results. The analysis and performance have been fully validated experimentally on a 20–28 V input, 380 V output hardware prototype. E xperimental results demonstrate that the proposed SAQR based converter is an excellent candidate for high efficient high step up applications.

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