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Design and Analysis of 4x4 Vedic Multiplier using Carry Save and Vertical Adder

AnkurMaloo
Electronics and Communication,
RCOEM, Nagpur, India

JyotiprakashChoudhary
Electronics and Communication,
RCOEM, Nagpur, India

Prof.PrasheelThakre
Electronics and Communication,
RCOEM, Nagpur, India

Abstract

In digital signal processing multiplication is one of the key operations between two sequences. Multiplication is used in convolution of two signals used especially for filter design operation. So it is necessary that multiplication should be performed efficiently with less area and delay. Vedic mathematics is one of the method by which we can reduced area and delay. In this paper we have design 4x4 Vedic multiplier by using the concept of Vedic mathematics; we have used UrdhvaTiryabhyam which is one of the 16 sutras which are used in Vedic mathematics. We have design Vedic multipliers using vertical adder and carry save adder in Xilinx 14.7 software using VHDL and stimulation result are obtain and there area and delay are computed.

Keywords: *Vedic Mathematics, UrdhvaTiryagbhyam, Vertical adder and Carry Save adder*

INTRODUCTION

Multiplier is the basic block in any DSP processor with the advancement in the technology the operation time must be reduced with the conventional method the time and area which is required is much larger, so some alternate method must be needed so that area and delay can be reduced for that vedic mathematics is one of the method by which we can reduced area and delay. Vedic mathematics [1] depends upon the sixteen sutras out of which we have used UrdhvaTriyakbhyam [2] sutra or UT sutra which means vertical and crosswise, which is specially used for the multiplication of two numbers. The algorithms which are used in the Vedic mathematics are much simple and also easy to design.

The used of Vedic mathematics in multiplier design results in reduced in area required and also delay is less. The most important advantage of Vedic multiplier is that linearity of Vedic multiplier from 2 bit Vedic multiplier we can bulid 4 bit Vedic multiplier from 4 bit Vedic multiplier we can bulid 8 bit multiplier and so on. And another advantage of Vedic multiplier is that as the number of bits increases the delay increases at very slow rate, due to which even at large no of bits operation the delay is less.

Next important thing while designing the Vedic multiplier is the adder which is used for adding partial product. For fast operation the adder which is used must also perform addition faster for that we have used carry save and vertical adder for addition and the result of both the adder is computed in terms of delay and LUTs is obtained and compared.

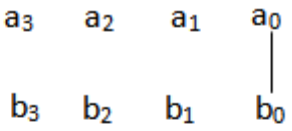
URDHVA-TRIYAGBHYAM SUTRA

The word “UrdhvaTiryakbhyam” is Vedic

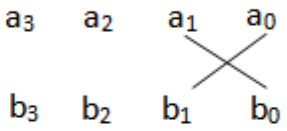
sutra which means vertical and crosswise multiplication [3]. This alogrithm can be applied to integers, floating point complex numbers and can be used in decimal and binary number system both. The number of operation that has to be performed is same as that in conventional multiplication method; only thing is that delay is less. Advantage of using this type of multiplier is that as the number of bitsincreases, delay and area increases very slowly as compared to other conventional multipliers [4].

The 4 bit multiplicayion steps are as follows:

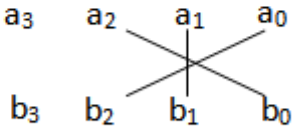
Step1



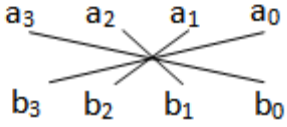
Step2:



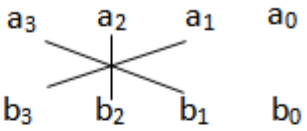
Step3:



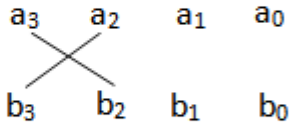
Step4:



Step5:



Step6:



Step7:

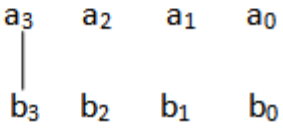


***Fig1: 4** bit Vedic Multiplier method*

In the above step, 4-bit binary numbers $a_3\ a_2\ a_1\ a_0$ and $b_3\ b_2\ b_1\ b_0$ are considered. The result obtained is stored in $p_0\ p_1\ p_2\ p_3\ p_4\ p_5\ p_6\ p_7$ .In the first step a_0 and b_0 is multiplied and the result obtained is stored in p_0. Similarly, in second step $[a_0, b_1]$ and $[a_1,b_0]$ are multiplied using a full adder and the sum is stored in $p_1$and carry is transferred to next step. Likewise, the process continues till we get the result.

VEDIC MULTIPLIER USING CARRY SAVE AND VERTICAL ADDER

In these architectures first partial products are obtained by 2x2 multipliers and then these partial products are added to obtain the result. The additions are performed using two different adders carry save adder [5] and vertical adder and area (in terms of LUTs) and delay is obtained.

Vedic Multiplier For 4x4 Bit using Carry Save Adder:

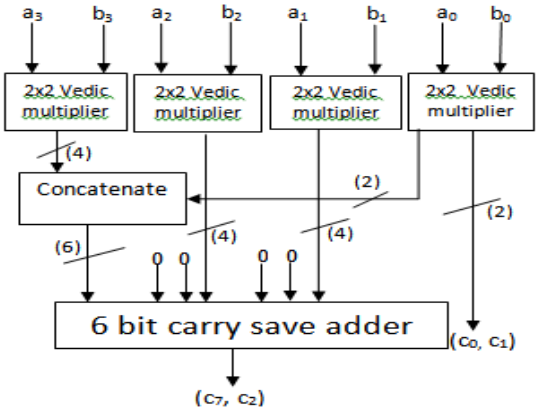


Fig 2: *Vedic Multiplier for 4x4 Bit using single CarrySave Adder*

In this 4x4 Vedic multiplier using carry save the partial product are first computed using 2x2 vedic multiplier and last two bits of the LSB product is directly given to the output as c_0 and c_1 bits the remaing two bits of the LSB partial product is then concatenate with the MSB partial product and this is first six bit input to carry save adder and the remaining 2 input with zero padding is applied to carry save adder [6]. First of all it will perform addition without taking care of carry and the result which is obtained is stored in a six bit register and then it is added with carry and final answer is obtained. The advantage of this adder is that at a time we add3 inputs which is not the case in ripple carry and carry look ahead adder [7].

Table1: *Design summary of 4 bit multiplier using carry save adder*

Slice Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	20	82,000	1%
Number used as logic	20	82,000	1%
Number using O6 output only	13		
Average Fanout of Non-Clock Nets	3.23		

```
Delay:              2.500ns (Levels of Logic = 6)
  Source:           a<0> (PAD)
  Destination:      p<5> (PAD)

  Data Path: a<0> to p<5>
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             10   0.000   0.498  a_0_IBUF (a_0_IBUF)
     LUT4:I0->O             2   0.043   0.554  r1/z<3>1 (q0<3>)
     LUT6:I0->O             2   0.043   0.554  aw/FA2/Cout1 (aw/X<1>)
     LUT6:I0->O             4   0.043   0.442  aw/FA8/Cout1 (aw/C2)
     LUT3:I0->O             1   0.043   0.279  aw/FA9/Mxor_S_xo<0>1 (p_5_OBUF)
     OBUF:I->O                  0.000          p_5_OBUF (p<5>)
    ----------------------------------------
    Total                       2.500ns (0.172ns logic, 2.328ns route)
                                        (6.9% logic, 93.1% route)
```

Fig3: *Total combinational delay*

b)Vedic Multiplier For 4x4 Bit Using 4input Vertical Adder:

In this architecture we have used 4 input adders in which it adds 4 bit at a time and gives two bit carry and 1 bit sum. First partial products are obtained using 2x2 Vedic multiplier, the partial product obtained from LSB 2x2multiplier whose output is Q0(3:0). Then its two lsb bits {Q0[1:0]} is directly equal to output last two ls b bits which is p[1:0], the remaining bits Q0(3:2) gets added with Q1(1:0) , Q2(1:0) and carry then Q3(1:0) gets added with Q1(3:2) , Q2(3:2) and carry and atlast Q3(3:2) gets added with carry.

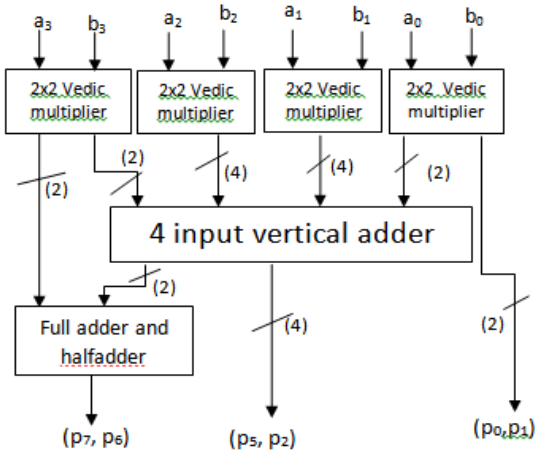


Fig 4: *4 bit Vedic multiplier using vertical adders.*

Table 2: *Design summary of 4 bit Vedic multiplier using verical adders.*

Slice Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	15	82,000	1%
Number used as logic	15	82,000	1%
Number using O6 output only	7		
Average Fanout of Non-Clock Nets	2.74		

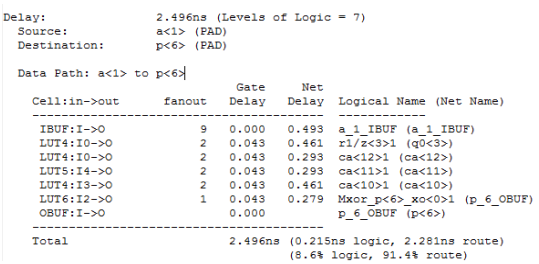


Fig5: *Total combinational delay*

Table 3: *Comparison of carry save and vertical adder.*

Properties	4x4 Vedic Multiplier Using Carry save adder	4x4 Vedic Multiplier Using verical adders
Delay	2.5ns	2.496ns
LUTs	20	15

CONCLUSION

Area and delay are the two measure parameter of any design in VLSI for efficient operation area and delay must be less. In this paper we have design 4x4 vedic multiplier using carry save and vertical adder.

In carry save adder addition is performed in two stages in stage one all the bits are added without taking care of the carry and in next stage the carry which is generated is get added with the sum obtain in stage 1. While in vertical adder all the bits are added simultaneously and respective two bit carry is generated and 1 bit sum is generated.

Since, the operation is performed in single stage LUTs are required much less and also delay is less as compare to carry save adder.

FUTURE SCOPE

Multiplication is key operation in signal processing application so it very crutial that multiplication operation should be performed in no time. In this paper we have design a 4x4 multiplier that has less area and delay than conventional design which can be used in number of application in DSP processor like basic building block for higher order multiplication, in convolution and correlation operation and in dft operation. And it can also be used in complex multiplication.

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