MAT JOURNALS
Journal of VLSI Design and Signal Processing
Volume 2 Issue 1

On-Chip Structure for Timing Uncertainity Measurement Induced by Noise in Integrated Circuits

J. Jagan Pradee, Praveen P N
Department of ECE, SSM College of Engineering, Erode, Tamil Nadu, India
E-mail: 4p.praveen@gmail.com

Abstract

Noise such as voltage drop and temperature in integrated circuits can cause significant performance variation and even functional failure in lower technology nodes. In this paper, we propose an on-chip structure that measures the timing uncertainty induced by noise during functional and test operations. The proposed on-chip structure facilitates the speed characterization under various workloads and test conditions. The basic structure is highly scalable and can be tailored for various applications such as silicon validation, monitoring operation condition and validating logic built-in-self-test conditions. Simulation results show that it offers very high measurement resolution in a highly efficient manner.

Keywords: *Noise, voltage, temperature, measurement, resolution*

INTRODUCTION

During the past, technology scaling has greatly improved performance and circuit integration density. Integrated circuits (ICs) performance has, however, become less predictable by simulations at design stage because of process and environmental (temperature, crosstalk and supply voltage noise) variations. Actual circuit timing on silicon was prone to have larger variation and less predictability from design stage [1, 2]. Therefore, performance limiters, such as noise in the circuit, need to be identified as early as possible during first silicon test and debug and when performing speed characterization. Power supply noise (PSN) and temperature's impact on functional operation of the chip as well as test was extensively investigated in the past several years. Power consumption and voltage drop during test is significantly higher than that of functional mode mainly because of the excessive switching

generated in the circuit by scan patterns. The excessive switching may due to the transitions from zero to one and viz. also it causes the temperature rise, which resulted in hot spots in the chip impacting circuit reliability. PSN and temperature shows both local and global effects on circuit timing, it can cause several impacts.

A chip will have so many layouts each consists of different path resistance. Higher path resistance cause temporary malfunction to the circuit. The amount of noise induced into the circuit is dependent on many parameters including test patterns, test environment and the system in which the chip is operating. In addition, customer test environment and production test environment can very well be different when measuring the noise. In addition, the excessive noise could result in miss-binning of the chip under test. Supply voltage noise induced by: 1) circuit switching during both functional and test modes (IR-drop) and 2) package lead (Ldi/dt) cannot be easily measured by external equipments [3–5]. The parasitics introduced by the equipments make them also unreliable to precisely measure circuit timing in presence of the noise and variations.

On-chip measurement architectures gained significant attention in recent years and to be embedded in the chip for rapid first silicon test, debug, speed characterization, timing margining, IR-drop and temperature measurement and wear-out mechanism analysis, for which all cause timing uncertainty in the device under test. This is possible mainly because of the much smaller/no parasitics, low cost and the high accuracy that the on-chip test and characterization architectures provide. Such architectures can help to record the operation condition in the test mode as well as in the field and help to perform post-silicon calibration. For instance, proposed matter SKITTER, an on-chip measurement circuit, to measure timing uncertainty from combined sources in the circuit. Although, very effective in capturing the noise effects, it requires large area overhead. The on-chip droop detector system designed in enabled voltage transient detection as well as a capability to induce voltage transients in a controlled manner to test and debug IC. The architecture was capable of measuring low-frequency noise very accurately in the circuit, however, it will not be able to measure high frequency voltage noise as effectively, e.g., during launch-to-capture cycle in delay test schemes [6, 7].

In this, we proposed a low-cost and light-weight on-chip structure called supply noise-and temperature-aware timing measurement instrument (TSUNAMI), considering combined effect of supply noise and temperature on clock and on a reconfigurable delay line to accurately measure the induced timing uncertainty even under process variations. TSUNAMI requires very low area overhead but provides high resolution and sensitivity to voltage noise, especially as technology scales.

The structure of TSUNAMI consists of two major parts namely: 1) a noise capture (NC) sensor that is based on a reconfigurable delay line (RDL) to capture various noise effects (supply noise, temperature, clock skew and clock jitter) and 2) a control vector (CV) unit that configures the NC sensor and controls the measurement process. Both require negligible area on the chip. TSUNAMI can operate in different applications/modes for various purposes. In functional mode, it can measure timing uncertainty: 1) during every clock cycle of interest and 2) within a particular clock cycle when applying the functional workload. The change in the timing information of the PSN sensor can be converted to the actual noise (e.g., power supply noise) information [8–10]. This is helpful for silicon validation and can be employed to monitor the operating condition of the chip in the field. In test mode, TSUNAMI can help to measure voltage noise during scan and launch-to-capture cycle as well as during logic built-in-self-test (LBIST).Various analyses can then be performed according to the noise level measured by TSUNAMI.

The original sensor design was very area efficient when compared with existing solutions. It, however, leads to longer measurement time, as it requires multiple measurements on different C values. The first version of the sensor worked fine for silicon validation, but may be undesirable for other applications such as validating LBIST conditions or continuous monitoring noise in the field. One of the unique advantages of this sensor is its flexibility and scalability, as it is designed based on the RDL. With some modifications, the sensor can be applied to different applications that have different requirements on tradeoffs among measurement resolution, measurement time and area overhead. Therefore, we believe it is valuable to discuss the tradeoffs in different applications and how

TSUNAMI PSN sensor can adapt to them in this paper. This paper has the following additional contributions over previous paper: 1) various applications that TSUNAMI can target are discussed in details; 2) variant TSUNAMI structures specifically tailored for these applications are developed; 3) problem modeling and design flow considering a wide range of design choices that TSUNAMI offer are now included; and 4) new simulation results are presented to evaluate the variant TSUNAMI sensor and efficiency of the proposed structures are shown [11, 12].

TSUNAMI ARCHITECTURE

Today's modern designs include very large power distribution network. The voltage noise distribution in the design is not uniform as different blocks in the chip switch differently. Therefore, to take a snapshot of the noise distribution in the circuit, we need to insert sensors and measure the noise at various locations of interest under different workloads and test conditions. For instance, one area of interest for sensor insertion is near critical paths. The information can then be analyzed for characterization during post-silicon test, debug, and calibration. The architecture of TSUNAMI, shown in Figure 1, consists of PSN sensors, which are distributed across the layout to capture the noise at different locations and a CV unit, which controls all the sensors.

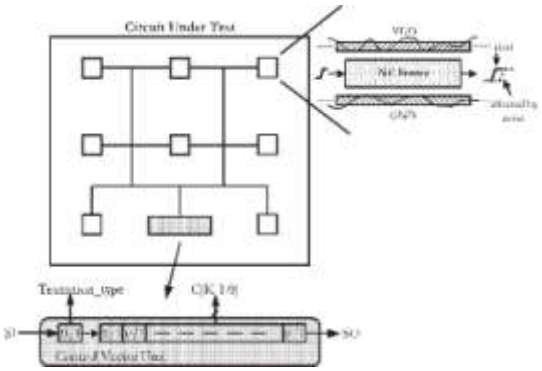

Fig. 1: *TSUNAMI Architecture.*

Transitions are generated at the input of the PSN sensor and propagated through its components. The arrival time and slew of the transitions are affected by the noise on the power/ground lines generated by circuit switching, temperature, clock skew and clock jitter. The PSN sensor is designed to be sensitive to the noise. For the sensor to capture the noise it is preferred to be designed as a single macro and placed between power and ground lines in a standard cell design style. The noise on the power/ground lines will impact the transition propagation time (as it impacts gates' delay in the sensor). The impact of noise can, therefore, be observed as an additional delay. Figure 2 shows the structure of the PSN sensor that consists of the following components: (a) a RDL; (b)

a transition generation (TG) cell; and (c) a transition capture (TC) cell.

RECONFIGURABLE DELAY LINE

A RDL is composed of *K* reconfigurable stages in addition to an extra fixed stage of *m* buffers; each reconfigurable stage contains a multiplexer choosing from an input branch with/without buffer, thereby providing different delay values, while the fixed stage is a series of buffers providing an additional delay that increases beyond what the *K* reconfigurable stages provide without introducing an additional reconfigurable stage. Thus, by controlling the select signals *C* [0], *C* [1], . . . , *C* [*K* − 1], the delay of the entire line becomes reconfigurable. Furthermore, delay of the buffer at each stage of RDL is twice the buffer delay in the previous stage. Thus, if each MUX has a delay of t_x and the minimum-sized buffer has a delay of t_b, the minimum and maximum delay that RDL can provide. Different *C* values create different paths between the input (In) and output (Out) of the RDL. When *C* = 00 . . . .00 = 0, the path only includes the MUXes, making it the shortest path. When *C* = "00 . . . .01" = 1, the path, however, goes through the first buffer and the remaining MUXes. Finally, when *C* = "11 . . . .11" = 2^K − 1, the path goes through all buffers and MUXes, making it the longest path. The key is to find the *C* value that allows propagation of a transition from input-to-output of RDL in just one clock cycle in presence of the noise. This *C* value is further analyzed for understanding the amount of the noise incurred by the applied pattern. Even for the same control vector *C*, the total delay varies at different noise levels. When the delay line is always reconfigured to be constant (e.g., one clock cycle), the variance of the control vector *C* is the fluctuation on the power supply, assuming the temperature stays about the same. Hence, the magnitude of power supply noise can be measured and converted to a digital value. The more the noise on the RDL, the lower the speed of the buffers and MUXes in the sensor. Thus, the transition takes more time to go through the RDL resulting in an error, signaling that a smaller *C* value is needed.

The sensor can capture both high-frequency short-duration noise and low-frequency long-duration noise on a cycle-by-cycle basis. Specifically, when transitions are generated every clock cycle and propagated through the delay line, high-frequency noise will be captured at a specific clock cycle when the transition requires a smaller C value to be able to

properly propagate t hrough RDL. The correct *C* value will be measured to identify the high-frequency noise level average over that specific clock cycle. As the power supply noise is usually pattern dependent for given circuit and packaging, the behavior of the noise will repeat when the same pattern is applied again. Therefore, by applying the same pattern several times, the correct *C* value will be identified, which represents the worst case noise magnitude during the time when the circuit is operating under the pattern. If the application requires the measurement time to be fast (as low as one clock cycle, e.g., for measuring power during launch-to-capture cycle in delay test), one of the variant PSN sensors can be employed so that only one run is needed (i.e., the pattern is only applied once and the measurement can be done on any target clock cycle). In very-high speed design, the number of stages in the RDL can be limited, which affects the noise measurement range. One possible solution is to eliminate the fixed delay induced by fixed stage. Another solution is to design the sensor as a multi cycle path, so that it captures, for example, noise magnitude in every two cycles. Using custom designed MUXes with smaller delay would be another alternative.

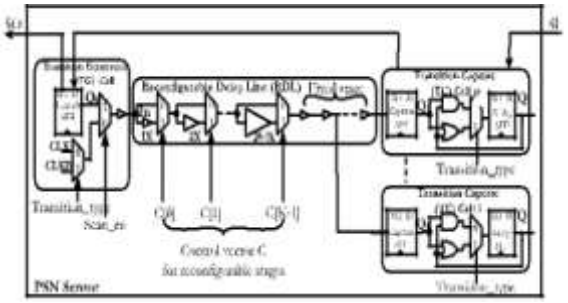

Fig. 2: *Variant NC Sensor Structure for Condition Monitoring and BIST Validation.*

TG CELL

TG cell is inserted at the input of the RDL as shown in Figure 2, which consists of two MUXes and a launch scan flip-flop. Transitions at the input of the RDL are generated depending on the circuit operation mode.

Functional and Scan Modes

In these modes, when a workload or a test pattern is applied, the sensor must be able to measure the delay of the RDL in every clock cycle based on the applied *C* input. Thus, clock signal CLKor the inverted clock CLKB can be fed into the RDL when a series of rise transitions (transition type = 0) or fall transitions (transition type = 1) are needed.

Launch-to-Capture Mode

In this mode, initial values can be shifted during scan mode (Scan_en = 1) to the

launch SFF generating the desired transition at launch cycle. In this mode, only one transition is needed when Scan_en = 0 in either launch-off-capture or launch-off-shift scheme. Figure 2 shows the scan path (SI to SO) going through the FFs in the NC sensor. Shifting certain values into the three scan FFs will ensure the following:

1) generating a rise/fall at TG cell during launch cycle in delay test and 2) 1/0 at the capture SFF and the sticky SFF as the initial value.

TC CELL

TC cell is implemented at the end of the RDL to capture transitions. It consists of two SFFs, namely capture SFF and sticky SFF, and a combinational logic to decide whether any of the transitions is not captured properly. To better understand the process, let us assume the type of transition applied to RDL is rise (Transition_type = 0), as shown in Figure 3.

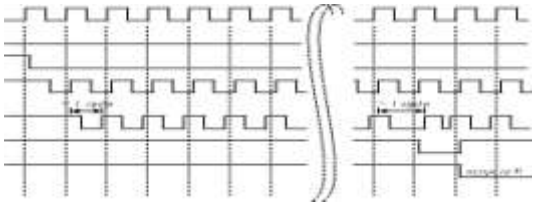

Fig. 3: *Explanatory Waveform Example of Rise Transitions being Generated and Captured.*

It is quite manageable to control the 4-bit *C* value during calibration and measurement. The scan chain is controlled by the external tester. The *C* value is shifted into the scan chain that goes to all sensors. Depending on the design requirement, different *C* values can be applied to each individual sensor for finer control. Then, the workload is applied to the chip and the NC sensors start capturing transitions generated by the TG cells. After the workload application is over, results in terms of whether the transitions are captured at each sensor are shifted out for analysis. If a new round of measurement is needed, a new control vector (*C*) is generated and the same procedure is repeated. The collected data is then analyzed for each sensor to measure the amount of noise that each sensor experiences.

CALIBRATION

The initial values Q_1 and Q_2 at capture SFF and sticky SFF, respectively, are both set to 1 during scan mode. During the measurement, if a rise transition is not captured, Q_1 becomes 0 and so does Q_2 after one cycle. Then, Q_2 at the sticky SFF stays low even if later Q_1 becomes 1 again after a successful capture of rise transition. Later, when Q_2 is shifted out for analysis,

it is certain that there is at least a transition fail to be captured during measurement. In other words, there is a large noise that made the transition so slow that failed to be captured on-time by the TC cell. *C* value is then reduced further to make the path shorter; the pattern application is repeated to see if the sensor fails to capture the transition again under the same test environment. This process continues until the path passes the test. A binary search method can be employed to find the proper *C* value quickly. The *C* value that makes the path passes the test shows that the path is short enough that propagates the transition on time to the TC cell in one clock cycle. That *C* value is the amount of noise that the NC sensor experienced. Without loss of generality, the smaller the *C* value is, the more noise (higher amplitude or longer duration of the power supply noise or higher temperature gradients or both) appear on the PSN sensor. Control vector (CV) unit is the second main component in the TSUNAMI architecture, as shown in Figure 1. CV unit applies *C* values to the PSN sensors. It is flexible: it can be designed to provide one universal C value to all the sensors, or it can be designed to provide different C values to each individual sensor for finer control. The area overhead is extremely small either way. Hereafter, we use *C* value and control vector interchangeably as both show the select signals for the PSN sensors. In the CV unit, control vectors are applied to all PSN sensors from the scan chain, which includes *K* -bit control vector *C* and 1-bit "transition_type."

Calibration is required before the noise measurement to establish a mapping relationship between *C* value and supply voltage. This process begins under no or little background noise condition to identify the *C* value that makes the path delay one clock cycle. To achieve this, a stable V_{dd} must be applied to the sensor. As temperature also plays a role in circuit delay, the calibration process should be performed at fairly similar temperature so that during the noise measurement the impact of temperature on delay can be excluded. This can be achieved by warming up the circuit under test before we actually perform calibration. We also assume there are certain on-chip methods in place to measure temperature to verify that temperature during calibration is indeed close to that during measurement. IR drop because of leakage will make the voltages at sensors different from the external supply voltage. This leakage component is, however, relatively

constant, almost independent of workload and activities of the chip. When comparing the *C* values during the noise measurement and the mapping relationship established during calibration, the sensors capture the dynamic behavior of the noise during functional and test operations.

To analyze the impact of the noise on the sensor, new supply voltage V_{dd} is generated and adjusted at a fine granularity and applied to the entire circuit. Measurements are performed for each selected $V_{dd} = v_i$. The measurement results (i.e., control vectors) serve as calibration values for given V_{dd}. In other words, a mapping relationship between control vector *C* and supply voltage V_{dd} is established.

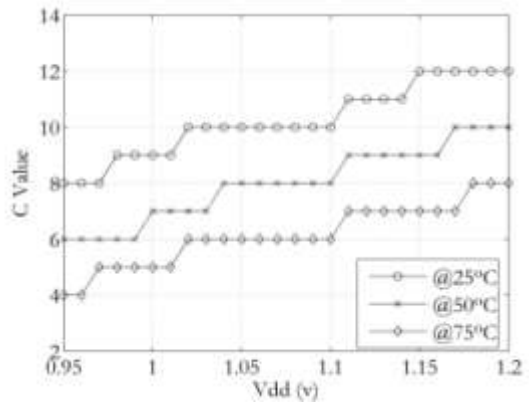

Fig. 4: *Relationship between V_{dd} and Control Vector C Value (Obtained using Rise Transitions).*

USING TSUNAMI IN DIFFERENT APPLICATIONS

Applications

TSUNAMI can operate in different applications/modes for various purposes. Three potential applications that TSUNAMI can target include, but not limited to, are as follows: 1) silicon validation; 2) operating condition monitoring; and 3) validating built-in self test (BIST) conditions.

Silicon Validation

Silicon validation is a necessary process performed after fabrication to examine the functionality and speed of a chip under different operating conditions. Upon a malfunction, silicon validation and debug will identify the root cause of it. Unlike pre-silicon verification where simulation tools provide a full capacity of controllability and observability, silicon validation is extremely difficult. TSUNAMI improves observability of the noise profile and consequent timing uncertainty in the system. Specifically, TSUNAMI can measure timing uncertainty: 1) during every clock cycle of interest; 2) within any particular clock cycle when applying the functional workload; and 3) during scan and launch-to-capture cycle. The timing information

collected by the NC sensor can be converted to the actual noise (e.g., power supply noise) information. Thus, the measurement in both functional mode and test mode can help silicon validation. Various analyses can then be performed according to the noise level measured by the TSUNAMI. For example, during scan and launch-to-capture cycle, the noise level can be used to analyze the impact of *Ldi /dt*. Meanwhile, the reconfigurability of the baseline NC sensor adds controllability to the silicon validation procedure. This makes it applicable to sensors experiencing process variations and different noise distributions at different locations.

Continuous Monitoring of Operation Condition

TSUNAMI with some modifications can be employed to continuously monitor the operation condition of the chip in the field. This is useful because the noise distribution in the system aging effects. Once the operating condition worsens to a level that could potentially cause timing issue or functional failure, TSUNAMI can either warn the user about the situation or, if the period of time as a result of changes in temperature, leakage and this can be quite helpful for critical applications such as can change when the chip is used in the field for an extended automatic, medical, military, and space applications. In this application, TSUNAMI is required to continuously monitor the operation condition as the system operates in functional mode. Therefore, it is not practical to have a back and forth procedure that the baseline TSUNAMI sensor posses.

Validating LBIST Conditions

Another potential application for TSUNAMI is to serve as a part of the BIST procedure to validate the test conditions. This is particularly useful in the case that the operating conditions in the field may be worse than what the chips experience during manufacturing test. Such situation can make diagnosis extremely difficult and the root cause of performance issues becomes puzzling. TSUNAMI can provide a quick validation on the current test condition in the field to see whether it meets certain specification in terms of a combined effect of power supply noise, temperature and clock variations. One such example of using TSUNAMI in BIST is that, if the chip is used in a car, every time when the engine starts, BIST patterns are applied to the chip, and TSUNAMI sensors can tell

whether or not the actual operating condition is worse than what is expected. When that does happen, it shows a potential hazard and can generate an alarm signal (e.g., engine check light). This can help to diagnose various performance issues in the field and improve product yield and safety of individuals. In addition, TSUNAMI can help to reduce the gap between LBIST during manufacturing test and LBIST in the system by reporting the noise profile on the chip. In this application it is only required for TSUNAMI to validate a pass/fail and an accurate measurement of the specific noise level may not be necessary. Similar to continuous monitoring of operation condition, modifications are needed for the sensor to largely reduce measurement time.

CONCLUSION

The proposed TSUNAMI architecture provided a low-cost and light-weight solution to measure timing uncertainty induced by voltage drop and temperature in ICs. TSUNAMI can work at different applications and operation modes. It can be employed for speed characterization during silicon validation, operating condition monitoring in the field and BIST validation for various workloads and test conditions. Simulation results showed that TSUNAMI offered high resolution at low technology nodes at significantly reduced area and power overheads compared with the existing work. Its variant designs offered a wide range of design choices that can be tailored for specific applications and requirements. Our future work includes fabrication of the proposed structure on a test chip, silicon data collection and analysis and sharing the results with the community. In addition, we will also be exploring improvements on resolution. Possible improvements could be replacing the regular buffers with low-Vt buffers or even inverters. Replacing MUXes with tri-state buffers could also improve resolution by allowing more stages of buffers inserted.

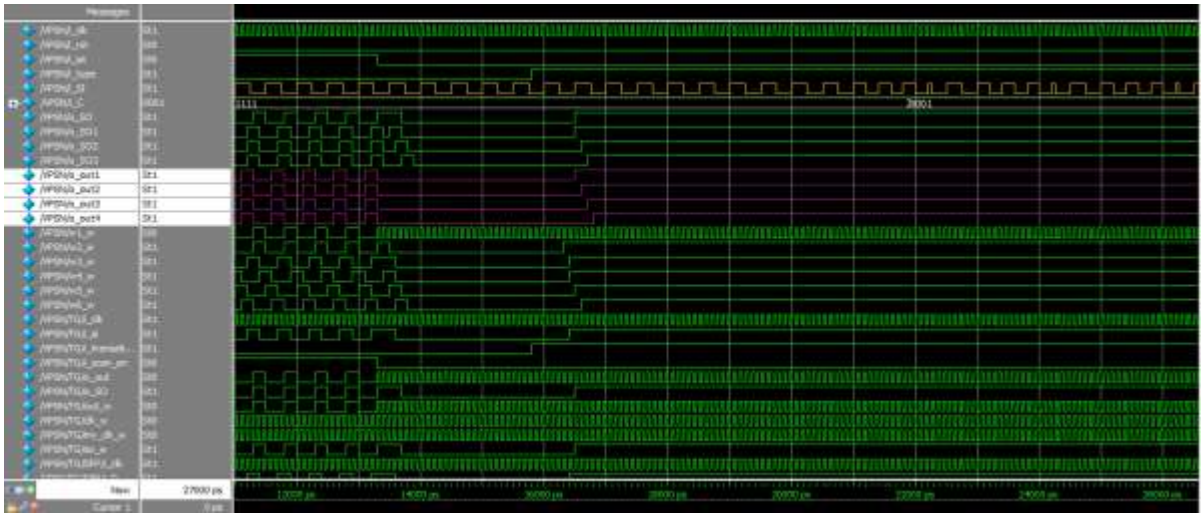

Fig. 5: *Final Output of PSN Sensor*

REFERENCES

1. J. Saxena, K. M. Butler, V. B. Jayaram, S. Kundu. Case study of IR-drop in structured at-speed testing. *In Proc. Int. Test Conf*. 2003; 1098–1104P.
2. J. Choi, M. Swaminathan, N. Do, R. Master. Modeling of power supply noise in large chips using the circuit-based finite-difference time-domain method. *IEEE Trans. Electromagn. Compat.* 2005; 47(3): 424–439p.
3. Y. Sasaki, K. Yoshikawa, M. Nagata, K. Ichikawa. Co-evaluation of power supply noise of CMOS microprocessor using on-board magnetic probing and on-chip waveform capturing techniques. *In Proc. IEEE Int. Meeting Future Electron Devices*. 2012; 1–2p.
4. S. K. Rao, C. Sathyanarayana, A. Kallianpur, R. Robucci. Estimating power supply noise and its impact on path delay. *In Proc. IEEE VLSI Test Symp*. 2012; 276–281p.
5. H. Xu, V. F. Pavlidis, W. Burleson, G. De Micheli. The combined effect of process variations and power supply noise on clock skew and jitter. *In Proc. Int. Symp. Qual. Electron. Design*. 2012; 320–327p.
6. M. Tehranipoor, K. Butler. Power supply noise: A survey on effects and research. *IEEE Design Test*. 2010; 27(2): 51–67p. Apr. 2010.
7. Z. Abuhamdeh, B. Hannagan, J. Remmers, A. L. Crouch. A production IR-drop screen on a chip. *IEEE Design Test*. 2007; 24(3): 216–224p.
8. J. Wang, D. M. Walker, X. Lu, A. Majhi. Modeling power supply noise in delay testing. *IEEE Design Test*. 2007; 24(3): 226–234p.

9. P. Pant, J. Zelman. Understanding power supply droop during at-speed scan testing. *In Proc. IEEE VLSI Test Symp;* 2009.
10. K. Arabi, R. Saleh, M. Xiongfei. Power supply noise in SOCs: Metrics, management, and measurement. *IEEE Design Test*. 24.
11. R. Franch, P. Restle, N. James, W. Huott. On-chip timing uncer-tainty measurements on IBM microprocessors. *In Proc. Int. Test Conf*. 2007; 1–7p.
12. R. Petersen, P. Pant, P. Lopez, A. Barton. Voltage transient detection and induction for debug and test. *In Proc. Int. Test Conf*. 2009; 1–10p.

J. Jagan Pradeep is currently working as Associate Professor In SSM College of Engineering, Anna university, TamilNadu,India. He has completed B.E, M.Tech and PhD from Anna University.

E-mail: jgnprdp@gmail.com

Praveen P N, received the B.E degree in Electronics and Instrumentation from Anna University, Tamil Nadu, India in 2006 and doing M.E in Anna University 2013-2015 batch, in SSM college of engineering, Tamil Nadu, India.

E-mail: 4p.praveen@gmail.com