MAT JOURNALS
e-ISSN: 2581-8449
Volume 5 Issue 2

Design of an Efficient Multiplier Using Transistor Level Modified Adders

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DOI: *http://doi.org/10.5281/zenodo.2837838*

Abstract

The endless improvement of modern mobile, compact devices and applications has caused an enormous effect for ultralow power circuit design. Various methods and techniques have been applied successfully to the power, performance region of the design spectrum for lower power consumption. In some applications wherever ultralow power consumption is that the primary requirement and performance is of secondary importance, a more aggressive approach is secure. The new applications mainly depend on the transistor count of circuit with longer economical battery life. The minimum energy point is obtained as an ultralow-power 0.15 V. At this minimal energy point, an ultralow-power 10T 1-bit full adder circuit at sub threshold region and it can be used for energy refrainment applications. It exhibits imperious performance in terms of design standards like average power, propagation delay and transistor count at optimal supply voltage i.e., at 0.15 V. The proposed design uses the 10T 1-bit full adder using 4-bit multiplier compared to conventional 1-bit full adder using 4-bit multiplier circuit. The performance metrics like propagation delay, average power, transistor count are reduced compared to conventional method. The designed 4-bit multiplier is simulated using Tanner tool.

Keywords: *Full adder, hall adder, propagation delay, transistor count, ultra low power*

INTRODUCTION

An adder is a digital circuit that is used to performaddition operation. This adder is widely used in the arithmetic logic unit or ALU of a computer and other types of processors. There are two types of adders are available such asHall Adder and Full Adder.

Half Adder

The half adder consist of XOR gate and AND gate and their input variables are represented as A and B.

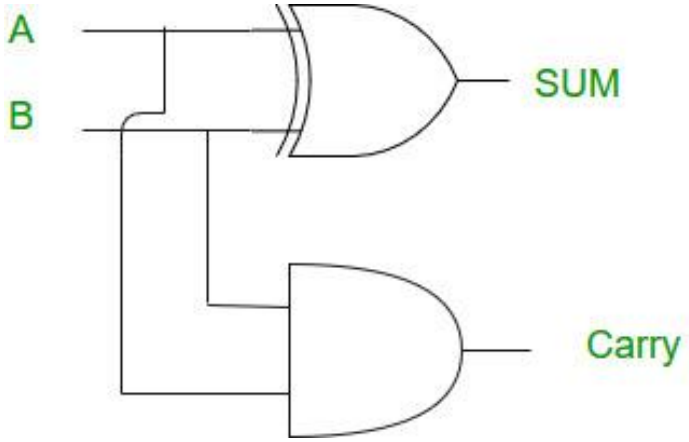


Figure 1: *Logic diagram of half adder.*

The output variables are represented as S and C. The carry signal portraysacascaded output to the next digitof a multi-digit addition.

The simplest half-adder design, pictured above, incorporates an XOR gate for Sum and an AND gate for Carry. The Boolean logic for the sum will be A'B+AB' whereas for carry will be AB shown in Fig. 1.

Full Adder

The three 1 bit numbers can be added using a 1 bit full adder and they are denoted as A, B and C_{in}. Where, A and B are the operands, and C_{in} produce sum and carry as output and it is carried from thepreviouslesssignificant stage. The full adders are usually used to add the cascaded adders. They are commonly used to add the binary numbers of following bits 8, 16, 32, 64 etc.

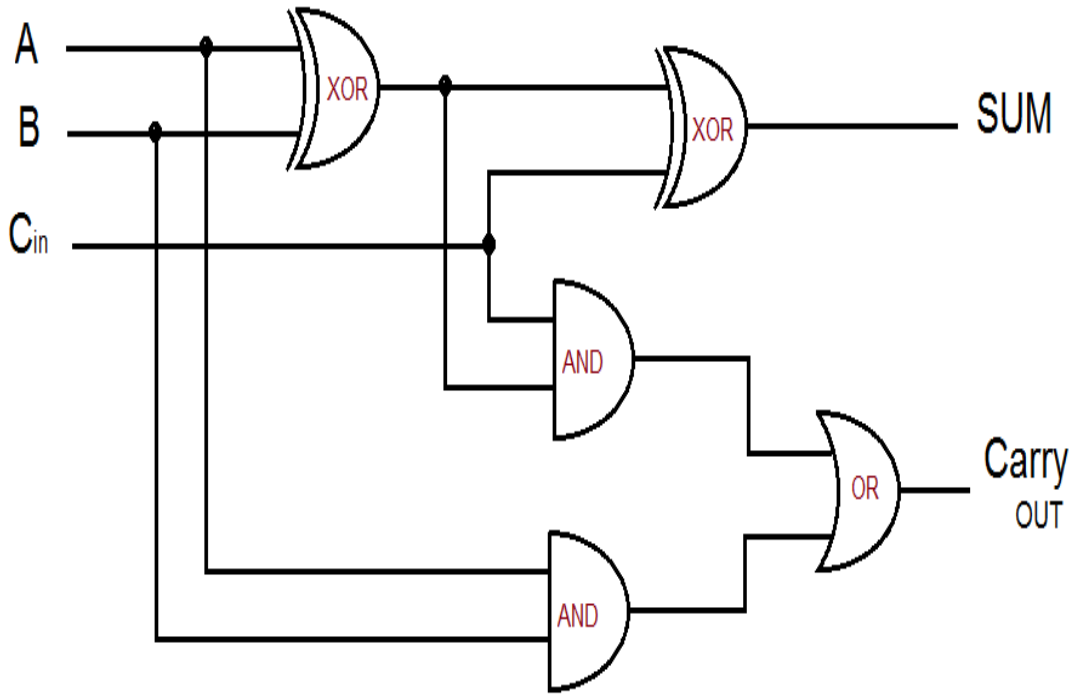


Figure 2: *Logic diagram of full adder.*

The circuit produces a two bit output. Output carry and sum typically represented by the signals C_{out} and S is shown in Fig. 2, where in decimal system. The carry output is obtained by using extra one OR gate. The full adder is constructed ny usingtwo half adders.

Multiplier

Multipliers play a major role in the digital and signal processing methods.The basic multipliers includes the gates such as AND gate, full adders and half adders. The multipliers are designed by using the method of low power consumption, high speed and less area. Multipliers are used in various implementations in VLSI design process. The multiplier has different methods such as binary multiplication, iterative multiplication, parallel and serial multiplications.

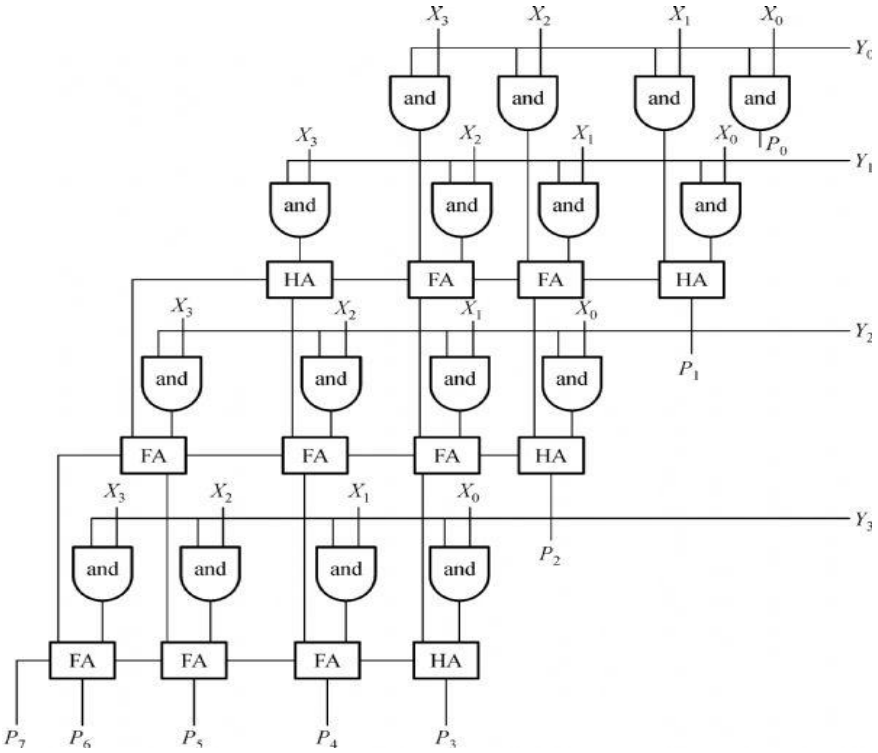


Figure 3: *Structure of 4-bit multiplier.*

The basic structure of 4–bit binary multiplier is shown in Fig. 3. The above structure contains the main components of half adder, full adder and AND gate.

EXISTING METHOD–NORMAL FULL ADDER

In this implement, without change the resulting logic the terminal OR gate before the carryout output may be retrieved by an XOR gate. There are two methods to design a normal full adder and they are designed by using the transistors and another method is designed by using the gates.

Using particular two types of gates is beneficial if the circuit is being executed using simple IC chips that contain particular gate type per chip.

The normal full adder circuit it has 14 PMOS and 14 NMOS to provide 1 bit full adder output.

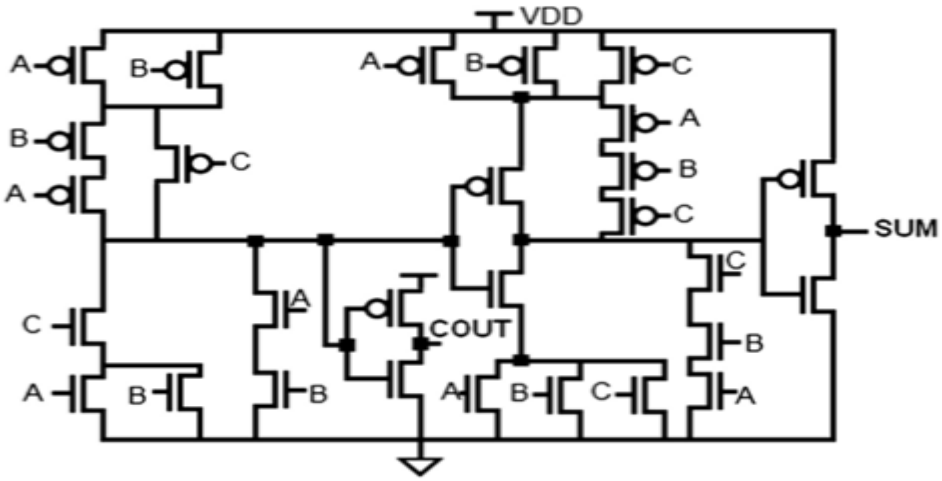


Figure 4: *Circuit diagram of normal full adder.*

The circuit diagram of the normal full adder is shown in Fig. 3. Which contains 28T (transistors) to provide 1-bit full adder output. The above circuit is implemented in 4 - bit multiplier and the parameters such as propagation delay, transistor count, and the power are analysed in exciting method.

PROPOSED METHOD–10T FULL ADDER

To reduce propagation delay, transistor count, and the power of normal full adder using 4–bit multiplier is replaced with the 10T (transistor) full adder [21] using 4-bit multiplier.

The adder which contains only 10 transistors to provide 1 - bit full adder output is shown inFig. 4. It contains 5 PMOSFET and 5 NMOSFET.

This circuit consists of two blocks. They are sum block and the other one is carry block. The circuit is designed using two XOR gates [2] and one multiplexer. Sum block is implemented using two XOR gates. Two inputs A and B are applied to this gate and A⊕ B is the output that is obtained.

The multiplier is designed by implementing the adder in the 4-bit multiplier. It is used to design the multiplier, subtract, integrator and differentiator. In order to perform the arithmetic operation, the one bit full adder cell is used and the outcome of them are equal to the one bit full adder cells.

This output is given as input to the second XOR gate with four MOSFETs with different input C. This XOR gate produces A⊕ B ⊕ C as output which is the output of Sum block (SUM). Carry block consists of selector circuit that consists of 2 MOSFETs.

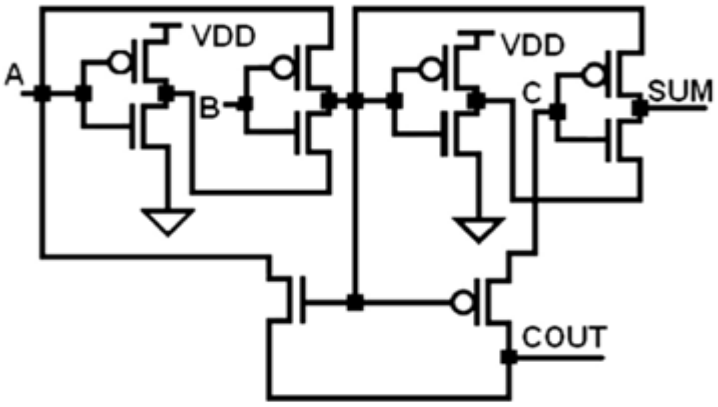


Figure 5: *Circuit diagram of 10T full adder.*

The output of first XOR gate is the selection line of this carry block, which means that the carry block output depends on 'A⊕ B'.The output of carry block is 'A' if 'A ⊕ B' = '0'. Then the COUT is 'C' if 'A ⊕ B' = '1'.

Operation of Multiplier

Multiplication is one among the fundamental operation. The other operations are addition, subtraction and division. The addition of the whole number repeatedly is termed as multiplication. Addition of different numbers is equal to the multiplication of two numbers. The multiplier factor can be written first and multiplicand second. For example, 13 multiplied by 11 can be calculated by adding 3 copies of 4 together. Here, 13 and 11 are the factors and 143 is the product is shown in Fig. 5.

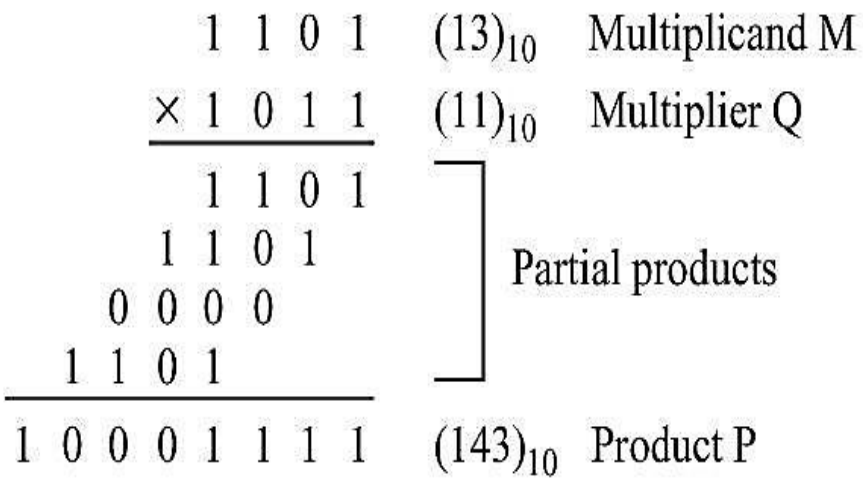


Figure 6: *Example of multiplication.*

The main property of this method is commutative property. It provides the output of 4 inputs by taking the 3 inputs and also provides the equal value of adding the 3 inputs. So, it will not affect the result of the multiplication by using addition. This primary method provides the multiplication of real numbers, integersand rational numbers (Figure 6).

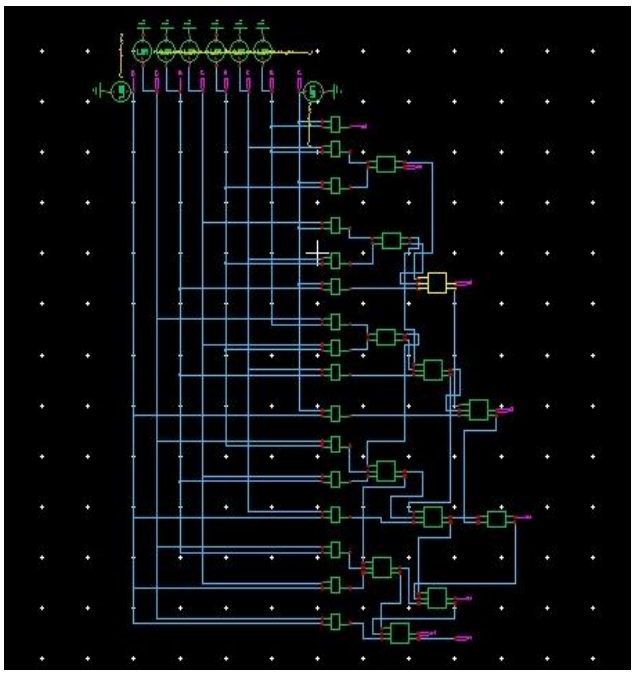


Figure 7: *Schematic of 4-bit multiplier.*

The symbols are created for half adder, full adder, AND gate and these symbols are designed as proposed 4 bit multiplier circuit (Figure 7).The binary multiplier of combinational logic circuits are used to perform the multiplication by two binary numbers in digital system. This method is frequently used method for various applications in order to implement the different algorithms in DSP.

Commercial applications like computers, mobiles, high speed calculators and a few general purpose processors needs binary

multipliers. Compared with addition and subtraction, multiplication could be an advanced method.In multiplication process, the number which is multiplied by the other number is said to be multiplicand and the number multiplied is called as multiplier.

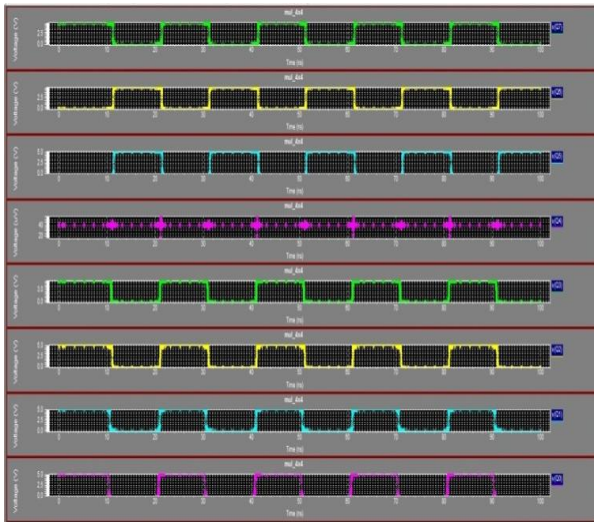


Figure 8: *Waveform of 4-bit multiplier.*

It contains inputs as A_0 to A_4, B_0 to B_4 and the output obtained as Q_0 to Q_7 is shown in Fig.8. The output waveform of 4-bit multiplier. The first cycle shows multiplied 3x3 value and the second cycle shows multiplied 6x6 value. The output it generates as binary form (0's and 1's).

SIMULATION RESULTS

Propagation delay, average power and transistor count of the proposed 10T full adder using 4-bit multiplier discussed.

Propagation Delay

Propagation delay is the amount of time it takes for the top of the signal to travel from the sender to the receiver. It can be computed as the ratio between the link length and therefore, the propagation speed over the specific medium. Propagation delay is same asd/s where, 'd' is a distance and 's' is a wave propagation speed.

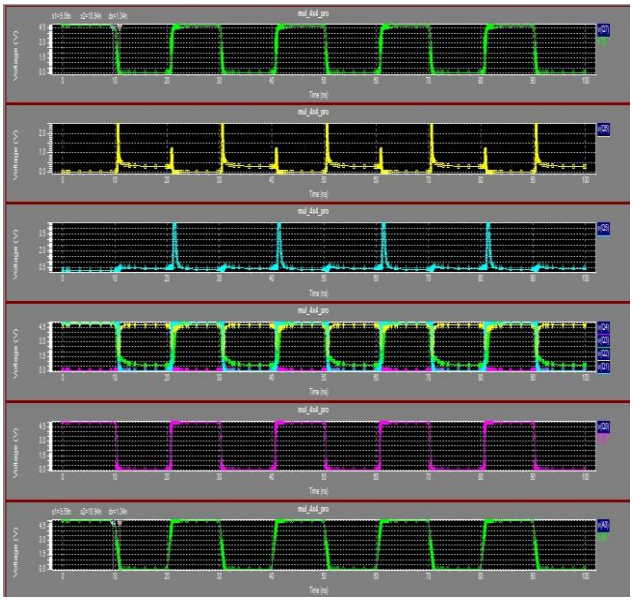


Figure 9: *Delay of proposed circuit.*

A full adder has an overall gate delay of threelogic gates from the inputs A and B to the carry output Cout. Fig. 9 shows delay for the proposed 4-bit multiplier circuit. It consumes 1.34ns time, which is 28% lesser than that of the existing 4-bit multiplier circuit due to the reduction of area and transistor count.

To process data at a faster rate and improve overall performance the gate delays in digital circuits are reducing. The determination of the propagation delay of a connected circuit requires determine thelongest path of propagation delays from input to output and by casting each t_{pd} time on this path. The results of race conditions due to theinequality in propagation delays of logic elements is the major contributor to glitches in the asynchronous circuits. For every 15cm of wires length contains an approximatepropagation delay of 1ns. The propagation delay of the logic gates are ranges from 10nano second to Pico second depends upon the technology used.

Average Power

The average power is that the average amount of work done or Energy transferred per unit time.

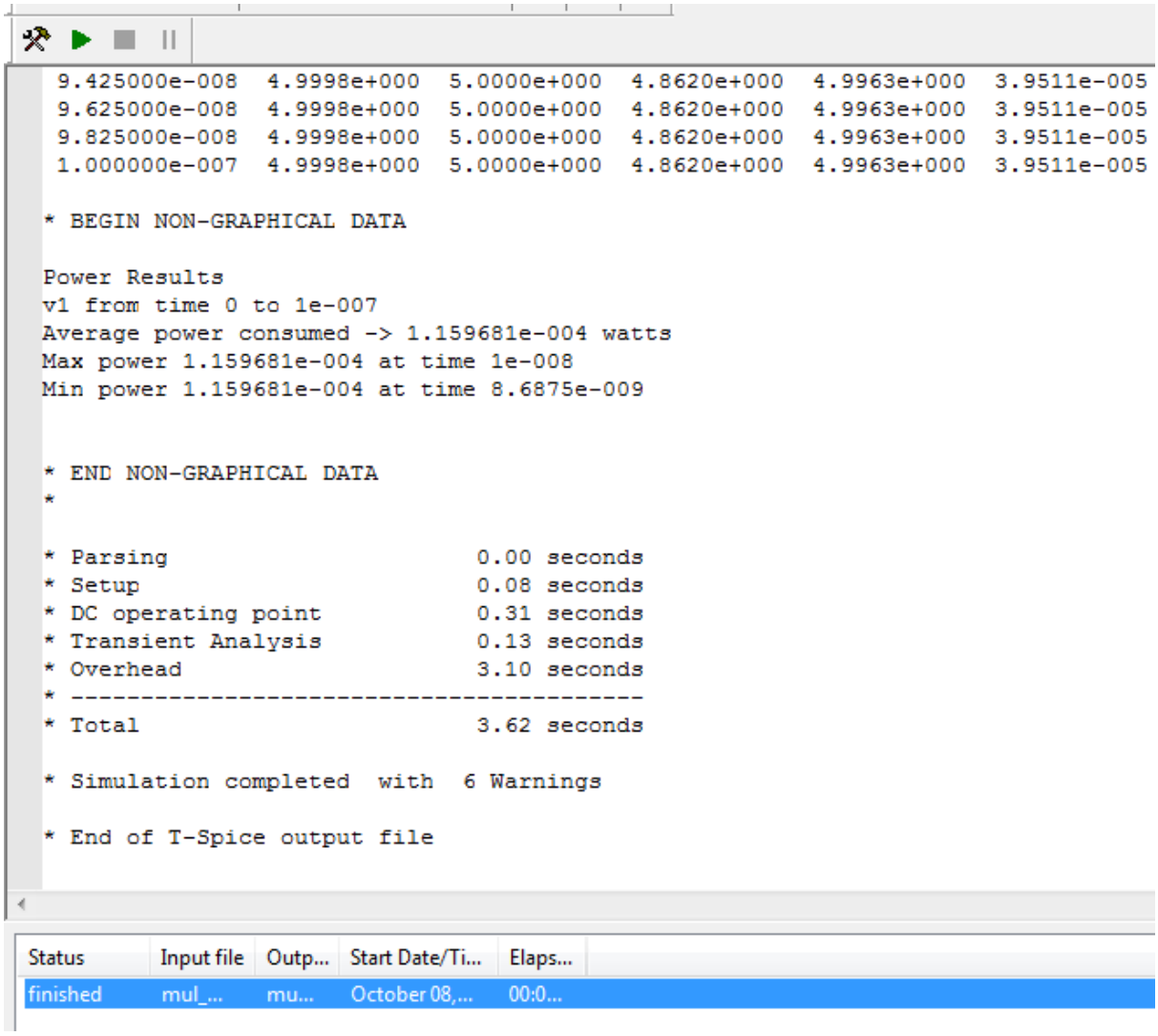


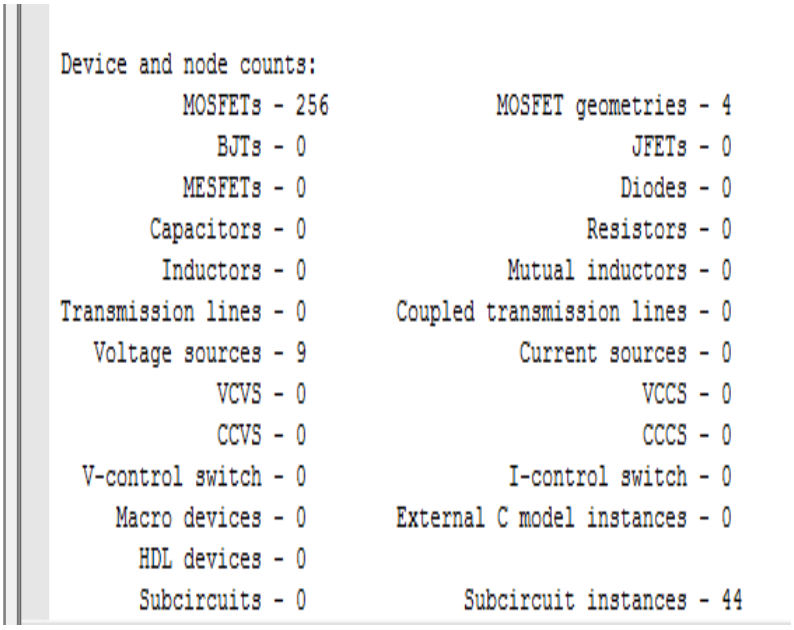
Figure 10: *Power consumption of proposed circuit.*

The above Fig. 10 shows power for the proposed 4–bit multiplier circuit. It consumes 115.9 mW, which is 30% lesser than that of the existing 4-bit multiplier

circuit. The DC operating point is 0.31s and the transient analysis of the circuit is 0.13s. Here, the power is reduced because it uses 10T using 1-bit full adder.

Transistor Count

The transistor count denotes the number of transistors which is used in exciting and proposed 4–bit multiplier.



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Device and node counts:
          MOSFETs - 256          MOSFET geometries - 4
             BJTs - 0                    JFETs - 0
          MESFETs - 0                 Diodes - 0
       Capacitors - 0               Resistors - 0
        Inductors - 0            Mutual inductors - 0
Transmission lines - 0   Coupled transmission lines - 0
   Voltage sources - 9           Current sources - 0
             VCVS - 0                    VCCS - 0
             CCVS - 0                    CCCS - 0
  V-control switch - 0           I-control switch - 0
    Macro devices - 0   External C model instances - 0
      HDL devices - 0
       Subcircuits - 0        Subcircuit instances - 44
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Figure 11: *Transistor count of proposed circuit.*

According to the transistor count the power, area and propagation delay of the circuit varies. The above Fig.11 shows thetransistor count of proposed 4 - bit multiplier circuit. It utilize 256 transistors for their multiplication function, which is 46% lesser than that of existing 4-bit multiplier circuit. The subcircuit instances used in the circuit is 44 and the 4 MOSFET geometrics are used.

Comparing with normal full adder using 4-bit multiplier and 10T full adder using 4 – bit multiplier, by using tanner tool.

Table 1: *Comparison analysis.*

S.NO	CONTENT	POWER (mW)	DELAY (ns)	TRANSISTOR COUNT
1.	EXISTING METHOD	169.6	1.85	400
2.	PROPOSED METHOD	115.9	1.34	256

CONCLUSION

Low power, delay and transistor count, where the primary concerns for better multiplier design. The 10T full adder was implemented on proposed 4-bit multiplier in order to reduce transistor count, delay and power. The proposed 4-bit multiplier cell achieved delay of 1.34ns and power consumption of 115.9 mW with the transistor count of 256. While, the basic full adder cell had delay of 1.85ns and power consumption of 169.6 mW with the transistor count of400.

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Cite this article as: *S. Kaviya, & D. Kumar. (2019). Design of an Efficient Multiplier Using Transistor Level Modified Adders. Journal of VLSI Design and Signal Processing, 5(2), 17–27. http://doi.org/10.5281/zenodo.2837838*