MAT JOURNALS
Journal of VLSI Design and Signal Processing
e-ISSN: 2581-8449
Volume 5 Issue 1

Design of Low Power TPG for BIST Using Reconfigurable Johnson Counter

M. Nandini Priya[1*], R. Vivitadurga[1], U. Priya[1]
[1]Assistant Professor, Department of Electronics and Communication Engineering, Bannari Amman Institute of Technology, Sathyamangalam, Tamil Nadu, India
***Email:** nandinipriya@bitsathy.ac.in*
***DOI:** http://doi.org/10.5281/zenodo.2532997*

Abstract
Worked in Self-Test assumes an essential job in testing of VLSI circuits. Test designs created utilizing design generator is utilized to test the Circuit under Test. Regular technique for test design age includes in Reconfigurable Johnson Counter and LFSR which needs in relationship between's progressive test vectors. A Modern Low Power test design is created utilizing Reconfigurable Johnson Counter and Accumulator. A Low Power utilization gadget is basic for battery worked gadgets. The system for delivering the test vectors for BIST is coded utilizing VHDL and reproductions were performed with ModelSim 10.0b.

***Keywords:** Built-in-self-test (BIST), Multiple Single Input Change Vector (MSIC), Test Pattern Generator (TPG).*

INTRODUCTION

Testing a circuit each time before they startup, is called Built in Self-Test (BIST). The design has both test design generator and reaction analyzer on the circuit that will be tried. BIST lessens utilizing costlier ATE and the time required for testing. The Built in Self-Test contains test design generator, circuit under test, reaction analyzer and test controller.

The signal start test is given to test controller, the test patterns are generated using test pattern generator. The generated patterns were applied on circuit that is under test. The response analyzer block compares the response of the circuit with the predicted response. If the response of the circuit matches with the predicted response the pass signal is provided to the test controller else fail signal is provided. The examples can be created utilizing ROM, LFSR, counter. The CUT might be combinational or consecutive circuit. The reaction analyzer can be comparator or a LFSR used as signature analyzer. The patterns were applied to the CUT in two different ways namely serial and parallel BIST. For sending the test vectors inside the CUT and to obtain the response, clock pulse must be applied.

In parallel BIST single clock pulse is sufficient to apply test vectors where as in case of serial BIST, clock had to be applied frequently. Serial test pattern generator is used in test per scan and parallel test pattern generator is used in test per clock. In sequential TPG every single piece is stacked into sweep chain, when the important bits are accomplished the example is connected to CUT as vector. The yield reaction of CUT is stacked again into output chain. In parallel TPG test vectors are connected for individual clock beat.

In Test per filter plot the examples created are examined into output chain as a bit for each clock cycle. When the important test length is accomplished, the vectors from information filter registers are connected to circuit that will be tried. The response of the circuit is latched and stored in output scan register. Once the previous pattern is scanned out, the next pattern is scanned

into input scan register. The short coming of this technique is time required for testing the circuit using test per scan is higher and the need for additional hardware.

The patterns generated are directly applied to the CUT and gets processed within single clock cycle in Test per clock schemes. This method applies the vectors directly on the CUT without the need for scan registers. The output response is obtained in parallel from CUT.

LITERATURE SURVEY

M. Nourani et al., [1] proposed low change LFSR customizable to BIST and in addition check based BIST. Change between progressive bits and progressive examples were decreased to stifle the normal and pinnacle control amid testing process.X. Zhang et al., [2] proposed TPG technique which is energy efficient to attain high fault coverage. Controllability and Observability at the nodes of circuit is calculated that is primarily based on probability of the input signal. Weights at the input are determined using genetic algorithm based search.

To minimize the power requirement smoothing methodology was adopted in [3]. Between LFSR and input of the scan chain, additional multiplexer is added. The size of the multiplexer is chosen according to the degree of smoothing. This methodology was implemented to both parallel BIST and multiple scan chains.

S. Chun et al., [4] proposed the statistical code to skip the unnecessary test sequence during the test operation. The patterns which were incapable of determining faults also contribute power. So occurrence of such patterns were neglected to minimize the power. *Bin zhou et al.,* [5] generated TPG using ring counter. The values corresponding to partial freezing inputs were kept unaltered. This technique minimizes the space required for storing the patterns, average power and total power consumption.

Catch control safe test design assurance [6], depicts about disposing of intensity dangerous examples and to begin with the power safe examples as it were. The test age strategy includes two stages in particular test design refinement and low power test design recovery. Power safe examples are refined to recognize blames and distinguished utilizing power dangerous examples.

Touba &McCluskey proposed fast fault simulation process to determine identifying random patterns for non feedback bridging faults [7]. By adopting this technique single stuck at faults as well as non feedback bridging faults can be identified easily. Touba and McCluskey [8] proposed to determine test point to increase the probability of identifying faults. Insatiable calculation was utilized to distinguish undetected shortcomings. Prior methods embed test point just a single at any given moment. Here at first pseudo arbitrary examples were connected and blame free recreations were performed. The ways are followed by recognizing undetected shortcomings for each example.

Reaz et al., identified the random pattern testable faults using LFSR [9]. The deterministic test patterns were initially stored at ROM. The demerit of this technique is the space required for storing patterns at ROM is higher. In order to reduce the size many compression techniques has been proposed.

ElifAlpaslan et al., [10] proposed a technique to reduce power by minimizing switching activity. Usual techniques insert the logic gates to mask the unnecessary transition but this may in turn adds delay. Hence the design is modified at register

transfer level to achieve optimization. Power sensitive scan cells were replaced with frozen scan cells to minimize the shifting in scan chains.

In hardware partitioning technique [11], hardware is added to the circuit to control and observe the segment's inputs and outputs. So, the circuit is divided into small sub-circuits. Each sub circuit is directly controllable and observable. One way is to use multiplexer partitioning. The disadvantage of adding extra hardware is in the speed decrease and the cost of implementation.

Hafizur Rahaman et.al., proposed a technique to identify multiple stuck open faults[12]. In traditional techniques the patterns were produced as a sequence of test vectors. Based on error behavior test sequence length varies. Hence this approach reduces the time required for testing. Low power test patterns were generated by grouping the test patterns [13]. The generated test set is further reduced by performing ordering from high to low switching activity. The patterns that are incapable of detecting faults have been eliminated from the test set.

N.Ahmed et.al., [14] proposed different low power test design age strategies. When the grouping of test designs was created, LP-TPG embeds middle of the road designs. The requirement for embeddings halfway examples is to enhance the connection among the test designs in this way decreasing the power scattering.

Salvador Manich [15] proposed a technique to adopt reseeding technique to achieve the expected fault coverage. Arithmetic TPG use reseeding technique to achieve the high fault coverage. The time required to store the seed vector is reduced. Binary search is done to speed up the seed selection process.

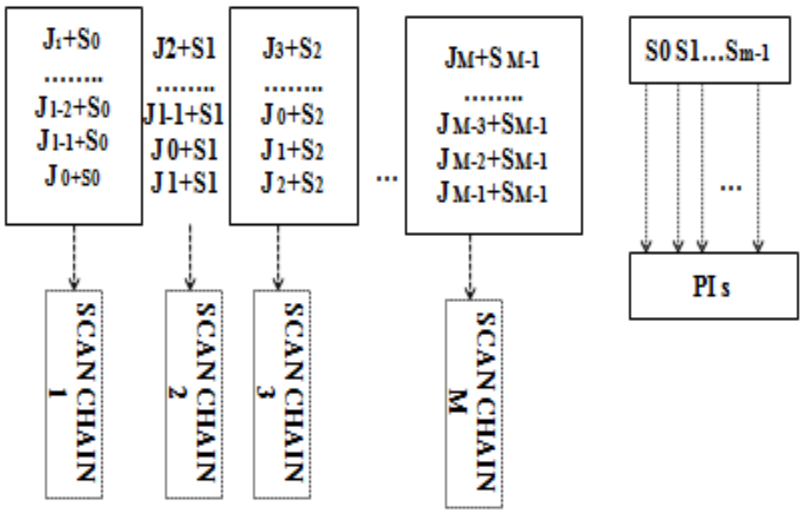

Figure 1:*Symbolic Representation of an MSIC Pattern.*

EXISTING METHODOLOGY

The Existing method produces the test design utilizing Reconfigurable Johnson counter and the seed vector. Test designs were produced by performing Exclusive-or activities between Johnson counter and seed vector.

Test Pattern Generation Method

The test design age engineering contains Reconfigurable Johnson counter and seed vector square. Test designs were produced by performing Exclusive-or tasks between Johnson counter and seed vector. The vectors got were used by the output chain. The produced examples were connected to the sweep chains as shown in the Figure 1.

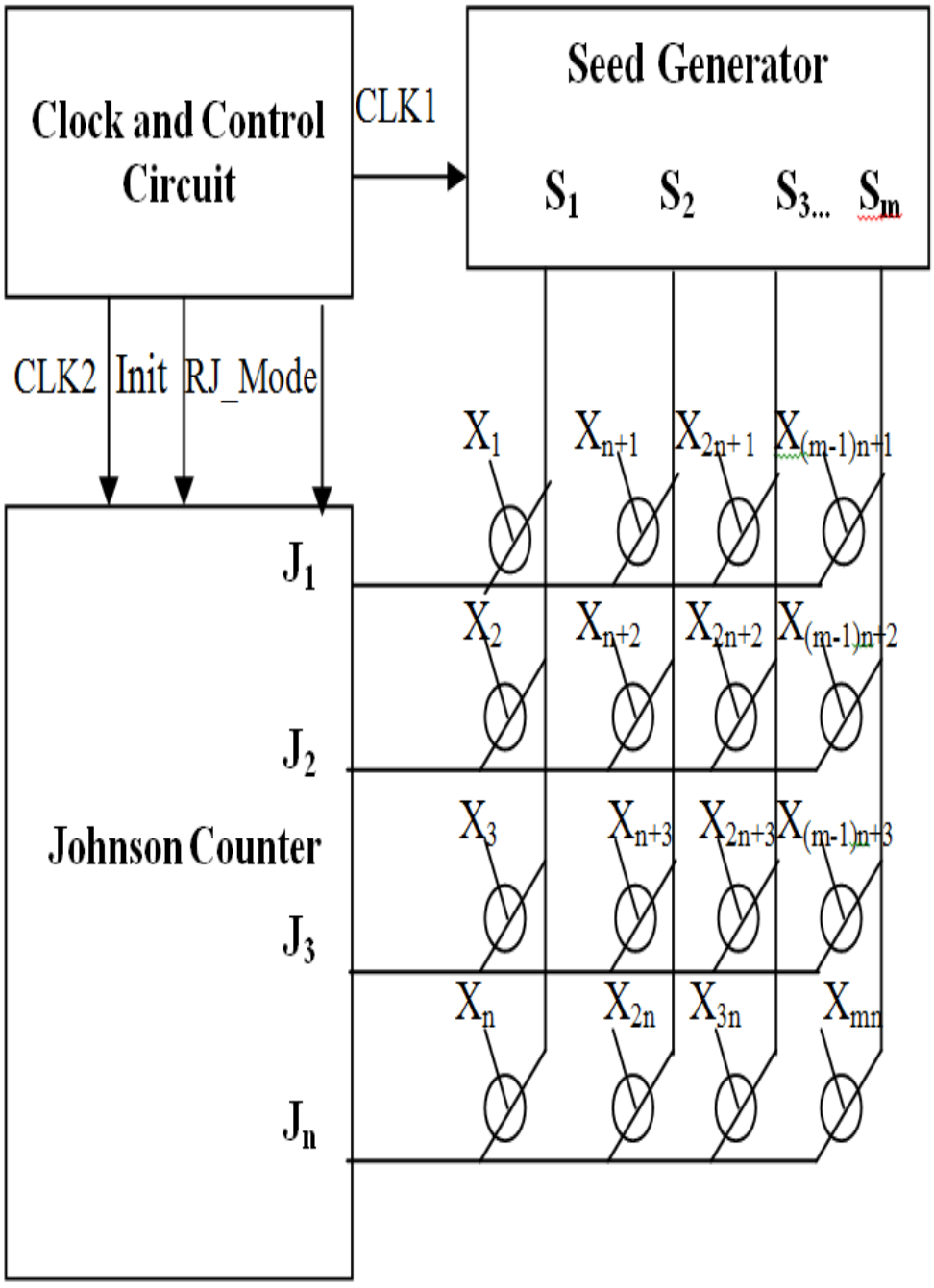

Figure 2:*Applying MSIC Vectors to Scan Chain.*

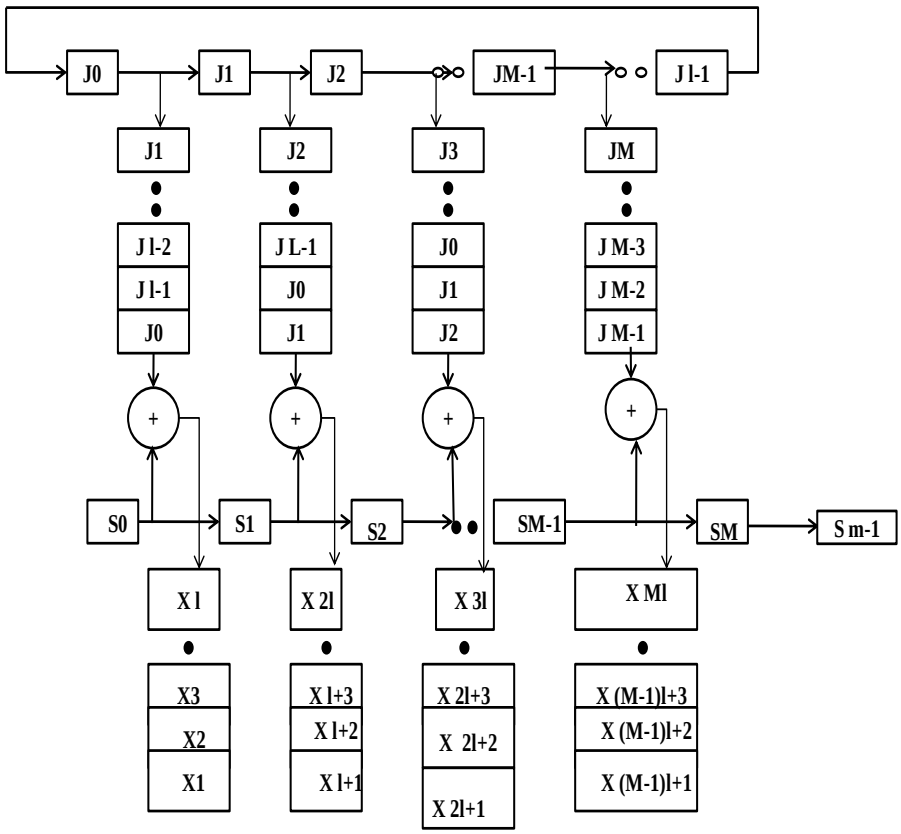

Figure 3:*Test Per Clock Schemes.*

The pattern generation method for BIST shown in Figure 2 involves generation of test vectors by performing Exclusive-or operation between the seed vector and reconfigurable Johnson counter. The Reconfigurable Johnson counter generates Johnson vector and the seed block generates the seed vector. The results obtained were loaded into the scan chain. The vectors are circularly shifted continuously and Exclusive-or operation is performed with the seed vector. The procedure is repeated until all the scan cells are loaded. The eight bit patterns generated were tested on 4*4 Multiplier circuits.

Test Pattern Generation Using Test per Clock

The Exclusive-or entryway gets contribution from reconfigurable Johnson counter and seed generator. The clock flag CLK1 and CLK2 were created utilizing clock and control circuit. The clock signal CLK1 is applied to seed generator block to produce seed vector. The clock signal CLK2 is applied to Johnson counter block to produce Johnson vector as shown in Figure 3.

The following procedure is adopted to generate the patterns:

1) The clock signal CLK1 is clocked to produce the seed.
2) The clock signal CLK2 is clocked to produce Johnson vector
3) Generate 2l Johnson vectors by repeating step 2.
4) Steps 1-3 were repeated until the specified test length is achieved.

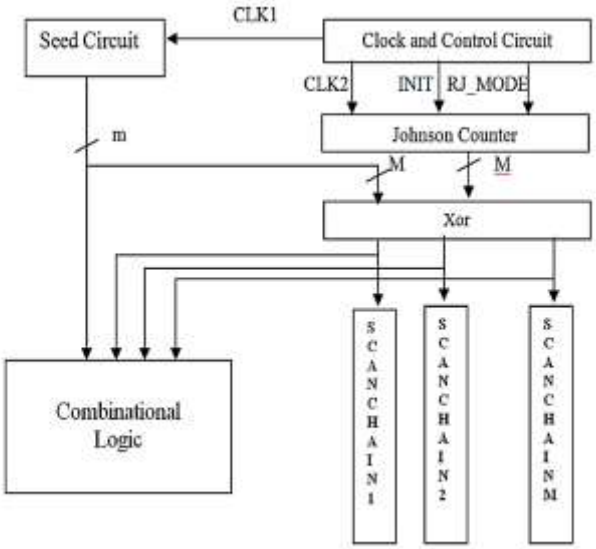

Figure 4:*Test per scan schemes.*

Test Pattern Generation Using Test per Scan

The clock and control circuit produces the clock flag CLK1 and CLK2. The information CLK1 was connected to seed generator to produce seed vector. The info CLK2 was connected to Johnson counter to create Johnson vector. The Exclusive-or gate is fed by the inputs from seed vector and the Johnson vector. The vectors produced were fed into scan chain and then applied to the circuit that is to be tested as shown in Figure 4.

The procedure for generating test pattern generation using test per scan are as following:

1) The clock signal CLK1 is clocked to produce the seed.
2) The value of RJ_Mode is assigned with the value 0 and Init is assigned with the value 1.
3) The clock signal CLK2 is clocked to produce Johnson vector.
4) Generate 2l Johnson vectors by repeating steps 2 and 3.
5) Steps 1-4 were repeated until the expected test length is achieved.

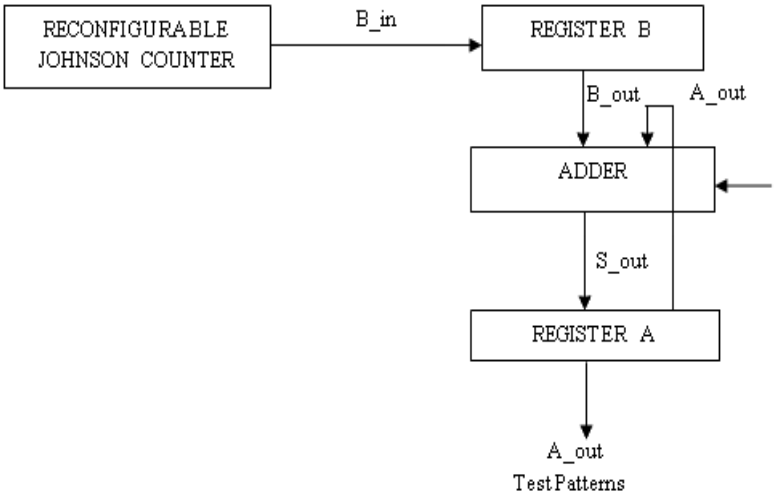

Figure* 5:TPG Using Reconfigurable Johnson Counter and Accumulator.*

PROPOSED METHODOLOGY

Cost, Power and Area are the testing territories in VLSI. The requirement for the versatile gadgets is expanding quickly. Thus Area and Power enhancement are fundamental. Here different structure for creating test designs for BIST was introduced. The created examples are tried on the circuit under test. The reaction acquired is contrasted with the known outcome with confirm the rightness of the circuit. The test designs created were connected on multiplier circuit. The correct working of the circuit is checked by contrasting and the known outcome. The circuits are intended to produce the test designs with less number of switches between progressive bits. The ensuing test changes between the progressive vectors were diminished to limit the power necessities.

TPG Using Reconfigurable Johnson Counter and Accumulator

Reconfigurable Johnson counter is joined with gatherer design as appeared in Figure 5 is proposed to produce test designs. The vectors were created utilizing an 8-bit Johnson counter. For the principal clock cycle, Register A will be instated to known esteem. The output of the Johnson counter J= J0 J1 J2,…, Jl-1 is stored in Register B. Full adder circuit performs addition operation of A_out from the previous generated test pattern, B_out from register B, and previous carry C_in. The result manipulated from the full adder circuit S_out is stored in register A. The generated patterns A_out= A_out1 A_out2….. A_out8 are sent out from Register A. The output A_out is the required test pattern.

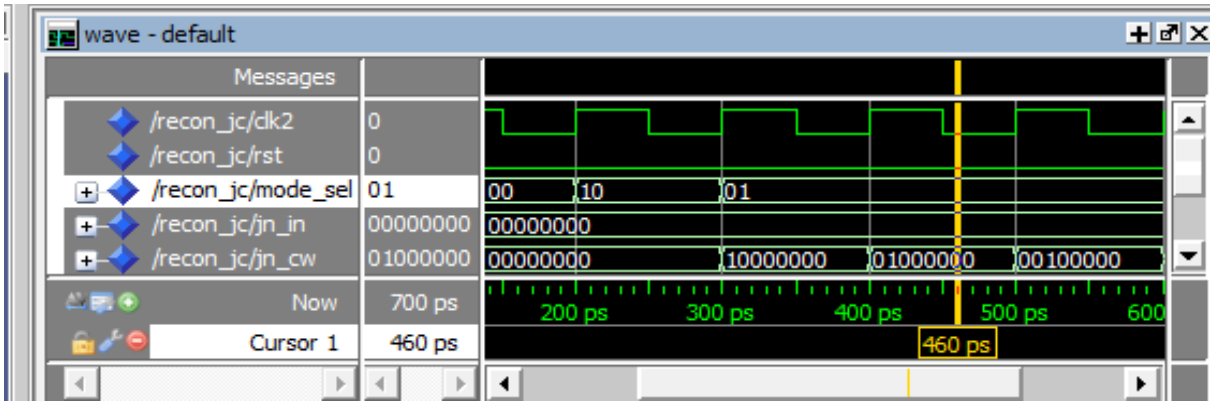

Figure 6:*Generation of Johnson Vector.*

SIMULATION RESULTS AND ANALYSIS

The different structure of the test design age for BIST is executed utilizing front end. The structure is coded in VHDL and mimicked utilizing ModelSim 10.0b programming. The test designs produced were tried on 4*4 Multiplier circuit. The investigation of zone and power are performed utilizing Xilinx ISE 9.1 programming.

Testing of Multiplier Testing of Multiplier using Reconfigurable Johnson Counter & LFSR

Generation of Johnson Vector

The simulation results for generating the Johnson vector is shown in the Figure 6. Whenever the mode_sel is “00” the counter acts in initialization mode. So the Johnson counter output Jc_cw is “00000000”. Whenever the mode_sel is “10” the counter acts in Normal mode. The input to the Johnson counter Jn_in is “00000000”. The output obtained after normal mode at Jn_cw is “10000000”. Whenever the mode_sel is “01” the counter acts in circular shift mode. The

input to the Johnson counter Jn_in is "10000000". The output obtained after circular shift mode Jn_cw is "01000000".

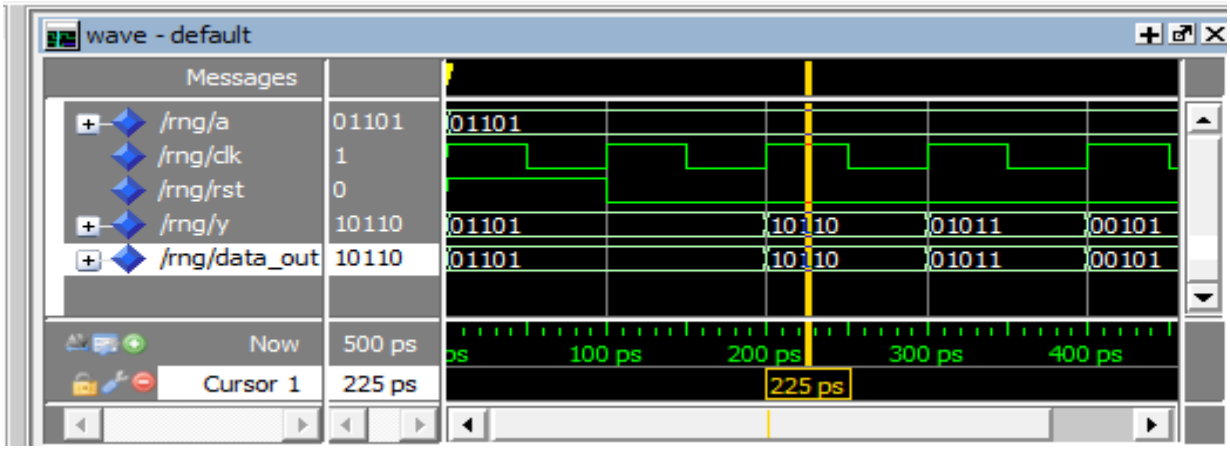

Figure 7:*Generation of Seed Vector.*

Generation of Seed Vector

The simulation result for generating seed vector is as shown in the Figure7. The input vector 'a' is fed as "01101". The rst value is set to the value '1' to reset the entire flip-flops. The rst value is set as '0' and the input vector is fed as '01101'. The corresponding output is obtained at the output data out.

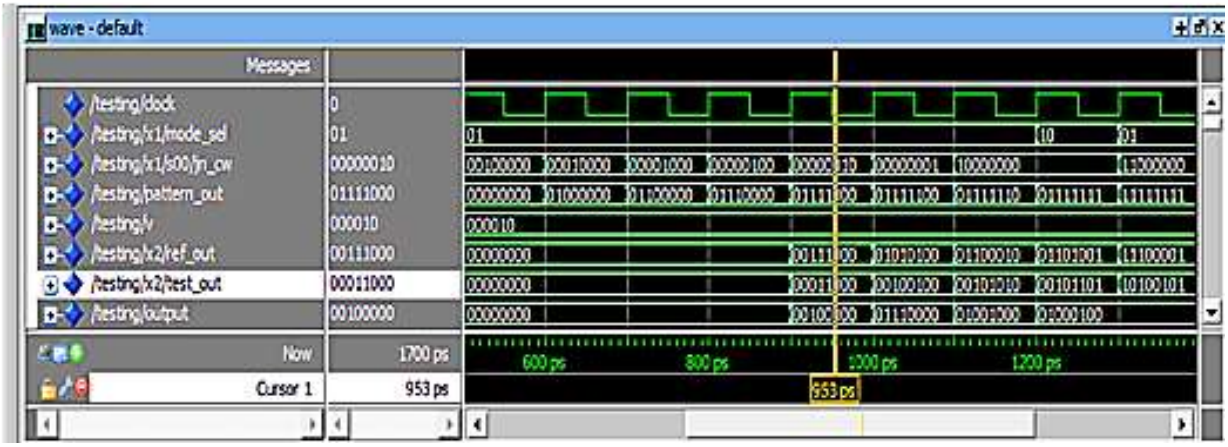

Figure 8:*Testing of Multiplier using Johnson Counter &Accumulator Architecture.*

Analysis of area, power, test length and delay for generating test patterns using reconfigurable Johnson counter and seed vector is performed. For implementing the testing on multiplier circuit using reconfigurable Johnson counter and seed vector 312 gates were required. The total power estimation is 41.79 mW and delay is 11.171 ns. The total number of patterns required to cover all possible stuck-at-faults is 12.

Testing of Multiplier Testing of Multiplier using Reconfigurable Johnson Counter &Accumulator Architecture

The recreation result for creating the testing multiplier circuit by applying test designs produced utilizing reconfigurable Johnson counter and collector engineering is appeared in the Figure 8. The timing is given to create Johnson vectors. The output signal ref_out is the expected result and test_out is the output after injecting the test patterns. Here the injected fault v

is set to the value "000010" indicating s-a-0 fault at second input bit of multiplier. Here the pattern "01111000" is applied on the multiplier circuit and the expected result of the multiplier circuit ref_out is "00111100". But the result obtained after injecting s-a-1 fault at first input bit of multiplier circuit test_out is "00011000". The results of ref_out and test_outobtained by applying the vector "00011000" are different. Hence the pattern "01111000" is capable of detecting s-a-0 fault at second input bit of multiplier.

Analysis of area, power, test length and delay for generating test patterns using Reconfigurable Johnson Counter and Accumulator is performed. For implementing the testing on multiplier circuit using Reconfigurable Johnson counter and Accumulator 160 gates were required. The total power estimation is 38.26 mW and delay is 6.314 ns. The total number of patterns required to cover all possible stuck-at-faults is 12.

Table 1:*Analysis Report*

Table Head	**Table Column Head**			
	Area (Gate count)	***Power (mW)***	***Test Length***	***Delay***
Reconfigurable Johnson Counter and LFSR (Existing Methodology)	312	41.79	12	11.171
Reconfigurable Johnson counter & Accumulator (Proposed Methodology)	160	38.26	12	6.314

CONCLUSION

The design for creating test designs for BIST is proposed. Reconfigurable Johnson Counter and Accumulator is utilized to produce the test designs with decreased region overhead. The single information change designs created to enhance the connection between's the progressive test designs in this manner decreasing force prerequisites. This strategy to produce the different test designs changing in single piece position for BIST plans is coded utilizing VHDL and reproduced utilizing ModelSim 10.0b. The entryway check and power utilization of the test design age were broke down utilizing Xilinx ISE 9.1 programming. 100% blame inclusion is accomplished and time inclusion is same as time required for producing designs utilizing existing procedure. The region decrease of 49% and power decrease of 8% are accomplished while producing test designs utilizing Counter, Decoder and Accumulator.

REFERENCES

1. NouraniM., Tehranipoor M., & Ahmed N.Low-transition test pattern generation for BIST-based applications.*IEEE Transaction*. March 2008. 57(3), pp.303–315.
2. ZhangX., Roy K., & Bhawmik S.POWERTEST: A tool for energy conscious weighted random pattern testing.*Proceedings of 12th International Conference VLSI Design*. January 1999. pp. 416–422.
3. Abdallatif S. F. Q. &Abu-Issa S.Multi-degree smoother for low power consumption in single and multiple scan-chains BIST.*Proceedings of 11th International Symposium Qualitative Electronic Design*. April 2010.pp. 689–696.
4. ChunS., Kim T., &S. Kang. A new low energy BIST using a statistical code.*Proceedings of Asia South Pacific Design Automation Conference*. March 2008.pp. 647–652.

5. Bin Zhou, Yi-zheng Ye, Zhao-lin Li, Xin-chun Wu &Rui Ke. A new low power test pattern generator using a variable-length ring counter.*Proceedings of Qualitative Electronic Design*. March 2009.pp. 248–252.
6. Yi-Hua Li, Wei-Cheng Lien. Capture-Power-Safe Test Pattern determination for At-Speed Scan-Based Testing.*Proceedings of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. January 2014,33(1).
7. Touba &McCluskey. Test Point Insertion for Non-Feedback Bridging Faults.In *IEEE International Conference*. 1997, pp. 54–60.
8. Touba &McCluskey. Using path tracing for test point placement.*In IEEE Conference*,1996.pp. 2–8.
9. ReazM.B.I, Yasin F.M., Sulaiman M.S.& Ali M.A.M. The simultaneous logic and IDDQ testing of CMOS ICs with mixed-mode testing facility for sequential circuits.*In IEEE Conference Publications*. 2003. pp. 234–235.
10. AlpaslanElif, Huang Yu, Xijiang Lin. on Reducing Scan Shift Activity at RTL.*In IEEE Journals & Magazines*. 2010.pp. 1110–1120.
11. McCluskeyE.J.&Bozorgui-Nesbat S.Design for autonomous test', Computers.*IEEE Journals &Magazines*. 1981.pp. 1070–1079.
12. RahamanHafizur, Debesh K. Das, Bhattacharya Bhargab B. An Adaptive BIST design for detecting multiple stuck-open faults in a CMOS complex cell.*IEEE Jounals & Magazines*. 2008.pp. 2838–2845.
13. PomeranzIrith (Fellow). Low-Power test generation by merging of functional broadside test cubes.*IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.July 2014. 22(7),pp. 1570–1582.
14. AhmedN., Tehranipur M.H. &Nourani M. Low power pattern generation for BIST architecture.*Proceedings of the 2004 International Symposium on circuits and systems*.2, pp. 689–692.
15. ManichSalvador, Lucas Garcia-Deiros, &Joan Figueras. Minimizing Test Time in Arithmetic Test-Pattern Generators with Constrained Memory Resources. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.November 2007. 26(11).

Cite this article as: *M. Nandini Priya, R. Vivitadurga, & U. Priya. (2019). Design of Low Power TPG for BIST Using Reconfigurable Johnson Counter. Journal of VLSI Design and Signal Processing, 5(1), 7–16. http://doi.org/10.5281/zenodo.2532997*