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Study on a Compact and High Speed 4-bit BCD Adder

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Abstract

Speed, simplicity and efficiency in data storage are the highlights of using binary data for arithmetic operations in computer systems. But it is an irony that human beings have preferred decimal as the number base for all calculations done by hand even with the advent of binary data. Commercial databases contain more decimal data and their consequent conversion to binary and then back to decimal when used with binary arithmetic hardware reiterates the need for a decimal arithmetic hardware support in financial and commercial applications. As the use of an adder circuit is indispensable in both platforms of binary and decimal we opt the Binary Coded Decimal (BCD) adder. Compactness of gadgets, speed and abating power consumption has turned out to be an inevitable aspect over a plethora of applications. Concentrating on reducing area here we analyze different 1-bit adder cells namely SERF adder, 10T adder, 8T adder, and 6T adder cells. Simulations were done in Cadence Virtuoso tool at 180nm and 90nm for technology independence. The 6T adder outperforms in terms of area, power and PDP and is implemented in 4-bit BCD adder estimating the delay and power consumed against the conventional design in 90nm technology. Simulation results estimate that the proposed BCD adder outperforms the conventional design in all design aspects of area, power, PDP and delay.

Keywords: *Static energy recovery full adder (SERF), ripple carry adder (RCA), 10 transistor (10T), 8 transistor (8T), 6 transistor (6T)*

INTRODUCTION

In the present era there is an increasing demand for decimal arithmetic hardware support in financial and commercial applications due to three inevitable reasons [1]. The approximate representation of fractional decimal numbers, commercial databases with more decimal data and their corresponding conversion lag between binary and

decimal, and the decimal software running on top of the underlying binary hardware in most of the commercial applications constitutes the package that reiterates the significance of decimal arithmetic hardware support in today's commercial platform. Now, we know that the use of an adder is obvious be it binary or decimal and hence we concentrate on the Binary Coded Decimal (BCD) adder. The conventional design of a 4-bit BCD adder is constituted by two 4-bit full adders and carries detection logic circuit [2]. In the initial stage one of the 4-bir full adder computes the binary addition results generating a carry if the addition result is greater than the decimal number '9'. Consequently, the result needs to be corrected by adding the decimal number '6' which is preceded in the next stage by the other full adder cell. Two AND gates and one OR gate constitute the carry detection logic circuit. Compactness, convenience and high speed are the trademarks of this generation. It applies to all aspects of life and accessories. In our digital life this can be achieved by working on the basic core circuits for which we suggest the adder cell as it is the heart of any digital computation. Apart from fundamental arithmetic operations it exists as a part and parcel of the division, multiplication, subtraction and exponentiation operations. It finds its place in designing all types of processors like Digital Signal Processors (DSP), microprocessors etc. It is equally important to observe that in most of the digital systems the adder lies in the critical path that determines the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is an inevitable design aspect. The design criterion of a full adder is actually multi-faceted. The transistor count which is of primary concern, while power consumption and speed being the other two important design criteria. A plethora of full adder designs are already reported in literature, which is based upon different logic styles like, static CMOS, dynamic, transmission gate, or pass transistor logic. Each has got its own pros and cons. Here, we target on compactness and speed without compromise on power consumption for which we consider different 1-bit adder cells designed using XOR - XNOR gates. SERF adder, 10T adder, 8T adder and 6T adders are compared against the conventional adder cell with 28 transistors in terms of Area, Average power, Delay and Power delay product.

The remaining part of the paper is organized as follows. Next section gives a review on the conventional 1-bit full adder

cells namely the 28T, 16T and the 14T adder cell. Brief information on the area reduced adder cells analyzed in this paper is postulated under section III. The simulation results of various adder cells compared against the conventional 28T adder cell at 180nm and 90nm is depicted in Results and Discussions that constitutes section IV. The concluding summary of the analysis and the implemented BCD Adder is brought about in Conclusion.

On the conventional adder cells

Complementary C-CMOS Adder Cell

The complementary CMOS (C-CMOS) full adder is based on the regular CMOS structure with pull-up and pull-down network comprising of 28 transistors (Figure 1) [3]. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes.

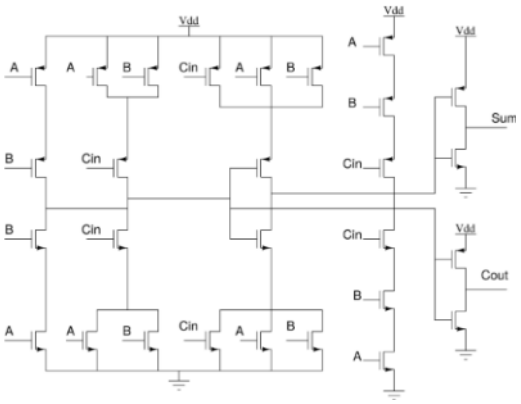

Fig. 1: *Conventional 28 Transistor Full Adder Cell.*

On the other hand the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area which have urged researchers to look for reduced transistor adder cells. The equations that form the Sum and Carry are as follows.

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = AB + Cin*(A \oplus B) \quad (2)$$

16T Adder Cell

The full adder cell realization of the circuit using 16 transistors as depicted in Figure 2 operates with full output voltage swing but consumes significant amount of power and has more delay compared to other adders having less transistor count which makes it undesirable for compact VLSI applications [4].

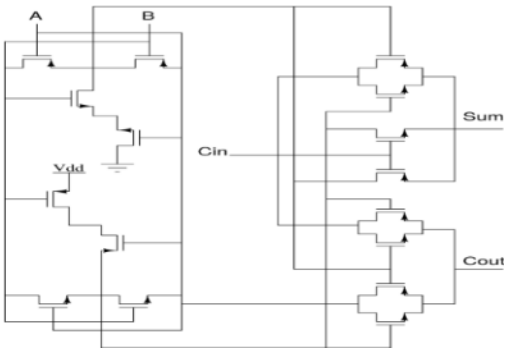

Fig. 2: *16T Adder Cell.*

14T Adder Cell

With the goal of further minimizing the number of transistors, XOR and XNOR circuits based on pass transistor logic were used and as a result the 14T full adder circuit as portrayed in Figure 3 was designed [4]. Researchers reveal that this design offers better delay and power performance compared to 16T full adder but it suffers from the threshold loss problem of approximately 0.4 V.

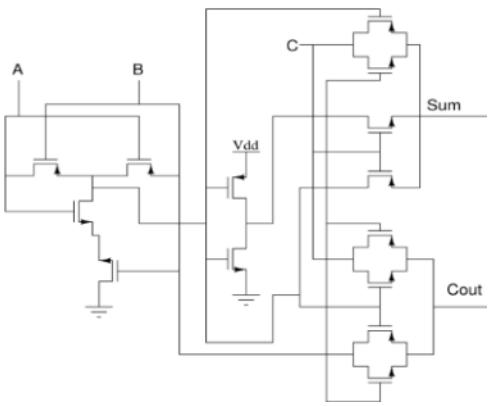

Fig. 3: *14T Adder Cell.*

ANALYSIS OF REDUCED AREA ADDER CELLS

As we target on occupying less silicon area we analyze few adder cells that exhibit less transistor count. As the essence of digital computing lies in the 1-bit full adder cell, their area reduction will consequently enable VLSI circuits to be more compact.

SERF Adder cell

The SERF adder comprising of 10 transistors, with no direct path to ground abates power consumption [5]. The reapplication of the charge stored at the load capacitance to the control gates and the elimination of a direct path to ground portrays the SERF adder as an energy efficient design. On the contrary due to multiple threshold loss issues this design cannot be cascaded at low power supply voltage. Figure 4 portrays the SERF adder cell. It is designed by rewriting the Sum and Carry equations as given in equations (3) and (4).

$$Sum = \overline{A \oplus B \oplus Cin} \quad (3)$$

$$Carry = (A * (A \oplus B)) + (\overline{Cin} * (A \oplus B)) \quad (4)$$

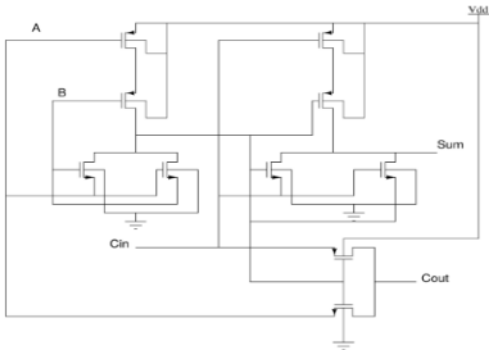

Fig. 4: *SERF Adder Cell.*

10T Full Adder Cell

The further designed 10T full adder (Figure 5) uses inverter-based 4T XOR gates in its design and shows remarkable improvements in power and delay [5–9]. It also reduces the silicon area. This reveals better performance than the SERF adder cell. The drawback of this circuit is that it also suffers from threshold loss problem of 0.35 V. The Sum and Carry equations realizing the circuit is as given below.

$$Sum = A \oplus B \oplus Cin \quad (5)$$

$$Carry = AB + Cin*(A \oplus B) \quad (6)$$

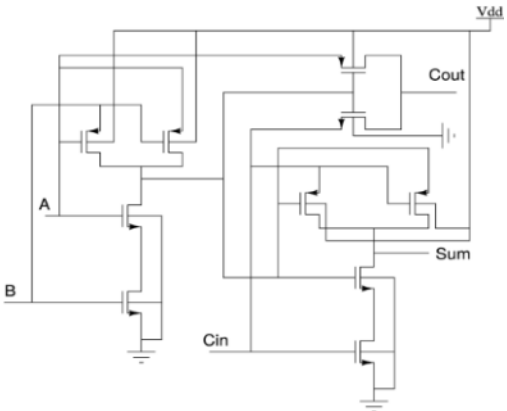

Fig. 5: *10 Transistor Full Adder Cell.*

8T Full Adder Cell

The three transistor XOR gate forms the 8T adder cell [5]. It acquires less silicon area. The design of 3T XOR gate is shown in Figure 6.

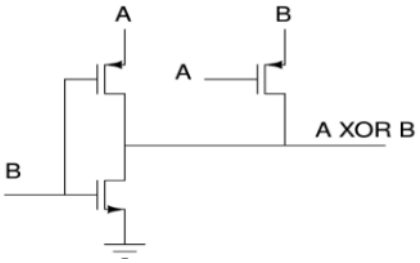

Fig. 6: *3 Transistor XOR Gate.*

The Sum output function is formed through a cascade of 3T XOR gates while Carry is realized using a wired OR logic in accordance with the equation given. The Boolean equations that form the Sum and Carry output functions are as listed.

$$Sum = A \oplus B \oplus Cin \quad (7)$$

$$Carry = AB + Cin*(A \oplus B) \quad (8)$$

Figure 8 depicts schematic of the above discussed 8T adder cell formed using 3T XOR gate.

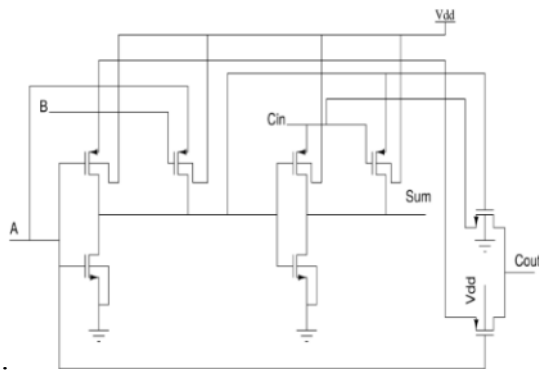

Fig. 7: *8 Transistor Full Adder Cell.*

6T Full Adder Cell

To prove that area can still be reduced we have the 6T adder designed with mere three multiplexers. Each multiplexer is designed using only two transistors as shown in Figure 8. The multiplexer can be used as both XOR and XNOR gate. In peer designs of 10 transistor adder the XOR/XNOR gates were designed using four transistors which increased the area. The 6T adder uses three multiplexers in its design making it more area efficient. In the present day world all VLSI devices need to be compact as portability is a main design consideration. This 6T adder is apt for such applications.

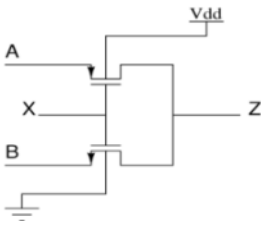

Fig. 8: *2 Transistor Multiplexer Design.*

The output of MUX1 signal is used as select signal in MUX2 where Cin and Cinbar are input signals. MUX2 generates the Sum output. The output of MUX1 is also used as select signal for MUX3 where Cin and A are input signals. The output of MUX3 is carry signal Cout. These can be designed as shown in Figure 9 by rewriting Sum and Carry equations as given. MUX1 is used to generate (AB) signal. It is used as control signal in both MUX2 and MUX3. MUX2 is used to generate Sum signal and MUX3 is used to generate carry signal.

$$Sum = (A \oplus B)*\overline{Cin} + (A \overline{\oplus} B)*Cin \quad (9)$$

$$Carry = (A \oplus B)*\overline{Cin} + (A \oplus B)*A \quad (10)$$

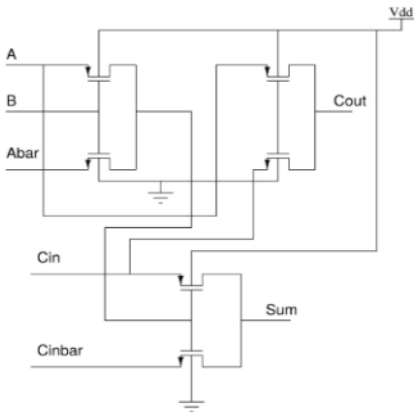

Fig. 9: *6 Transistor Full Adder Cell.*

On the design of 4-bit bcd adder

As portrayed in Figure 10 the conventional design of 4-bit BCD adder comprises of two 4-bit full adders and a carry detection logic circuit. The two 4-bit full adders are basically Ripple carry adders where the carry output of one full adder cell is propagated onto the succeeding full adder cell. Each 1-bit full adder cell has to wait for the carry signal from its preceding cell to compute the result.

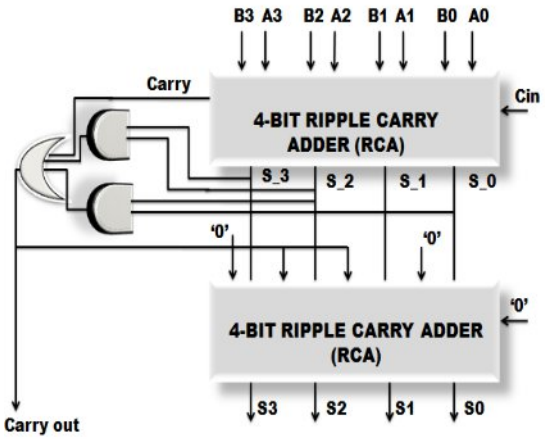

Fig. 10: *4-Bit BCD Adder.*

In our design we have implemented the analyzed 6T adder cell to form the Ripple carry adder as it occupies the least silicon area. The carry detection logic circuit is formed using two AND gates and one OR gate. The AND gates are designed using pass transistor logic with 2 transistors to reduce area while the OR gate occupies 3 transistors.

SIMULATION RESULTS AND DISCUSSIONS

The 1-bit full adder designs were simulated in Cadence Virtuoso tool. The adders were analyzed at both 180 nm and 90 nm for technology independence at 1.8V and 1V supply voltage. Their corresponding values of average power, delay, power delay product and area in terms of number of transistors were compared. The adder occupying least area with better delay and power performance is implemented in 4-bit BCD adder whose design parameters of area, average power, delay and power delay product is once again evaluated against the conventional design. As we scale down the technology, better power and delay performance is observed. The analysis details for 180 nm technology are tabulated in Table 1.

Average Power Comparison

The 6T adder cell consumes low power with a power saving of 99.99%, the SERF adder consumes 99.98% less power, while 10T adder shows 99.97% improvement and the 8T adder 58.13% than the conventional 28T adder design.

Delay Comparison

The SERF adder and the 8T adder cell exhibits 16.7% more delay than the conventional adder and the 10T adder shows mild increase of 0.04%. On the contrary we have the 6T adder with 19.96% improvement than the peer design.

Power Delay Product Comparison

The 8T adder outperforms other designs with least PDP followed by the 6T adder design. However, the 10T and SERF adder shows significant hike when compared against the conventional.

Area Comparison

It is evident that the 6T multiplexer based adder holds least transistors than the 8T, 10T and the SERF adder with 10 transistors. The conventional adder makes use of 28 transistors.

Table 1: *Simulation Results of 1-bit Adder Cells at 180 nm.*

Metric	**28T Adder**	**SERF Adder**	**10T Adder**	**8T Adder**	**6T Adder**
Area (Transistor)	28	10	10	8	6
Avg. Power (W)	1.019x 10^{-3}	1.752x 10^{-7}	2.159x 10^{-7}	4.266x 10^{-4}	0.7256x 10^{-7}
Delay (ns)	499.8	500	250	500	400
PDP (Joule)	5.09x 10^{-10}	8.76x 10^{-14}	5.4x 10^{-14}	2.13x 10^{-10}	2.904x 10^{-14}

Table 2 draws a comparison for the simulations carried out in 90 nm technology whose details are discussed below.

Average Power Comparison

The SERF adder cell consumes low power with a power saving of 81.62%, the 10T adder consumes 99.98% less power, while 8T adder shows 29.75% improvement and the 6T adder 72.56% than the conventional 28T adder design.

Delay Comparison

The SERF adder and the 8T adder cell exhibits 10% and 20% more delay than the conventional adder. On the contrary we have the 10T and the 6T adder with 60% and 20% improvement than the peer design.

Power Delay Product Comparison

The SERF adder outperforms other designs with least PDP followed by the 6T and 10T adder design.

Table 2: *Simulation Results of 1-bit Adder Cells at 90 nm.*

Metric	**28T Adder**	**SERF Adder**	**10T Adder**	**8T Adder**	**6T Adder**
Avg.Power (W)	2.551x 10^{-7}	0.468x 10^{-7}	1.792x 10^{-7}	6.559x 10^{-5}	0.6998x 10^{-7}
Delay (ns)	500	550	200	600	400
PDP (Joule)	4.038x 10^{-14}	2.57x 10^{-14}	3.58x 10^{-14}	3.94x 10^{-10}	2.8x 10^{-14}

With Area as the focus, delay and power as indispensable design aspects we find that 6T adder elicits desired performance suiting the need of the hour. The simulation results comparing 4-bit Ripple carry adder designed with 6T adder against the conventional design is tabulated. The proposed design proves 89.33% power efficiency, 20% improvement in delay with 78.57% area efficiency and 91.47% PDP. The simulation results are tabulated in Table 3.

Table 3: *Simulation Results of 4-bit Ripple Carry Adder.*

Metric	**Conventional RCA**	**6T RCA**
Area(Transistors)	112	24
Avg. Power (uW)	8.671x10^{-7}	0.925x10^{-7}
Delay (ns)	500	400
PDP (Joule)	4.34x10^{-13}	0.37x10^{-13}

Table 4: *Simulation Results of 4-Bit BCD Adder.*

Metric	**Conventional RCA**	**6T RCA**
Area (Transistors)	231	55
Avg.Power (uW)	35.85	5.364
Delay (ns)	500	313.5
PDP (Joule)	1.79x10^{-11}	0.168x10^{-11}

Table 4 tabulates the results of the proposed 4-bit BCD adder proving 76.19% area reduction, 83.64% power efficiency, 90.6% improvement in PDP and 37.3% reduction in critical path delay. These performance results are compared against the conventional design.

CONCLUSION

With increasing demand for decimal arithmetic hardware support in financial and commercial applications the BCD adder finds its place in today's market. Being an arithmetic tool speed is a factor which we can never give off at a compromise and thereby we focus on speed and compactness. With an effort to meet the technology trends of portable compact VLSI circuits we considered the heart of digital circuits which is the adder. Myriad designs based on varied XOR–XNOR gates namely the SERF adder, 10T adder, 8T and 6T adders were analyzed and compared against the conventional 28T. Power efficiency of BCD adder has already been achieved as reported in literature. We, therefore, focus on area and speed parameters. Simulations proved that the 6T multiplexer based adder showcases area and delay efficiency without compromise in power performance. The performance of the 4-bit BCD adder built on the proposed 6T adder also proves efficient when compared against the conventional realization. The Ripple Carry adder though having a simplified structure suffers from the issue of propagation delay. As the title highlights two design aspects of compactness and High speed, we target to focus on mitigating the issue of propagation delay in conventional design of BCD adder using Ripple carry adders.

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