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Implementation of Full Adder Using CMOS And DFAL Adiabatic Logic

[1]Himani Sharma, [2]Prachi Ahuja, [3]Shylaja V karatangi, [4]Amrita Rai, [5]Reshu Agarwal
[1,2]UG Scholar, [3]Assistant Professor, [4]Associate Professor
[1,2,3,4]Department of Electronics and Communication Engineering
[5]Assistant Professor, [5]Department of Computer Science and Engineering
GLBITM, Greater Noida, India
***Email:**[1]himanisharma199628@gmail.com, [2]prachiahuja2495@gmail.com,*
[3]shilajachalageri@gmail.com,[4]amritaskrai@gmail.com, [5]agarwal.reshu3@gmail.com,
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Abstract

Power dissipation has always been a major concern in today's world. With increase in technology, sizing and power consumption is a great analyzing parameter. Thus, each year new technologies are designed to meet the requirements using adiabatic techniques. Adder possesses importance in designing of ALU, digital signal processing, ripple counter. Designing of adder using conventional technique (CMOS) often create complexity and sizing issue with more energy dissipation. In this way, thus structuring adder with adiabatic system to determine previously mentioned issues. Here in this paper full adder is planned first utilizing CMOS procedure and after that utilizing DFAL (diode free adiabatic rationale) method and accordingly contrasting outcomes and ordinary cmos circuit.

Keywords: *DFAL, adiabatic techniques, CMOS*

INTRODUCTION

"Adiabatic" is a Greek word which suggest to a framework in which development occur without gain or loss of power. We realize that there are some tradition strategies to diminish control scattering, for example, by lessening supply voltage, diminishing capacitance and decreasing exchanging movement. But these techniques are not sufficient enough to meet today's requirement [3]. Hence, most of our concern is towards building adiabatic technique which is promising design for low power design.

Adiabatic logic works with the concept of switching activities which reduces the power by tracing back the path and giving stored energy back to supply [8]. Thus, adiabatic term is used for low power VLSI circuits.

In cmos circuit switching power due to charging and discharging is shown below:
Energy/transition = $C_L*(V_{dd})^2$(1)
Power =$C_L*V_{dd}^2*f$(2)

Short circuit power dissipation is due to non-rise-fall times. In this input has finite rise and fall. Direct current path is established from V_{dd} to GND while PMOS and NMOS are ON for short period of time[4].The short circuit current in cmos circuit is shown in fig. 1.

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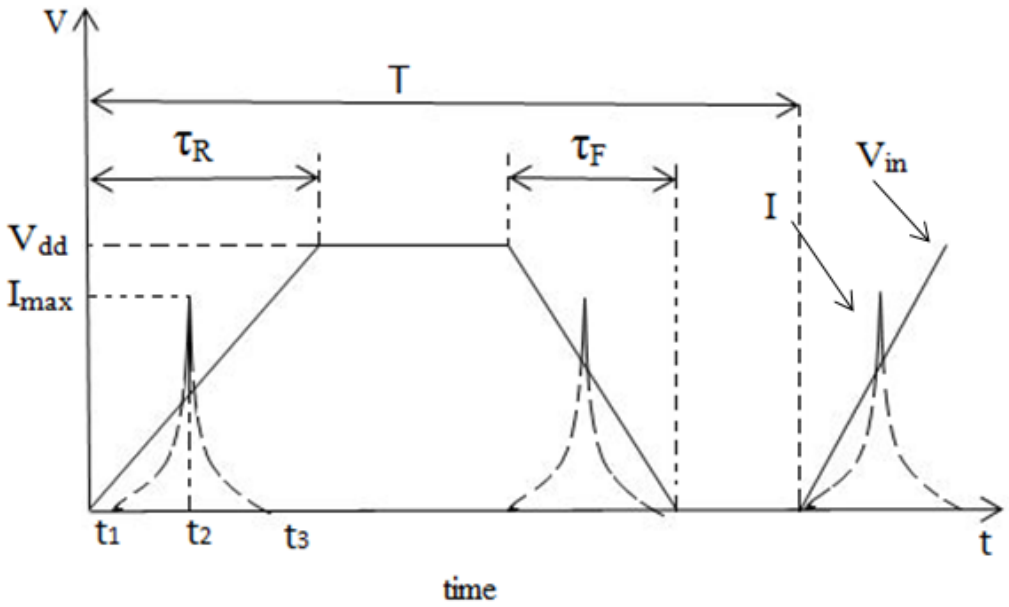

Fig: 1. *Short circuit current*

There is some little static dissemination because of reverse bias leakage between dispersion areas and the substrate. Also, sub limit conduction can add to the static dissemination. A straightforward model that portrays the parasitic diodes for a CMOS inverter ought to be taken a gander at so as to have a comprehension of the spillage associated with the gadget [6].

The word 'exchanging' (dynamic dispersal) here means a ton. It's not simply that inputs are exchanging, it's the yields too. That is on the grounds that, there's additionally control scattering that occurs while inputs switch and yields don't switch. So here, at whatever point input changes from rationale 1 to rationale 0, the yield changes from rationale 0 to rationale 1 and see charging current spilling out of Vdd to CLOAD which results to rise control. What's more, the other way around remains constant when input changes from rationale 1 to rationale 0.

ADIABATIC TECHNIQUE

The energy loss duringcharging and releasing way can be limited with the assistance of adiabatic exchanging. The charging and releasing of the hubs are finished by utilizing steady current amid adiabatic exchanging. The utilization of time shifting voltage supply regardless of settled voltage supply prompts the abatement in the rate of change in exchanging.The charging and discharging in the adiabatic circuits using both pull up network and pull down network[8].The energy is recycled using both pull up and pull down network for charging and discharging the output node capacitance.

The adiabatic logic family can be majorly classified into two categories as partially adiabatic techniques and fully adiabatic techniques. In partially adiabatic circuits, some of the charge is made to transfer to the ground while in fully adiabatic circuits,the whole load capacitance charge is made to recycle back to the power supply.Both logic families perform differently in terms of power clock synchronisation and operating speed. The partial adiabatic logic family includes techniques like Diode Free Adiabatic Logic (DFAL), Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL), 2N- 2NP adiabatic Logic etc. [2]. The fully adiabatic logic family includes pass

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transistor adiabatic logic (PAL), Split- Rail charge recovery logic(SCRL).

In this paper, the efficiency of adiabatic techniques over the conventional CMOS technique is stated by implementation of DFAL technique for designing of full adder. The most important feature of DFAL technique is that it is diode free.

In DFAL technique, split level power clock supply Vpc and Vpc are used. The voltage difference between the two is Vpc/2 which results in the minimisation of voltage difference leading to further reduction in power dissipation. The load capacitance is charged and released gradually by split dimension clock which prompts further minimisation of intensity dispersal. An additional NMOS transistor is connected in the draw down system in DFAL circuits. This NMOS transistor recycles back the charge to the power supply and hence recovers the adiabatic losses.

FULL ADDER IMPLEMENTATION

Full adders are logical circuits which are of very much importance. It has got many applications such as in designing of ALU, digital signal processing, ripple counter etc. Full adder performs the addition of binary numbers[1]. It takes 3 input bits A, B andC_{in}among which A and B are operands and C_{in} is the carry generated from the sum of previous bits.

The circuit generates the two output bits Sum and Carry. The schematic diagram of full adder can be shown as.

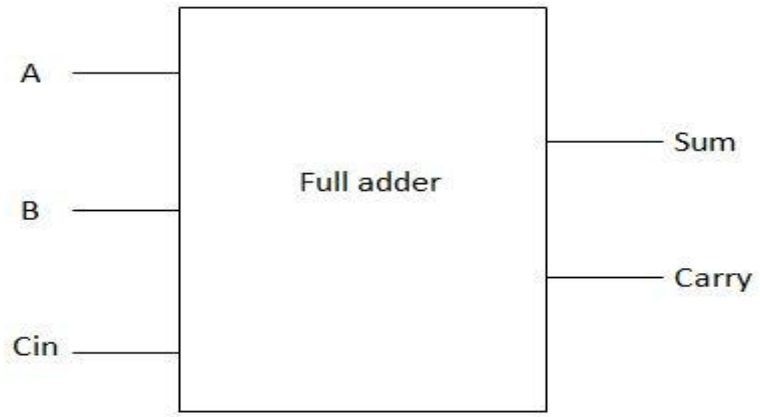

Fig: 2. *Block diagram of Full adder*

The logic of Full adder is in such way that there arises 8 input combinations as the values of inputs A, B and C can vary as 0 or 1.The truth table of full adder is shown in table1.

Table:1.*Truth table of Full Adder*

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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From the above table, the output expressions for sum and carry can be drawn.

The expression for sum is:
Sum = (A.$\bar{B}$.$\bar{C}$) + (A$\bar{B}$.C$\bar{)}$ + (A$\bar{B}$.$\bar{C}$) + (A.B.C)
Sum= (AB⊕C) ⊕ (3)

The expression for carry obtained is:
Carry = (A.B) + Cin(AB⊕)
Carry= (A.B) + (B.Cin) + (A.Cin) (4)

With the help of output expressions the full adder can be represented as combination of basic logic gates. It is clear from the expressions that the combinational circuit will require two X-OR gates, twoAND gates and one OR gate. The logic circuit for full adder is shown in fig3.

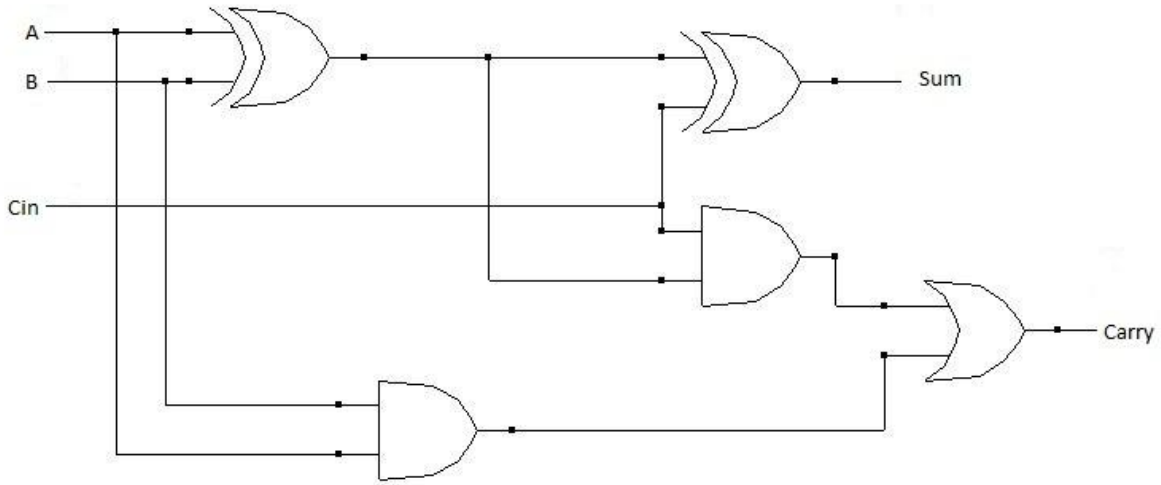

Fig: 3. *Logic circuit of Full adder*

Conventional Full Adder

To implement the full adder using CMOS logic,several approaches with different logic styles can be used. Different logic styles vary in terms of their performance thus have resulting in variations in power dissipation, size, complexity etc. All the approach is good in terms of one performance parameter by keeping others at expense. The conventional approach is one among the approaches possible. It is the simplest approach to design the adder to yield the logic functions.

The conventional CMOSframework mainly constitutes the two functional blocks. One is pull up network consisting of p-channel MOS transistors and another is pull down network consisting of n-channel MOS transistors. The NMOS and PMOS are complementing each other.The device switching is the main cause of power dissipation in CMOS circuits [1]. The conventional full adder implementing the sum and carry expressions are shown in fig4 and fig.5 respectively.

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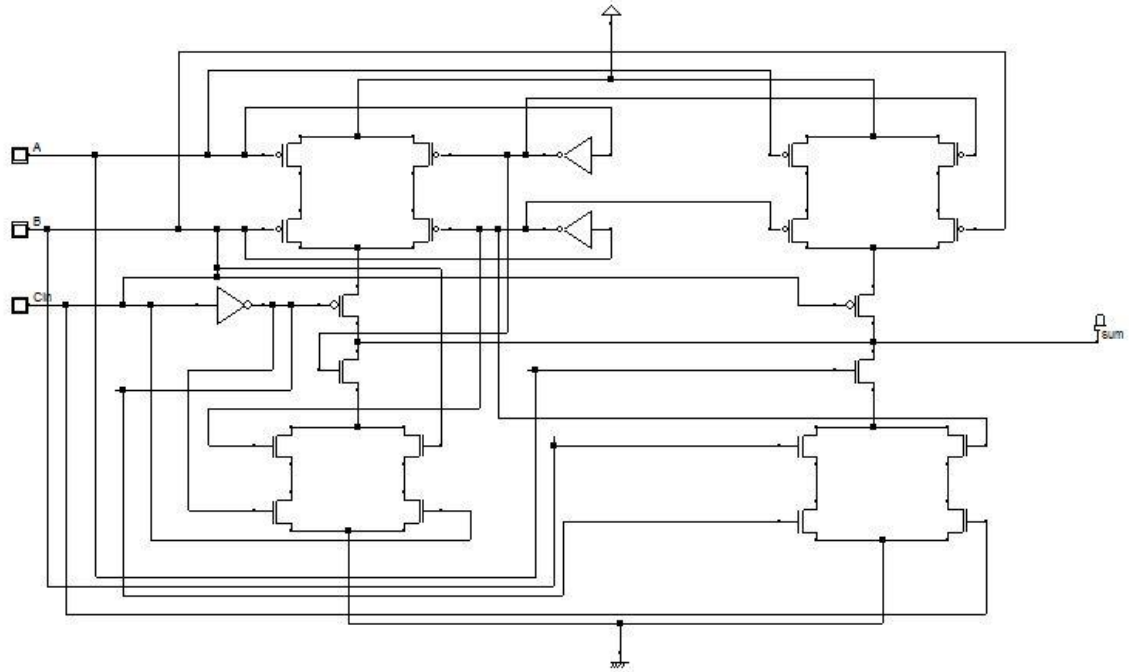

Fig:4. *CMOS implementation of Sum expression*

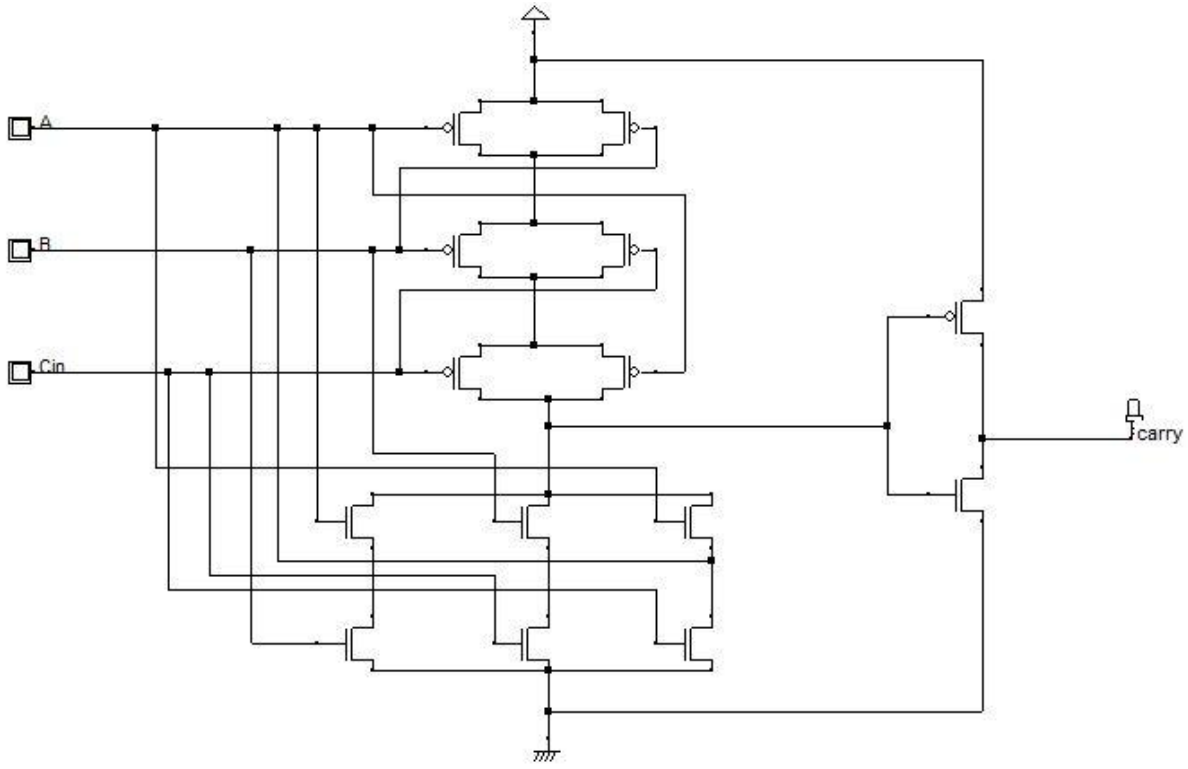

Fig:5. *CMOS implementation of carry expression*

The And-Or-Invert(AOI) logic is used to implement the expression of sum and carry of full adder. To represent the And operation, the NMOS transistors are connected in series and the PMOS transistors are connected in parallel while to represent the OR operation, the configuration is just opposite of the previous one.

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The AOI logic reduces the number of gates thus resulting in reduced complexity and area with increased speed.

Diode Free Adiabatic logic adder

The diode free adiabatic logic solves the problem of high power dissipation faced by conventional CMOS logic. The energy from the power supply can be recycled using this technique. The presence of the diodes in the charging and releasing way in the ordinary circuits is the fundamental driver of intensity dispersal. The DFAL rationale takes care of the issue by expelling every one of the diodes from these ways. The whole and convey squares of full viper utilizing diode free adiabatic rationale are appeared in fig.6 and fig. 7 separately

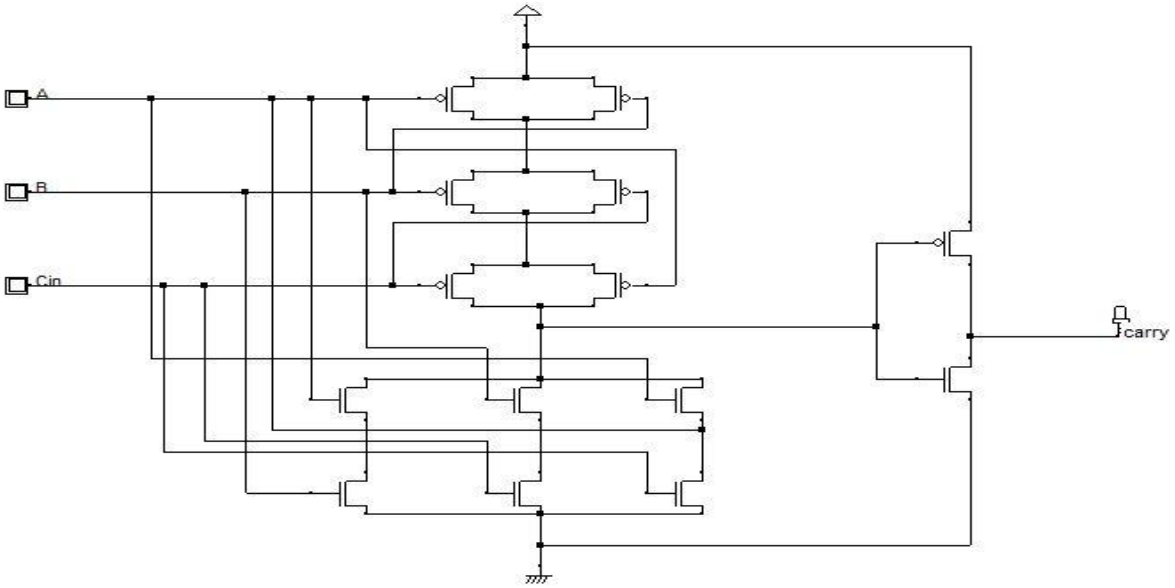

Fig:6.*DFAL implementation of Sum expression*

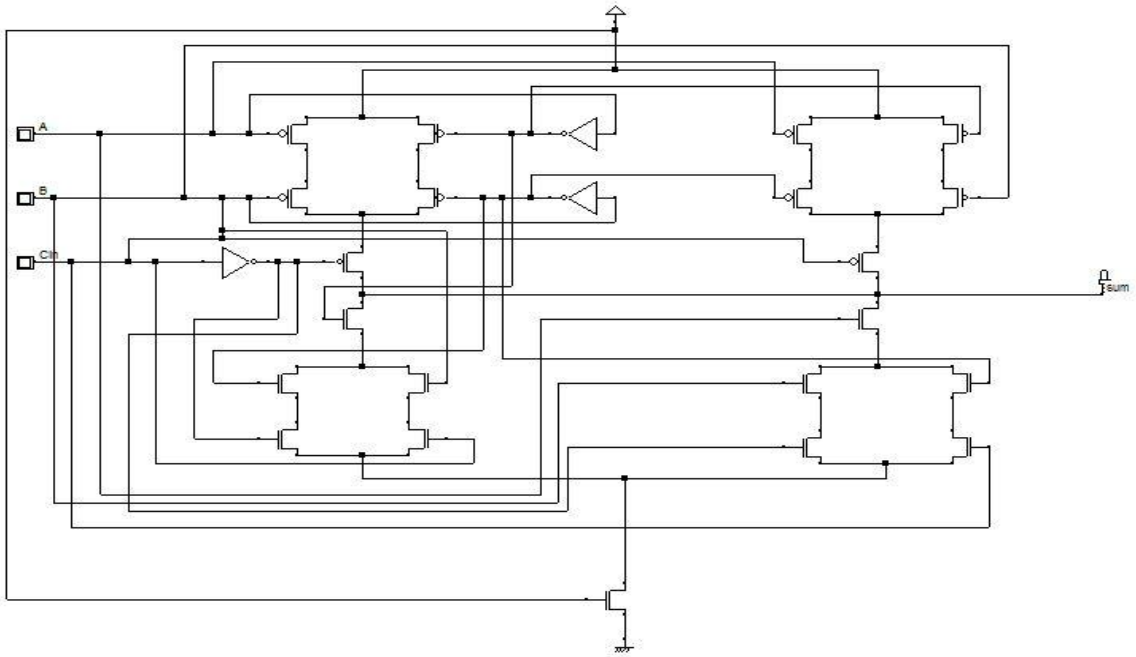

Fig:7. *DFAL implementation of carry expression*

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The switching activity in DFAL circuit is slow, which is a very important factor for power loss. Hence, resulting in less power dissipation.The shortcomings in the conventional approach such as large delay, high power dissipation are solved to much extent using DFAL approach.

WAVEFORMS

The implementation of the sum and carry expressions of full adder is done using DFAL adiabatic technique. The output waveform of sum logic for full adder implemented by DFAL is shown in fig.8.

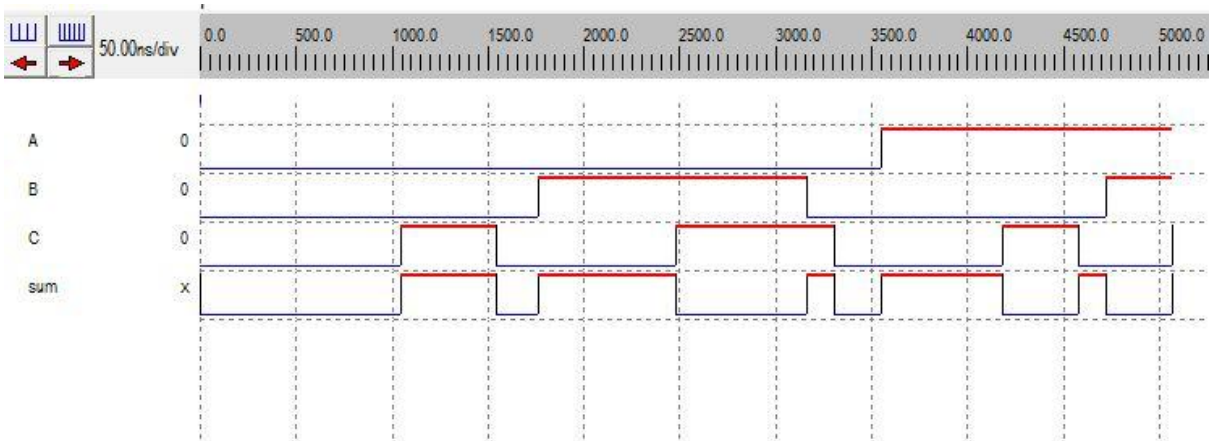

Fig:8.*Output waveform of Sum expression*

The output waveform of carry logic for full adderimplemented by DFAL technique is shown in fig. 9

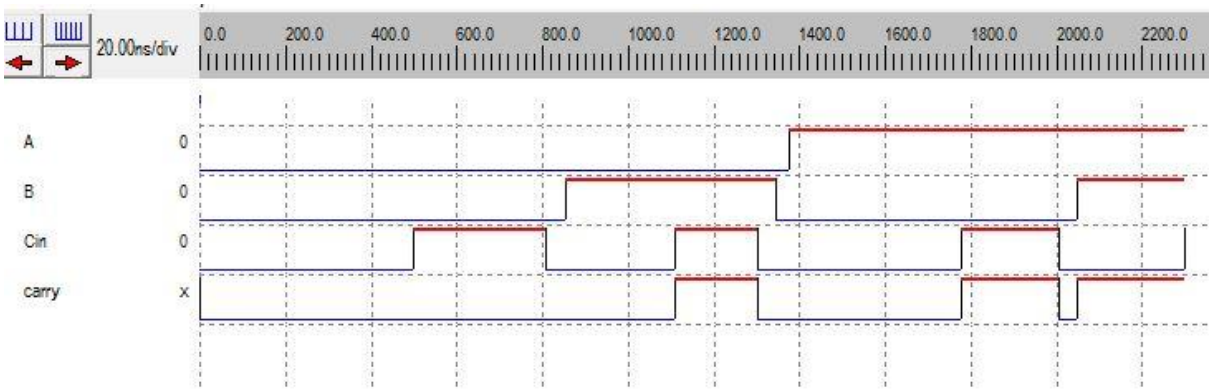

Fig:9.*Output waveform of carry expression*

CONCLUSION

Adiabatic techniques are sub categorized into fully adiabatic and partially adiabatic. Fully adiabatic circuits are much more complex to design than partially. But the latter is not as efficient as former. Thus, we can say that partially adiabatic circuits are fair compromise between power consumption and complexity trade off.

Above, we have described all about full adder implementation using DFAL and conventional method. It is very much evident that power dissipation in conventional method is much more than DFAL technique. This so happened because in DFAL technique we have used an additional NMOS transistor. This transistor is making the circuit diode free. In conventional method while discharging, circuit dissipates a lot of power whereas this is cured in DFAL method.In this paper we too got to know a lot about adiabatic families,its working, type and benefits

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over conventional technique. Reduction in size and power conservation is the heated topic in today's scenario. Thus, we have observed that adiabatic is better than CMOS method.

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