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Study of Characteristics Curves Top-Gated Graphene FET Using SILVACO TCAD

Muhammad Johirul Islam[1], Rifat Sami[2], Md. Shafiqul Islam[3], Md. Iqbal Bahar Chowdhury[4]
[1]Research Assistant, [2,3] Student, [4]Associate Professor
Department of Electrical and Electronics Engineering, United International University, Bangladesh
[1]johir021@yahoo.com, [2]samirifat@yahoo.com, [3]shafiq2eee@gmail.com, [4]ibchy@eee.uiu.ac.bd

Abstract
This work presents a SILVACO TCAD based fabrication and device simulation of a top-gated graphene field-effect transistor. Effects of channel length and channel doping concentrations on the characteristics curves (transfer and output characteristics) of the GFET are also investigated and analyzed physically to obtain more physical insight.

Keywords*: Graphene FET, Transfer Characteristics, Output Characteristics, SILVACO TCAD, ATLAS, ATHENA.*

INTRODUCTION

Graphene, a monolayer of carbon atoms packed into a two-dimensional (2D) honeycomb lattice, has demonstrated high mobility, high carrier velocity and excellent thermal conductivity as well as possessed optimum electrostatic scaling owing to its monolayer thin body [1]. Therefore, graphene is promising in serving as the channel material for ultrafast and scaled transistors. According to the International Technology Roadmap for Semiconductors [2], graphene has emerged as one of the most promising alternatives to silicon for the fabrication of high-performance switching devices. Graphene has many advantages of carbon nanotubes such as higher mobility and larger critical current densities. Unlike, carbon nanotube based FET, high on currents can be achieved in graphene based FET (GFET) without the requirement of assembling large parallel arrays of nanotubes [3].

When an electric field is applied at the gate of the GFET, the charge carriers in the 2D channel are changed from electrons to holes, where the Dirac point is the minimum point showing the transition. However, zero bandgap of monolayer graphene causes the on-off current ratio not to reach the desirable limit. Using narrow ribbons (called nano-ribbons) [4] or applying a perpendicular electric field to the bilayer graphene structures [5] results in a bandgap of up to 400 meV with an associated significant mobility degradation or significant band-to-band tunneling respectively.

There has been extensive research performed into graphene field effect transistors (GFET) since its discovery in 2004 [6]. The first graphene FET has been fabricated in April 2007 [7], whereas, the first gigahertz graphene FET has been fabricated in December 2008 [8]. In order to investigate the effects of various parameters on the performance of graphene FET, compact modeling as well as simulation based analysis are needed. First TCAD based simulation has been performed in [9], where SILVACO TCAD tools are used. Although [9] demonstrates characteristics curves under various conditions and determines various performance parameters (like DIBL (Drain-Induced Barrier Lowering), subthreshold slope etc.), proper physical

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understanding is not obtained from this work.
This work aims to provide a better physical insight of a GFET structure implemented and simulated using SILVACO TCAD and also, attempts to explain the physics of variations of characteristics curves of this GFET against the variations of the channel length and the channel doping concentration. The structure chosen in this work is a top-gated GFET in [10]. The fabrication of this structure is simulated using ATHENA tool and the device simulation is performed using the ATLAS tool of SILVACO TCAD.

STRUCTURE AND METHODOLOGY

SIMULATION OF FABRICATION PROCESS USING ATHENA

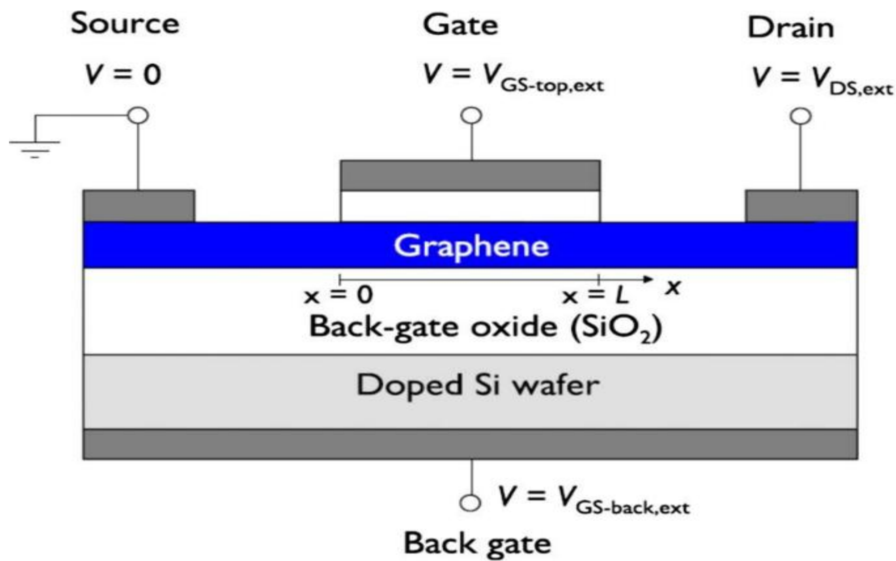
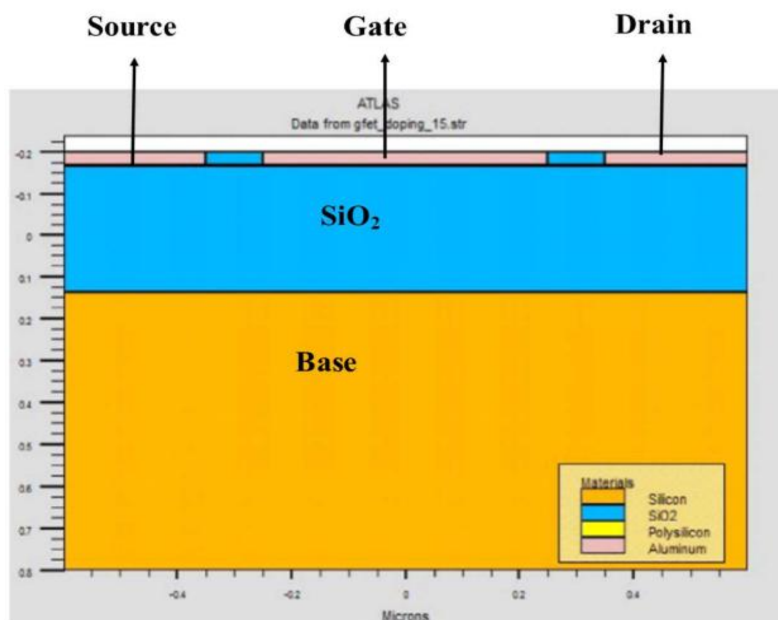


Fig.1: *Cross-sectional view of top-gated GFET structure reported in [10] and simulated in this work.*



(a)

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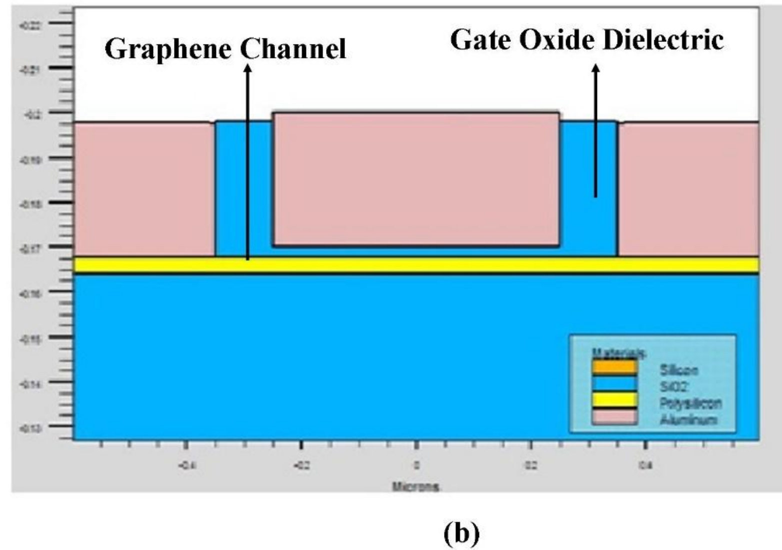

(b)

Fig. 2: *GFET structure implemented using Athena of SILVACO TCAD Tools. (a) Full view (b) Enlarged view of the channel region. Dimensions are defined in Table 1.*

In this work, the fabrication of silicon on insulator (SOI) based graphene channel FET (GFET) [reported in [10] and shown in Fig. (1)] is simulated using SILVACO ATHENA tool. Silicon doped with boron of $10^{15} cm^{-3}$ is used as p-type base for the GFET. (100) surface orientation is chosen for the silicon so that the fixed charge as well as the interface charge to be generated within the silicon-di-oxide (SiO_2) layer during oxidation is minimized [11]. Over silicon wafer a thick and long SiO_2 layer is grown by oxidation using dry oxygen at $1000^0 C$ temperature and 1 atmospheric pressure. The oxidation is performed under chlorine-rich environment to ensure the neutralization of mobile alkali ions in the oxide layer [11]. The thin graphene channel (5 nm) is then deposited using arsenic doping of $10^{15} cm^{-3}$ over SiO_2 layer. Since SILVACO TCAD possesses no information about graphene, polysillicon can be simulated as grpahene by changing its properties (bandgap, effective density of states and mobility for electrons and holes and permittivity) with those of graphene. Over the channel region, a thin (3 nm) gate oxide dielectric (SiO_2) is formed as top gate. Aluminium is used for the source, drain and top gate contacts. The fabricated device using ATHENA is shown in Fig. (2), where Fig. (2)(b) shows the enlarged view over the graphene channel region. Table 1 presents the materials and dimensions of various regions and contacts of the fabricated GFET.

Table 1: *Dimensions of GFET Structure in SILVACO TCAD Tools.*

Graphene Structure Region	Material	Thickness	Length	Doping
Top Gate contact	Aluminum	97 nm	500 nm	-
Top gate Dielectric (gate oxide)	SiO_2	3 nm	500 nm	-
Source Contact	Aluminum	100 nm	250 nm	-
Drain Contact	Aluminum	100 nm	250 nm	-
Channel	Polysilicon	5 nm	1200 nm	$1 \times 10^{19} cm^{-3}$ (Arsenic)
Dielectric layer on Base	SiO2	295 nm	1200 nm	-
Base	Silicon	400 nm	1200 nm	$1 \times 10^{15} cm^{-3}$ (Boron)
Insulator within gate and drain	SiO2	100 nm	100 nm	-
Insulator within gate and source	SiO_2	100 nm	100 nm	-

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DEVICE SIMULATION USING ATLAS

The virtually fabricated graphene FET is analyzed for characteristics curves using ATLAS tool of SILVACO TCAD. Various physical and mathematical models have been used to perform analysis in ATLAS. Shockley-Read Hall(SRH) model and Lombardi model (CVT) are used as physical models for the recombination mechanism and the carrier mobility respectively. Interface charge is assumed as zero whereas the fixed charge is chosen as $3 \times 10^{1}0 Coul/cm^{2}$. For numerical simulations, Newton and GUMMEL (maximum trap 4) models have been used.

RESULT AND DISCUSSION

This section represents and analyzes the simulation results obtained using SILVCO TCAD. Effect of variation of channel doping concentration and channel length on the characteristics curves are also investigated in this section.

The Figs. (3) (a) and (b) show the transfer characteristics and the output characteristics of a p-channel GFET using the dimensions mentioned in Table 1. From Fig. (3)(a), it is seen that, unlike Si MOSFET devices, the GFET is conducting for both positive and negative gate voltages- a characteristic feature of monolayer graphene based GFET. When the gate voltage is negative, the channel is accumulated with large number of holes and when the gate voltage is positive, the channel becomes inverted and contains a large number of electrons. The two branches of the transfer characteristics are separated by a point, usually called as Dirac point, and shows the minimum current. Therefore, when gate voltage is zero, unlike Si MOSFET devices, the GFET is not switched off. From Fig. (3)(b), three regions are identified, namely first linear region (Region I), inflection point (Region II) and the second linear region (Region III). This peculiar behavior can be explained as follows. For a positive gate voltage and for small V_{DS}, the entire channel is n-type with the voltage across the channel at the drain end is lower than that at the source end, resulting a thinner channel at the drain end. Under this condition the drain current increases linearly with V_{DS} and the $I_D - V_{DS}$ curve corresponds to the first linear region. As V_{DS} increases, the voltage across the channel at the drain end decreases and the channel at the drain end gets thinner. The inflection point is reached when $V_{DS} = V_{DS,crit}$ (region II). At this point, the channel ceases at the drain end i.e. pinch-off occurs and the voltage across the channel at the drain end corresponds to the voltage at Dirac point i.e. the voltage across the channel at the drain end becomes minimum. If V_{DS} is increased beyond the voltage at the inflection point, the pinch-off point moves towards the source end and the voltage across the channel at the drain end corresponds to the gate-to-source voltage V_{GS} which is at the left side of the Dirac point of Fig. (3)(a). As a result, the channel at the drain end becomes p-type. This 'p-type' region near the drain end increases as V_{DS} increases. This is because of the fact that as V_{DS} increases beyond the inflection point, the voltage drop across this 'p-type' portion of the channel increases, whereas, the voltage across the 'n-type' portion of the channel remains fixed at $V_{DS} = V_{DS,crit}$. Therefore, a second linear region in the $I_D - V_{DS}$ characteristic curve has been observed for $V_{DS} > V_{DS,crit}$. It is evident that $V_{DS} > V_{DS,crit}$, the graphene channel becomes ambipolar- 'p-type' near the drain end and 'n-type' near the source end. In this ambipolar channel, the pinch-off point acts as the place of recombination for the holes coming from the drain end and the electrons coming from the source end and no energy is released in this recombination owing to the zero bandgap of monolayer graphene [3].

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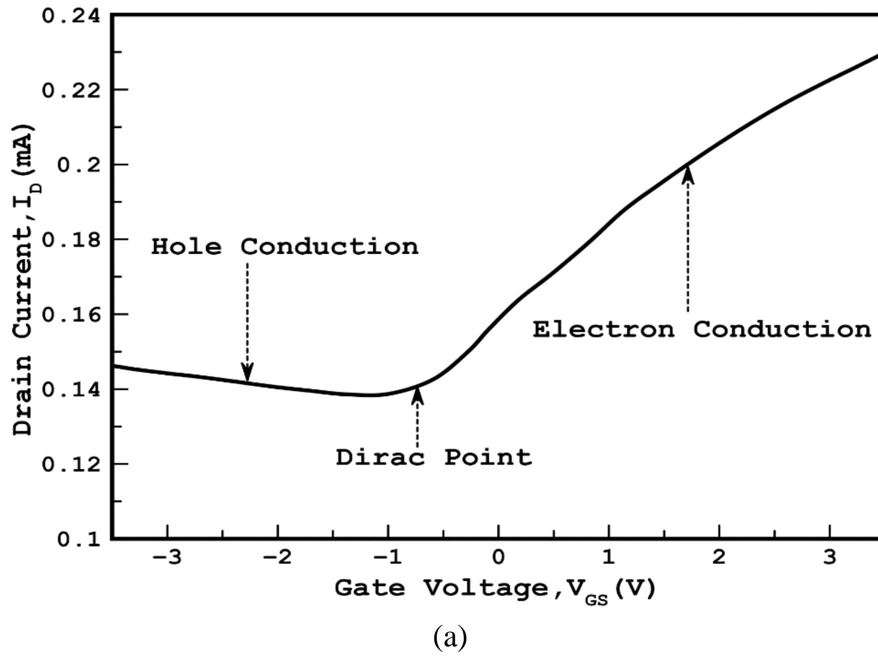
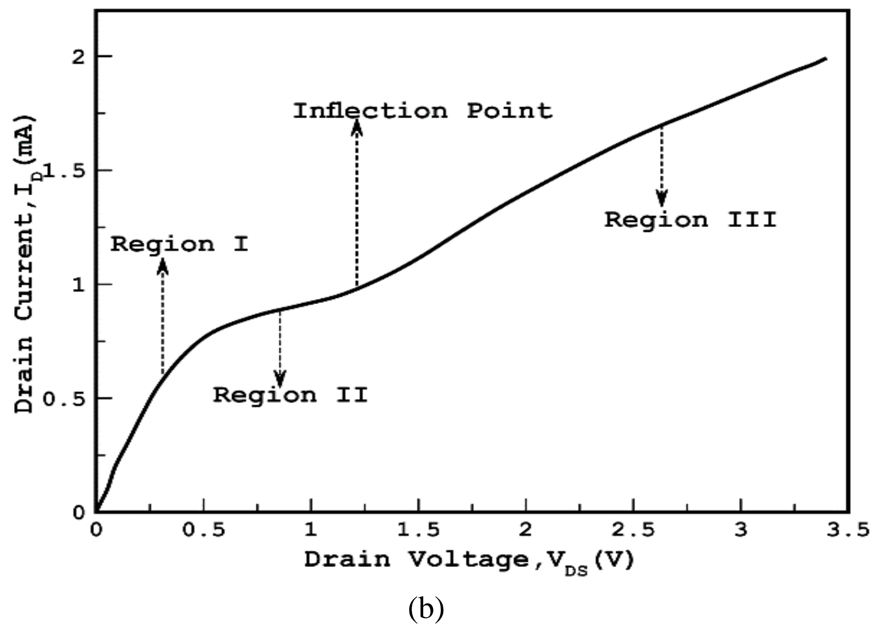


(a)



(b)

Fig. 3: *Characteristics curves obtained using ATLAS of SILVACO TCAD Tools. (a) Transfer Characteristics (b) Output Characteristics.*

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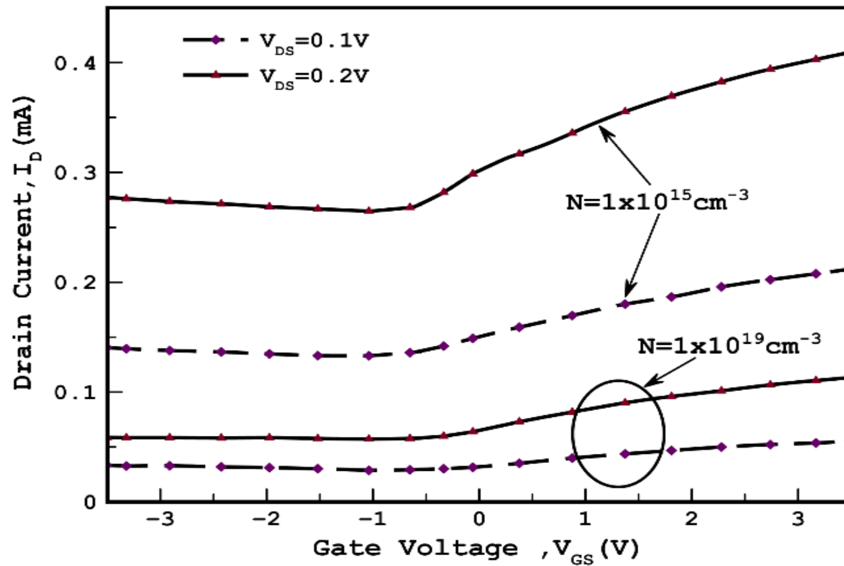

Fig. 4: *Effects of different channel doping level ($N = 1 \times 10^{15} cm^{-3}$ and $N = 1 \times 10^{19} cm^{-3}$) on the Transfer Characteristics (I_D vs V_{GS}) for two values of V_{DS}, namely $V_{DS} = 0.1V$ and $V_{DS} = 0.2V$.*

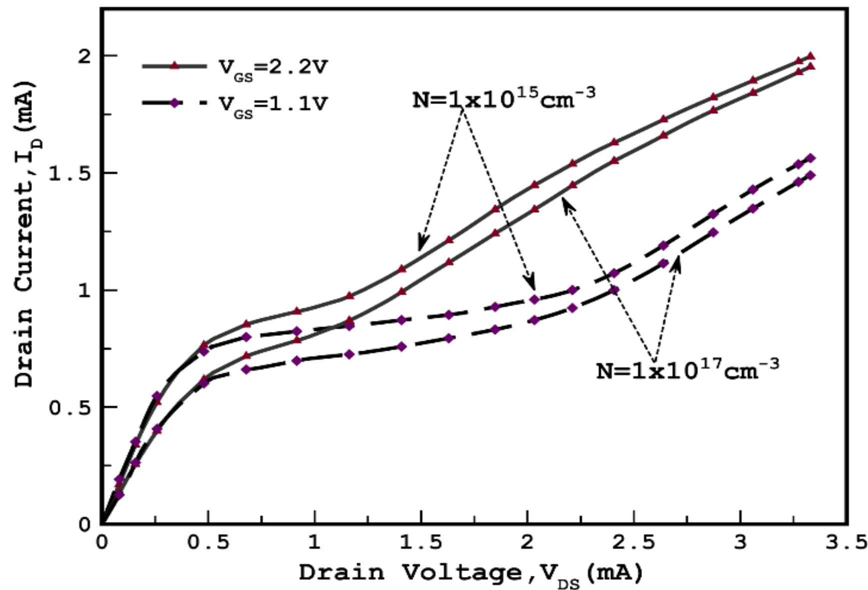

Fig. 5: *Effects of different channel doping levels ($N = 1 \times 10^{15} cm^{-3}$ and $N = 1 \times 10^{17} cm^{-3}$) on the ($I_D$ vs V_{DS}) Output Characteristics for two values of V_{GS}, namely $V_{GS} = 1.1V$ and $V_{GS} = 2.2V$.*

The effects of the channel doping levels on the characteristics curves are demonstrated in the Figs. (4) and (5). It has been observed from Fig. (4) that when the channel doping level is increased, the drain current is decreased. This is due to the fact that a larger portion of gate voltage is required to invert the channel for increased channel doping level and as a result, the drain current I_D decreases for higher doping levels. The same is also evident from Fig. (5). On the other hand, the

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increase of drain to source voltage (V_{DS}) causes electrons move with a higher electric field i.e. move at a higher pace and hence, results in an increase in the drain current. This increase due to increase of V_{DS} has also been observed in Fig. (4). However, from Fig. (4) it can be seen that the increase in the drain current for the positive gate voltages is higher than that for the negative gate voltages and especially, for higher doping levels, the drain current for negative V_{GS} becomes almost constant. Indeed, for larger doping levels and small $|V_{GS}|$, the increase in the majority hole accumulation in the p-channel when negative V_{GS} is applied is insignificant compared to the heavier channel doping levels and this makes the drain current almost insensitive to negative and smaller V_{GS}. Fig. (4) also shows that the inflection point for lower doping levels occurs at a lower V_{DS} than that observed for higher doping levels. This is expected. When doping level is low, lower positive top-gate voltage is required to accumulate electrons in the channel and hence, $V_{DS,crit}$ becomes lower as is evident from $V_{DS} > V_{DS,crit} = V_{GS-top} - V_0$ [3] where

$$V_0 = V^0_{GS-top} + \left(\frac{C_{back}}{C_{top}}\right)(V^0_{GS-back} - V_{GS-back}) \quad (1)$$

where superscript '0' indicates value corresponding to Dirac point.

Figs. (6) and (7) show the effects of the variation of the channel length on the characteristics curves of GFET. Both these figures show that the increase in the channel length decreases the drain current. This decrease is expected as the mobile carriers need to traverse a longer distance in the channel before reaching the drain for long channels. Two observations can be made from Fig. (6). The first one is that the drain current is almost constant for negative V_{GS}, which is expected as the channel doping level is higher. The second observation is that the change in drain current for changing drain to source voltage (V_{DS}) is greater when channel length is lower. From the stated condition of the Fig. (6), it can be pointed out the GFET is working in the first linear region of Fig. (7) and in this region, the increase in the V_{DS} causes a larger electric field for the short channels resulting in a larger change of drain current.

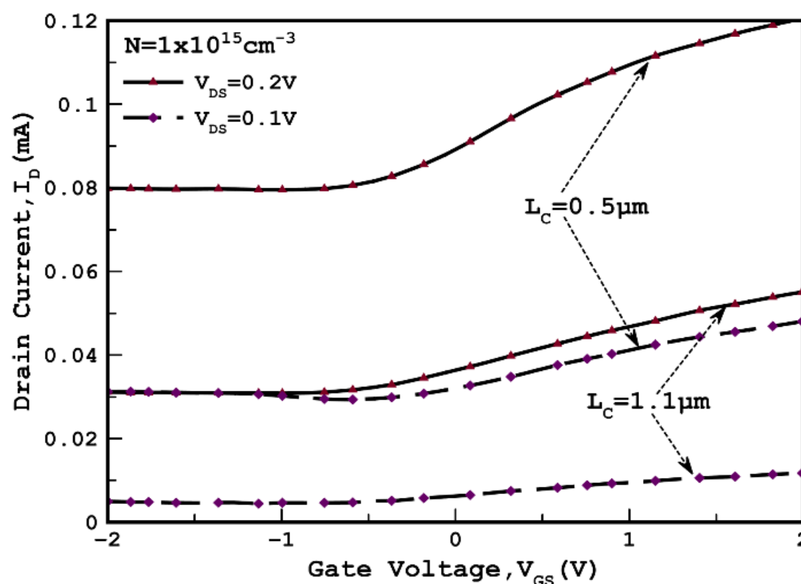

Fig. 6: *Effects of different channel length ($L_C = 0.5\mu m$ and $L_C = 1.1\mu m$) on the Transfer Characteristics (I_D vs V_{GS}) for two values of V_{DS}, namely $V_{DS} = 0.1V$ and $V_{DS} = 0.2V$.*

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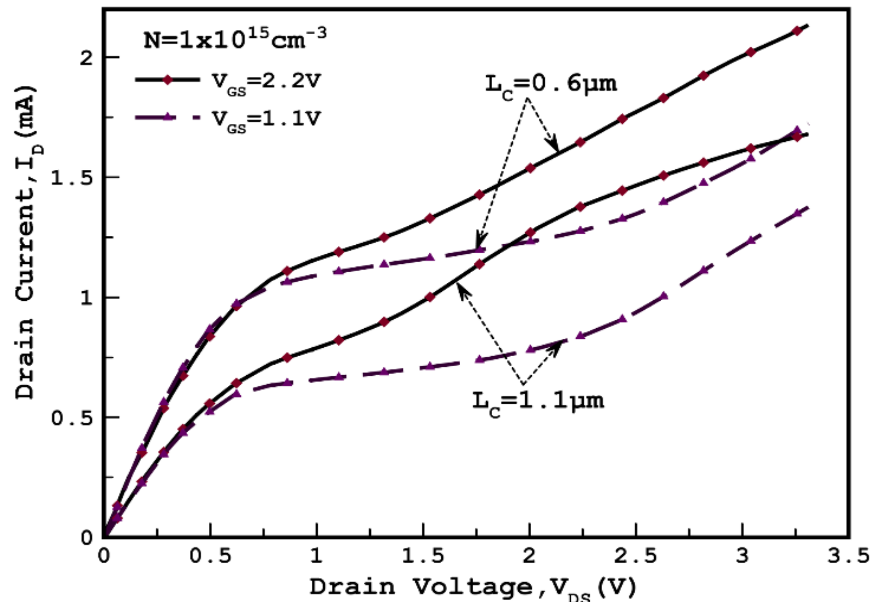

Fig.7: *Effects of different channel length ($L_C = 0.6\mu m$ and $L_C = 1.1\mu m$) on the output characteristics (I_D vs V_{DS}) for two values of V_{GS}, namely $V_{GS} = 1.1V$ and $V_{GS} = 2.2V$.*

CONCLUSION

A SILVACO TCAD based fabrication process and device simulation of a monolayer graphene field effect transistor has been performed in this work. The obtained characteristics curves are also analyzed physically. This work also show that for achieving higher drain current, channel doping level should be minimized and/or channel length should be reduced. Compared to the previous TCAD based simulations [9], this work provides better physical insight.

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