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Energy-Efficient Wireless Interconnect Design for Non-Destructive Testing (NDT) Applications

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Energy-Efficient Wireless Interconnect Design for Non-Destructive Testing (NDT) Applications

by

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Abstract

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A method for non-destructive, wireless testing of integrated circuits(ICs) is presented in this thesis. This system is suitable for applications which require testing after the manufacturing of ICs. According to Moore's Law the number of transistors in an IC doubles every two years, the current probing equipment will also have to reduce its size accordingly which will be difficult after a certain point. The proposed system relies on near field communication in order to transfer data between probe and device under test. The probe and IC will include small antenna and a transceiver circuit. The antenna and the transceiver circuit can be integrated into the device without affecting the real estate and performance. Major advantages of non-destructive probing include no damage to the pads of test chip, higher test frequencies and less maintenance which will lead to higher pin densities. The antenna and transceiver circuit to be incorporated on the test chip are completely CMOS compliant.

The presented system here is a prototype which consists of a transceiver circuit along with an ultra-wideband antenna. The system was implemented in IBM 180nm CMOS process. The transceiver circuit communicates at a high frequency of 21.5GHz which in turn reduces the area consumed by the antenna and the transceiver circuit. The results obtained for our system show that an energy efficient wireless interconnect has been successfully implemented for future non-destructive testing applications.

Acknowledgement

I would like to express my deepest gratitude to Professor Byun, my advisor for taking me as his student and training me. His patience and encouragement were valuable to me throughout the course of this research.

And finally, thanks to my parents and friends for their support and encouragement.

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Chapter 1 Introduction

1.1 Introduction

Printed Circuit Board(PCB) was introduced in early 20th century and have been a common method to integrate electrical systems. The PCB's were able to accommodate only a few discrete components. As the years passed, the complications of the circuits increased which necessitated the need to be able to accommodate as many circuits as possible. Later in mid-20th century advent of monolithic integrated circuits(IC) enabled smaller and more compact circuits. Additionally, the advancement in mass production enabled cheaper and more reliable IC's. Later, the discrete components were integrated on single chip needed for a system called system on chip [1]-[4] for maximum benefit of integration.

The testing of chips is also a vital part of the chip manufacturing process. Testing of a chip is performed through probes which are made to contact with the chip in order to test it. The chip which will have pads for contact, wear out eventually due to constant contact and pressure applied during testing. If the chip is damaged or worn out, repair and retest is not possible. This makes it necessary for us find a solution to test the chips in a non-destructive manner. And also as the size of the IC's shrink it is becoming tougher to test those physically as very small probes are required which indirectly increase the testing cost. The increase in consumer electronics has forced manufacturers to mass produce which makes it even more difficult to test every single chip with contact process. The risk of damage is also higher when contact is tried for internal circuit nodes, which don't have pads outside for testing. There have been earlier advancements in this field[[5]-[10].

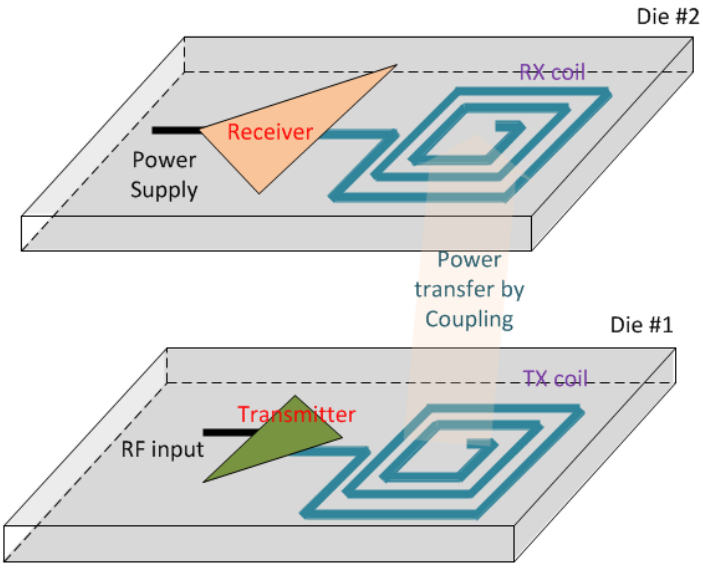


Figure 1.1: Concept of inductive coupling.

The drawback in IC design is that even as the channel length is reducing the pad size is the same as the older technologies because of the lack of appropriate probing systems. Fig. 1.1 tries to give the outline of concept of inductive coupling for power transfer [9]. The power is transferred through coil antenna as shown in figure through an inductive link formed between the transmitter and receiver. The data is also collected through the same inductive coupling link formed between those two. The proposed testing equipment has to be fast and low power consuming in order to maximize the performance. We have tried to introduce an alternative for this problem by introducing on-chip antennas for testing. We achieve that by embedding a RF transceiver in the circuits along with the antenna.

1.2 Thesis organization

The thesis is organized into six sections. The first one is about the transmitter, which will introduce about the transmitter components, their design and a few results to support their use in this system. The second one will introduce about on chip antenna, their design, results and how we used it in our system. The third one covers about the receiver part of the transceiver which will elaborate the functioning and design of components like Low noise amplifier, mixer etc. Later their results and layout will be shown after merging the transmitter

and receiver. The last section will shed some light on critiques, future scope and will conclude this thesis.

1.3 Contributions

In this work we tried to implement a system for Non-contact wireless testing of IC's in which my contribution will include designing the antenna which covers a wide range of frequencies used by the system designed. Including the fact that antenna covers a wide range of frequencies a new concept of manual metal fill was introduced in this antenna's design. Metal fill is usually done by the foundry when certain metal densities are not fulfilled. In this case, as it is a prototype and the frequency of the system chosen was not high enough, the antenna size was way much bigger than expected and metal fill was unavoidable for which the solution was to include the metal fill manually and we re-simulated the antenna to check for its results.

Chapter 2 RF Transmitter

2.1 Introduction

In a fundamental sense, communication is an action in which information is conveyed from one point to the other. When human beings are considered, this can be simply illustrated as a discussion among two people. There are number of various conversational experiences like face to face, over phone or email etc. Although it basic human interaction seems simple but they include analog (in electronic realm and biological definition) and digital types. Both types form relationship which is present everywhere among us. In this research we are just going to realize an RF transmitter which will be explained in detail in later sections.

RF Transmitter is a key block of any communication which includes sending required data to the receiver through a channel. The transmitter has to meet certain design requirements, in this case die size, efficiency of power use and voltage headroom. Basic transmitter design includes a VCO which generates the required frequency signal to carry the data, a modulator which modulates the data with the carrier signal and a power amplifier to boost the signal through the antenna. As transmitter is a vital part of establish a communication it justifies to explain in detail about conventional and prior works.

The Transmitter implemented and designed in this system works at 21.5 GHz frequency and uses amplitude modulation to modulate the data taken from an input buffer. Basic concepts of the VCO have been introduced with layout and results. VCO is followed by modulator and its results. In the last section a brief detail about the implemented power amplifier has been presented along with the layout and results. In the end a full layout of the transmitter including all the blocks has been shown.

2.2 VCO

A Voltage Controlled Oscillator generates an oscillated waveform whose frequency is varied with the DC input provided. Generally VCO's are characterized as harmonic oscillators and relaxation oscillators. The harmonic oscillators generate a sinusoidal waveform. Some examples include ring-VCO, LC-VCO etc. The LC-VCO uses LC tank to generate its signal whereas ring VCO uses positive feedback system. However, the relaxation oscillators generate saw-tooth or triangular waveform. They have three topologies: 1) emitter-coupled VCO's, 2) grounded-capacitor VCO's, and 3) delay-based ring VCO's. The harmonic oscillators are said to have good accuracy for frequency control over relaxation oscillators.

An oscillator has to generate stable periodic output while compensating any losses which is generally achieved by using negative resistance or positive feedback. For start-up of an oscillation the basic requirement is that in the system transfer function at least one pair of complex conjugate poles is in the right-half plane(RHP) [11]:

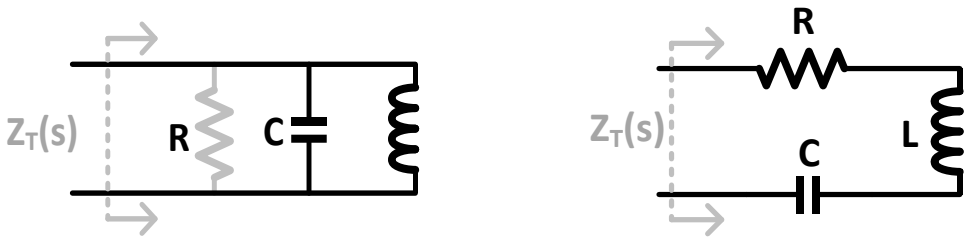
$$P_{1,2} = \alpha \pm j\beta \tag{2.1}$$

This requirement is not sufficient for steady state oscillation. When subjected to an excitation such as power supply, a system having poles as in (2.1) will exhibit a sinusoidal response growing exponentially:

$$x(t) = A \cdot e^{\alpha t} \cdot \cos \beta t \tag{2.2}$$

where, A is determined by initial conditions. The oscillation build up is governed by the exponential behavior later driving the system into a nonlinear regime which finally reaches a steady state mode of operation.

The implemented VCO uses LC-tank to generate the 21.5GHz signal which is fed to modulator in the following stages. The major objective of this section is to go over some fundamentals from textbook rather than focusing whole study on just VCO's to make it easier for a designer to be able to smoothly design a functioning VCO for the required system.



(a) (b)

Figure 2.1: (a) Parallel LC tank. (b) Series LC tank

2.2.1 LC-VCO

LC tanks, also referred as LC resonators consist of an inductor and a capacitor connected in parallel or series. The resonator losses are generally included by using resistive components, which in simpler form can be represented as shown in Fig. 2.1. The tank impedances of the circuits shown in Fig. 2.1 are:

$$Z_T(j\omega) = \frac{1}{\frac{1}{R} + j\,.\,(\omega C - \frac{1}{\omega L})} \quad (\textit{Parallel RLC}) \quad (2.3a)$$

$$Z_T(j\omega) = R + j\,.\,(\omega L - 1/\omega C) \quad (\textit{Series RLC}) \quad (2.3b)$$

The reactive terms in (2.3) above cancel out resonance frequency:

$$\omega_o = 1/\sqrt{LC} \quad (2.4)$$

At ω_o, the impedance is resistive and is equal to R, whereas the phase response is exactly zero. In parallel RLC for frequencies below ω_o the impedance is inductive and for above ω_o it is mainly capacitive. The series RLC circuit behaves opposite to parallel RLC circuit. Magnitude and phase of LC tank impedance for series and parallel configurations is shown in Fig. 2.2 [11].

The resonator's quality factor, Q, indicates the ability to retain energy after considering various losses present in the elements. It helps in determining the phase noise performance of

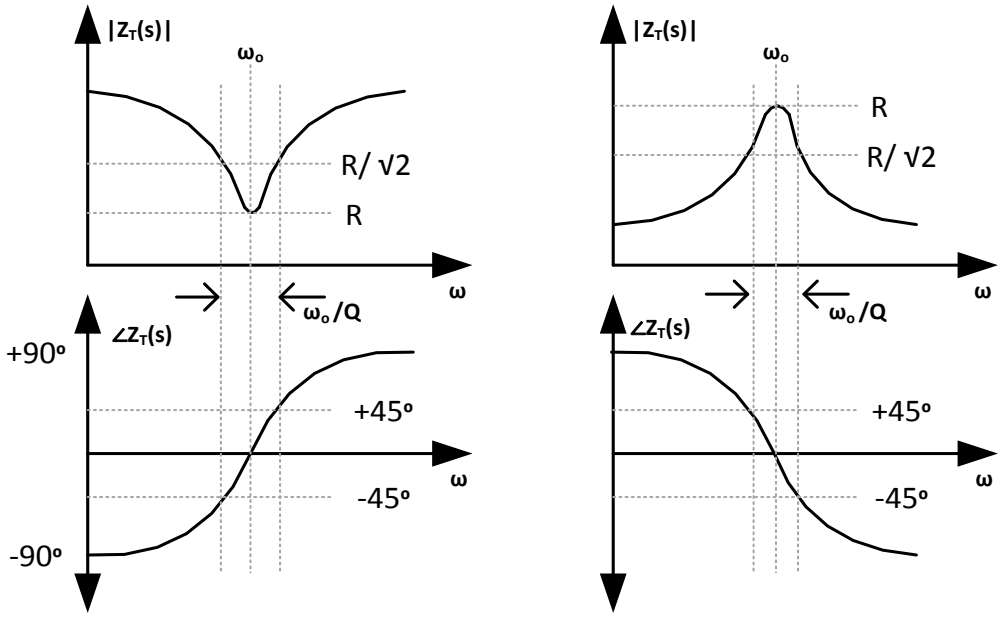


Figure 2.2: Magnitude and phase of LC tank impedance for (a) Series and (b) Parallel configurations.

LC-VCO's. In general, Q of a network is defined as:

$$Q \equiv \omega \cdot \frac{Energy\ stored}{Average\ power\ dissipated} \tag{2.5}$$

And alternatively, Q can be expressed as:

$$Q = \omega_o/\Delta\omega_{-3dB} \tag{2.6}$$

where $\Delta\omega_{-3dB}$ is the -3dB bandwidth of the impedance response. Thus, sharper impedance response is achieved from larger Q value and greater rejection of spectral energy away from ω_o.

Generally, the most common type of VCO used is the tail biased cross coupled topology. As mentioned earlier the purpose of this thesis is not to focus on VCO rather it is the system, previously implemented VCO in [12] was used here. As seen in Fig 2.3, this topology is differential which is preferred as differential operation is known to suppress the common mode

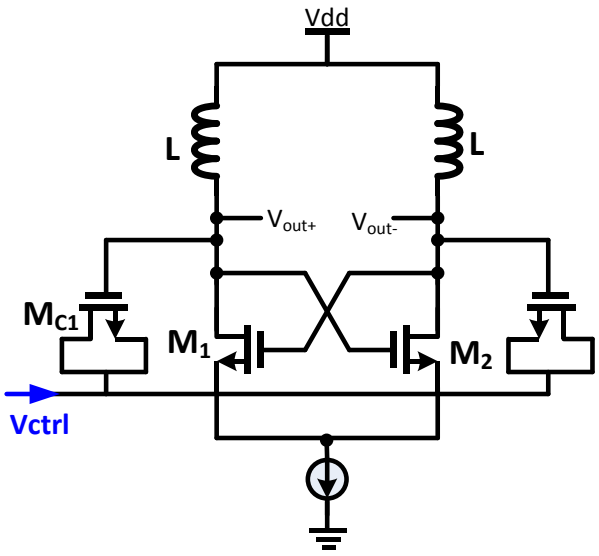


Figure 2.3: Complete schematic of the LC-VCO used in this system

disturbances when share the same substrate. Cross coupling of the active devices which is positive feedback configuration used to damp the negative resistance found to be $-1/g_m$, which are introduced from inductor and capacitor. This assumes that both transistors have same W/L ratio and must be true to achieve equal output resistance. And also from [13], the LC tank provides a phase shift of 180° which is then added to the 180° phase shift contributed by the half circuit common source. Now to determine natural frequency of oscillation, as the circuit is symmetrical we use the half circuit small signal equivalent which is illustrated in Fig. 2.4 [12]. Now by using KVL at V_{out} and V_L we get:

$$g_m V_{in} + \frac{V_{out}}{r_o} + sCV_{out} + \frac{V_{out}-V_L}{R} = 0 \tag{2.7a}$$

$$\frac{V_L-V_{out}}{R} + \frac{V_L}{sL} = 0 \tag{2.7b}$$

After solving for transfer function we get:

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m r_o s(R_p+sL)}{s^2 r_o CL + s(L+r_o CR_p) + r_o + R_p} \tag{2.8}$$

Where, R_p represents the parasitic resistance from the capacitor and inductor. Now we substitute s with jω and we can ignore imaginary parts as we are only concerned with real part.

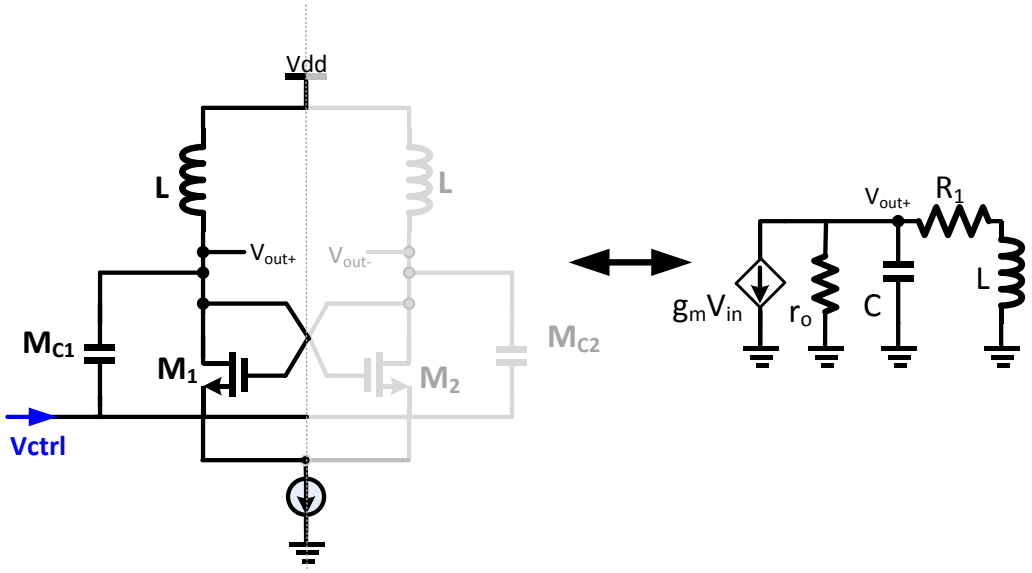


Figure 2.4: Half circuit small signal equivalent of LC-VCO

Additionally, if we assume $r_o >> R_p$, r_o becomes the dominant factor of the resistances. Now we can solve for natural frequency, we get:

$$-\omega^2 r_o CL + r_o = 0 \tag{2.9}$$

and solving more for ω, we receive:

$$\omega = \frac{1}{\sqrt{LC}} \tag{2.10}$$

The following section will shed some light on inductors used in standard 180nm CMOS process.

2.2.2 Inductor

Inductors in CMOS technologies have been a hot topic from past decade as they play an important role in any analog circuit. Traditionally, inductors implemented in IC technologies have not been good quality as compared to off-chip inductors because of metal layer trace resistance, eddy currents in the substrate, and power losses in substrate coupled between metal and substrate [14]. However, the cost and area constraints of off-chip inductors encourage on-chip inductors in RF transceivers. A basic requirement of any inductor is quality factor, in our case, a quality factor of 10 or more is considered good for using in our system. The circular spirals provide higher Q than square and octagonal spiral structure but due to

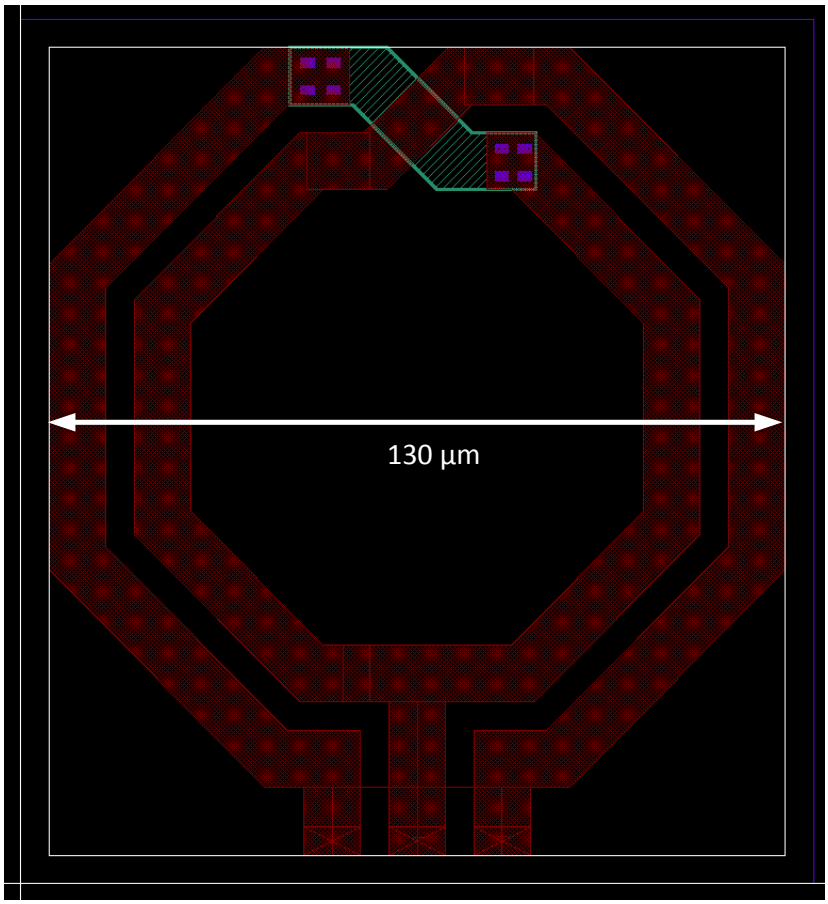


Figure 2.5(a): Inductor layout in Cadence used for our VCO

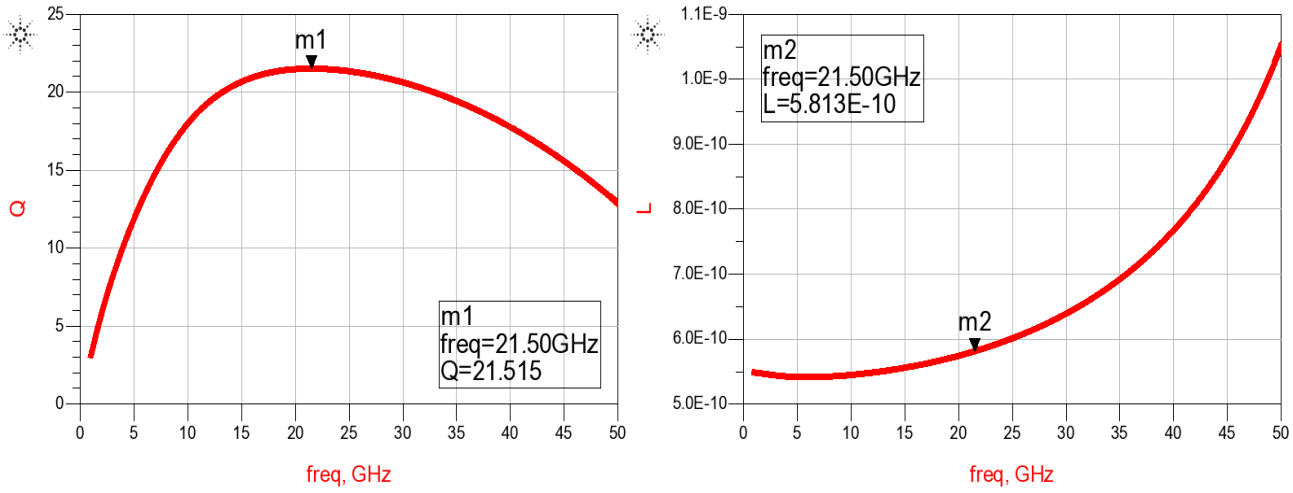


Figure 2.5(b): Shows the simulated Q value(left) and L value(right) of the inductor used

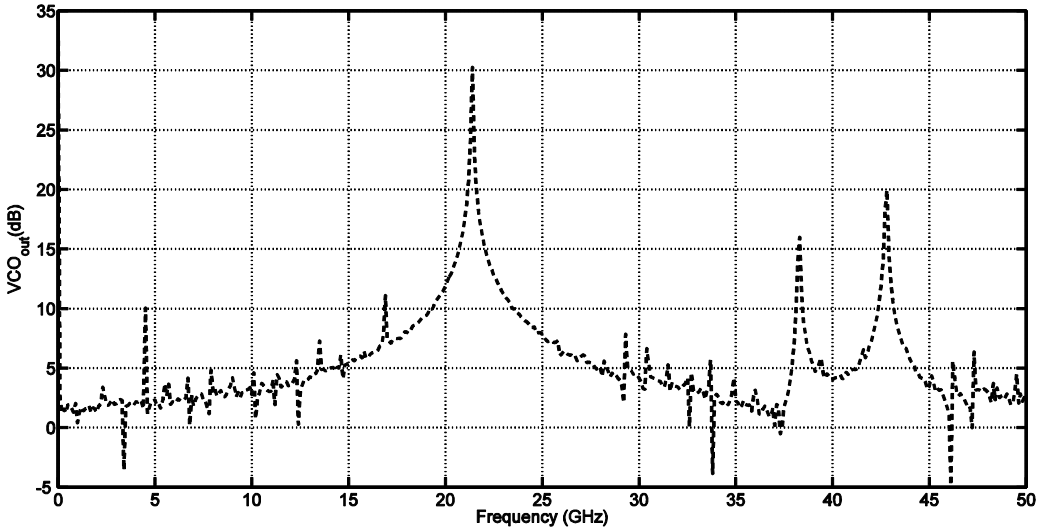


Figure 2.6: Simulated Output spectrum of VCO after RC Extraction

fabrication constraints from foundry, design rules of not able to support circular shape, octagonal spirals are next best alternative [15].

In the IBM 180nm process, which is a six metal layer process, we have chosen top most layers i.e; metal layer 5(green) and 6(red) to implement the inductor. The thickness and parasitic capacitance of the conductor plays a key role in deciding the quality factor(Q) of the inductor. The top layer is thickest among all the six layers with a thickness of 4µm which help reduce resistive losses and also has lower parasitic capacitance to the substrate. The top layer was used to design the coil of the inductor, whereas the metal layer 5 was only used to cross over to inner turns. A center tap was introduced in the middle to avoid using two inductors as in reality. Fig. 2.5a shows the inductor layout used for our VCO and Fig.2.5b shows the Q and inductance(L) value of the inductor used. It should be noted that thickness, width, space between conductor and turns, all play a significant role in varying the Q and L value of the inductor. The best inductor values were used in the whole system only after considering the above factors.

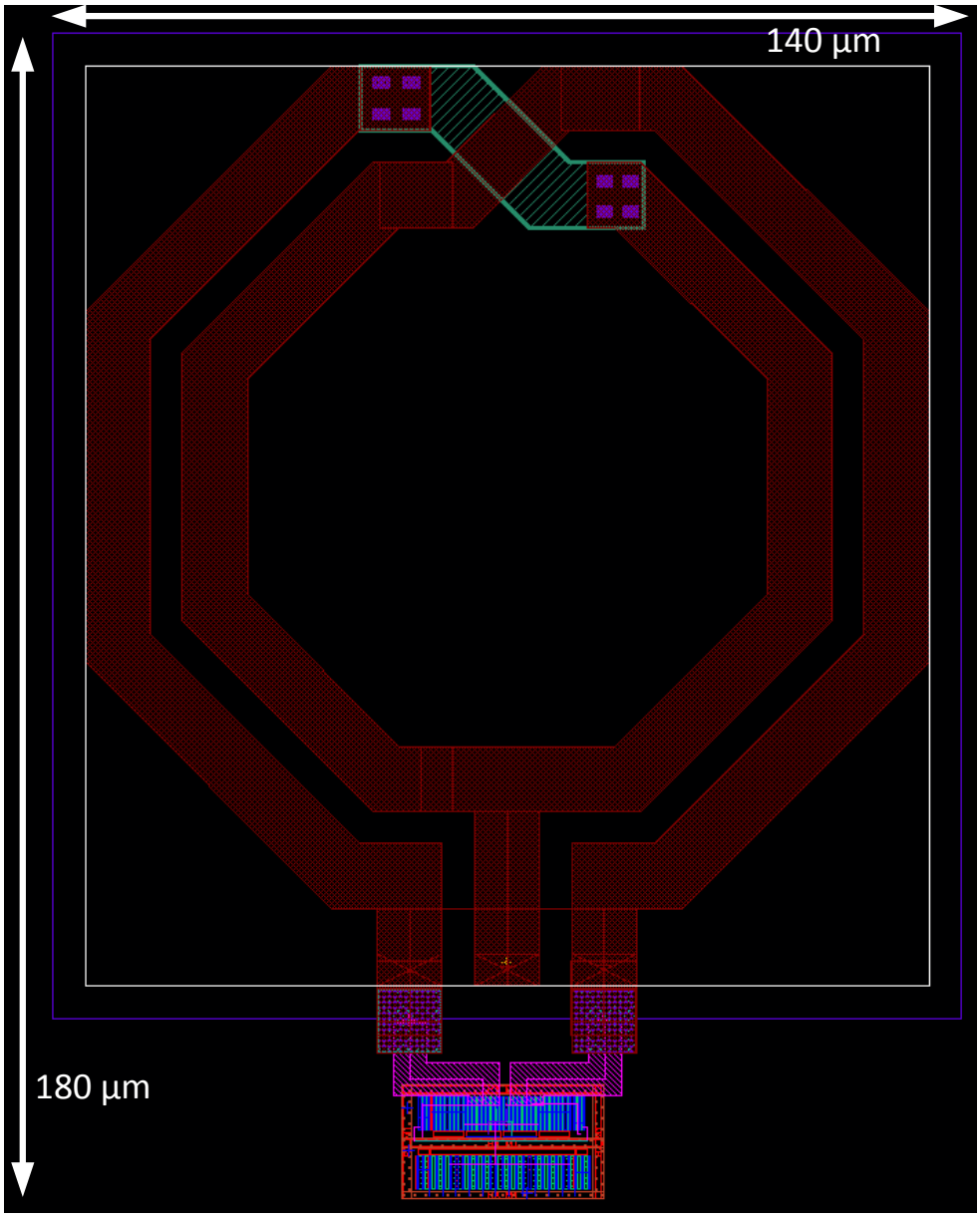


Figure 2.7: Final layout of the whole LC-VCO used in our system with dimensions

Layout and Result

The output spectrum of the VCO when simulated using schematic showed it's frequency at 24.6GHz. Later, when the VCO was re-simulated with layout, the frequency came down to 21.5GHz (Fig2.6). Fig. 2.7 shows the final layout of the whole LC-VCO used in our system with dimension. The VCO takes 1.8V from the power supply and consumes 11.25mW power.

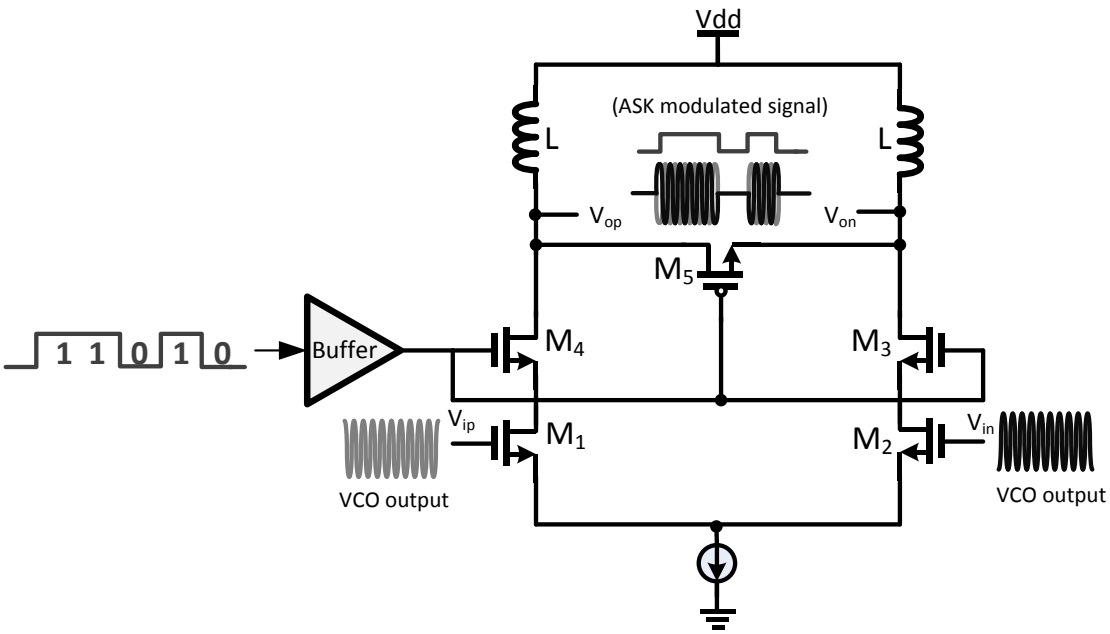


Figure 2.8: ASK modulator FET configuration

2.3 Modulator

Recent years have made radio spectrum extremely valuable due to increased demand for wireless communication. The data is transmitted in a way that it will occupy very little spectrum while maintaining the desired quality. However, complexity of the circuit in implementing is another factor which is inversely proportional to cost savings. Therefore, a trade-off can be expected between efficiency and complexity.

When low-frequency baseband signal is converted into a high-frequency band-pass signal, the process is called as modulation. A way to represent a modulated signal is:

$$x(t) = a(t).\cos[2\pi f_c t + \phi(t)] \qquad (2.10)$$

where, a(t) is the amplitude of the signal, f_c is the center frequency and $\phi(t)$ is the phase of the signal. Both amplitude and phase may contain the required information if the modulated signal is centered at f_c. If a(t) is time varying and $\phi(t)$ is fixed then it's amplitude modulated and if the reverse is true then it is angle modulated which include frequency modulation and phase modulation.

2.3.1 ASK modulator

ASK modulator implementation can be considered the easiest in CMOS configuration. The basic principle includes, the output will be high if the data provided is high and opposite otherwise. Fig. 2.8 shows the FET configuration of the implemented ASK modulator for this system [16]. The data is fed from the input buffer to the modulator which usually controls the signal for the later stages. The input from VCO is provided to transistors M_1 and M_2 from the free running VCO previously designed and is controlled by the data from the buffer provided at transistors M_3 and M_4. The current bias circuit of two transistors is connected for providing bias to the modulator (not shown here). Transistor M_5(PMOS) is connected across the output terminals which are fed to an inductor. The same inductor which was designed previously for the VCO was used in order to maintain stability between VCO and modulator. Again, the inductor here has a center tap which is connected to the power supply to be given to the modulator. For best results of the modulator, one should test the modulator and VCO together while optimizing the modulator for best results. Furthermore the designer has to ensure that output signal at the modulator is at the carrier frequency and also spurious harmonics do not interfere. But, as previously mentioned our focus is not only on the modulator which makes this design a better alternative than complicated designs consuming less power.

Layout and results

Fig. 2.9 shows the layout used for this system including the inductor and shows that this modulator is very area convenient. The modulator consumes 6.07mW of power from a power supply of 1.8V.

2.4 Power Amplifier

Power amplifiers are usually the output stage of the transmitter. Basically, they are classified into two main types: current mode and switching mode. The ultimate goal for designing the best power amplifier will be to have highest degree of linearity along with maximum efficiency, but both are inversely proportional. Switching mode PA's have high efficiency whereas current mode PA's are known to have good linearity. Non-linear power

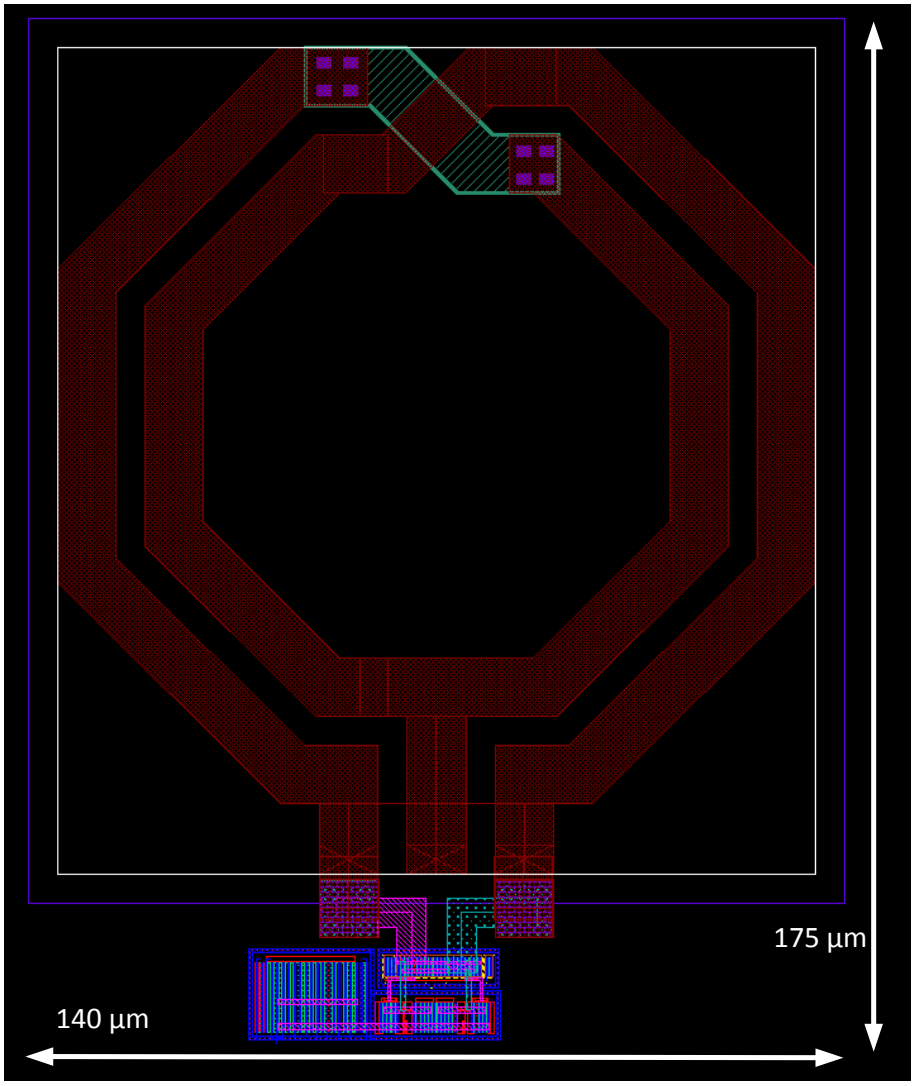


Figure 2.9: Layout of modulator.

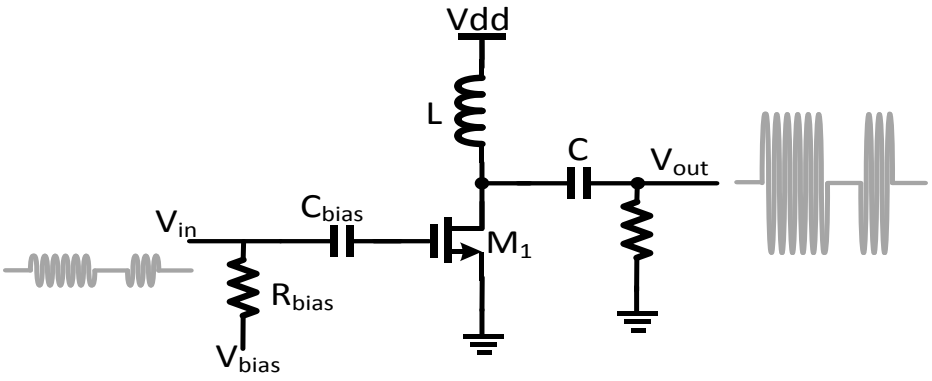


Figure 2.10: Circuit implementation of the power amplifier used.

amplifiers offer greater efficiency and simplicity than linear power amplifiers. The current mode PA varies according to their conduction angle. The power efficiency improves as the conduction angle decreases but the linearity declines as well. The class of power amplifier is mostly chosen according to the application of the system. In our system the communication range is in millimeters which make the power amplifier efficiency less important than its linearity which led us to choose class A amplifier for our system.

2.4.1 Class A power amplifier

Fig. 2.10 above shows a class A amplifier designed and implemented for this system. In this class of amplifier, the current always flows through the transistor as it is biased in active region for entire input cycle, which ultimately results in lower power efficiencies. It has a conduction angle 360° i.e; bias point is located in the middle of IV curves and the signal is amplified during full signal period. A standing bias current flows during the whole waveform cycle even if no amplification is taking place. The maximum attainable efficiency from a class A power amplifier is only 50%.

The modulated output signal is fed to the power amplifier at the gate of transistor M_1. An external bias was connected between modulator output and power amplifier input to control the common mode of the input to the power amplifier for better efficiency of the power amplifier. The power amplifier showed a gain of 19dB at 23.9GHz. The output from the power amplifier was fed to the antenna through the matching network connected to avoid return loss and to allow smooth flow of signal from power amplifier to the antenna.

Layout and results

Fig. 2.11 shows the layout of the implemented class A amplifier along with the inductor which was used in VCO and modulator both. Fig. 2.12 shows the plot of the simulated gain of the power amplifier. The power amplifier has a power supply of 1.8 V and consumes 19.1mW of power in order to work efficiently. And finally, fig. 2.13 shows the complete layout of the transmitter(antenna not included).

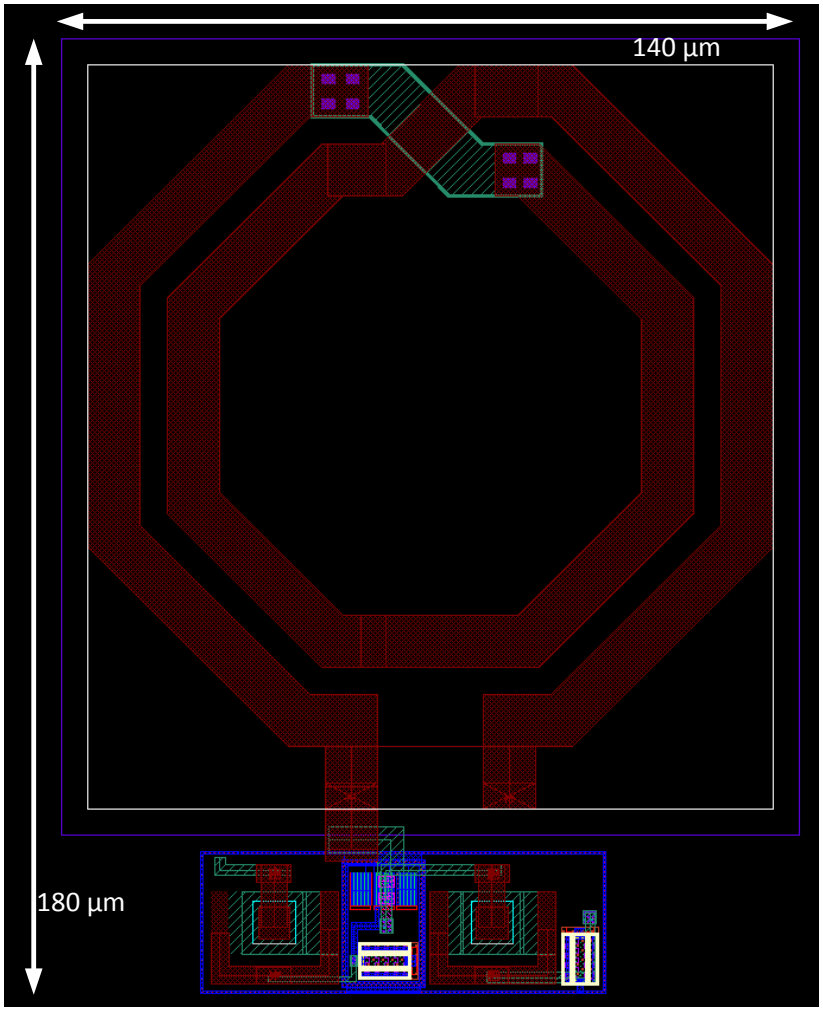


Figure 2.11: Layout of the implemented power amplifier for this system

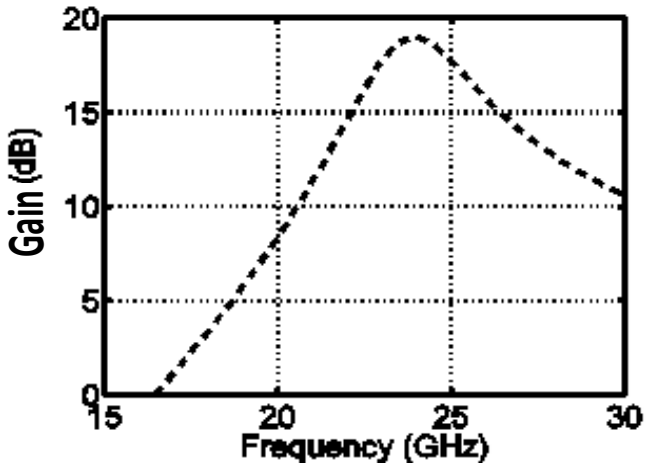


Figure 2.12: Simulated gain of the power amplifier

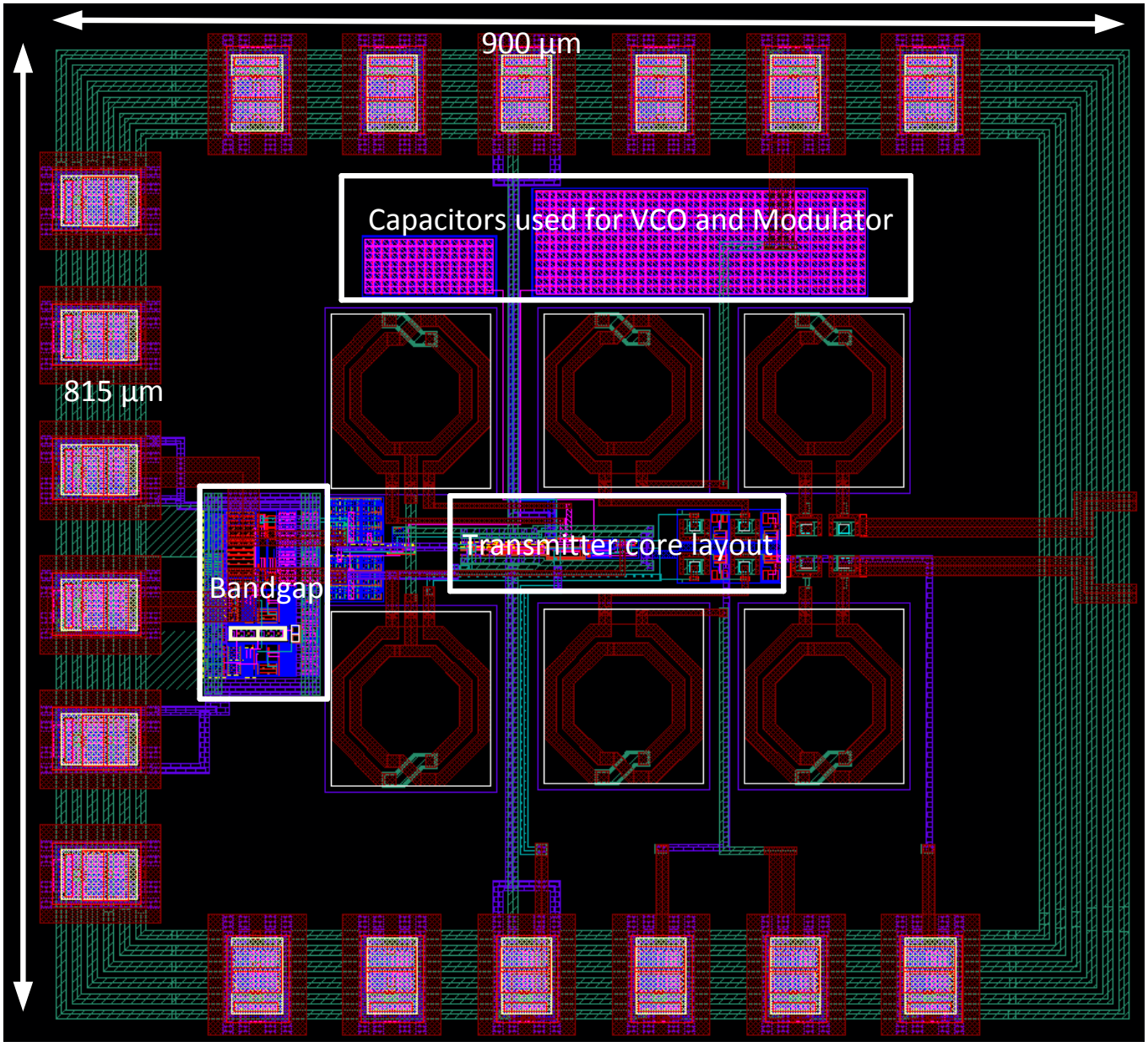


Figure 2.13: Layout of the transmitter being used in this system, with dimensions

Chapter 3 Antenna design

3.1 Introduction

This chapter will deal with the most important component of our system. For non-contact interconnect system, antenna design is the key. The data sent is to be received but the communication distance is relatively smaller than other applications i.e; we require the antenna to work at around 1mm distance which is just before the contact to the surface while testing.

First we will introduce some of the major concepts briefly required while designing an antenna. Later sections will show the designed and implemented antennas with their design parameters and results. In the end we will introduce matching and will show the implemented matching circuit designed for this system.

Antenna Parameters

Antenna parameters are used to determine the performance of the antenna. Terms like bandwidth, radiation pattern, return loss, antenna impedance and gain, which are discussed below.

Bandwidth

Bandwidth is a rudimentary antenna parameter. It specifies the region in frequency within which the antenna parameters, such as gain, return loss, radiation pattern etc. are within acceptable range from those at the center frequency. Bandwidth is often the determining parameter for the antenna and also helps to decide upon which antenna to prefer. For

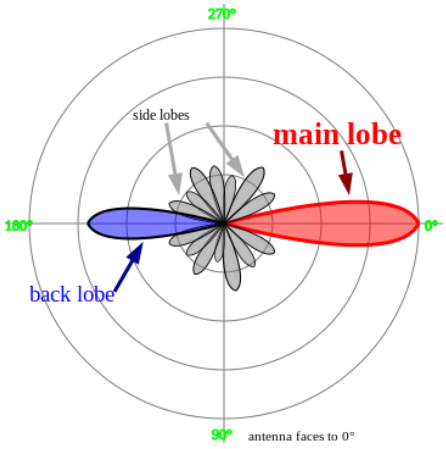


Figure 3.1: Diagram of antenna side lobes

instance, narrowband antenna cannot be used where a system needs to work over a wide range of frequency i.e; for wideband operation.

Return loss

Return loss(RL) is an important parameter for an antenna and is used to measure the effectiveness of the signal which is transferred from source to the antenna. The return loss can be defined as the ratio of the incident power(P_{in}) over the reflected power(P_{ref}) back from antenna to the source and can represented as:

$$RL = 10 \log_{10} \frac{P_{in}}{P_{ref}} (dB) \quad (3.1)$$

Typically, return loss is calculated over a range of frequencies of an antenna to get a good representation of its radiating properties. For good power transfer, RL should be high. If it is low, standing wave phenomena's occur(resonances) and will end up in a frequency ripple of gain etc. In practical, RL value of about -10dB is acceptable.

Radiation Pattern

Radiation pattern is the most common term used to describe the antenna. It is "the spatial distribution of a quantity that characterizes the electromagnetic field generated by the antenna"(IEEE,1993). Radiation pattern can help selecting the antenna needed according to the application. For instance, omnidirectional antenna will be required for cell phone use as the

user's location is not fixed which necessitates sending the signal in all directions for optimal reception. 3D radiation patterns are represented on spherical coordinate system indicating radiation power strength surrounding the antenna. Fig. 3.1 shows the diagram of antenna side lobes [17]. It illustrates how the energy of EM waves is emitted from an antenna.

Antenna impedance

Antenna impedance is a complex number which helps while matching the antenna so that the small antennas are able to resonate. Antenna is said to be resonating and radiating when the imaginary part is zero or almost zero. Usually while designing the antenna the complex part is varied and tried to reduce with the help of inductors and capacitors. We can tell about antenna behavior from the real and imaginary part of impedance when we use them as a function of frequency.

Directivity and Gain

Directivity defined by IEEE is "the ratio of the radiation intensity in a given direction from the antenna to the radiation intensity averaged over all directions". Mathematically, directivity can be expressed as :

$$\mathrm{D} = \frac{\omega}{p_t/4\pi} = \frac{4\pi|E(r)|^2}{\int |E(r)|^2 \, d\Omega} \tag{3.2}$$

where, ω is radiation density per solid angle and p_t is total power transmitted by the antenna and is also the solid angle [18].

The antenna gain is related to radiation efficiency through directivity of the antenna. The antenna gain can be defined as the radiation intensity in the beam direction and the total power delivered to the port of antenna. Gain can be expressed as:

$$G = e_{rad} e_{pol} D \tag{3.3}$$

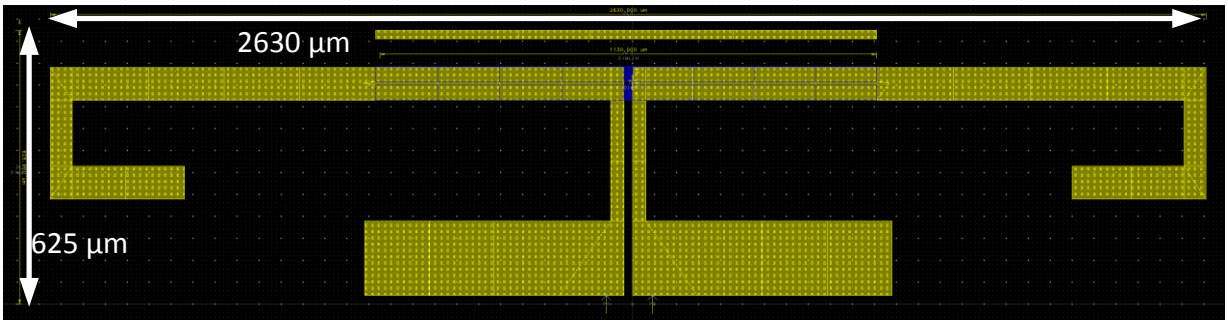


Figure 3.2: Yagi antenna used for initial simulations in ads(metal fill not shown)

Where e_{pol} is the total polarization efficiency and e_{rad} is the total radiation efficiency. Higher the value of gain, it represents higher the directivity of the antenna.

3.2 Narrowband Antenna

The narrowband antenna was designed and implemented for this system. Yagi antenna which is a narrow bandwidth antenna was simulated in ADS. Fig. 3.2 shows the Yagi antenna design which was used for simulation in ADS. The Yagi antenna consists of three elements which include a driven element, a directive element and a reflector. The antenna is totally 2630µm in length and 625µm in width. Fig. 3.3 shows the substrate file which was used in ADS to represent the 6 metal 180nm CMOS process for simulations. Fig. 3.4 shows the layout of the antenna in Cadence which was used in the system. Fig. 3.5 shows the return loss plot of the antenna. The top metal layer was used to implement the antenna's driven element and director. The reflector was placed under the metal and was made of metal 1. The top layer was chosen for its thickness and resistance and its closeness to the surface for required emission. Finally, fig. 3.6 shows the radiation pattern of the antenna.

The antenna was simulated with chunks of other metals. This was done due to foundry constraints of IBM 180nm CMOS process. The empty space around the antenna will be filled with metal 1 to metal 5 as a fabrication requirement. This design was not used in our system as later we designed UWB antenna which looked more promising for this application.

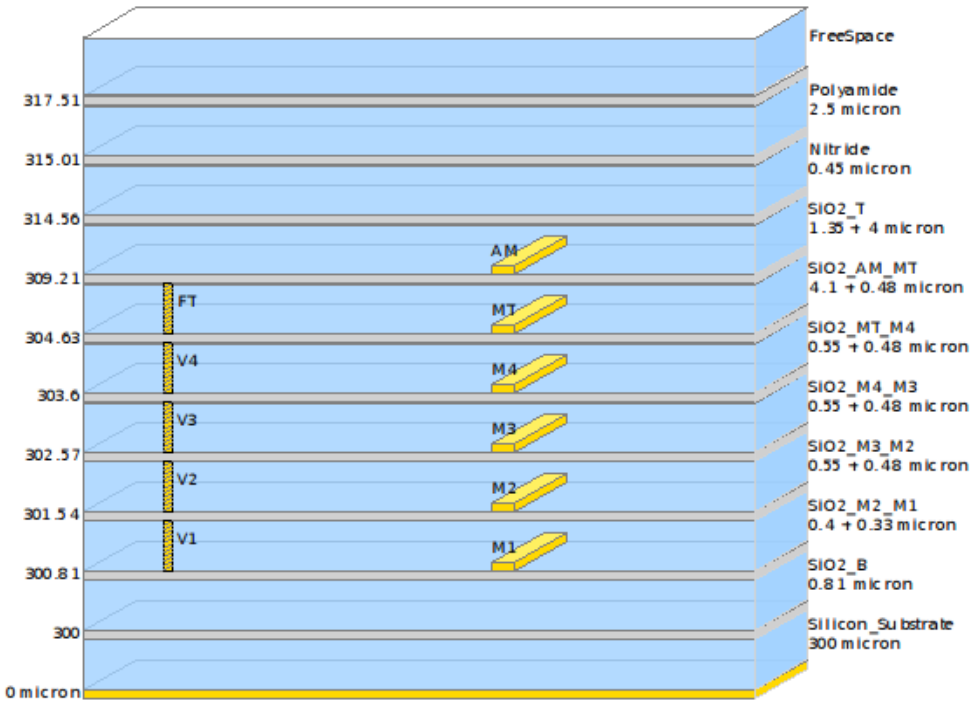


Figure 3.3: The substrate file used in ADS to represent the 6 metal 180nm CMOS process for simulations.

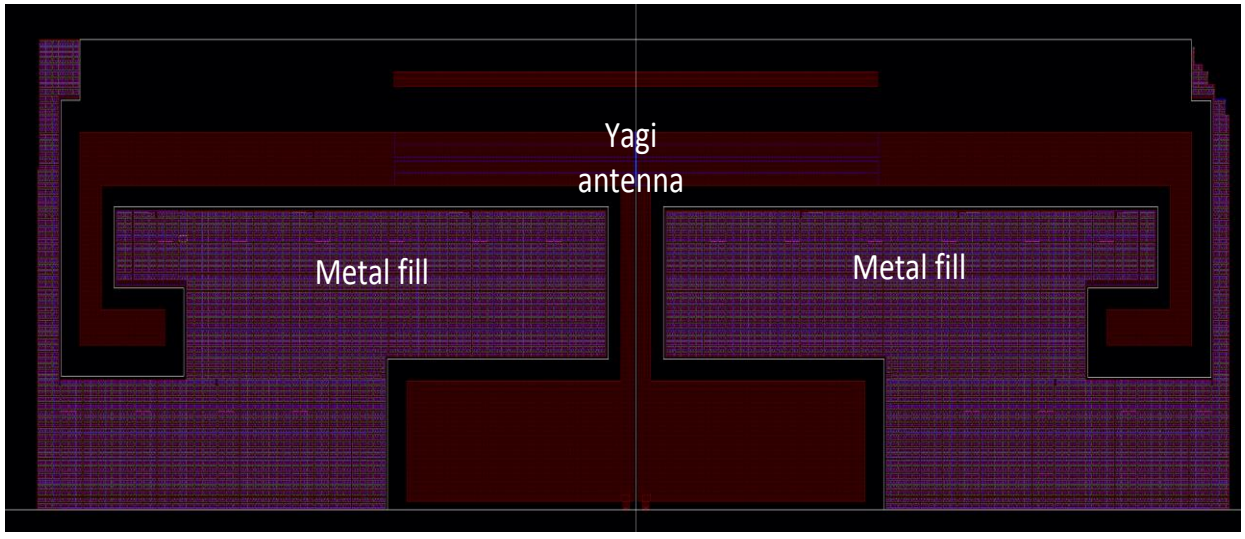


Figure 3.4: Complete layout of the antenna implemented in Cadence including metal fill.

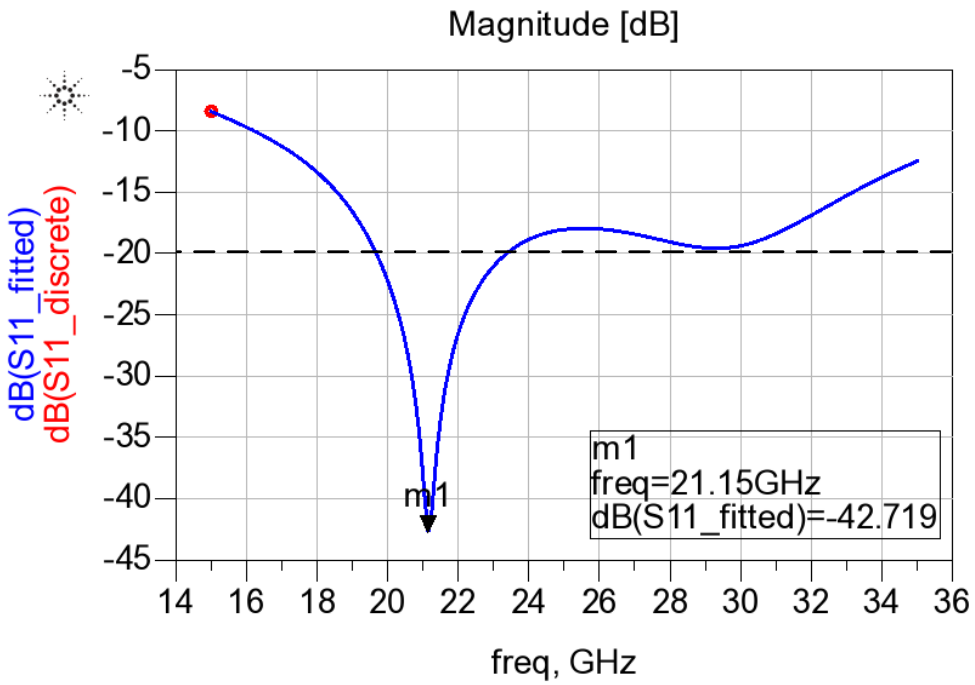
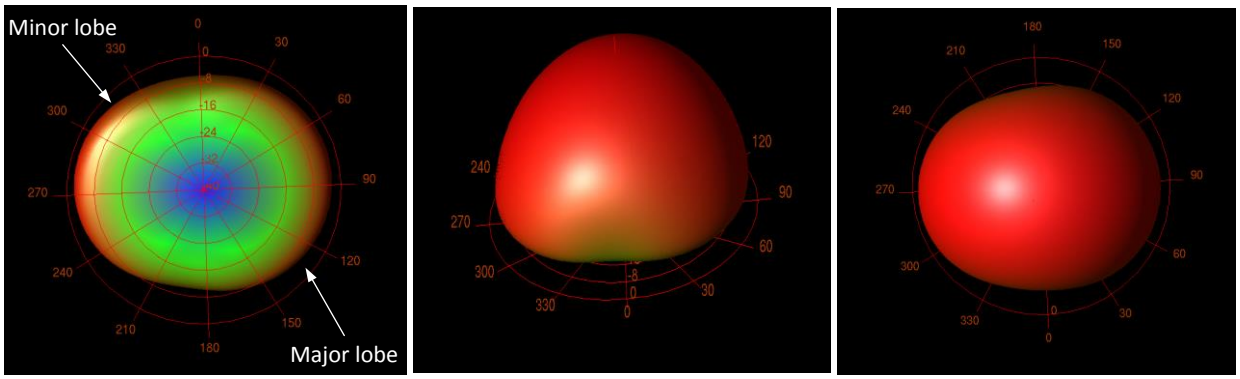


Figure 3.5: Simulated return loss(S11) plot for the Yagi antenna simulated in ADS.



(a) (b) (c)

Figure 3.6: Simulated Radiation pattern of Yagi antenna shown from a) bottom, b) side, and c) top view.

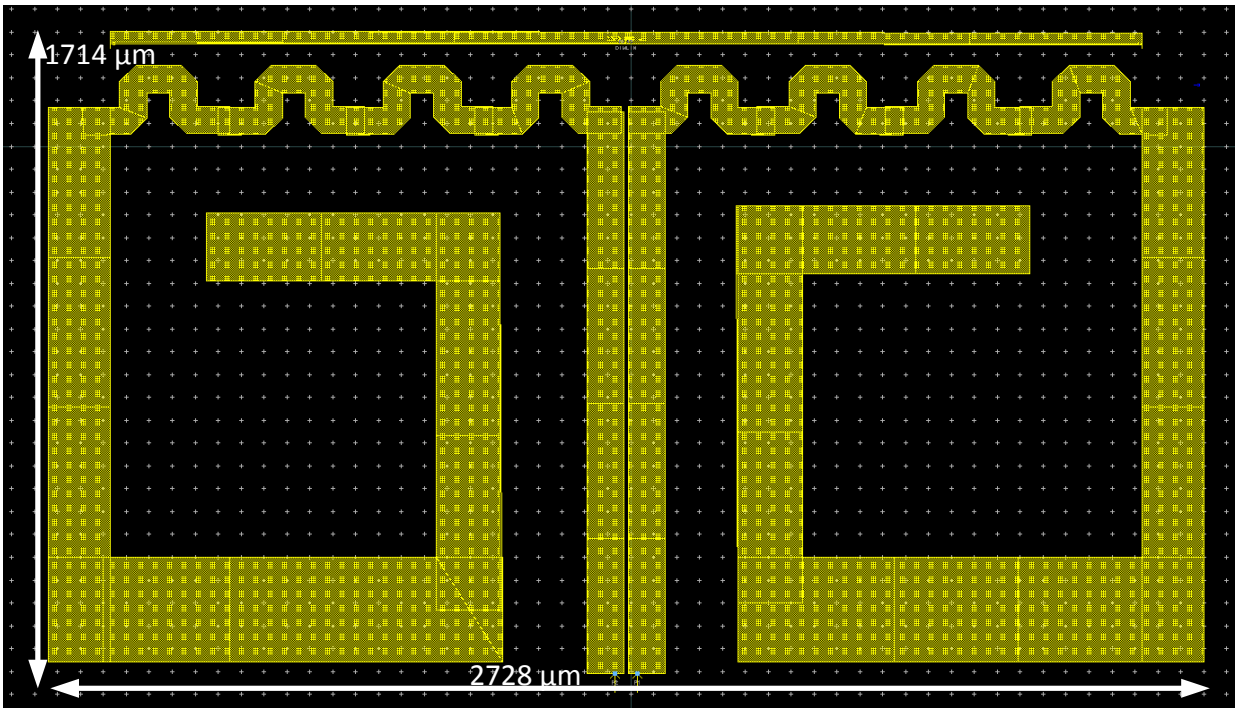


Figure 3.7: Design used in ADS to simulate for UWB antenna.

3.3 Ultra-Wide Band Antenna

Ultra-wide band antenna was designed for this system. This antenna was also simulated in ADS with the same substrate file mentioned earlier. This design was chosen over Yagi antenna in our system as it covers a wide range of frequency from 14GHz – 30GHz. Fig. 3.7 shows the design which was used for simulations in ADS. The antenna is 2728µm in length and 1714µm in width. Fig. 3.8 shows the layout of the antenna made in Cadence. Again the top metal was used in order to implement the design. Fig. 3.9 shows the return loss plot for this antenna in which it can be observed that the antenna shows return loss of <-20dB over almost 15GHz frequency range. Typically, a return loss of -10dB is acceptable as mentioned earlier. Fig. 3.10 shows the radiation pattern of the antenna.

The antenna was again simulated with additional metal pieces around it because of foundry restrictions of not having empty space. Fig. 3.11 shows the S21 or gain plot of the antenna.

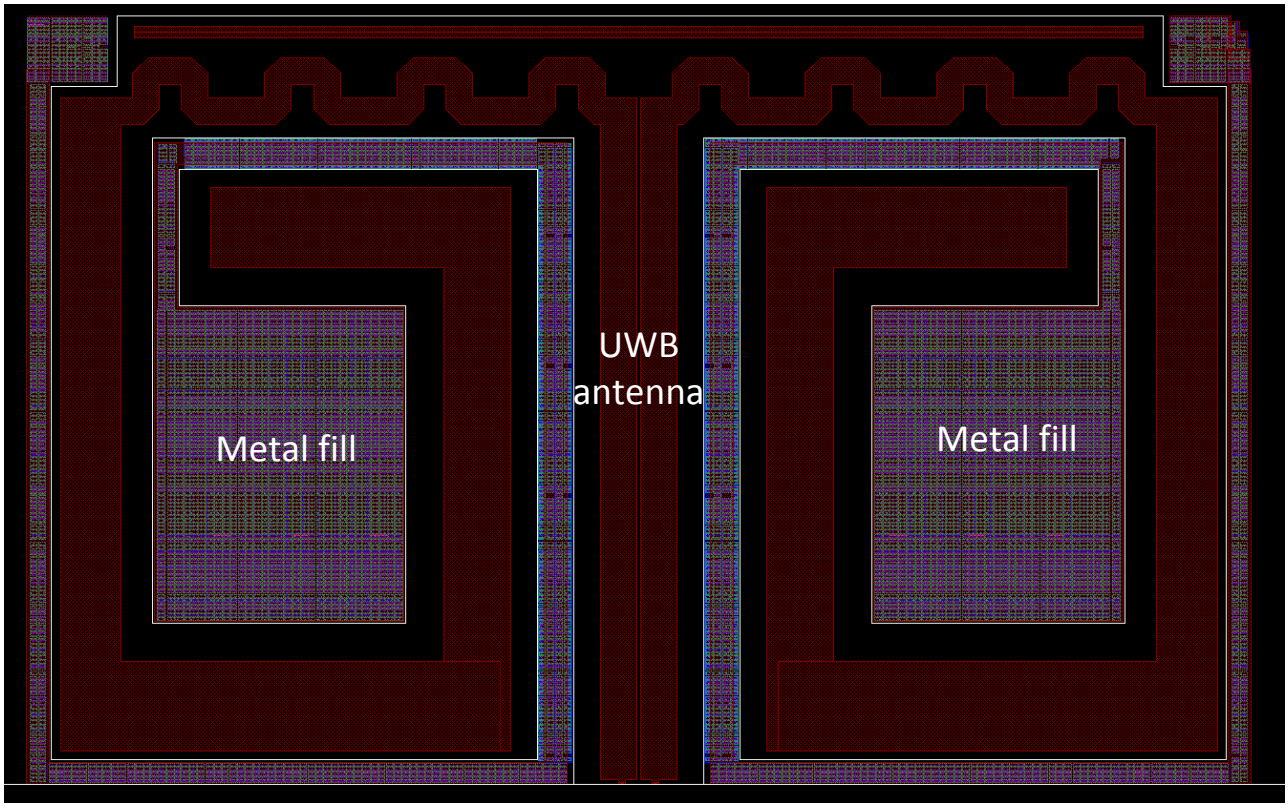


Figure 3.8: Layout of UWB antenna designed in cadence for this system.

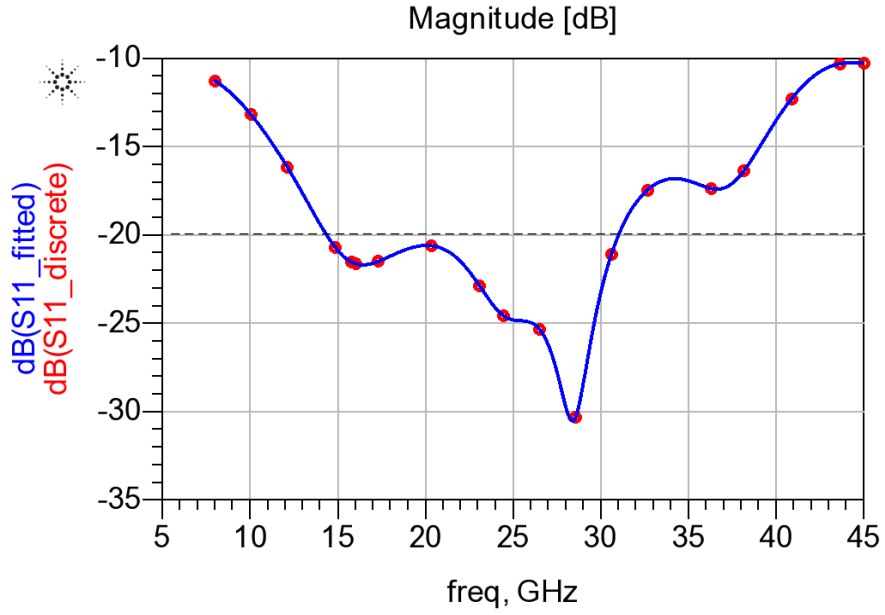
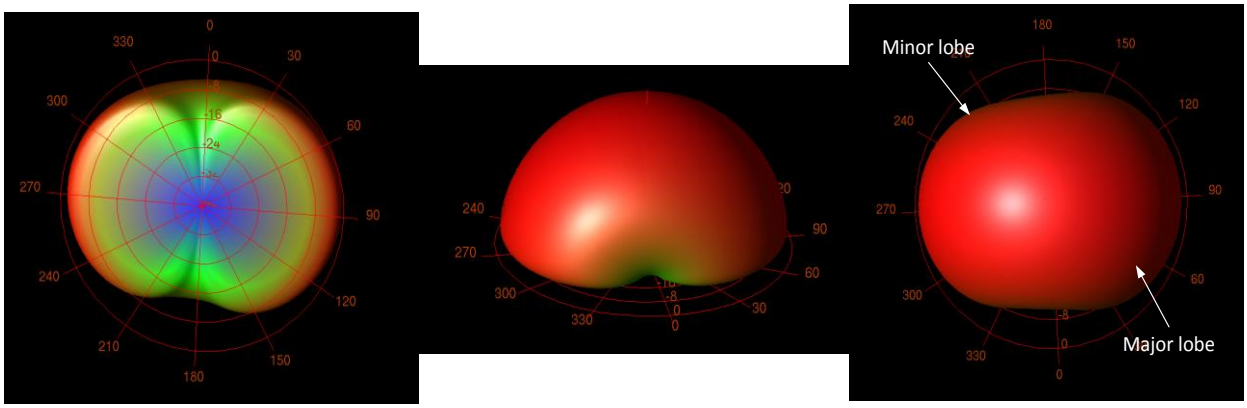


Figure 3.9: Simulated return loss(S11) for UWB antenna.



(b) (b) (c)

Figure 3.10: Simulated Radiation pattern of UWB antenna shown from a) bottom, b) side, and c) top view.

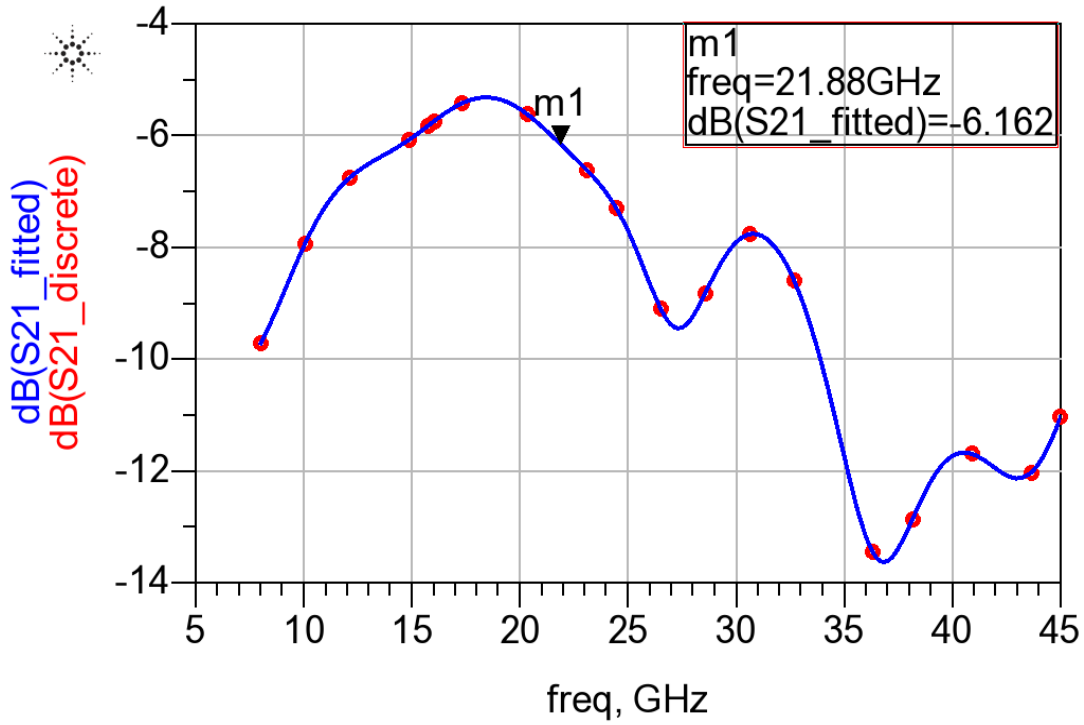


Figure 3.11: Simulated Gain or S21 plot of UWB antenna.

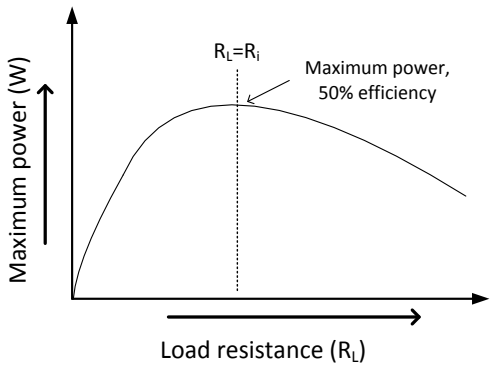


Figure 3.12: Plot for relation between maximum power transfer and load impedance.

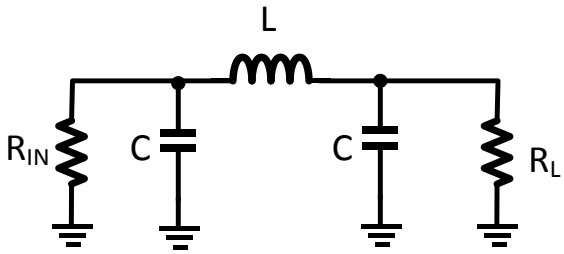


Figure 3.13: Low pass pi matching network.

3.4 Impedance matching

Impedance matching is a pivotal part of any wireless transmission. It is the process of making one impedance look like the other by using LC components. This avoids the power reflection from antenna back to the circuit. The circuit impedance and antenna impedance are calculated and later used to find the LC component values to get the imaginary part in antenna impedance as close to zero as possible. Fig. 3.12 shows the plot for the relation between maximum power transfer and load impedance.

Matching circuit was introduced in the transmitter as well as receiver circuit after and before the amplifier circuit respectively. A low pass pi matching network was chosen for this communication. The circuit was simulated in ADS and then later layout was implemented in Cadence. Fig. 3.13 shows the circuit implementation of the matching circuit. The value of the inductor was chosen so as to satisfy the space requirement as well as to attain considerable matching losses.

Chapter 4 RF Receiver

4.1 Introduction

Receiver is a pivotal block in any communication system. This chapter explains RF receivers in detail. The first section will highlight designing and implementing Low Noise Amplifier in detail. The later sections will highlight other receiver components such as mixer, differential amplifier, buffer converter and output driver. Their design process, layout and results of the individual components are shown in this chapter.

4.2 Low Noise Amplifier

Low Noise Amplifier(LNA) is the first gain stage after an antenna in receiver. LNA as the name suggests reduces the noise which had added on to the signal during transmission and receiving. The most challenging part of designing LNA is to design it within the design constraints and should also meet the specifications. The amplitude of signals coming from the receiver antenna are usually in range of milli-volts, therefore signal amplification is necessary before feeding it to the mixer. The LNA requires having a certain amount of gain because of this reason and should be sufficiently linear in order to avoid back propagation of signal to antenna. For portable devices, power and area consumption are to be kept in mind. For the sake of understanding, gain, stability and noise figure of the LNA are explained briefly here.

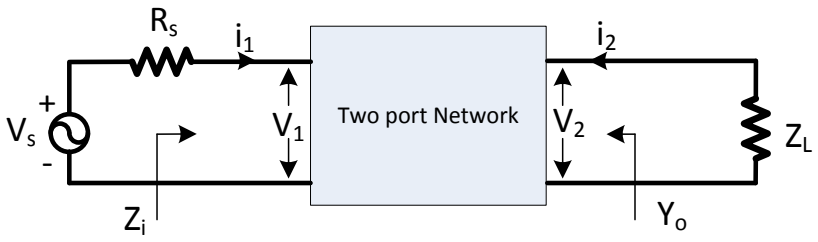


Figure 4.1: Basic two port network

S-parameters

Scattering parameters or S-parameters are complex numbers that represent how voltage wave propagates in RF environment in a matrix form. They are used to characterize and model an n-port linear network [19]. Fig.4.1 shows a basic two port network, and linear equations describing the behavior of this network can be written as:

$$b_1 = S_{11}*a_1 + S_{12}*a_2 \quad (4.1)$$

$$b_2 = S_{21}*a_1 + S_{22}*a_2 \quad (4.2)$$

where, a_1, a_2, b_1 and b_2 are traveling waves representing incident voltages at the ports. The S-parameters: S_{11}, S_{12}, S_{21} and S_{22} correspond to input reflection coefficient, reverse gain coefficient, forward gain coefficient, and output reflection coefficient respectively and are defined by:

$$S_{11} = \frac{b_1}{a_1}, \quad \text{where } a_2 = 0 \quad (4.3)$$

$$S_{12} = \frac{b_1}{a_2}, \quad \text{where } a_1 = 0 \quad (4.4)$$

$$S_{21} = \frac{b_2}{a_1}, \quad \text{where } a_2 = 0 \quad (4.5)$$

$$S_{22} = \frac{b_2}{a_2}, \quad \text{where } a_1 = 0 \quad (4.6)$$

For most calculations, port reference impedances Z_S and Z_L are assumed positive and real. I_1 and I_2 are currents of input and output ports respectively. Z_0 is the reference impedance which is used for all the ports here. The independent variables a_1 and a_2 can be related to port currents and voltages as follows:

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} \tag{4.7}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} \tag{4.8}$$

Similarly, the dependent variables b_1 and b_2 can be represented as:

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} \tag{4.9}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} \tag{4.10}$$

Gain and stability

The gain of an amplifier is mainly affected by the transistor itself and the input output matching network. Fig. 4.2 shows a simplified block diagram of the same [20]. When a wave travels through different impedance lines, a fraction of wave is reflected as result the incident wave loses some of its magnitude. The extent of incident wave power loss depends on the similarity of impedances at both ends of the circuit. To maximize the power transfer and to reduce the reflected power loss, matching is performed. Reflection coefficient is a performance parameter which shows to what extent the impedances are matched. The input and output reflection coefficients Γ_{in} and Γ_{out} for a two port network are defined by [21]:

$$\Gamma_{in} = \frac{b_1}{a_2} = S_{11} + \frac{S_{11}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.11}$$

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{4.12}$$

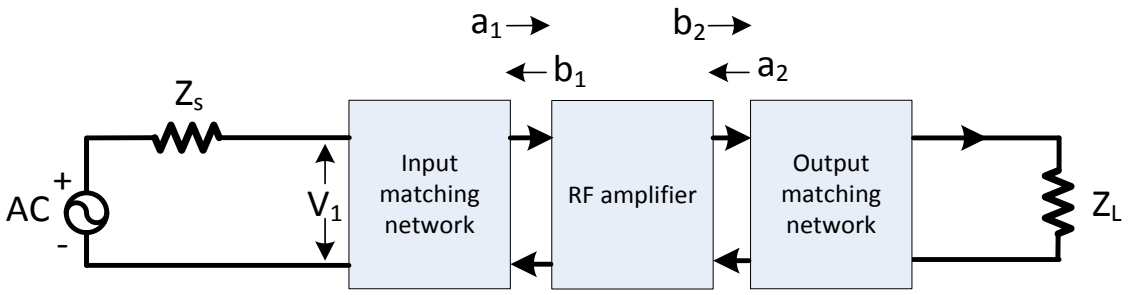


Figure 4.2: Simplified RF amplifier block diagram with matching circuit.

Where,

$$\Gamma_L = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{4.13}$$

$$\Gamma_S = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.14}$$

where, Z_0 is the reference impedance, Γ_L is the source reflection coefficient, Γ_S is the reflection coefficient. The amplifier has maximum power transfer if $\Gamma_{in} = \Gamma^*_S$ and $\Gamma_{out} = \Gamma^*_L$.

There are several definitions for gain of an amplifier. The voltage gain(A_V) is voltage at the output port over voltage at the input port of the amplifier and is given by:

$$A_V = \frac{V_2}{V_1} = \frac{S_{21}(1+\Gamma_L)}{(1-S_{22}\Gamma_L)(1+\Gamma_{in})} \tag{4.15}$$

The power gain(G) of the amplifier is the actual power amplification of the amplifier, and is defined by:

$$\textit{Power gain} = \frac{Avaialable\ power\ at\ output}{Power\ at\ the\ input} \tag{4.16}$$

For IC implementations, generally the LNA is matched to a 50 ohm generalized input and output impedance.

Noise Figure

Noise figure is used to measure the noise performance of an RF amplifier. The noise factor accounts for the degradation in the signal's sound to noise ratio(SNR) due to the amplifier as the signal traverses the receiver front end. It is defined as the total output noise power divided by the output noise power due to the source. It is defined mathematically as:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{4.17}$$

Where SNR_{in} and SNR_{out} at the input and output of the amplifier respectively. When the noise factor is expressed in dB, it is called noise figure:

$$NF\ (dB) = 10 \log F \tag{4.18}$$

So far the basic concepts required to implement a LNA are covered briefly in order to help the designer build his own LNA. The LNA can be categorized into two on the basis of range of frequency as Narrow band and Wide band LNA. We will discuss about wide band LNA in the next section. In later section we will go over Narrow band LNA and its use in our system.

4.2.1 Ultra Wideband LNA

Ultra wide band(UWB) LNA's usually play a significant role in portable devices as they occupy very less space and can work in a large bandwidth. They are usually inductor-less LNA's as the presence of inductor limits the frequency range of the circuit.

Inductor-less LNA design has to satisfy many conditions such as higher gain and lower noise figure with higher forward gain. These circuits are mainly based on Shunt feedback (SFB) [22] or CG topologies. Input matching is provided using feedback impedance with either pure resistance or with a parallel capacitor at the cost of output impedance. The CG amplifier's basic benefits include $1/g_m$ source terminal impedance and better linearity but with lower voltage gain. In CG amplifier, availability of gate terminal enables the circuit to operate without pure DC node which are known as g_m boost CG circuits [23].

Gm Boost Technique

In the conventional CG-LNA circuit(fig. 4.3(a)), differential gain(A_v), differential input impedance R_{in} and NF are given by [24],

$$A_v = g_{m1}.R_L \tag{4.19}$$

$$R_{in} = 2/g_{m1} \tag{4.20}$$

$$NF = 1 + \frac{\gamma}{\alpha} + \frac{4Rs}{RL} \tag{4.21}$$

where, g_{m1} is the trans-conductance of the transistor M_1, α is the ratio between zero bias drain conductance and γ is the excess channel thermal noise coefficient.

Fig. 4.3(b), shows a differential capacitive cross coupling (CCC) LNA which uses passive amplification to boost the input at no extra voltage supply which limits the voltage supply and matching trade off. The g_m boosting techniques include applying signal at both source and gate pins simultaneously to increase the swing of V_{GS} [23]. The addition of inverting gain (A_{NEG}) gives smaller bias current, smaller noise contribution and power consumption, while effective g_{m1} is boosted due to input impedance matching. Reference [24], shows that the A_{NEG} can be implemented using a CCC, and also at A_{NEG} almost unity, A_v, R_{in}, and F are reduced to,

$$A_v = 2g_{m1}R_L \tag{4.22}$$

$$R_{in} = 2R_s = 1/g_{m1} \tag{4.23}$$

$$F = 1 + \frac{\gamma}{2\alpha} + \frac{4Rs}{RL} \tag{4.24}$$

By comparing conventional CG LNA, the NF and R_{in} are reduced by a factor of half with increase in trans-conductance and also reduced power consumption.

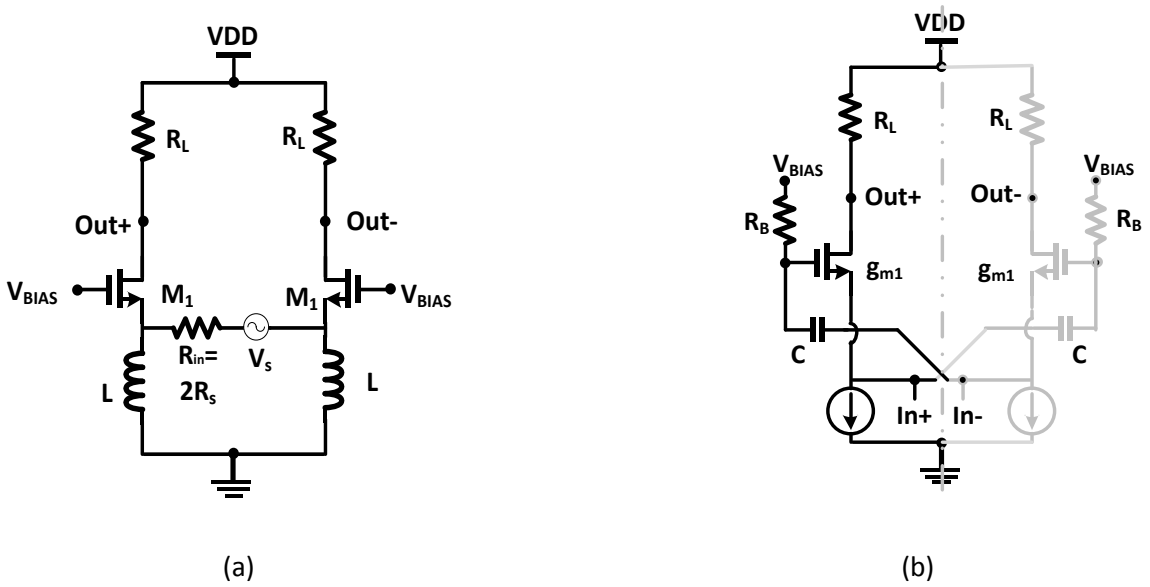


Figure 4.3: (a) Conventional Differential CGLNA[**[24]**, (b) Differential CCCLNA **[23]**.

Fig 4.4, depicts the proposed circuit which includes three stages namely, g_m boosting stage, main amplifier stage and CS stage to furthermore enhance the gain. The transistor M_2 and resistor R_5 constitute main CG amplifier and similarly M_1, M_3 and R_3 is named as g_m enhancing circuit [23]. The basics of g_m boosting technique state that by applying the signal at both source and gate terminal of a CG stage, increases the swing at the drain of the MOS transistor. This technique also helps in reducing the NF of the circuit at no extra power supply [23]. This approach has been applied in many recent circuits [25], [26] with an additional CCC added, which enables the g_m boosting effect at no additional cost of power supply [23]. But as the CCC depends on passive amplification the g_m boost is limited to less than one. This problem can be solved by using inductive transformer but considering the area constraint this approach has been neglected in this circuit. The proposed circuit is a double boosted g_m enhanced LNA as the CCC in addition with the two CG stages connected to the input increases the gain to considerable levels.

The linearity of the whole LNA degrades at low voltages but can be overcame by using CG circuit instead of CS circuit as the first stage of the LNA [25], which has lower NF comparatively. The P-MOS transistor forms an active load and avoids huge voltage drop through R_3 [23]. The

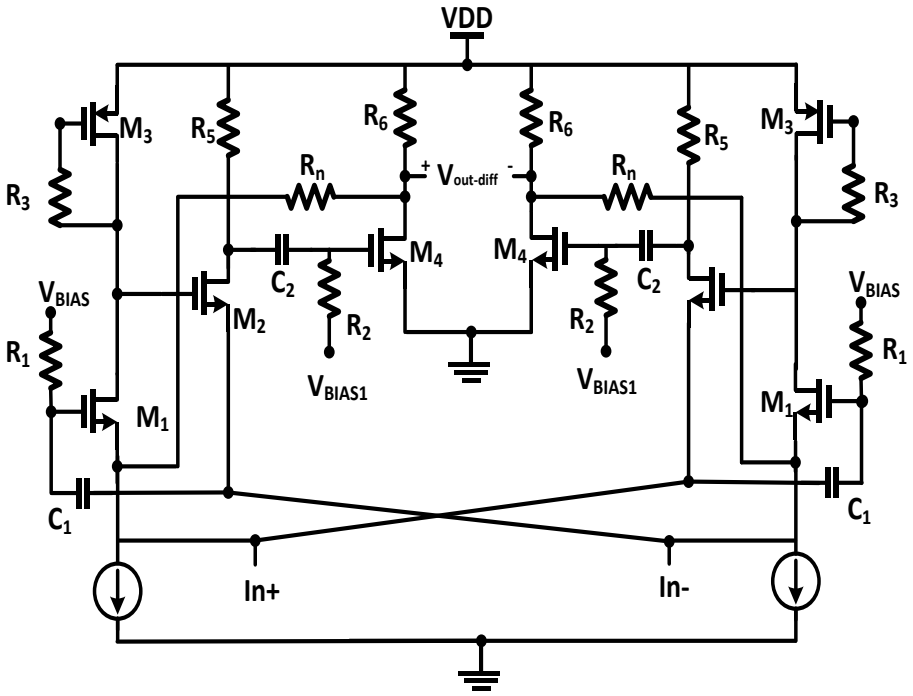


Figure 4.4: Schematic of proposed CG double gm boost LNA

current by both first and second CG stage is shared from a common current source. Transistor M_4 and R_6 were added as a CS stage after the main amplifier which enhances gain, which when has high overdrive voltage will give reliable input linearity(IIP3) measurement results [23]. Capacitor C_2 and resistor R_2 have been added to provide external bias to the circuit for better gain after the CS stage. Resistor R_n have been introduced as feedback which extends from the output of CS stage to the input of the first CG stage which is observed to lower input reflection(S_{11}) without affecting other factors of the LNA. The input signals were biased at 600mV before providing to achieve the best performance from the circuit.

The ratio of currents in both the circuits is set by an external bias to M_1 in order to isolate the biasing part from RF parts [23]. M_2 transistor here doesn't require any additional RC-bias tee as the gate is DC- coupled [23]. And finally, the LNA is loaded with a 50fF capacitor replacing a mixer for simulation purpose.

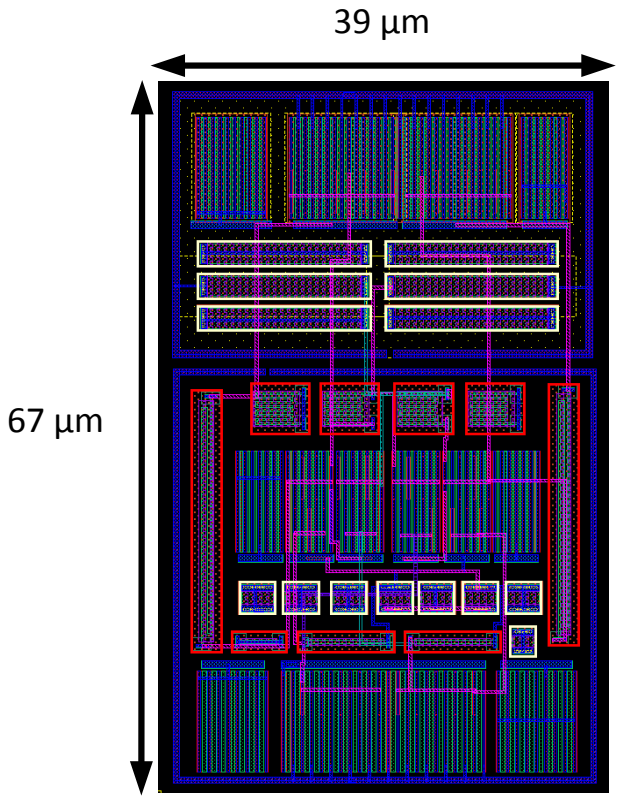


Figure 4.5: Layout of the proposed LNA with dimensions

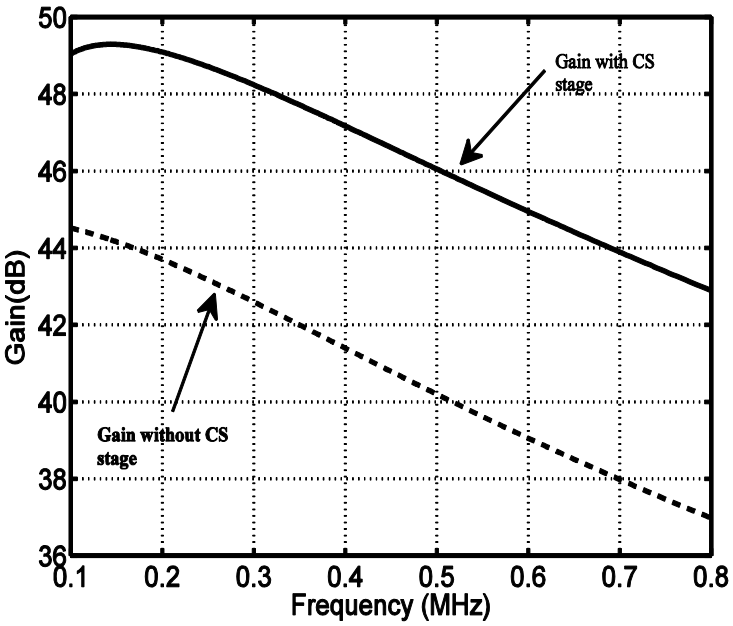


Figure 4.6: Plot showing simulated Voltage gain with and without CS stage

Layout and Results

The proposed LNA has been simulated in 180nm using Golden-Gate simulator in Cadence. The LNA core layout, shown in fig. 4.5 shows it occupies only 39 um x 67 um i.e; an area of 0.0026 mm^2. The simulated results for voltage gain are shown in fig. 4.6. The maximum gain at 150MHz for the circuit with the CS stage is noted at ~49dB and for the circuit without the CS stage is found to be approximately more than 44dB at 100MHz.

The LNA consumes 1.6mW of power through a supply voltage of 1.8V in 180nm. The above LNA gave the following results for NF, shown in fig. 4.7. The NF_{min} is observed at 400 MHz to be 4.69dB and the range of NF of the LNA is from 4.69-5.48dB. The forward gain(S_{21}) and S_{11} simulations were performed by providing true differential mode S-parameters. The NF and S_{21} parameters were also simulated with the help of Golden-Gate and Cadence software.

Fig. 4.8 depicts S_{21} results which show that the proposed LNA has almost more than 39dB gain with ~46dB of maximum gain at 150MHz. The LNA is matched at 50 ohms impedance at input and output. Fig. 4.9 shows the S_{11} results of the proposed LNA. The S_{11} was observed to vary significantly with the addition of resistor R_n allowing us to attain a reasonable input reflection level at approximately -10dB. Fig. 4.10 shows the input and output third order points IIP3 and OIP3 respectively obtained for the proposed LNA. The IIP3 is noted to be -26.6 dBm and OIP3 at 17.37 dBm which was attained with a trade off with NF and power supply. And finally table 1 shows the comparison of this LNA's results with prior arts.

The frequency requirements of the designed system compelled us to design another LNA which encompasses the 21.5GHz frequency. A narrowband LNA was designed specifically for this system.

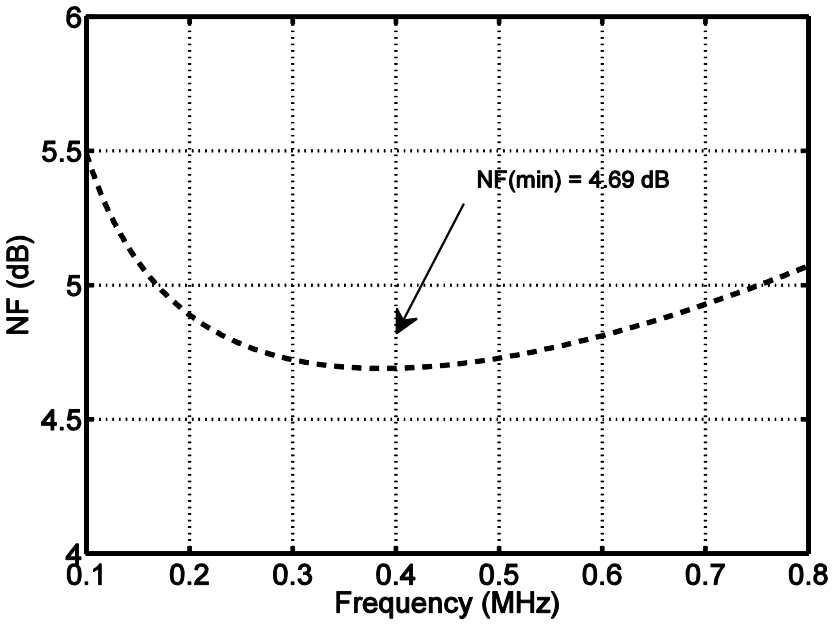


Figure 4.7: Plot showing the simulated Noise Figure(NF)

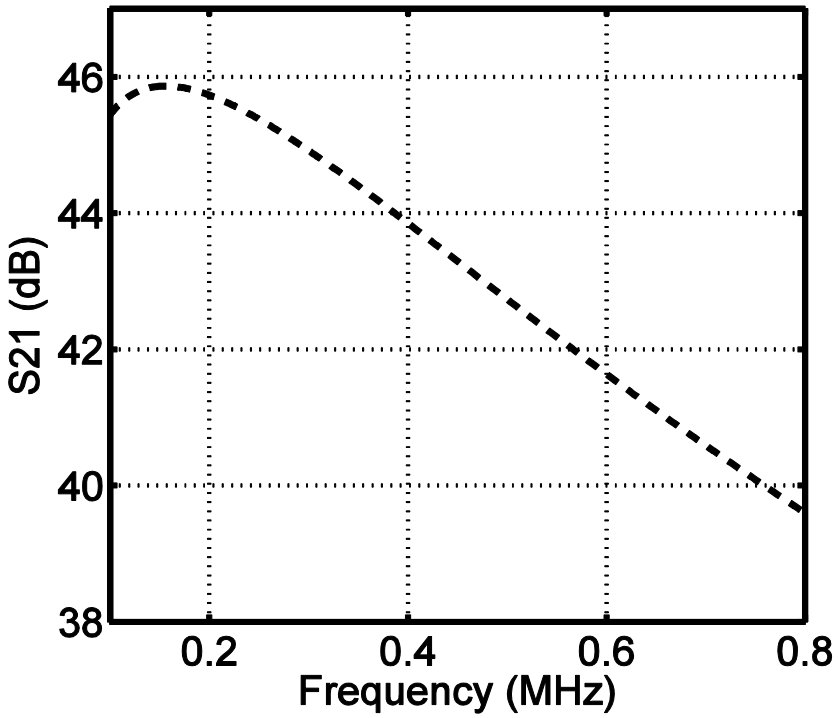


Figure 4.8: Plot showing the simulated forward gain(S_{21})

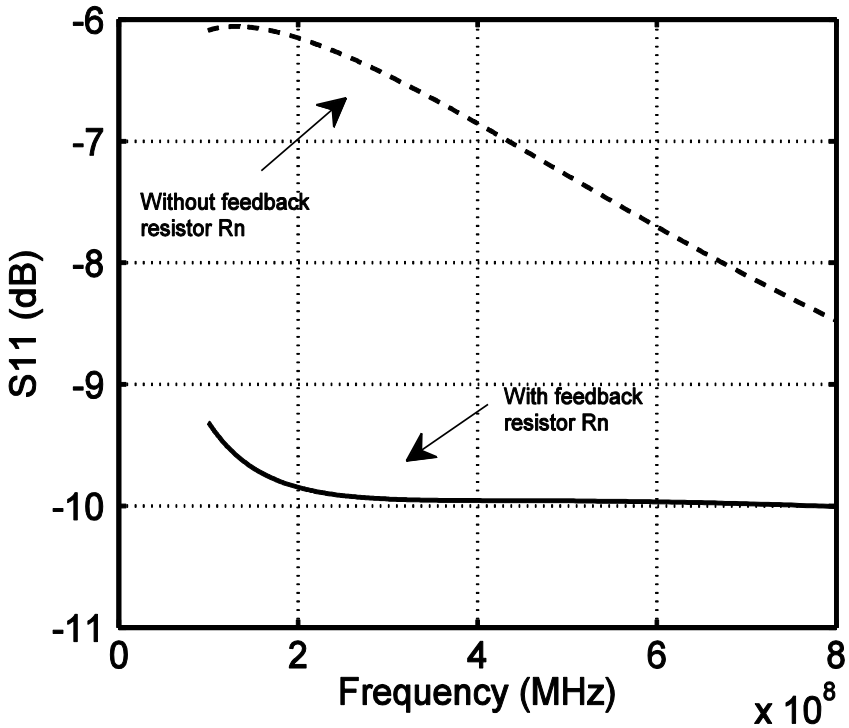


Figure 4.9: Plot showing the simulated input reflection(S_{11}).

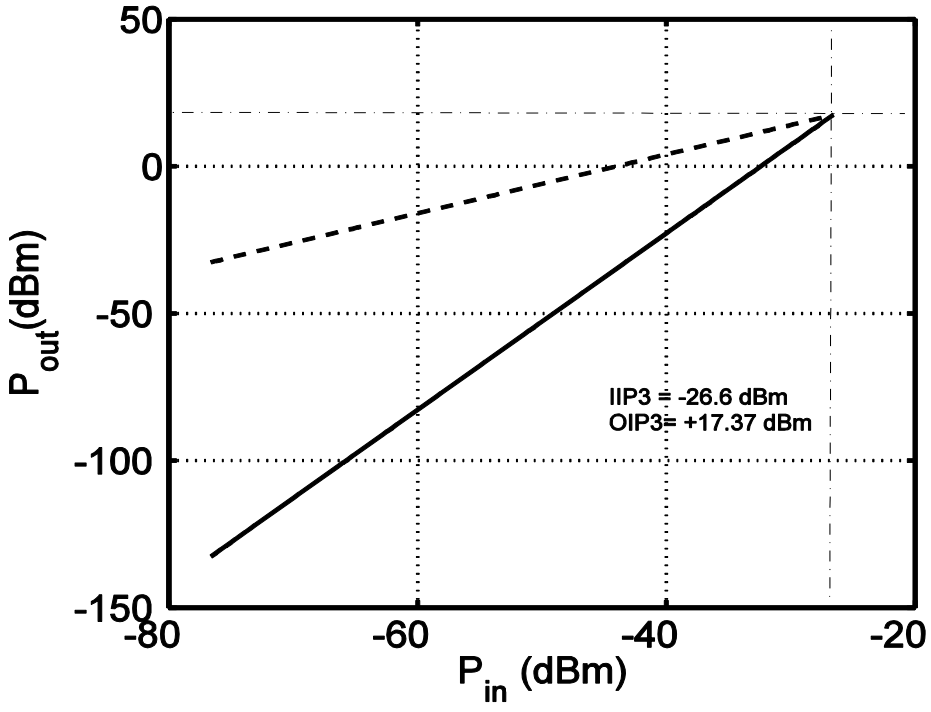


Figure 4.10: Plot showing the simulated input and output third order points IIP3 and OIP3.

Table 1
Comparison of proposed LNA with prior arts

References	[23]	[27]	[28]	[29]	**This Work**
Process	130nm	130nm	90nm	180nm	**180nm**
BW(GHz)	0.1-2.7	0.01-1.4	0.1-1.66	0.04-0.9	**0.1-0.8**
Vdd (V)	1.2	1.8	1	1.8	**1.8**
Power (mW)	1.32	0.9	0.425	43.2	**1.6**
S_{21}or Gain(Gv) (dB)	11.2 (Gv)	22(Gv)	10.5(S_{21})	20.3(Gv)	**39.5-45.9(S_{21})**
NF (dB)	4.0	7	5.9	4	**4.69 - 5.48**
IIP3 (dBm)	-12	-17	-4.5	-10.8 - 12.7	**-26.6**

4.2.2 Narrow band LNA

Fig. 4.11 shows the LNA which was designed specifically to meet the requirements of the system. The LNA has two stages. The input is given at the gate of the first stage which has the signal output from the receiver antenna. The matching network was introduced for the antenna which was added to the LNA during simulations as load impedance, 50 ohms. A bias circuit was connected to the input end in order to control the common mode of the signal fed at the input.

Usually, in narrowband LNA's the frequency of operation and gain is determined by the inductor used. The inductor forming the LC tank helps the LNA in achieving good results for forward gain, reverse isolation, etc.

Layout and results

Fig. 4.12 shows the layout of the LNA which was implemented in the design. Fig. 4.13 and Fig. 4.14 show the NF and forward gain of the LNA respectively. We can see from the plot that the minimum NF achieved here is 6.21 dB.

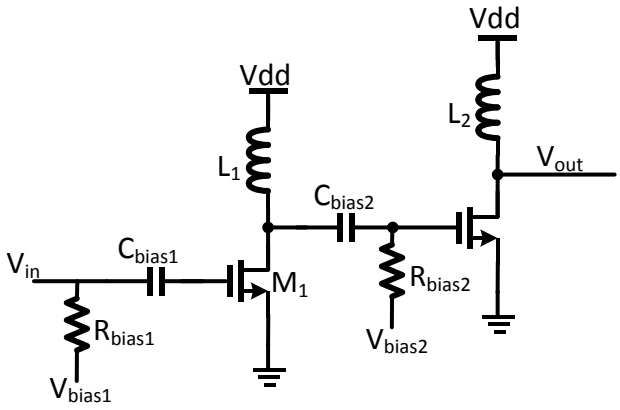


Figure 4.11: Circuit configuration of the implemented LNA

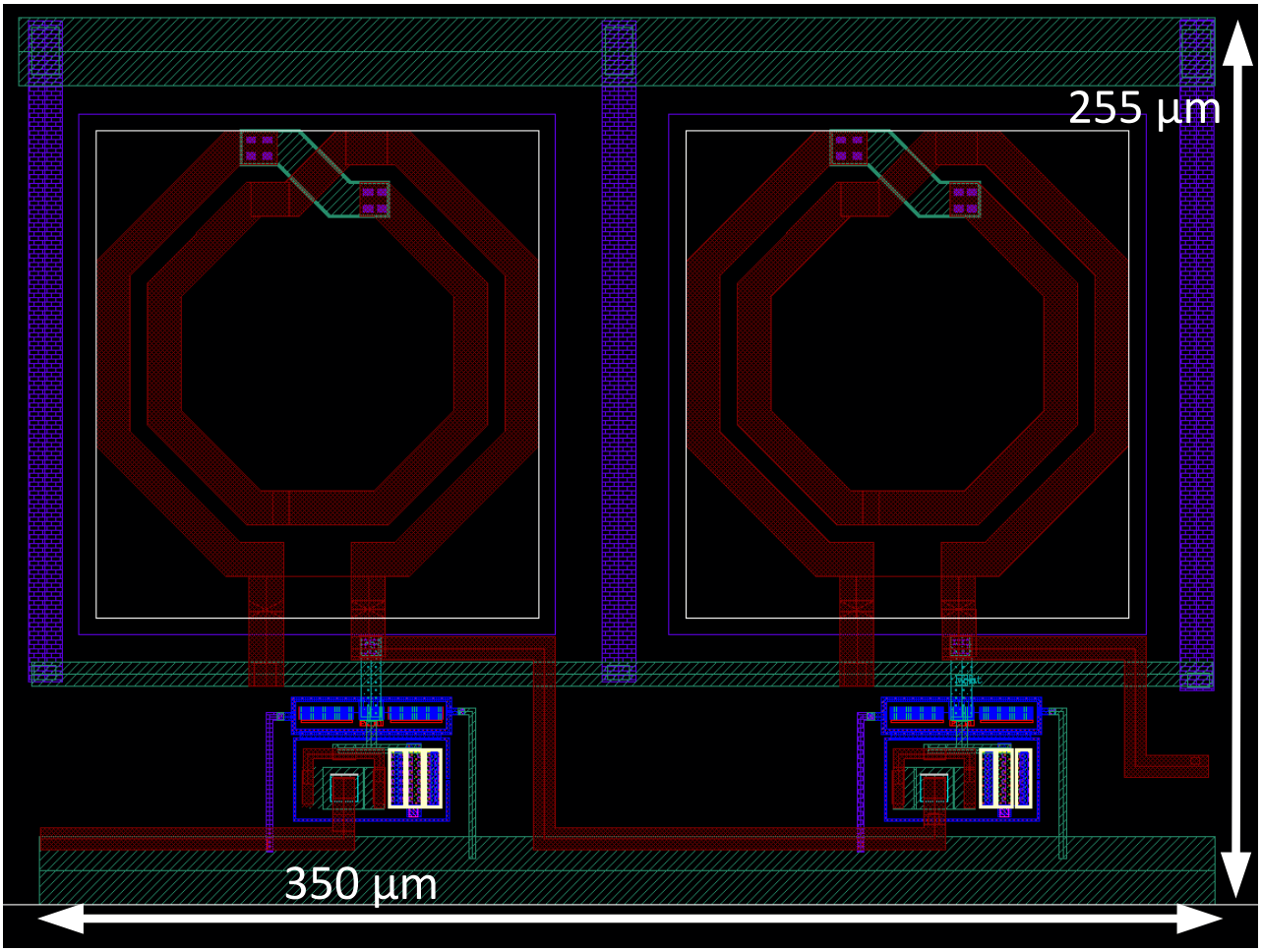


Figure 4.12: Layout of the implemented LNA

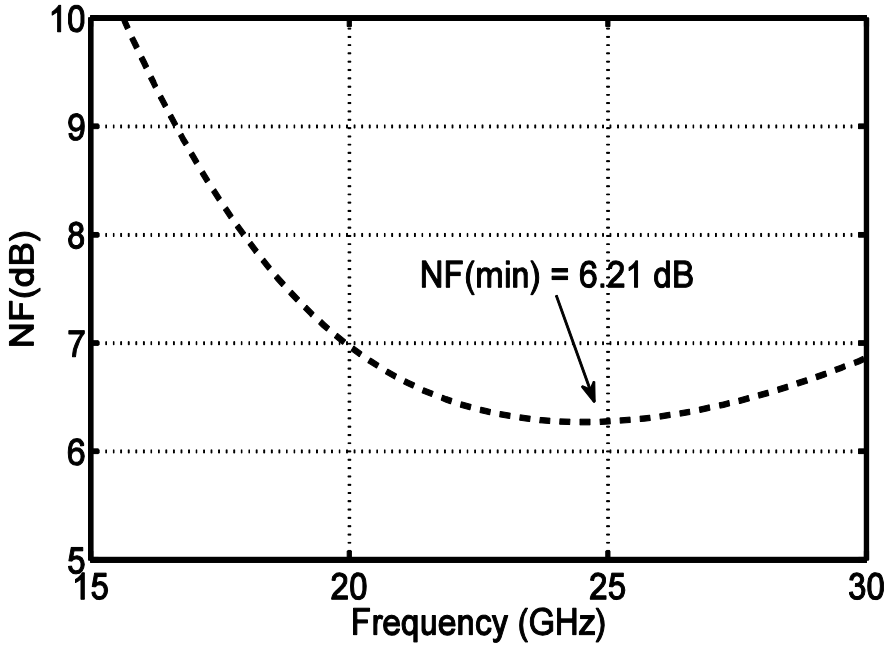


Figure 4.13: Simulated NF of the LNA

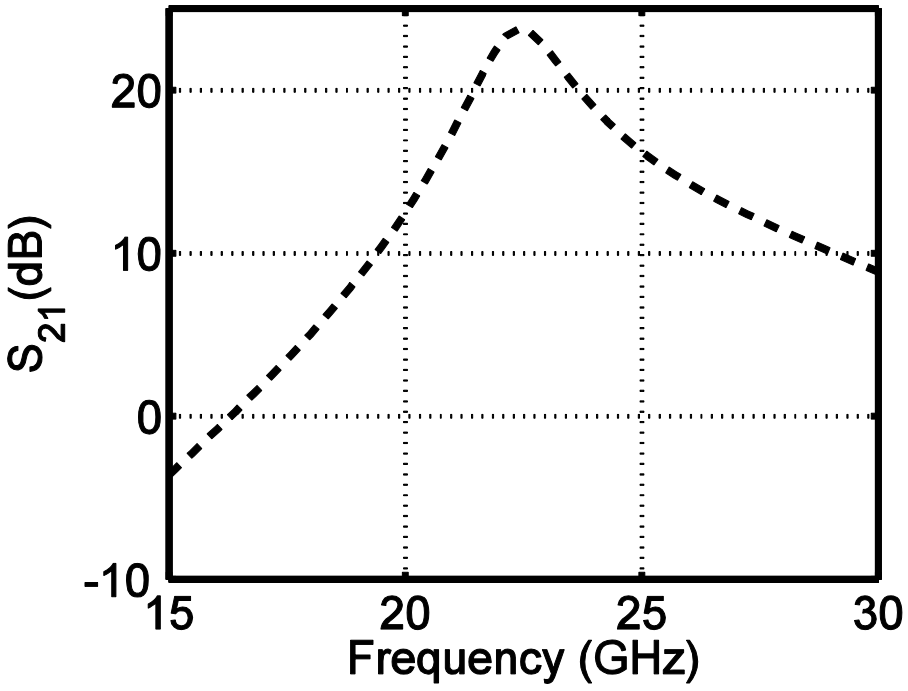


Figure 4.14: Simulated S21 of the LNA

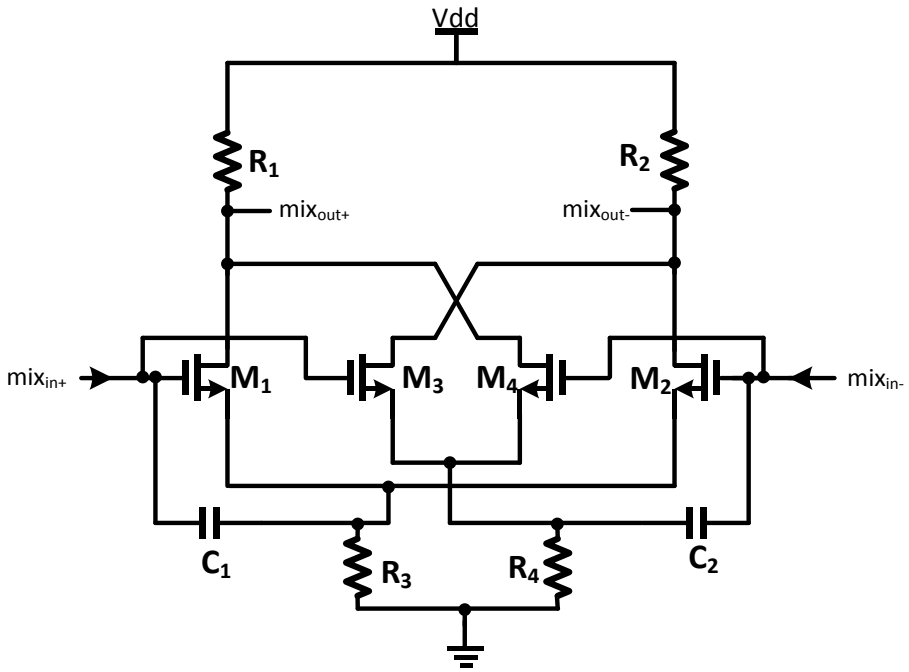


Figure 4.15: circuit configuration of the implemented mixer for this system

4.3 Mixer and demodulating circuit

The signal from the LNA is fed to the mixer as it traverses through the channel between mixer and LNA. The mixer down converts the carrier frequency to baseband. It is followed by a chain of differential amplifiers followed by a buffer converter for input common mode equalization and has output driver as the final stage of the receiver.

4.3.1 Mixer

The mixer was chosen with a non-coherent configuration as it lacks power hungry clocking circuits which reduce the power consumption by the mixer. The mixer operates under the design principles of the Gilbert cell multiplier circuit [30]. The RF and LO inputs have the same carrier frequency. As a consequence we receive the same baseband signal at the output which was originally used to modulate the signal.

Fig. 4.15 shows the circuit configuration of the implemented mixer for this system. The ASK-modulated signal is fed to transistors M_1 through M_4, which is traditionally considered the RF input for the mixer. The input passing through the capacitor(C_1 and C_2) to the sources of the transistors will be considered as LO input to the mixer. The mixer here can be considered as

envelope detector as it will follow the envelope of the ASK-modulated signal. The drains of the two differential amplifiers present in the mixer are cross coupled and have resistors as the load.

The process in this mixer begins with multiplication of the two sinusoidal input signals that are multiplied together. These signals can be described as:

$$s_1 = A\sin(\omega_1 t + \varphi_1) \tag{4.25}$$

$$s_2 = B\sin(\omega_2 t + \varphi_2) \tag{4.26}$$

By using product-to-sum trigonometric identity and rearranging, we get two different frequency components:

$$s_1 \times s_2 = \frac{-AB}{2}(\cos((\omega_1 + \omega_2)t + (\phi_1 + \phi_2))) - (\cos((\omega_1 - \omega_2)t + (\phi_1 - \phi_2))) \tag{4.27}$$

The first term is the sum or image frequency signal and is followed by baseband signal. Also the first signal is in additive form and the other in subtractive form. After the multiplication of the positive component with its compliment a baseband signal is obtained. The additive signal will be filtered out in later circuit while the other will be amplified rail-rail for later transmission. The analysis and operation of Gilbert mixer is involved and exhaustive and has become focus of whole theses and journals. Our aim is to just use the conventional implemented structure in our system from previous analysis performed [30]-[32]. Fig. 4.16 shows the layout of the mixer used in our system. Fig. 4.17 shows the spectral output of the mixer designed. The mixer consumes only 3.61mW of power from a power supply of 1.8V.

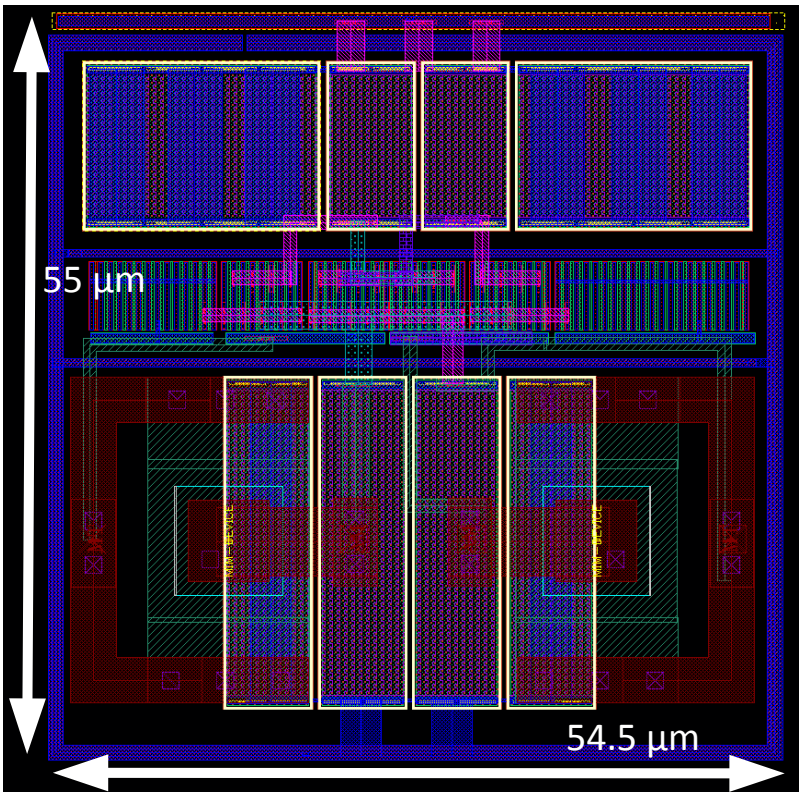


Figure 4.16: Layout of the implemented mixer for this system

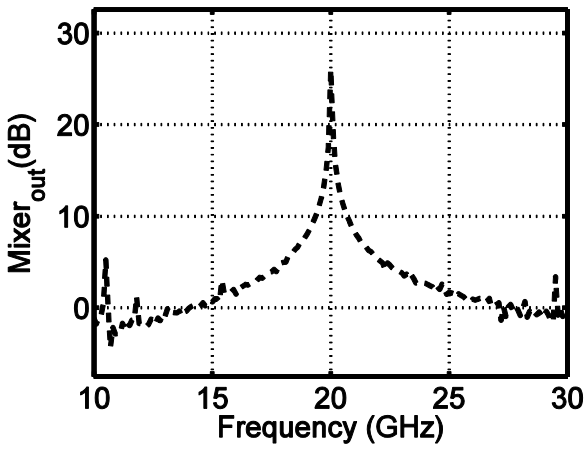


Figure 4.17: Shows the simulated spectral output of the mixer designed.

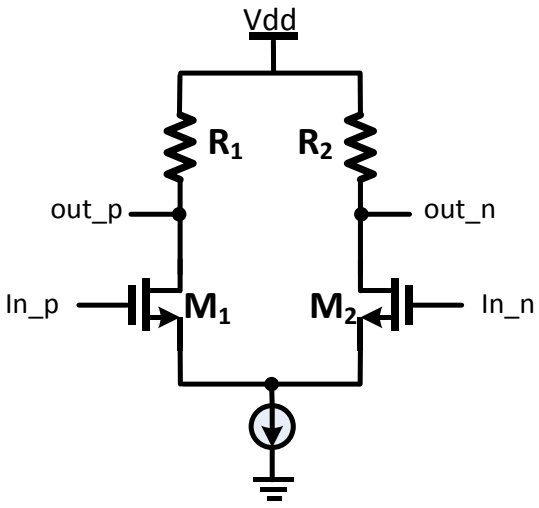


Figure 4.18: Circuit configuration of the differential amplifiers.

4.3.2 Differential amplifier and Buffer converter

The output from the mixer was given to the differential amplifiers which act as low pass filter. There were three differential amplifiers used to perform this operation. Fig. 4.18 shows the circuit configuration of all the differential amplifiers used in the system[13]. All the three differential amplifiers differ among themselves by the load resistor values. The differential amplifier helps to amplify the signal and removes the additional high frequency peaks present in the signal. The differential amplifiers were arranged in a decreasing order of their load resistance so as to bring down the circuit impedance equal to the output 50Ω load of the SMA cable to be connected at the output.

The output from mixer is differential as mentioned earlier and is also at different common modes because of down-conversion used by the mixer. To get rid of this problem we have used a RC feedback control circuit, which is the buffer converter. One can see in fig. 4.19 the circuit configuration of the implemented buffer converter. It controls the overall gain while settling on a single common mode voltage. The transient signal settles after 100ns which tells us that about 100ns of data cannot be recovered which will be the initialization period before any significant data can be recovered. The settling time depends on the RC feedback network. A very large resistance of 700 kΩ with a capacitor of 128fF was chosen for the best transient response. Fig. 4.20 shows the layout of the buffer converter implemented here.

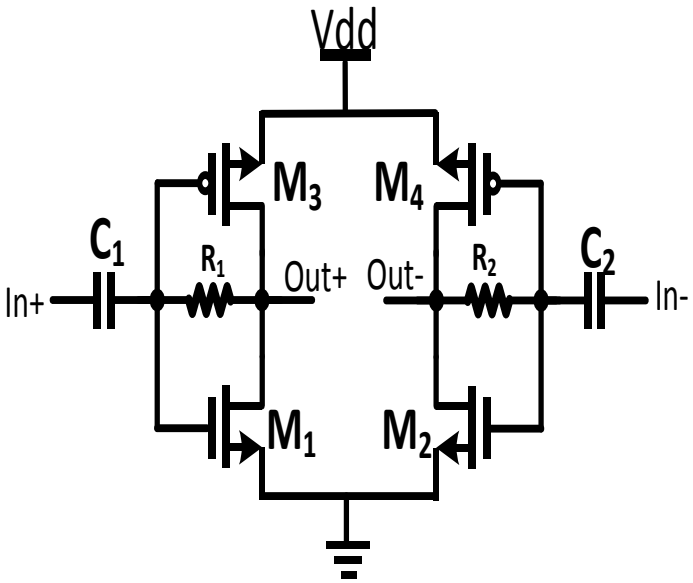


Figure 4.19: Circuit implementation of the buffer converter.

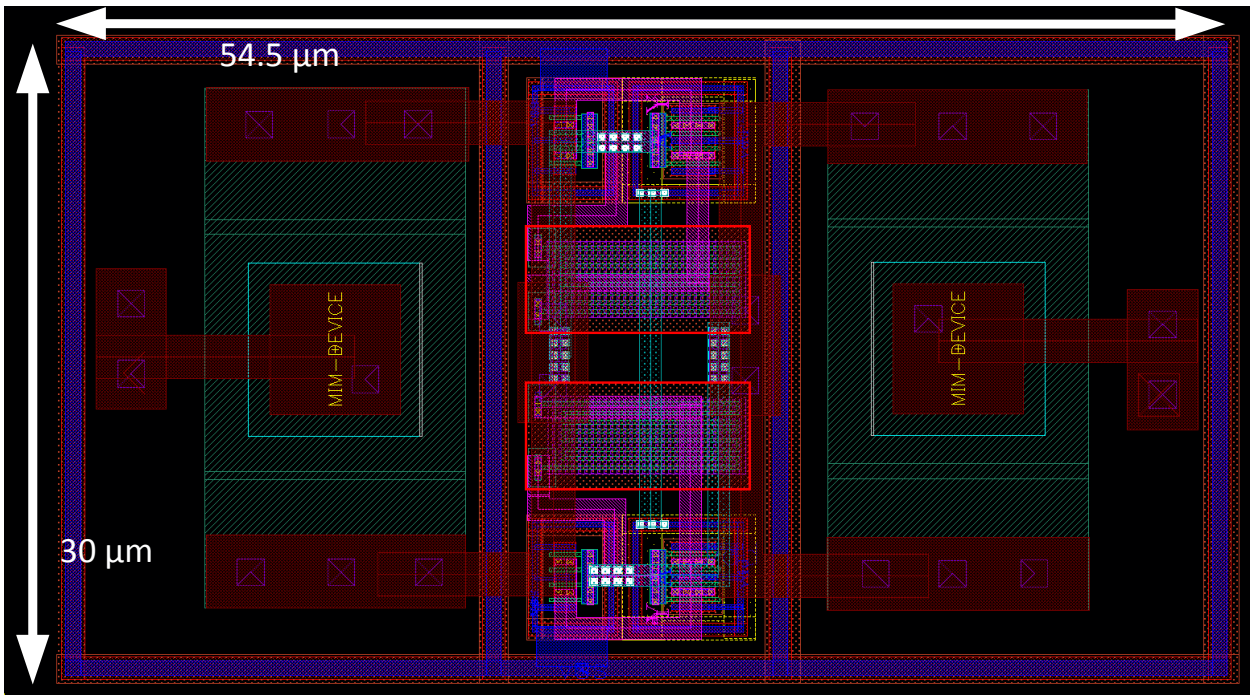


Figure 4.20: Layout of the buffer converter used for this system

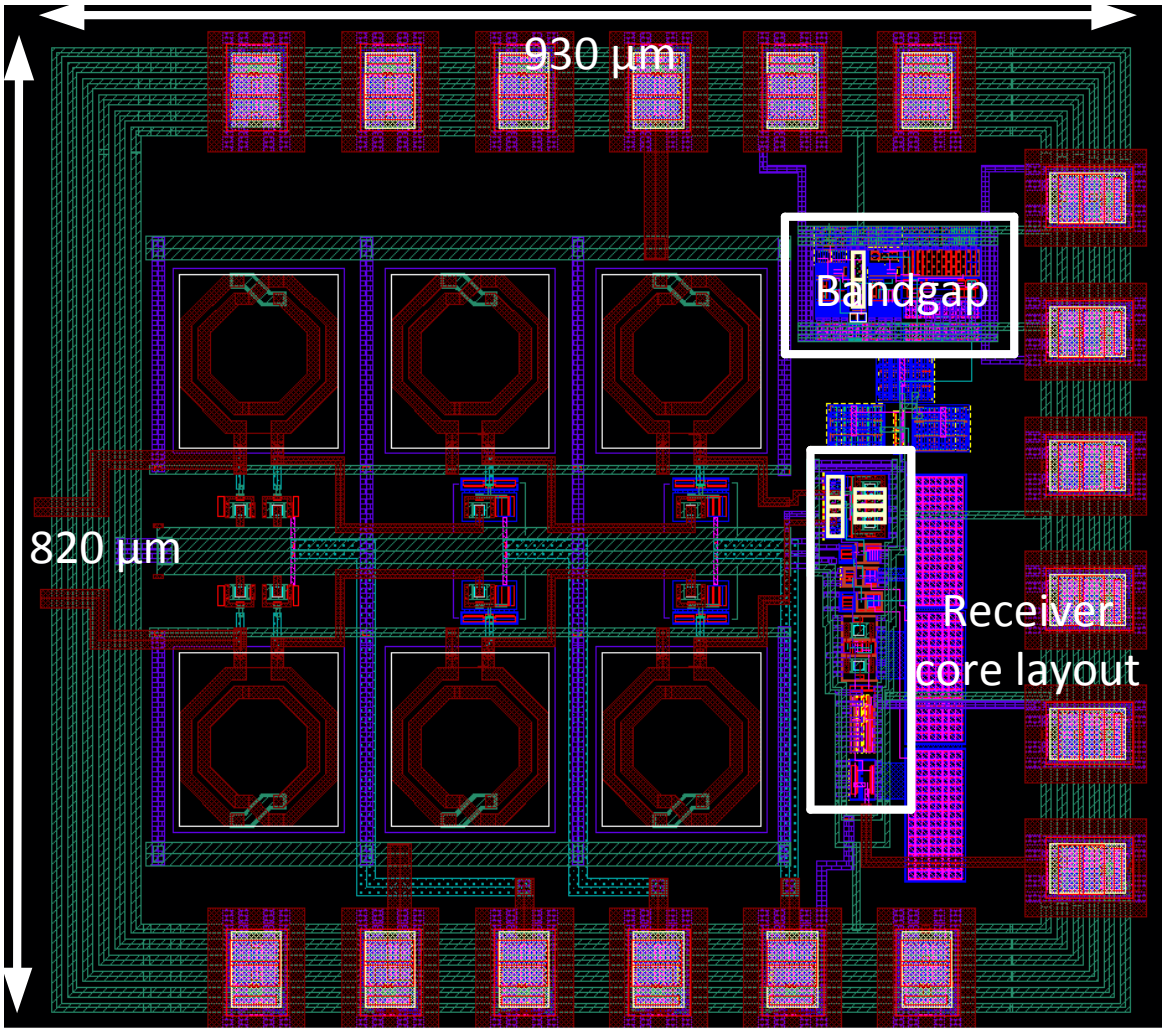


Figure 4.21: Complete layout of the receiver(antenna not included)

The other components following the buffer converter include inverter chain and output driver. The inverter chain includes multiple inverters to make the signal from rail to rail. The output driver is of 50Ω which is equivalent to the connecter at the output of the receiver. Fig. 4.21 shows the complete layout of the receiver. The receiver as a whole occupies 930µm by 820µm.

Chapter 5 RF Transceiver

5.1 Simulation Setup and Final Layouts

We have reached the final step where we present all the results associated with the designed system and merge the transmitter and receiver presented in earlier chapters. Thus far we have shown performances of individual components and have explained why we have chosen that particular component over others. In every RF design there is a chance of parasitics and one must consider them during the initial simulations as well. We can simply connect a capacitor of 10fF on schematic nets, in order to model the parasitic resistances and capacitances. Furthermore, relying only on schematic simulations is not recommended which made us perform post extract simulations. The next section shows the post extract simulation results.

The whole layout of the transmitter and receiver was RC extracted excluding the inductors. The test bench consists of transmitter, receiver, vcvs, inductors and power supply inputs. Fig. 5.1 shows the complete layout of the transmitter along with the UWB antenna. And Fig. 5.2 shows the complete layout of the receiver. Fig. 5.3 shows the complete test bench schematic in cadence used to simulate this design. The transmitter contains the extracted layout of the whole transmitter and similarly receiver block contains layout of the whole receiver. The inductors were placed during simulation and also the bias inputs were given. Vcvs(available in cadence by default) was used instead of the antenna to estimate the losses which can occur during transmission. The whole system consumes a power of just 134.02mW from a 1.8V voltage supply.

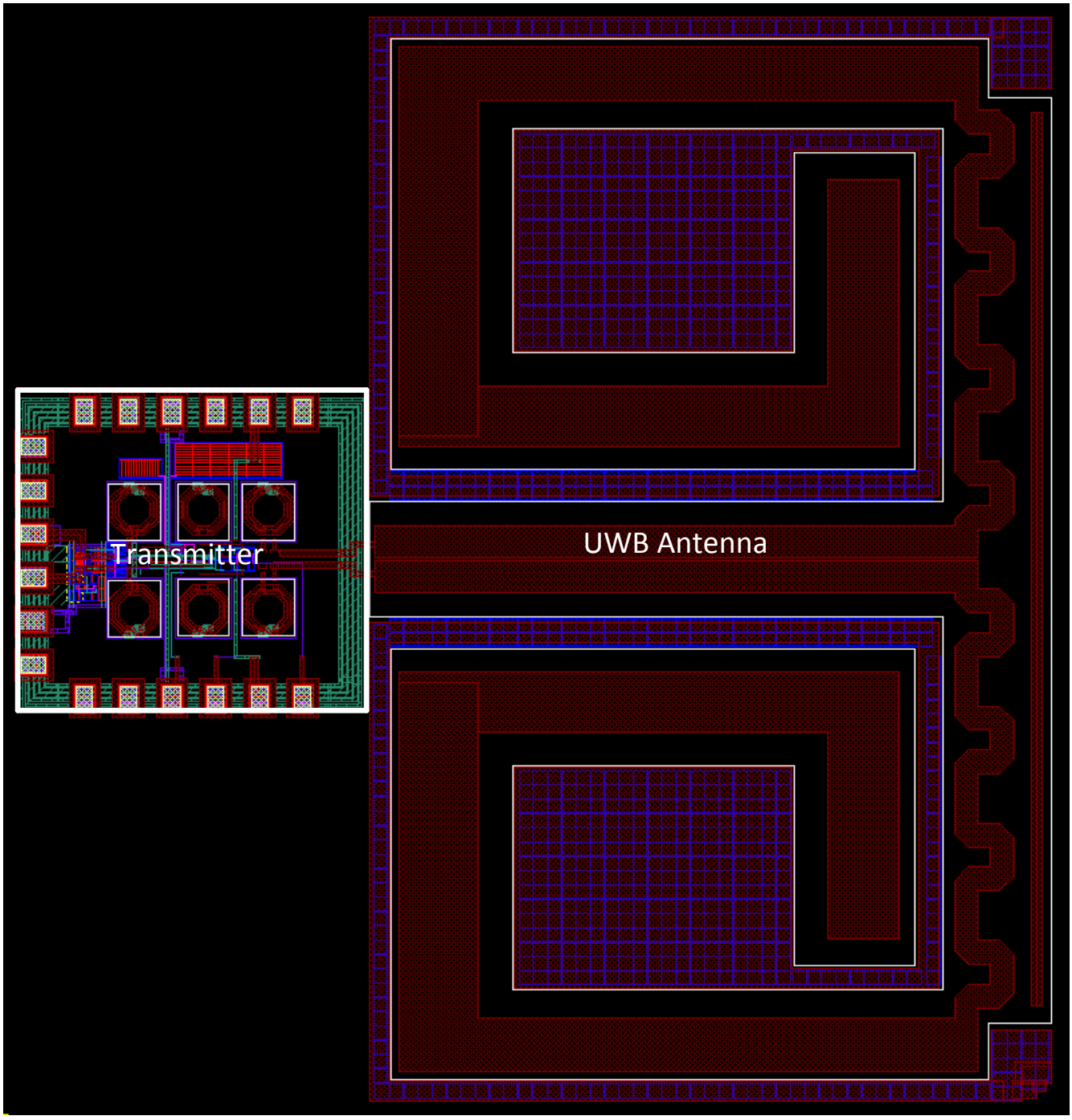


Figure 5.1: Transmitter complete layout.

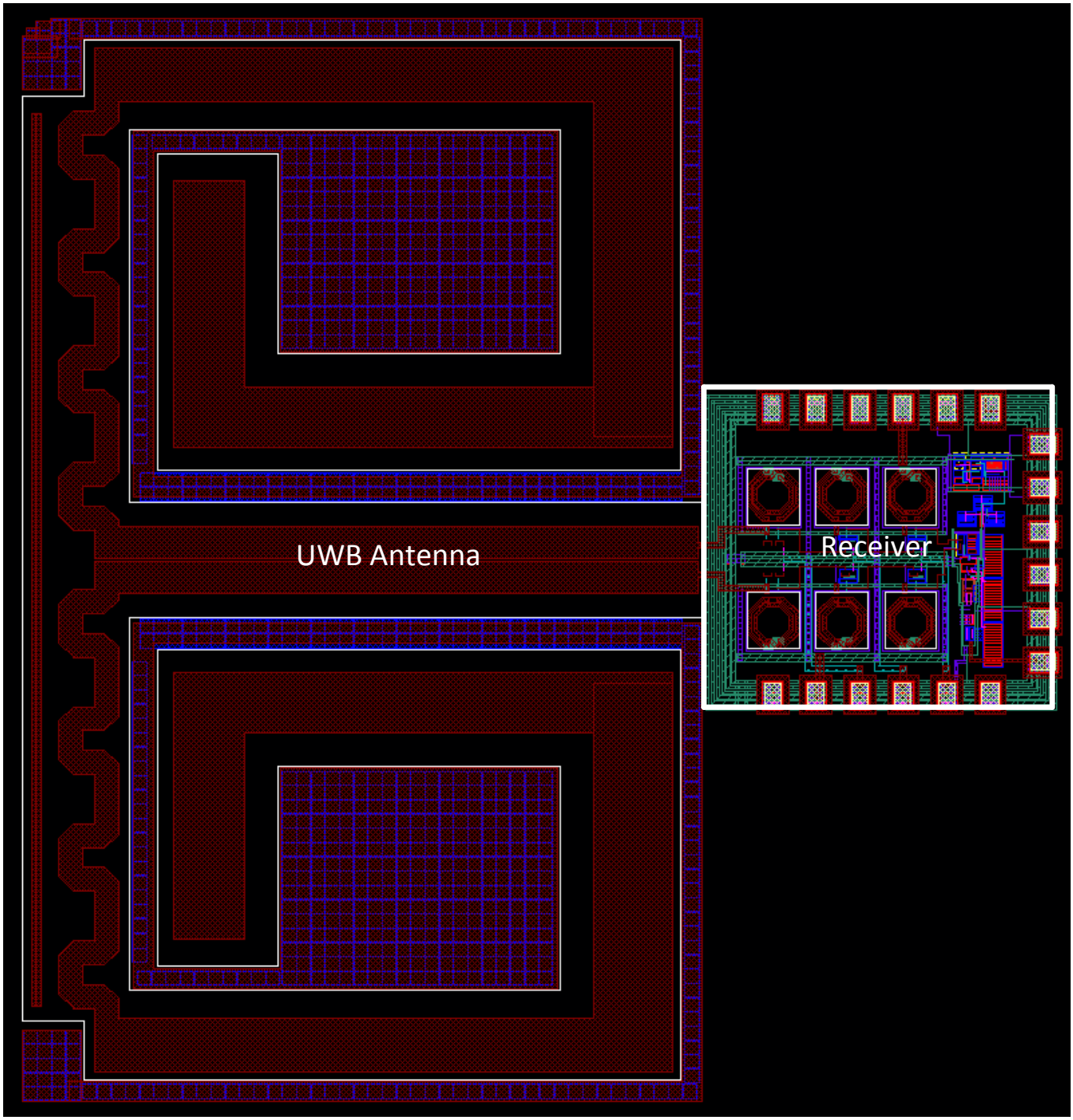


Figure 5.2: Complete receiver layout.

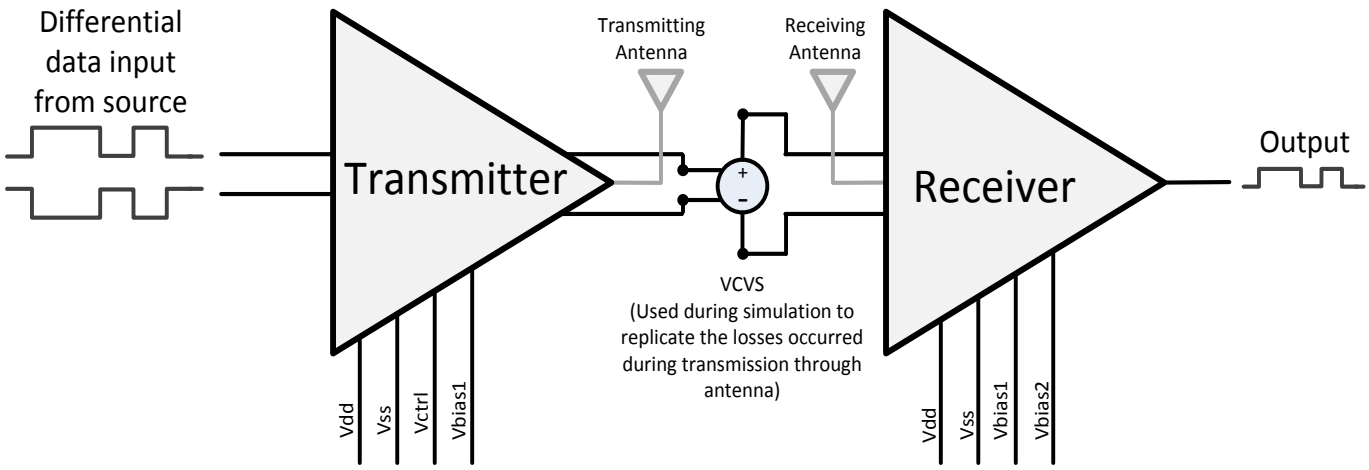
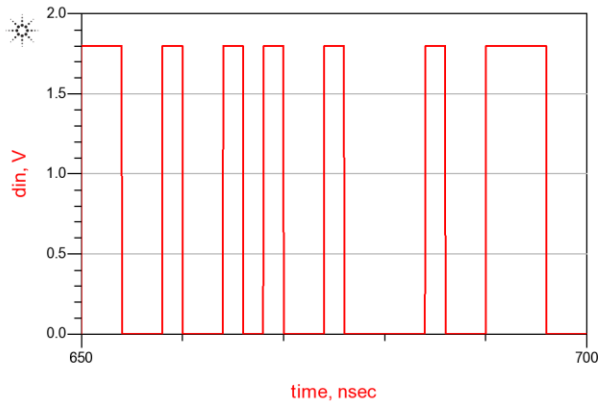


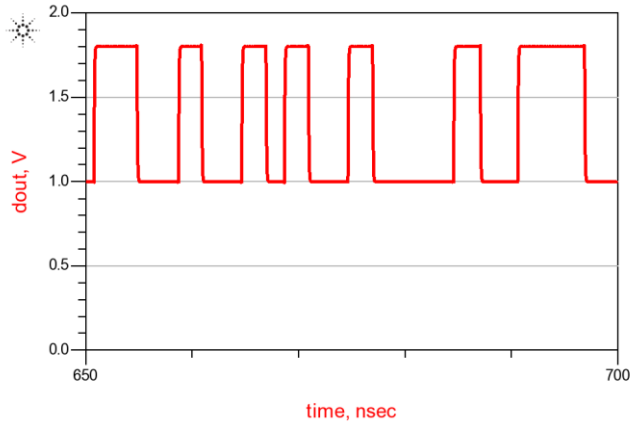
Figure 5.3: Schematic setup used to simulate the system

5.2 Post extract simulation results

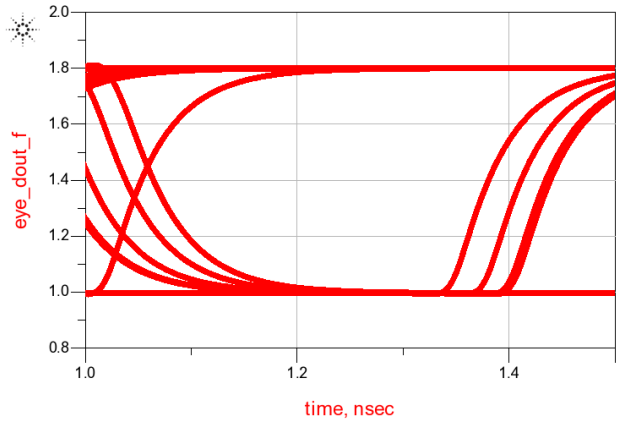
Post extract simulations are 90% accurate to our knowledge. And post extract simulation was performed here to get the most accurate data for this thesis. The input data was generated from a random bit generator in which the frequency desired was chosen. Eye pattern or eye diagram was used to check the performance of the receiver for different data rates. It is used to indicate the quality of signal received and recovered by the receiver in the end. Sweeps of different data is performed and overlapped with reference to time in order to obtain the eye diagram by the oscilloscope. Fig. 5.4 (a) shows the 500MHz input data given to the transmitter, fig. 5.4 (b) shows the output data received at the receiver and fig. 5.4 (c) shows the eye obtained for the 500MHz signal data input. Similarly fig. 5.5 (a) shows the 1GHz input data given to the transmitter, fig. 5.5 (b) shows the output data received at the receiver and fig. 5.5 (c) shows the eye obtained for the 1GHz signal data input.



(a)

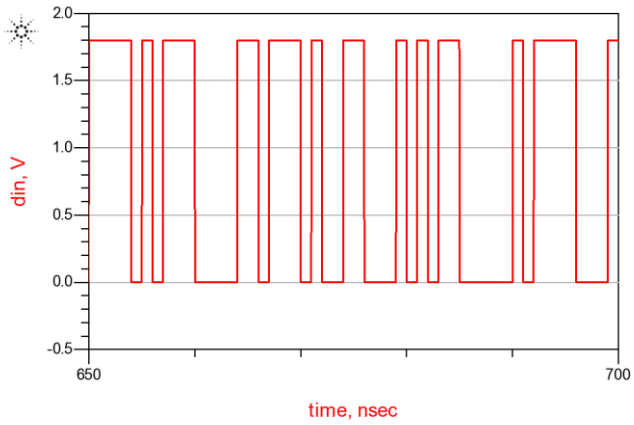


(b)

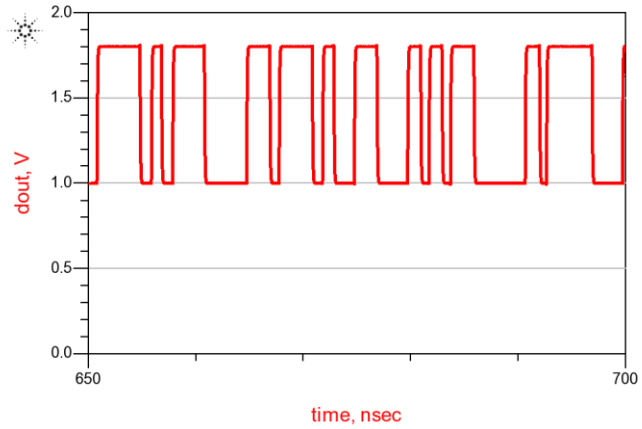


(c)

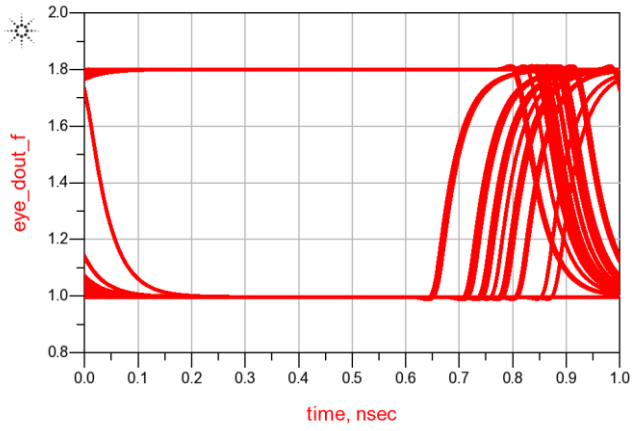
Figure 5.4: (a) shows the 500MHz input data given to the transmitter, (b) shows the output data received at the receiver and (c) shows the eye obtained for the 500MHz signal data input.



(a)



(b)



(c)

Figure 5.5 : (a) shows the 1GHz input data given to the transmitter, (b) shows the output data received at the receiver and (c) shows the eye obtained for the 1GHz signal data input.

Chapter 6 Discussion

6.1 Critiques and Future scope

The main objective of this work was to implement a transceiver with an on-chip antenna. The system was successfully implemented considering the fact that we used 0.18um CMOS technology. The highest frequency we were able to attain after comparing all components was 22G, which in the end limited the reduction in the size of the antenna used. The on-chip antenna is found to be highly directional making it suitable for chip testing but probably not suitable for other applications which require large distances communication or signal to be radiated in all directions.

The limiting factor of this system was mostly because of LNA. The LNA used in this system restricted our plan of using higher frequency. The Gilbert mixer along with the receiver circuit is able to demodulate only up to 1Gbps data. Improving the LNA and mixer for much higher frequency seems probable in lower channel length technologies.

6.2 Conclusion

As for this research, we were successfully able to implement a system with on chip antenna and showed a testing alternative for IC's. The original plan was to design the whole system at much higher frequency so as to reduce the size of the antenna. Probably in processes with smaller channel lengths this system implementation will be more meaningful as it will reduce the size of the antenna along with the transceiver circuit as achieving higher frequencies in lower channel length processes is much easier.

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