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RF TRANSCEIVER DESIGN FOR ELECTRONIC TOLL COLLECTION (ETC) SYSTEM USING COMPACT DIPOLE ANTENNA

by

Anjana Chowdary Devineni

Thesis submitted to the
Benjamin M. Statler College of Engineering and Mineral Resources
at West Virginia University
in partial fulfillment of the requirements
for the degree of

Master of Science
in
Electrical Engineering

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Yaser P. Fallah, Ph.D.

Lane Department of Computer Science and Electrical Engineering

Morgantown, West Virginia
2015

Keywords: CMOS, Electronic Toll Collection (ETC), Low Noise Amplifier (LNA)

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Abstract

RF Transceiver Design for Electronic Toll Collection (ETC) System Using Compact Dipole Antenna

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Electronic Toll Collection (ETC) system is one of the types of traffic control system that has rapid development in the recent years. ETC system is one of the major applications of Dedicated Short Range Communication (DSRC) which operates in the frequency band of 5.8GHz, used for the transfer of information between the road side unit (RSU) and the on board unit (OBU) which are situated at the toll station and on the vehicle respectively. The working of the system is based on RFID technology. ETC system is implemented in the 0.18µm CMOS technology, which is an aggressive technology in terms of its low cost and easy integration of the RF circuits.

A compact dipole antenna based low-cost RF transceiver for ETC system is designed in this thesis. Amplitude Shift Keying (ASK) modulation technique is employed in the implemented RF transceiver. In transmitter side, a class-E power amplifier is used to amplify the signal power. In order to send and receive the signal, a dipole antenna operating at a frequency of 5.8GHz is used. A low-power and energy efficient Low-Noise Amplifier (LNA) is used in the receiver block which consumes very less power and has a minimal noise figure compared with prior arts. A self-mixer is used for the down-conversion of the signal. Results of this design demonstrate the working of the transceiver at 5.8GHz frequency up to an input data rate of 400 Mbps.

Dedication

To My Parents

To My Advisor Professor Byun

Acknowledgements

I would like to thank my advisor Professor Byun for his encouragement and support and guiding me efficiently throughout my research. I couldn't have done this without his constant support. I wish to express my sincere gratitude to my committee members Professor Graham and Professor Fallah for their time and cooperation. I would like to thank my lab mates for helping me at different stages of my research. I am deeply grateful to my parents Mr. Rajendra Prasad and Mrs. Suseela. This work couldn't have been completed without their endless love and support. Love you mom and dad. You are a great source of inspiration and motivation for me. Also, I would like to thank my friends who were always with me in my tough times.

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1 INTRODUCTION

1.1 ELECTRONIC TOLL COLLECTION (ETC) SYSTEM

One of the important applications in the wireless communication is the Electronic toll collection (ETC) system which is mainly designed for the purpose of avoiding the delays caused on the roads due to the collection of tolls from the vehicles. The system determines the type of vehicle whether it is enrolled in the ETC system or not and accordingly collects toll from the vehicle electronically without requiring the vehicle to stop. Wireless communication takes place for collection of tolls between an antenna which is installed on the toll gate and the on-board equipment which will be discussed in the following paragraph. For the vehicles that are not equipped with an ETC system or those who doesn't have ETC card the operation of ETC system can be explained in two steps. In the step 1, an ETC card be rented anywhere in the airport when the car is picked. In the step 2, the ETC card is inserted into the ETC device at the exclusive ETC equipped gate or at general or shared ETC gate. At exclusive ETC gate only the cars with the ETC card can be passed, whereas at the general gate both the cars that are with and without ETC card can be allowed, however those that doesn't have ETC card have to pay the toll at this gate. Main disadvantage of this kind of shared gates is that even if the vehicle possesses the card it should wait if it is followed by any non ETC equipped vehicle so that the wait time increases in this case.

The ETC system uses RFID technology. This system uses mainly dedicated short range communication (DSRC) between the on board unit (OBU) which is installed on the vehicle and the roadside unit (RSU) which is installed at the toll collection station (1) as shown in the Figure 1.1. The vehicles that are equipped with OBU can be passed without stopping at the toll station. Toll can be collected automatically as all the vehicles that are equipped with ETC are recorded and the toll is automatically deducted from their accounts. Korean and Japanese ETC systems use the 5.8 GHz DSRC system by utilizing ASK modulation. Many of the previous implemented works uses SiGe-BiCMOS process which is expensive and uses lots of external components like filter and all (2). So in order to make it more efficient by reducing the cost and size, a fully

integrated CMOS transceiver is implemented which is more compatible and can be easily integrated with another applications such as car navigation, smart phones etc. ETC system is designed such that each vehicle is detected only by one toll gate such that data exchange between the toll system and the vehicle is guaranteed. Main control of the system lies with the receiver as it must communicate properly with the toll gate. Receiver should have accurate sensitivity in order to determine the toll gate properly. If the receiver has low sensitivity it cannot determine its nearest toll gate properly and as a result interference may occur with other gates and thus this causes interruption in detecting the vehicle (2). So LNA is placed at the first stage of the receiver in order to minimize the noise and power consumption with sufficient gain and low input return loss. Another key aspect that should be considered while designing is that it should consume very less power. In many of the previous works using ASK modulation, a phase locked loop (PLL) is used for down converting the RF signal to base band signal. However in this design without using PLL, low power consumption is achieved using LNA. Antenna should be designed such that it doesn't interfere with other band of frequencies and should have only a narrow beam with high gain.

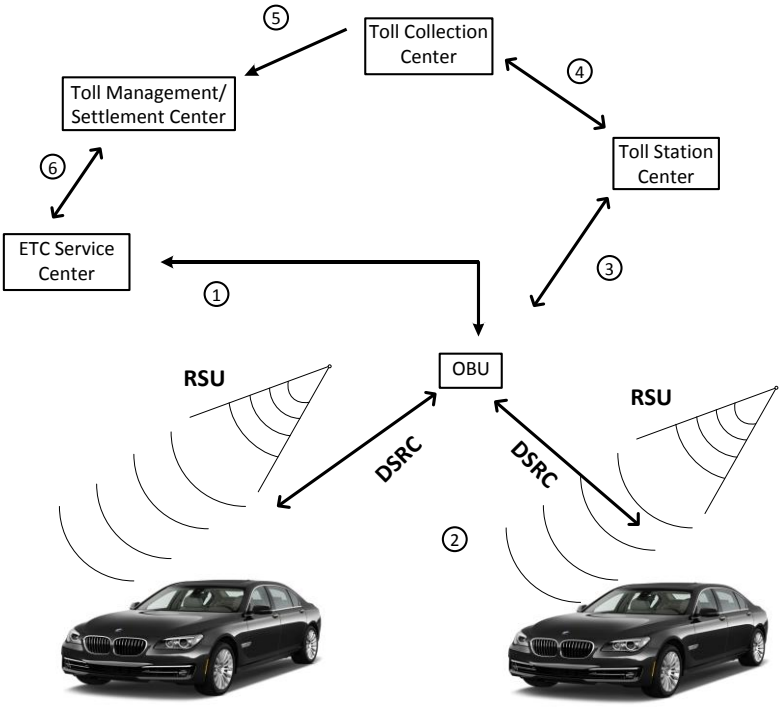


Figure 1.1: ETC system block diagram

1.2 THESIS ORGANIZATION

This thesis is organized as follows. Chapter 2 presents a detailed explanation of RF transmitter and various components that are used as a part of RF signal transmission. Chapter 3 describes the overview of RF receiver block which mainly concentrates on the design of low noise amplifier (LNA) which is the key component of the receiver. Other components that are used in the receiver are also discussed briefly in this section. Antenna Design is discussed briefly in chapter 4. Chapter 5 presents the final layout of the transmitter and receiver and the final post extracted results at different data rates. The future scope of this work is discussed briefly and suggestions are given.

1.3 CONTRIBUTION

A compact dipole antenna based RF Transceiver for Electronic Toll Collection (ETC) System has been implemented in this work. As a part of this, RF Transmitter and RF Receiver blocks were designed and simulated. A capacitor cross coupled common-gate LNA is the proposed design in the RF receiver block. EM simulator ADS has been used for the implementation of compact off-chip Dipole antenna for the frequency of operation at 5.8 GHz. Antenna substrate design was based on the specifications of the PCB.

2 TRANSMITTER

Transmitters are generally used to generate and transmit electromagnetic waves that are carrying messages or signals. Transmitter generates alternating current which is applied to the antenna and thus the antenna produces radio waves. There are many applications of the transmitters in day-to-day life as they are used in radios, mobile phones, wireless computer networks, aircrafts, radar sets, etc. The main function of transmitter is to combine the data signal which is the carrier signal with the radio frequency signal and thus generates a modulated signal.

In the following paragraphs, RF transmitter architecture which includes VCO, an ASK Modulator and an RF Power Amplifier is presented along with the circuit, layout and the post extracted simulation results.

RF TRANSMITTER

General architecture of the RF transmitter is as shown in Figure 2.1. It consists of a Voltage Controlled Oscillator (VCO), ASK Modulator and a Power Amplifier (PA) which operate at 5.8 GHz signal frequency.

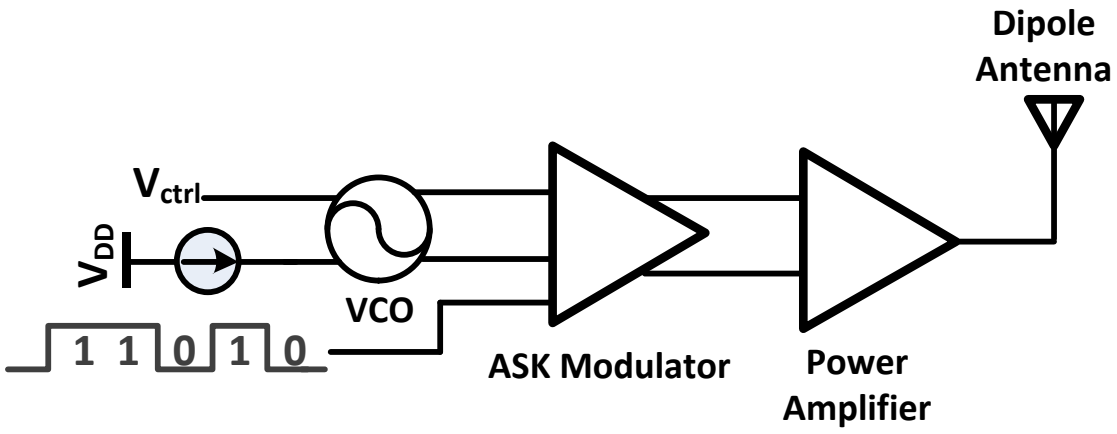


Figure 2.1: ASK transmitter block diagram

2.1 VCO

A voltage controlled oscillator is the most important building block in many analog and digital circuits. The VCO is an electrical circuit which generates an output voltage that is oscillatory. The output voltage of VCO changes in accordance with the applied input voltage. VCO'S operate in a wide range of frequencies i.e from a very low frequency (few Hz) to a very high frequency (hundreds of GHz). VCO center frequency is determined as the periodic output signal generated when the control voltage of the VCO is set at zero voltage. By tuning the control voltage of the VCO, the desired center frequency can be obtained. For a general VCO design, capacitors which are used as varactors control the oscillation frequency of the VCO. One or more than one varactors also may be employed for this purpose of adjustment of the frequency of the oscillations of the VCO. VCO can be implemented in many ways and ring VCO and LC-VCO are among the commonly used type of oscillators.

2.1.1 RING VCO

Ring oscillators are generally specified as they are made from many gain stages or delay stages in feedback i.e. output of the last stage is fed back to the input of the first stage. There are many tradeoffs involved in the design of the ring oscillator such as speed, power, area and application domain (3). A ring VCO is generally used in the clock generation subsystem. As it is easy to integrate, ring VCO is used as the basic building block in many digital and analog circuits. Main application of ring VCO is it used as a clock recovery circuit in many serial data communications. Basically, a ring VCO must provide a phase shift of 2π and also it will provide a unity gain at the center frequency which is the oscillation frequency. If there are N stages in any ring VCO, then each stage must provide a phase shift of π/N which contributes to a phase shift of π and left with a phase shift of π to complete the total phase shift of 2π. So, the remaining phase shift is provided by the DC inversion (4). The delay stages for any ring VCO may be single ended or differential. For DC inversion to take place, odd number of stages say 2N+1 are used for a single ended delay stage and even number of stages say 2N are used for a differential delay stages. Ring VCO with both single ended and differential delay stages are as shown in the Figure 2.2.

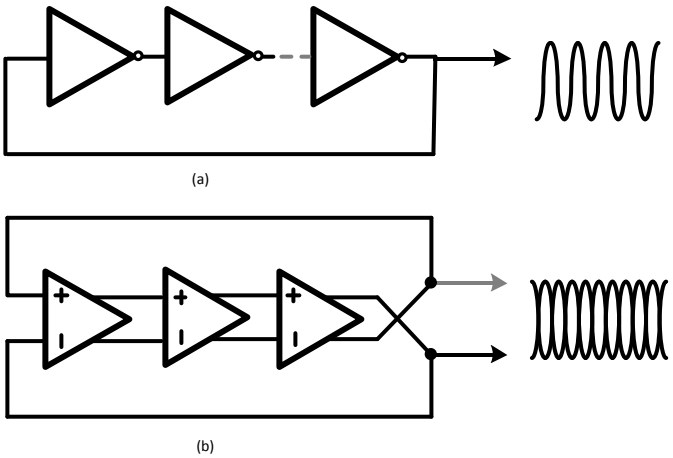


Figure 2.2: (a) Single-ended Ring Oscillator

(b) Differential Ring Oscillator

Usually ring VCO is preferred over LC-VCO in some cases because it consumes less chip area as there is no need to use bulky inductors as in LC-VCO and also the power consumption for ring VCO is very less when compared to LC-VCO. However, achieving good frequency stability by using ring VCO is very difficult. Also ring VCO has more phase noise when compared to LC-VCO as ring VCO consumes 450 times more current than LC-VCO in order to achieve same phase noise (5). As the impact of noise is more in any communication channel, it is better to avoid the noise impact in order to get good signal strength. As the ETC system requires a frequency of exactly 5.8 GHz and also the noise interference should be minimized in order to receive the signal from the vehicle, so due to this reason we preferred LC-VCO in our circuit rather than ring VCO.

2.1.2 LC-VCO

LC-VCO also referred to as LC tanks are made up of series or parallel connected inductors and capacitors. Generally LC tanks may contain both resistive and reactive components. In most of the cases, LC tanks are usually represented as series or parallel RLC circuits (6) as shown in the Figure 2.3. For both series and parallel RLC networks, the impedance function can be expressed as shown in equations 2.1 and 2.2:

$$Z(j\omega) = \frac{1}{\frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right)} \qquad (Parallel\ RLC\ circuit)\ (2.1)$$

$$Z(j\omega) = R + j(\omega L - 1/\omega C) \qquad (Series\ RLC\ circuit)\ (2.2)$$

The resonant frequency of the LC tank is denoted by ω_0 is given by equation 2.3 as:

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (2.3)$$

From the above equation resonant frequency ω_0 is equal to the resistance R and hence the impedance of the circuit is purely resistive and phase is equal to zero. Below the resonant frequencies the impedance of the circuit is inductive. For frequencies above the resonance, the impedance of the circuit is mostly capacitive. For the series RLC circuits, the conditions are

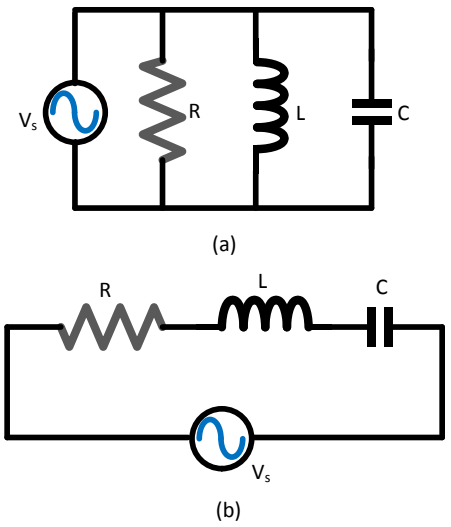


Figure 2.3: (a) Parallel LC tank

(b) Series LC tank

completely opposite. Also, for any inductor the most important factor to be taken into consideration is the Q factor. Q factor is the one which determines the bandwidth of any inductor relative to its center frequency (f_c). If a particular inductor has a high Q factor, then it means that there is low damping such that the oscillations of the circuit are continuous for a longer time. Also, higher Q factor has a higher rejection of spectral energy away from the

resonant frequency. Usually for any inductor, Q factor peaks at the center frequency of the oscillations. Conventionally, Q factor is expressed in terms of resonant frequency (f_r) as:

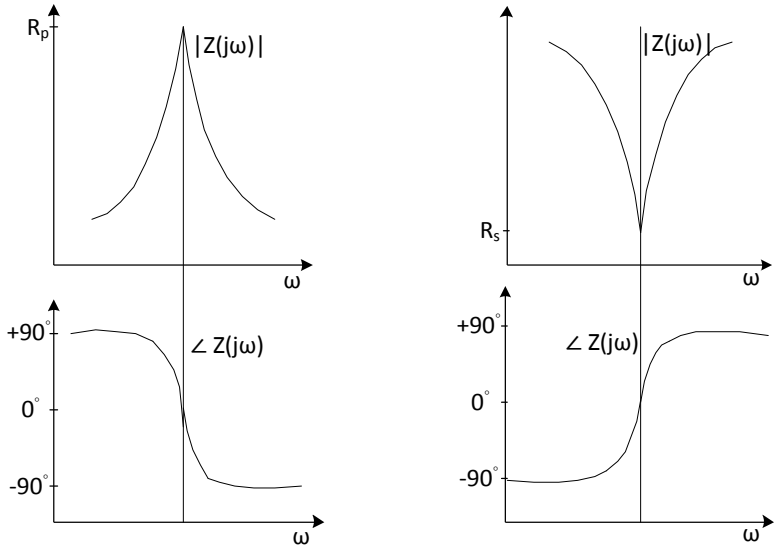
$$Q = \omega \frac{Energy\ stored}{Average\ power\ dissipated} \tag{2.4}$$

$$Q = 2\pi f_r \frac{Energy\ stored}{Average\ power\ dissipated} \tag{2.5}$$

The Q factor also describes the steepness of the phase of the impedance or the sharpness of the magnitude of the impedance. So, Q factor at -3dB bandwidth can also be given as follows:

$$Q = \frac{\omega_0}{\omega_{-3dB}} \tag{2.6}$$

At resonance, the Q factor of the series and parallel RLC circuits can be expressed as follows:



(a) (b)

Figure 2.4: Magnitude and phase diagrams for (a) Parallel and (b) Series LC tank

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \qquad \text{(Parallel RLC circuit)} \tag{2.7}$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \quad \text{(Series RLC circuit)} \quad (2.8)$$

2.1.3 CROSS-COUPLED DIFFERENTIAL TOPOLOGY

Many methods are considered in the design of LC VCO's which includes linear feedback methods and negative resistance concepts. So the same analysis methods are used in the design of LC-VCO. The oscillator can use more than one LC resonator in order to achieve differential operation and hence this configuration of LC-VCO is called as cross-coupled differential oscillator or a negative-g_m oscillator (7). Negative resistance is seen at the drain of M_1 and M_2 and expressed as (8):

$$R_{in} = -\frac{2}{g_m} \quad (2.9)$$

For any cross-coupled differential configuration of transistors, LC VCO can be designed in four topologies which may have NMOS and PMOS devices. So we can have two topologies with NMOS with tail current either at the source or at the drain terminal. In the same way for the PMOS devices, tail current can be either at the source or at the drain terminal as shown in the Figure 2.5.

Negative resistance approach:

$$=> \frac{1}{R_a} + \frac{1}{R_f} \leq 0 \quad (2.10)$$

$$R_a = -\frac{2}{g_m} \quad (2.11)$$

The resistance R_a must be greater than or equal to $1/g_m$ and hence the circuit can be described as negative transconductance oscillator. One of the sources of noise in any VCO circuit is contributed by the tail current. The noise produced is called flicker noise which is later converted to as phase noise for the VCO. So, for this reason the oscillations of the VCO should be symmetric and hence device sizes of both the NMOS are made equal.

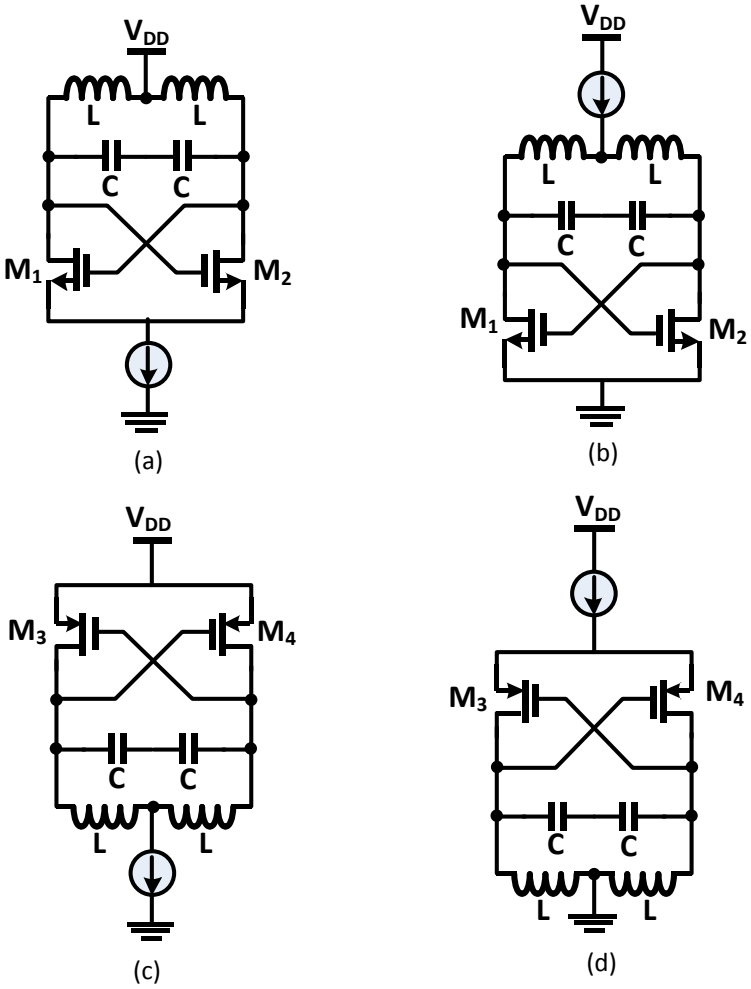


Figure 2.5: Cross-coupled differential topology (a) with an nMOS pair and a tail current at the source (b) with an nMOS pair and a tail current at the drain (c) with a pMOS pair and a tail current at the drain (d) with a pMOS pair and a tail current at the source.

Small signal model of the cross coupled LC-VCO with non-ideal LC tank is shown in the Figure 2.6. By analyzing the small signal model, the natural frequency of oscillations of the VCO can be determined. As the VCO is symmetric, analysis of small signal model of the half circuit is done. By using Voltage law,

$$g_m V_{in} + \frac{V_{out}}{r_0} + sC_1 V_{out} + \frac{V_{out} - V_L}{R_1} = 0 \tag{2.12}$$

$$\frac{V_L - V_{out}}{R_1} + \frac{V_L}{sL_1} = 0 \tag{2.13}$$

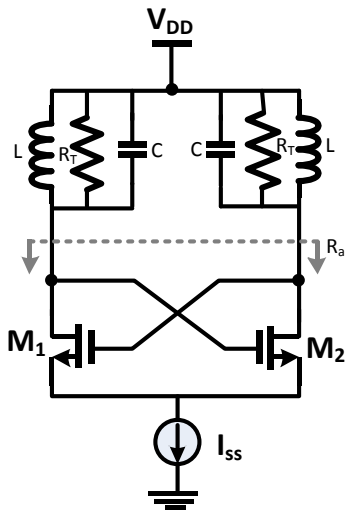


Figure 2.6: LC-VCO with non-ideal LC tank

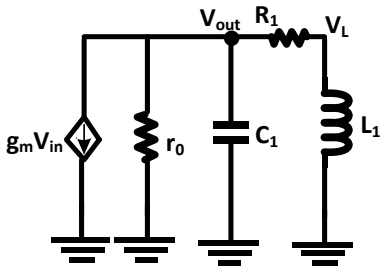


Figure 2.7: Small signal model of the LC-VCO

Solving for transfer function from the two equations 2.12 and 2.13, we get H(s) as shown in equation 2.14.

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m r_0 s(R_T + sL_1)}{s^2 r_0 C_1 L_1 + s(L_1 + r_0 C_1 R_T) + r_0 + R_T} \qquad (2.14)$$

Solving the denominator part for getting the frequency of oscillation by plugging in s=jω and equating the imaginary part to zero, we get the value of ω=$1/\sqrt{L_1 C_1}$.

From the Figure 2.8 (6) R_a is the resistance of the differential cross-coupled transistors, R_f is the parasitic resistance created from the frequency selective network and g_m is the small signal transconductance of the any of the transistors M_1 and M_2 as both the transistors are of the same size to achieve equal output resistance of $1/g_m$, which is considered to be as a negative

resistor. Of all the VCO topologies, tail-based NMOS design saturates slowly and hence has higher output oscillations when compared to the others. So this topology is implemented in this design.

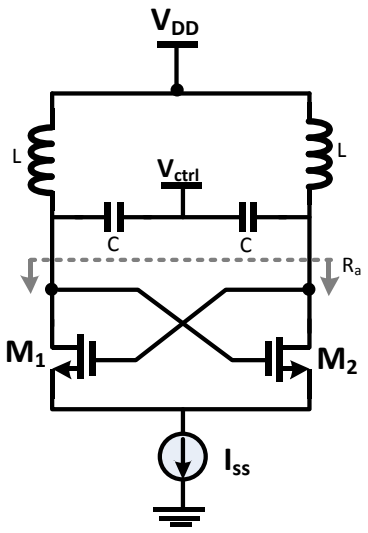


Figure 2.8: NMOS cross-coupled LC VCO used in this design

2.1.4 ON-CHIP INDUCTORS

As the growth of the modern wireless communications through wireless local area networks is increasing in day-to-day life and demand for smaller size and lower cost products is increasing, requirement of highly integrated monolithic microwave integrated circuits are needed. Traditionally off chip inductors are often used in many circuits due to their good quality but at the same time using many off chip components increases the area and cost. For this purpose using on-chip inductors in wireless communication systems is desirable. On-chip inductors are used mostly in narrow-band loads, resonators and matching networks in RF circuits. Use of such kind of on-chip inductors improves the circuit performance in terms of noise figures, insertion loss, gain and efficiency (9). Q factor of the inductor mainly depends on shape, width, thickness, spacing and diameter of an inductor. Usually by using these on-chip inductors, losses also should be considered in their design. Losses in on-chip inductors are mainly classified as metal losses and substrate losses.

Choice of geometry is chosen such that there should be minimum losses and the design should be area efficient. Inductor design may be square shaped, circular, octagonal or spiral. Among all the designs of on-chip inductors, circular structure has higher Q factor when compared to others (10). For any structure, higher inductance can be obtained within less space by filling the inner space with more number of turns so that the effective area is also reduced. But as we increase the number of turns, substrate layers are closer to the inductor which accounts for substrate losses and hence self-resonance is lowered. So, to overcome this kind of substrate losses thickest possible metal layer should be placed to minimize the substrate capacitance. By using these thick metals not only substrate losses are reduced also self-resonance of the inductor is increased. In this design, we used two single-ended inductors which is termed as a differential inductor so that the twice the inductance value is obtained and layout is compact and common mode losses are suppressed and the quality factor is also improved (11). In this design, top metal layers M6 and M5 i.e. AM and MT layers are used in the inductor design in order get high Q factor at the desired frequency of 5.8GHz (12). The turns of the inductor are designed using AM layer considering that the effect of losses are less, whereas the contact between the outer and inner turns is made by using MT layer.

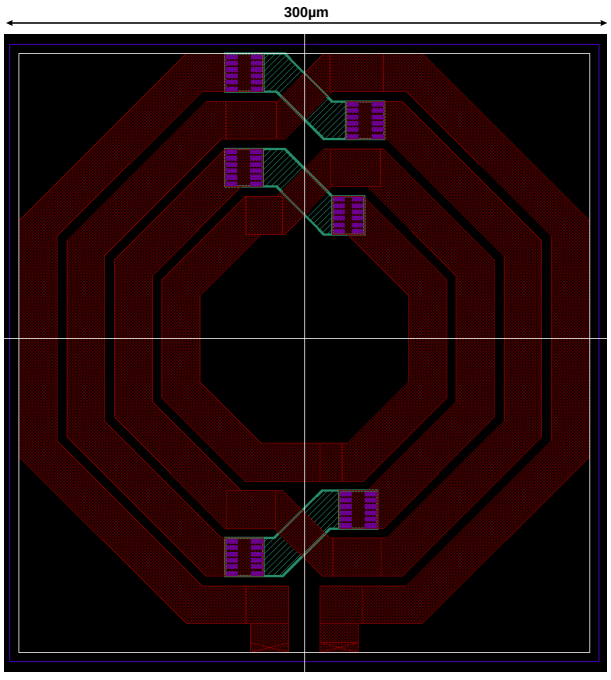


Figure 2.9: Inductor layout

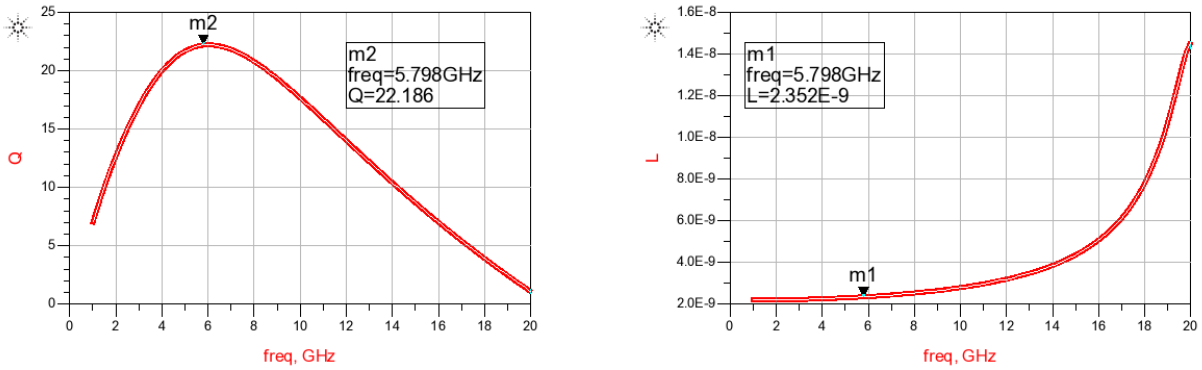
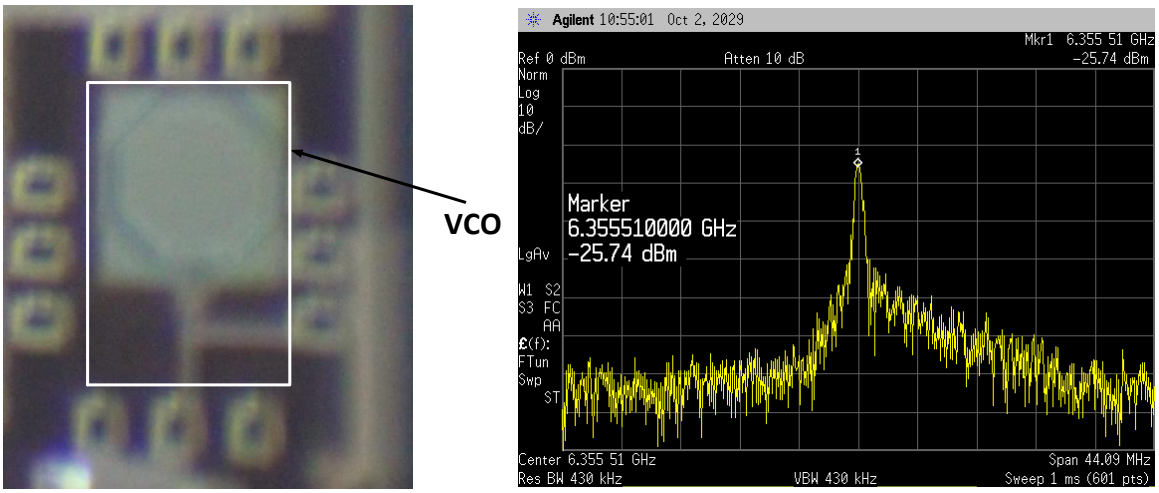


Figure 2.10: Measured quality factor (Q) and inductance (L) values of the inductor at 5.8 GHz frequency

Figure 2.9 shows the inductor layout used in the design of LC-VCO. In order to get a high Q factor i.e. any value greater than 15 at the central frequency of ETC system i.e. 5.8 GHz, a 300 µm radius inductor with four turns and with the width of each turn equal to 20 µm is used. From the figure it can be noticed that a good quality factor is achieved at the required frequency. Power to the inductor is supplied through its center tap. Differential output of the VCO is measured at the two terminals of the inductor. Total power consumed by the VCO is measured as 11.6 mW. Figure 2.11 shows the die photo and the VCO frequency plot for a frequency of 6.35 GHz.



(a) (b)

Figure 2.11: (a) Die photo of VCO (b) VCO frequency plot from the chip test

Figures 2.12 and 2.13 shows the output spectrum and output signal of the Voltage controlled oscillator respectively after post extracted simulation.

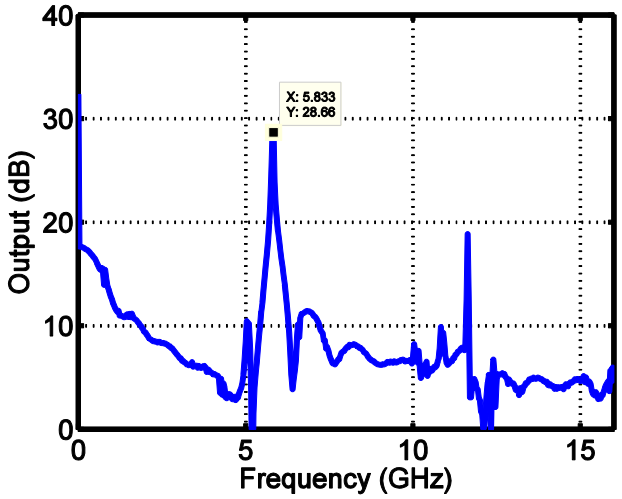


Figure 2.12: VCO spectrum at ETC frequency

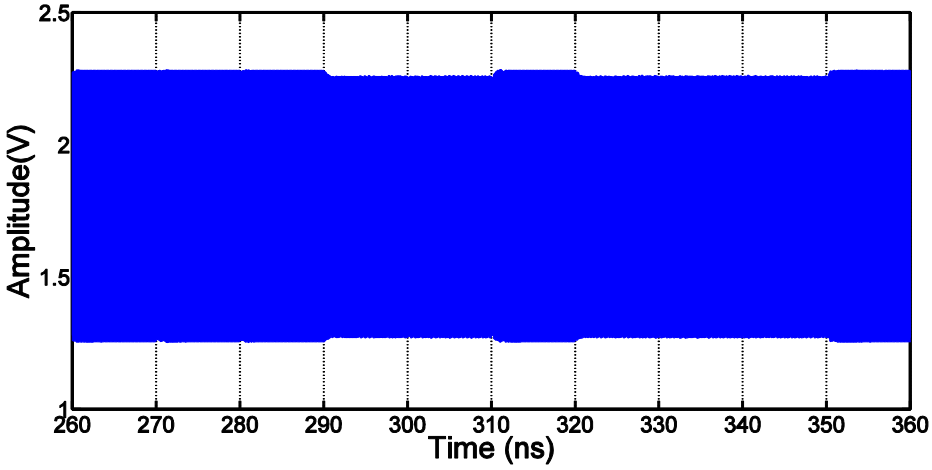


Figure 2.13: VCO output at 5.8 GHz frequency

2.2 MODULATOR

Generally modulation technique in any communication channel is used for the purpose of transmitting information by using a carrier wave. Amplitude modulation in particular is varying the amplitude of the carrier wave in accordance with the modulating signal. This simply means if the data input is high, then the carrier signal is transmitted and if the data is low, then

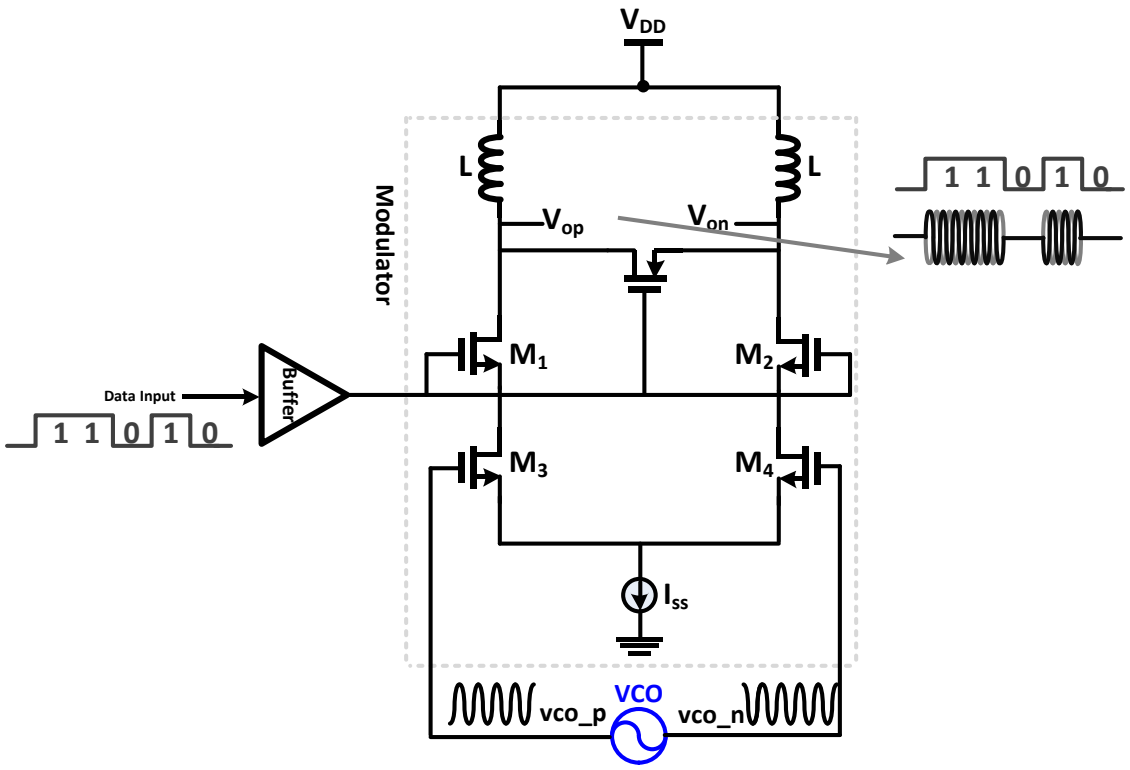


Figure 2.14: Modulator with VCO

the carrier signal is not transmitted. Figure 2.14 shows the modulator circuit coupled with VCO and the RF data source. The carrier signal is directly fed into the transistors M_3 and M_4 of the ASK modulator and the transistors M_1 and M_2 acts as a switch for modulating the carrier signal (13). Important thing to be considered while designing a modulator is that it should operate at the same center frequency of 5.8GHz like the VCO. Modulator block consumes a power of 12.05mW. Layout of the VCO with modulator and its post extracted simulation results are as shown in the Figure 2.15 and Figure 2.16 respectively.

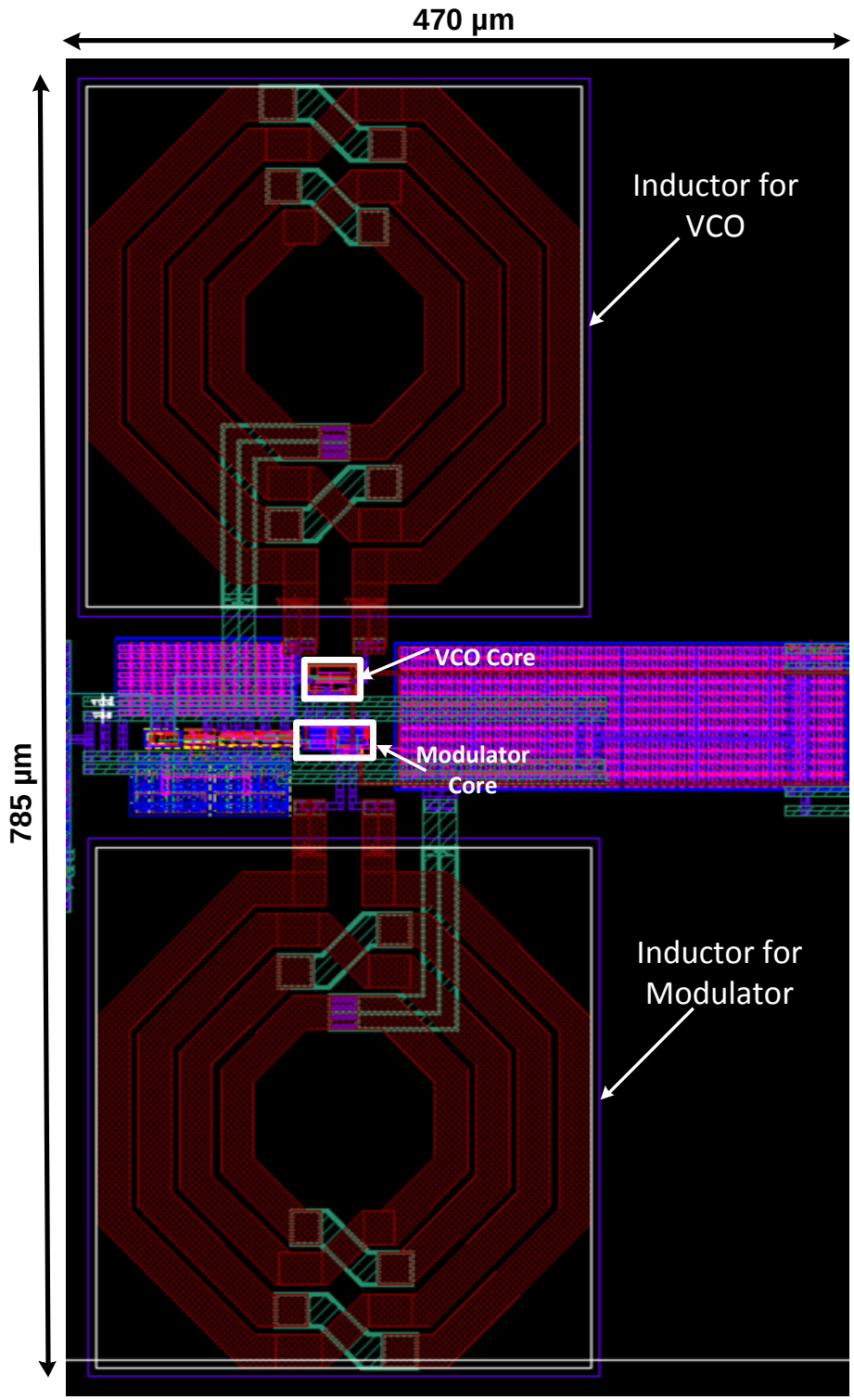


Figure 2.15: Layout of the VCO and Modulator

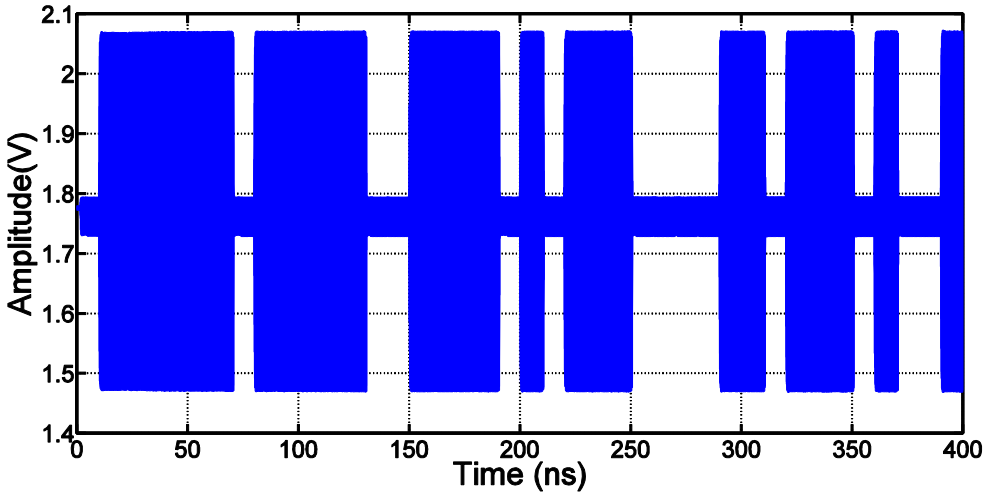


Figure 2.16: Modulated output at 5.8 GHz frequency

2.3 POWER AMPLIFIER

In the real world, power amplifiers are used to amplify the signals without compromising the signal integrity so that the information is transmitted to the next level. Amplification of the input signal (P_{IN_RF}) is done by converting the available DC power (P_{DC}) to RF output (P_{OUT_RF}) without any change in the shape of the input signal. Some of the power which is not converted to output is dissipated as heat, which is shown in Figure 2.17.

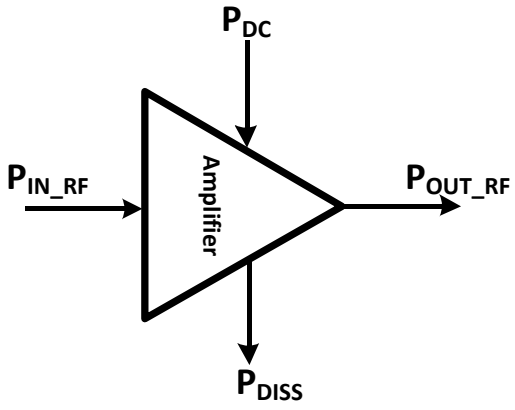


Figure 2.17: Power diagram of RFPA

Figure 2.17 has two inputs P_{IN_RF} and P_{DC} and two outputs P_{OUT_RF} and P_{DISS} where P_{DISS} is the dissipated heat at the output. The supply efficiency is given by η_s which is the ratio of output power obtained to the total DC power consumed and is given by

$$\eta_s = \frac{P_{outrf}}{P_{DC}} \tag{2.13}$$

Input RF power is not taken into consideration for calculating the supply efficiency, however the power-added efficiency (PAE) by considering the RF input power and the amplifier gain (G_{rf}) is given by (14)

$$PAE = \frac{P_{outrf} - P_{inrf}}{P_{DC}} \tag{2.14}$$

$$PAE = \frac{P_{outrf} - \frac{P_{outrf}}{G_{rf}}}{P_{DC}} \tag{2.15}$$

Gain in dB is usually expressed as the ratio of output power to the input power as

$$G_{dB} = 10\log_{10}\frac{P_{outrf}}{P_{inrf}} \tag{2.16}$$

Another way to define the overall efficiency (η_{total}) of a PA is given by

$$\eta_{total} = \frac{P_{outrf}}{P_{DC} + P_{inrf}} \tag{2.17}$$

η_s and η_{total} are the best methods to measure the efficiency of the PA.

2.3.1 CLASSES OF OPERATION OF PA

While designing any PA, there are a lot of tradeoffs between efficiency and linearity. So the main classification in power amplifiers is based on their linearity and switching. Class-A, B, AB and C power amplifiers have similar circuit configuration and operate based on their linearity and distinguished primarily based on their biasing conditions. Class- A power amplifier is a completely linearly operated amplifier as it produces output exactly as the input without any clipping. However the efficiency is low for this type of amplifiers and to improve efficiency,

which eventually decreases the linearity, reduced conduction angle is proposed. Main concept involved is to bias the active devices with low quiescent current and to turn the active devices using input signal. Based on this conduction angle concept, biasing of amplifiers from Class- B, AB and C are categorized (15). They are usually termed as transconductance amplifiers. A general topology for Class- A, B, AB and C amplifiers are shown in Figure 2.18. The main drawback of these amplifiers is that the amplitude is limited, have less efficiency and require very large current to deliver power.

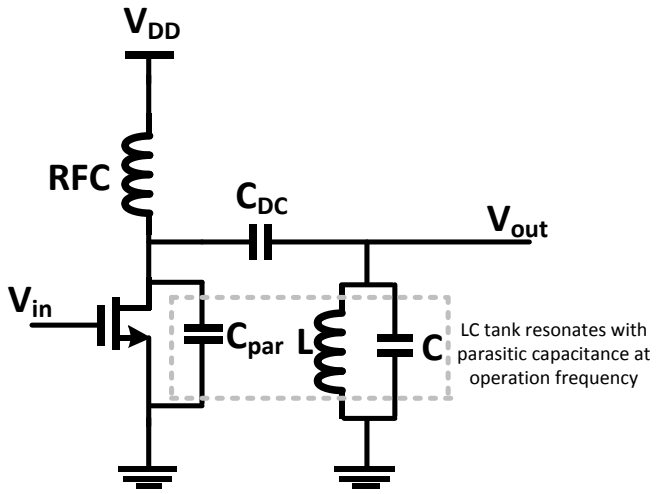


Figure 2.18: General topology for class-A, B, AB and C power amplifiers

Class- D power amplifiers mainly consist of voltage controlled switch. The output network for this type is tuned to the fundamental frequency. As the output device is fully switched, they have maximum efficiency and sometimes referred to as digital amplifiers as they are fully switching, ON and OFF. These amplifiers employ switching capacitances and this limits their efficiency at high frequencies. Conventional Class- D PA is shown in Figure 2.19.

Class- E PA has higher efficiency when compared to other classes and thus stands out from them. Class- E operation mainly depends on some set of drain voltage and current waveforms. Figure 2.20 shows the conceptual model of Class- E PA. The transistor is modeled as a switch with an intrinsic output capacitance followed by the series resistance. Drain of transistor M_1 is connected to the peaking inductor (L) which is tuned to get a high Q value at ETC system frequency of 5.8 GHz.

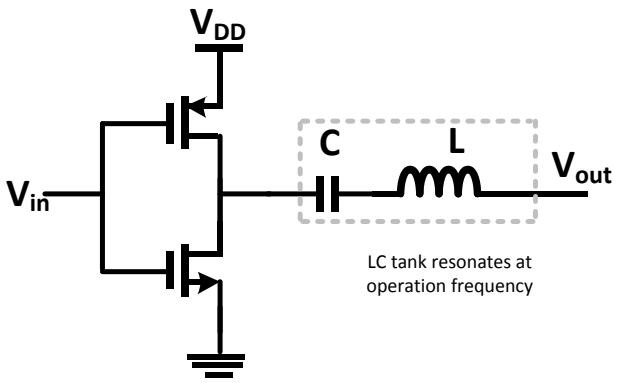


Figure 2.19: A voltage switching class-D power amplifier

The parasitic capacitance C_{par} serves a vital role in the operation of Class- E PA. When the transistor is ON then the drain mode is grounded and hence the supply voltage is applied directly to inductor L. As a result of this, linear current is produced across the inductor and thus used to produce sinusoidal output. In the same way when the transistor is OFF, then the current flows completely through the capacitor which makes the drain voltage to peak.

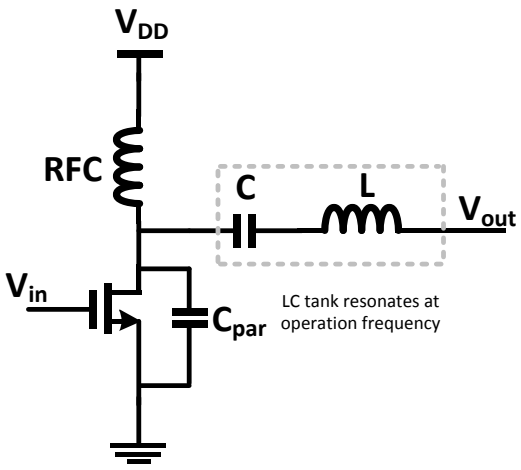


Figure 2.20: A voltage switching class-E power amplifier

The generated output signal has same phase and frequency as the input signal with amplification of the signal along with amplification in power. The size of drain capacitance can be varied from a very low value to a very high value because Class- E PA can allow a larger drain capacitance value and thus a larger overall efficiency can be obtained. As this design involves the use of off-chip antenna and thus need higher efficiency, which is eventually the reason for

choosing Class- E PA over other types of power amplifiers. Total power consumed by the Power Amplifier is measured as 60.3 mW. Layout and post extracted results of the PA and whole transmitter layout are shown in the Figure 2.21 and Figure 2.22, Figure 2.23 respectively.

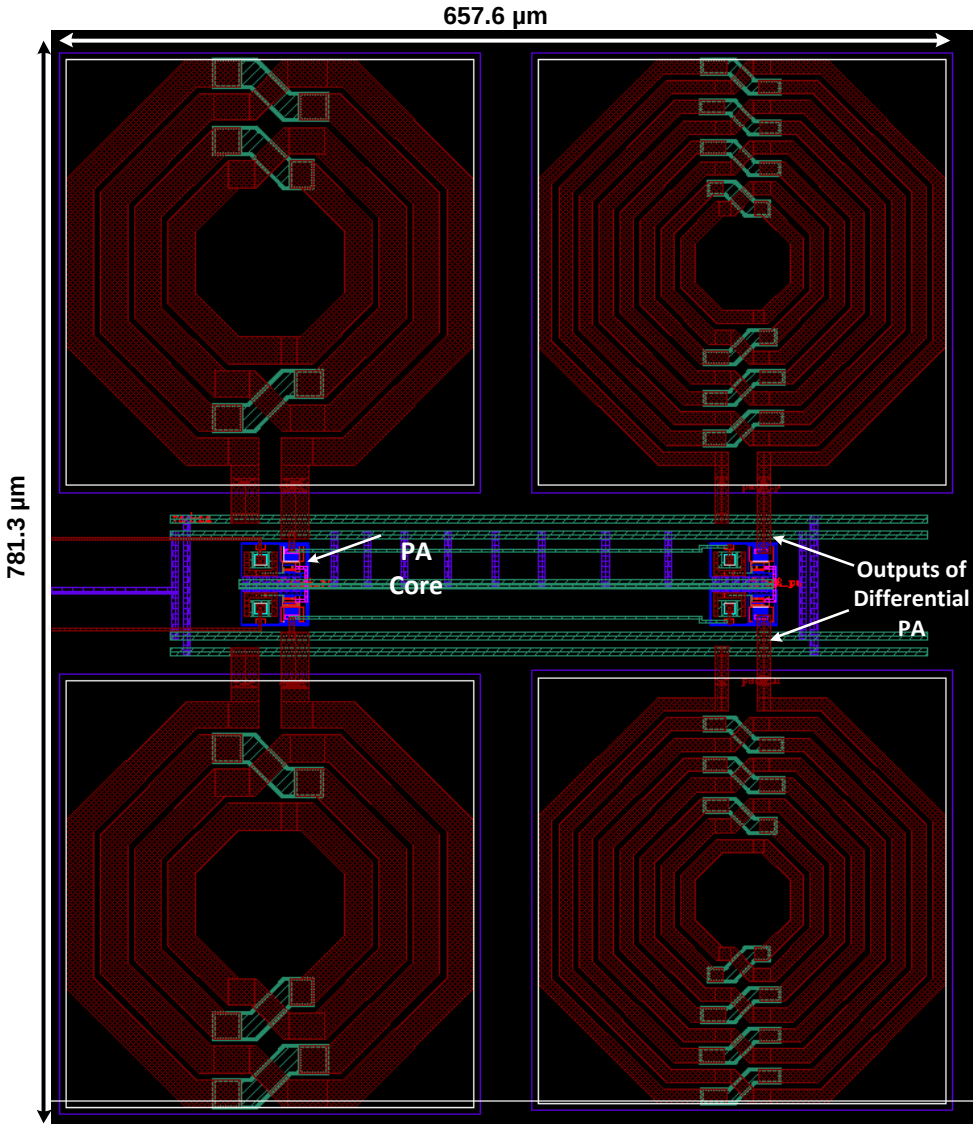


Figure 2.21: Layout of the differential Power Amplifier

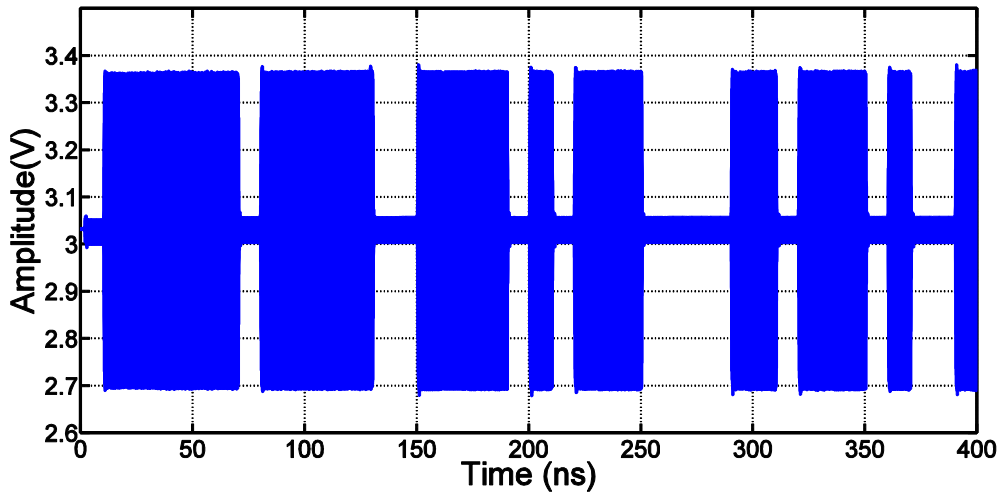


Figure 2.22: Amplified output of the power amplifier at 5.8 GHz frequency

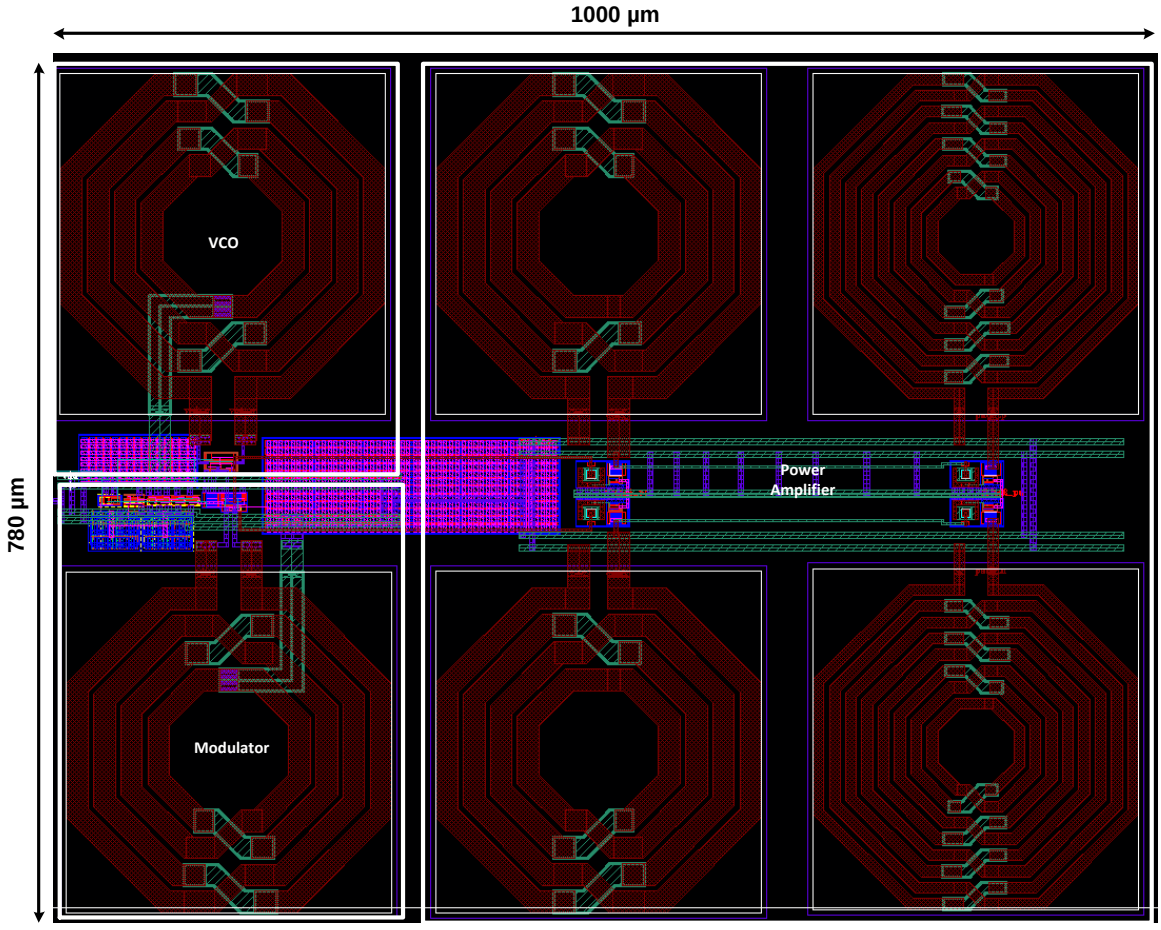


Figure 2.23: Final layout of Transmitter

3 RECEIVER

This chapter presents an overview of RF receiver with detailed explanation of all the components especially LNA. Layout of each component and post extracted results are shown.

RF RECEIVER

The RF Receiver mainly consists of Low-Noise Amplifier (LNA), down-conversion mixer, differential amplifier, buffer convertor and output driver. Block diagram of RF receiver is shown in the Figure 3.1. The transmitted signal from the TX block is received by the off-chip antenna and then it converts them to the radio waves and then transmitted to the receiving antenna. The receiving antenna is situated at the RX block and it is used to transmit the radio waves onto the next block which is the primary consideration in our design i.e. LNA. The design of LNA is shown in the next section which includes its layout, and also a results table which shows the comparison of this work with the previous works at almost the same frequency range.

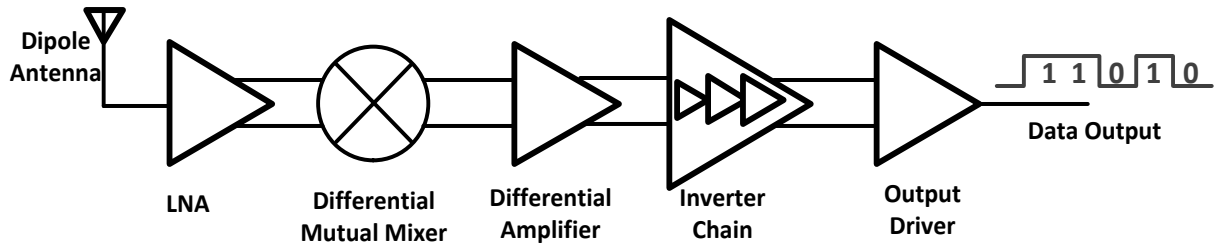


Figure 3.1: Block diagram of RF Receiver

3.1 LOW-NOISE AMPLIFIER (LNA)

A low noise amplifier plays a key role in the receiver block in many wireless communications. This design presents an approach to design a 5.8 GHz capacitive cross- coupled common-gate low noise amplifier (CCCG-LNA) for electronic toll collection system. In this design a low-power low noise amplifier (LNA) for an electronic toll collection (ETC) system that is utilizing 5.8 GHz frequency and is used mainly for dedicated short range communication (DSRC) (16).

In most of the works, ASK transceivers are mostly designed on the basis of low-IF conversion architecture (2) that utilizes a phase locked loop (PLL) and a radio frequency (RF) mixer to convert the RF signal input to the baseband signal output, as shown in the Figure 3.2.

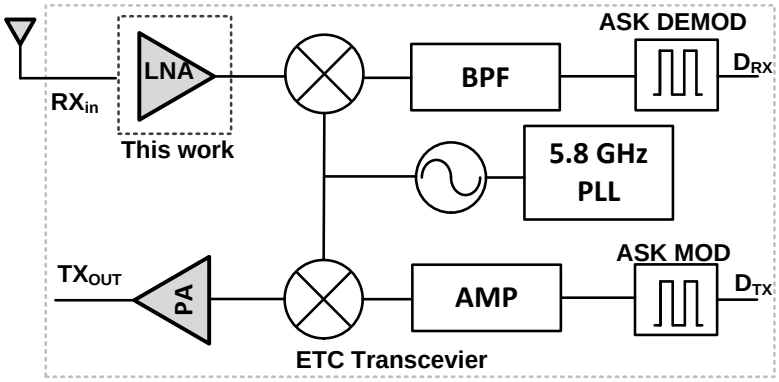


Figure 3.2: Block diagram of ASK Transceiver

An LNA is the most important block of the receiver as it is used to reduce noise distortions from the transmitter part and provide high gain to the receiver part. Designing an LNA for the receiver side is especially one of the major challenges in the aggressively scaled supply (i.e., 0.55 V) for ultra-low-power transceiver design. Furthermore as ETC systems operate at 5.8GHz and a novel narrow band LNA with lower noise figure, higher gain, and low input return loss at aggressively scaled supply should be should be designed to avoid any interference from other frequency bands.

The popular LNA topology is either common source (CS) or common gate (CG) structures (17) (18) (19) (20) (21) (22). A CG-LNA induces more noise when compared to CS-LNA. However a CG-LNA can provide much better noise figure performance with noise reduction techniques such as multiple feedback techniques (20) and noise cancellation methods (21) (22) (23).

3.1.1 Conventional Common-Gate LNA Design

Figure 3.3 shows the typical equivalent circuit for the input stage of a CG-LNA.

The input admittance can be expressed by (17):

$$Y_{in} \approx g_m + s\left(C_{pad} + C_{gs}\right) + \frac{1}{sL_s} \tag{3.1}$$

Where g_m, C_{pad} and L_s are the transconductance of M1 transistor, parasitic pad capacitance and input source degeneration inductor, respectively. The *noise factor (NF)* including the channel noise and induced gate noise (17) is given by Eq. 3.2:

$$NF_{CG-LNA} = 1 + \frac{4kT\gamma g_{d0}\Delta f}{\frac{4kT}{R_S\Delta f}}\left(\frac{1}{g_m R_S}\right)^2 + \frac{4kT\delta g_g \Delta f}{\frac{4kT}{R_S\Delta f}}\left(\frac{1}{g_m R_S}\right)^2 \quad (3.2)$$

Where $g_g = \frac{(wC_{gs})^2}{5g_{d0}}$ and $g_m R_s \approx 1$.

Eq. 3.2 can be further simplified as

$$NF_{CG-LNA} = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{w_0}{w_T}\right)^2 \approx 1 + \frac{\gamma}{\alpha} \quad (3.3)$$

Where α, β and γ are bias-dependent parameters, ω_T and ω_0 are unity current gain frequency and operating frequency of MOSFET respectively.

From the Eq. 3.3, the induced-gate contribution to the noise factor is insignificant. Therefore, if the transconductance (g_m) is increased, the CG-LNA can provide higher gain and low noise figure when compared to CS-LNA (17).

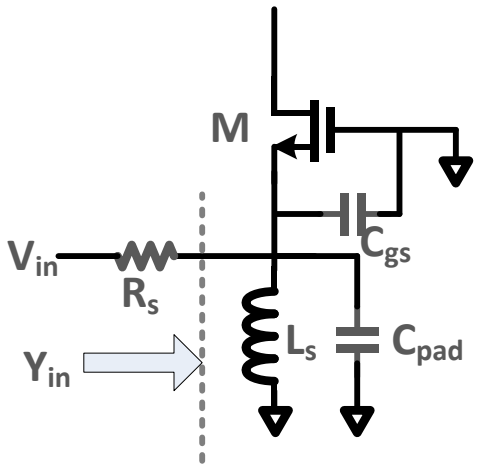


Figure 3.3: Basic CG-LNA stage

3.1.2 G_m boosting for CG-LNA

As gate noise is negligible and hence ignoring gate noise, Eq. 3.3 can be expressed by:

$$NF_{CGLNA} \approx 1 + \frac{\gamma}{\alpha}\frac{g_{mi}}{\frac{1}{R_S}}\left(\frac{1}{G_m R_S}\right)^2 \quad (3.4)$$

Where g_{mi} is the small-signal transconductance and G_m is the total effective transconductance. These both are related using the inverting amplification gain *A* as $G_m=(1+A)g_{mi}$. Considering the inverting amplification gain *A* using g_m boosting, noise factor can be expressed by:

$$NF_{CGLNA} \approx 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)} \tag{3.5}$$

Where $(1+A)\ g_{mi} = 1/R_s$ is the impedance matching for the LNA which is equal to 100 Ω.

3.1.3 CAPACITIVE CROSS COUPLING

CS input stage offers the possibility to achieve low NF by increasing their input quality factor (Q) (24). But the drawback with common source structure is the performance of parameters such as linearity and sensitivity of input matching is degraded. Common gate amplifiers overcome these drawbacks and exhibit better linearity and input matching (23). The capacitive cross-coupling has been used for common-gate structure for enhancing the gain and matching (24). Also by using capacitive cross-coupling the noise figure of common gate structure is improved.

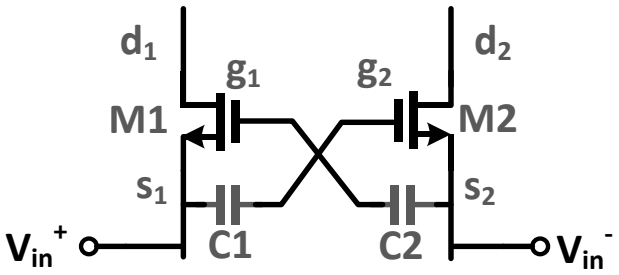


Figure 3.4: Capacitive cross coupling technique

Figure 3.4 shows the circuit of capacitive cross coupled CG- differential LNA. Cross coupled capacitors induce noise at the gate of transistors M_1 and M_2, which is almost insignificant and method to reduce the noise effect is shown in the proposed design.

3.1.4 PROPOSED DESIGN

Figure 3.5 shows the proposed dual capacitive cross-coupling CG- LNA which operates at a frequency of 5.8 GHz. Input signal to the LNA is applied to the differential transistors M_1 and M_2. The capacitors C_1 and C_2 provide positive feedback to the LNA. Due to capacitive cross coupling to CG-LNA, the noise effect from M_1 and M_2 input transistors can be decreased as the

effective transconductance (G_m) of transistors M_1 and M_2 is increased. Moreover, the dual capacitive cross-coupling with input source degeneration inductors can provide enough voltage headroom and aggressive supply scaling, eventually delivering a dramatic power reduction. Plot of noise figure of the proposed CG-LNA is shown in the Figure 3.6. It is difficult to achieve the noise figure of CG-LNA's below 2.5 dB. The simulated noise figure of the proposed design is 2.4 dB. Most of the CG-LNA's achieve less NF at the cost of loss in power consumption or any other parameter (17). But implemented cross coupled CG-LNA is a good example, as it balanced all the parameters in a considerable range.

On chip inductors L_1 and L_2 are used for input matching purpose. There is a tradeoff between measured noise figure and return loss of LNA. As the noise figure is reduced, simultaneously the return loss of LNA will increase. In order to improve the reflection coefficient of the LNA (S_{11}) transistors M_3 and M_4 are cascaded to M_1 and M_2 respectively. Input return loss plot (S_{11}) for the proposed CG-LNA is shown in the Figure 3.7. Simulated refection coefficient parameter (S_{11}) of this design is -15.72dB at a center frequency of 5.8GHz. As there is always a tradeoff between the LNA parameters, due to this capacitive cross coupling NF is reduced, but at the same time gain of the LNA is reduced. So in order to improve the gain of CG-LNA cross coupling transistors M_5 and M_6 are added. As a result of this addition, gain of the LNA is increased. In the same way inductors L_3 and L_4 are used for peaking of gain at the center frequency that is at 5.8 GHz. Gain plot (S_{21}) is shown in the Figure 3.8. The simulated gain (S_{21}) of CG-LNA is 16 dB and the measured voltage gain is about 32.2 dB at 5.8GHz for ETC system which is shown in the Figure 3.9. Linearity is another important parameter which determines how efficiently the LNA is working in the specific frequency range. The dynamic range of the circuit is determined by linearity along with the noise figure (24). The input referred transconductance (IIP3) of the capacitive cross coupled CG-LNA can be obtained using the following expressions (24):

$$IIP3 = 8\sqrt{\frac{2G_s}{3|(-K_{3gm}+K_{2gm}{}^2/G_s)|}} \tag{3.6}$$

$$IIP3 = 4\sqrt{\frac{G_s}{3|K_{3gm}|}} \tag{3.7}$$

Where K_{2gm} and K_{3gm} are the second order and third order transconductance nonlinear coefficients and G_s is the transconductance of the source. Both second and third order coefficients determine the third order intercept point of the LNA. Usually the third order intercept point of capacitive cross coupled CG-LNA is higher when compared to the conventional CG-LNA (24). The third order intercept IIP3 for proposed design is +7.26 dBm. Plot of IIP3 is shown in the Figure 3.10.

3.1.5 SIMULATION RESULTS

The proposed LNA circuit for the Chinese ETC system is simulated in the Cadence Virtuoso simulator in 0.18µm CMOS process. Figure 3.11 shows the layout of the proposed CG-LNA which occupies a chip area of 0.8*1.08 mm^2 including pads. LNA core occupies very less area, whereas most of the occupied space is contributed by the inductors.

The differential LNA in 180nm process consumes 0.58 mW of power from a 0.55 V supply voltage and the output voltage swing at the sources of M_5 and M_6 are sufficient enough to drive 50 Ω output load. The voltage gain of LNA in 0.18µm is 32.2 dB at 5.8 GHz center frequency. The measured power gain (S21) is 16 dB at the same frequency.

The simulated reflection coefficient (S11) for the proposed design is -15.72 dB at 5.8 GHz. Simulation in 0.18µm process gives a NF of 2.4 dB. Third order intercept point (IIP3) for the proposed design is about +7.26 dBm. Noise figure and S- parameters are simulated through Golden Gate simulator in Cadence.

Table I shows the performance summary of this work and the comparison results of this work with the narrowband LNA's of almost the same range. The proposed design has low power consumption and good gain when compared to the previous works.

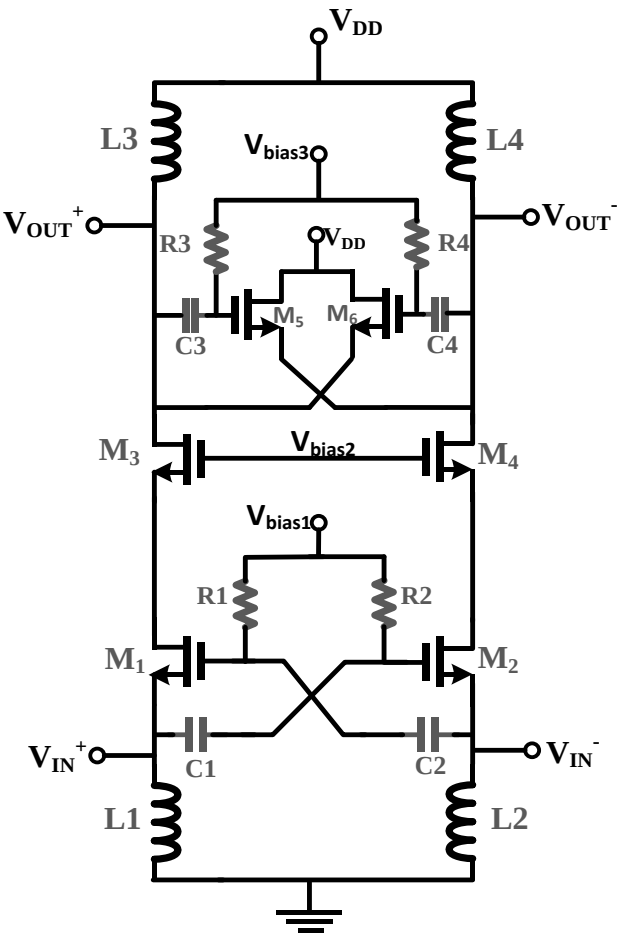


Figure 3.5: Proposed CG-LNA

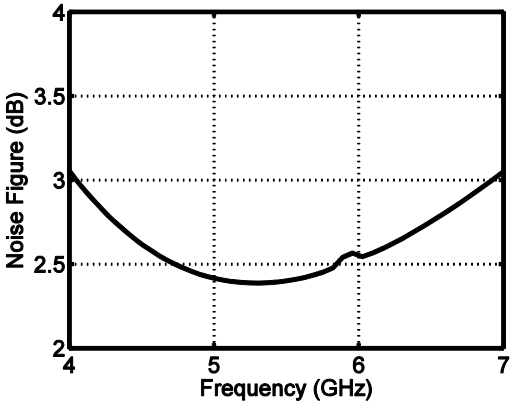


Figure 3.6: Simulated Noise Figure vs input signal frequency

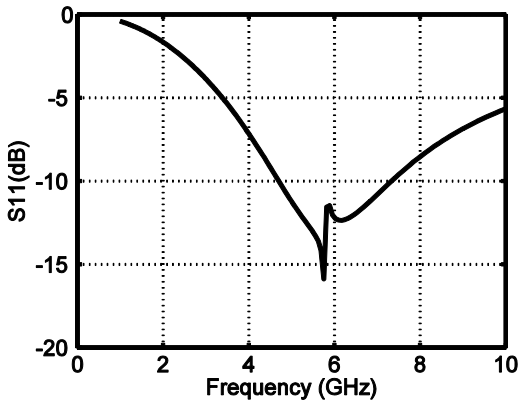


Figure 3.7: Simulated S11 vs input signal frequency

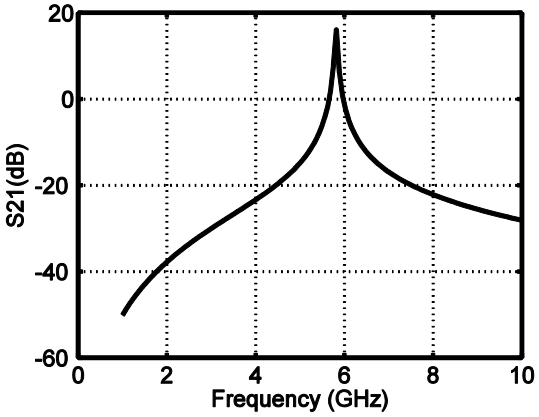


Figure 3.8: Simulated S21 vs input signal frequency

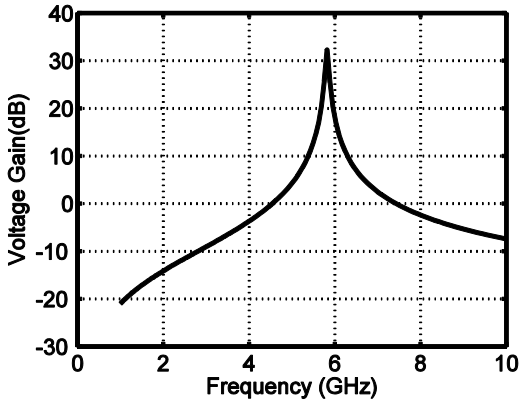


Figure 3.9: Simulated voltage gain vs input signal frequency

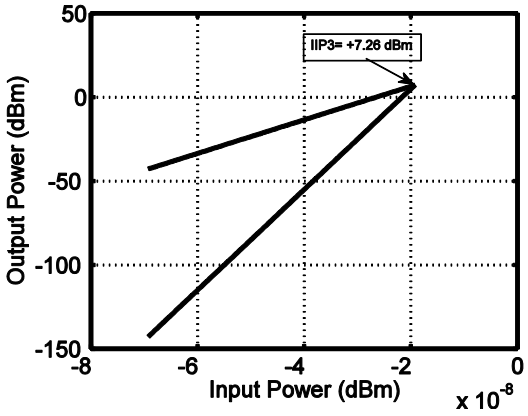


Figure 3.10: Simulated IIP3 for the proposed LNA

TABLE 3.1: PERFORMANCE SUMMARY OF DIFFERENT NARROWBAND LNA'S

References	Gain(or) S21 (dB)	Frequency (GHz)	NF (dB)	S11 (dB)	IIP3 (dBm)	Power (mW)	Supply (V)	CMOS Technology
(24)	12.2	900 M	3.0	NA	+6.7	20	2.7	0.5 µm
(23)	23	0.1-1.77	2.35	-35	-2.85	2.8	2	0.09 µm
(16)	12.7	5.8	2	< -10	-4	16.2	1.8	0.18 µm
(17)	7.1	6	3.0	-11	+11.4	6.48	1.8	0.18 µm
(25)	10.9	5.2	3.7	-11	-5	5.7	1.8	0.18 µm
(26)	9.4	5.8	2.5	-13.5	+7.6	3.42	1.8	0.18 µm
(27)	17	5	3.5	-14	-14.5	10	2.5	0.25 µm
(2)	48	5.8	5	-14	-28	NA	1.2	0.13 µm
This work	**16.03**	**5.8**	**2.4**	**-15.72**	**+7.26**	**0.58**	**0.55**	**0.18 µm**

A 5.8 GHz CG-LNA for the Chinese ETC standard is presented in this paper. Novel Capacitive Cross Coupled CG-LNA architecture is proposed in this paper. Proposed LNA has reduced power consumption of 0.58 mW and allowing a less noise figure among CG-LNA's which is 2.4 dB and also shows good performance in terms of power when compared with the existing works. Figure 3.12 shows the amplified output of the LNA.

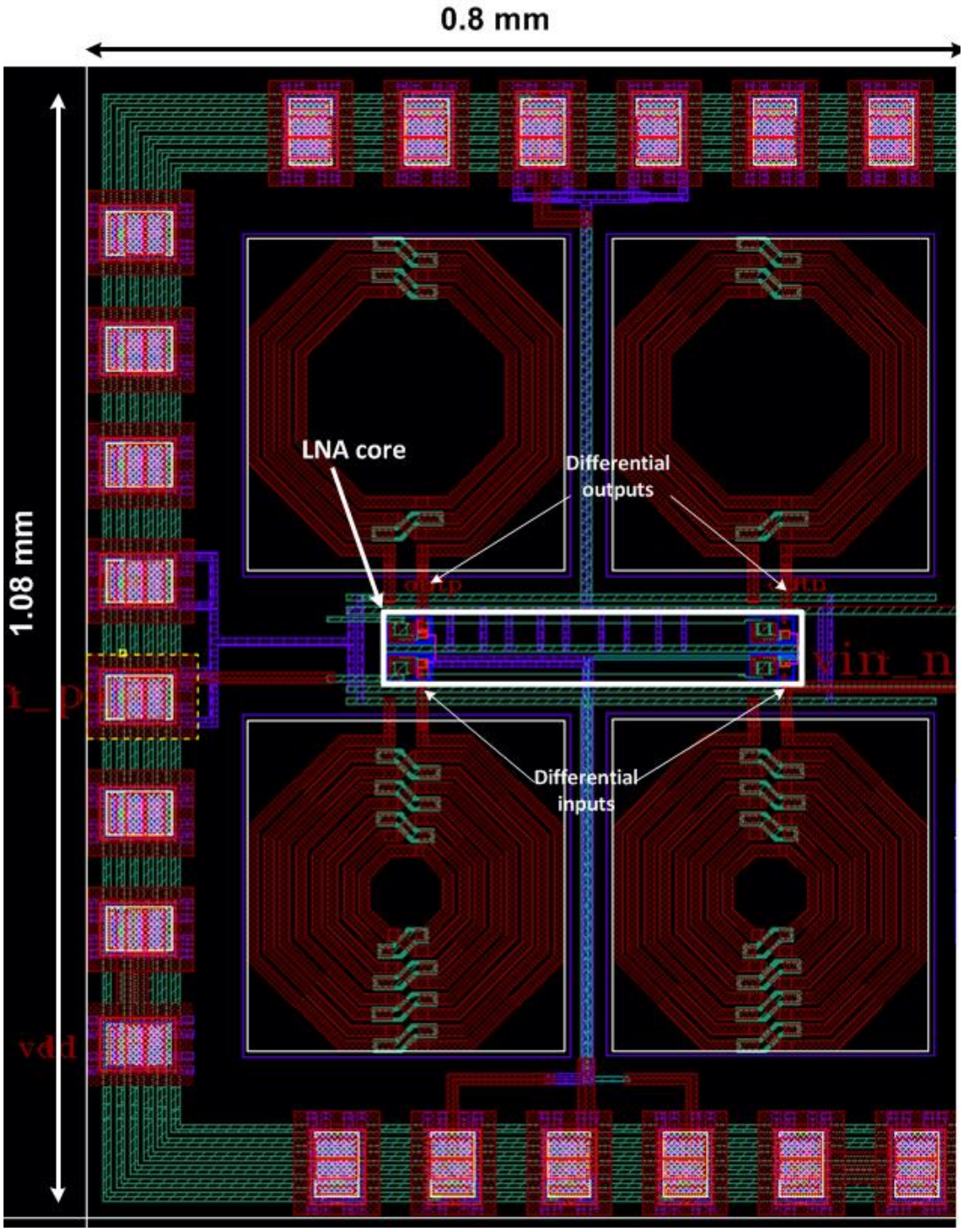


Figure 3.11: Layout of the Capacitive cross coupled CG-LNA

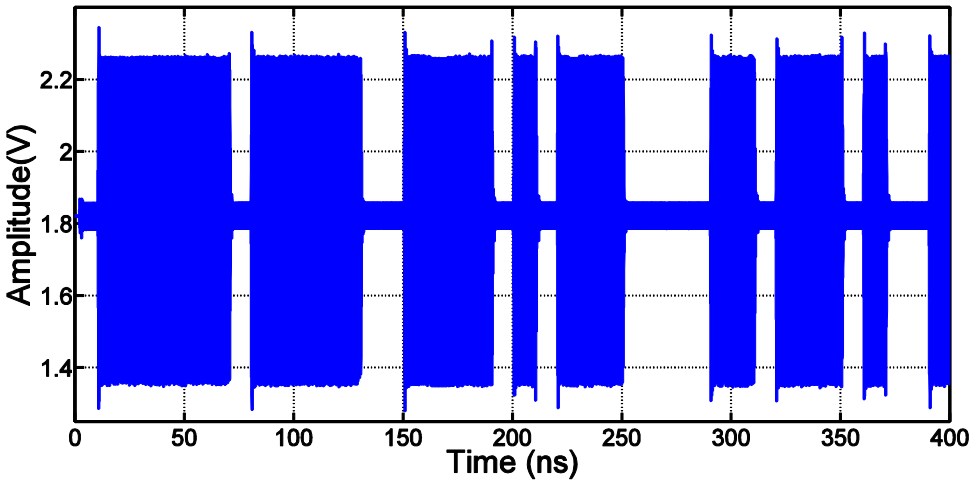


Figure 3.12: Amplified output of the LNA at 5.8 GHz frequency

3.2 MIXER

An ideal mixer is used for the translation of modulated signal around one carrier frequency to another carrier frequency. Mixers can be either linear circuits or non-linear circuits. An ideal mixer may consist of three ports which are local oscillator (LO), radio frequency input (RFIN) and intermediate frequency output (IFOUT) ports. Local oscillator signal is usually of fixed amplitude. Figure 3.13 shows the ideal mixer with three ports. The mixer produces sum and difference frequencies based on the RF input applied.

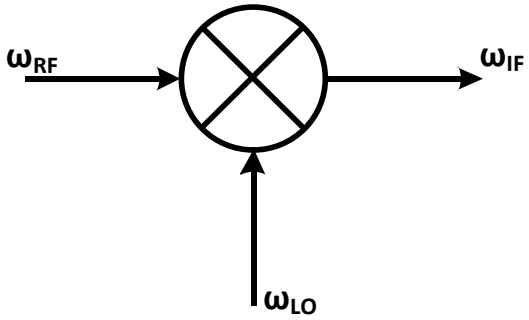


Figure 3.13: Ideal mixer

Mixer generally multiplies two input signals and then generates sum and difference of their frequency products. If A and B be two input signals then the output of the mixer can be given by:

$$A = Y_1 cos\omega_1 t \tag{3.7}$$

$$B = Y_2 cosw_2 t \tag{3.8}$$

After passing through the mixer, then it generates

$$A.B = (Y_1 cos\omega_1 t).(Y_2 cos\omega_2 t) \tag{3.9}$$

Solving the above equation we get

$$A.B = \frac{Y_1 Y_2}{2}\cos(\omega_1 - \omega_2)\, t + \frac{Y_1 Y_2}{2}\cos(\omega_1 + \omega_2)\, t \tag{3.10}$$

From the above equation, the sum frequency signal that is generated is usually removed by filtering and the difference frequency signal that is generated is the IF frequency signal. While designing any mixer, the primary design aspect to be considered is usually conversion gain which is the ratio between the IF signal which is the difference between the RF and the LO signal and the RF signal. Also noise consideration in the mixer design may be based upon either single sideband or double side band. In the single side band only the noise from frequency ω_1 is added to the front end of the mixer whereas in double side band mixer, both side bands are made available to the IF port of the mixer and thus its conversion loss is 3dB less when compared to the single side band signal.

Mixer can be designed in two types either active or passive. Passive mixers have good linearity when compared to the active mixers, but usually suffer from the high conversion losses and eventually they have higher noise figures when compared to the active mixers. On the other hand, although the design of double side band mixers is much complicated than the single side band mixers, their performance is much better when compared to the single side band mixers. For this reason, double side band type which is the active Gilbert mixer is chosen in this receiver design. This Gilbert mixer removes unwanted RF and LO signals by filtering techniques and by cancellation (28).

The Ideal Gilbert mixer is shown in the Figure 3.14. RF signal is applied to transistors M_1, M_2, M_3 and M_4 and the main function of those transistors is to provide voltage to current

conversion. Performance of the mixer can be improved by adding degeneration resistors at the drain terminals of transistors M_1 and M_2. Mixer design is based on the design of LNA and considering its gain and linearity. The previous block which is LNA has an input and output impedance value of 50 Ω and thus the input impedance value for the mixer is also 50 Ω.

The mixer implemented in this design has the basic approach of an active Gilbert mixer. In this design the local oscillator and the LNA both operate at the same carrier frequency of 5.8 GHz. The mixer is fed with the amplified output RF signal that is generated from the LNA and then it is down-converted and then given to the differential amplifier. The outputs of mixer consist of the sum and difference frequency signals. The output signals both are ASK modulated and the additive signal is passed on to the next set of differential amplifiers from which further filtering of the signals take place. The schematic and layout of the mixer circuit is shown in Figure 3.14 and Figure 3.15 respectively.

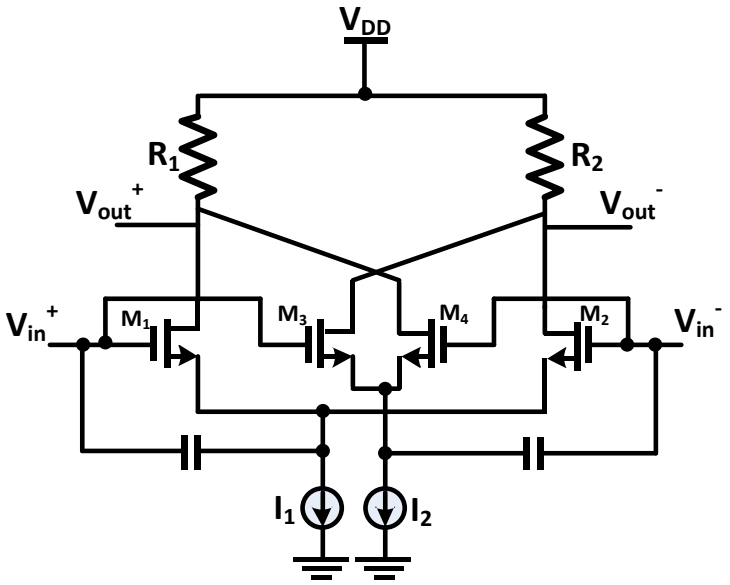


Figure 3.14: Schematic of mixer

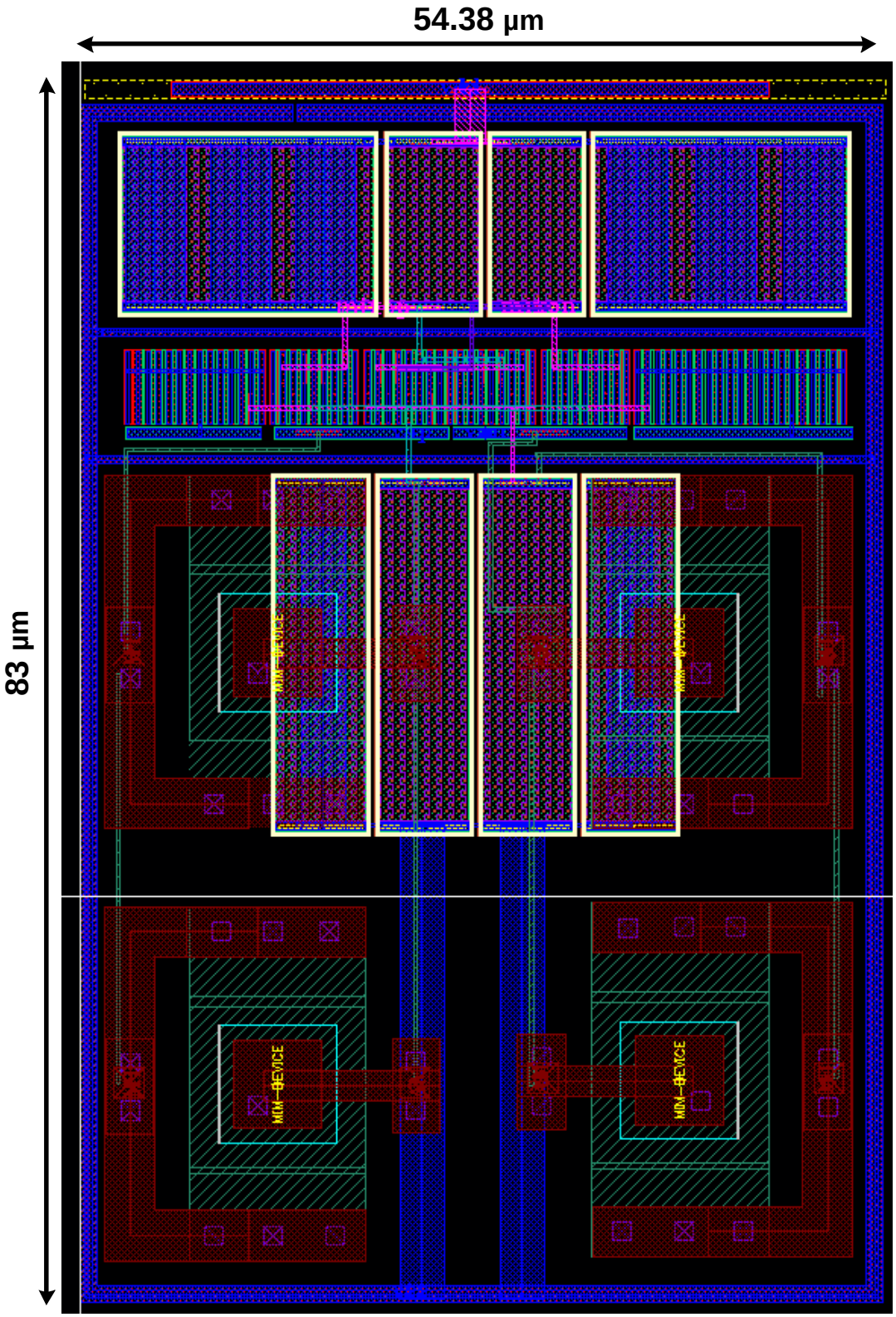


Figure 3.15: Layout of mixer

3.3 DIFFERENTIAL AMPLIFIER

A differential amplifier is the one which is used for the amplification of the difference of the two input signals applied to it. The common mode voltage applied to both the input voltages is cancelled. As in most of the cases the common mode voltages are cancelled out which eventually leads to cancellation of common mode noise in the circuits. The output of the differential amplifier is given by

$$V_{out} = (V_{in+} - V_{in-}) + A_c \frac{(V_{in+} - V_{in-})}{2} \tag{3.11}$$

Where V_{in+} and V_{in-} are the inputs applied, A_d and A_c are the differential and common mode voltages of the amplifier. Ideally the common mode voltage for the amplifier is zero i.e. A_c=0. For obtaining a good common mode gain, usually the common mode noise and the bias voltages of the amplifier are made as null.

Another important parameter in the design of the differential amplifier is the common mode rejection ratio (CMRR) which is defined as the ratio of differential mode gain to the common mode voltage gain. CMRR is mainly characterized by how efficiently it rejects the common mode voltages that are applied. CMRR is defined as follows:

$$CMRR = \frac{A_d}{A_c} \tag{3.12}$$

As already stated, for an ideal differential amplifier A_c is equal to zero and hence CMRR should be infinite (29). The main advantage of using a differential amplifier in any analog circuits is that it has high gain, high input impedance, low output impedance and also exhibits a very good noise cancellation effect. Gain of any differential amplifier is given by

$$A_v = -g_m R_D \tag{3.13}$$

Where A_v is the gain and g_m is the transconductance of the input differential amplifier.

Figure 3.17 shows the circuit schematic of the ideal differential amplifier that is used in the receiver circuit. Three differential amplifiers are used in the receiver block in order to amplify

the signal and at the same time with the change of the output differential signals that are generated. In order to generate a smoother differential signal, a set of 3 differential amplifiers are connected end to end such that the signal is amplified to a maximum extent and becomes smooth before going to the buffer converter. The final output of the differential amplifier is as shown in Figures 3.17 and layout is shown in the Figure 3.19.

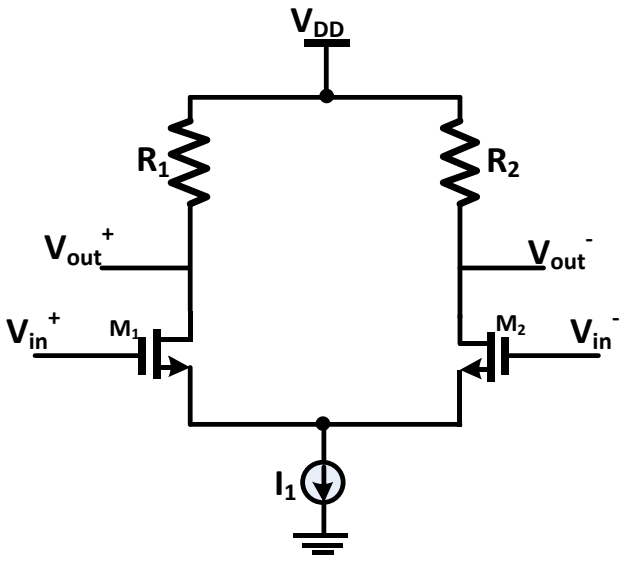


Figure 3.16: Schematic of the differential amplifier

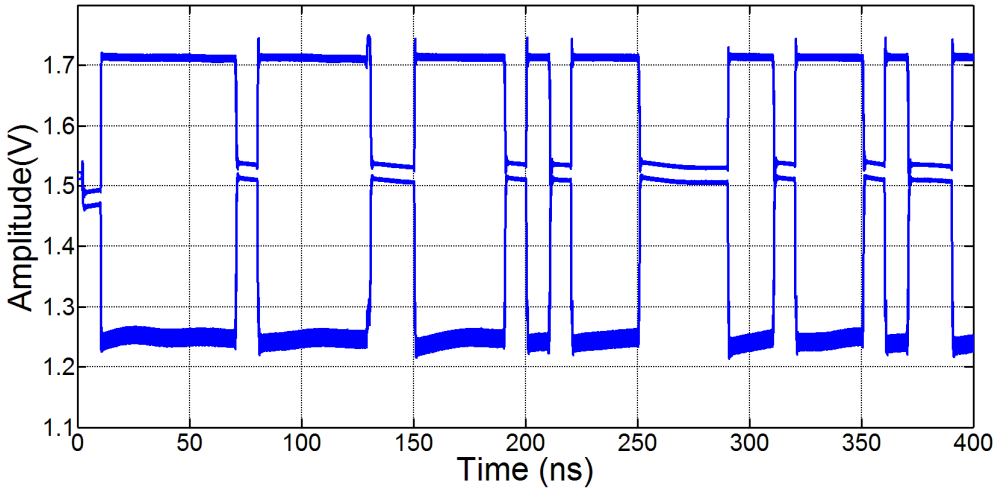


Figure 3.17: Output of the differential amplifier

3.4 OTHER KEY BLOCKS IN THE RECEIVER

The differential outputs generated from the differential amplifier are amplified but they don't have the same common mode voltage biasing. So, in order to have the same common mode operation buffer convertor is introduced after the differential amplifier circuit. The circuit controls the overall gain and at the same time settles the common-mode voltage of the circuit. The circuit (12) of the buffer convertor is shown in the Figure 3.22.

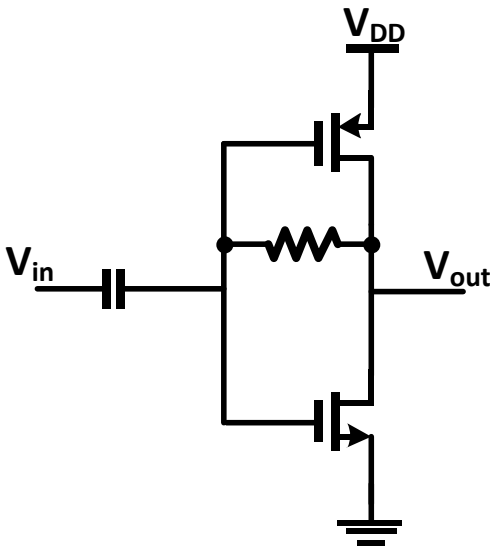


Figure 3.18: Schematic of buffer convertor

The output of the buffer convertor has the same common mode voltage, but in order to make the signal transmit from rail-to-rail, an inverter chain is placed after the buffer convertor block. Figure 3.23 and 3.24 shows the layout and output of the buffer convertor respectively. The signal after passing through the set of inverters, maintains its shape. Figure 3.25 shows the schematic of the inverter chain. Figure 3.26 and Figure 3.27 shows the layout and output of the inverter chain respectively.

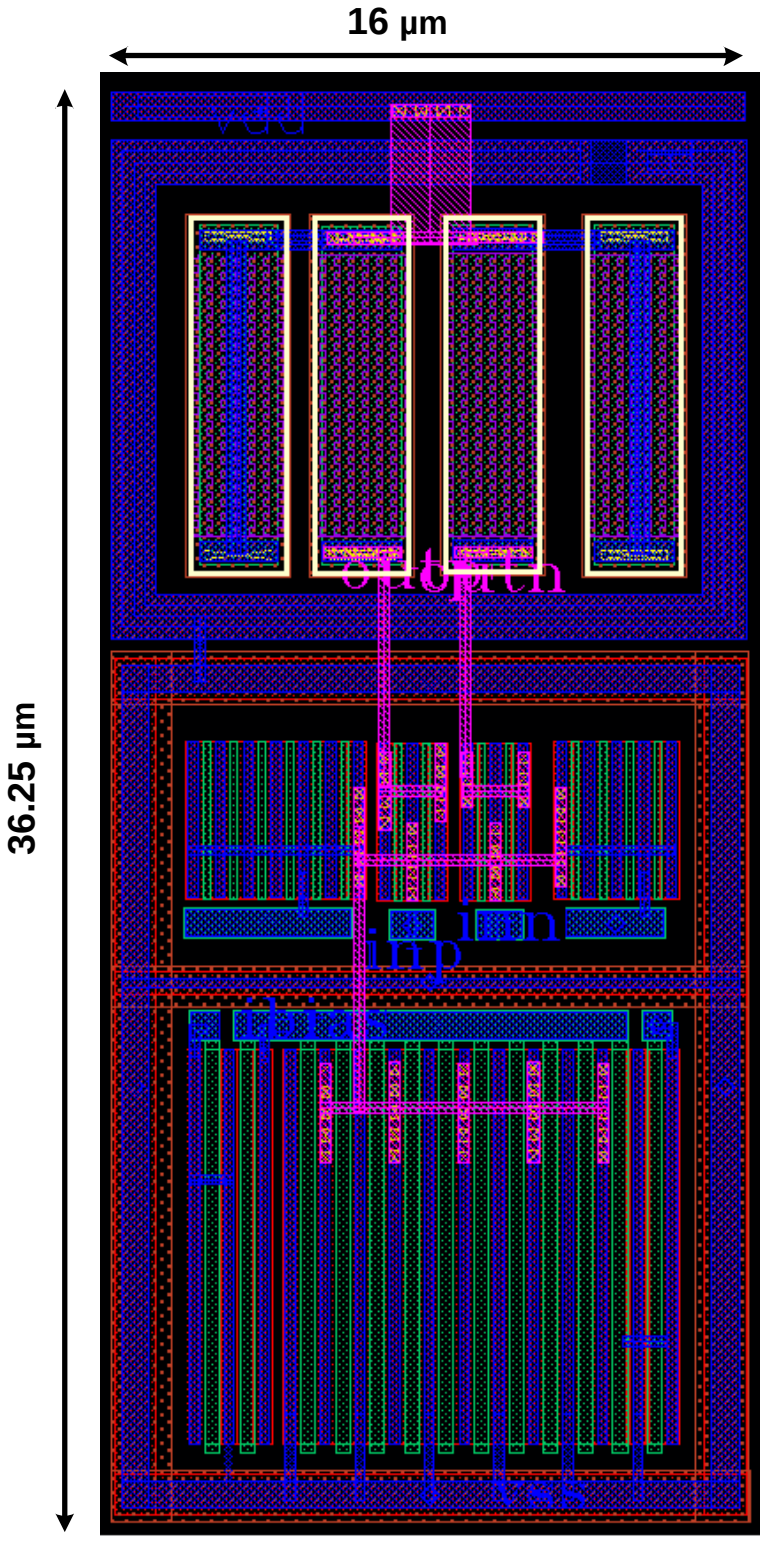


Figure 3.19: Layout of the differential amplifier

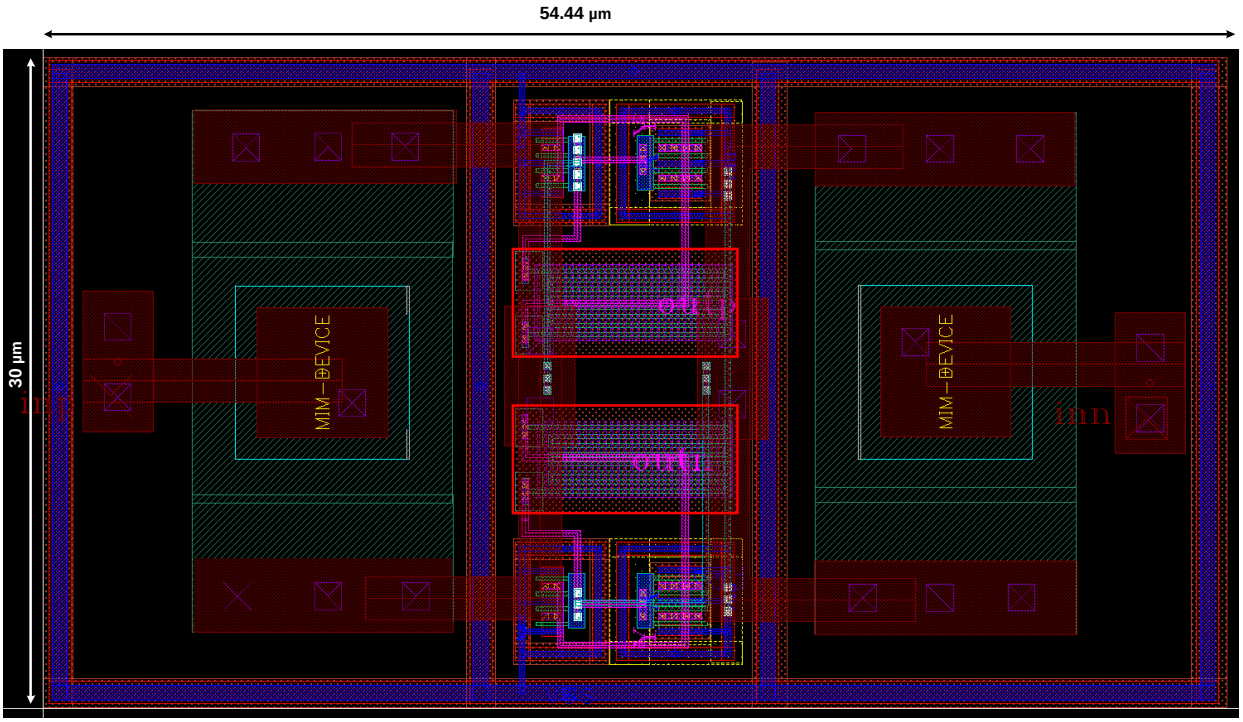


Figure 3.20: Layout of the buffer convertor

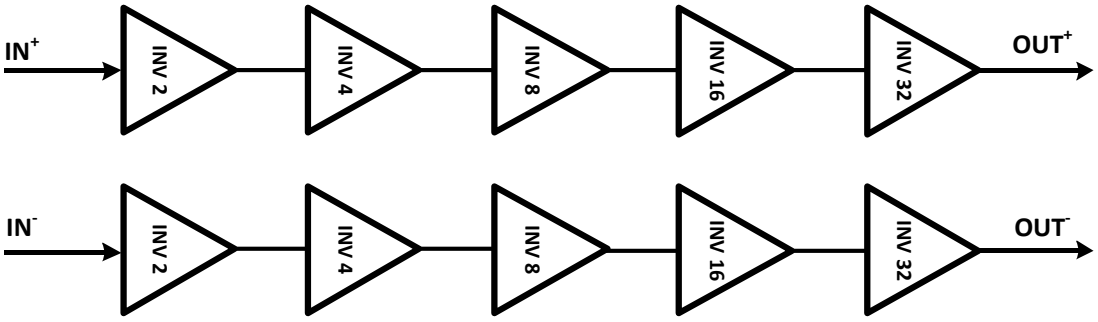


Figure 3.21: Schematic of the inverter chain

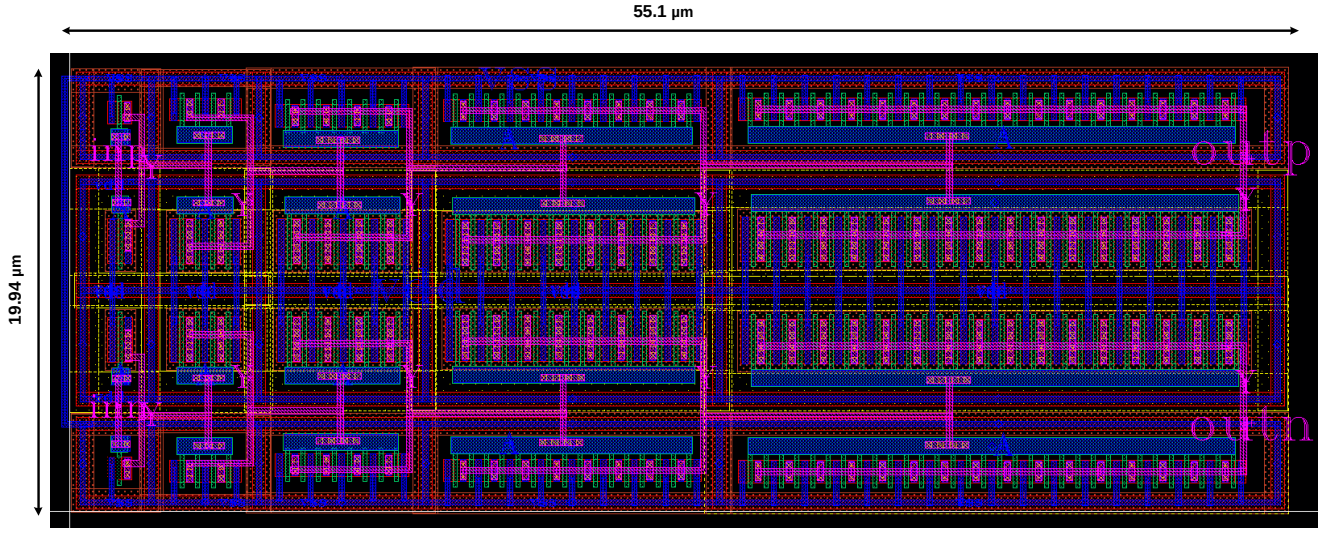


Figure 3.22: Layout of the inverter chain

After the inverter chain, a 50 ohm output driver is placed in order to drive the off chip components. Schematic and layout of the output driver is shown in the Figure 3.28 and Figure 3.29 respectively.

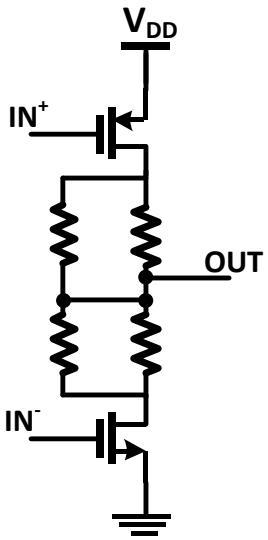


Figure 3.23: Schematic of the out driver

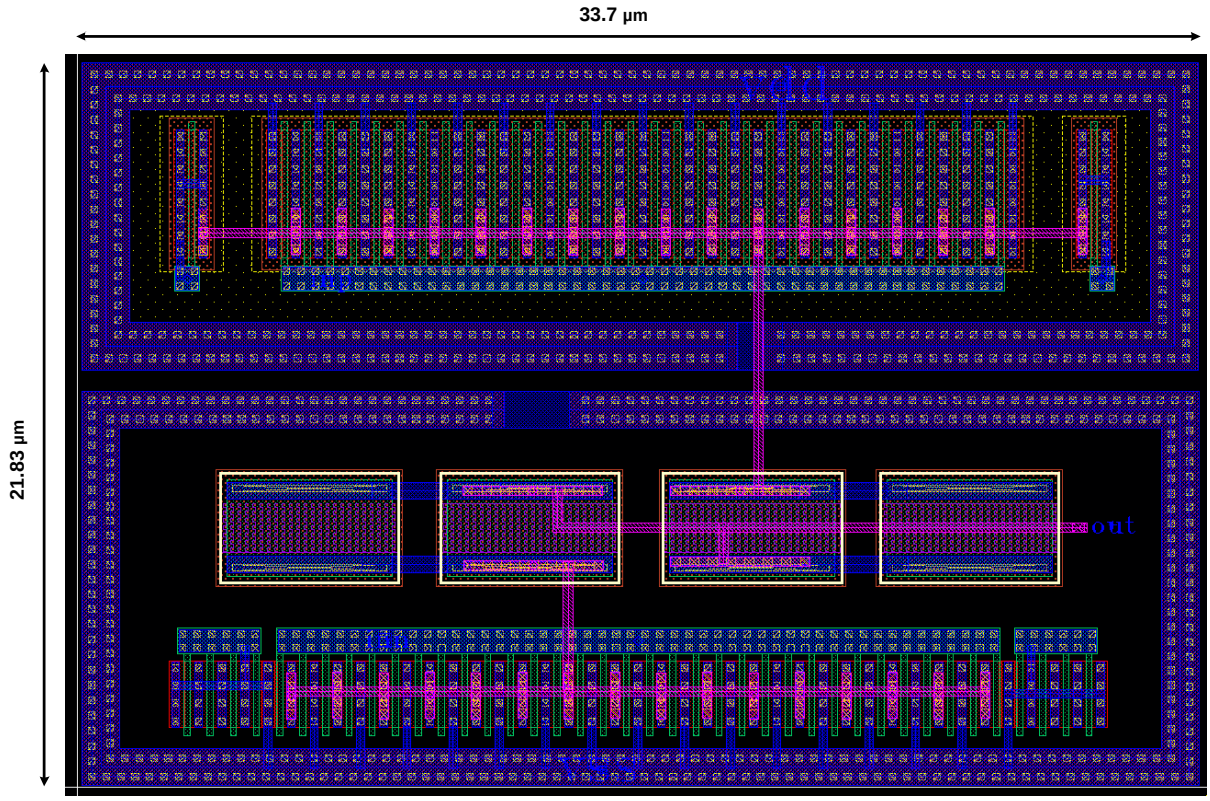


Figure 3.24: Layout of the out driver

Final layout of the receiver block is shown in the Figure 3.30 with all the receiver blocks such as LNA, Mixer, Differential amplifier, Buffer convertor, Inverter chain and the output driver.

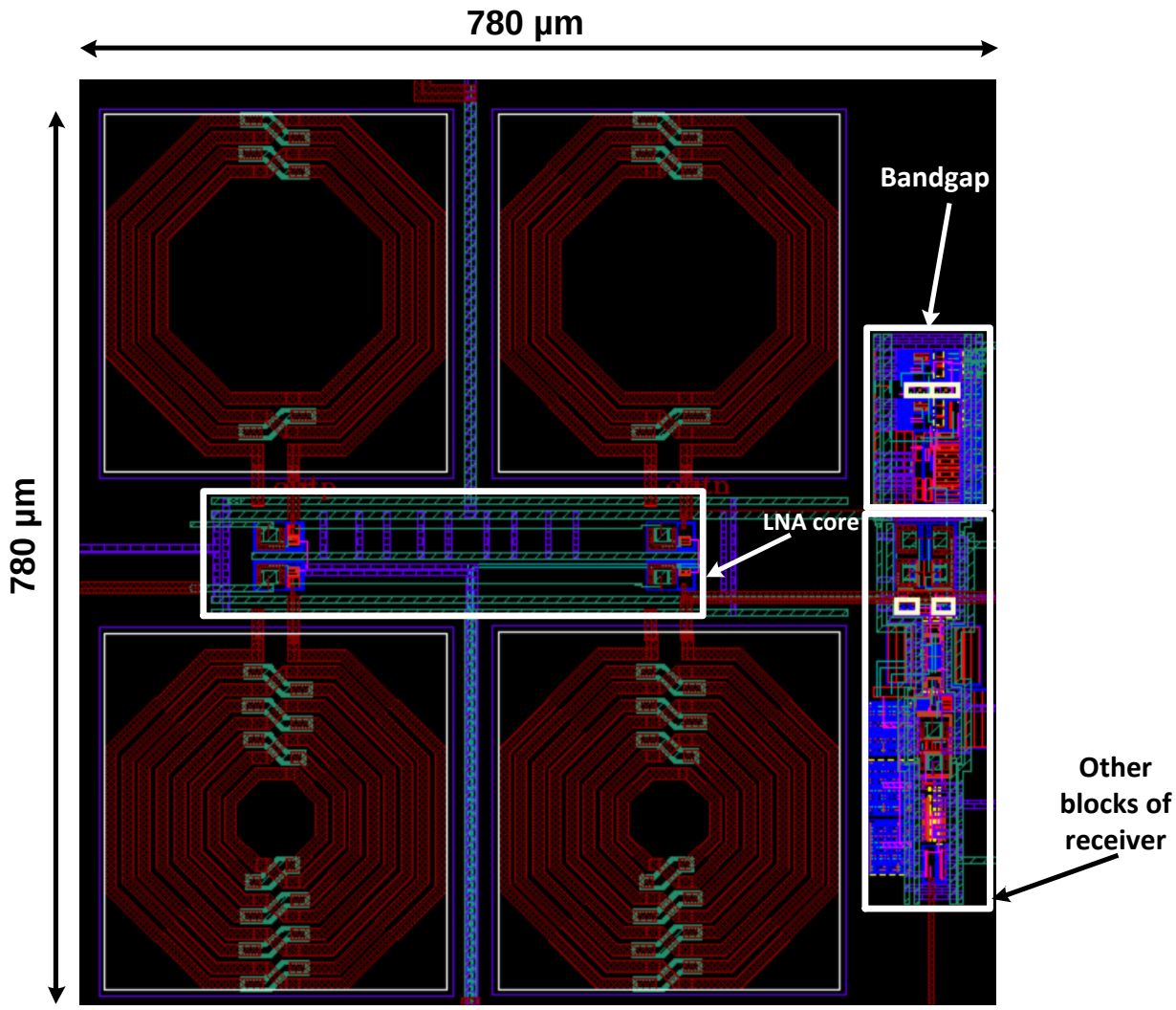


Figure 3.25: Final layout of the receiver

4 ANTENNA DESIGN

The basic function of an antenna is either for conversion of electric power into radio waves or radio waves to electric power. Antennas that are used at the transmitting end are termed as transmitting antennas and those used at the receiving end are termed as receiving antennas. The receiving antenna may produce a small amount of voltage that is used for the amplification of the receiver. The main application of antennas includes radio broadcasting, RADAR communication, satellite and mobile communications, wireless communications etc. Figure 4.1 shows the radiation pattern of transmitting and receiving antenna.

Classification of antennas is based on several factors as below (30):

- Frequency and size-Antennas used for HF are different from antennas used for VHF, which in turn are different from antennas for microwave. The wavelength is different at different frequencies, so the antennas must be different in size to radiate signals at the correct wavelength.
- Directivity-
    - Omnidirectional**:** Receive or radiate signal in all directions.
    - Semi directional**:** Provide specific, directed signal coverage over large areas.
    - Highly-directional: Used for point-point links.
- Physical construction: Antennas can be constructed in many different ways, ranging from simple wires, to parabolic dishes, to coffee cans.

Figure 4.1 shows the transmission pattern of transmitting antenna and the receiving antenna.

There are several factors that should be considered while designing any antenna and those factors are considered as antenna characteristics.

- **Radiation Pattern:** The antenna pattern is a graphical representation in three dimensions of the radiation of the antenna as a function of angular direction. Antenna radiation performance is usually measured and recorded in two orthogonal principal planes (E-Plane and H-plane or vertical and horizontal planes).

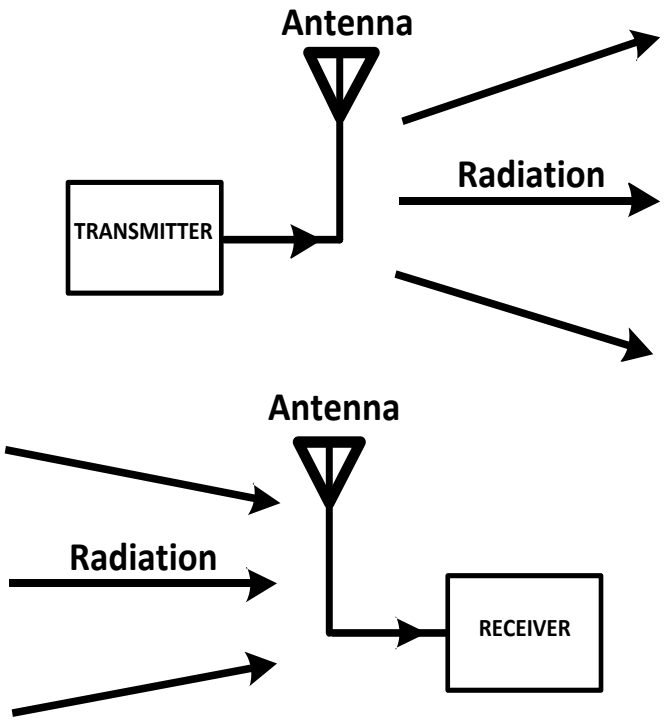


Figure 4.1: (a) Transmitting antenna (b) Receiving antenna

- **Antenna Gain:** Gain is the ratio of the maximum radiation in a given direction to that of a reference antenna for equal input power. Antenna gain depends on the mechanical size, the effective aperture area, the frequency band and the antenna configuration.

$$G = E_{antenna}.D$$

- **Front-to-back ratio:** It is the ratio of the maximum directivity of an antenna to its directivity in a specified rearward direction.
- **First Null Beam width:** The first null beam width (FNBW) is the angular span between the first pattern nulls adjacent to the main lobe.
- **Antenna Lobes:** Main lobe is the radiation lobe containing the direction of maximum radiation.

- **Half-power beam width:** The half power beam width (HPBW) is the angle between the points on the main lobe that are 3dB lower in gain compared to the maximum.
- **Polarization:** Polarization is the propagation of the electric field vector.
- **Frequency bandwidth:** It is the range of frequencies within which the performance of the antenna, with respect to some characteristics, conforms to a specified standard.
- **Antenna impedance**: Maximum power coupling into the antennas can be achieved when the antenna impedance matches the cable impedance.
- **Mechanical size**: Mechanical size relates to achievable antenna gain.

Antennas may be classified into several categories based on their shapes like wire antennas, micro strip antennas, travelling wave antennas, log-periodic antennas, reflector antennas, aperture antennas, etc.

Dipole antennas come under the category of wire antennas. Wire antennas may be of different types like short dipole, dipole, half-wave dipole, monopole, folded dipole etc. Dipole antenna is one of the simplest and most widely used antennas. It consists of two identical conductive elements such as metal wires or rods, which are usually bilaterally symmetrical. The antenna that is employed in this design is the folded dipole antenna which is a half-wave dipole with two additional wires connecting at both of its ends. Main use of using this antenna is that it gives high input impedance when compared to other dipole antennas.

When the antenna radiate, the electromagnetic field structure changes as there is change in the radiation with the distance from the antenna. These radiation regions are divided into three categories, namely reactive near-field region, radiating near-field region and far-field region.

Reactive near-field region is the one in which maximum antenna radiation pattern of the antenna is absorbed. In most of the cases, the maximum radiation occurs at a distance of $R < 0.62\sqrt{D^3/\lambda}$ from the antenna where R is the radius, D is the maximum length of the antenna from the figure and λ is the wavelength. Usually high amount of reactive power is confined within this region. The region after this reactive near-field region is the radiating near-field or Fresnel region. This region usually has boundaries in the range of $R \geq 0.62\sqrt{D^3/\lambda}$ and

$R < 2D^2/\lambda$ where D is again the largest dimension of the antenna and λ is the wavelength. This region usually doesn't exist when the size of the antenna is small when compared to the operating wavelength. The third region is the radiating far-field or Fraunhofer region where all the power is directed radially outwards. Field pattern doesn't depend on the distance R of the antenna (31).

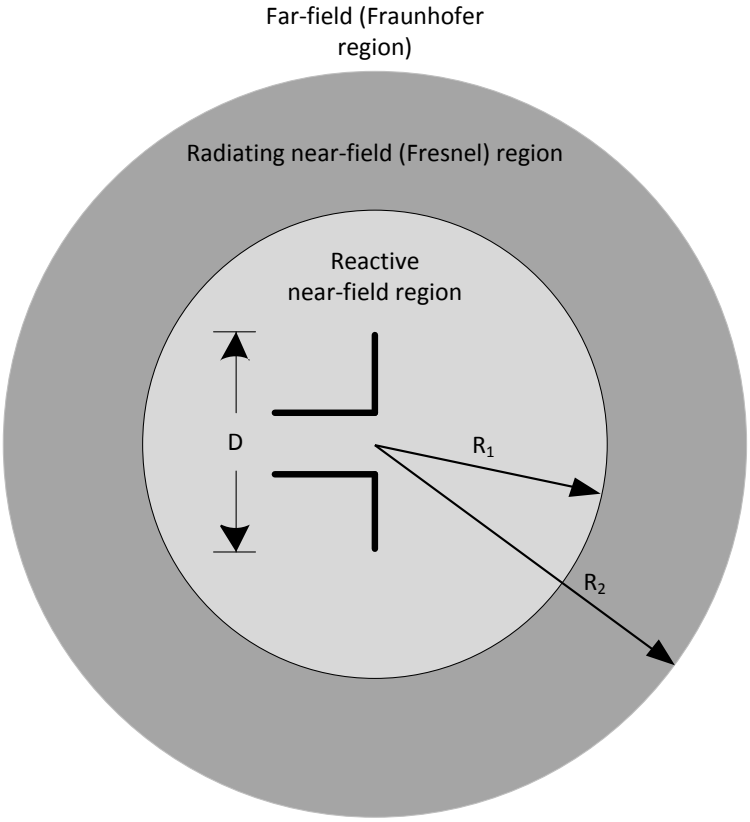


Figure 4.2: Field regions of an antenna

In the analysis of the antenna, the fundamental antenna parameters that need to be considered are S-parameters. The performance of the antenna is based on the antenna design during which S-parameters play a crucial role. By these S-parameters, broadband characterization is possible. Usually the S-parameters are defined by measuring the voltage travelling waves between the N-ports of an N-port network as shown in the Figure 4.3 (31).

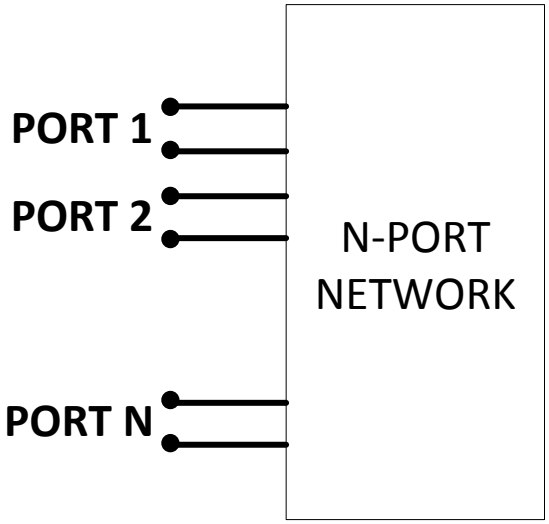


Figure 4.3: An N-port network

The S-parameters are usually defined from the two-port network as shown in the fig []

Input reflection coefficient, when port 2 is matched, $S_{11} = \frac{b_1}{a_1} \Big| a_2 = 0$

Reverse transmission gain, when port 1 is matched, $S_{12} = \frac{b_1}{a_2} \Big| a_1 = 0$

Output reflection coefficient, when port 1 is matched, $S_{22} = \frac{b_2}{a_2} \Big| a_1 = 0$

Forward transmission gain, when port 2 is matched, $S_{21} = \frac{b_2}{a_1} \Big| a_2 = 0$

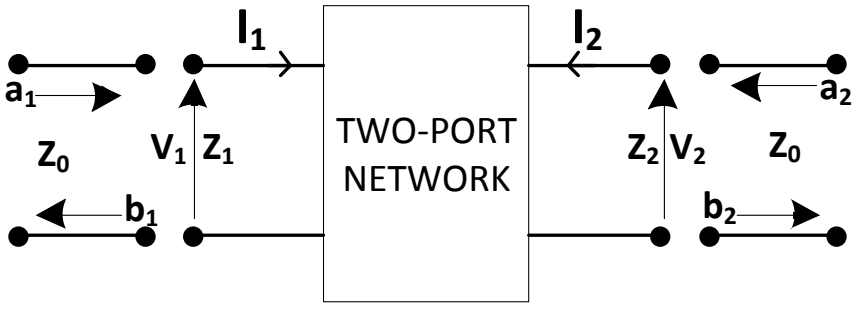


Figure 4.4: Two port network definition

V_1= Voltage at port 1 and a_1= signal incident at port 1

V_2= Voltage at port 2 and b_1= signal reflected at port 1

I_1= Voltage at port 1 and a_2= signal incident at port 2

I_2= Voltage at port 2 and b_2= signal reflected at port 1

Z_0=Characteristic impedance, Z_1=port 1 impedance and Z_2=port 2 impedance

The dipole antenna designed for this ETC system should transmit signals only at a frequency of 5.8 GHz and should reject all other unwanted frequencies. The reflection loss should be high such that signal is allowed to pass completely to the receiver block. In the Figure 4.5 dipole antenna of 60.25*19 mm^2 is shown with a reflection loss of -18.7 dB. After designing many versions to make it compact and to get a good reflection coefficient at ETC frequency of 5.8 GHz, an antenna with dimensions of 47*8 mm^2 as shown in the Figure 4.6 is designed and has a reflection coefficient of S_{11} equal to -35dB at 5.8 GHz which means that signal is reflected perfectly at the desired frequency. The thickness of the dielectric chosen for the substrate design in the simulation of the dipole antenna is 40 mils and the dielectric constant is set as 4.4. Figure 4.7 shows the substrate design for this simulation.

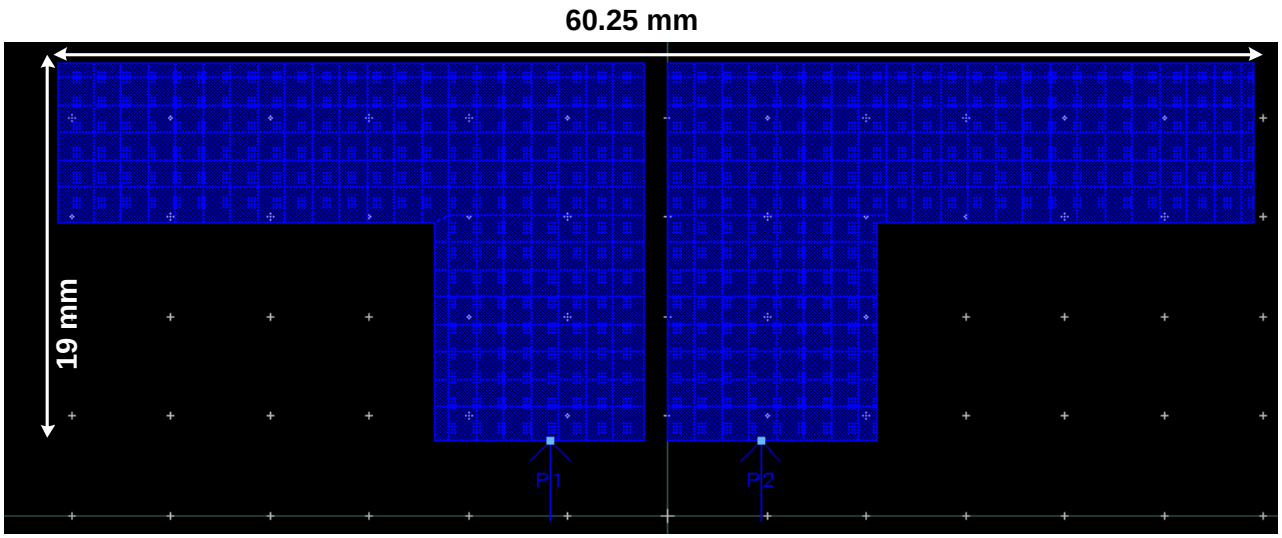


Figure 4.5: Simulated Dipole antenna in ADS with large size

Figure 4.6 shows the plot for the reflection coefficient at 5.8 GHz frequency which has a value of -18.7 dB and Figure 4.9 and Figure 4.10 gives the S11 and S21 plot of compact antenna respectively.

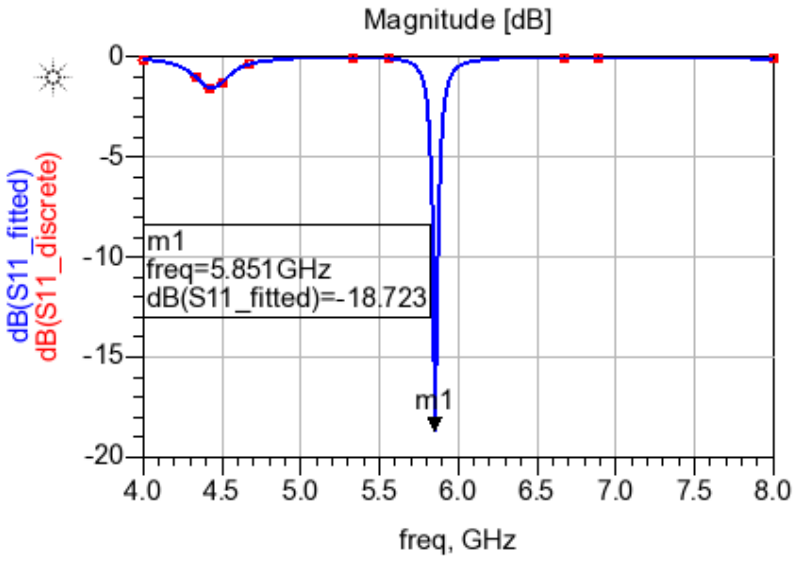


Figure 4.6: Simulated S11 plot

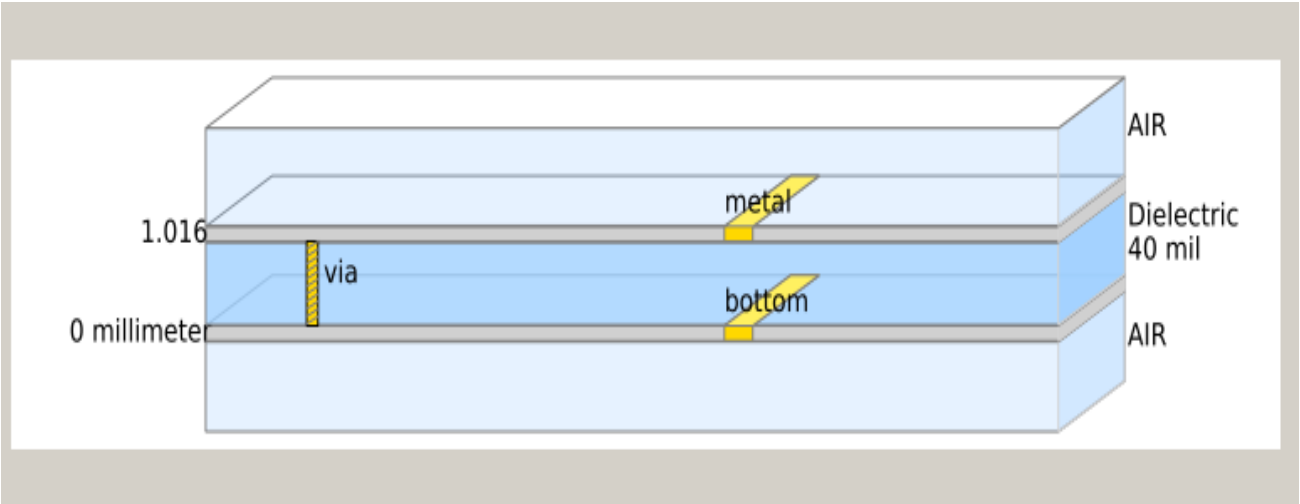


Figure 4.7: Substrate design of simulated compact Dipole antenna in ADS

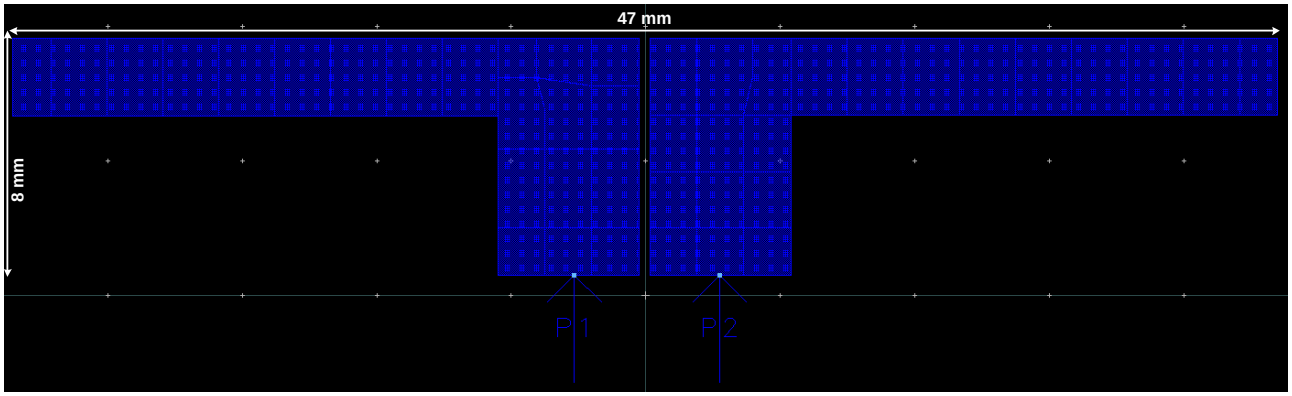


Figure 4.8: Simulated compact Dipole antenna in ADS

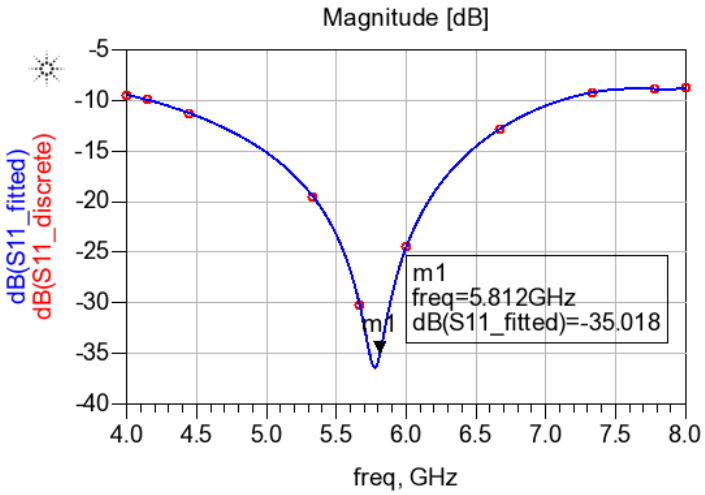


Figure 4.9: Simulated S11 plot

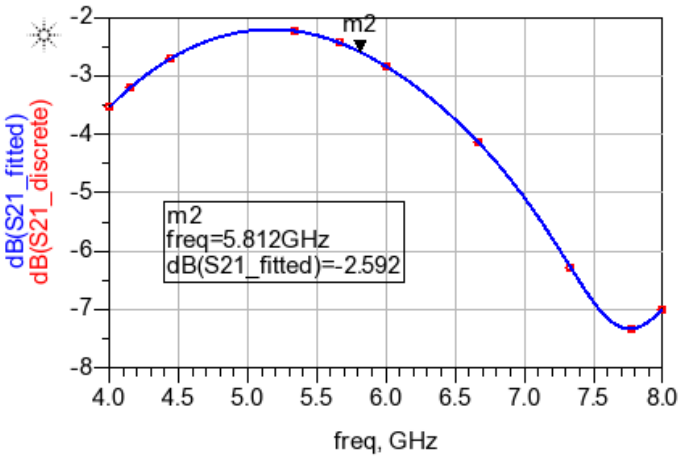


Figure 4.10: Simulated S21 plot

5 FINAL RESULTS

In the previous chapters all the individual components of the transmitter and the receiver are discussed in detail. In this chapter the whole circuit i.e. both the transmitter and the receiver blocks are connected to the pad frame and the final layouts are shown. Post extracted simulation results of the whole system are shown. Usually for any design in CMOS technology, during schematic based simulation, parasitic elements effect is not considered. However, after the actual chip test, final results may differ from the simulation results as parasitic effects are added and thus the results are not as expected. So in order to get final chip test results closer to the simulation results, best thing is to add a small capacitance at every output node which so that results are closer to the final anticipated results. Another thing is simulating the entire circuit after RC-extraction so that both R and C parasitic effects are added and thus working of the circuit is predictable. Without considering these effects expecting final results to be closer to the simulation results is not suggestible. So for this reason QRC extraction should be done for the layout after DRC and LVS checks are performed.

Figure 5.1 and Figure 5.2 and Figure 5.3 shows the final schematic, layout of the transmitter and receiver separately. In most of the prior works (32), (33), (2), (34), (35) maximum data rates achieved using ASK modulation technique are 1.024 Mbps and 4.096 Mbps. Figure 5.4, Figure 5.5 and Figure 5.6 shows the input data, output data and the final recovered data at 100 Mbps of the ETC system respectively. The system is working up to the data rate of 400 Mb/s. The signal is exactly recovered at the output. Although the parasitic losses are taken into consideration the signal swing at the output is good which means that the effect of these parasitic capacitances is less and the signal is recovered properly.

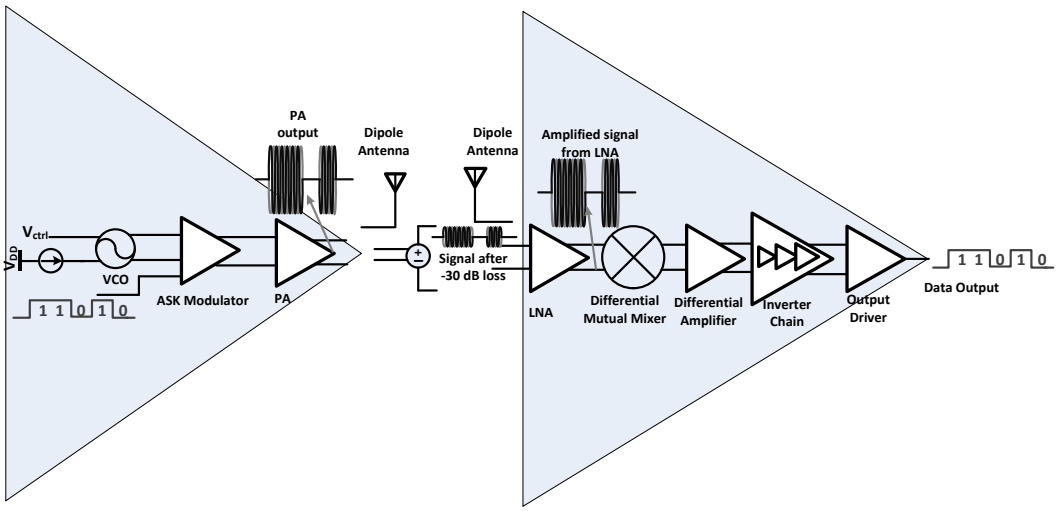


Figure 5.1: Schematic of the ETC transceiver

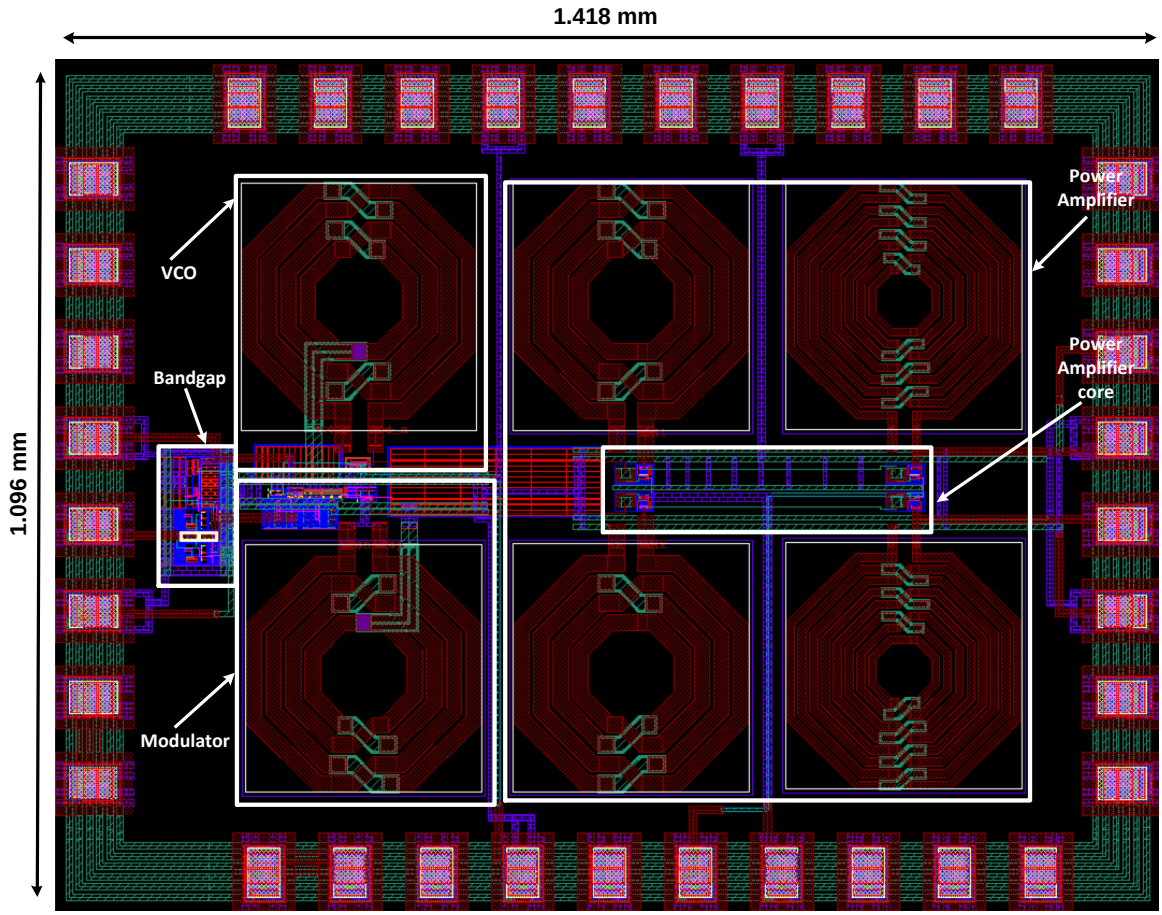


Figure 5.2: Final layout of the ETC transmitter connected to the pad frame

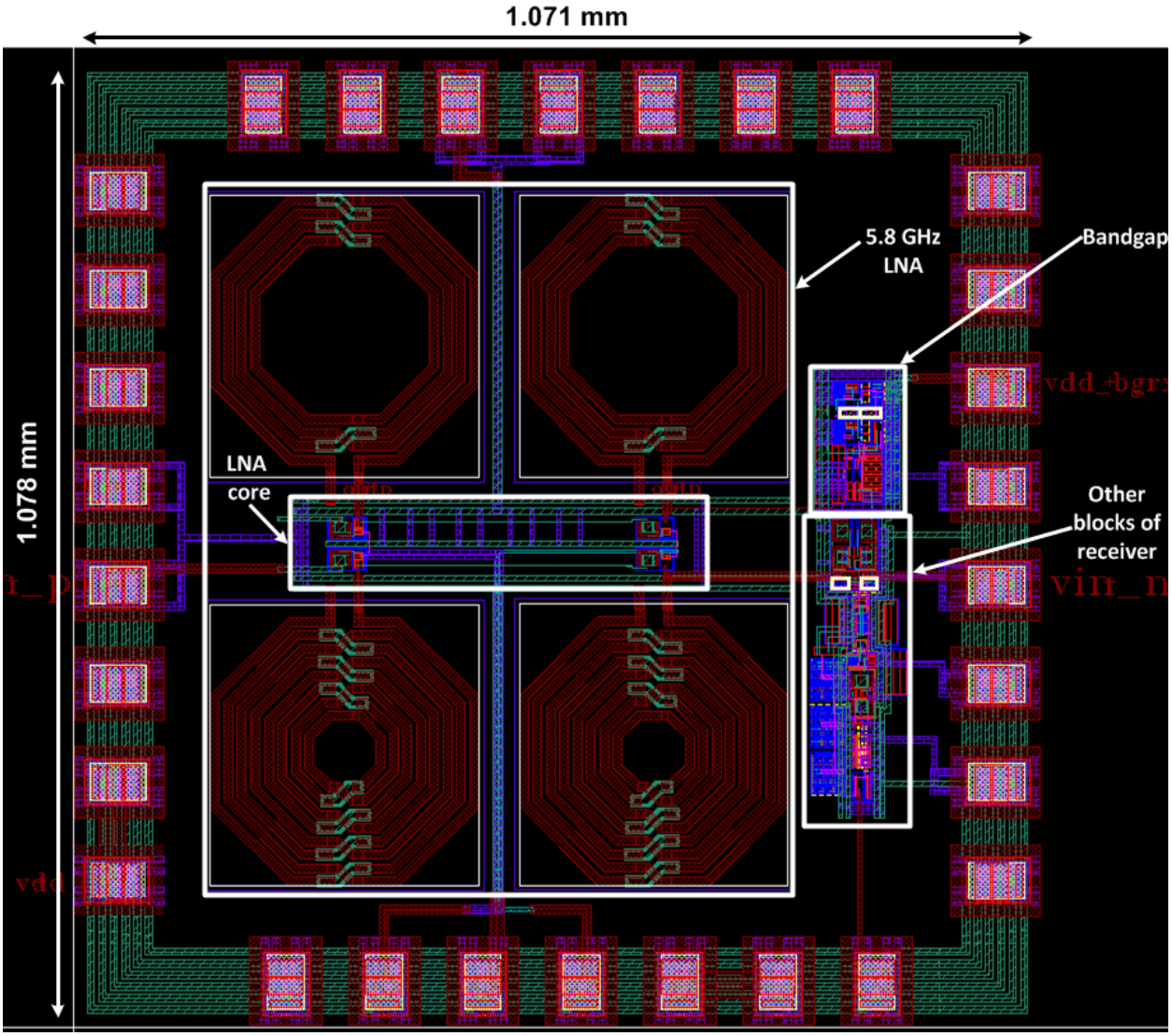


Figure 5.3: Final layout of the ETC receiver connected to the pad frame

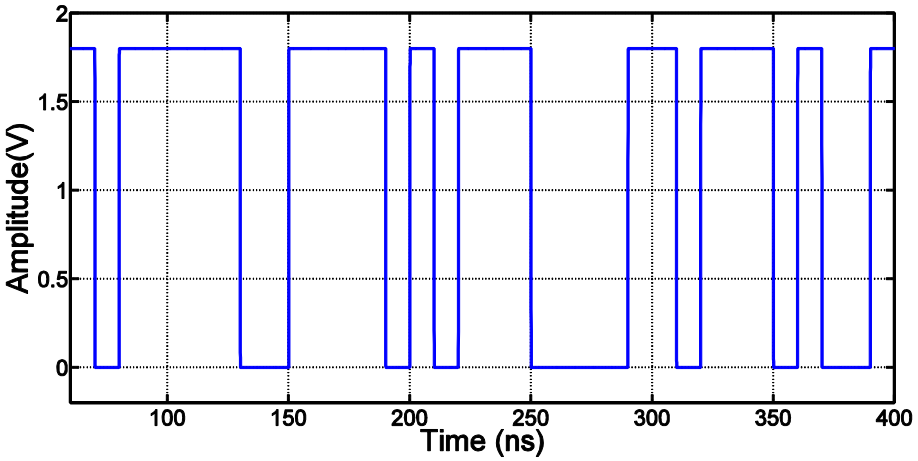


Figure 5.4: Input data at 100 Mbps

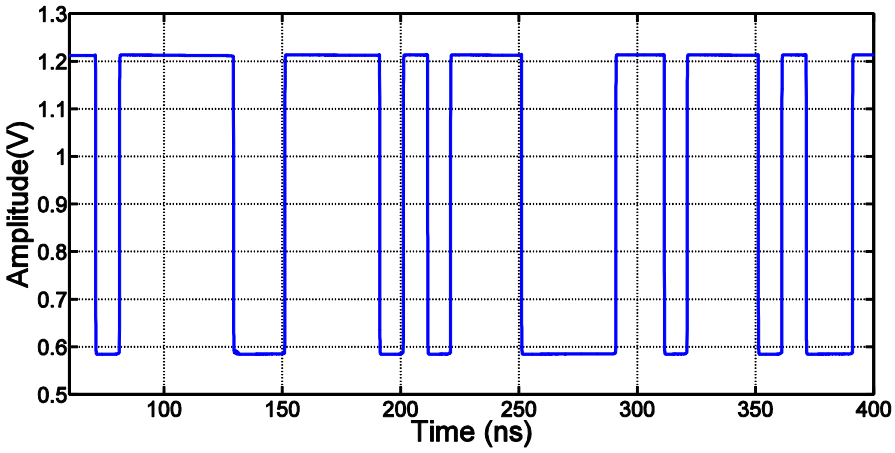


Figure 5.5: Output for input data of 100 Mbps

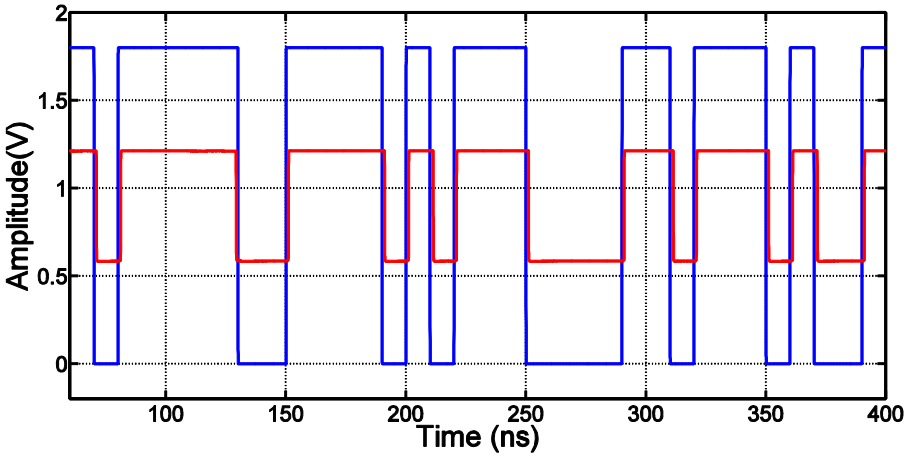


Figure 5.6: Output data (red color) traced the path of input data (blue color)

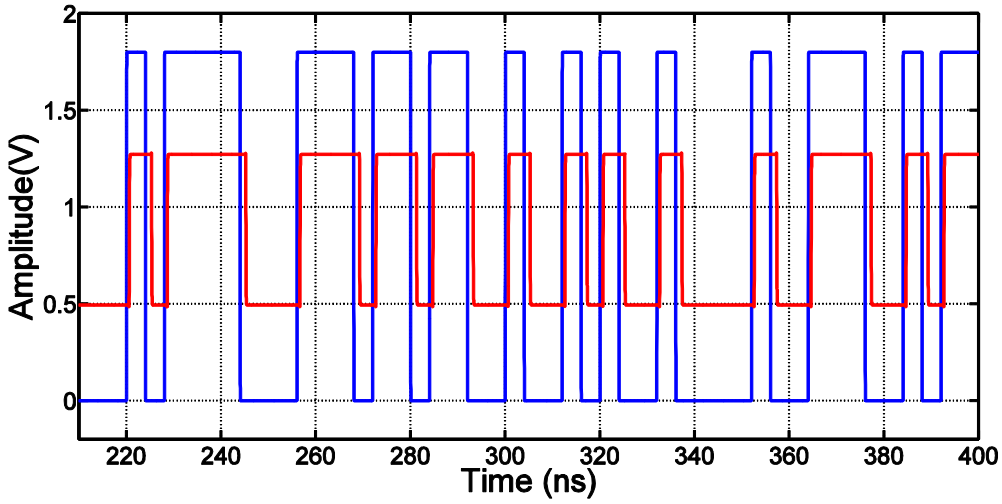


Figure 5.7: Output data (red color) traced the path of input data (blue color) at 250 Mbps

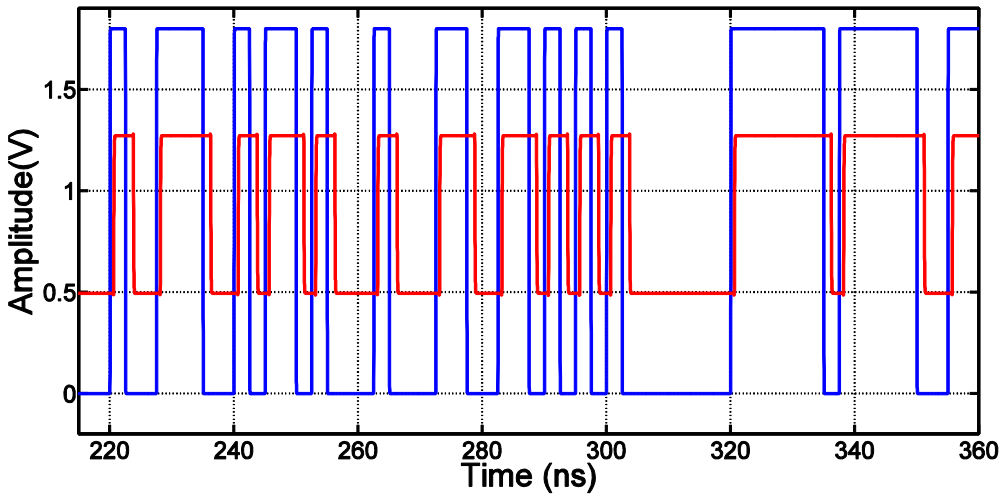


Figure 5.8: Output data (red color) traced the path of input data (blue color) at 400 Mbps

5.1 CONCLUSION

A compact dipole antenna based RF Transceiver for Electronic Toll Collection (ETC) System has been implemented in this work. A capacitor cross-coupled CG-LNA has been implemented in this design which is the major contribution for the receiver block with a tremendous low power at an aggressively scaled supply voltage. All the post extracted results are discussed which are almost accurate and the working of the chip can be predicted based on the post extraction results which include all the effects produced due to parasitic resistances and capacitances.

5.2 FUTURE SCOPE

Future implementation of this project includes the design of much compact off chip Antenna with matching network such that the signal is transmitted properly by the transmitting antenna and can be received by the receiving antenna without much loss. Using class- E power amplifier for high efficiency in turn increased the transmitter system power which is a limitation that needs to be overcome in future. Also, this system can be implemented for higher input data rates so the overall efficiency of the system increases and much faster transmission takes place at the ETC system frequency and the system can be made useful for real time application by providing much lesser delay time when compared to the already existing works.

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