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Mixed Signal Integrated Circuit Design for Custom Sensor Interfacing

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Abstract

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Low-power analog integrated circuits (ICs) can be utilized at the interface between an analog sensor and a digital system's input to decrease power consumption, increase system accuracy, perform signal processing, and make the necessary adjustments for compatibility between the two devices. This interfacing has typically been done with custom integrated solutions, but advancements in floating-gate technologies have made reconfigurable analog ICs a competitive option. Whether the solution is a custom design or built from a reconfigurable system, digital peripheral circuits are needed to configure their operation for these analog circuits to work with the best accuracy.

Using an analog IC as a front end signal processor between an analog sensor and wireless sensor mote can greatly decrease battery consumption. Processing in the digital domain requires more power than when done on an analog system. An Analog Signal Processor (ASP) can allow the digital wireless mote to remain in sleep mode while the ASP is always listening for an important event. Once this event occurs, the ASP will wake the wireless mote, allowing it to record the event and send radio transmissions if necessary. As most wireless sensor networks employ the use of batteries as a power source, an energy harvesting system in addition to an ASP can be used to further supplement this battery consumption.

This thesis documents the development of mixed-signal integrated circuits for use as interfaces between analog sensors and digital Wireless Sensor Networks (WSNs). The following work outlines, as well as shows the results, of development for sensor interfacing utilizing both custom mixed signal integrated circuits as well as a Field Programmable Analog Array (FPAA) for post fabrication customization. An Analog Signal Processor (ASP) has been used in an Acoustic Vehicle Classification system. To keep these interfacing methods low power, a prototype energy harvesting system using commercial-off-the-shelf (COTS) devices is detailed which has led to the design of a fully integrated solution.

Acknowledgments

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Chapter 1

Introduction

Compact, low-power, electronics are paving the way for the future of mankind. Advancements in micro-electronics have led to a small, contained package known as a wireless mote. The wireless mote works as a part of a larger whole, communicating with other motes of its kind to form a Wireless Sensor Network (WSN). These WSNs are able to monitor and report large amounts of data, ranging from temperatures and sounds to seismic activity. The one drawback of the WSN is that it employs digital motes.

These digital motes usually have a data converter (Analog-to-Digital) built in to their input. This allows the mote to read from an analog sensor, and convert the data into the digital domain for processing. A drawback for this design is that the analog sensor must output data that meets the dynamic range of the built-in data converter. To bridge this gap, an analog circuit can be used to interface between the sensor and the wireless mote. This interface can act as an amplifier, add temperature compensation, or act as a converter (not necessarily converting from analog-to-digital, but converting currents to voltages, resistances to voltages, or capacitances to voltages).

Electronics that operate in the digital domain draw large amounts of power due to the use of a data converter for conversion from the analog domain. A front-end Analog Signal Processor (ASP) can be used to decrease power consumption without hampering the operation of the WSN. An ASP allows the more power-consuming digital mote to stay in a low-power sleep state, while the ASP monitors data coming in from the analog sensor. When the ASP detects an event, it sends a wake-up to the digital mote to start recording

the desired event. Once the event is over, the digital mote can return to its low-power state while the ASP continues to monitor input from the analog sensor.

An ASP can make large improvements to a wireless mote's power consumption, but another technique can be utilized to increase battery life even further. Energy harvesting refers to a system that scavenges excess energy from the environment and converts it to electric power, usable by the wireless mote. This excess energy can be in the form of heat, sunlight, vibrations, radio waves, or even pH levels in a body of water. An energy transducer is used to convert these different forms of energy into something usable by the mote. For the mote to make use of this extra power, an energy harvesting system is used to control the input from the transducer, store the energy, and apply it to the mote when needed.

Combining the aspects of sensor interfacing, analog-signal processing, and energy harvesting to a WSN can greatly improve upon its operation capacity. Analog integrated circuits (IC) are the most reasonable way of accomplishing this feat, allowing for low-power operation, finely tuned control schemes, and the ability to produce an output suited to a specific wireless mote. A custom mixed-signal integrated circuit can be designed to meet all of an application's needs, but requires a long design cycle as well as an expensive fabrication process. This becomes a problem when changes in the environment or application require a different operation from the integrated circuit.

A reconfigurable integrated circuit allows for changes in performance or optimization to be handled post-fabrication. Devices such as the Field Programmable Analog Array (FPAA) are perfectly suited to changing design constraints. A well-designed FPAA can be used to handle all of the needs set forth by a WSN, while leaving the door open to changing design constraints that may arise in the future.

1.1 Outline

Chapter 2 will provide an overview on all of the necessary components needed for sensor interfacing, including custom ICs, reconfigurable ICs, Energy Harvesting, and all of the peripherals needed to operate these systems. Chapter 3 will cover using a Custom IC as an interface between a WSN and a custom analog sensor. Chapter 4 will cover utilizing a

reconfigurable IC as a front-end ASP between an analog sensor and a WSN for an Acoustic Vehicle Classification project. Chapter 4 will also detail improvements made to the reconfigurable IC for future interfacing applications. Chapter 5 will cover a prototype design of an Energy Harvester, used for supplementing battery consumption of a wireless sensor mote as well as designs for an integrated, custom energy harvesting system. Finally, Chapter 6 will provide a summary and conclusion from this work, as well as discuss the future for this research.

Chapter 2

Background

Analog integrated circuits are still one of the most important aspects of modern electronics. Living in an analog world, any time a digital computer needs to interface with the environment, data converters must be used to cross the threshold between binary and analog. However, data converters are not the only aspect of interfacing between these two domains. Data converters require their input to be received with a certain amplitude, frequency, and must be in the form of a voltage. This requires a specific output from an analog sensor. If a specific sensor is needed for an application, an interface between the sensor and the data converter must be used to modify the sensor output. This interfacing circuit can be as simple as discrete components set up as a filter, or as complicated as an integrated front-end signal processor.

2.1 Wireless Sensor Networks

A Wireless Sensor Network (WSN) is a system comprised of wireless motes that communicate data via radio transmission. The system can be comprised of a single mote reporting to a base station, or thousands of motes communicating both with each other and to a central base station. One of the main functions of a Wireless Sensor Network is to collect and report data. A wireless mote that is used to collect data, especially audio data, requires an "always on" approach so that it does not miss an important event [1]. This approach leads to large power consumption, and as a wireless device, this results in battery life being

a limiting factor. This can be addressed through the use of energy harvesting (as discussed in Section 2.6) or through the use of an Analog Signal Processor (ASP) that operates while the digital mote is in a low-power sleep mode. The ASP can be a custom integrated circuit (IC) or a reconfigurable device [2]. Such devices require fine tuning of the analog front-end, but result in decreased power consumption [3, 4].

During operation, data is usually collected from an analog sensor. A specific wireless mote such as a TelosB or PanStamp have inputs with built-in Analog-to-Digital Converters (ADC). Each converter has specific input requirements for reading data and converting it to the digital domain. WSNs are typically used as surveillance networks such as systems that monitor acoustics [5]. When a WSN is set up to monitor a location, it can be done using microphones, vibration sensors, light-sensors, or proximity sensors. These sensors usually operate in the analog domain and require interfacing circuitry to work with the wireless mote.

2.2 Analog Sensor Interfacing

An analog sensor is a device that takes an occurrence of a natural phenomenon and converts this data to an electrical signal. Analog sensors will operate as long as they are connected to a power source. This allows the sensor to be constantly outputting data based on the input of the device. Analog sensors come in the form of microphones, light sensors, proximity sensors, vibration sensors, gyroscopes, thermistors, capacitive sensors, thermocouples, or humidity sensors. In most cases, the output from these sensors is input to an ADC to allow for analysis in the digital domain. When considering a WSN, most wireless motes have built-in ADCs to convert to the digital domain.

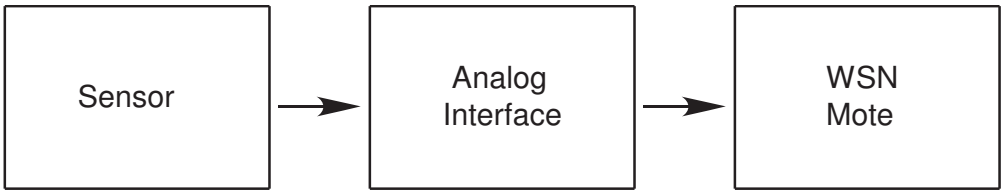

Figure 2.1: Sensor Interfacing flow chart.

When dealing with an analog sensor that outputs a voltage, some situations allow for the output of the sensor to be sent directly to the ADC input pin of the wireless mote. In a scenario where the sensor output is not large enough to be detected by the ADC, an interfacing amplifier must be added for operation. An analog sensor that does not output a voltage requires more consideration when interfacing with a wireless mote. Sensors such as thermistors or capacitive-based sensors output no voltage at all. These sensors must be combined with an interfacing circuit to generate a voltage that can be read by the WSN (Fig. 2.1).

Analog sensors monitor different types of events, but are classified more often by their type of output. As stated, most sensors output a voltage. To interface this voltage with a wireless mote, it usually requires amplification. Sensors such as thermocouples require more than a simple amplifier, and need temperature compensation at the measurement location [6]. To accomplish this, a thermocouple amplifier is used with an additional cold-junction compensation circuit to reduce measurement error [7]. For sensors such as thermistors, a circuit like the Wheatstone Bridge can be used to convert this sensor output to a voltage. Capacitive-based sensors can connected as part of a bridge [8] or attached to oscillators [9], with changes in capacitance corresponding to measurable changes in oscillator output frequency.

The interfacing circuit needs to take into consideration both the constraints of the WSN as well as the operation of the analog sensor. For instance, when dealing with a thermistor, a bridge circuit can be used to convert the resistance value to an output voltage [10]. However, the bridge circuit needs to be customized to operate with the respective resistor range. Utilizing a bridge circuit can result in the output railing too early, or no response at all depending on the size of the other resistors in the bridge. To ensure operation, the bridge must use resistors that will generate a voltage for the specific resistor range of the thermistor [11]. This can be done using discrete components, by replacing resistor sizes to match the analog sensor; however the discrete systems will be much larger and tend to consume more power. A reconfigurable IC can be used as long as the necessary parts are included in its build kit. Custom IC solutions are expensive, but will yield the best results. By prototyping different forms of sensor interfacing with a custom integrated circuit, a reconfigurable IC can

be designed that covers the necessary aspects of sensor interfacing for multiple analog sensor types [12].

2.3 Field Programmable Analog Arrays

The Field Programmable Analog Array (FPAA) is a reconfigurable mixed-signal integrated circuit. The FPAA fills a parallel purpose to the Field Programmable Gate Array (FPGA). The FPGA allows for digital logic circuits to be synthesized post fabrication on the IC. An FPAA also allows for post fabrication circuit synthesis, but focuses more on analog designs [13, 14]. The designs can range from simple systems to complex designed. FPAAs can be used to synthesize common devices such as amplifiers or can be used to set up a fully functioning front-end Analog Signal Processor [15].

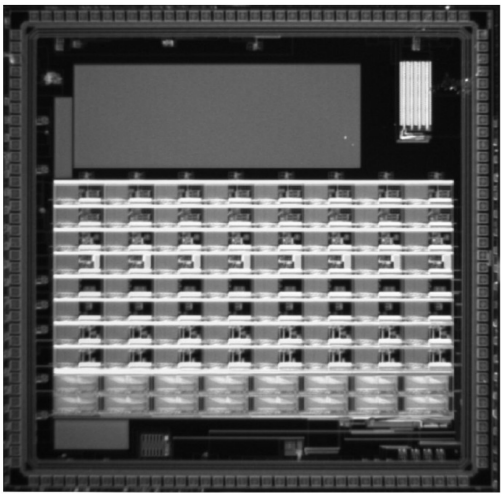

Figure 2.2: Die photo of Reconfigurable Analog/Mixed-Signal Platform (RAMP).

The FPAA, or Reconfigurable Analog/Mixed-Signal Platform (RAMP) detailed in [16] makes use of the FPAA structure to focus on providing an increased number of signal processing and computational elements (Fig. 2.2). The RAMP consists of ten stages of Computational Analog Blocks (CABs) including specific stages for spectral-analysis, transconductors, sensor interfacing, mixed-signal, digital computation, and general transistors. Each of the ten stages is repeated over eight channels which can be connected individually or as a group.

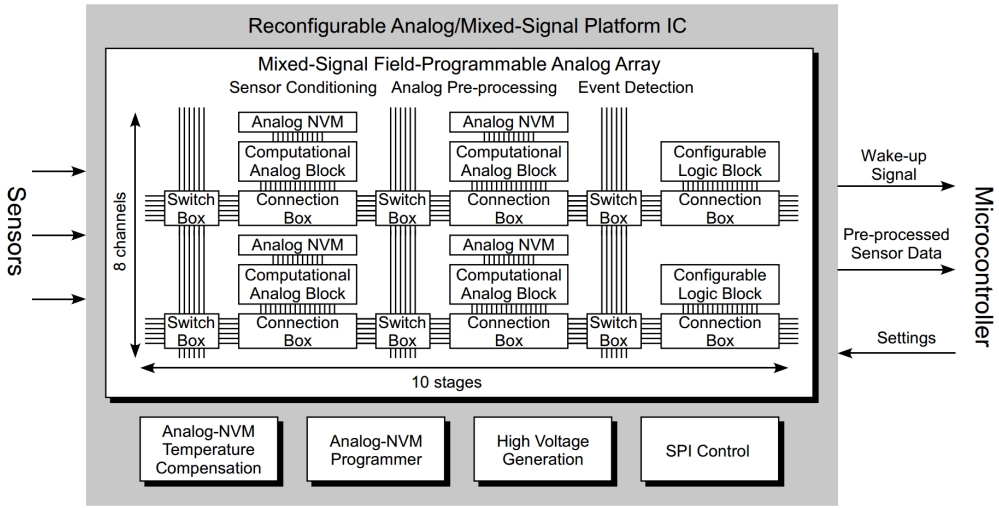

Figure 2.3: RAMP block diagram.

The channels in the spectral-analysis stage include bandpass filters in the form of capacitively coupled current conveyor (C4) filters, peak detectors, adaptive-time-constant filters, and operational transconductance amplifiers (OTAs). The channels in the mixed-signal stage include comparators, sample and holds, pulse generators, timers, and starved inverters. The digital stages include Lookup Tables and JK flip flops for digital logic.

Reconfiguration of the RAMP is achieved via two different switch regions. Programmable switches in the switch box allow for system wide connections to be made between CABs and the connection boxes allow for local routing within a given CAB (Fig. 2.3). These switches are implemented using SRAM-controlled T-gates (NMOS and PMOS transistors connected in parallel to create a rail-to-rail switch). Each T-gate switch is connected to an individual SRAM cell that can be set to "on" or "off." A particular configuration is loaded into the FPAA using an on-chip serial peripheral interface. In total, 20,380 switches are included in the RAMP [16].

Each of the CABs are connected to tunable biases, allowing for the performance of the individual circuits to be modified to fit a design constraint where applicable. Floating-gate transistors have been leveraged to provide accurate bias currents for the circuits that include programmable parameters (such as corner frequencies, gain, etc.).

2.4 Floating-Gate Transistors

A floating-gate transistor is the building block of modern flash memory. The structure of the floating-gate is a transistor with a capacitor attached in series with the gate. This capacitor causes the gate of the transistor to be "floating" and gives the device its name. Charge can be applied to the floating gate to create a memory cell, or in the case of analog electronics, a controlled current source. By loading a specific amount of charge onto the floating-gate, a corresponding current is allowed through the transistor [17, 18].

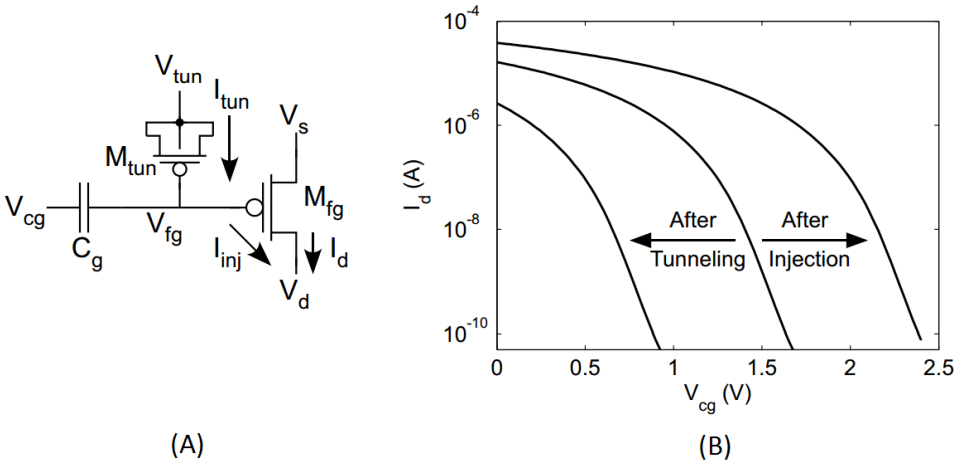

Figure 2.4: (A) Schematic of Floating-Gate Transistor. (B) Floating-Gate Transistor IV relationship.

Two different processes are used to apply or remove charge from a floating-gate. Hot-carrier injection is used to add charge to the floating-gate and Fowler-Nordheim tunneling is used to remove charge. Fig. 2.4 details the schematic, (A) of a floating-gate transistor as well as the IV relationship, (B) of the floating-gate after tunneling and after injection. Injection occurs when a large source-to-drain potential is applied to the floating-gate transistor, causing high energy carriers to impact-ionize at the drain. A fraction of the ionized electrons disperse with enough energy to overcome the oxide barrier and inject onto the floating node [17]. A MOSCAP, M_{tun} (PMOS transistor with source, drain, and body connected on one side, with gate on the other) is connected to the floating node and is used for tunneling to remove charge to the device. To initiate tunneling, V_{tun} is raised to a high voltage, typically higher than the reverse breakdown voltage of the source/drain, but less than the breakdown

of the well-to-substrate junction [19]. The use of floating-gate transistors lets the RAMP implement a wide range of different applications. This research details the use of the RAMP as a sensor interface in Chapter 4, but also begins the process of implementing an energy harvesting system on the reconfigurable IC in Chapter 5.

2.5 Energy Harvesting

Energy Harvesting (EH) refers to scavenging excess energy from the environment for use with an electrical circuit. Once harvested, this energy is stored on the circuit for immediate or future use [20]. An energy harvesting system can be broken down into five different sub-systems: the Energy Transducer, Power Converter, Control Unit, Storage Buffer, and Application Unit (Fig. 2.5). The sub-systems interact linearly and start with the Energy Transducer. The transducer converts a specific type of energy into a voltage. This could be in the form of a photovoltaic cell for sunlight, a thermoelectric generator for heat, a piezoelectric generator for vibrations, an electromagnetic transducer for radio waves, or a micro-fuel cell for chemical reactions [21]. Each harvesting application requires a specific transducer to match the energy to be harvested, and the output of the transducer can be alternating-current (AC) or direct-current (DC) depending on the respective harvested energy.

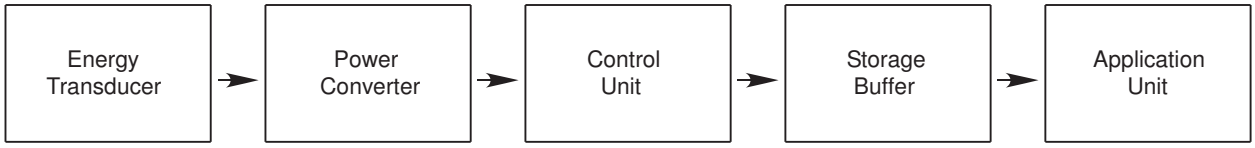

Figure 2.5: Energy Harvesting System flow chart.

The voltage output of the transducer is used as an input to the second stage of the EH system, the power converter. The power converter takes this input and converts it to a desired level for storage in the circuit. The type of power converter used is mainly dependent on the transducer, and in essence, the type of energy being scavenged. An electromagnetic or piezoelectric transducer will produce an AC output, requiring the use of an AC-to-DC converter such as a half or full-wave rectifier. A photovoltaic cell or thermoelectric generator

produce a DC output, requiring a DC-to-DC converter such as a charge pump, buck/boost converter, or low-dropout regulator. The type of power converter needed will also impose limitations on the IC. For instance, a DC-to-DC buck/boost converter requires a large inductor that can not be integrated, requiring an off-chip device, while the charge pump does not require an inductor and can be fully integrated.

After the signal is passed through the power converter, it is picked up by the third stage of the EH system, the control unit. The control unit optimizes the efficiency of the harvesting process by making changes to the operation of the power converter [22]. The method used by the control unit is selected based on the energy transducer and power converter. The simplest unit is Design-Time Component Matching, where the output of the transducer is connected directly to the storage buffer. Maximum Power Point Tracking ensures the power converter is operating at maximum efficiency through a closed loop structure [23]. Reference Voltage Tracking switches between a normal operation and open circuit mode to make use of the linear relationship between the transducer's maximum voltage and the open circuit voltage. The Perturb and Observe method periodically applies small variations to the power converter, such as varying the duty cycle of a buck/boost converter or the switching frequency of the charge pump. This causes small changes in the circuit operating point and output power. The output power is recorded and compared to its value before the variation. Based on the difference between the two values, another variation is performed in the same or opposite direction.

The storage buffer is where the energy is held until it is needed for use by the circuit. This storage unit can be a battery or super capacitor. The final stage of the EH system, the application unit, is specific to the device being powered. This stage determines how and when the energy from the storage buffer is used to either power or supplement power for an electronic device. In the context of a WSN, this decision could be made based upon how often the wireless mote will be awake and using its radio [24]. If the mote is constantly broadcasting, the amount of energy harvested may only be enough to supplement power, increasing the preexisting battery life. If the mote only broadcasts once a minute, and is in sleep mode otherwise, the harvested energy may be enough to power the mote exclusively.

When working with a specific scenario, the energy transducer must match the application

environment. When monitoring industrial machinery such as a coal gasifier, heat is the most common source of excess energy. An energy harvesting system in this environment would use a thermoelectric generator to convert the scavenged heat into electrical energy for later use.

2.6 Coal Gasifiers

A coal gasifier refractory is used to convert coal into compounds that can be used for industrial energy (carbon monoxide, hydrogen, or natural gas). A gasifier is heated up to extreme temperatures (greater than 1300°C) to initiate the conversion from coal to a useable form of energy. The erosive conditions caused by such high temperatures cause degradation of the refractory over time. This breakdown leads to the the refractory lining being penetrated due to the slag inside the gasifier. By monitoring the internal conditions of the refractory, an early warning system can alert when the system needs shut down for repairs before a catastrophic failure occurs. Currently, openings are drilled into the refractory wall for sensors to be placed inside the lining. However, this causes a loss of integrity at the access point. A refractory lining is only as stable as its weakest point, and using a sensor in this manner weakens the whole system.

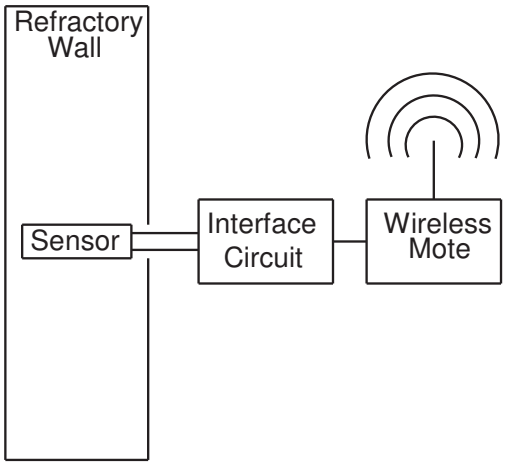

Figure 2.6: Diagram of sensor, interface circuitry, and wireless sensor mote with respect to the coal gasifier.

The custom integrated circuit detailed in Chapter 3 is for use with a new system designed

to circumvent this problem. By embedding sensors directly in the bricks used to build the refractory wall, the integrity of the gasifier liner remains undisturbed. The custom IC has been designed to interface between the embedded brick and a wireless sensor network as shown in Fig. 2.6.

2.7 Chapter Summary

This chapter covered the subjects that will be put to use in the body of this thesis. Wireless sensor networks are a good match for low-power analog integrated circuits, and will be utilized throughout the following work. The focus of this thesis involves interfacing between analog sensors and WSNs. This process will be covered with both custom ICs (for use with a coal gasifier) and reconfigurable integrated circuits such as the RAMP described in this chapter. A custom IC solution will be described first in Chapter 3 as a prototype for improvements made to the reconfigurable solution in Chapter 4. This chapter also covered the basics of an energy harvesting system which will be discussed in detail in Chapter 5.

Chapter 3

Custom Integrated Circuits

One of the largest barriers for working with analog integrated circuits is the lengthy design procedure behind fabricating a new chip. However, when dealing with a custom analog sensor, sometimes a custom solution is required. A custom IC was designed for use with thermocouples, thermistors, and capacitive-based sensors. This IC contains circuits for thermocouple amplifiers, a bandgap temperature sensor for cold-junction compensation of the thermocouples, a Wheatstone-bridge circuit for use with resistive-based sensors, and a circuit for use with capacitive-based sensors.

This IC was designed for an application measuring the internal characteristics of a coal gasifier. For this project, custom thermocouples, thermistors, and capacitive-based sensors were fabricated in-house at West Virginia University to monitor coal gasifiers. The IC was designed to work specifically with these custom sensors. A micrograph of the custom integrated circuit can be seen in Fig. 3.1.

3.1 Operational Amplifier (OpAmp)

All four types of circuits included on the custom IC require the use of an Operational Amplifier (OpAmp). The OpAmp works as the main component of the thermocouple amplifier and is used as an output buffer for the cold-junction compensator [7]. The Wheatstone bridge requires two OpAmps to generate a voltage proportional to the change in resistance. The capacitive-based sensor uses the OpAmp as a comparator to build a relaxation oscillator

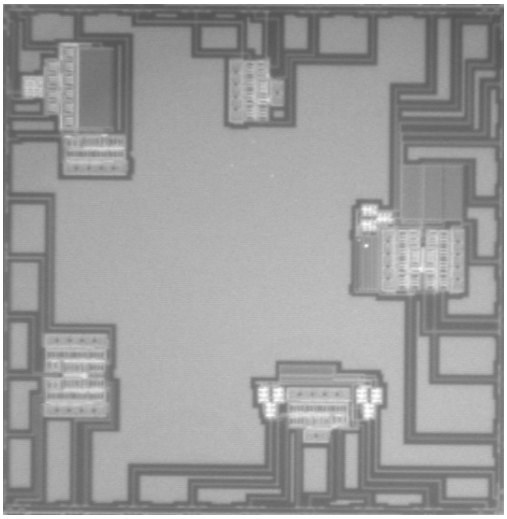

Figure 3.1: Die photo of Half-Micron IC Designed for Custom Sensor Interfacing.

for reporting capacitance changes in the sensor. The same OpAmp design and layout was used for each of the applications required on the IC.

To fit the constraints put forth by all of the required circuits, a two-stage CMOS OpAmp was designed [25] (Fig. 3.2). The OpAmp was designed with a systematic approach, addressing each performance metric and tuning the circuit parameters to optimize performance [26]. By focusing on general performance metrics such as input common-mode range, open loop gain, common-mode rejection ratio, and slew-rate, a general purpose OpAmp was designed. When making the decision to use PMOS or NMOS transistors as the input pair, the application was the deciding factor. Since the analog sensors have a low DC value, utilizing PMOS input transistors allows for an input that is close to ground to be sensed more reliably than if an NMOS input pair was [27].

3.2 Thermocouple Interfacing

A thermocouple outputs a temperature-dependent voltage. As a voltage output, this is already in the correct domain for use with a wireless mote. However, a problem arises when the voltage is too small for the ADC input on the wireless mote. To allow for the mote to read the signal from the thermocouple, an amplifier must be used at the interface between the two devices. The thermocouples fabricated have slightly different properties based on

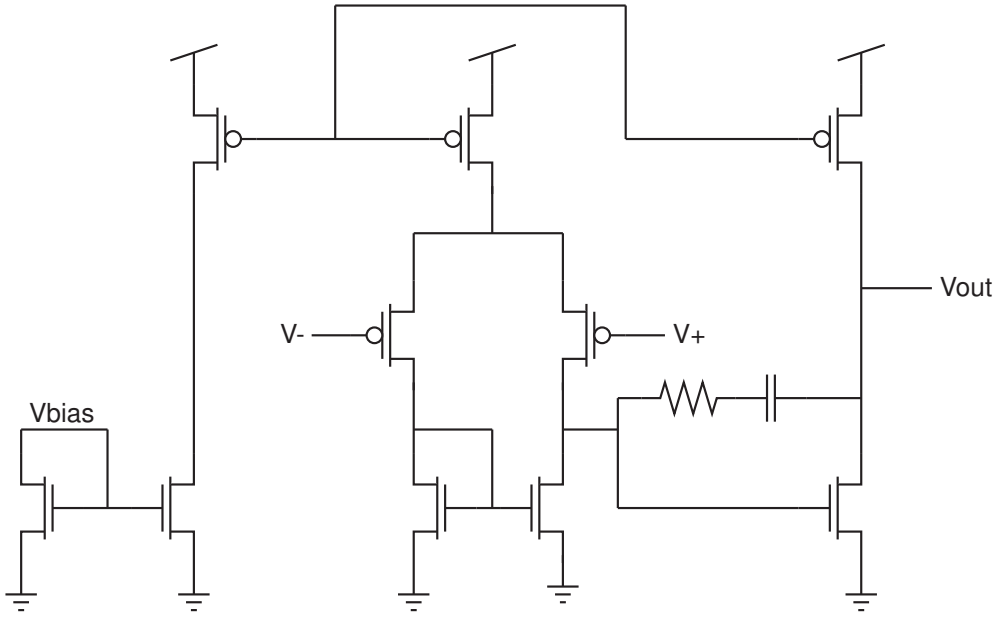

Figure 3.2: Schematic of Operational Amplifier.

the materials used, but all operate within a similar range of about 25mV. The amplifier on the IC uses a non-inverting design, with added capacitors for noise filtering (Fig. 3.3).

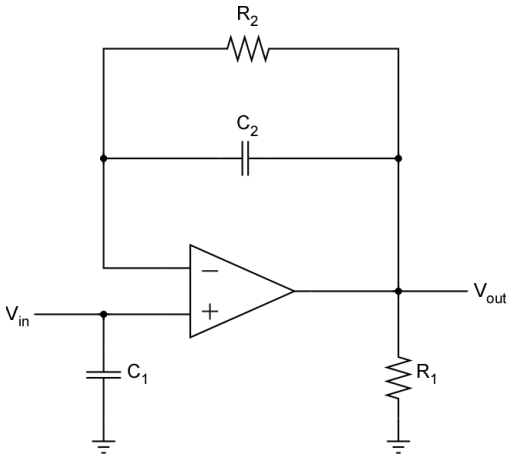

Figure 3.3: Schematic of Thermocouple Amplifier.

The circuit was first tested without cold-junction compensation. The thermocouple amplifier received its input directly from the thermocouple, and reported furnace temperature without any temperature-measurement compensation. The thermocouple amplifier reported the actual furnace temperature within a 4% margin of error. On Fig. 3.4, plot (A) shows

the measured temperature versus actual temperature. The thermocouple has been designed to operate above 1000°C, and plot (B) shows the percent error from this temperature up to its maximum of 1500°C.

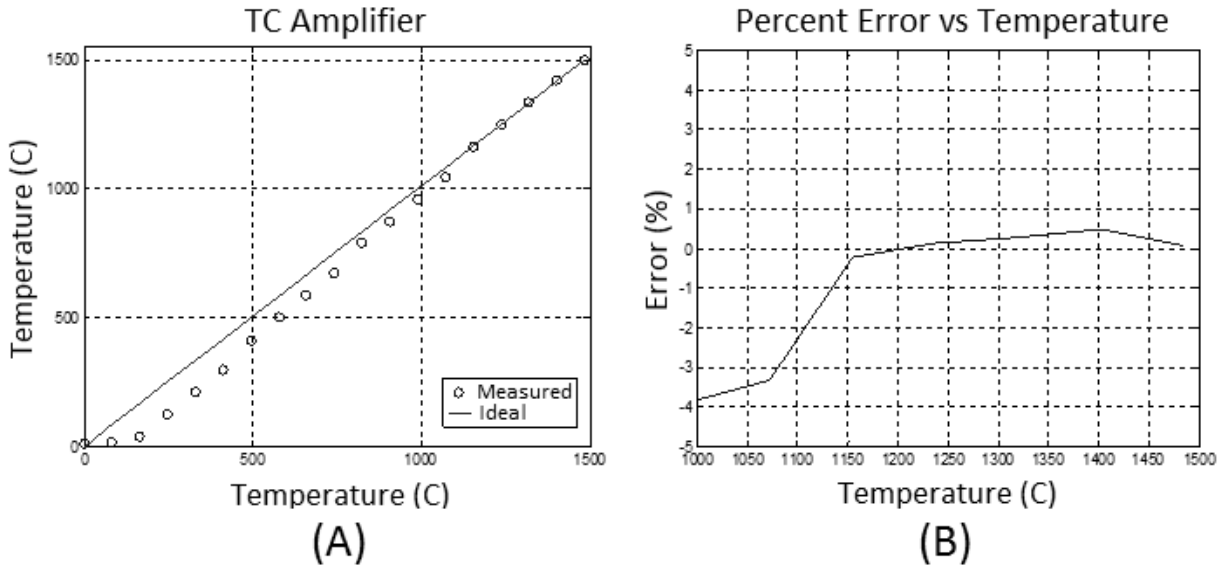

Figure 3.4: (A) Output of Thermocouple Amplifier. (B) Percent Error of Thermocouple Amplifier Performance.

3.2.1 Temperature-Measurement Compensation

Due to the properties of a thermocouple, and the fact that multiple types of metal are used to connect the sensor to the circuit (creating small, parasitic thermocouple additions), the temperature of the circuit amplifying the signal must be taken into consideration. An offset must be added to the thermocouple voltage to compensate for errors introduced from the parasitic thermocouples. To compensate, a temperature-dependent Bandgap circuit ((B) of Fig. 3.5) is used to generate an offset proportional to the temperature of the interfacing circuit and wireless mote. This circuit is referred to as a Cold-Junction Compensator (CJC).

The operation of the Bandgap Temperature sensor is based around the concept that the forward voltage of a diode is temperature-dependent (Eq. 3.1,3.2). For the circuit used as the cold-junction compensator, the base-emitter junctions of the Bipolar Junction Transistors (BJTs) act as diodes due to the transistors being in diode connection.

$$I = I_s(e^{\frac{V_D}{nV_T}} - 1) \tag{3.1}$$

$$V_T = \frac{kT}{q} \tag{3.2}$$

This circuit was tested over a range of 0-120°C, accounting for the full range of temperatures that may be encountered when measuring the thermocouple outside of the furnace. The output of this circuit was designed to correspond to the measurement compensation needed for the WVU-designed thermocouple and is shown in (A) of Fig. 3.5.

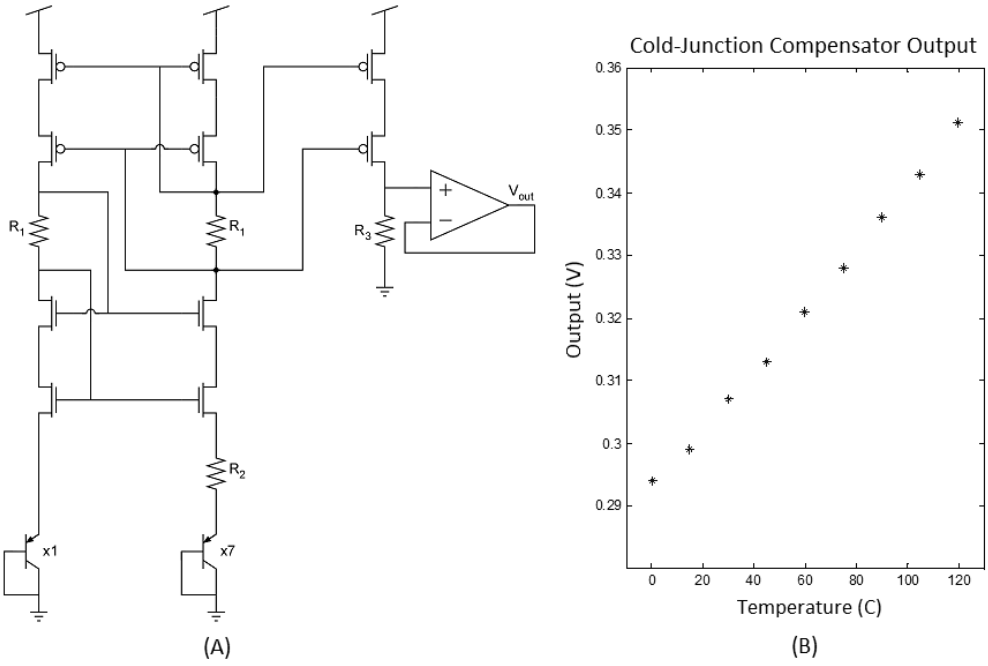

Figure 3.5: (A) Schematic of Temperature Dependent Cold-Junction Compensator. (B) Output of Temperature Dependent Cold-Junction Compensator.

The thermocouple amplifier and cold-junction compensator were designed and tested separately to ensure circuit performance. After their operation was verified, the circuits were then combined to more accurately report the temperature inside of the furnace. The offset generated by the Bandgap circuit is added to the thermocouple's negative terminal, increasing its "ground" potential and allowing for more accurate measurements. Fig. 3.6 shows the full circuit schematic with the cold-junction compensator connected to the negative

terminal of the thermocouple. Fig. 3.7 shows the the output and percent error with cold-junction compensation implemented to the circuit.

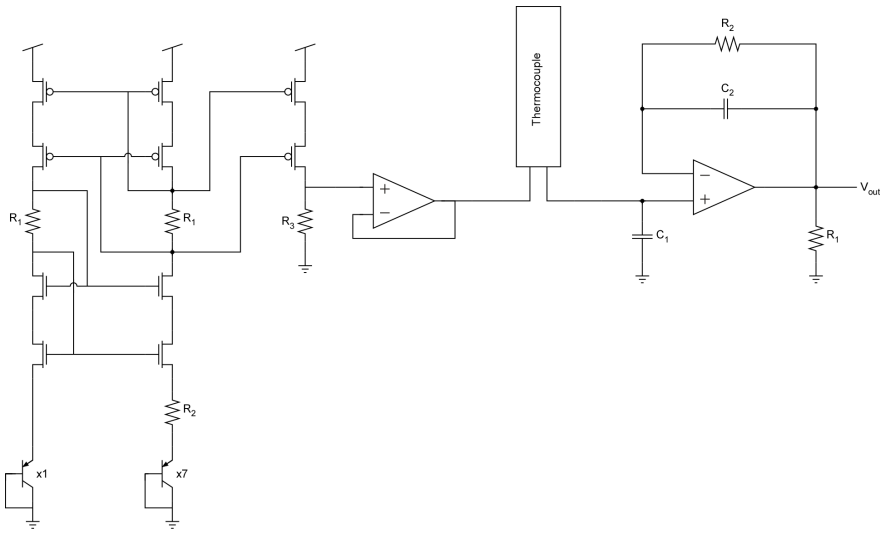

Figure 3.6: Schematic of Full Thermocouple Interfacing Circuit (Amplifier with Cold-Junction Compensator).

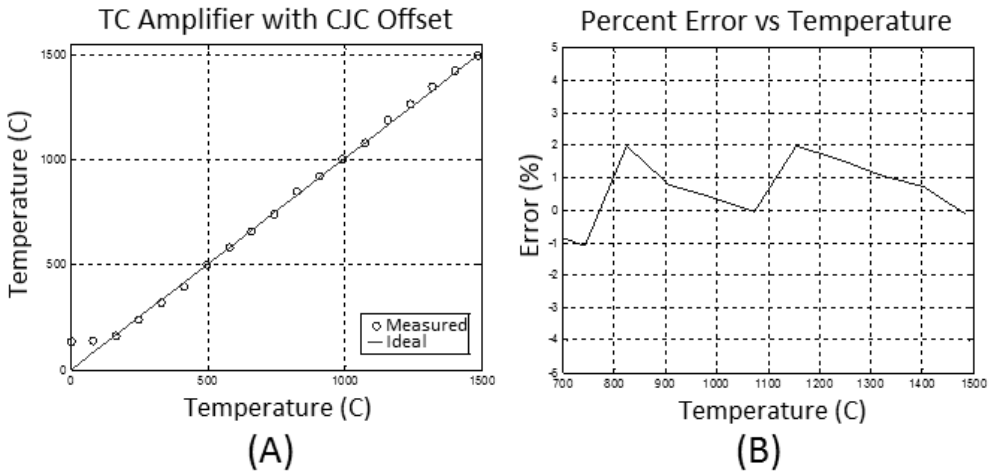

Figure 3.7: (A) Output of Full Thermocouple Interfacing Circuit (Amplifier with Cold-Junction Compensator). (B) Percent Error of Full Thermocouple Interfacing Circuit Performance

The CJC adds a static offset to the thermocouple depending on the temperature where the measurement is taking place. This offset is then seen by the thermocouple amplifier, via the negative terminal of the thermocouple, allowing for a more accurate temperature reading. As stated, without cold-junction compensation, the thermocouple amplifier reported

the furnace temperature to within a 4% margin of error. With cold-junction compensation, the thermocouple amplifier reported the furnace temperature to within a 2% margin of error. Fig. 3.8 shows the measured temperature versus actual temperature for just the thermocouple amplifier and with the cold-junction compensation included. At extremely low temperatures, the cold-junction compensator causes error, but it is opposite in magnitude to the circuit without compensation. At mid to high temperatures, the cold-junction compensator increases the accuracy of the reading.

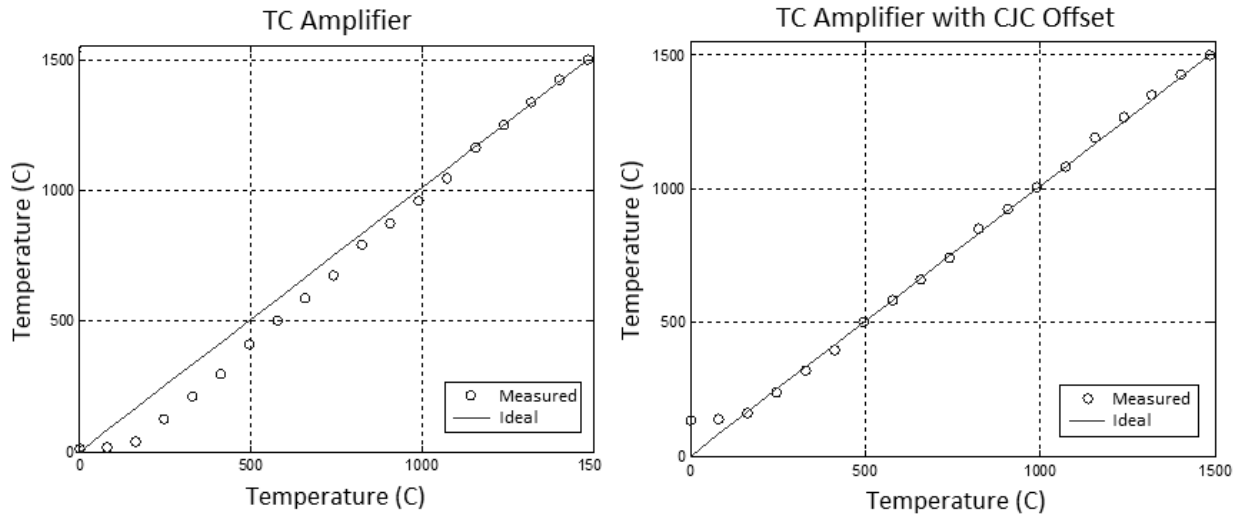

Figure 3.8: Comparison between output of Thermocouple Amplifier with and without Cold-Junction Compensation.

3.3 Thermistor Interfacing

To interface between a thermistor and a wireless mote, the resistance value of the thermistor must be converted to a voltage readable by the mote. A bridge circuit allows for this conversion to be possible. The Wheatstone Bridge (Fig. 3.9) is a specific type of bridge that utilizes two OpAmps to generate a rail-to-rail voltage output from the sensed resistance value. Three static resistors: R_1, R_2, an R_{mid} are calculated based on the resistance values of the sensor's minimum (R_{min}) and maximum (R_{max}) values (Eq. 3.3). The reference values V_{ref1} and V_{ref2} are calculated based on the chosen resistance values (Eq. 3.4).

$$R_{mid} = \frac{R_{max} - R_{min}}{2} + R_{min} \tag{3.3}$$

$$V_{out} = V_{ref2} + \delta(\frac{R_2}{R_1})(V_{ref1} - V_{ref2}) \tag{3.4}$$

This circuit is an integrated version of the circuit that was previously implemented using discrete, commercial components for the coal gasifier project. This circuit is designed to interface with the WVU-designed resistive-based sensors. Two testing methods were used to test this circuits performance. The first test utilized a hand-turned variable resistor to generate a base-line performance test. The second testing method utilized a thermistor and furnace to show the circuit's performance in a real scenario. The Wheatstone-bridge correctly reports the temperature inside of the furnace to within a 3% margin of error (shown in Fig. 3.10).

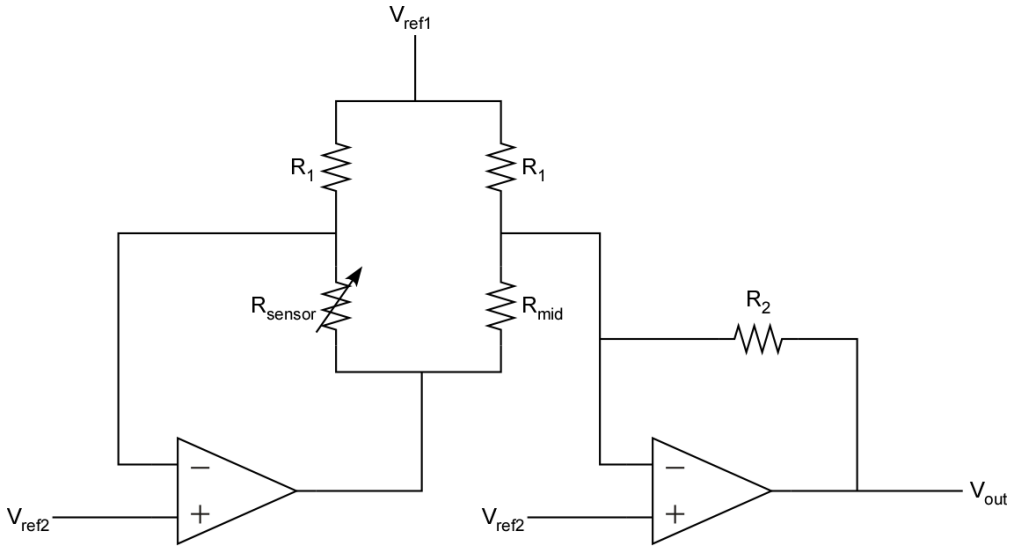

Figure 3.9: Schematic of Wheatstone Bridge.

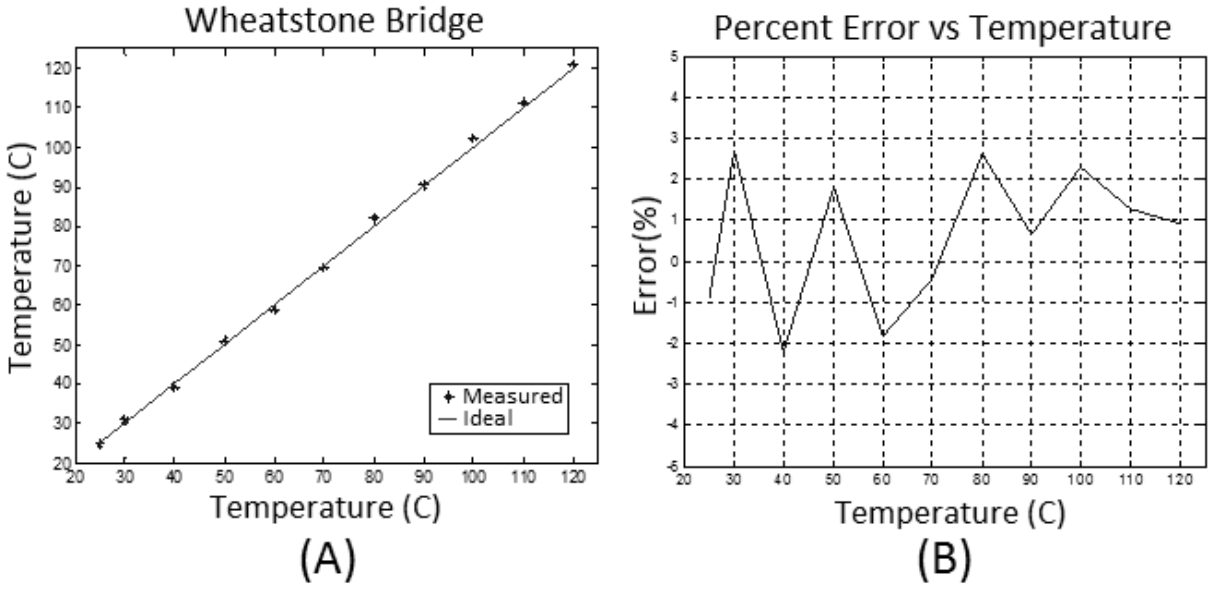

Figure 3.10: (A) Output of Wheatstone Bridge. (B) Percent Error of Wheatstone Bridge Performance

3.4 Capacitive Sensor Interfacing

The third type of analog sensor used by the coal gasifier project was capacitive-based. This sensor produced a different capacitance value based on the temperature inside the furnace. As the wireless mote can not read capacitance values, a conversion to the voltage domain was required at the interface. To accomplish this, a relaxation oscillator was designed and is shown in Fig. 3.11. This circuit produces a 50% duty cycle oscillation with a frequency that is inversely related to the size of a capacitor [28]. As the wireless mote can perform some signal analysis, the frequency of the input was used to determine the capacitance value of the analog sensor. As the capacitance grows larger with increasing temperature, the relaxation oscillator takes longer to charge/discharge, causing a decrease in output frequency. Fig. 3.12 shows the circuit performance, detailing the decrease in output frequency corresponding to an increase in sensor capacitance.

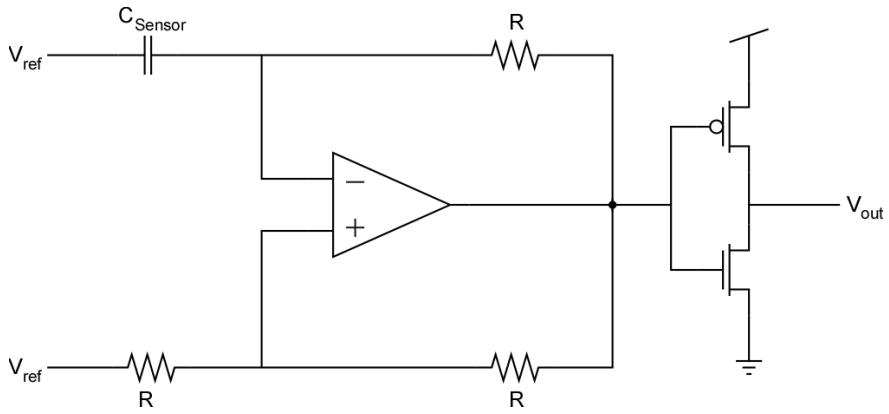

Figure 3.11: Schematic of Capacitive Sensor Interfacing Circuit.

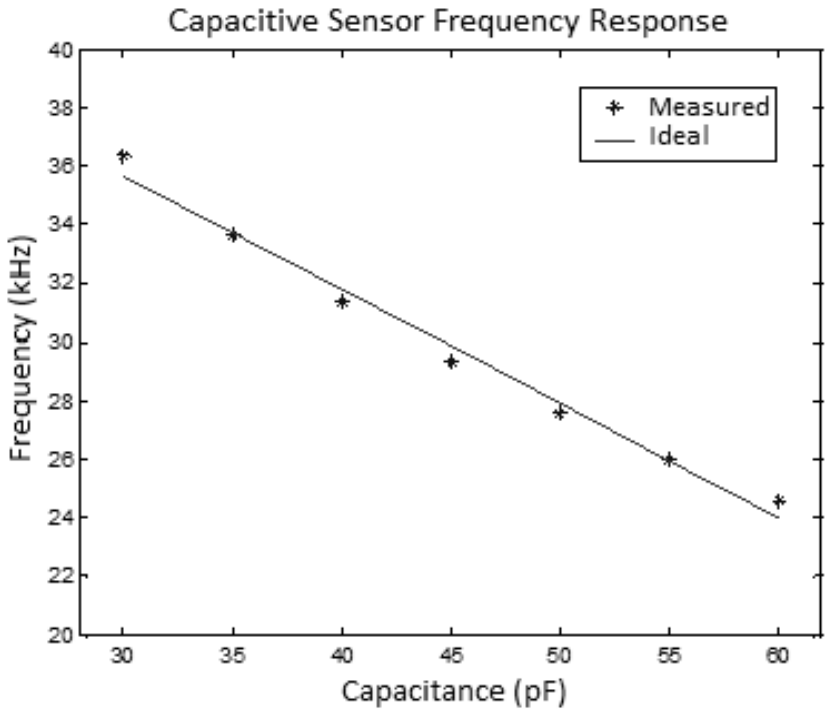

Figure 3.12: Output of Capacitive Sensor Interfacing Circuit.

3.5 Digital Peripheral Circuitry

At the time of fabrication, thermocouple output values had already been characterized for the custom sensors, allowing for the thermocouple amplifier to be fully integrated. The resistance values for the thermistors however, were not yet determined. This called for a circuit that could be modified to allow for a range of resistance values. To accomplish this, digital circuits were used as a peripheral to the Wheatstone Bridge, allowing for different R2 and Rmid values to be used based on the design constraints. Fig. 3.13 shows the schematic for choosing resistor sizing. Selection 1 and 2 use binary inputs to determine how many resistors will be added together for the desired resistance value. T-gates are used as switches to make the connection between the input and output flow through the resistors specified by the binary input.

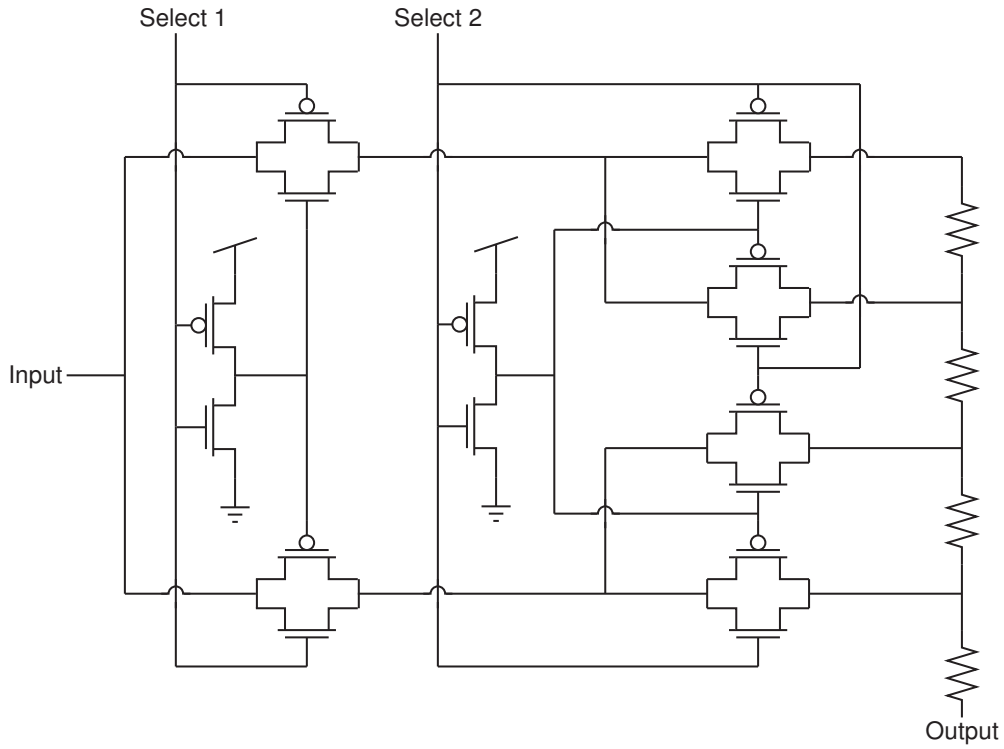

Figure 3.13: Schematic of digital circuitry used to select resistor size.

3.6 WSN Transmission

To test the performance of the sensor interfacing circuit, they were connected to both a multimeter and TelosB wireless mote. The TelosB was used to broadcast the data via its antenna back to a base-station for recording. The attached multimeter was used to verify the data being recorded at the base-station. Fig. 3.14 shows a comparison between (A) the data measured by the multimeter for verification and (B) the data received wirelessly by the WSN base-station.

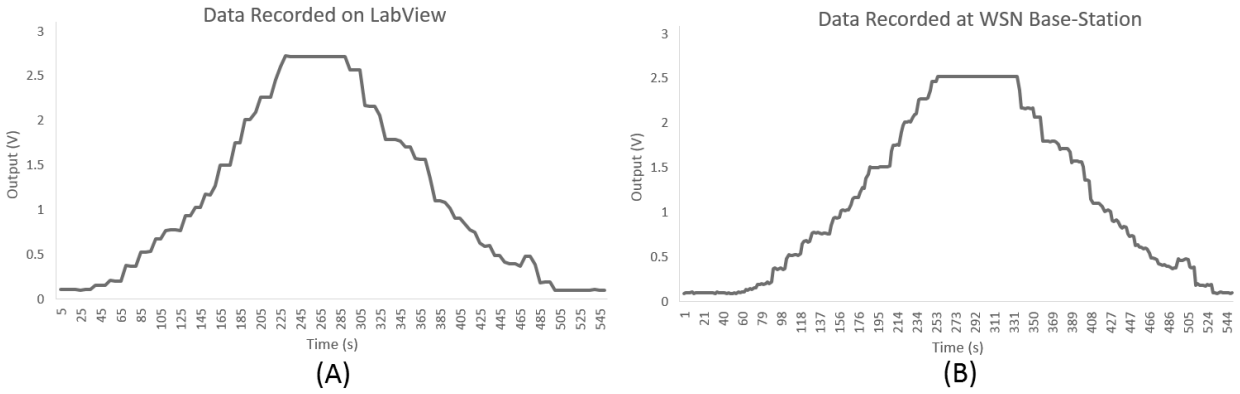

Figure 3.14: (A) Sensor data recorded at multimeter for verification. (B) Sensor data recorded at WSN base-station

3.7 Chapter Summary

This chapter covered the design and testing of a custom integrated circuit for use as an interface between analog sensors and a wireless sensor mote. The circuits described were designed specifically to function with the analog sensors designed at WVU to work in a coal gasifier. The characterization of each circuit confirms their operation as well as gives important insight for adding these systems to a reconfigurable integrated circuit such as the FPAA. A system as large as the FPAA has a long design cycle and an expensive fabrication process. By prototyping these circuits on a custom IC, the need to iterate on a physical design for the FPAA has been lessened, furthering its interfacing capabilities.

Chapter 4

Reconfigurable Integrated Circuits

Digital circuit designers can rely on the Field Programmable Gate Array (FPGA) to synthesize circuits without having to go through an expensive fabrication process. New advancements in Floating Gate technology have allowed for Analog Circuit Designers to make use of the Field Programmable Analog Array (FPAA). By programming a floating gate transistor to a specific value, a bias current can be generated for each individual analog circuit on the FPAA. This allows for specific systems to be synthesized with custom biases to match their performance constraints.

The FPAA allows for large-scale applications to be designed and implemented post-fabrication. Applications that would normally require a custom integrated circuit can be achieved completely using the FPAA. For the FPAA to encompass the needs of an application, the circuits built into its Computational Analog Blocks (CABs) must cover a wide range of analog applications, as well as be reconfigured based upon a specific scenario.

4.1 Printed Circuit Board (PCB) Design

The original version of WVU's FPAA [16] printed circuit board (PCB) was designed to operate with either an Arduino or a TelosB wireless mote connected via a serial pin. The Arduino or TelosB was used to interface between a computer and the FPAA for programming. A sketch is loaded on to the micro-controller that describes the internal structure of the FPAA. When a connections list is passed to the controller, a binary file is gener-

ated containing which switches should be set as well as what target values will be used by the floating-gates. The binary file is then passed via serial connection to the FPAA for programming.

A new, four layer PCB has been designed that allows the FPAA to interface with a PanStamp wireless mote. Fig. 4.1 shows the two sides of the new PCB without population of the discrete devices (including the FPAA and PanStamp). Image (A) shows the top of the board and (B) shows the bottom of the board where the footprint for the PanStamp can be seen (bottom center). The PanStamp is similar to the TelosB, but is housed in a smaller package. By making this change, the PanStamp has been included directly on the FPAA PCB. Along with the change to mote interfacing, improvements were made to the external systems housed on the PCB. The main upgrade includes changes to the power-management sector of the PCB.

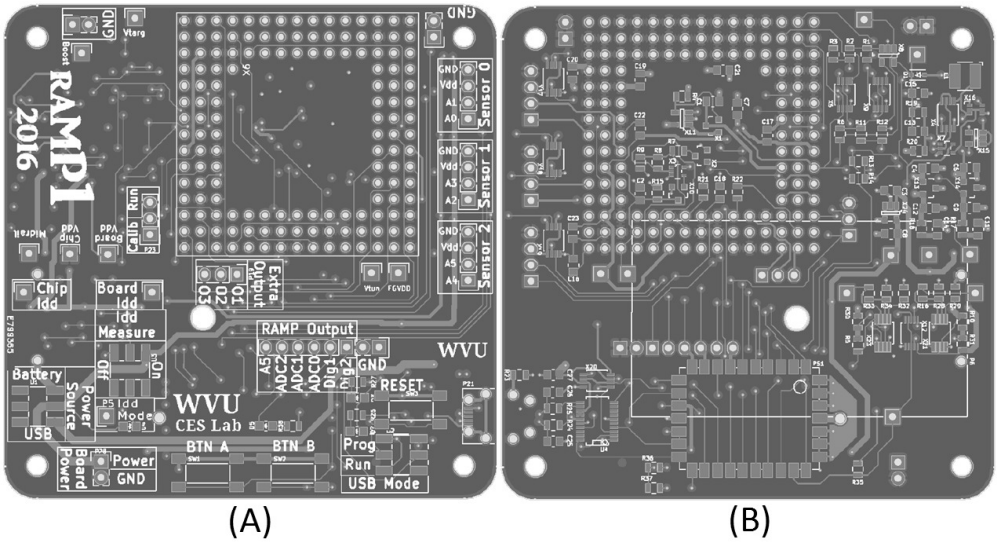

Figure 4.1: (A) Front side of new PCB. (B) Back side of new PCB.

This sector houses the regulators used for generating the necessary voltages required by the FPAA (Digital Vdd, Analog Vdd, Mid-Rail, and the boosted voltage required for floating-gate injection) from either USB or battery power. This is also the sector where power measurements can be made. In the previous iteration of the PCB, a resistor was in series with both board power and chip power. This resistor was shorted using header pins. To measure how much power was being consumed by either the chip or the entire

board, the short between the header pins was removed and the pins could be probed to measure power consumption. With the new design, whether or not the resistor is shorted or in series is controlled using a slide switch. The slide switch enables a digital switch that places the resistor in series with the power supplies. Included with the resistor is an on-board instrumentation amplifier with an output connected directly to an output pin. This allows for precision measurement of the power consumed by the total system as well as the power consumed by the FPAA itself.

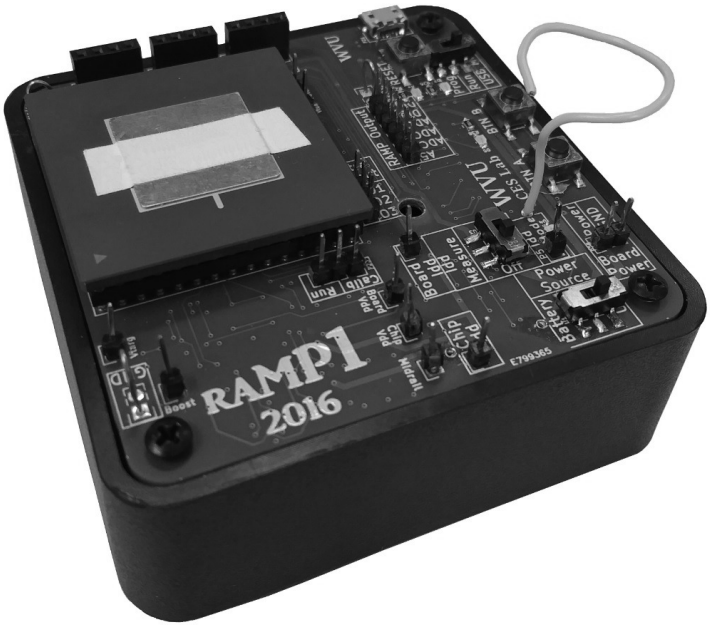

Figure 4.2: Photograph of new PCB fully populated with FPAA, external devices, antenna, and case.

In addition to including the PanStamp directly on the PCB, a USB transceiver was also included in the design. This transceiver allows for the board to be plugged in directly to the computer via USB port. The USB connection can be used for both power and data transmission or just one of the two. With the implementation of the PanStamp and transceiver, the FPAA, as well as all peripheral devices are now housed in one package.

Another improvement made by the inclusion of the PanStamp is more accessible wireless programming. A device called the PanStick is a peripheral PCB for the PanStamp. The PanStick houses a PanStamp, allowing for ease of operation. By using two PanStamps, one housed on the FPAA PCB and one on the PanStick, commands can be sent to the FPAA

via radio communication. The connection file is sent to the PanStick, which has a sketch loaded that causes it to pass the connection file via the antenna. The PanStamp on the FPAA queries the PanStick, receiving the new connection file, and builds the system on the FPAA.

4.2 Acoustic Vehicle Classification

The two Hibernets papers [29, 3] detail how an integrated circuit can be used as an analog signal pre-processor for classifying vehicle presence and vehicle class based on audio data received from a microphone. These papers covered an analog signal processor (ASP) that monitors incoming audio for event detection. The "event" being the occurence of a passing car or truck. The ASP both detects a vehicle presence as well as classifies that vehicle as a car or a truck. This demonstrative project for an ASP's capabilites has been titled Acoustic Vehicle Classification. This project was first discussed in [30] and expanded by the Hibernets papers. To further the scope of this project, as well as demonstrate the abilities of a fully reconfigurable analog system, the project has been recreated on the RAMP. While the RAMP has signal pre-processing components, it is a generic system and has not been designed to work specifically for this application.

The same sampled vehicle data used for the Hibernets projects [29, 3] was used for the project conducted on the RAMP. The data-set consists of forty audio signals: twenty car signals and twenty truck signals. An example car audio signal can be seen in Fig. 4.4. As in the previous projects, the desired outcome is for the system to listen to an audio signal and first determine if a vehicle is present then classify it as either a car or truck. To accomplish this, the data-set was cut in half: ten cars/ten trucks are used for training while the other half is used for testing. The training data-set allows the system to set specific parameters for its components based on the given audio data. The testing data-set is used to determine how well the established system works without any ability for the system to be biased to the data.

To analyze the audio signal, a series of eight parallel, linear systems have been synthesized on the RAMP. A flow chart of the full system design can be seen in Fig. 4.3. Each of the

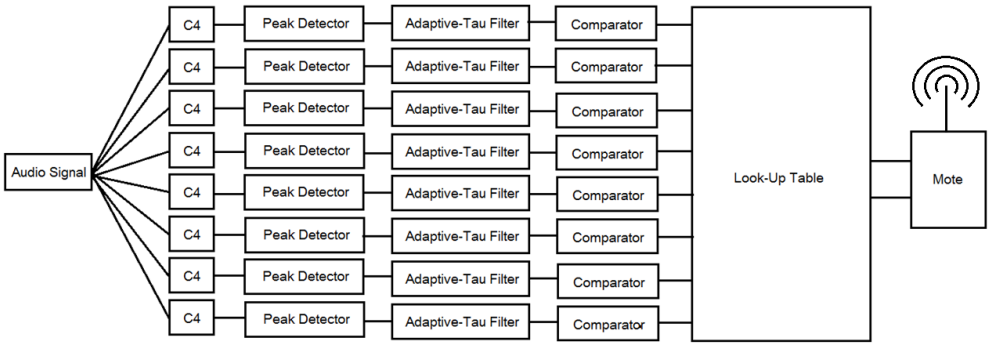

Figure 4.3: Chart detailing the signal flow within the RAMP.

eight parallel channels utilizes the same set of circuits, but each channel has specifically tuned parameters based on the data as well as differences in circuit performance between channels that must be taken into consideration. The system starts by breaking down the signal into eight different frequency bands from 100-1100Hz with close to half-octave spacing using C4 Bandpass filters [31]. The signal is then passed through a peak detector to rectify out the positive half of the signal. An adaptive-tau low-pass filter is then used to produce the Root Mean Square (RMS) voltage of the signal, giving an estimation of the power from each channel. After being passed through a buffer to decrease attenuation, the system uses a comparator to generate a digital signal from a reference determined by the training algorithm. A lookup-table (LUT) is used to analyze the output from the eight comparators to produce two digital signals: one for detecting a vehicle and one for classifying that vehicle as either a car or a truck. Finally, the wireless mote receives data from the two LUT output pins. Once a logical high has been detected from the "vehicle detected" pin, the mote listens to both LUT pins for a set period of time and makes a final decision about the presence of a vehicle.

4.2.1 C4 Bandpass Filters

Eight Capacitively Coupled Current Conveyor (C4) filters (Fig. 4.5) are available on the RAMP, one in each channel of stage 0. Each filter is set up to catch a different frequency range from the input audio signal. The audio signals in the testing data-set have a frequency range from 100 and 1100Hz. To break down this frequency range, each filter is responsible

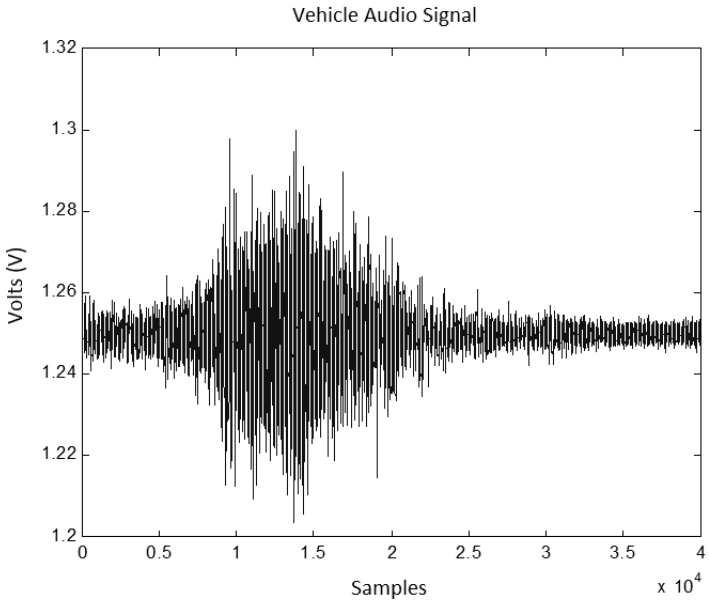

Figure 4.4: Example vehicle audio signal from testing data-set.

for a different range. To account for the full frequency range, the filters are separated by 1/2.353 octave spacing. Exact half-octave spacing was not possible while catching the full signal range.

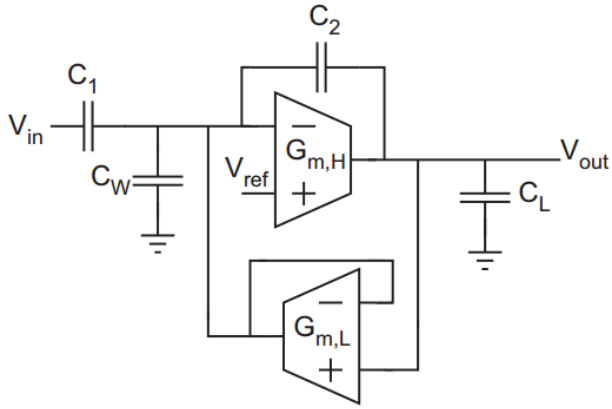

Figure 4.5: Schematic of the C4 Bandpass filter.

The C4 circuits are controlled using the bias currents for each of the Operational Transconductance Amplifiers (OTAs) used in its design. The upper corner frequency is controlled by the OTA $G_{m,H}$ and the lower corner frequency is controlled by $G_{m,L}$. On the RAMP, through the use of floating gates, a current can be generated as a bias for each OTA. By setting the bias currents at separate values, the C4 will operate with set corner frequencies [32]. To set up the C4 filters with the correct octave spacing, each C4 had to be built on the RAMP and tested separately. Due to mismatch on the RAMP itself, each C4 will perform differently with the same bias currents.

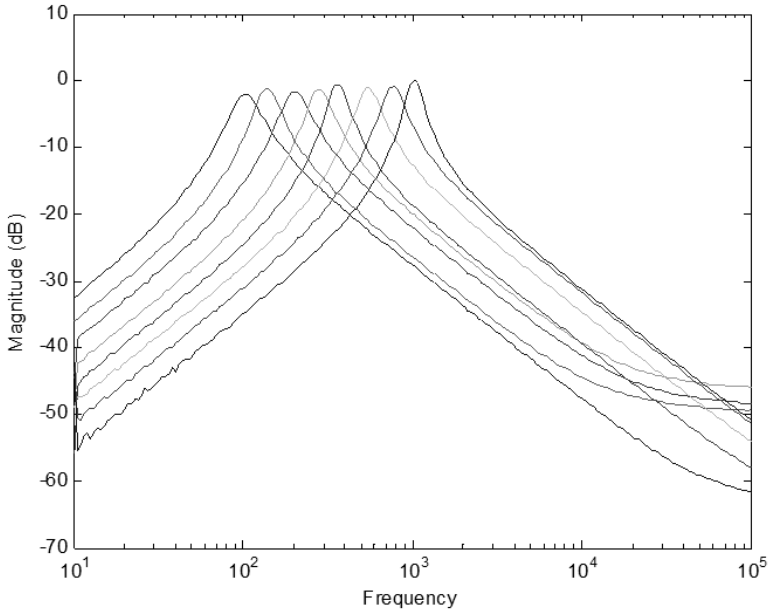

Figure 4.6: Frequency Response for all eight of the C4 Bandpass filters.

A Stanford Research Systems Model SR785 Dynamic Signal Analyzer (DSA) was used to test the frequency response of each C4. The DSA generated an array of sine waves starting at a frequency of 10Hz and ending at 100kHz. By outputting the sine waves to the C4 and reading the gain/attenuation at each frequency, the DSA was able to plot the response shown in Fig. 4.6. To ensure the filters would perform the same during testing as during full operation, the RAMP was loaded with all of the circuits to be used in the system. The output of one C4 filter can be seen in Fig. 4.7. The more circuits that are built onto the RAMP at one time caused more parasitics on the CAB lines, attenuating the signals more

than if only one circuit was built at a time.

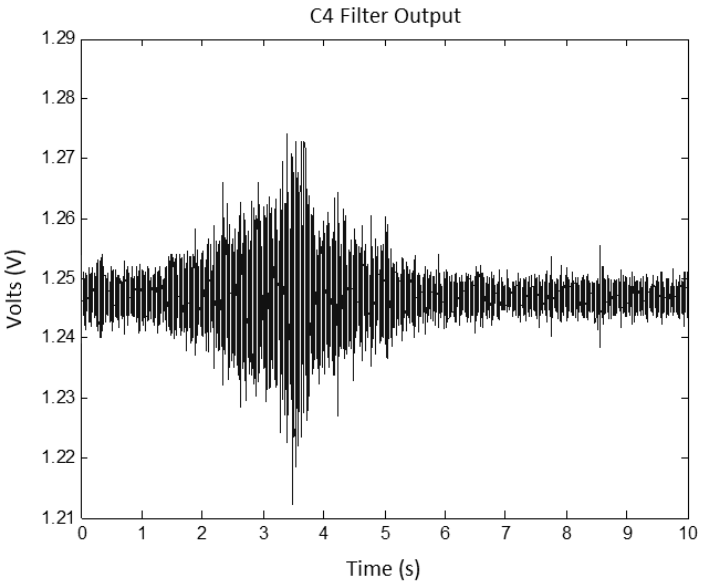

Figure 4.7: Output of the C4 Filter from one of the training data-sets.

4.2.2 Peak Detectors

After filtering through the C4s, the next step for the system is to generate the RMS voltage for an estimation of the power in each band. The first step for RMS estimation is to positively rectify the signal, removing the negative half. To accomplish this, a Peak Detector circuit was used (Fig. 4.8). The Peak Detector on the RAMP has a similar operation to the C4 filters, with two OTAs, $G_{m,A}$ and $G_{m,D}$. $G_{m,A}$ controls the attack rate and $G_{m,D}$ controls the decay rate. The attack rate refers to how quickly the output of the peak detector will follow an increase seen on the input. The decay rate refers to how quickly the output will follow a decrease seen on the input. The attack and decay rates are set using the bias currents for the two OTAs [33]. Also like the C4s, each peak detector performs differently, calling for each circuit to be built on the RAMP and tested separately. An example of the peak detector output can be found in Fig. 4.9.

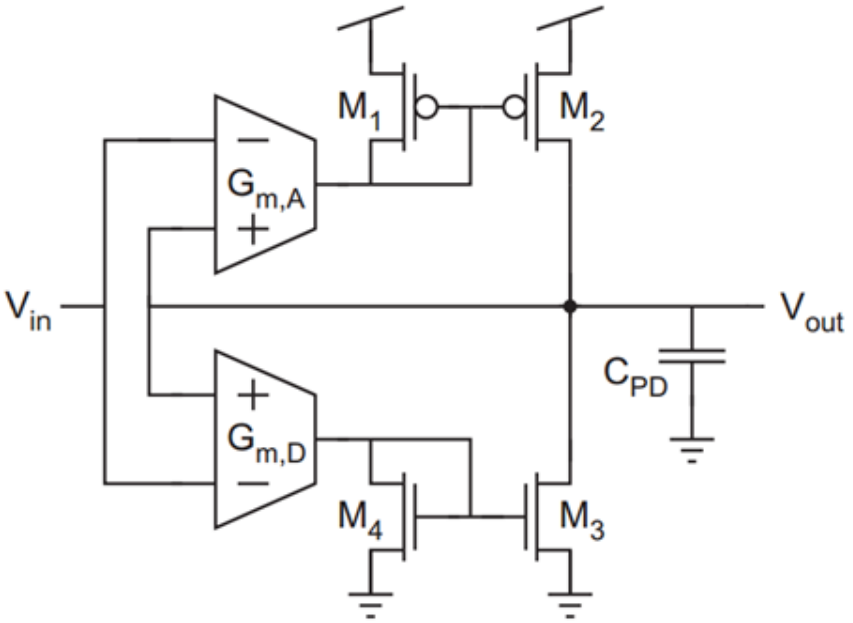

Figure 4.8: Schematic of the Peak Detector.

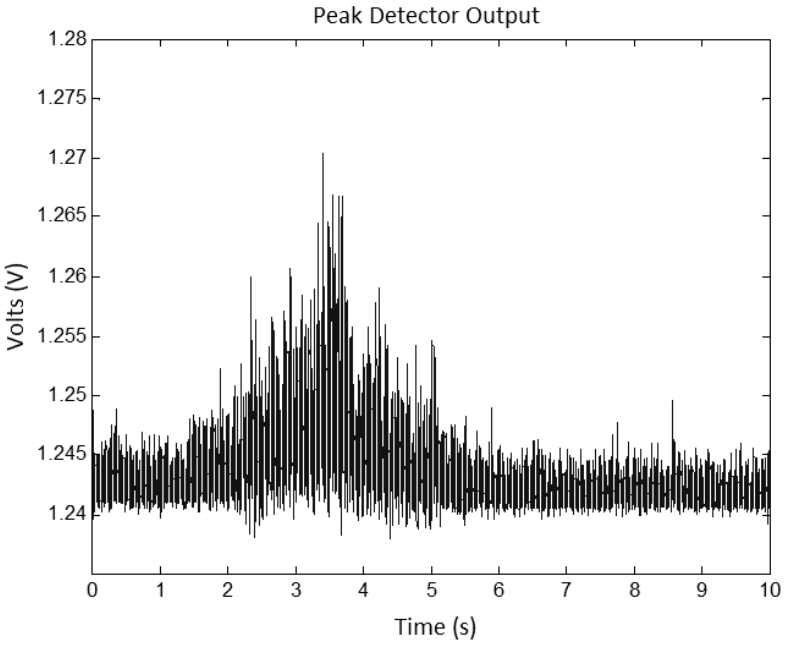

Figure 4.9: Output of the Peak Detector from one of the training data-sets.

To accomplish half-wave rectification, the attack rate (set with the bias current of $G_{m,A}$) needs to be high enough to follow the envelope of the signal. The decay rate (set with the bias current of $G_{m,D}$) is where the distinction is made between half-wave rectification and a full envelope of the signal. The decay rate needs to be high enough to track the signal back towards the analog ground, but low enough that it does not go below ground. The rate also needs to be high enough to ensure that nothing important is lost from the signal. To find an estimation of the decay rate, an average between the bias currents were found that produced both a full envelope and only the local maximums. From this average, a "perturb and observe" method was used to narrow in on the desired value for each of the peak detectors.

4.2.3 Adaptive-Tau Filters

To finish the RMS estimation, the output from the peak detector circuits needs to be passed through a low-pass filter to remove the ripple brought in from the audio signal. For this stage, an Adaptive-Tau, low-pass Filter was used due to availability on the RAMP (Fig. 4.10). This Adaptive-Tau filter has an expansive non-linearity allowing for an amplitude-dependent time constant. For small differential voltages, the filter has a low, linear transconductance, resulting in a long time constant to help with suppressing ripple. For larger differential voltages the time constant decreases, resulting in a better temporal response [33].

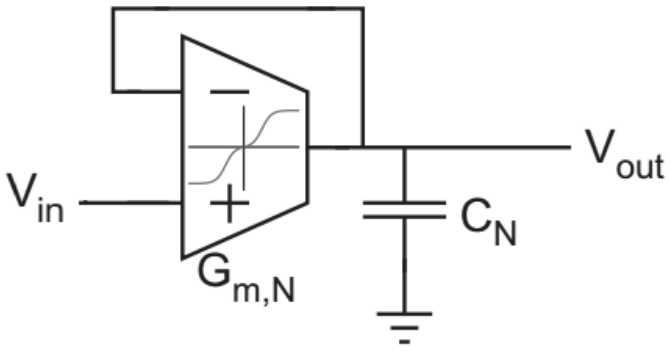

Figure 4.10: Schematic of the Adaptive-Tau Low-pass Filter.

Unlike in the previous stages, the bias current for the OTA $G_{m,N}$ is only needed for

operation and does not need fine tuning for a specific region of operation. However, when the output of the filter is connected to the comparator stage through the CAB lines, the signal experiences more attenuation than if it is sent directly to an output pin. To decrease the effects of this attenuation, a buffer has been added to the end of the filter, ensuring that the RMS estimation is unperturbed for use by the comparator stage. An example output of the buffered Adaptive-Tau Filter (and in essence, the RMS estimation) can be found in Fig. 4.11.

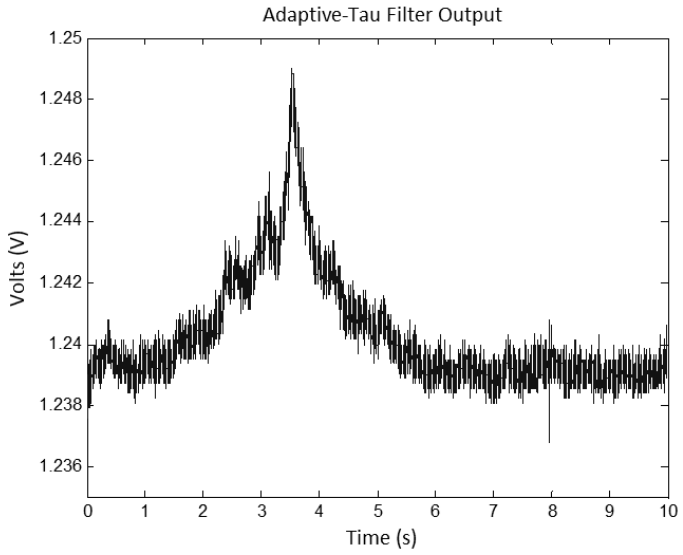

Figure 4.11: Output of the Adaptive-Tau Filter from one of the training data-sets.

4.2.4 Training Algorithm

The output of the RMS estimation is compared to a reference value to generate a digital signal. This reference value is determined via the training algorithm. At this stage of the project, the training algorithm implements a simple procedure to determine the necessary reference voltage. With the full system built onto the RAMP, the twenty training data-sets are passed into the system and read from the buffered output of each of the eight Adaptive-Tau filters. The training data-sets include markers for when a vehicle is actually present. Using these markers, the output of the RMS estimation was cut so that only the period when a vehicle was present was being observed. From this sub-set of data, two averages

were found for each of the eight bands; one from the car training set and one from the truck training set. These two averages give a general estimation of the power in each band when a car or truck is present. A median was determined for each band between the two averages and used as the reference value for the comparator in each band. Since this reference value is below the average for a truck, it will always trip the comparator when a truck is present, and being above the average for a car, it will only periodically trip the comparator when a car is present.

This distinction between when a car or truck is present allows for digital codewords to be developed for each case. After setting the reference values, the output from each comparator was documented. The output of the eight comparators comprise an eight bit codeword for use by the lookup-tables. Using the markers for the audio signals, every codeword was observed from each of the eight comparators while a vehicle was present. Two codewords were chosen for both a car and a truck based on the two most commonly observed codewords while each was present. The two codewords will be used by the lookup-tables to generate a detection and classifier output.

4.2.5 Digital Decision Making

The RMS estimation is used by the comparators to generate a digital signal for each of the eight sub-bands. The positive terminal of each comparator is connected to the buffered output of one Adaptive-Tau filter. The reference value for each comparator determined by the training algorithm is generated with a current source and resistor. The current source generates from a floating-gate transistor and connects to the resistor and comparator at a central node. The bottom of the resistor is connected to mid-rail and its combination with the current source allows for a reference voltage to be generated. The current source can be finely tuned by the floating-gate to set the reference voltage at the desired value.

The eight comparator outputs generate the codeword to be used by the lookup-table. However, the lookup-table only has six input pins. To catch all eight bits of the codeword, three lookup-tables are required. The lower four bits are input into one lookup-table and the upper four bits are input into a second table. The outputs of the first two lookup-tables

are then input into to a third and final table for combination. The lookup-tables are set up using digital logic directly in their netlists. When MATLAB parses the netlists to build the connection file required for use by the RAMP, it uses the digital logic to set the individual connections in the programmable logic section of the digital RAMP CABs. When either of the two codewords associated with a car is present, the detection pin (pin 1) of the lookup-table goes high. When either of the two codewords associated with a truck is present, the classification pin (pin 2) of the lookup-table goes high.

The final step in the decision making process is done using the PanStamp mote connected to the RAMP PCB. The mote receives two inputs from the final lookup-table. To decrease system power consumption, the mote stays in a low-power mode until it receives a high input from either of the lookup-table pins. Once a high has been read, the mote listens to the two outputs for a period of four seconds. While it is listening to these pins, it adds their output together and computes a moving average of the combination. After completing its calculation, it makes a final decision based on the end result of the moving average. Considering the digital values from the lookup-tables are based on the rails of the RAMP, a high value corresponds to 2.5V, and the combination of the two pins could result in a maximum of 5V. If the final moving average is above 2.5V, the mote determines that a truck is present. If the final moving average is above 0.3V but below 2.5V, the mote determines that a car is present.

4.2.6 Results

Utilizing the PanStamp wireless mote for making the final decision of vehicle detection and classification reduces the risk of a false positive, but also increases the latency of the response. Since the mote must listen for four seconds before making a decision, a delay is introduced that would not be present if the lookup-tables were used to trigger a decision. However, given the frequency of observing the correct codewords, even outside of vehicle presence, the increased latency is acceptable to improve system performance.

After training the setup using the initial data-set, the performance of the system was analyzed using the testing data-set. The testing data-set matches the structure of the training

data-set (ten cars/ten trucks), but is made up of entirely different samples. The system accurately detected 18/20 vehicles (90% success rate) and classified 14/20 vehicles (70% success rate). Fig. 4.12 shows a graphical representation of the ideal system performance (A) and the actual system performance (B).

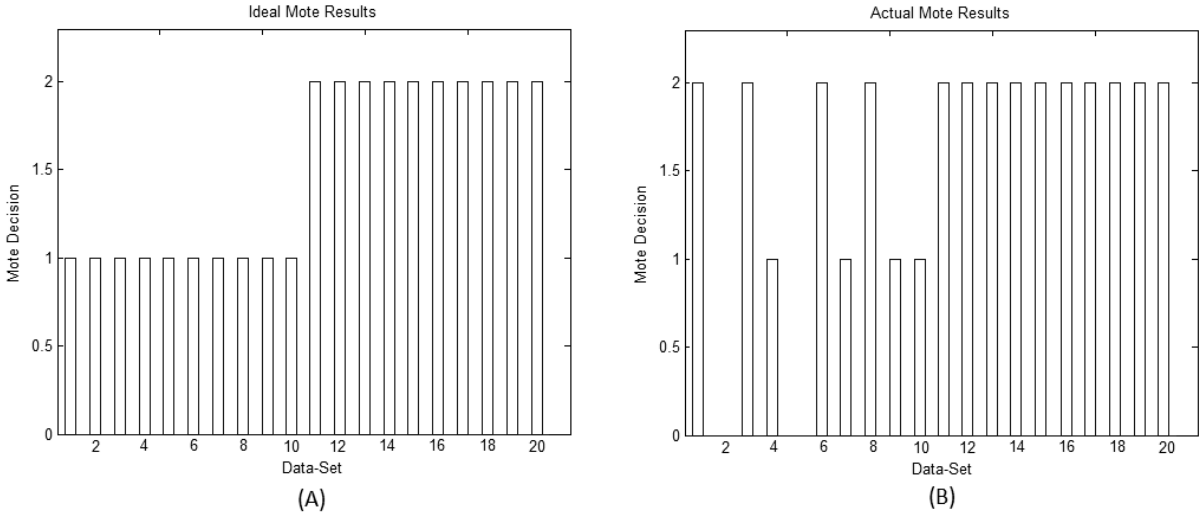

Figure 4.12: (A) Ideal response, showing PanStamp decision for all 20 cases (0=no vehicle detected, 1=car, 2=truck). (B) Actual response of system from testing data-set. Showing PanStamp deicison for all 20 cases (0=no vehicle detected, 1=car, 2=truck).

The PanStamp mote outputs a value of "1" if a car is dected and a value of "2" if a truck is detected. Due to the larger signal amplitude of trucks, the system was able to correctly detect and classify 10/10 trucks. The system incorrectly classified four of the cars as trucks, and missed two of the cars completely. Additional work with the training algorithm will strive to increase these values to 100% detection with 100% correct classifcation.

4.3 Additions to the FPAA

For the second iteration of the RAMP FPAA, improvements were made to its peripheral systems, such as the integrated charge pumps and high-side switches, but there were also changes made to the CABs, including an extra stage, as well as modifications to previous stages. The first iteration of the RAMP included eight analog stages and two digital stages (with eight repeating channels in each stage). The second iteration added a ninth analog

stage as well as increasing the size of the spectral analysis analog stage. The ninth stage added did not follow the convention of the preexisting CABs. Instead of the stage having eight repeating channels, each of the channels included a different circuit, hence the naming convention of "Unique CAB." The enlargement of the spectral analysis stage allowed for the C4 Bandpass filters to be replaced with Biquad filters.

4.3.1 Biquad Filter

On the second iteration of the RAMP, the Biquad filter was an upgrade and replacement to the C4 Bandpass filter [34]. The C4 filter operated as a bandpass filter, but was able to change operation based on the two bias currents, setting the corner frequencies. If the lower corner frequency was set low enough, the C4 could perform similarly to a low-pass filter. Similarly, if the upper corner frequency was set high enough, the C4 could perform similarly to a low-pass filter. The problem with the C4 is that it requires very accurate capacitor matching to achieve uniform gain for similar quality factors. Utilizing the Biquad makes this process easier.

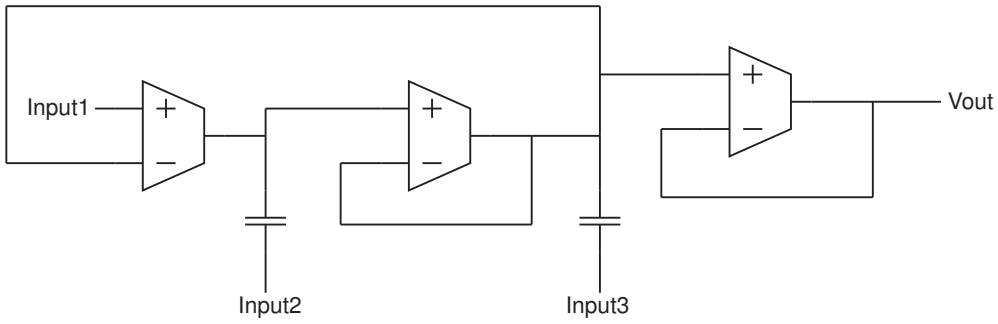

Figure 4.13: Schematic of Biquad Filter.

To fix this issue, the C4 was replaced with the Biquad filter (Fig. 4.13). The Biquad filter operation is based on more than just one input. There are three points for input into the circuit. By choosing a specific input, and setting the other two inputs to analog ground, the biquad is able to operate as either a low-pass, high-pass, or bandpass filter. With each of the three inputs connected to the CAB lines, when the circuit is connected on the RAMP, it is forced into a specific region of operation, only allowing for the desired performance. Two

versions of the Biquad filter have been added to the design, with differences in the size of capacitors used. The first version, utilizing a smaller set of capacitors was used to replace the C4 filters in the spectral analysis stage. The second version, using a larger set of capacitors was added in one of the Unique CABs.

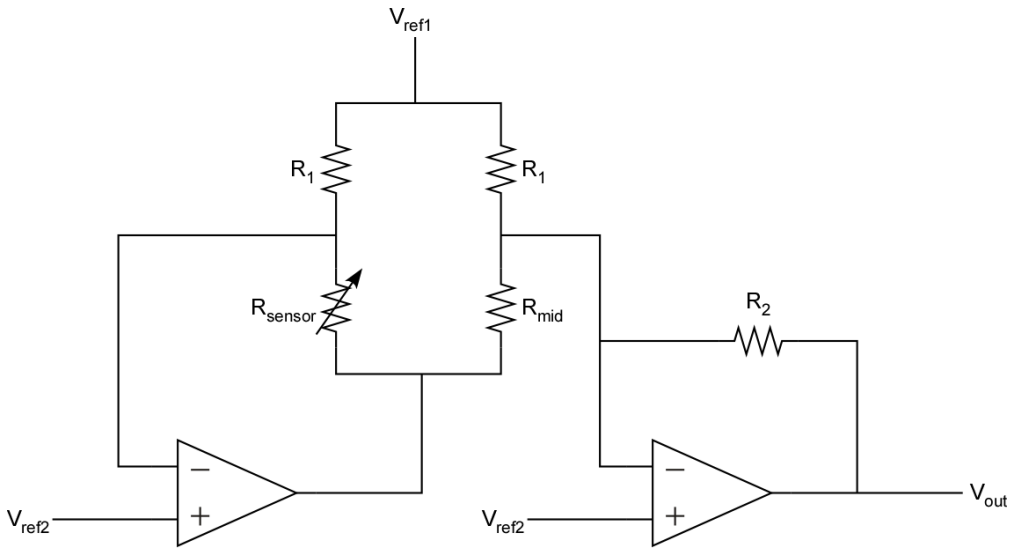

Figure 4.14: Schematic of Wheatstone Bridge.

4.3.2 Wheatstone Bridge

To increase the sensor interfacing capabilities of the RAMP there needed to be additions to the circuits included in the CABs. While the Wheatstone Bridge circuit used in the IC from chapter three could be synthesized from the existing components on the RAMP, the circuit itself would have to be connected via the CAB lines, adding additional parasitic capacitances and resistances to its operation. While parasitics can never be fully avoided, allowing the circuit to be connected fully within one CAB would decrease such negative effects. Due to this consideration, one of the circuits added to the Unique CAB was a pre-built Wheatstone Bridge with its two inputs connected directly to the pads on the IC, for minimizing parasitics. The Schematic for the Wheatstone bridge used in the Unique CAB as well as the custom IC from chapter three is shown in Fig. 4.14.

4.3.3 Oscillators

To increase the range of applications available to the RAMP, two different clock generators were added with the inclusion of the Unique CAB. A Ring Oscillator was added to perform fifty percent duty cycles and an Integrate and Fire Neuron was added for a variable pulse period generator. Due to their inclusion in the Unique CAB, only one instance of each circuit was added to the new design.

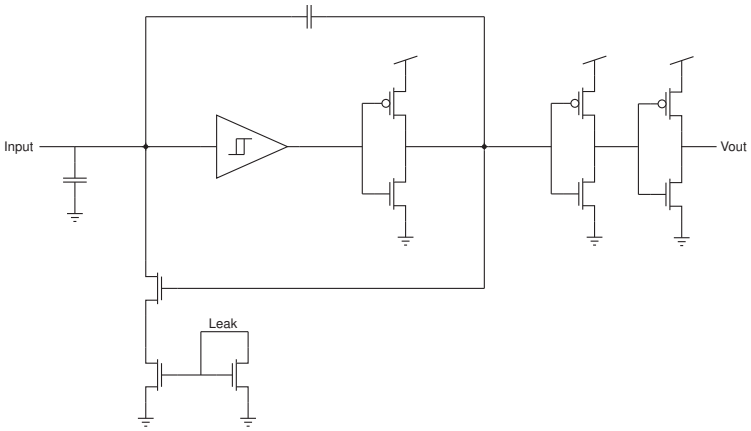

Figure 4.15: Schematic of Integrate and Fire Neuron.

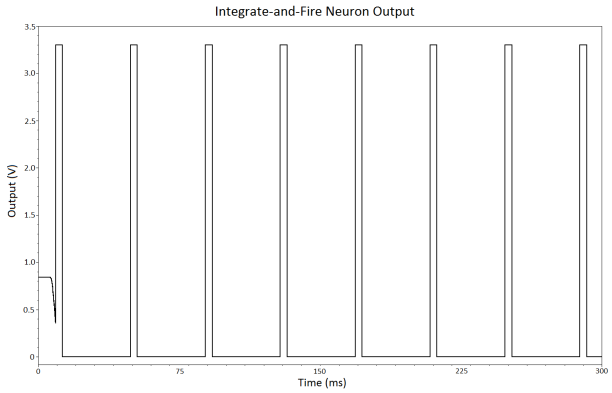

Figure 4.16: Simulated Output of Integrate-and-Fire Neuron.

A current-starved design was used for the Ring Oscillator (RO) added to the Unique CAB [35]. This circuit was added as a preliminary step for including an energy harvesting system directly on the FPAA. The design used for the RO is the same as the one detailed in chapter five and can be found in Fig. 5.5. A current-starved RO allows for a wide range

of frequency outputs based on the current limitations input to the inverters. Normally, a Ring Oscillator is operated with a voltage control. The RO added to the Unique CAB was designed with built in current mirrors to set up the voltages needed by the inverters [36]. This design allows it to be controlled by the floating-gate transistors with ease, as they generate a current for use by the CAB elements.

An Integrate-and-Fire Neuron was the second clock generator added to the Unique CAB [37] (Fig. 4.15). This circuit mimics the behavior of a neuron from the human brain. To begin firing, a current is dumped on to the input pin in a manner similar to how a neuron is contacted within the brain. A leakage current is used to control the pulse width of the clock cycle and will be generated from the floating-gate transistors. A Schmitt trigger is utilized to set up hysteresis within the neuron, allowing for a duty cycle controlled by the leakage current [38]. A simulated output of the neuron is shown in Fig. 4.16.

4.4 Chapter Summary

This chapter covered the use of a reconfigurable integrated circuit for custom sensor interfacing. A new PCB design was detailed that increases FPAA performance as well as includes all peripherals needed for interfacing with a computer for programming. The Acoustic Vehicle Classification project originally described in the Hibernets paper was recreated fully on the RAMP, and while results still need improvement, the scope of RAMP applications has been increased. From the prototype custom integrated circuit in chapter three, additional circuits were added to the newest version of the FPAA to increase its ability as a sensor interfacing device.

Chapter 5

Energy Harvesting

5.1 Energy Harvesting with COTS devices

A prototype energy harvesting (EH) system was designed utilizing commercial-off-the shelf (COTS) devices. The design was built and tested to verify operation utilizing input from a thermoelectric generator. The system was then verified by powering a TelosB wireless sensor during periodic radio transmissions. A schematic of the system is shown in Fig. 5.1.

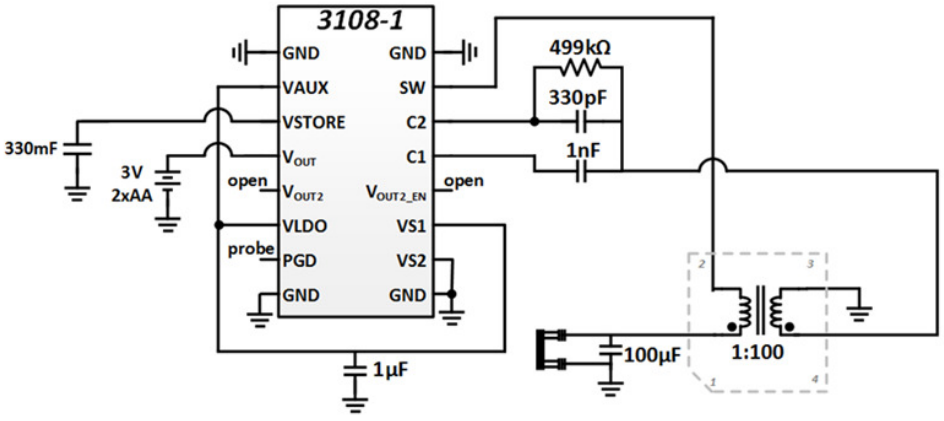

Figure 5.1: Schematic of COTS Energy Harvesting System.

The system was designed to operate with a Thermoelectric Generator (TEG) with an output of 1V at 75°C. The LTC3108-1 was used as the power converter and control unit. The power converter implemented by the LTC3108-1 is a boost converter requiring an ex-

ternal transformer used to step up in the input voltage. A Maximum Power Point tracking system is implemented by the LTC3108-1 to ensure the energy from the TEG is utilized at peak efficiency. A 330mF super capacitor was used as the storage buffer and Design-Time component Matching was used to output the desired voltage for the TelosB wireless mote.

To test the system, the TEG was used to power the storage buffer for five minutes while the TelosB was in a sleep state. Once the system was charged up, the TelosB woke from its sleep state and transmitted a package over the radio for five seconds. Once the radio transmission had ended, the TelosB returned to its sleep state, waiting sixty seconds before repeating a five second transmission. The harvested energy was able to fully power the TelosB for the full duration of an hour long test. Fig. 5.2 shows the voltage levels for the storage buffer and regulated output voltage used by the TelosB wireless mote. Given enough time, the voltage stored on the super capacitor may have dropped low enough to end regulation on the system output, causing the TelosB to lose power. With a custom IC solution, a wireless sensor mote would be able to operate fully on harvested power with reasonable transmission rates.

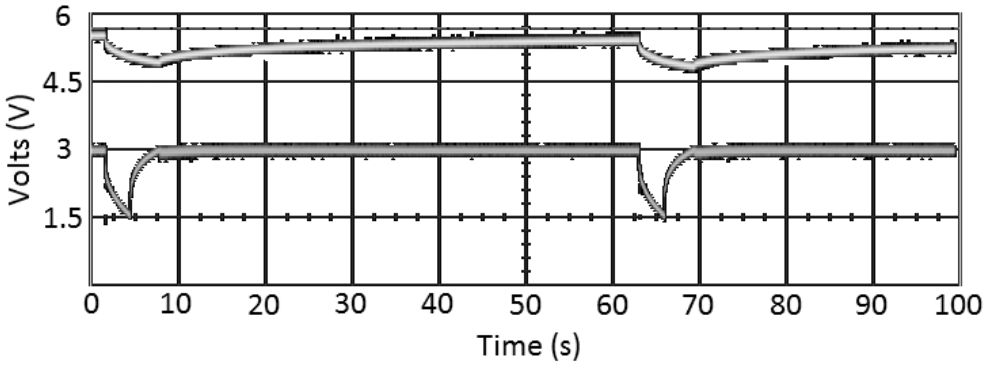

Figure 5.2: WSN test of COTS Energy Harvesting System. The top line corresponds to the voltage in the storage buffer. The bottom line corresponds to the voltage being used by the TelosB wireless mote. Periodic decreases in voltage correspond to radio transmission.

5.2 Energy Harvesting with an IC

An integrated circuit has been designed that will continue and build upon the knowledge gained from the prototype energy harvesting system. This IC is the first step towards

integrated an EH system onto the FPAA. The following stages are used in the system: Energy Transducer - a thermoelectric generator will be used to convert excess heat to a voltage that will be used as an input and supply to the EH system, Power Converter - a Charge Pump DC-to-DC converter will be utilized to step up the input voltage to a higher value for storage, Control Unit - A Maximum Power Point Tracking system will be used to ensure the output of the thermoelectric generator is utilized at peak efficiency by the charge pump, Storage Buffer - a super capacitor will be used to store the energy for later use, Application Unit - a Design-Time Component Matching scheme will be used to connect the storage buffer directly to a wireless mote.

The Power converter stage of the EH system steps up the voltage input from the thermoelectric generator to a value more suitable to the desired application. The Charge Pump used in this stage was designed to operate from a shared input and supply voltage as low as 100mV. As long as the input/supply voltage is between 100mV and 1.5V, the circuit will step up the voltage by about 400%. Most charge pumps require a non-overlapping clock generator to operate. The charge pump used in this design makes use of three charging stages and only requires one clock signal for operation. Fig. 5.3 shows a singular charge transfer switch. This switch is repeated five times in series to generate the correct output voltage. The clock signal is generated by a Ring Oscillator. The Control Unit consists of the feedback from the output of the charge pump back to the biasing of the Ring Oscillator.

The output of the Charge Pump is sent to the non-inverting input of an Operational Transconductance Amplifier (OTA). This OTA converts the voltage from the charge pump into a current that is used as the bias for the Ring Oscillator. As the charge pump increases in voltage, the OTA output current will increase, causing the Ring Oscillator to increase in output frequency. This will in turn, increase the output of the charge pump. This cycle will continue until the system reaches a steady-state. The current design has the system reaching a steady state at approximately a 400% increase from the input voltage. This cycle is responsible for the Maximum Power Point control unit operation. A block diagram of the control unit can be found in Fig. 5.4.

A Ring Oscillator (RO) makes use of an odd number of inverters to force oscillation in a closed loop. The RO used in this design takes advantage of current starved inverters

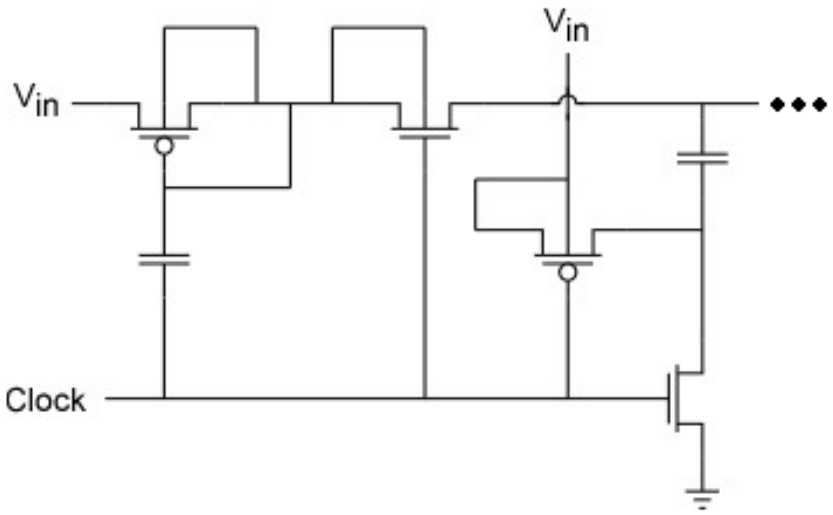

Figure 5.3: Circuit Schematic of Single-Clock Charge Pump Charge Transfer Switch.

to ensure that the energy being harvested is not wasted on powering the oscillator. The starved inverters stop a current dump from occurring between the supply and ground every time there is an inversion. By placing the Ibn and Ibp transistors above the inverter, it is ensured that only a desired amount of current will be flowing through the inverters at any time. This RO also utilizes a start-up circuit, ensuring that it will only start oscillation once the enable pin is connected to the thermoelectric generator. Fig. 5.5 shows a schematic of the current-starved ring oscillator.

The OTA takes the voltage output from the charge pump and converts it to a current for biasing the Ring Oscillator. The connection between the output of the Charge Pump and the frequency of the RO allows for the Maximum Power Point control unit operation. As the output of the Charge Pump increases, the voltage input of the OTA increases proportionally. With an increase to the input voltage, the OTA produces a larger output current. Since the output current is connected to the starved inverters in the ring oscillator, this increase in current allows for the RO to oscillate at a higher frequency. This process will continue until the Charge Pump has reach a maximum operating level. The OTA was designed to keep power consumption low to ensure efficient energy harvesting. While the OTA is generating the bias for the oscillator, the OTA itself requires a bias. Fig. 5.6 shows the chosen OTA design. Since this bias will remain constant, a static current reference was used.

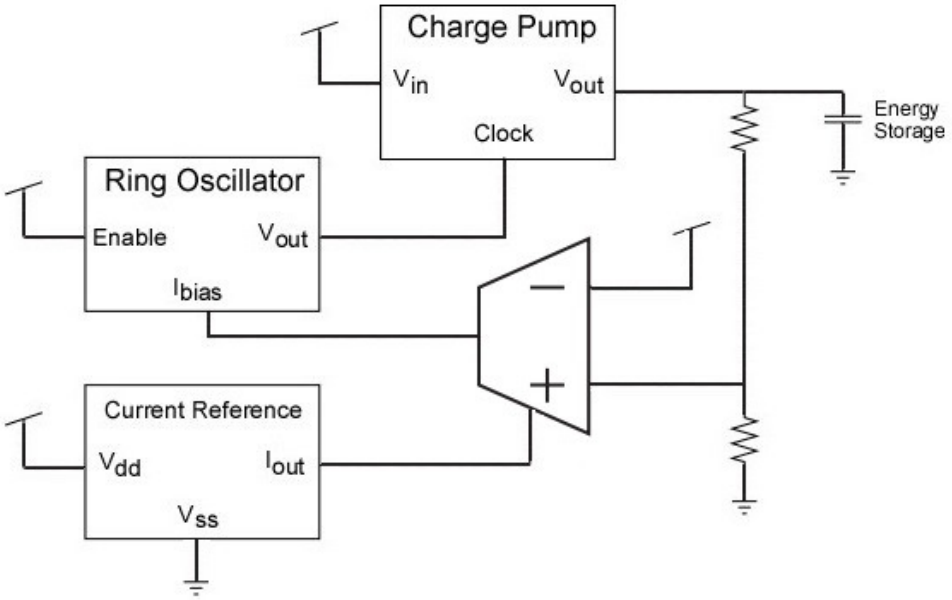

Figure 5.4: Block Diagram of the closed-loop control unit.

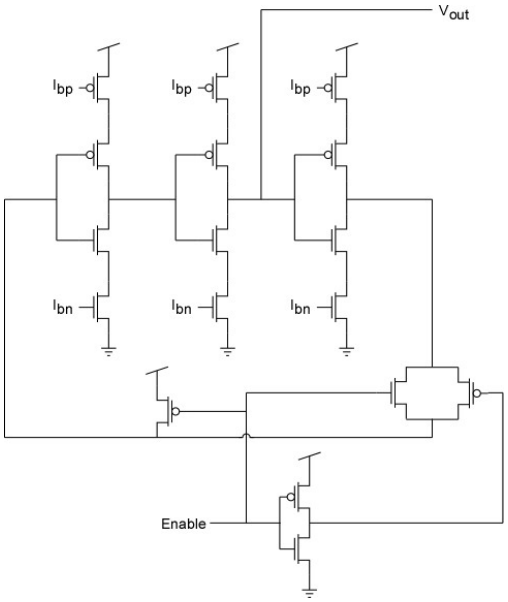

Figure 5.5: Schematic of Ring-Oscillator Clock Generator.

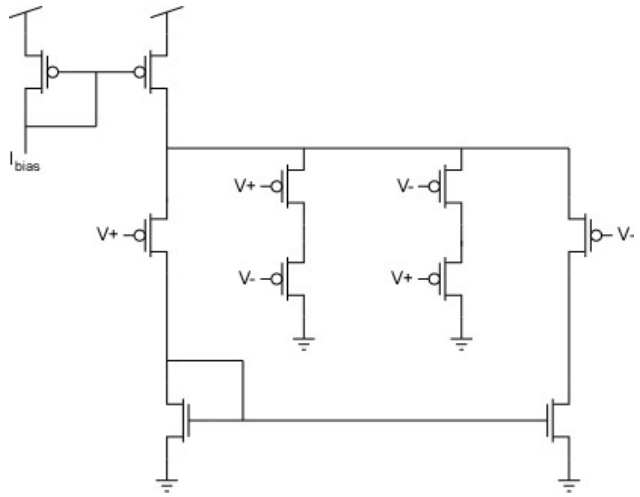

Figure 5.6: Schematic of Operational Transconductance Amplifier (OTA).

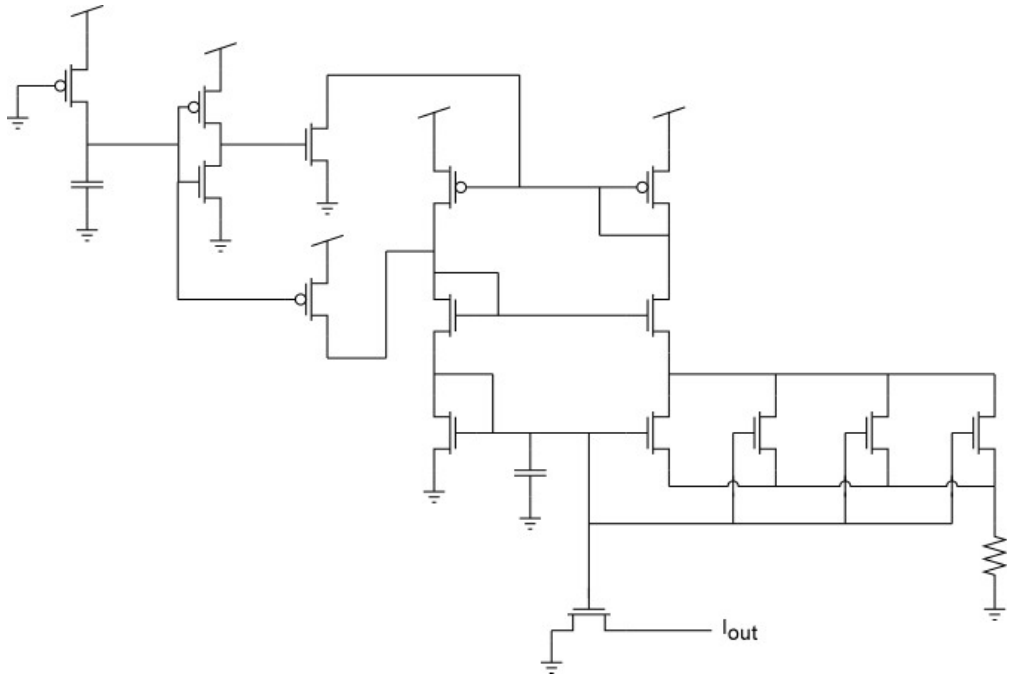

Figure 5.7: Schematic of Temperature Independent Current Reference.

The Current Reference (Fig. 5.7) generates a bias for the OTA. Since the OTA requires a constant bias, a stable current source was chosen. This current source is temperature independent and its bias is set by the size of a resistor [39]. This resistor could be included on the integrated circuit, or left off-chip to be modified at a later date. The current mirror required by the OTA to utilize the current generated by this source has been built into the OTA design.

5.3 Chapter Summary

This chapter covered two methods for designing an Energy Harvesting system. Section 5.1 detailed the use of commercial-off-the-shelf components to build a system that scavenges excess heat for conversion to electrical energy. The COTS system was then used in a test to power a TelosB wireless mote during a periodic radio transmission. This prototype system was used as a stepping stone to begin development on a custom integrated solution in Section 5.2. The custom IC improves upon the COTS design and is the first step for integrating an Energy Harvesting system on the Field Programmable Analog Array.

Chapter 6

Summary and Conclusions

This work has attempted to improve upon the sensor interfacing, signal processing, and energy harvesting capabilities of the Field Programmable Analog Array. The integrated circuit described in chapter three was a good prototype system for improving interfacing on the reconfigurable FPAA. By testing circuits on a custom IC in between FPAA design cycles, these systems were added to the FPAA without as much worry for their projected operation.

Sensor interfacing is a very broad subject, and subsequently it is very difficult to cover every possible scenario with a reconfigurable IC. By iterating on different interfacing applications, improvements to the FPAA have been made to bring it closer to an all inclusive system. However, more experience with countless other scenarios is needed before the FPAA will be able to be used as an all-purpose sensor interface.

The Acoustic Vehicle Classification project successfully detected 90% of the vehicles from the audio data. Unfortunately, it only classified 78% of these vehicles correctly (70% of all vehicles). The focus of this thesis was the characterization, setup, and fine-tuning of the hardware used as a front-end signal processor for this application. Future research will focus on a more comprehensive training algorithm that interacts directly with the hardware. By integrating the training algorithm with the circuit synthesis process on the FPAA, more advanced algorithms will be explored that make changes to the hardware specifications to look for improvements in the final results.

The energy harvesting COTS prototype was a first step in realizing such a system on

the FPAA. The designs for the integrated system will continue to be improved upon before fabrication during the next FPAA design cycle. While implementing this system on the FPAA is the next goal, a reconfigurable energy harvesting system is the true goal for this research. An energy harvesting system based on the capabilities and structure of the FPAA would make this field more accessible to engineers, especially those without analog IC design experience.

Chapter 7

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