

2001

CMOS fingerprint sensor electrostatic modeling

Praveen Kumar Soora
West Virginia University

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CMOS Fingerprint Sensor Electrostatic Modeling

Praveen K. Soora

**Thesis submitted to the
College of Engineering and Mineral Resources
at West Virginia University
in partial fulfillment of the requirements
for the degree of**

**Master of Science
in
Electrical Engineering**

**Lawrence A. Hornak Ph.D., Chair
Biswajit A. Das Ph.D.
Stephanie C. Schuckers Ph.D.**

Department of Computer Science and Electrical Engineering

**Morgantown, West Virginia
2000**

**Keywords: Biometrics, Fingerprint, CMOS Sensor, Parasitic Capacitance
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ABSTRACT

CMOS Fingerprint Sensor Electrostatic Modeling

Praveen Soora

The use of Biometrics in personal identification is an important emerging technology in modern electronic society. Fingerprints are one of the most popular biometric technologies, currently used in majority of biometric applications. In recent years, solid-state capacitive fingerprint sensors which image fingerprints using Silicon CMOS Technology are gaining much acceptance in the market. This research work is carried out to quantify and explore approaches for achieving improved sensitivity of the capacitive imaging process through reduction of parasitic capacitances and sensor cell scaling for future generation devices. Evaluation of sensor cell and array geometries was completed using a commercial 2-D electrostatic field solver. The modeling activities performed include analysis of sensor cell and sensor plate size, their relationships, evaluation of ESD ring coupling, and exploration of cell and array layout approaches for achieving reduced parasitic capacitance.

Sponsoring Agency: Veridicom Inc., Santa Clara, CA.

Committee:

Dr. Lawrence Hornak, Chair

Dr. Biswajit Das

Dr. Stephanie Schuckers

ACKNOWLEDGEMENT

I would like to express my sincere gratitude and thanks to my advisor Dr. Lawrence Hornak for providing valuable advice, guidance and encouragement throughout this research work. As my committee chairman his patience, suggestions and reviews certainly made the completion of this thesis possible. I was fortunate to have him as my advisor and as a teacher in the classroom.

I would like to extend my thanks to my committee members Dr. Biswajit Das and Dr. Stephanie Schuckers for their generous time and kind co-operation.

The encouragement and assistance of fellow research students in my lab is greatly appreciated. My heartfelt thanks to my friends for their constant support and encouragement.

Financial support for this research was provided by Veridicom Inc., Santa Clara, CA. Their support is very much appreciated.

Last but not least, my special thanks to my parents without whose love and blessings none of this would have been possible. I would also like to thank my brother Ravi for his encouragement throughout my education. Finally, I wish to thank my sisters for their love and support.

Dedication

This research work is dedicated to my father the best teacher in my life. Though he passed away 10 years back, I always feel he is still with our family and supports me whenever I need him.

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Chapter 1

Introduction

1.1 Biometrics

The automated measurement and identification of biological and behavioral characteristics of an individual is called biometrics [1]. If a human physiological or behavioral characteristic has the following properties, universality: which means that every person should have the characteristic, uniqueness: which means that no two persons should be the same in terms of the characteristic, permanence: which indicates that characteristic should be invariant with time, and collectability: which indicates that characteristic can be measured quantitatively then it could be used as a biometric[1]. As this technology becomes more economically viable, technically mature and the public becomes aware of the applications and strengths, the field of biometrics will play a crucial role in identification technology and the shaping of privacy policies.

1.1.1 Personal Identification Systems

Automated biometric personal identification systems represent a new and emerging technology. Initially, biometric technologies were considered to be highly technical, high cost systems, and can only be used in forensic and military applications, but with the availability of inexpensive embedded computing, cheaper sensing technologies, and increasing demand for identification, biometrics have emerged as mainstream[1].

The architecture of an automated identity authentication system is shown in Fig 1.1. It has four components: biometric reader or sensor, system knowledge, enrollment module and authentication module. During enrollment, one of the biometric measurements are captured by the biometric interface and required information is taken by feature extractor and stored in a database. In authentication mode, the person to be authenticated indicates his identity. Next, the system reads the relevant biometric

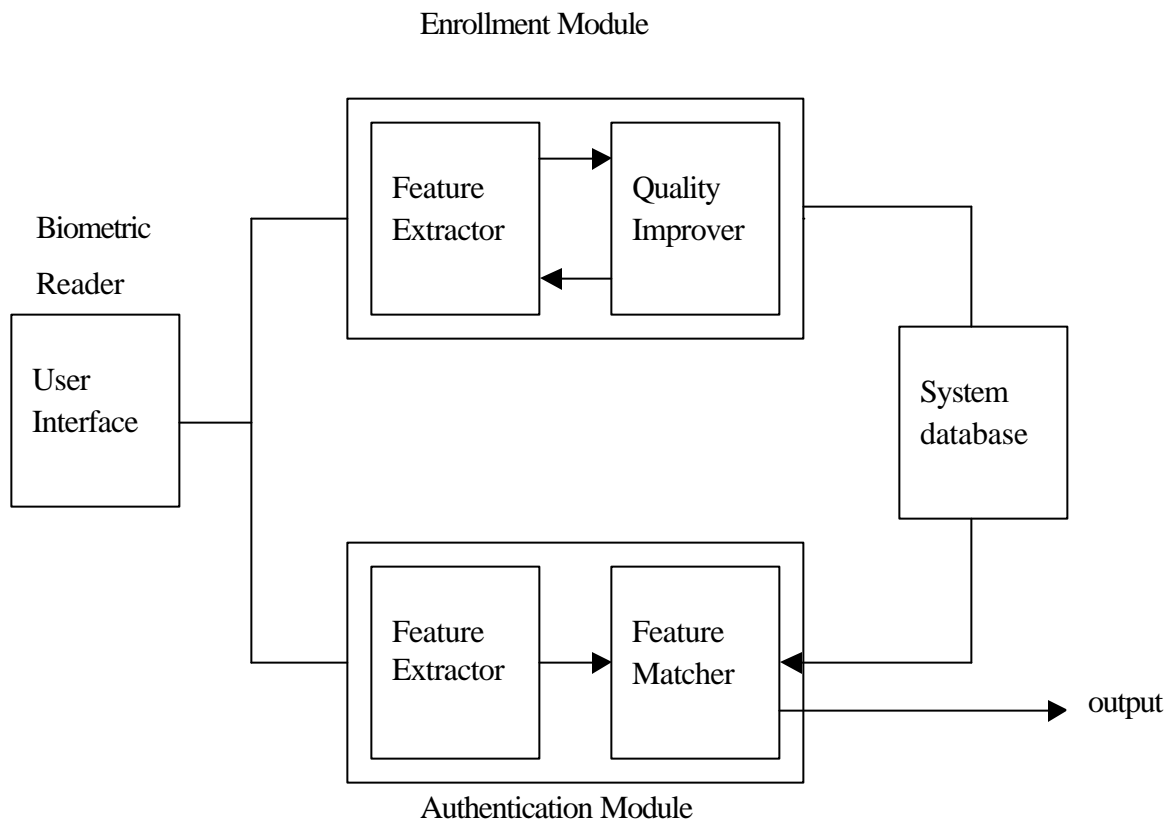


Fig 1.1 Architecture of typical Biometric Identification System[6]

measurements, extracts features and compares with that of the information stored in the database. Lastly, the system then decides the subject is valid or invalid [6] [1].

There are two types of matching that an authentication module performs: one-to-one matching which confirms the subject validity directly, and one-to-many matching which searches whole database and then decides the validity. In other words, if a system is asked to determine the identity of a person who presents himself to the system, the system compares particular biometric feature with the enrolled features. This type of matching is called one-to-many matching. If a person supplies his identity to the system usually by presenting a machine readable identification card and the system is asked to confirm that the person is who he says he is, this type of matching is called one-to-one matching.

1.1.2 Biometric Technologies

As with any technology, all the biometric technologies have their own strengths and limitations. Though there are a number of biometric technologies, each appeals to a particular identification application.

The following are the few biometric technologies that are currently commercially available[1].

- ***Voice:*** Voice print is acceptable in almost all societies and voice capture is unobtrusive. To identify a person over the telephone, voice may be the only feasible biometric as most of the other technologies require the individual to be present at the identification system. Though it has the properties of universality and collectability, it lacks permanence and uniqueness properties as it is a behavioral characteristic and is affected by person's health, emotions etc.
- ***Infrared facial and hand vein thermograms:*** The human body radiates heat and an infrared sensor device could capture an image indicating different levels of heat. Infrared facial thermograms are acceptable since their acquisition is non-contact and has a non-invasive sensing technique. A related technology is to scan the back of a clenched fist to determine the hand vein structure.
- ***Fingerprints:*** Fingerprints are one of the most popular and oldest biometric technologies used historically in forensic applications for criminal investigations. These are formed on human fingers depending on the initial conditions of embryonic development and therefore they are believed to be unique to each person and it also is permanent, universal and collectable.
- ***Face:*** Face is considered among the most natural biometrics because this can be used in visual interactions. It is very challenging to develop face recognition techniques because of the effects such as aging, facial expressions, slight

variations in the imaging environment and variations in the pose while taking the image.

- ***Iris:*** Visual texture of the human iris is considered to be unique for each person and each eye. An iris image is usually captured using a non-contact imaging process.
- ***Ear:*** The shape of the ear and the structure of the cartilaginous tissue on the pinna are distinctive, but not unique to each individual. No commercial systems are available yet in this field.
- ***Gait:*** Gait is the peculiar way one walks and not supposed to be unique for each individual. This is a behavioral biometric and can be used in identity authentication.
- ***Keystroke Dynamics:*** This is a behavioral biometric based on the fact that each person types on a keyboard in a distinct way. It is not unique to each individual but offers sufficient information to be used in some identification applications. Some commercial systems are available in the market in this field.
- ***DNA:*** Deoxyribo Nucleic Acid is the ultimate unique code for each individual except for the fact that identical twins have the identical DNA patterns. It is currently used mostly in forensic applications after fingerprint images for identification because of its high recognition rate. Identification systems involving this technology currently are not fully automated on the time scales necessary for rapid identification.
- ***Signature:*** The signature of a person is known to be a characteristic of that individual. It is widely acceptable in many government, commercial and legal transactions as a method of personal identification. Signatures are a behavioral biometrics, which depends on physical and emotional conditions of the persons.

- ***Retinal Scan:*** The retinal vasculature structure is supposed to be a characteristic of each individual and each eye. It is the most secure biometrics with the qualities of universality, uniqueness, permanence and collectability. The image capture method necessitates cooperation of the subject, entails contact with the eye piece and requires efforts of the user.
- ***Hand and Finger Geometry:*** Another method of identification is hand geometry, which has captured half of the physical access control market [1]. Finger geometry is related to hand geometry and is a new technology which relies only on geometrical invariants of index and middle fingers. Though this is more accurate than hand geometry, its technology is not as matured as that of hand geometry.

1.1.3 Applications

It is expected that in the coming years, the rising number of applications may increase the demand for the biometric identification systems. Some of the applications where biometric technology is already in use or would evolve and be used include:

- Transactions via e-commerce
- Search of digital libraries
- Computer Logins
- Access to internet and local networks
- Document encryption
- Credit cards and ATM cards
- Access to office buildings and homes
- Protecting personal property
- Tracking and storing time and attendance
- Law enforcement and prison management
- Automated medical diagnostics
- Access to medical and official records.

1.2 State of the art in Biometric finger print model

The use of fingerprints as a biometric is the oldest mode of personal identification and also is the most prevalent in use today [9]. However, this technology still is largely limited to law enforcement applications. It is expected that a recent combination of factors such as small and inexpensive fingerprint capture devices, fast computing hardware, recognition rate and speed to meet the rising needs of many applications, and the rapid growth of network and Internet transactions will favor the use of fingerprints as personal identification for the much larger market segment [9].

Currently much research is going on in this area, and the fingerprint technology is becoming very popular in biometric identification systems. This is the main reason behind the selection of fingerprint technology as a primary topic for this research work. Though there are few small sized solid state capturing devices available, they still suffer from low sensitivity, low robustness etc. This research work is concentrated on enhancing the sensitivity of fingerprint capturing device.

The following sections review the state of the art in biometric fingerprint models and future advances in this field, which includes a brief introduction about fingerprint image and the principle of fingerprint identification system.

1.2.1 Finger Print and its Verification

Fingerprints are graphical flow-like images present on human fingers. The lines that appear are called 'ridges' and the spaces between ridges are called 'valleys'. Fingerprint matching is done by comparing features on these ridges of one fingerprint with that of another.

The two most important structures on a fingerprint image which are used for matching are a ridge ending and ridge bifurcation as shown in Fig 1.2. An ending is a feature where a ridge terminates and a bifurcation is a feature where a ridge splits into

two paths. Both the structures collectively are called minutiae, shown in figure 1.3, which is attributed with features like type which says whether it is an ending or bifurcation, location of the structure determined by (x,y) coordinates, and direction in which the ending and bifurcation appears. These attributes are represented by binary values which combined together called minutiae template which is actually stored for matching purposes. There are other features of the fingerprint that are used in matching. For more information please refer to[9].

Fingerprint matching is done by two methods, *verification* which is based on one-to-one matching or one-to-few matching and *identification* which is based on one-to-many matching.

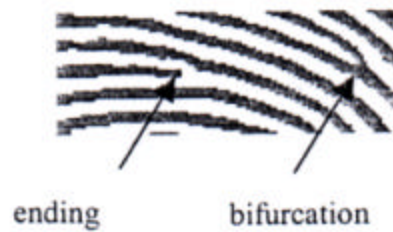


Fig 1.2 Finger print which shows ending and bifurcation[9]



1.3 (a) minutiae

1.3(b) minutiae graph

Fig 1.3 Extracting features of Finger print minutiae[9]

Verification or one-to-one matching is done by comparing the claimant fingerprint against the enrollee fingerprint to decide the validity of the fingerprint. For this, initially a person enrolls his fingerprint into the system database which is stored in compressed format along with the person's other identity such as his name [9]. For example, to access his account at an ATM, the person would still have to present his card on which his name appears and then he would press his finger against a fingerprint sensor such that the identity can be verified. Verification based on one-to-few matching is done similarly but the person may not need to present his identity as this type of matching is done in a system where access is restricted to few users from which the system can easily determine whether the presented fingerprint matched with one of the fingerprints in the database. Most of the biometric verification systems use one-to-one or one-to-few matching for faster service which would be on the order of a few seconds.

Identification or one-to-many matching is significantly different from one-to-one matching in that it requires comparing the presented fingerprint against a database of many fingerprints. This is the typical fingerprint searching that law enforcement authorities use with the aid of automatic fingerprint-identification systems[3].

1.2.2 Principle of fingerprint authentication system

An automatic fingerprint identity authentication system consists of four main components, viz; acquisition, representation, feature extraction and matching[6].

Acquisition: There are two primary methods of capturing a fingerprint image, inked and live scan. Acquisition of inked fingerprints is laborious. Therefore live scan fingerprint has become popular technology which is done based on the techniques like frustrated total internal reflection, ultrasound total internal reflection, thermal sensing, and sensing of differential capacitance.

Representation: Representation of a fingerprint is done based on the unprocessed gray-scale profile, entire ridge structure (ridge-based), and land mark based representation.

Though each has its own design constraints, all of the above are used in representation of fingerprint images in different scanning methods. Landmark or minutiae based representation has one important advantage in terms of privacy. One cannot reconstruct the entire fingerprint image from the fingerprint landmark information alone. The American National Standard Institute [ANSI] – National Institute of Standards and Technology [NIST] standard representation of a fingerprint is based on minutiae location and orientation[6]. The typical minutiae of a fingerprint is shown in Fig 1.3 in the previous section.

Feature Extraction: A feature extractor finds the ridge endings and bifurcations on the input fingerprint images. The minutiae extraction is not a complicated task if ridges can be perfectly located in the input fingerprint image. Reliable minutiae-extraction algorithms should not assume perfect ridge structures since in practice it is not possible to obtain a perfect ridge image[6].

Matching: The matching phase defines a measurement of similarity between test and reference fingerprint representation. The matching module also defines a threshold by which a decision is made about the validity of the fingerprint [6].

1.2.3 Various Fingerprint Image Sensing Devices

There are primarily three types of image capture devices, optical, solid state and other [9].

Optical fingerprint capture devices have a long history dating back to the 1970's. These devices operate on the principle of frustrated total internal reflection (FTIR). Efforts have been put to reduce the size of these devices. There are also other optical technologies than FTIR such as fiber optics [6]. Some of the new optics-based sensing units offer much lower prices and smaller sizes than did their predecessors [3].

Recently, solid state sensors have become popular in the market. These are made up of microchips which contain a surface that images the fingerprint by one of the following technologies. Capacitive sensor devices incorporate a sensing surface composed of a rectangular array of about 100,000 conductive plates over which a dielectric is placed. The other plate of the capacitor is the skin of the user finger. The ridges of the fingerprint are close to the surface and have high capacitance whereas the valleys have lower capacitance. The other surfaces proposed are pressure sensitive which uses piezoelectric material, and temperature sensitive sensors which respond to the temperature difference between the ridges and valleys [9].

Two major companies which ship solid state sensor chips, SGS-Thomson and Veridicom, use dc capacitive sensors, while Thomson-CSF's finger chip uses thermal sensing. Hughes briefly pursued an RF impedance based array device but did not commercially pursue this device. Harris FingerLoc IC is also a capacitive fingerprint sensor but instead of measuring capacitance with dc, it uses an ac electric field [3].

Low cost and compact size are the two most important factors that decide the future of a product in the large volume personal verification market. Solid state sensors have an edge where their compact size approaches a lower limit of size needed to capture the surface area of finger, about 1x1 inch with a fraction of an inch depth [9]. Target price range for acceptance of solid state sensors in broad application areas is considered to be on the order of \$10 per unit or less.

Optical scanners have the advantage of being able to support larger image capture size. It is costly to manufacture a large solid state sensor due to yield considerations[9]. There is also an assertion that because the finger never directly touches the chip in optical scanning systems, the device is inherently safer than capacitive direct contact sensing devices. But the IC companies have developed a chip coating that even scratching with a diamond scribe cannot damage it[3]. On the whole, solid state finger print capturing devices are dominant in the market place now, having greater flexibility for various applications.

1.3 CMOS Review

Complementary Metal Oxide Silicon (CMOS) technology is at the heart of Silicon solid state fingerprint sensor approaches. In this chapter, a brief explanation of CMOS devices and its various technologies are mentioned. Explaining in detail about CMOS device structure is beyond the scope of this dissertation.

1.3.1 Complimentary MOS Transistor

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has become prominent as soon as digital switching circuits have emerged. The fabrication of large scale IC digital circuits became possible with MOS transistors from the fact that its size can be reduced for use in densely packed circuits [10]. The density achievable has recently made large (100k to 300k elements) fingerprint sensor arrays viable.

The Complementary MOS device is a combination of n-channel and p-channel MOS transistors integrated on the same chip as shown in Fig 1.4. The CMOS has an unique characteristic of practically zero standby power, which makes them particularly useful in digital and VLSI applications[11].

The main features of CMOS technology are polysilicon gate(n-type for n-channel MOSFET and p-type for p-channel MOSFET), refractory metal silicide on the

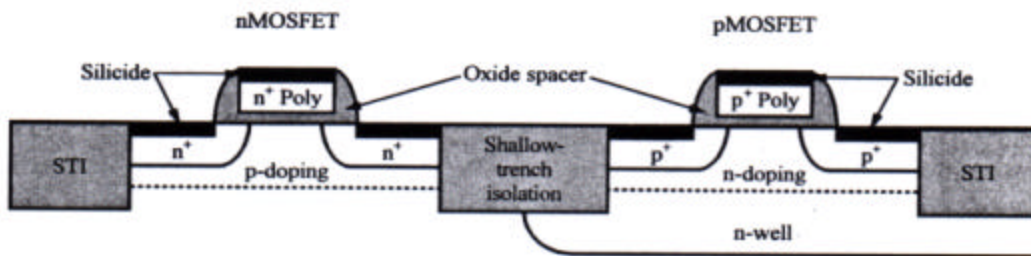


Fig1.4 CMOS device cross section [11]

polysilicon gate and on the source and drain diffusion regions, and shallow-trench oxide isolation between the channels [11].

1.3.2 CMOS process flow and planarization

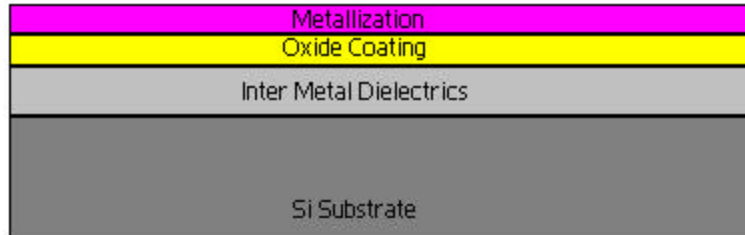


Fig1.5 The deposition process of various layers on Si substrate in CMOS fabrication

The fabrication process of CMOS involves deposition of various films over the silicon substrate in the order shown in the above figure. It is not appropriate to discuss about each process here, but the films and materials which lie over the oxide coating are a major concern in this work as this is what the plates are made of in a fingerprint sensor. So, a brief description about the planarity of the device, interconnect metals, and dielectrics is given below.

The deposition of both insulating and conducting films on a flat silicon substrate as it proceeds to metallization process results in an increasingly nonplanar structure of the device. This loss of planarity creates two problems. One is local issue, that is maintaining step coverage without breaks in the continuity of fine lines, and another is global, the inability to produce fine line pattern over the substrate with the loss of planarity. The techniques for making the microchip flat are commonly referred to as planarization techniques. There are various techniques available, such as LOCAL Oxidation of Silicon(LOCOS), Chemical Mechanical Planarization(CMP), encapsulation etc., to achieve planarity of the device but these are a function of the height and spacing of the features. The features which are narrow and closely spaced are more readily planarized than the features which are wide and spaced apart. This is the most important factor to consider while designing a fingerprint sensor device or any microchip device.

Al and Silicide are the most commonly used materials for metallization in VLSI devices. As circuits become more complex, the area utilization of the silicon surface becomes difficult. To avoid these problems, multilevel metallization schemes are used which aids in providing additional surface area and solving topological problems of interconnection. Three layer metallization is often used with thin insulating films deposited which serve as barrier between these layers. These inter metal dielectrics (IMD) should have a reasonably low dielectric constant and a high electric breakdown electric field strength. SiO_2 and Si_3N_4 are commonly used materials for these intermediate layers in fingerprint sensor devices[5].

1.4 Capacitive Fingerprint Scanning Devices

Conventional forms of fingerprint sensing devices such as optical detection and pressure detection suffer from the disadvantages of high cost and bulkiness [12].

The capacitive fingerprint sensor which avoids the aforementioned problems is composed of 2-D array of sensing elements using standard CMOS processing covered by a thin dielectric layer as shown in fig 1.6. Each sensing element acts as capacitor bottom plate, while the finger surface acts as grounded top plate which is assumed to be an equipotential surface. Each active element detects the change in electric field (and hence change in capacitance) induced by the proximity of the fingerprint valleys and ridges to the cell plates. The different values of these capacitances are measured and an electronic representation of the fingerprint is obtained [12].

The choice of dielectric material and thickness is critical in the design of sensor model. The requirement that the top dielectric or passivation layer be exposed to the external environment is completely foreign to typical IC technology. The finger which is placed on the sensor chip contacts this dielectric material, and therefore the material has to be made chemically rigid enough to resist skin oils, moisture, salts, acids that can migrate to the silicon, electrically isolated to prevent electrostatic discharge, and

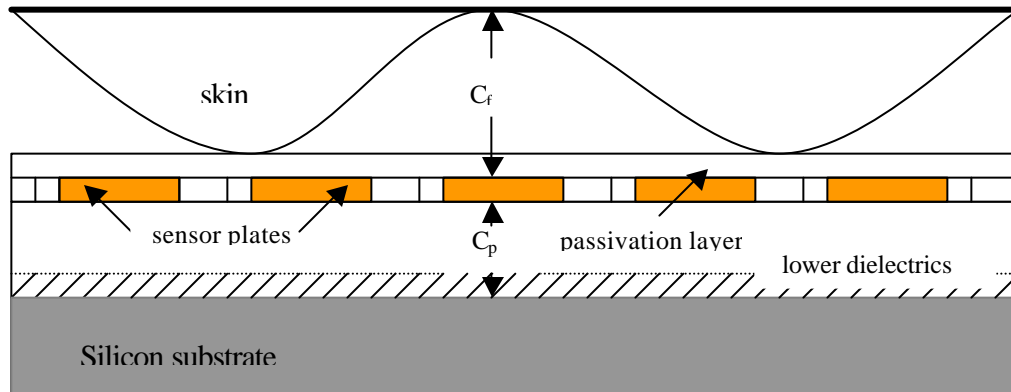


Fig 1.6 Typical Capacitive Sensor Design

mechanically strong to avoid surface scratching. Major companies like Veridicom use a special type of coating material as a passivation layer which is 100 times the strength of glass (see Appendix-A for complete specifications). Such a rugged design withstands frequent use of the sensor for commercial applications like cell phones and laptops and for outdoor use in applications such as an access control device for a vehicle or ATM[8]. The sensitivity of the device is directly proportional to the ratio of C_f / C_p , (see in figure) where C_f is the capacitance between the finger and the sensor plate and C_p is the parasitic capacitance associated with each sensor plate, which includes substrate, neighboring plates, grounded grids etc. So, sensitivity can be increased by maintaining a high C_f / C_p ratio by altering the dielectric constant and thickness of lower dielectrics[8]. In our modeling, high C_f / C_p ratios are explored by providing shielding to the sensor plate, and changing the size of sensor plates and shields.

1.4.1 The Veridicom Sensor Cell

At the time of this research, the family of capacitive fingerprint sensor devices manufactured by Veridicom each consist of a sensor array of 300x300 elements, fabricated using a standard digital 0.5 micrometer CMOS process[8] A block diagram of the fingerprint scanner chip is shown in Fig 1.7.

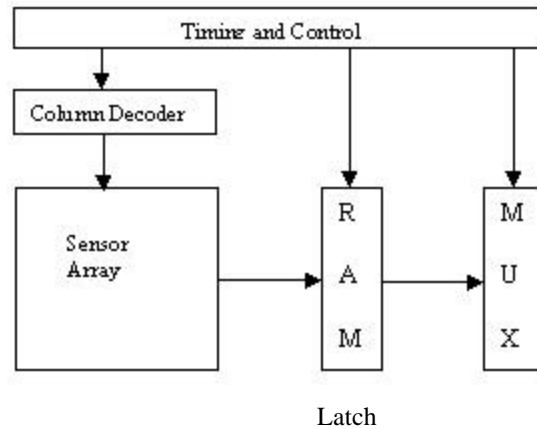


Fig 1.7 Block diagram of the chip

The following Fig 1.8 shows an individual Veridicom FPS 100 sensor cell with associated column read out circuit [8]. A simple sample & hold logic circuit is used to read the measured capacitances through a series of row-column selections.

Basic device operation is described in [8]. The entire read cycle timing diagram is shown in the Fig 1.9. At the beginning of each cycle, sensor plates are activated by row enable signals RE and RAD. Each sensor plate is then pre-charged using PRE. Source follower T_1 buffers the voltage appearing on sensor node and the row select signal RAD gates this voltage onto a column data bus, COL, through source of T_2 . C_A in sample & hold logic stored with precharge voltage V_A by pulsing SHA. After PRE is released current source I_s drains the deposited charge from the plate during a fixed period of interval. Now, this new voltage V_B is sent to C_B by pulsing SHB.

A subsequent circuit subtracts V_B from V_A to remove pattern noise caused by transistors T_1 and T_2 (due to variations in their threshold voltages) and give an output which is approximately proportional to the gap between the finger and the sensor plate[8].

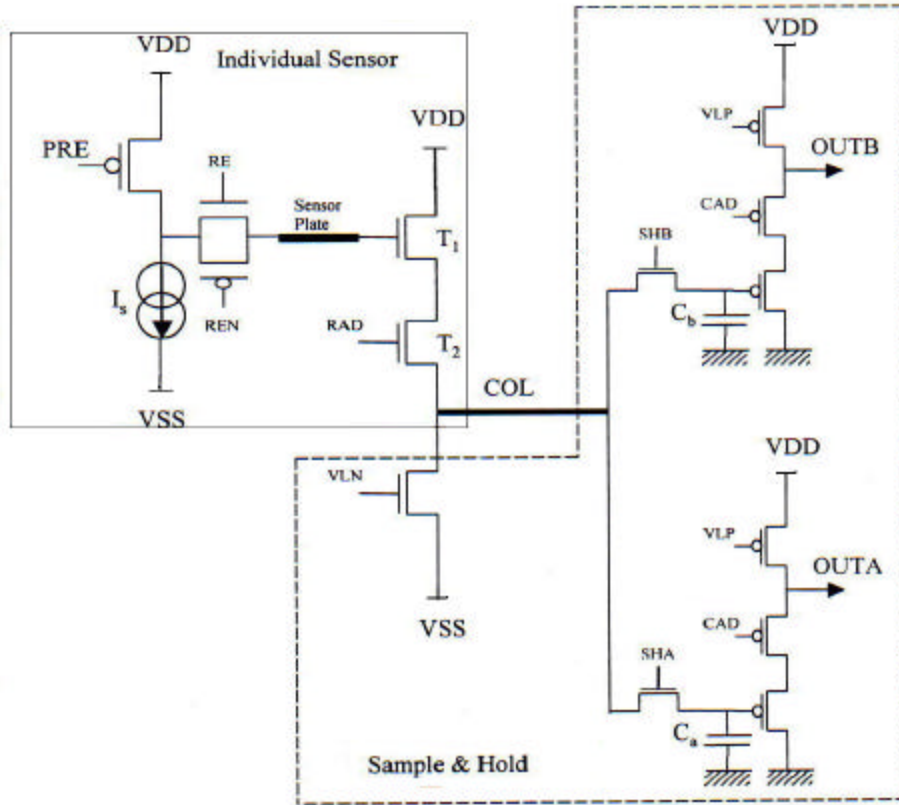


Fig 1.8 Individual Sensor Cell with Sample and Hold Logic[8]

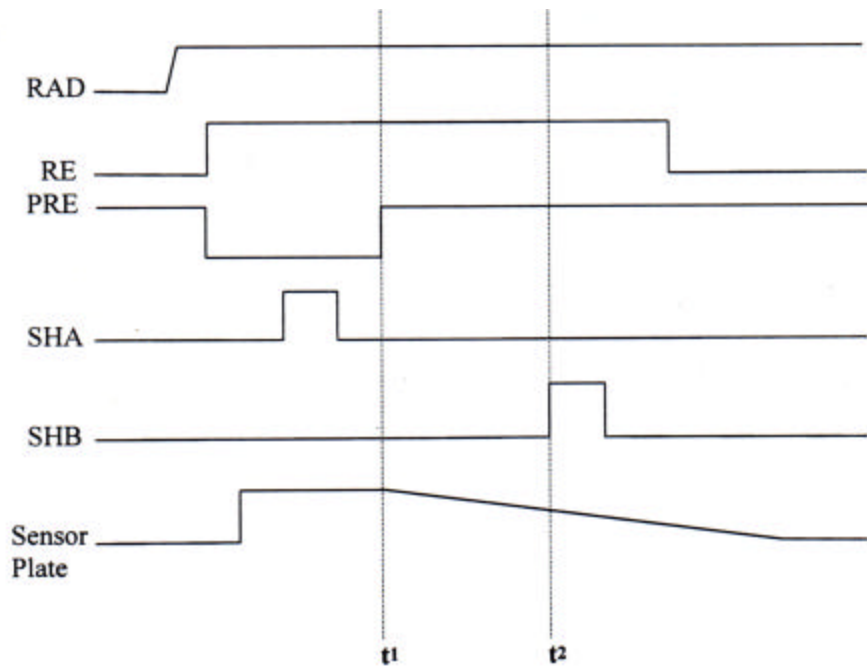


Fig 1.9 Sensor row access timing Diagram [8]

The calculation for capacitance from this sensed voltages can be illustrated by the following,[13].

$$V_A = V_a + V_{\text{Noise}}$$

$$V_B = V_b + V_{\text{Noise}}$$

V_A , V_B are the voltages at beginning and end of sample & hold period respectively, which includes noise as well. V_a and V_b are voltages at same periods but without noise. We have relationship of charge and voltage as,

$$q = CV$$

Let the charges at above two intervals be q_1 and q_2 .

∴ Change in the charge or net charge is

$$q_2 - q_1 = C (V_B - V_A) \text{ becomes}$$

$$q_2 - q_1 = C (V_b - V_a) \text{ ----- (1)}$$

From the timing diagram, we can write as,

$$q_1 - q_2 = I_s (t_2 - t_1) \text{ -----(2)}$$

Equating (1) and (2),

$$C (V_a - V_b) = I_s (t_2 - t_1)$$

$$C = I_s \frac{(t_2 - t_1)}{V_a - V_b}$$

$$\text{Or } C \propto \frac{1}{(V_a - V_b)}$$

Therefore, the capacitance measured by the capacitive sensor is inversely proportional to voltage sensed which in turn is directly proportional to the distance between the finger and chip.

1.4.2 Parasitic Capacitance

The parasitic capacitance is defined as the unwanted capacitance sensed by the sensor plate from neighboring sensor plates, neighboring underlying shields (which is one of the solutions to reduce the parasitic capacitances explained later), neighboring guard grids and the silicon substrate. All the capacitances involved with each sensor element including the object capacitance are shown in the following Fig1.10. Of all these the main contributor is the grounded guard grids which sit on either side of the sensor plate. The neighboring plates and shields provide secondary contributions.

In order to reduce the parasitic capacitance, the current design of the sensor cell incorporates a shielding plate under the sensor plate in each cell which follows the sensor plate voltage. The underlying shield plate and its size relative to the sensor plate, and the position of both (sensor plate and underlying shield) relative to the grounded grid and neighboring sensor plates are critical to the control of parasitic capacitances.

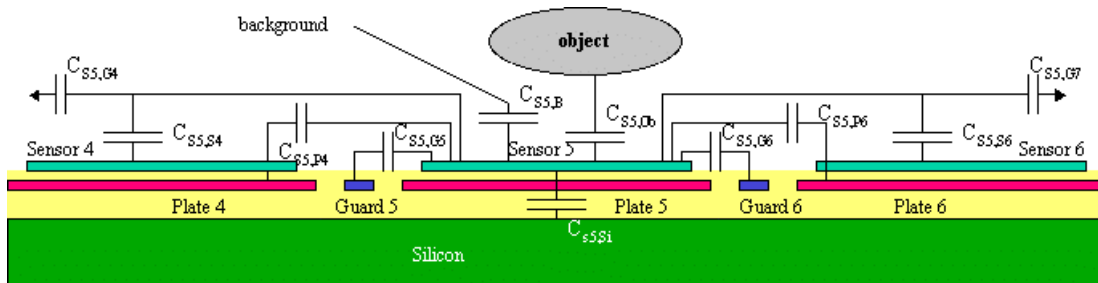


Fig 1.10 Various capacitances involved for sensor plate 5, all of them except sensor to object capacitance $C(s5, obj)$ contribute towards total parasitic capacitance.

1.5 Research Overview

Though the capacitive fingerprint sensors are available commercially and are used in many applications, increased performance and device operation understanding is still sought. Approaches for achieving improved depth sensitivity of the capacitive imaging process are of particular interest. This goal is closely tied to the need to understand the role of capacitive parasitics in the device geometry and layout and seek means to reduce their contribution to the total capacitance. In addition, new modes of device operation that may enhance performance or further improve user acceptance represent important avenues of investigation.

The primary objective of this work is to quantify and explore these approaches through the use of appropriate models and simulation software. The results of this work will serve as a guide for future device designs.

The research is composed of a set of related studies. These studies are summarized briefly below.

- ***Vertical sensitivity using structured objects in static and swipe mode:***

To start with, most current device designs are not efficient in resolving the capacitance variation when the object distance goes beyond 100 micrometers. To evaluate the ability of existing model to detect and resolve spatial features from capacitance variations, structured objects named here as “Virtual Test Objects(VTO)” are used as test objects. The swipe imaging has become popular in fingerprint capturing devices recently This type of imaging differs from static imaging in that user swipes his finger across a tiny fingerprint scanner instead of just putting over it for more privacy. The parasitic capacitance effect and the row spacing of such a model when different sized sensor cells are used in the array are important factors to be considered. The model is tested in swipe mode and based on the coupling capacitances of this uniform cell array of different cell sizes, the row spacing of linear arrays could be evaluated.

- Embedded sensor plate:***

The passivation layer overlaying the chip is essential in order to protect the device from chemical and physical wear and tear. The material of this top dielectric layer and its thickness are critical in this regard and must not adversely effect the capacitance measurement ability of the sensing elements. To see the effect of this passivation layer on vertical sensitivity, the model is tested with and without this layer to evaluate the thickness of the layer that could be used.
- Well structure of underlying shield plate:***

The primary parasitic capacitances impacting a sensor cell are the mutual capacitances of the sensor plate with Si substrate, the guard grid surrounding its cell, and the neighboring plates. Though the flat underlying shield helps in suppressing the sensor to Si substrate coupling, it doesn't isolate the neighboring guards, and plates. To extend the advantage of having the shield under the sensor plate, the design of shield plate is slightly modified by tilting its edges vertically so that it covers the sensor plate on either side as well. The effect of this well-shaped structure was evaluated for its ability to reduce sensor plate coupling to neighboring elements.
- Electrostatic Discharge Ring:***

With consideration of a linear swipe type device, the impact of bringing the external ESD ring to within close proximity of the linear sensor arrays was raised as a potential concern. The distance of the ring from the last sensing element is greatly depended on the height of the ESD ring. These two factors are evaluated.
- Mixed size cells and sensor plates in the array:***

In order to explore row to row spacing in a linear array, an array with different sized cells in one dimension is designed. This one dimensional array can be considered as one single column of a linear array. The effect of capacitive coupling between such cells are evaluated by varying the gaps in between the cells. Reducing the sensor plate size relative to shield plate decreases the

measurement ability of sensor plate, therefore to balance these two issues a mixed array is designed with different size of sensor plates keeping shield plate size fixed. This is done with the intent of reducing electrostatic field coupling, by having many small sized sensor plates in each row.

- **Adaptive Arrays:**

Each sensor plate in the array has grounded grid which is a major contributor towards parasitic capacitance array. If some of the grids in the array are switched off and relative sensors are interconnected then the parasitic capacitance can be reduced to some extent. This experiment is done considering possibility of grid switching and electrical interconnections between the sensors.

The following chapter, describes the sensor physical model, simulation parameters and the software used to perform the electrostatic modeling to obtain the effect of geometry and layout design changes on capacitances. The results and detailed explanation of above mentioned modeling activities are given in Chapter 3. Finally, results are reviewed, approach to be taken for future work is mentioned and conclusions about this work are made in the final chapter.

Chapter 2

Simulation Theory and Software

A requirement underlying this entire body of work is the need to calculate capacitance. A basic one dimensional ten cell array is used for performing modeling activities in this work.

The capacitance developed between the sensor plates and the finger surface is the desired parameter to be determined in these simulations along with the parasitic capacitances between the sensor plates and other components in the sensor. These capacitances are indicated schematically in Fig1.10. The theory involved in calculating these capacitances considering all the neighboring elements such as guards, shield plates, sensor plates is illustrated in this chapter. Before going into that, a brief introduction is given about the software tool used for this calculations.

2.1 Software Tool

Given the complexity of the geometry of the sensor cell and the need to understand multi-cell interaction analyzing this model analytically will not give sufficient information. Therefore, an electrostatic modeling tool will be used to calculate these capacitance values. This tool must provide flexibility of change in geometry, parameters, materials, excitations, etc., so that different types of designs can be tested in one simulation by performing required number of iterations. The tool must also give accurate results with minimal error and be fast enough to run on a system in a practical time frame.

The Software tool used throughout this work is *Maxwell 2D Field Simulator* from *Ansoft* Corporation. This is an interactive software package that uses finite element analysis to solve two-dimensional static electromagnetic problems [17].

Maxwell 2D quickly obtains critical device parameters such as force, torque, inductance, and *capacitance* from the physical design information.

The changes in geometry, material and electrical parameters are evaluated automatically by the integrated parametric analysis module. This module allows all design options to be thoroughly explored within a simulation. Maxwell 2D uses the finite element method and its adaptive automatic mesh refinement feature ensures accurate, converged solutions. The simple flow of the software along with status monitoring and error checking features provide a structured analysis environment. The executive user interface guides user to specify the appropriate geometry, material properties, and excitations for a device. The software then automatically creates the required finite element method, iteratively calculates the desired electrostatic field solution and quantities of interest such as inductance and *capacitance*. Finally, it allows the user to analyze, manipulate, and display field solutions [18].

In the next section, detailed explanation of electrostatic field equations and capacitance matrix is given .

2.2 Electrostatic Field Simulation

The electrostatic field simulator computes static electric fields arising from potential differences and charge distributions [18].

2.2.1 Field Equations

The electrostatic field simulator solves for the electric potential, $\phi(x,y)$, in this field equation:

$$\nabla \cdot (\epsilon_r \epsilon_o \nabla \phi(x,y)) = -\rho$$

where,

- $\phi(x,y)$ is the electric potential.
- ϵ_r the relative permittivity. It can be different for each material.
- ϵ_o is the permittivity of free space, 8.854×10^{-12} F/m.
- $\rho(x,y)$ is the charge density.

This equation is derived from Gauss's Law, which indicates that the net electric flux passing through any closed surface is equal to the net positive charge enclosed by that surface. In differential form, Gauss's Law is,

$$\nabla \cdot \mathbf{D} = \rho$$

where $\mathbf{D}(x,y)$ is the electric flux density, since $\mathbf{D} = \epsilon_r \epsilon_0 \mathbf{E}$, then:

$$\nabla \cdot (\epsilon_r \epsilon_0 \mathbf{E}(x,y)) = \rho$$

In a static field, $\mathbf{E} = -\nabla f$. Therefore,

$$\nabla \cdot (\epsilon_r \epsilon_0 \nabla f(x,y)) = -\rho$$

which is the equation that the electrostatic field simulator solves using the finite element method.

After the solution for the potential is generated, the system automatically computes the E-field and D-field using the relations $\mathbf{E} = -\nabla f$ and $\mathbf{D} = \epsilon_r \epsilon_0 \mathbf{E}$. [18].

2.2.2 Capacitance

Two conductors separated by an insulator are said to form a capacitor. The conductors usually have charges of equal magnitude and opposite sign, so that the net charge on the capacitor as a whole is zero. The electric field lying in between the conductors is proportional to the magnitude of this charge, and it follows that the potential difference 'V' between the conductors is also proportional to the charge magnitude 'Q'.

The Capacitance 'C' of a capacitor is defined as the ratio of magnitude of the charge 'Q' on either conductor to the magnitude of the potential difference 'V' between the conductors.

$$C = \frac{Q}{V}$$

From the definition it follows that the unit of capacitance is one Coulomb per Volt. A capacitance of one coulomb per volt is called one Farad [17].

In a single electric circuit, the capacitance represents the amount of energy stored in the electric field that arises due to a potential difference across a dielectric.

$$U_e = \frac{1}{2} C v^2$$

where U_e is the energy stored in the electric field, C is the capacitance, and v is the voltage across the dielectric.

The Maxwell 2D Field Simulator computes the capacitance between two conductors by simulating the electric field that arises when a voltage differential is applied. Then, by computing the energy stored in the field, the corresponding capacitance can be computed.

$$C = \frac{2U_e}{v^2}$$

To compute capacitances using this method, the E-field and D-field associated with a given distribution of voltages must first be computed. The electrostatic field simulator, which computes the electric potential at all points in the problem region, performs this task [19].

2.2.3 Capacitance Matrix

A capacitance matrix represents the charge coupling within a group of conductors. This is the relationship between the charges and voltages for the conductors. Given the four conducting objects as shown in Fig 2.1 with the outside boundary taken as a reference, the net charge on each object will be:

$$Q_1 = C_{10}V_1 + C_{12}(V_1 - V_2) + C_{13}(V_1 - V_3) + C_{14}(V_1 - V_4)$$

$$Q_2 = C_{20}V_2 + C_{12}(V_2 - V_1) + C_{23}(V_2 - V_3) + C_{24}(V_2 - V_4)$$

$$Q_3 = C_{30}V_3 + C_{13}(V_3 - V_1) + C_{23}(V_3 - V_2) + C_{34}(V_3 - V_4)$$

$$Q_4 = C_{40}V_4 + C_{14}(V_4 - V_1) + C_{24}(V_4 - V_2) + C_{34}(V_4 - V_3)$$

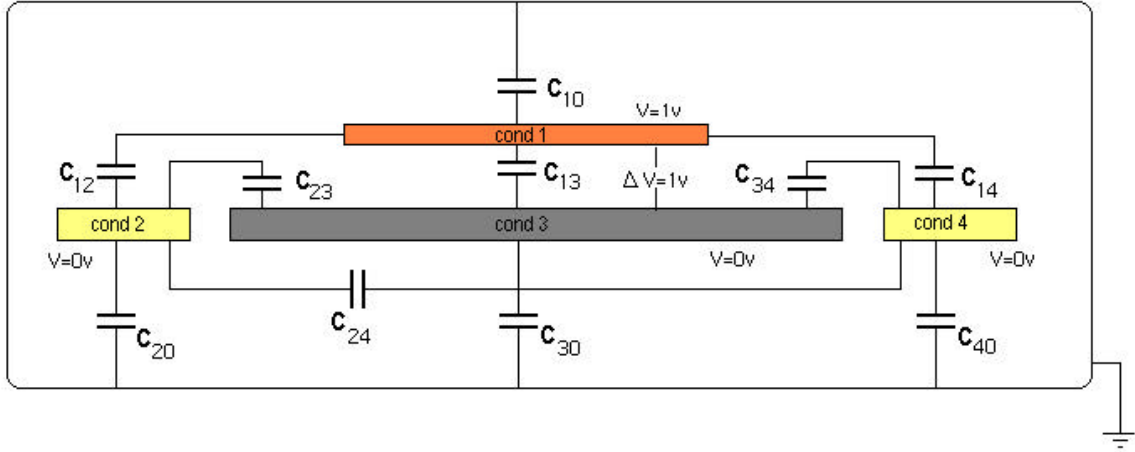


Fig 2.1 Capacitances between objects

This can be expressed as in matrix form as:

$$\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ Q_4 \end{bmatrix} = \begin{bmatrix} C_{10} + C_{12} + C_{13} + C_{14} & -C_{12} & -C_{13} & -C_{14} \\ -C_{12} & C_{20} + C_{12} + C_{23} + C_{24} & -C_{23} & -C_{24} \\ -C_{13} & -C_{23} & C_{30} + C_{13} + C_{23} + C_{34} & -C_{34} \\ -C_{14} & -C_{24} & -C_{34} & C_{40} + C_{14} + C_{24} + C_{34} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}$$

The capacitance matrix above gives the relationship between Q and V for the four conductors and ground. In a device with n conductors, this relationship would be expressed by an $n \times n$ capacitance matrix. Capacitance matrix values are specified in Farads (Coulombs/Volt). If one volt is applied to Conductor 1 and zero volts is applied to the other three conductors, the capacitance matrix becomes:

$$\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ Q_4 \end{bmatrix} = \mathbf{C} \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} C_{10} + C_{12} + C_{13} + C_{14} \\ -C_{12} \\ -C_{13} \\ -C_{14} \end{bmatrix}$$

The diagonal elements in the matrix (such as $C_{(1,1)}$) are the sum of all capacitances from one conductor to all other conductors. These terms represent the self-capacitance of the conductors. Each is numerically equal to the charge on a conductor when one volt is applied to that conductor and the other conductors (including ground) are set to zero volts. For instance, $C_{(1,1)} = C_{10} + C_{12} + C_{13} + C_{14}$.

The off-diagonal terms in each column (such as $C_{(1,2)}$, $C_{(1,3)}$, $C_{(1,4)}$) are numerically equal to the charges induced on other conductors in the system when one volt is applied to that conductor. For instance, in column one of the example capacitance matrix, $C_{(1,2)}$ is equal to $-C_{12}$. This is equal to the charge induced on Conductor 2 when one volt is applied to Conductor 1 and zero volts are applied to Conductor 2.

The off-diagonal terms are simply the negative values of the capacitances between the corresponding conductors (the mutual capacitances). In column one of the example capacitance matrix, the off-diagonal terms represent the capacitances between Conductor 1 and the other three Conductors; in column two, the terms represent the capacitance between Conductor 2 and the other conductors; and so forth.

We can observe that the capacitance matrix is symmetric about the diagonal. This indicates that the mutual effects between any two objects are identical. For instance, $C_{(1,3)}$, the capacitance between Conductor 1 and Conductor 3 ($-C_{13}$), is equal to $C_{(3,1)}$, the capacitance between Conductor 3 and Conductor 1[19].

2.2.4 Computing Capacitance

To compute a capacitance matrix for a structure, the Maxwell 2D Field Simulator performs a sequence of electrostatic field simulations. In each field simulation, one volt is applied to a single conductor and zero volts is applied to all other conductors as shown in the Fig 2.1. Therefore, for an n-conductor system, n field simulations are automatically performed.

The energy stored in the electric field associated with the capacitance between two conductors is given by the following relation,

$$U_{ij} = \frac{1}{2} \int_{\omega} \mathbf{D}_i \cdot \mathbf{E}_j d\omega$$

Where:

- \int_{ω} specifies the volume integral and $d\omega$ is the unit volume.
- U_{ij} is the energy in the electric field associated with flux lines that connect charges on conductor i to those in conductor j .
- \mathbf{D}_i is the electric flux density associated with the case in which one volt is placed on conductor i .
- \mathbf{E}_j is the electric field associated with the case in which one volt is placed on conductor j .

The capacitance between conductors i and j is therefore:

$$C = 2 U_{ij} / v^2 = \int_{\omega} \mathbf{D}_i \cdot \mathbf{E}_j d\omega$$

Limitations:

Though Maxwell 2D field simulator can compute capacitances with accuracy, it only gives information about capacitance for two dimensional geometries. All the capacitances calculated in this simulations are per unit length, assuming extension of the cross section into the depth of the simulation plane. Maxwell 2D assumes that capacitance lies in the cross-sectional geometry of the sensor model in which 3D effects can be ignored for the purpose of analysis.

Chapter 3

Model Description and Simulation Results

Introduction:

In the previous chapters, the physical model of a capacitive fingerprint device is introduced and the procedure to calculate the capacitance matrix is explained. This chapter introduces the geometrical views of sensor chip and sensor cells and motivates the model (in terms of geometry, internal elements, materials etc.), which was developed for actual simulations. The geometrical views of chip and individual cell of the fingerprint sensor is shown in the following Fig 3.1 below.

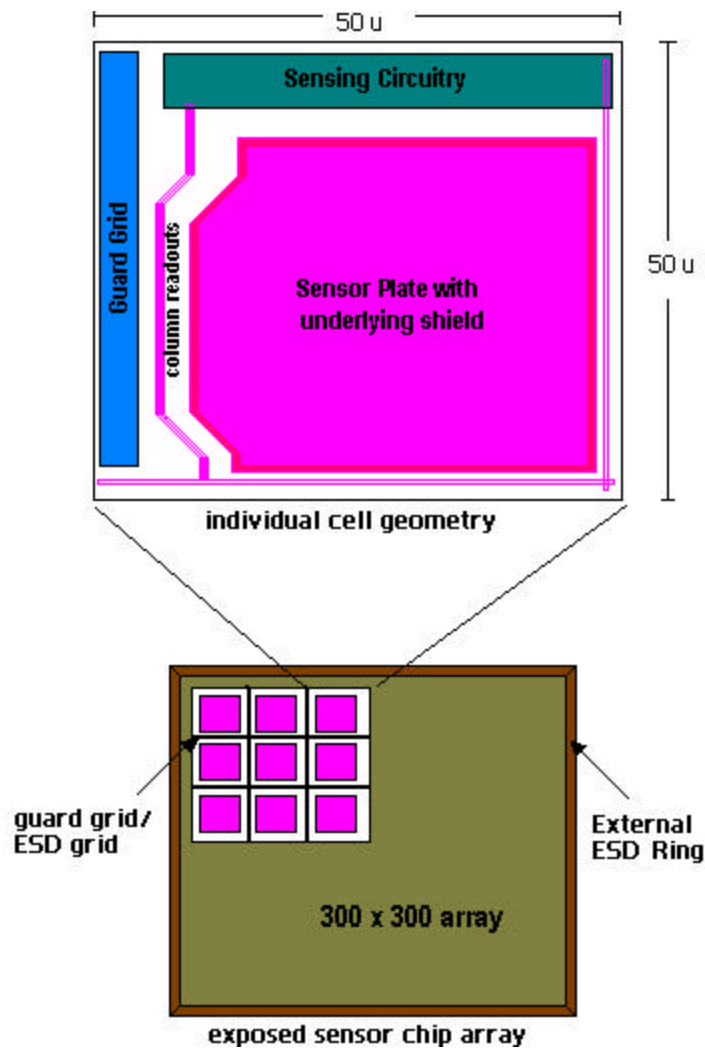


Fig 3.1 Complete sensor array with enlarged individual cell geometry[8]

A 3 x 3 cell array is highlighted on 300 x 300 cell array from which a single cell is enlarged to show the internal circuit layout of individual cell. Each cell of size approximately 50 x 50 micrometers has primarily a sensor plate, a shield plate, sensing circuitry and a guard grid, with over 60 % of the sensor cell area is devoted to the sensor plate[8]. The sensing circuitry consists of the CMOS circuits including sample and hold circuit which was introduced in the first chapter. The figure also shows the column readout line from the sensing circuit. The guard grid is placed between each cell for proper grounding of the circuit.

For the purpose of designing the geometry model for simulations a row of 10 cells is selected for modeling. Cells at the center of this row are used to simulate cells far from the actual array edges. It is assumed that all internal elements are similarly located in each cell to generalize the modeling of the device. Fig 3.2 shows a cross-sectional view of a 3-cell section showing the cell features used in the geometry model. The model was formulated keeping in view that future device designs might vary from the basic model. As a result, based on preliminary modeling work only those cell features are reflected in the geometry cross-section which have significant impact on fields. These are shown in the above figure and in Fig 3.5 in the next section.

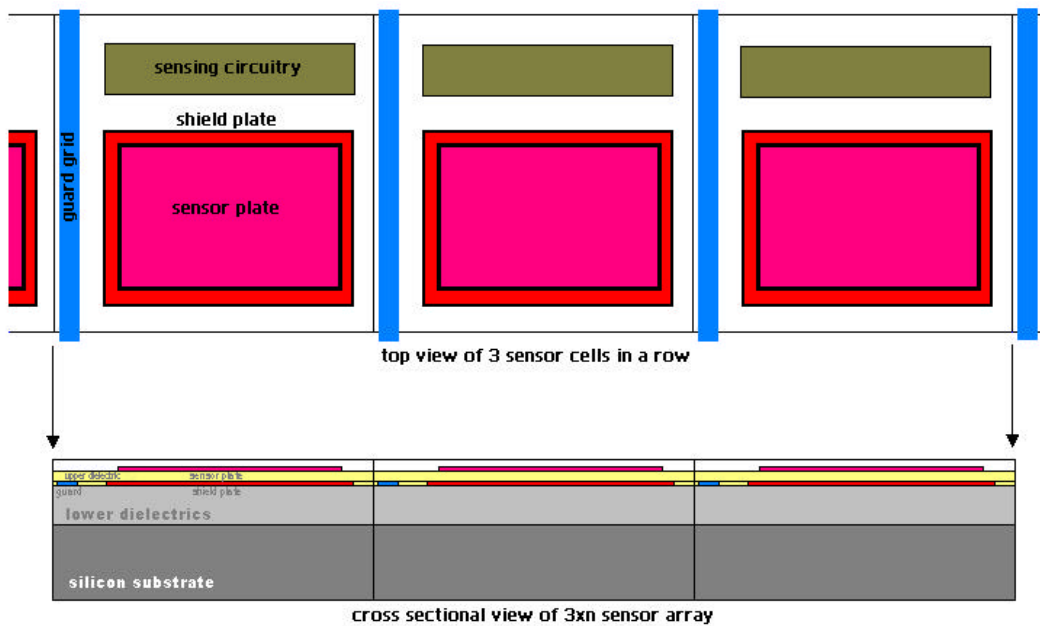


Fig 3.2 Top and Cross sectional view of one partial row of sensor chip

3.1 Parameters and Materials

The various sub-elements and their materials of a sensor cell are shown in the Fig 3.3 and are discussed briefly in this section.

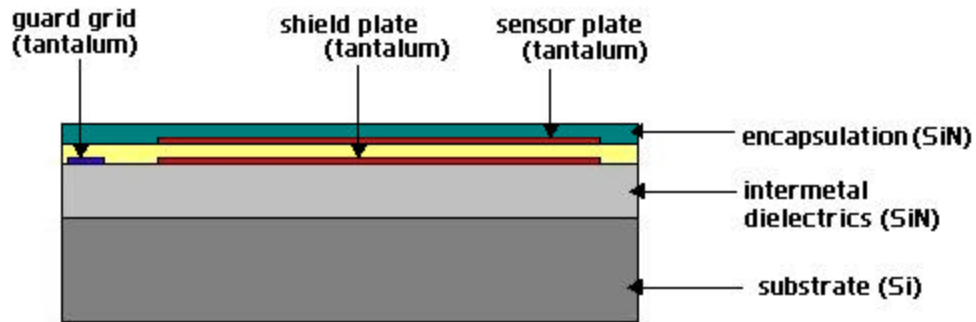


Fig 3.3 The various elements and their assigned materials in a sensor cell

The parameters used in the simulations through out this work are given below,

- | | |
|------------------------------------|---------------------------------|
| 1. Silicon substrate (Si) | 5. Space |
| 2. Silicon Plate (Sensor) | 6. Guard Grid |
| 3. Underlying Shield Plate (Plate) | 7. Right |
| 4. Left | 8. Inter Metal Dielectric (IMD) |

The materials used in the model generation and simulations are given below,

- | | |
|---------------------|--------------|
| 1. Silicon | 4. Tantalum |
| 2. Silicon di oxide | 5. Water Sea |
| 3. Silicon Nitride | |

3.1.1 Parameters used

Silicon (Si):

This name is used for the base substrate of the sensor cell in the model. This model consists of ten sensor cells horizontally having flexibility of change in their size. A parametric geometric model has been formulated in order to perform the

simulations and see the impact of sensor cell size on the capacitance. In this work cell sizes tested are 50 u, 100u, 200u, & 300 u. The results of these cells are given in next chapter.

Underlying Shield (Plate):

Plate is a 0.2 micron thick underlying shield for each sensor plate in each cell. It is assigned to the same material of that of the sensor plate, and it follows the sensor voltage. This plate is added in the model to reduce the parasitic capacitance with the substrate. This underlying plate relative to the sensor plate and position of both relative to the neighboring guards and shield plates are critical to the reduction of the dominant parasitic capacitances.

Sensor Plate (sensor):

Sensor Plate is also a 0.2 micron thick metal which is the actual sensing area in the model. A variable ‘factor’ is used to vary the size of the sensor plate size relative to the underlying plate. In this work, factors 0.5 to 1.0 are tested and an optimum one is used throughout the remainder work. The mathematical equation for the sensor plate is ,

$$\text{Sensor plate size} = \text{factor} * \text{sensor plate size}$$

Left:

Left is a 0.25 micron wide constant block on the left side of plate in each cell. This is being kept in the model to isolate the adjacent cells.

Space:

Space is another constant 2.25 micron block adjacent to the ‘Left’.

Guard:

Guard is a constant 1.5 micron wide and 0.2 micron thick grounded grid which is of major concern in this work. It acts as circuit ground path for the sensing elements and contributes to parasitic capacitance. These grids are very left of

Plate in each cell. In the following chapters some models are given to reduce the capacitance arising from grounded grids.

Right:

Right is a constant 1.5 micron block at the far end of each sensor cell.

SiN:

These are the rectangular silicon nitride blocks which isolate sensor plate from the underlying shield plates in the model. This nitride film thickness is 0.5 microns.

IMD:

These are the Inter Metal Dielectrics of thickness 3 microns which isolate the silicon substrate from the other elements of each cell in the model.

3.1.2 Materials Used [16]

Silicon:

Silicon is used as substrate in the model. Silicon's atomic structure makes it an extremely important semiconductor. Highly purified Silicon, doped with elements such as boron, phosphorus, and arsenic, is the basic material used in computer chips, transistors, silicon diodes, and various other electronic circuits and switching devices.

Silicon dioxide:

Silicon dioxide is used routinely as inter metal dielectric (IMD). Silicon dioxide is one of the most commonly encountered substances in electronics industry. It has the unique properties such as, the only native oxide of a common semiconductor which is stable in water and at elevated temperatures, an excellent electrical insulator, and capable of forming a nearly perfect electrical interface with its substrate.

Silicon Nitride:

This material is used as an insulator between the sensor plate and the underlying shield plate. It is also used as passivation layer which encapsulates the sensor plates. "Bulk" silicon nitride, Si₃N₄, is a hard, dense, refractory material. Its structure is quite different from that of silicon dioxide. CVD silicon nitride is generally amorphous, but the material is much more constrained in structure than the oxide. As a result, nitride is harder, has higher stress levels, and cracks more readily..

Tantalum:

Tantalum is used for sensor plates, underlying shield plates and guard grids in the model. It is a very hard metal and almost completely immune to chemical attack at temperatures below 150°C. Tantalum is used to make a variety of alloys with desirable properties such as high melting point, high strength etc. Tantalum has unique electrical, chemical and physical properties that lead to its application in a growing number of new and highly sophisticated applications. This is used as sensor plates because its hardness makes plates less prone to mechanical scratch damage, compression etc.

Sea Water:

A "standard" sea water has been defined as one containing 35 grams of salts per kilogram of solution. The human sweat has almost the same properties of sea water, hence this material is assigned to all the test objects in this work in order to get the effect of sweating finger.

3.2 Virtual Test Objects

Simulations of the parametric device array model were performed using two classes of test objects. One is a rectangular block which is used primarily to test the parasitic capacitances when the test block is at a certain distance from the sensor plates.

The other is a trapezoid model which is designed to simulate the dimensions of the ridges and valleys of a finger.

3.2.1 Rectangular Block

This is just a rectangular block designed to test the sensor plate performance when this object is at a certain distance. The block width is initially kept to 500 micrometers, to cover all the sensor plates in given model as shown in the Fig 3.4. However, the width of the block is variable and it will increase depending on the total model width, covering the sensor plates for all cell sizes as shown in Fig 3.5. The block is assigned to ‘water sea’ as explained in second chapter.

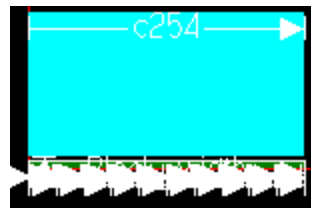


Fig 3.4 Rectangular Test Object on the sensor model of cell size 50 micrometers

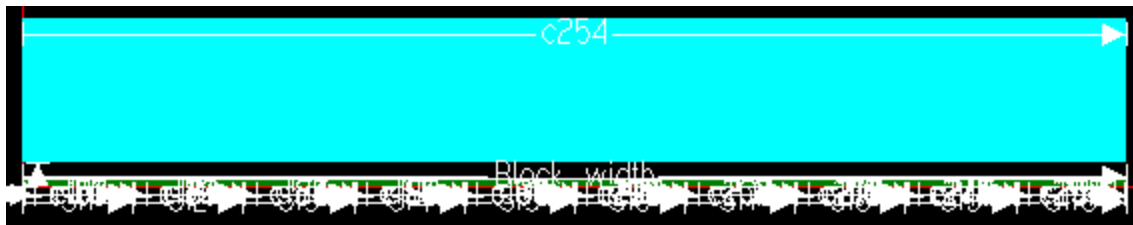


Fig 3.5 Rectangular Test Object on the sensor model of cell size 200 micrometers

3.2.2 Trapezoid Block

This is another test object used in simulations, which is a repetitive trapezoid block as shown in following Fig 3.6. The dimensions and material parameters used mimic that of the finger and enable changes in the profile and lends itself to easier physical interpretation. Here a deep recess is used and long sloped transition regions.

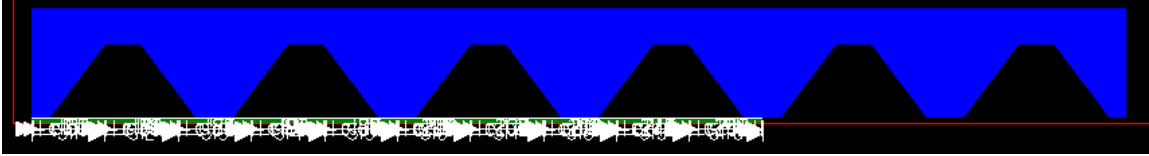


Fig 3.6 Trapezoid test object on the sensor model of cell size 200 micrometers

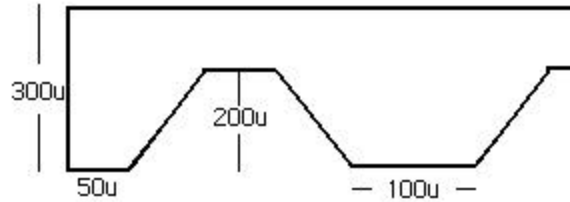


Fig 3.7 A piece of trapezoid and its internal dimensions

This abstract model is designed to test the sensor plates performance at ridges and valleys of the finger print image, the deepest point in the trapezoid object is approximately that of a valley depth in the finger print image. The test object is designed to a width of 3000 micrometers to accommodate larger cell sizes. The internal dimensions are shown in the Fig 3.7.

3.3 Sensor Model Study

This study is carried out on the basic parametric model using a rectangular test object which is shown in the Fig 3.8 below. The specific focus of this sensor model study is to explore the vertical sensitivity of the sensor as a function of cell resolution/sizing. In the following two sections, the results of sensor to object capacitance are shown with plots by testing different sensor plate sizes and different cell sizes respectively. The optimum one is selected after analyzing the results in each section to use in further work.



Fig 3.8 Sensor Model, consisting of 10 cells, a 1-D array with rectangular test object

3.3.1 Sensor Plate Size Study

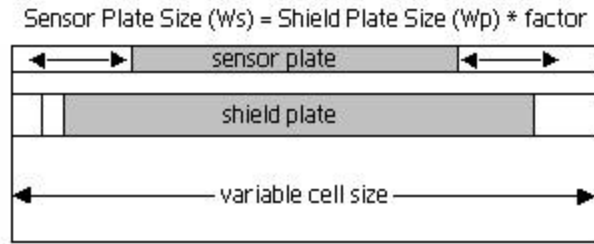


Fig 3.9 A Sensor Cell showing how cell size and sensor plate size can be varied

The primary concern in this work is the total parasitic capacitance impacting a cell especially the capacitances of the sensor plate to the Si substrate, the guard grid surrounding the cell and the neighboring plates. By reducing the sensor plate area which can be done by choosing *factor* value less than unity as shown in Fig 3.9, both the mutual capacitance between sensor plate and the guard grid can be significantly reduced. The *factor* is a constant used in model geometry to vary the sensor plate size relative to underlying shield plate.

The following plots show the simulation results which illustrate this for three sensor plate factors 'f' of 1.1, 1.0 and 0.8 where the sensor width is given by f * width of underlying shield plate.

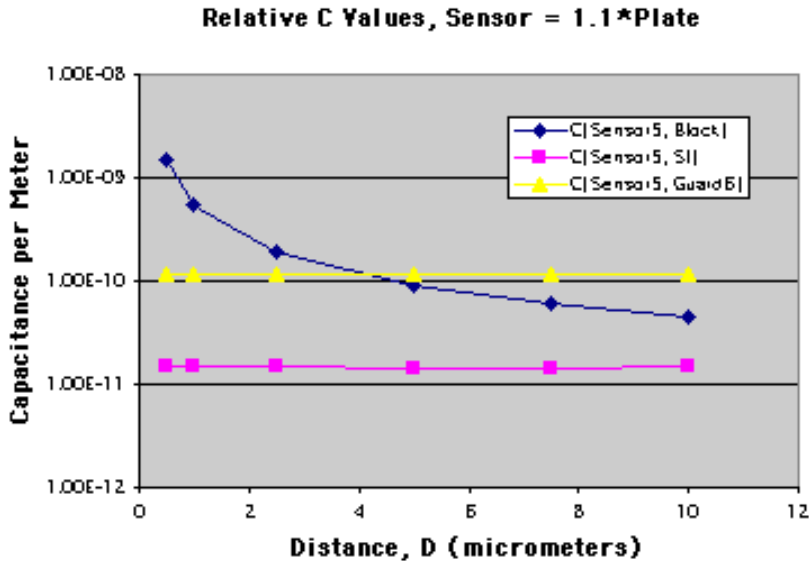


Fig 3.10 Plot showing typical capacitances with sensor factor =1.1

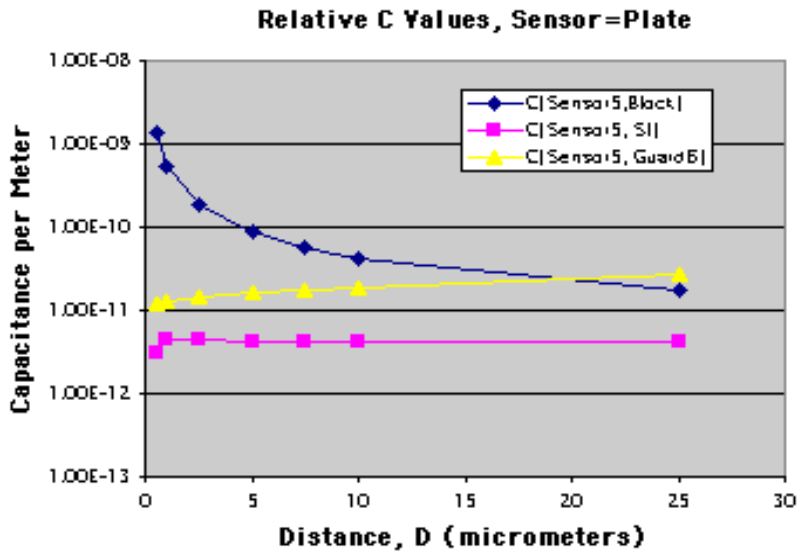


Fig 3.11 Plot showing typical capacitances with sensor factor =1.0

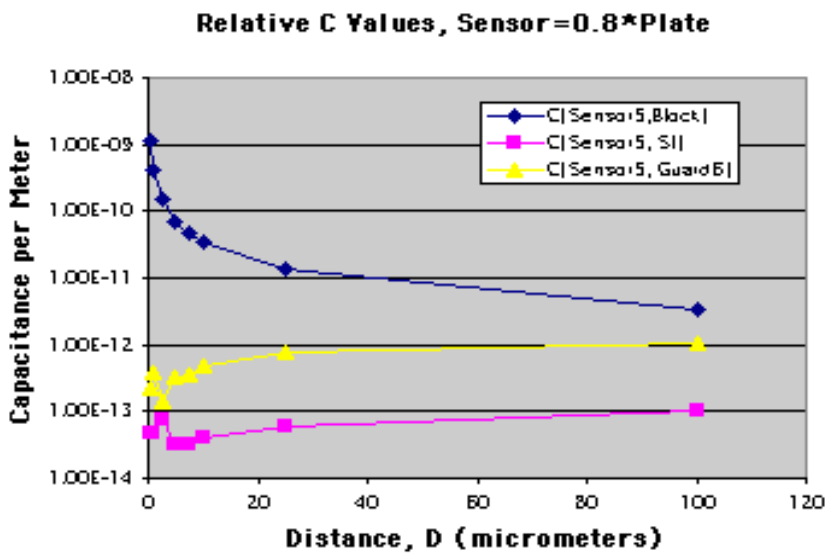


Fig 3.12 Plot showing typical capacitances with sensor factor =0.8

C[Sensor5, Block] represents the capacitance between sensor 5 and test block
 C[Sensor5, Si] represents the capacitance between sensor 5 and Silicon Substrate
 C[Sensor5, Guard6] represents the capacitance between sensor 5 and guard 6
 Distance, D is the distance between the test block and the sensor plates in microns

From these results, it is clear that a sensor scale factor of 1.1 is not consistent with extended cell sensing range. As we can see in the plots both guard and Si mutual capacitances become appreciable relative to the sensor and object capacitance, and therefore a significant part of the total sensor capacitance when the object is at large sensing distance. This large parasitic capacitance can be overcome by scaling of the sensor plate as indicated in the $f=1.0$ & $f=0.8$ plots. Based on the results obtained by the above simulations, a nominal scaling factor of 0.8 was adopted for subsequent simulations in this work unless otherwise specified. For this scaling factor, the coupling capacitance with the silicon substrate is insignificant and the coupling capacitance with the closest guard is on the order of magnitude of the sensor – object capacitance only at object distances of 50 micrometers and beyond.

Sensing the finger print valley depth which is given as 100-150 micrometers, will require even further suppression of this capacitance and other parasitic capacitances arising from neighboring cell elements. The total parasitic capacitance arising from all guards and neighboring shielding plates are taken into account in all the subsequent simulations performed.

Additional measures which were taken to suppress these parasitics include further reduction of ‘f’ in some cases and spacing the array with different ‘f’ for each cell (mixed array). But decreasing the sensor plate size reduces the capacitance between sensor and object, so care must be taken to see that these issues are balanced.

3.3.2 Sensor Cell Size Study

Initial simulations were being performed to see the impact of sensor cell size on the capacitance. While the model developed enables variation in guard size and left & right spacing, these values were held fixed at the values currently used for the 50 micrometer cell size. The following plots shows the simulation results for cell sizes of 50, 100, 200 and 300 micrometers. The cell size can be varied in the model as shown in the Fig 3.9, by which the size of underlying shield plate also increases or decreases

depending on the cell size. Calculating with chosen nominal factor between shield and sensor plates as $f= 0.8$, these cell sizes correspond to sensor plate/ shield plate ratios of 35.6/44.5, 75.6/94.5, 155.6/194.5, and 235.6/294.5 microns respectively.

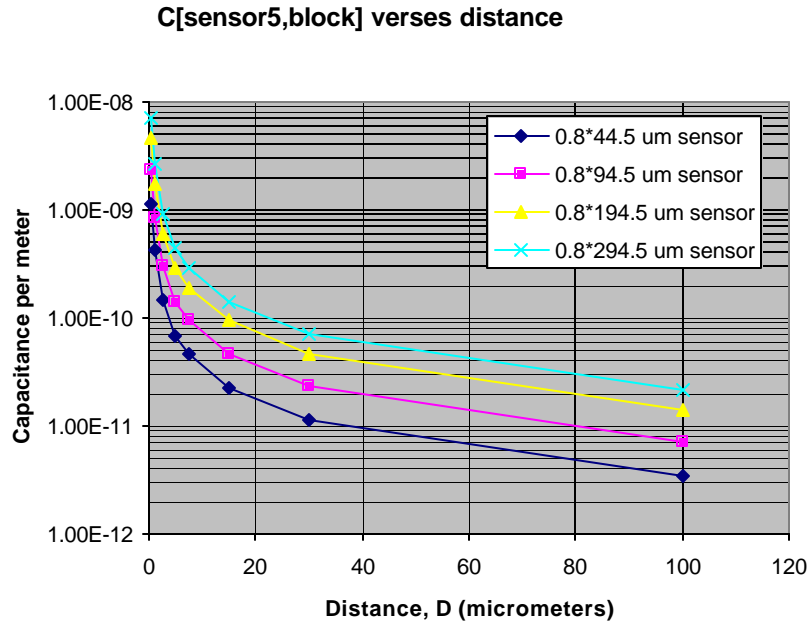


Fig 3.13 Linear Plot showing sensor to object capacitance with different cell sizes

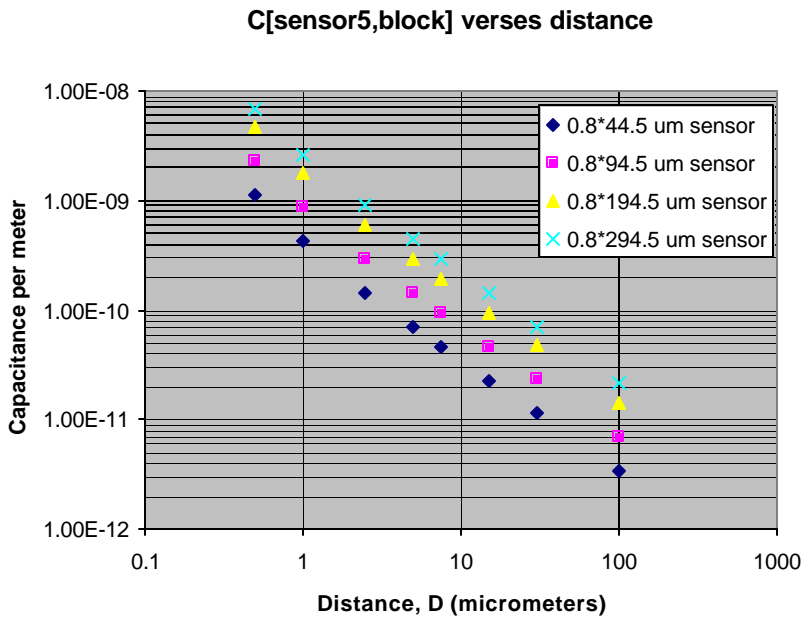


Fig 3.14 Distance shown in Logarithmic format for the above plot.

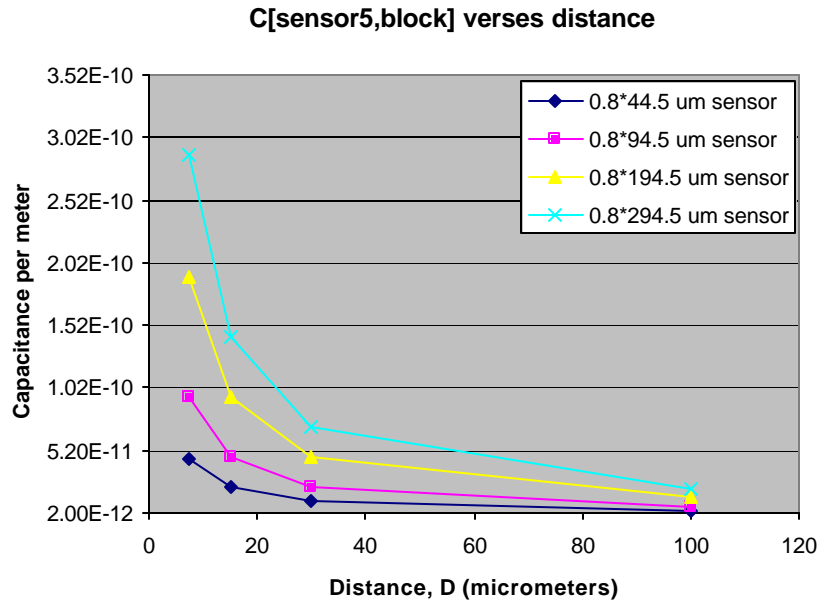


Fig 3.15 Expanded Linear Plot to see the difference in capacitance clearly.

In the above three plots, the first two show the simulation results for the intrinsic sensor-object capacitance, $C_{s5,block}$ in linear and log format for test object distances up to 100 micrometers. The last plot expands the scale of the linear plot in order to see the difference in capacitance at large distances from the sensor.

From the above results it is clear that the mutual capacitance between the sensor and the object under test will increase as we move towards larger cell (which has relative larger sensor) size. However, the intrinsic dependence of that capacitance on distance remains unchanged. As a result, for the large distances of interest here, the variation in capacitance remains the same but the values of capacitance may now move into a range which may be more readily detectable. Nevertheless, by using large sensors the resolution of the device decreases which is explored in further simulations.

The above three plots show *only* the sensor-object mutual capacitance as appropriate design measures have been taken in further work to reduce all parasitic capacitances to a level at least one order of magnitude beneath this primary capacitance.

3.4 Simulating with Virtual Test Objects

3.4.1 Testing the model with Trapezoid Object

The following are the results of the Veridicom sensor using a test object referred to here as the Virtual Test Object (VTO). This is a virtual version of what might be used as a structure (finger model) for sensor test. The dimensions and material parameters are described in the test objects chapter.

There are three types of simulations performed here: when VTO is in static mode, when VTO is in swipe mode, and to explore the vertical sensitivity of VTO which is placed again in static mode over the sensor model. The results of these models are in the following sections.

3.4.2 Static Mode

The VTO is placed over the sensor model statically with a maximum valley depth of 200 micrometers as described previously. This model is tested for the cell sizes of 50, 200 and 300 microns to test the vertical resolution of each sensor model with a fixed sensor plate factor of 0.8. The distance between the VTO and the sensor plates is kept less than 0.1 microns as shown in the following figures. This separation approximates contact. A gap is necessary because the model used during these simulations did not use a nitride film to encapsulate the sensor plate.

50 micron cell array

At this cell size, the ten cell 1-D sensor model spans only a single period of the VTO as shown in the Fig 3.16. An enlarged view of sensor model is shown in the following Fig 3.17. The simulation results are obtained for this model and plotted in the

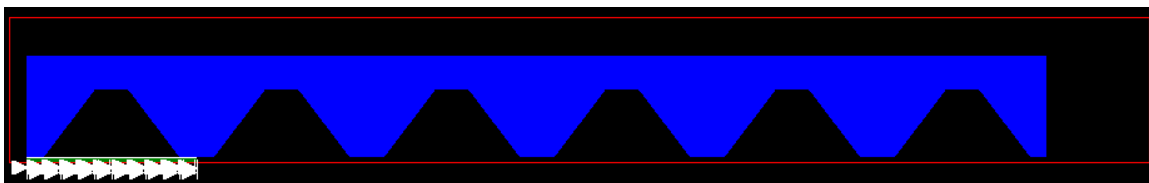


Fig 3.16 50 micron cell array with VTO in static mode

chart, Fig 3.18. The chart shows the individual capacitances between respective sensors and the VTO. For this 50 micron cell size the distance between the sensor and the object depth played a significant role, as expected. The capacitance value is very less and almost constant beyond 100 micron gap between object and the sensor. The total parasitic

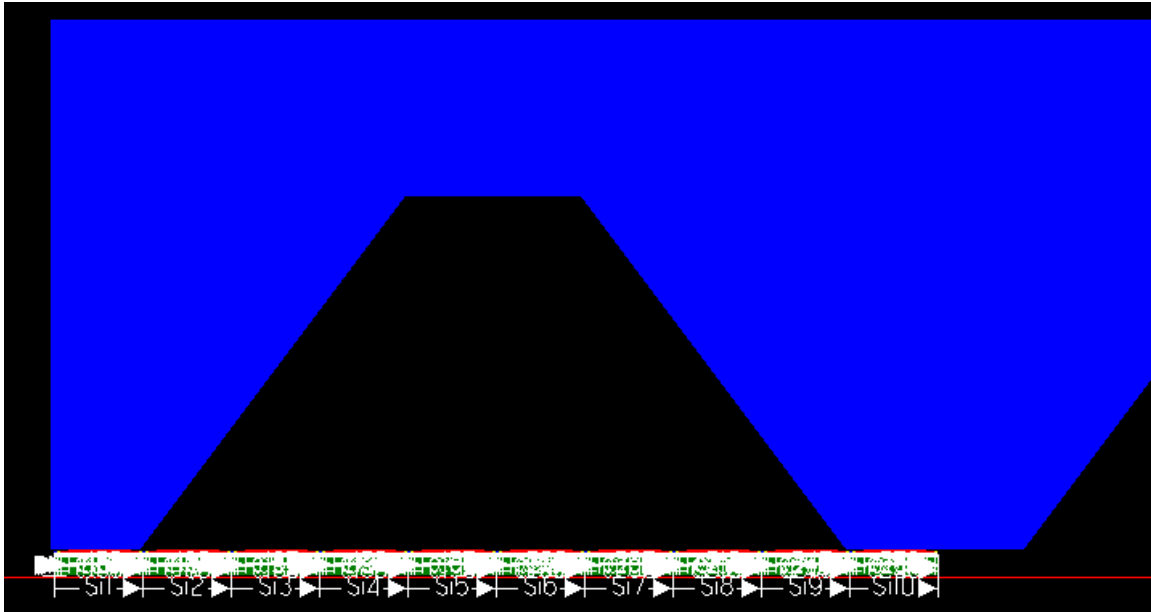


Fig 3.17 Enlarged view of 50 micron cell array covered by a single period of VTO

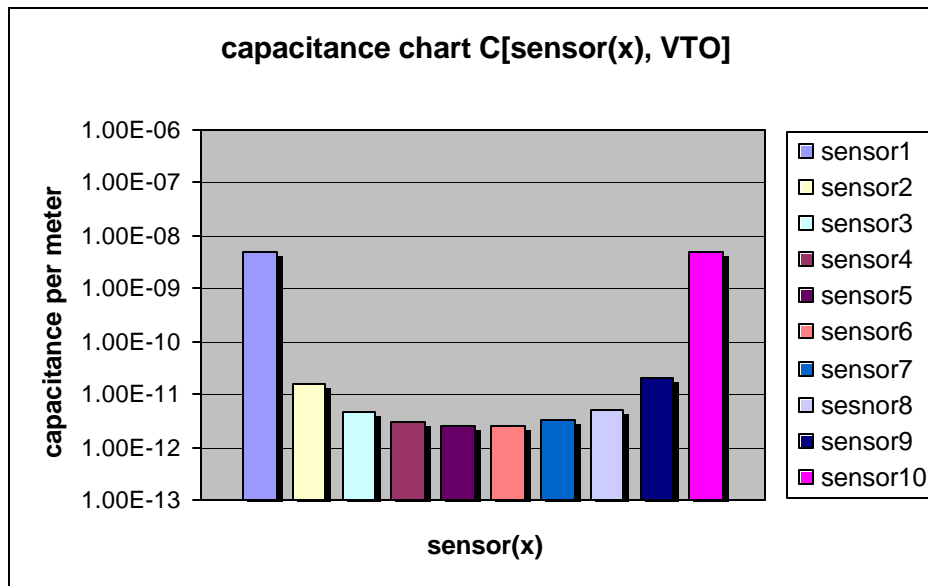


Fig 3.18 Logarithmic Chart for the sensor to object capacitance values

capacitance value is less than 10% of that of the capacitance between sensor and VTO when object is near to sensor plates. For sensor in contact with the object the Total Parasitic Capacitance is negligible, as for sensor 1 it is 7.44×10^{-14} where as, sensor1 to object capacitance is 5.09×10^{-09} and for sensor 2 the Total Parasitic Capacitance is 3.69×10^{-12} and to object it is 1.59×10^{-11} . For rest of the sensors which are covered by the valley part of the test object the total parasitic capacitance value is dominant and 10% more than the sensor to object capacitance.

200 micron Cell Array

The 200 micrometer cell array is covered by the VTO as shown above in the figure. Now each valley period is covered by two cells and therefore capacitance rise and drops are expected alternatively in the chart. The results are shown in the following chart, Fig 3.20.

With 200 micron cell size, results have changed significantly due to the large sensor plate size. Capacitance values band into two value ranges - one for when cells contact the structure, and the other for when they don't as appear in the chart. Note that no difference/structure is apparent in the low values representing cells in the recess regions irrespective of valley depth. The total parasitic capacitance value is less than 10% of that of the capacitance between sensor and VTO irrespective of object distance from the sensor plates. For sensor 3 which is in contact with the test object the total parasitic

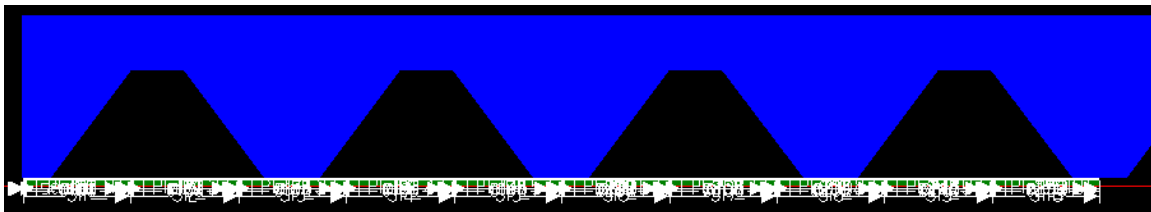


Fig 3.19 200 micron cell array with VTO in static mode

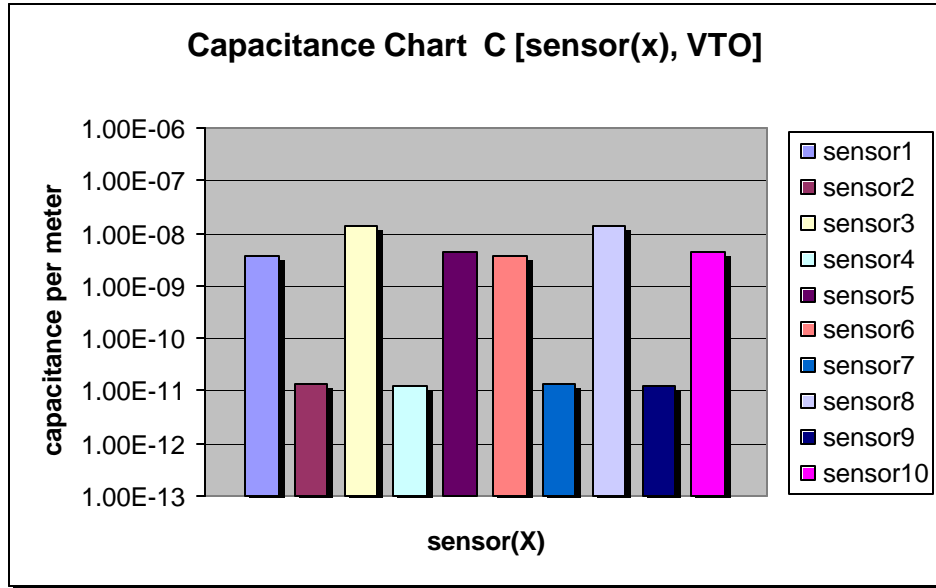


Fig 3.20 Logarithmic Chart for the sensor to object capacitance values

capacitance is 1.1×10^{-12} whereas the sensor3 to object capacitance is 1.4×10^{-08} and for sensor 4 which is exactly under a recess region the total parasitic capacitance is 3.96×10^{-12} whereas the capacitance between the sensor 3 to object is 1.26×10^{-11} . There is noticeable capacitance variation from sensor to sensor as a change in the structure of the object is covered by single sensor as expected.

300 micron Cell Array

This simulations were done expecting that large sensor plate gives still better performance, the sensor model width is now almost equal to VTO size as shown in the Fig 3.21. The results for this 300 micron cell size are almost similar to 200 micron cell size except that alternative capacitance rise and drops. The total parasitic capacitance value is absolutely less than 10% of that of the capacitance between sensor and VTO



Fig 3.21 300 micron cell array with VTO in static mode

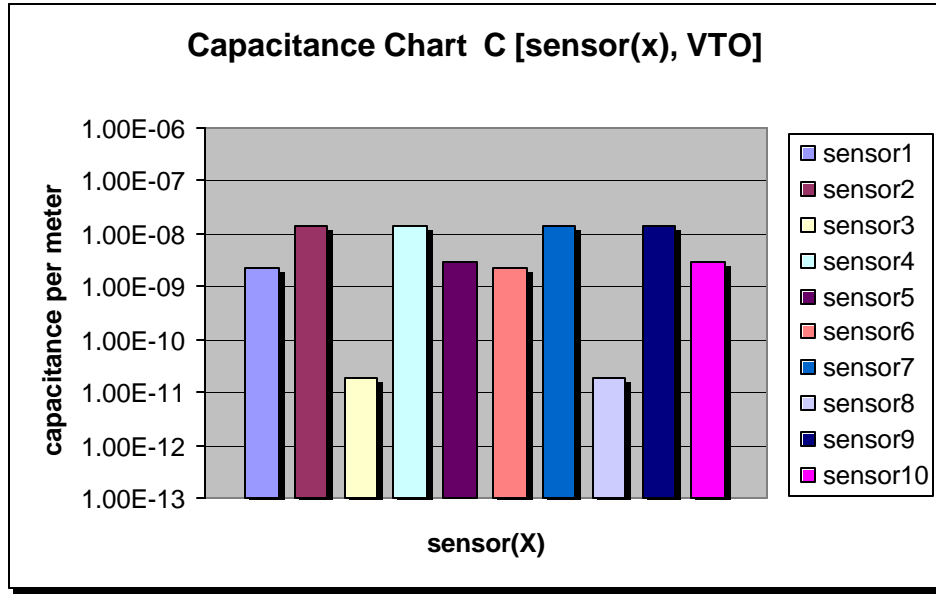


Fig 3.22 Logarithmic Chart for the sensor to object capacitance values

irrespective of object position on the sensor plates. The parasitic capacitance even when the sensor is exactly under a recessed region is 1.39×10^{-12} whereas the capacitance between the object and the same sensor is 1.92×10^{-11} .

While as expected, the object-sensor capacitance has risen for these large sensors, resolution of the valley sidewall and ridge structure apparent in Fig 3.18 has been lost.

3.4.3 Swipe Mode

Simulations are performed to verify the results of the model when the sensor is operated in SWIPE mode. The same test object which was used in previous model is used here with an exception that the VTO is moved on the sensor plates to get swiping effect on the sensor model.

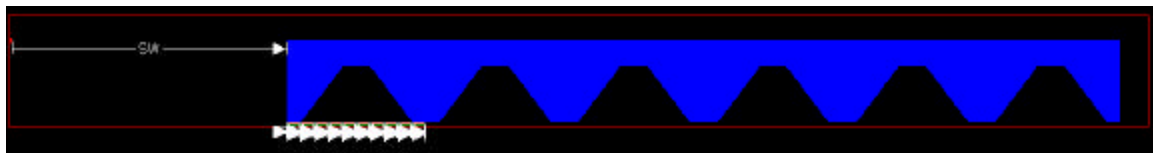


Fig 3.23 VTO in swipe mode on the sensor model

The reference point taken is the leading edge of sensor 5 and all the capacitance values are taken for sensor 5. The simulation setup is shown in Fig 3.23 and the test cases here are again for 50, 200 and 300 micrometer cell sizes with a fixed sensor plate factor of 0.8. The distance between the VTO and the sensor plates is kept less than 0.1 microns as before. The VTO is swiped for one complete period starting from a ridge with a step size of 75 microns and ending at the next ridge with reference to sensor 5. The position of object in each step during one complete period on 50 micron cell model is shown in Fig 1 of Appendix-B. The step size, starting point and the position of the object is same for all three cases which are described below.

50 micron Cell Array:

The following chart in Fig 3.24 shows the capacitance value between the reference sensor and the test object and total parasitic capacitance calculated at eight different positions in a 500 micron complete period of swiping the test object.

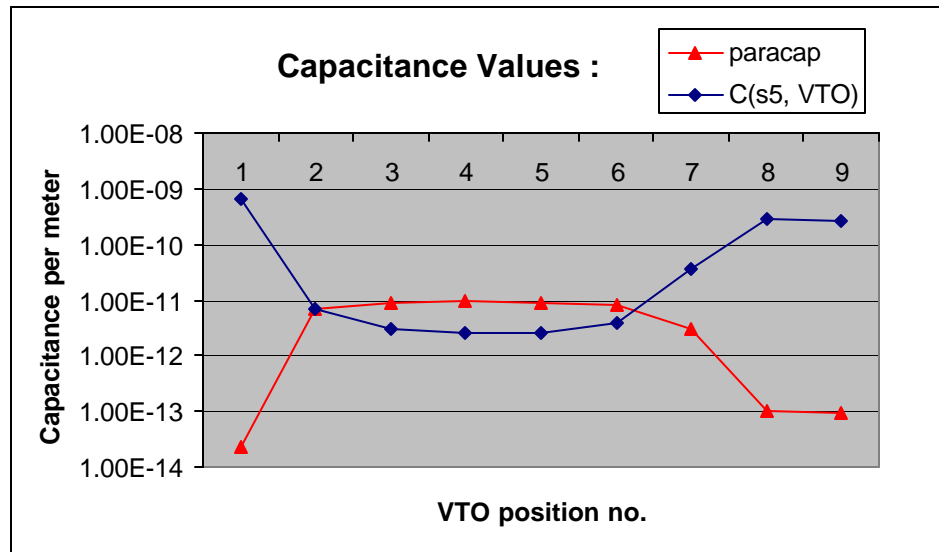


Fig 3.24 Logarithmic Chart for the sensor5 to object capacitance for 50 micron cell size
 $C(s5, VTO)$ = Capacitance between sensor 5 and at various positions of test object in swipe mode.
 Paracap=Total Parasitic Capacitance of sensor 5 at the same positions of test object.

Total parasitic capacitance is given by,
 $C(s5,p3)+C(s5,p4)+C(s5,p6)+C(s5,p7)+C(s5,g4)+C(s5,g5)+C(s5,g6)+C(s5,g7)+ C(s5,Si)+ C(s5,s4)+ C(s5,s6)$

The variation in capacitance value is very large, however it takes on two extreme point values (ridges and valleys) with an abrupt transition as shown in the figure above. The capacitance value is found to be very much less when the sensor plate completely lies in the valley region, and the parasitics especially caused by guard5 and guard6 are dominant. The object capacitance plot is almost a mirror image of the total parasitic capacitance plot.

200 micron Cell Array:

The following plot in Fig 3.25 shows the capacitance values of sensor 5 of 200 micron cell array at the same eight different positions as described above.

With 200 micron cell size, results have changed significantly as expected. Capacitance is increased in the valley region. The total parasitic capacitance value is almost less than 10% of that of the capacitance between sensor and VTO irrespective of position of the object from the sensor plates. At VTO position number 5 in the plot, the capacitance between the sensor 5 and test object is 1.27×10^{-11} and total parasitic capacitance is 4.04×10^{-12} . The parasitics are held almost constant for all positions of VTO as sensor plate size is increased.

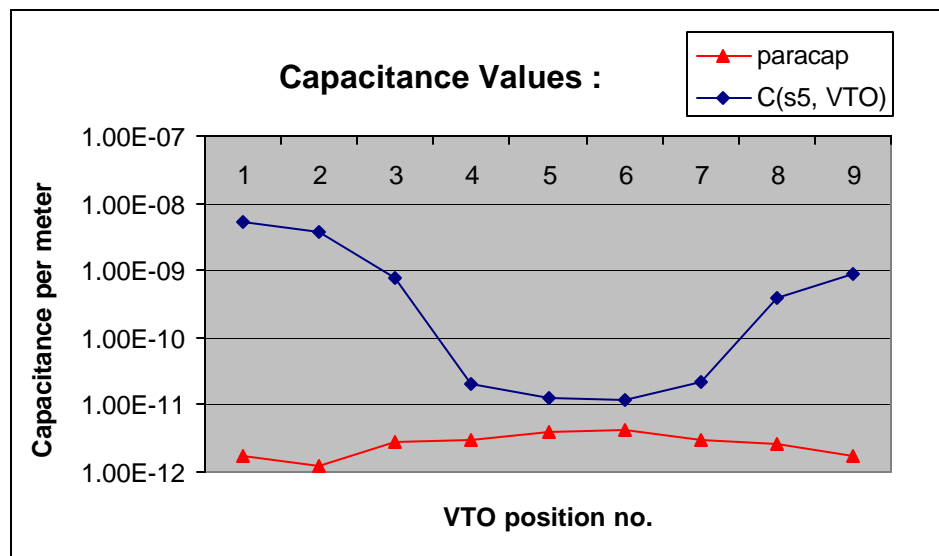


Fig 3.25 Logarithmic Chart for the sensor5 to object capacitance for 200 micron cell size

300 micron Cell Array:

The following plot shows the capacitance values of sensor 5 of 300 micron cell array at the same eight different positions as described above.

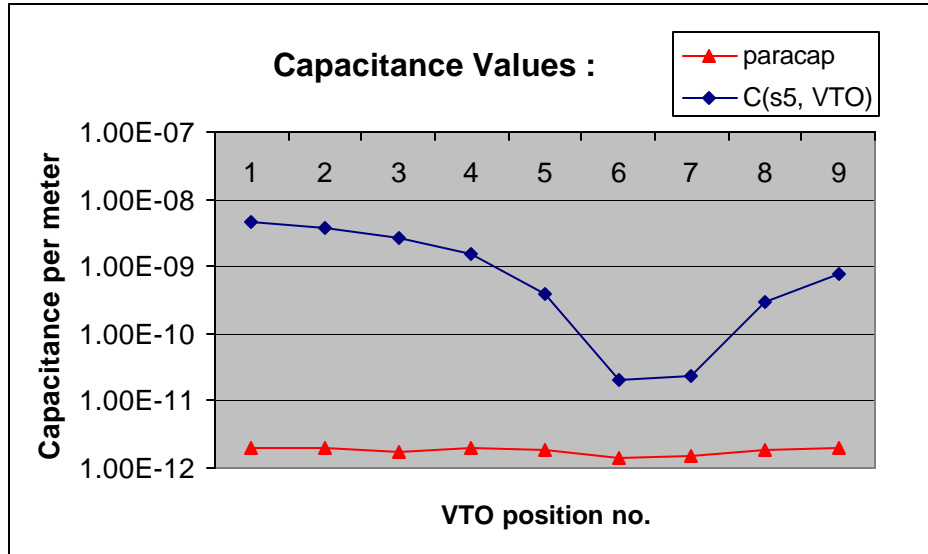


Fig 3.26 Logarithmic Chart for the sensor5 to object capacitance for 300 micron cell size

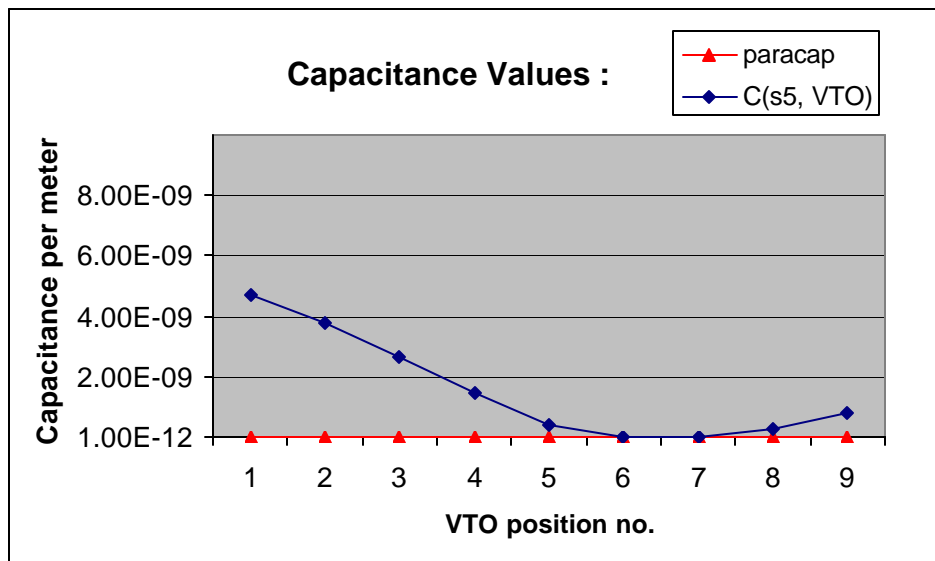


Fig 3.27 Linear Chart for the sensor5 to object capacitance for 300 micron cell size

The results for this 300 micron cell size trend similarly to 200 micron cell size results. The total parasitic capacitance value is less than 10% of that of the capacitance between sensor and VTO irrespective of position of test object from the sensor plates. At VTO position no. 6 where the test object lies exactly under a valley region, the capacitance between the sensor5 and VTO is 2×10^{-11} whereas the total parasitic capacitance is 1.39×10^{-12} . The large parasitic effect of guards 5 & 6 is negligible in 300 micron cell size. However, as stated earlier, resolution of ridge feature is lost.

Conclusions:

In swiping mode the large sensor plates are helping to raise the capacitance curve over the parasitics as the sensor experiences one of the ridges at all times, and it is also maintaining the parasitic curve to be constant through out the swiping period. However, large sensors lost the resolution of ridge feature. To maintain resolution, mixed sizes of cells can be used in an array. These arrays provide high capacitance measurement with large sensors and reasonable resolution with small sensors at the same time. The mixed arrays are investigated later in the chapter.

3.4.4 Change in Valley Depth or Vertical Sensitivity of Sensor Model

The above two simulations used the VTO which has a maximum valley depth of 200 microns. In order to explore the sensor model sensitivity over the farthest point on the test object, the maximum valley depth point has been reduced to 10 microns in steps. The cell size of 200 micrometers is used for this experiment.

The following Fig 3.28 shows the modified virtual test objects which have varied valley depths as described. The capacitance value between the reference sensor and the test object is calculated for five different values of maximum valley depth (VD) of the test object. The sensor-object capacitance is calculated at three positions of the test object for each Valley Depth which are under a ridge, valley, and ridge consecutively. The reference sensor is taken sensor 5.

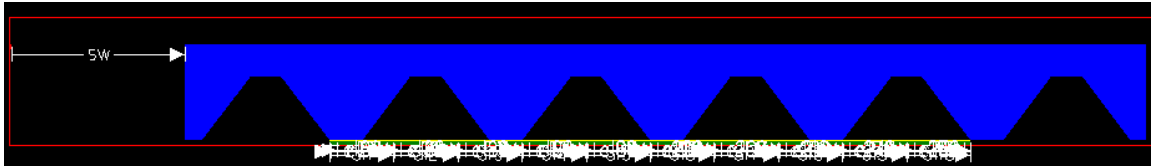


Fig 3.28(a) Virtual Test Object with Maximum Valley Depth of 200 microns which was used before



Fig 3.28(b) Virtual Test Object with Maximum Valley Depth of 100 microns

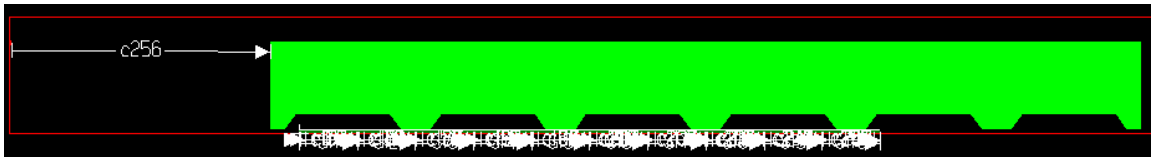


Fig 3.28(c) Virtual Test Object with Maximum Valley Depth of 50 microns



Fig 3.28(d) Virtual Test Object with Maximum Valley Depth of 25 microns

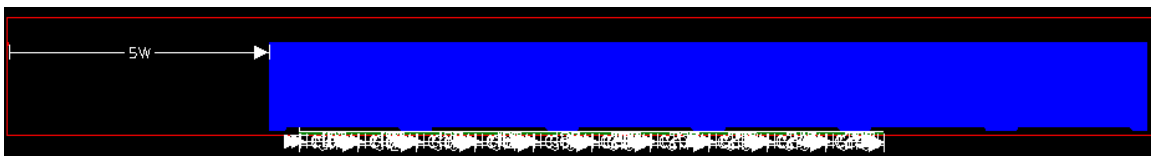


Fig 3.28(e) Virtual Test Object with Maximum Valley Depth of 10 microns

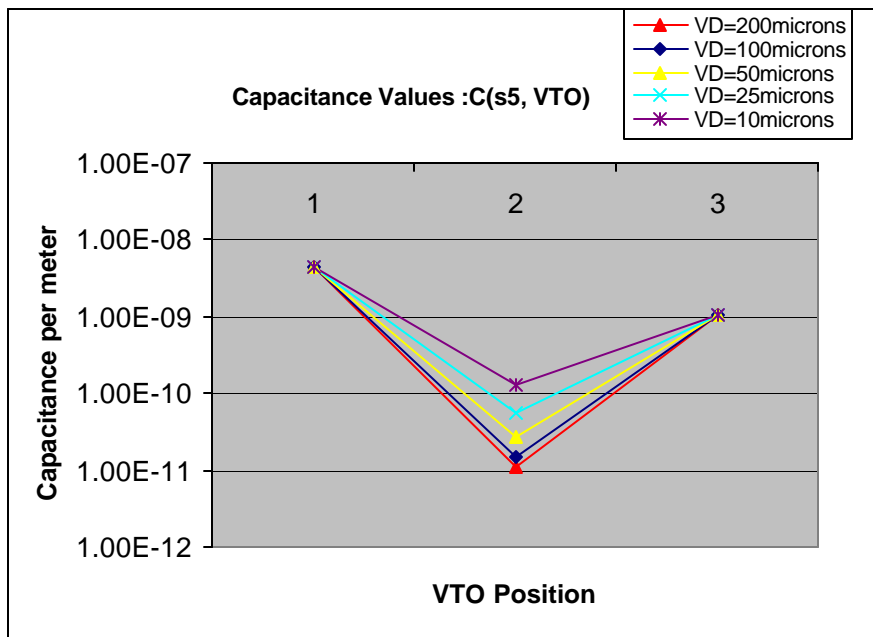


Fig 3.29 Comparing the different capacitance values in logarithmic plot

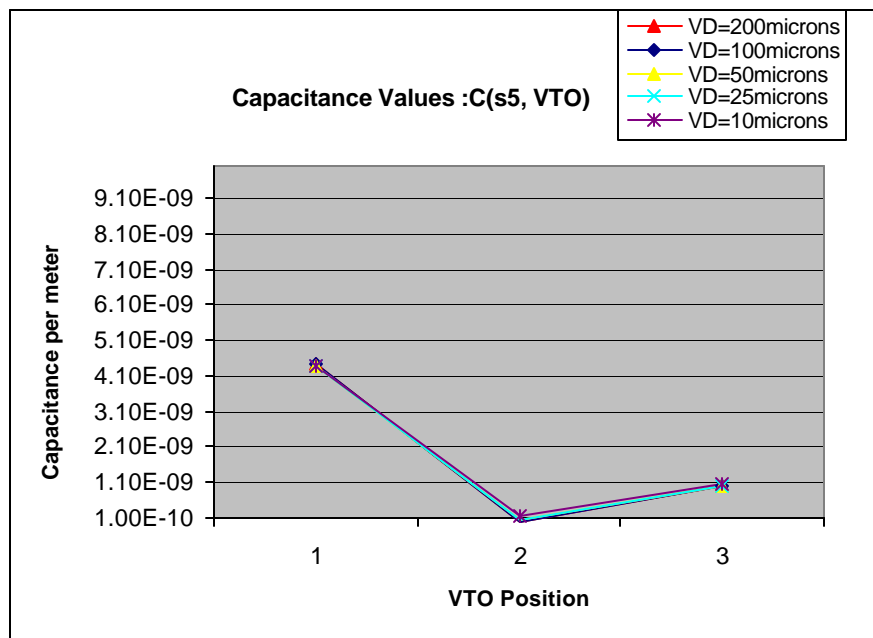


Fig 3.30 Comparing the different capacitance values in linear plot

The charts in the Fig 3.29 and 3.30 compare the capacitance value between reference sensor and the test object of different maximum valley depths. As said before the VTO positions 1,2 and 3 on x-axis specifies consecutive ridge, valley and ridge of the test object respectively.

There is a marked improvement in the capacitance under a valley point in each step when the valley depth is reduced. From the charts exactly 10% improvement in the capacitance is observed when valley depth is changed from 200 microns to 10 microns. At 200 micron valley depth the sensor is able to capture the capacitance though it is less in value.

3.5 Encasing the sensor plates

The initial model developed has the sensor plate on top of the nitride rather than encased in or coated with it. The physical issues such as chemical contamination, electrostatic discharge and scratching of the surface are the main concern in embedding this model.

In order to avoid the above possible device degrading agents, dielectric layers are inserted around the sensor plate, in other words the sensor plate has been embedded in a protective case as shown in the Fig 2 of Appendix-B.

The dielectric material used for encasing the sensor plates is Silicon Nitride which is a high resistive and protective material.

Effect of upper dielectric on the sensor to object capacitance

The effect of this nitride protective coating is tested by performing two type of simulations, one with nitride protective coating and another without it. The following plot in Fig 3.31 shows the results of these simulations. The model has used typical parameters as, sensor plate factor 0.8, sensor cell size 200 microns, test object is rectangular block which is shifted over the model to 100 microns distance.

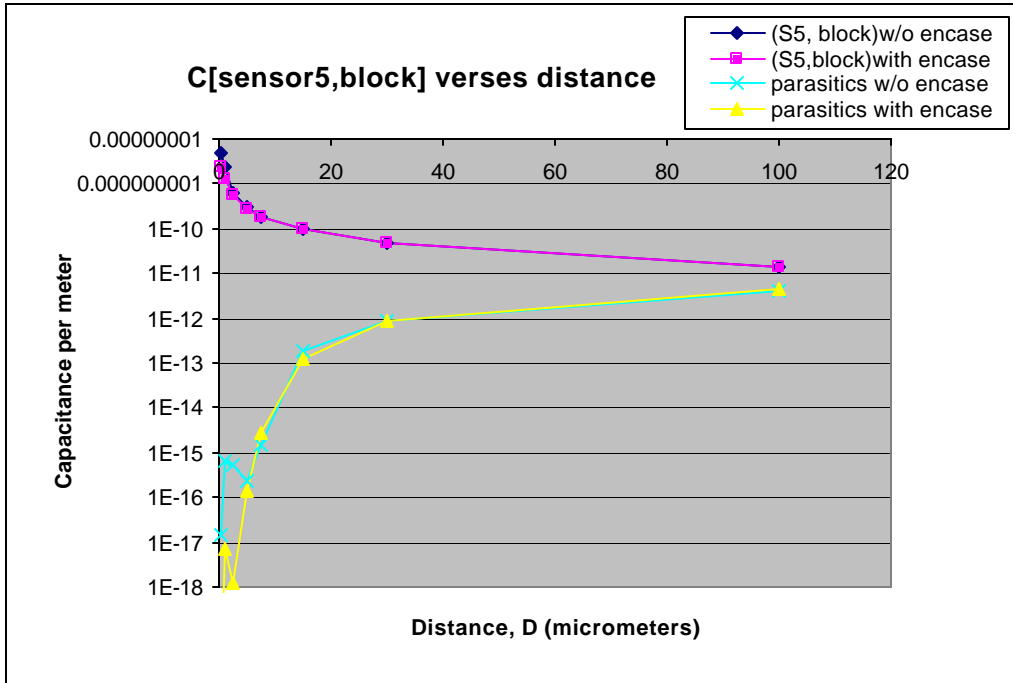


Fig 3.31 Logarithmic plot which compares the nitride coating effect

Total parasitic capacitance is given by,

$$C(s5,p3)+C(s5,p4)+C(s5,p6)+C(s5,p7)+C(s5,g4)+C(s5,g5)+C(s5,g6)+C(s5,g7)+ C(s5,Si)+ C(s5,s4)+ C(s5,s6)}$$

From the graph, we can say that there is virtually no effect of the nitride protective coating on the capacitance matrix. Given all device designs are embedded in a nitride protective coating, all the further simulation work has been done using this encasing model unless specified otherwise.

3.6 Vertical Lip (Well Structure)

In order to suppress the major contributor of parasitic capacitance, which is arising from the sensor plate to the guard grids, and silicon substrate an edge is being added on either side of the underlying shield as shown in Fig 3.32 below and the simulation geometry is shown in Fig 3 of Appendix-B.



Fig 3.32 A well-structured underlying shield plate under each sensor

The vertical edges added here is the modification to underlying straight shield plate that now looks like a well in structure. The vertical lips are designed such as to get variation in plug height from 0 microns to 0.5 microns. Simulations are done with change in plug height factor, and change in sensor plate size.

3.6.1 Theoretical Expectations

This well structure is made expecting that the field lines going onto the neighboring cells will terminate on the vertical lips. As underlying shield is following the sensor plate voltage, all the parasitics which are stopped by the vertical edges are expected to be suppressed.

The underlying shield, therefore acts as a well in which sensor plate is sitting, strictly speaking the sensor plate lies over and in between the vertical edges. The sensor plate factor is going to decide the advantage of having these edges. With 0.5 plate factor the sensor plate would be half of that shield plate and hence the field lines will drop off within the well and the parasitic capacitance will decrease. The model which has maximum plug height and minimum sensor plate factor is expected to give good results if other factors are not considered.

3.6.2 Testing and analyzing the model

The vertical lip model is tested with both trapezoid and rectangular block objects. Initially, it is tested to see the performance of plug height factors of 0.5 and 1.0 which

are half and full(maximum) vertical edges respectively, in suppressing the parasitic capacitances. The sensor plate size factor by default is 0.8 with a cell size of 200 micrometers and the test object is trapezoid used in swipe mode.

The following plot in Fig 3.33 shows the capacitance values when the vertical edge is at its maximum height in this model, i.e., plug height factor =1.0 The test object is operated in swipe mode to get the capacitance values at various points of ridge and valley of trapezoid. The ten positions on x-axis shows the successive position of test object from one ridge to subsequent ridge on reference sensor 5. Therefore the capacitance is decreased as sensor 5 is under a valley point and it is increased as sensor is encountered by a following ridge.

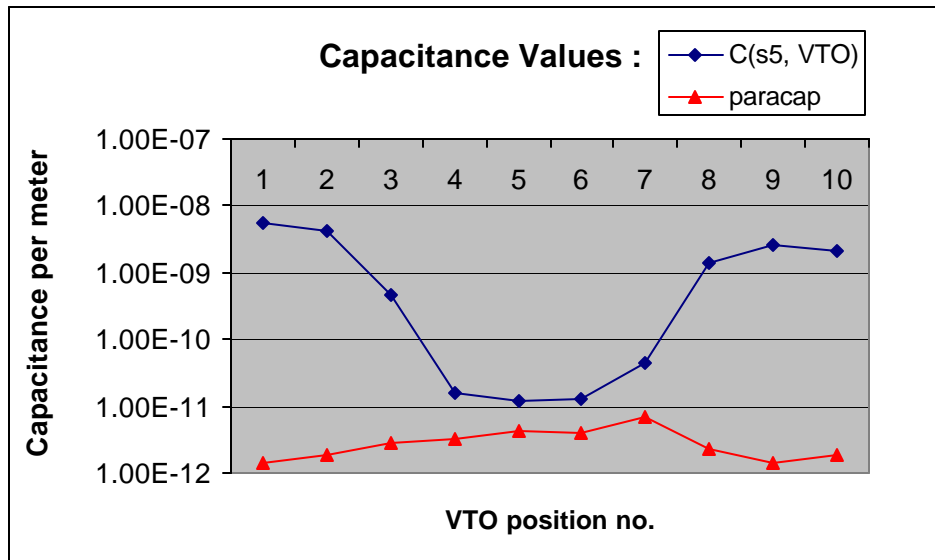


Fig 3.33 Logarithmic Plot showing the capacitance values for plug height factor=1.0

C(s5, VTO) is the capacitance between sensor 5 and the test object.

$$\text{Paracap (Total Parasitic Capacitance)} = C \{ (s5,p4) + (s5,p6) + (s5,rlip4) + (s5,llip6) + (s5,g4) + (s5,g5) + (s5,g6) + (s5,g7) + (s5, Si) + (s5, s4) + (s5, s6) \}$$

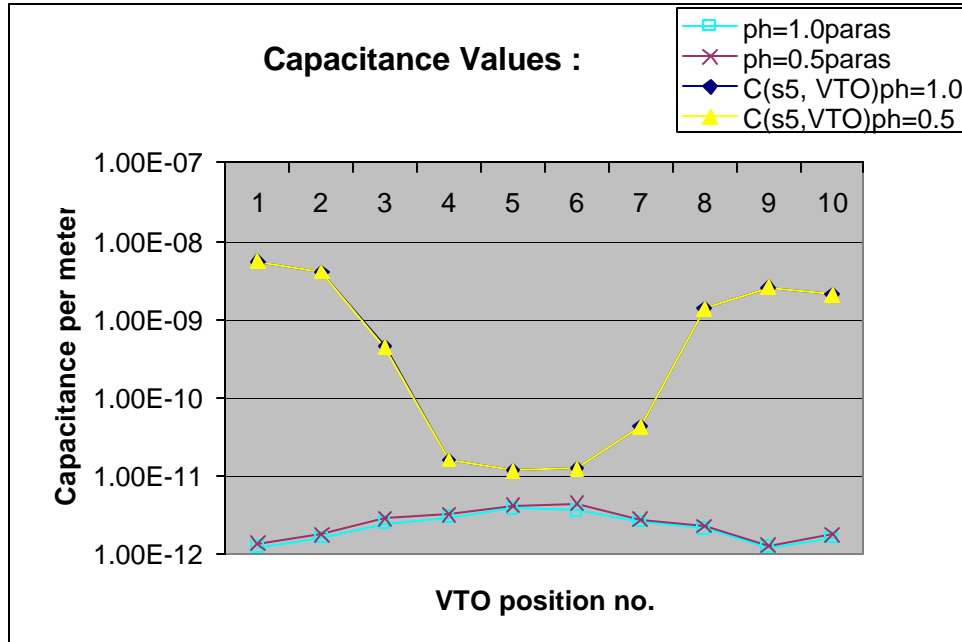


Fig 3.34 Logarithmic Plot comparing the capacitance values for plug height factor=1.0 and 0.5

“ph=1.0paras” denotes the total parasitic capacitance when plug height factor is 1.0

“ph=0.5paras” denotes the total parasitic capacitance when plug height factor is 0.5

“C(s5,VTO)ph=1.0” is the capacitance between sensor 5 and test object when plug height factor is 1.0

“C(s5,VTO)ph=0.5” is the capacitance between sensor 5 and test object when plug height factor is 0.5

The plot in Fig 3.34 shows the capacitance values of both plug height factors of 1.0 and 0.5. For comparing the plug height factors, they are drawn together here. The effect of vertical lip height on the capacitance is very less as the two curves are almost overlapping.

Testing the model with Rectangular Object

The vertical lip performance is tested by comparing the capacitance values with that of when vertical lip is not present i.e., plug height factor =0. Two sensor plate sizes are tested here of factor 0.8 and 0.5. The reference in this case again is taken as sensor 5. The results of sensor plate factor 0.8 are shown in the following Fig 3.35. If we look at the values of two models, i.e., when the sensor plate is with in vertical lips or without

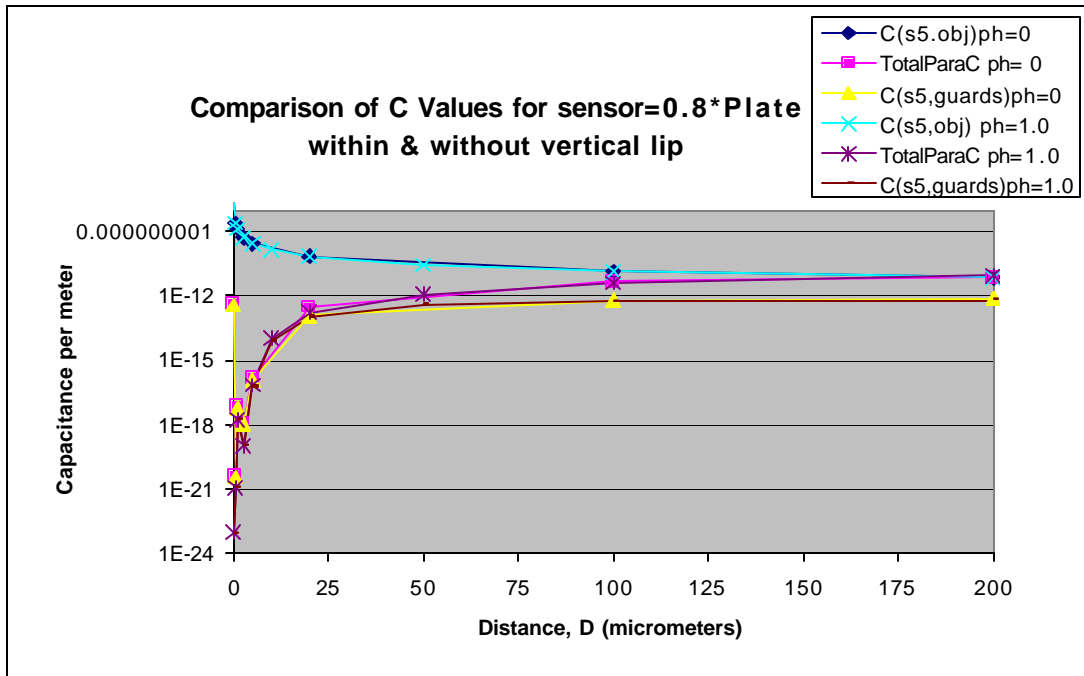


Fig 3.35 Logarithmic Plot comparing various capacitance values for plug height factor=0 & 1.0

ph = plug height factor

$$\text{TotalParaC (Total Parasitic Capacitance)} = C \{ (s5,p4) + (s5,p6) + (s5,rlip4) + (s5,llip6) + (s5,g4) + (s5,g5) + (s5,g6) + (s5,g7) + (s5, Si) + (s5, s4) + (s5, s6) \}$$

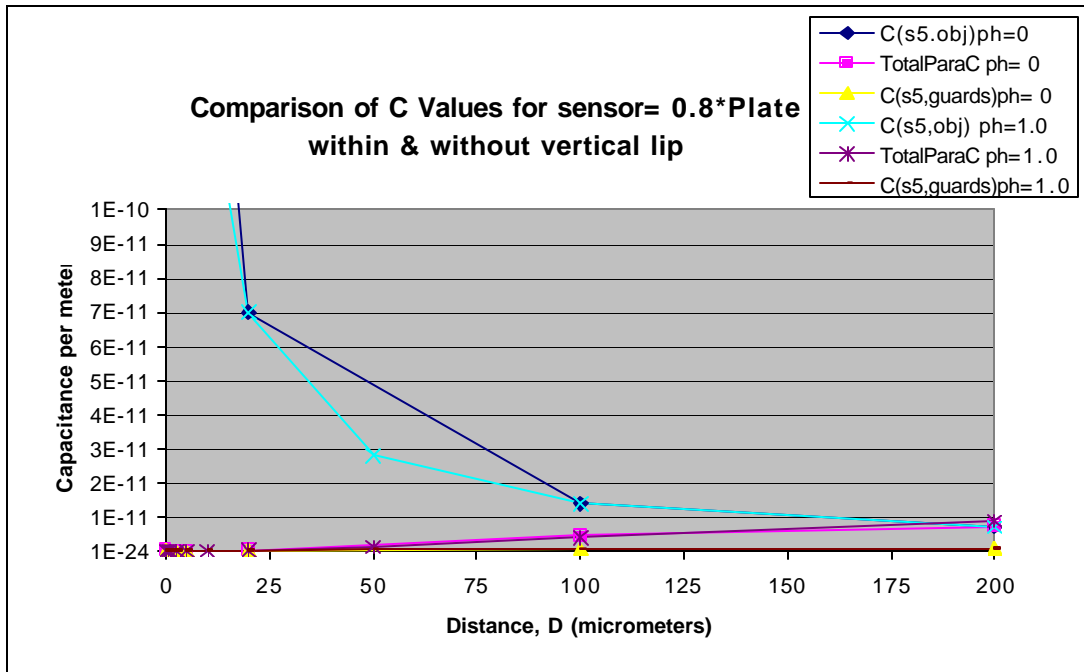


Fig 3.36 Linear Plot comparing various capacitance values for plug height factor=0 & 1.0

vertical lips, there is almost no difference between the sensor to object capacitance and also in between the sensor to guards capacitance. At a typical sensor to object distance of 100 micrometers, the capacitance between the sensor and guards when the sensor plate is within the vertical lips is 5.34×10^{-13} and without the vertical lips it is 6.41×10^{-13} . In other words, there is about 1% improvement observed when the sensor plate is within the well structure. If we look at the total parasitic capacitance when the sensor plate is within the vertical lips, it has a value of 3.91×10^{-12} and without the lips it is 4.54×10^{-12} . The same values are shown in linear plot in the Fig 3.36.

So for larger sensor plate factors where the flux lines will jump over the vertical edge from the sensor plate, this well structure will not help significantly. If we decrease the sensor plate factor, balancing against sensing area, the effect of vertical lips might be fruitful. So next, the lower sensor plate factor of 0.5 is tested and the results are shown in the following Fig 3.37.

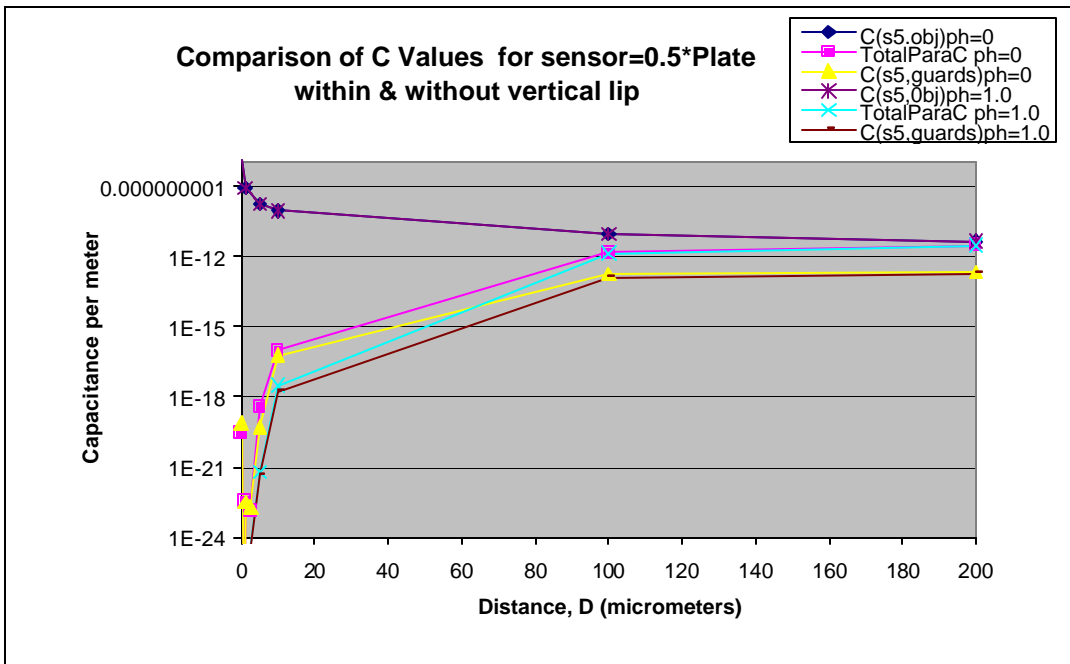


Fig 3.37 Logarithmic Plot of sensor plate factor 0.5 comparing plug height factors 0 & 1.0

Comparing the results with and without vertical lips as shown in above diagram, at 100 micrometer sensor to test object distance, there is not a good improvement in suppressing the parasitic capacitance by vertical lip edges. But, at small distances up to 100 micrometers there is a marked improvement observed. At a typical object distance of 10 micrometers, the capacitance between the sensor and guards when the sensor plate is within the vertical lips is 1.68×10^{-18} and without the vertical lips it is 6.01×10^{-17} . In other words, guards capacitance is suppressed approximately by 15% with well structured shield plate. If we look at the total parasitic capacitance when the sensor plate is without the lips it is 9.71×10^{-17} and when it is within the vertical lips, it has a value of 3.01×10^{-18} which is more than 15 % reduction in total parasitic capacitance.

Finally, it is observed that up to 100 micron object distance, these vertical edges have suppressed more than 10% of total parasitic capacitance. The same plot in linear form is shown in Fig 3.38.

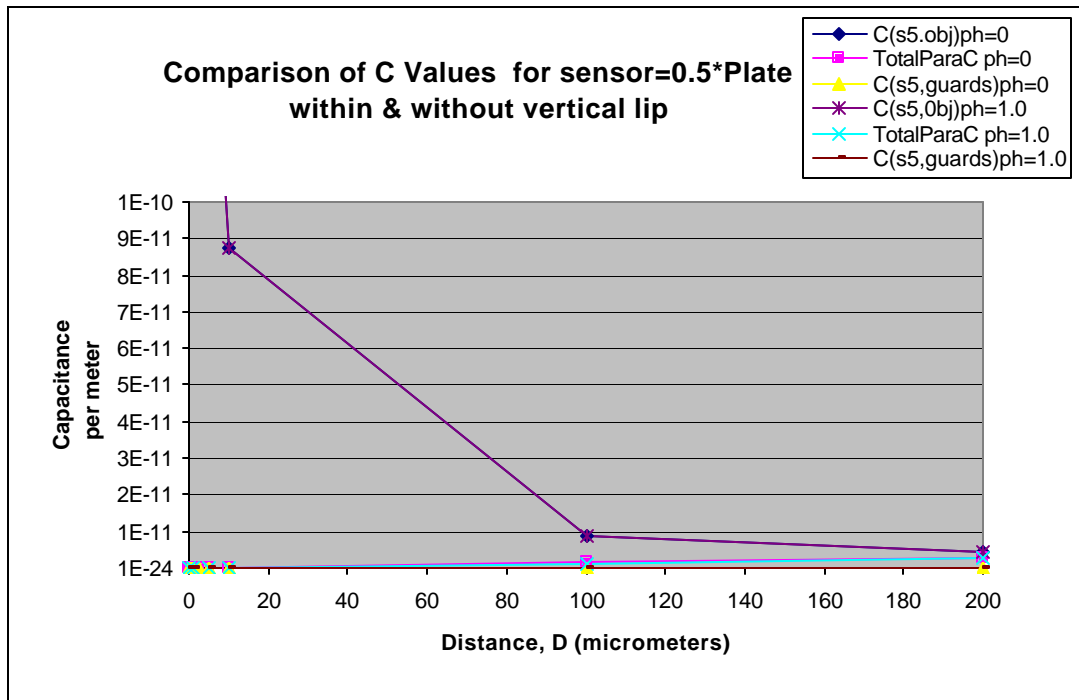


Fig 3.38 Linear Plot of sensor plate factor 0.5 comparing plug height factors 0 & 1.0

3.6.3 Approach suggested

From above results, the sensor plate size is going to play an important role in well structure models. Rather than just having vertical edges on shield plates, in which the sensor plate just lies over the edges, the term ‘well structure’ would be completely defined if the sensor plate is brought down into it. Then the field lines would not as readily cross the vertical lip heights. It has to be seen, how deep the sensor plate could be brought into the well with the same sensing sensitivity over the dielectric. The vertical lip edge height also is an issue to be considered.

These issues can only be resolved with consideration of the deposition processes forming the thin films and the effects on topography which may effect the scratch resistance of the device.

3.7 Electro Static Discharge

The process of Triboelectric generation, which is defined as transfer of electrons from the atoms on the surface, will take place when friction and separation occurs between materials. The resulting imbalance of electrons is called an electrostatic charge, because it tends to remain at rest or static unless acted upon by an outside force.

Materials with an imbalance of electrons will return to a balanced state when possible. When this happens rapidly, a zap or spark associated with rapid electrostatic discharge which is usually called ESD will take place. We may feel these sparks if the discharge that occurs is more than 3,000 Volts. Electrostatic discharges below this level cannot be sensed by human but may still be lethal to electronics and associated semiconductor devices[14].

3.7.1 Controlling the ESD

Amongst the various ESD controlling procedures, the primary method of control is to ground (bringing to same potential) all conductors that come in contact or near

proximity to the electronic devices. Grounding works only on conductors, it simply means that we make all conductors together at a common point so that electrostatic charges will flow from conductors to a common point and will therefore end up at same potential. One of the conductors we must ground here in our work is the human body[15].

3.7.2 ESD Grounded Grid

The electric properties of an ESD grid will play an important role in controlling the electrostatic discharge. An ESD grid will be either electrically conductive or dissipative, which means that the grid will conduct a charge when grounded. The difference in conduction and dissipation is defined by the materials resistance, which effects the speed of the discharge. By definition a conductive material has a surface resistivity of less than $1 \times 10^5 \Omega / \text{sq.}$, and a dissipative material is greater than $1 \times 10^5 \Omega / \text{sq}$ but less than $1 \times 10^{12} \Omega / \text{sq}$. Anything with a surface resistivity greater than $1 \times 10^{12} \Omega / \text{sq}$ is considered to be insulative and will essentially not conduct charges[15].

3.7.3 Effect of ESD Ring on the model

In the current devices, the exposed part of the sensor chip is surrounded by an external ESD ring as shown in Fig 3.1, to ground the human body when he places his finger on the chip. Though this ESD ring is placed for electrostatic discharge path, it is contributing towards parasitic capacitance. To test the external ESD ring effect on the capacitance values, the model is tested with two types of virtual ESD rings viz., a rectangular block and a trapezoid block. Two heights of this blocks are taken and tested the model.

Rectangular ESD Ring

A rectangular block has been used as a grounded ESD ring to control the electrostatic discharge. In this model the ring is placed on Si at left of the model as shown in the Fig 3.39 and 3.40. The Si is continuous between the ring and the model.

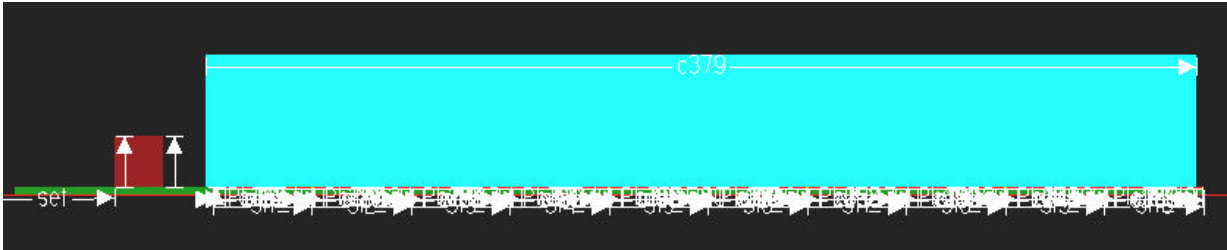


Fig 3.39 ESD Model with rectangular grounded ring of height 100 microns

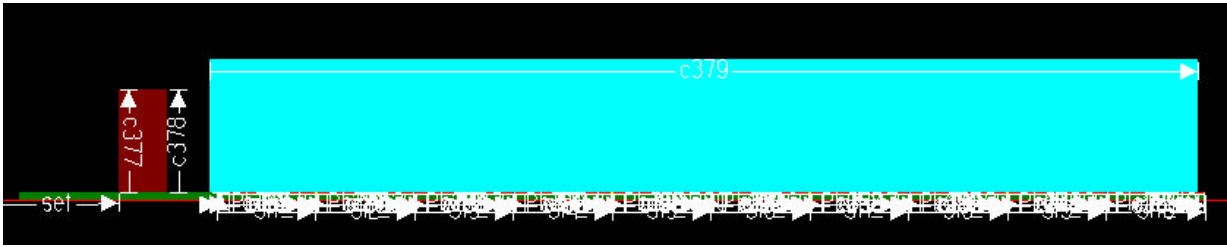


Fig 3.40 ESD Model with rectangular grounded ring of height 200 microns

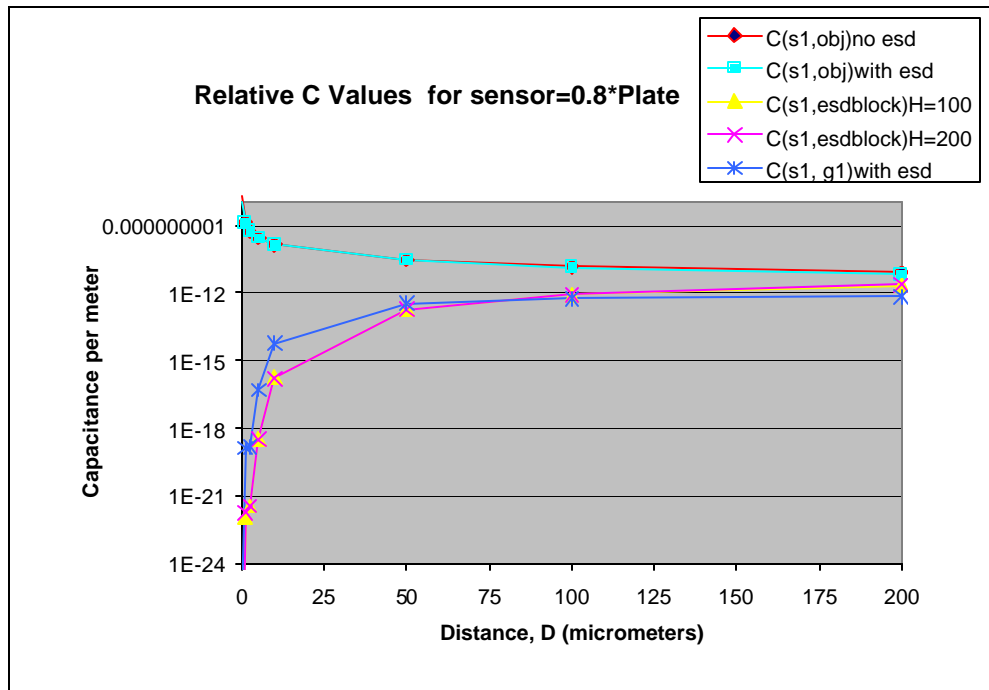


Fig 3.41 The logarithmic plot showing the capacitance values with and without ESD ring

“C(s1,obj)no esd” is the capacitance between sensor 1 and test object when there is no esd grid.
“C(s1,obj)with esd” is the capacitance between sensor 1 and test object when there is esd grid.
“C(s1,esdblock)H=100” is the capacitance between sensor 1 and esd block of height 100 microns.
“C(s1,esdblock)H=200” is the capacitance between sensor 1 and esd block of height 200 microns.
“C(s1, g1)with esd” is the capacitance between sensor 1 and guard 1 in the presence of esd grid.

The ESD ring of heights 100 microns and 200 microns are used. The ring is placed 100 microns away from the model. The effect of rectangular ESD ring on the model can be seen by comparing the results with that of the model which has no esd ring. The simulation results of this model are plotted in the Fig 3.41 along with the results of the model, which has no esd ring.

From the plot we can observe that there is little effect of the esd block on the capacitance between sensor and test object when the object is within sensing range. The capacitance of sensor1 to guard1 is more than the capacitance of esd block to sensor1 when the test object is below 100 micron distance. But when the test object is more than 100 microns far from the sensors the capacitance of esd grid is dominating. The height of the esd ring makes no difference in the capacitance values.

The esd ring effect is reflecting on total parasitic capacitance when it is 100 microns distance away from the model and the test object is 100 microns away from the sensor model.

Trapezoid ESD Ring

The trapezoid block is just like the previous one but the top side is just tilted as shown in Fig 3.42 and 3.43 in order to reduce the effect on total parasitic capacitance and more closely approximate the ESD ring geometry used in the current package. Again the ESD ring heights are taken as 100 and 200microns and used in the simulations and it is placed 100 micron distance away from the model.

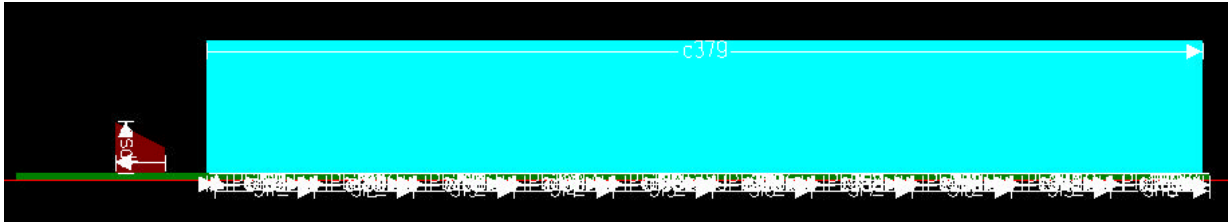


Fig 3.42 ESD Model with trapezoid grounded ring of height 100 microns

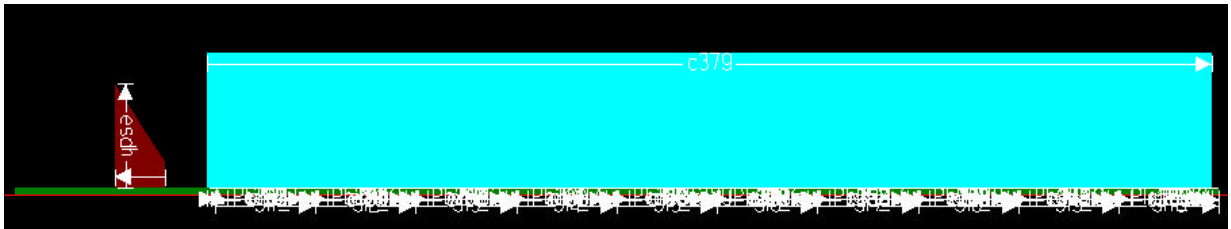


Fig 3.43 ESD Model with trapezoid grounded ring of height 200 microns

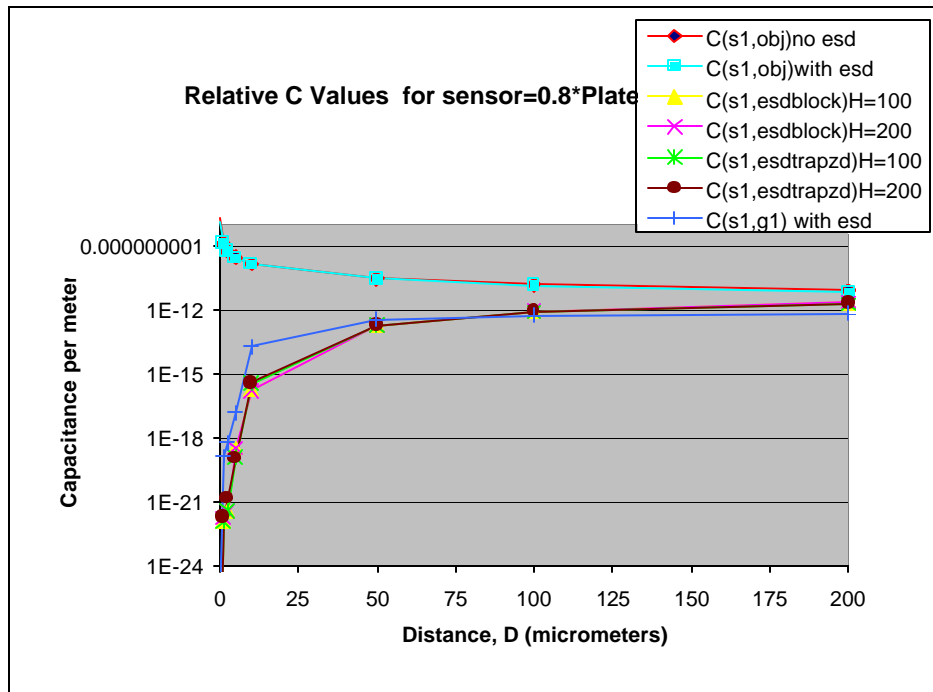


Fig 3.44 The logarithmic plot comparing the capacitance values with two types of ESD rings

“C(s1,obj)no esd” is the capacitance between sensor 1 and test object when there is no esd ring.

“C(s1,obj)with esd” is the capacitance between sensor 1 and test object when there is esd ring.

“C(s1,esdblock)H=100” is the capacitance between sensor 1 and rectangular esd ring of height 100 microns.

“C(s1,esdblock)H=200” is the capacitance between sensor 1 and rectangular esd ring of height 200 microns.

“C(s1,esdtrapzd)H=100” is the capacitance between sensor 1 and trapezoid esd ring of height 100 microns.

“C(s1,esdtrapzd)H=200” is the capacitance between sensor 1 and trapezoid esd ring of height 200 microns.

“C(s1, g1)with esd” is the capacitance between sensor 1 and guard 1 in the presence of any esd ring.

The results of this model are shown in the Fig 3.44. The results are as expected and similar to the previous model results. In the plot both results of rectangular and trapezoid grid are shown. There is no effect of the slant face of the grid at any point. The conclusions are same, if the test object is below 100 micron distance, the capacitance of grid to sensor 1 is much lower than the sensor 1 to guard 1. But when the test object is over 100 micron distance then it is contributing towards parasitic capacitance acting just like another guard grid. From this, we can say that the effect would be eliminated completely when the grid is placed at a distance equal to or greater than 150 microns.

3.8 Mixed Arrays

From the previous studies, it is understood that by using large sensors the resolution of the ridge feature is lost, and by using small sensors which experienced high parasitic coupling, the capacitance measuring capability is reduced. While testing the model in swipe mode it is stated that using mixed size of sensor plates would balance the above two contrary issues. This is based on the fact that small sensors give good resolution and large sensors will help in measuring the capacitance in higher ranges which used together in swipe mode, will increase the performance of the device.

Therefore, in this section mixed arrays are investigated in which different size of sensor cells and different size of sensor plates are used. First a model with different size of cells is designed (linear array) and later the model is tested with different size of sensor plates keeping the underlying shield plate constant (full- shield array). Both the models are tested with rectangular test block.

3.8.1 Linear Array

The model has been modified by placing different size of cells in a single array which is referred to here as Linear Array. The following set of simulations explore the inter sensor and parasitic coupling if large sensors are placed next to minimum size sensors in a variable size array. The sizes of cells used in this model are 50, 100, 200 and 300 microns respectively. Remaining cells are unchanged and to see the effect of parasitic capacitances between different size of cells a variable gap is maintained in between cells 1,2,3,4&5. A rectangular block is placed upon the sensor model and the block is moved to 200 microns away for each gap maintained in between the cells. Two type of simulations are performed here with this model, one with the air gaps between the modified cells and other one is with silicon filled gaps (continuous substrate).

Air gap Model

The following plots shows the total parasitic capacitance values for each gap maintained in between the cells. The plots are corresponding to first four consecutive cells of size 50, 100, 200 and 300 microns respectively. The air gap is varied up to 50 microns in between the cells as shown in the Fig 4 of Appendix-B

The total parasitic capacitance (TPC) is more for 50-micron cell, see Fig 3.45 and less for 300-micron cell, see Fig 3.48 as seen before. Increasing the gap between the sensor cells reduced the total parasitic capacitance to some extent, but the reduction is less than 5 % in all cases, even with a gap of 50 microns. The main contributors still are neighboring guards, plates and sensors as shown in the plots. Interestingly, neighboring sensor plates are more dominating than the neighboring guards and plates when the test object is beyond 50 microns, this is shown in the Fig 3.49 in which individual contributors are plotted separately. The data is taken at a typical gap of 10 microns between the cells.

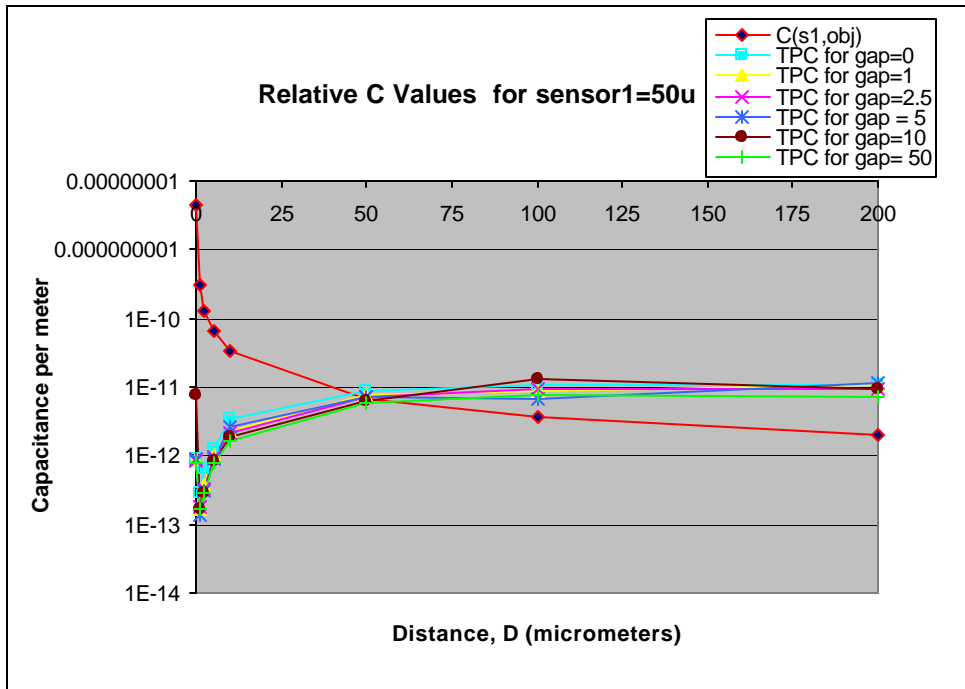


Fig 3.45 Logarithmic plot of sensor 1=50u

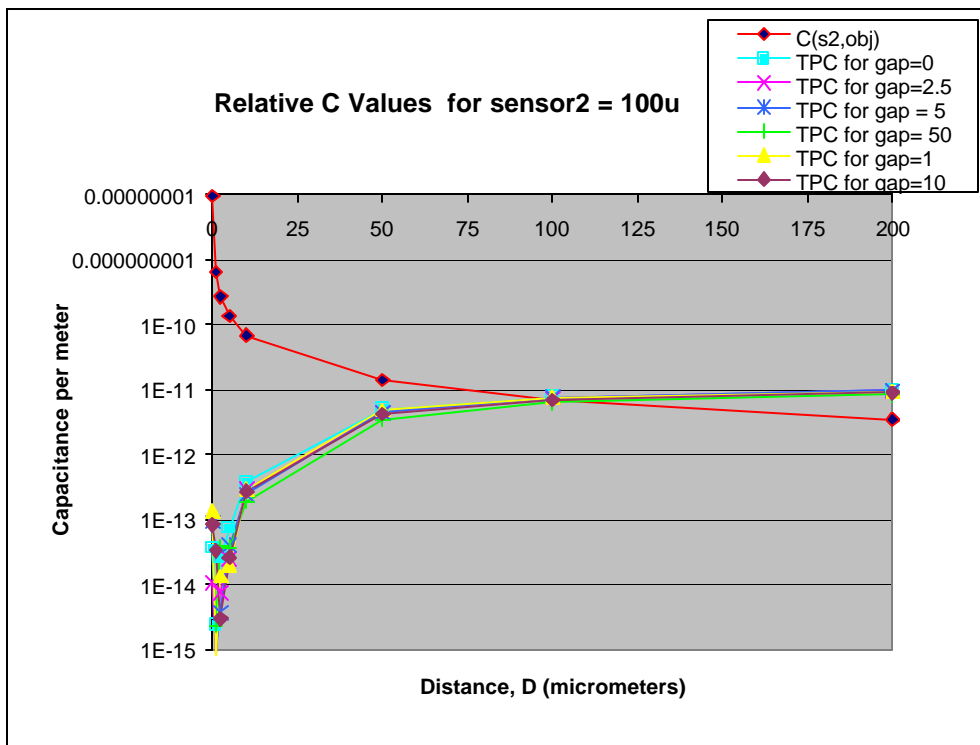


Fig 3.46 Logarithmic plot of sensor 2= 100u

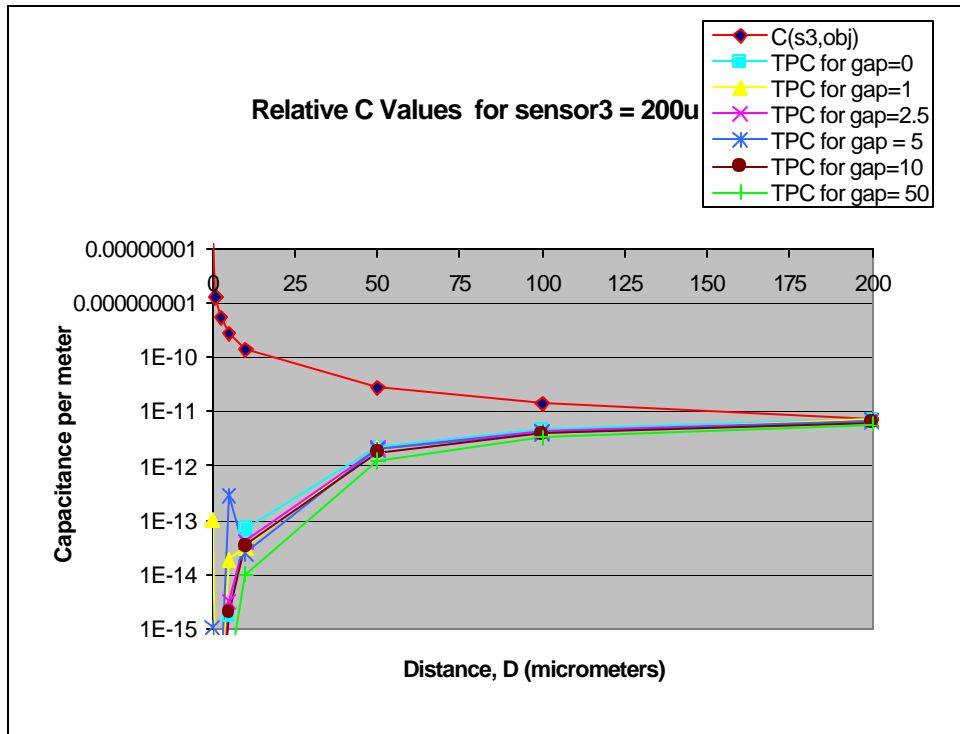


Fig 3.47 Logarithmic plot of sensor 3=200u

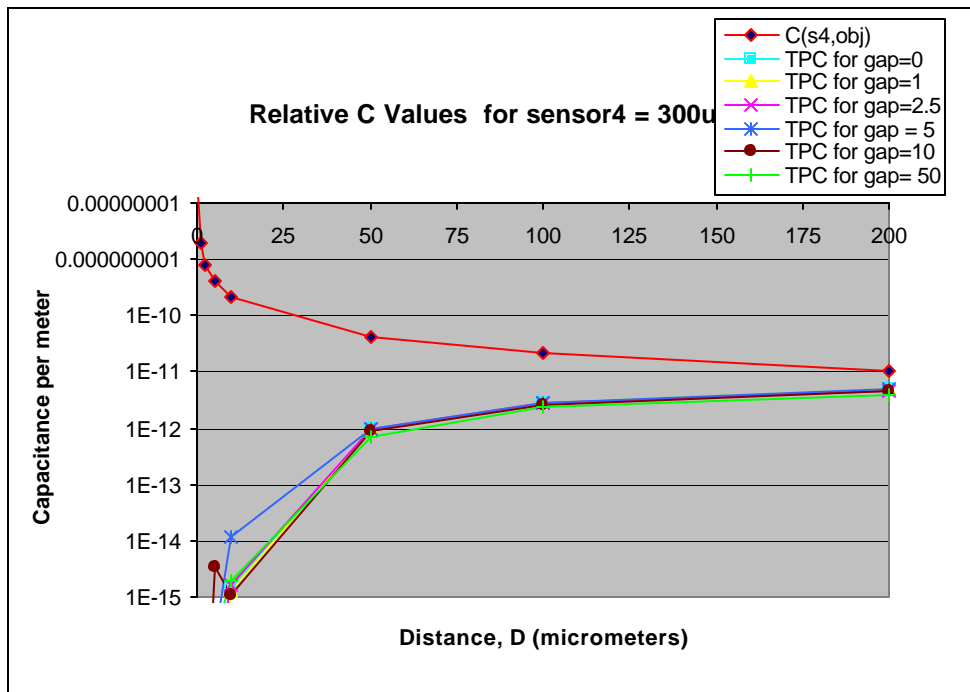


Fig 3.48 Logarithmic plot of sensor 4=300u

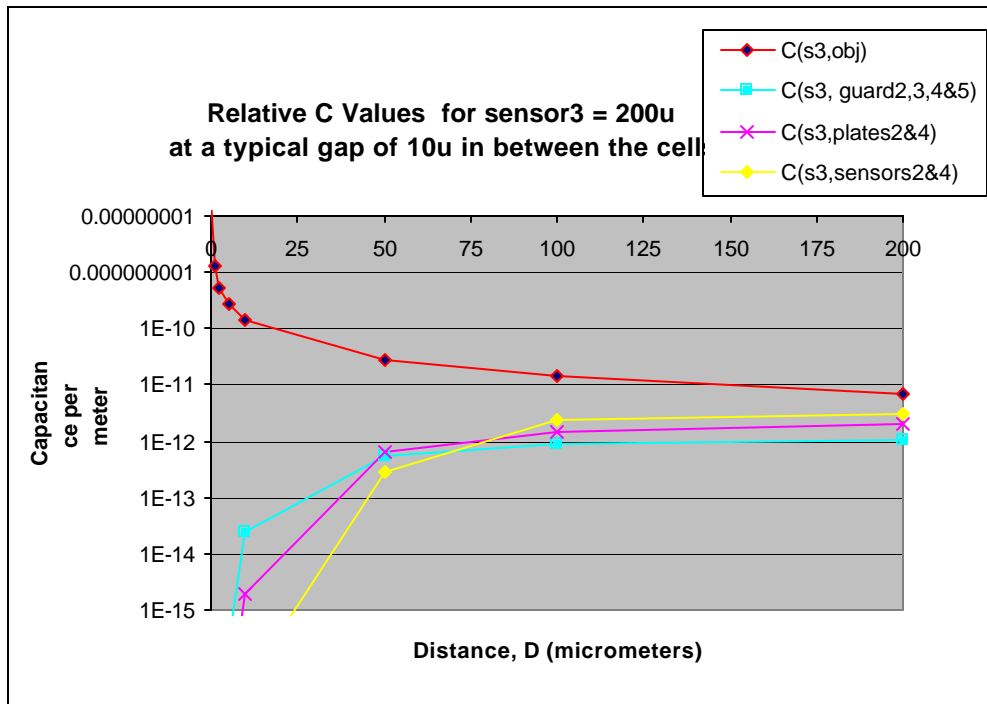


Fig 3.49 Logarithmic plot of sensor 3=200u

Silicon Filled Gaps

Keeping designing constraints in view, the cells are again separated but the substrate is now kept continuous. In other words, the silicon in the gaps is filled up to the height of silicon substrate as shown in Fig 5 of Appendix-B. The gap and all other parameters tested here are the same as in the above simulations. The following figures shows the sensor model at a typical gap between the cells in the model, with cell 3 placed in between the 100 micron cell and the 300 micron cell, maintaining variable gap from these neighboring cells, as shown and the silicon substrate is continuous throughout the model even in the gaps.

Total parasitic capacitance of the cell under test is reduced by introduction of a particular gap between neighboring large sensor cells, interestingly the total parasitic capacitance appears to peak for a gap of 5 microns as shown in the Fig 3.50. If the gap is increased above 10 microns the parasitics are reduced to some extent but the spacer

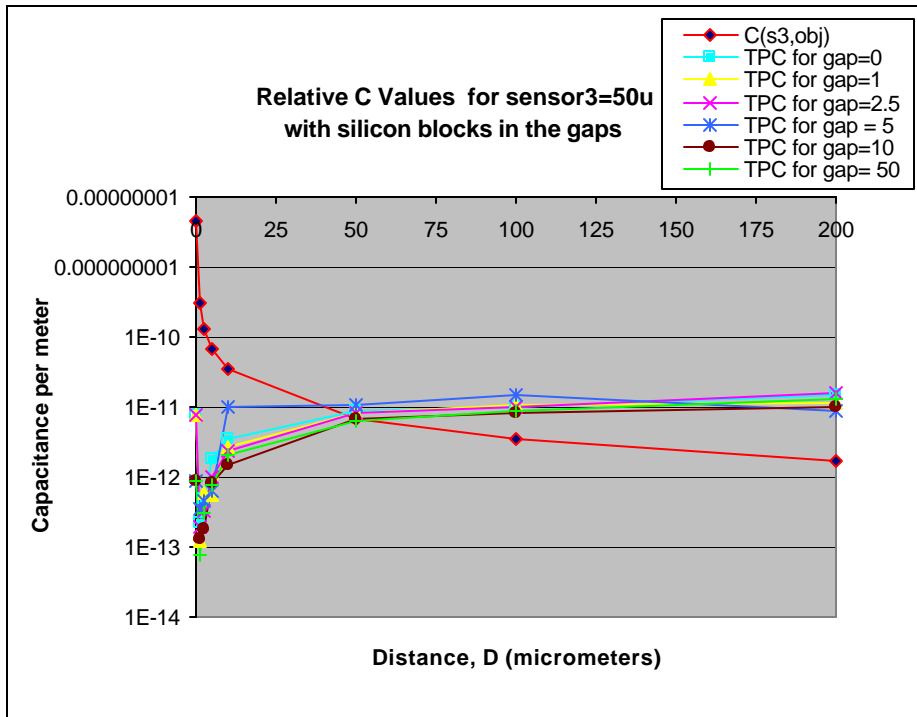


Fig 3.50 Logarithmic plot of capacitance values for sensor 3

TPC (Total Parasitic Capacitance) for sensor 3 = $C\{ (s3,g2) + (s3,g3) + (s3,g4) + (s3,g5) + (s3,p2) + (s3,p3) + (s3,p4) + (s3,p5) + (s3,s2) + (s3,s4) + (s3,Si) + (s3, \text{leftblock}) + (s3, \text{rightblock}) \}$

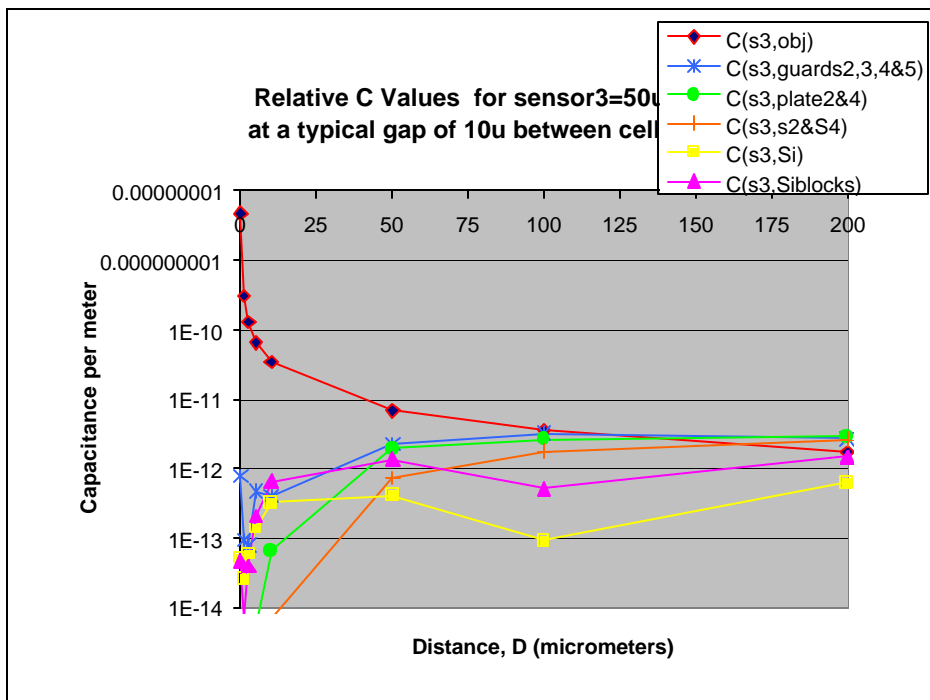


Fig 3.51 Logarithmic plot of capacitance values for sensor 3

regions which consists of silicon blocks between the differing sized sensors are a significant source of parasitics, exceeding that of the neighboring sensors at sensing distances less than 50 microns and even that of the guards for less than 30 microns, as from the Fig 3.51.

From above results, if the gap size is increased over 5 microns the total parasitic capacitance will increase, where the silicon substrate in the spacer region is added more into parasitics as shown in Fig 3.52, and hence the gap size is going to play an important role in reducing the total parasitic capacitance. On the other hand, the overall increase in total parasitic capacitance is less than 10% even when the gaps are 50 microns apart. Therefore care should be taken in choosing the gap size.

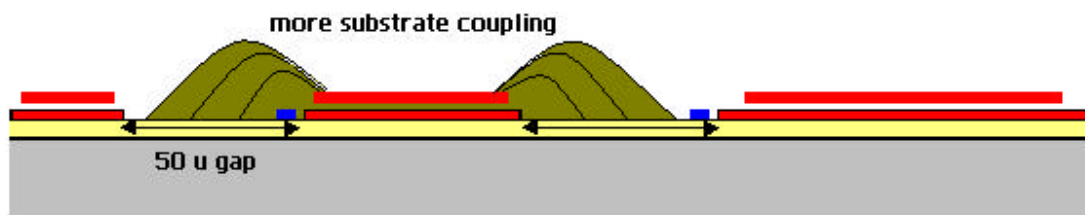


Fig 3.52 Linear array with exposed silicon substrate in spacer regions

Conclusions: This model indicates the need for shielding of the substrate if separations are to be made between rows of differing sized sensors. Given the results seen previously through other investigations in well structure model, extension of the plate (without a vertical lip) would reduce sensor-substrate and sensor-guard coupling.

3.8.2 Full Shield Array

In the previous experiment, the model is tested with different size of cells placed together with unshielded substrate in between to isolate large neighboring sensor cells. But the sensor plates experienced more parasitic capacitance with the presence of these unshielded substrate blocks. In this model instead of using different size of cells, different size of plates are used by varying the size of the sensor plates. Only the sensor plates are varied while other parts of the model are kept same as previous models with full shield. Gaps are not necessary in this model because small sensor plates are used which maintain

distance from the neighboring cells. In other words, each sensor plate in the array has full shield under it. The sensor plates are varied in the model with increasing sensor plate factor from 0.1 to 1.0 in steps of 0.1 units across the simulation region. This effectively makes this model as a variable sized sensor array within full shield and same grid size. As already seen the results of small sensor plate factors, this model is expected to experience a less parasitic capacitance as half of the cells in the model consists of very small size sensor plates. The simulation model shown in the Fig 6 of Appendix-B is of 50-micrometer cell size.

In this work, three cell sizes are tested which are 50, 200 and 300 micrometers. The size of sensor plates can be observed in the figure which increased linearly across the window, with maximum size at far end with 1.0 sensor plate factor. The first sensor plate is reduced by $0.1 \times \text{Shield Plate}$, second by $0.2 \times \text{Shield Plate}$ so on to tenth sensor plate which is reduced by $1.0 \times \text{Shield Plate}$.

50 micrometer Cell Array:

With 50 micrometer cells in the array the sensor plate size ranges from less than 5 microns up to 44.5 microns. The sensitivity of the sensor plate to sense the test object would become an issue as it's size goes down. The following plots in Fig 3.53 and 3.54 show the capacitance values of individual sensor to the test object as the object moves upwards to 200 micrometers. The idea of suppressing the parasitic capacitance by reducing sensor plate factor should balance against the decreasing sensor to test object capacitance.

The capacitance between sensor and test object is increased as expected, with increase in sensor plate size for all gaps between sensor and test object. Almost 10% rise in capacitance is observed with change in sensor factor from 0.1 to 1.0 in this 10 cell one-dimensional array. The total parasitic capacitance is increased linearly (not shown in the plots) with increase in sensor factor, but it is negligible for lower sensor factors, up to 0.6

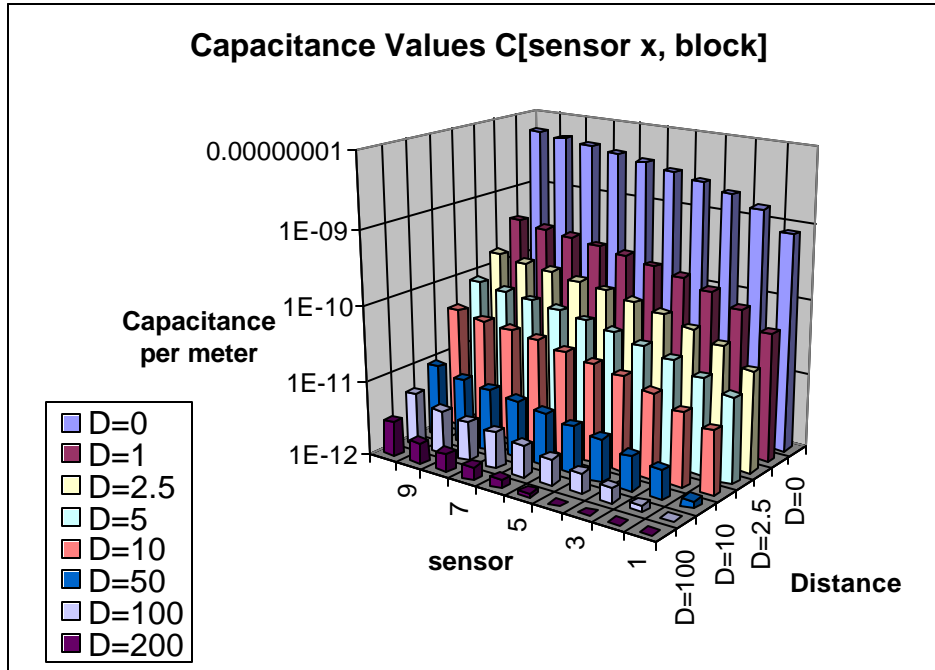


Fig 3.53 Logarithmic Plot for Capacitance values of individual sensors(50u) to test object
D is the distance between sensor plate and test object.

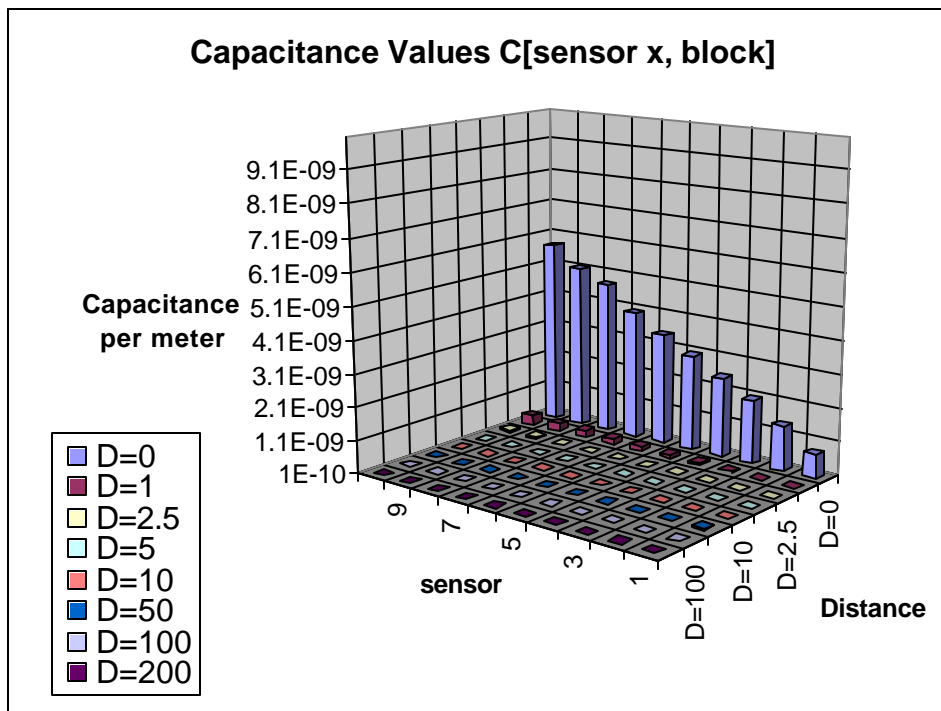


Fig 3.54 Linear Plot for Capacitance values of individual sensors to test object

factors. As the test object is moved more than 100 micrometer distance from sensor plates the smaller plates up to factor 0.5, are unable to sense the capacitance of sensor to test object, so if we increase the cell size to 200 micrometers there might be an overall improvement in the sensitivity of the small factor sensor plates.

200 micrometer Cell Array:

In this increased cell size array the sensor plates with the same factors range from less than 20 microns to 194.5 microns. Now the lowest factor sensor plate size is improved four times from that of above cell size. The plots in Fig 3.55 and Fig 3.56 show the capacitance values of individual sensor plates with the test object positioned exactly in the same manner as in 50-micron cell size array.

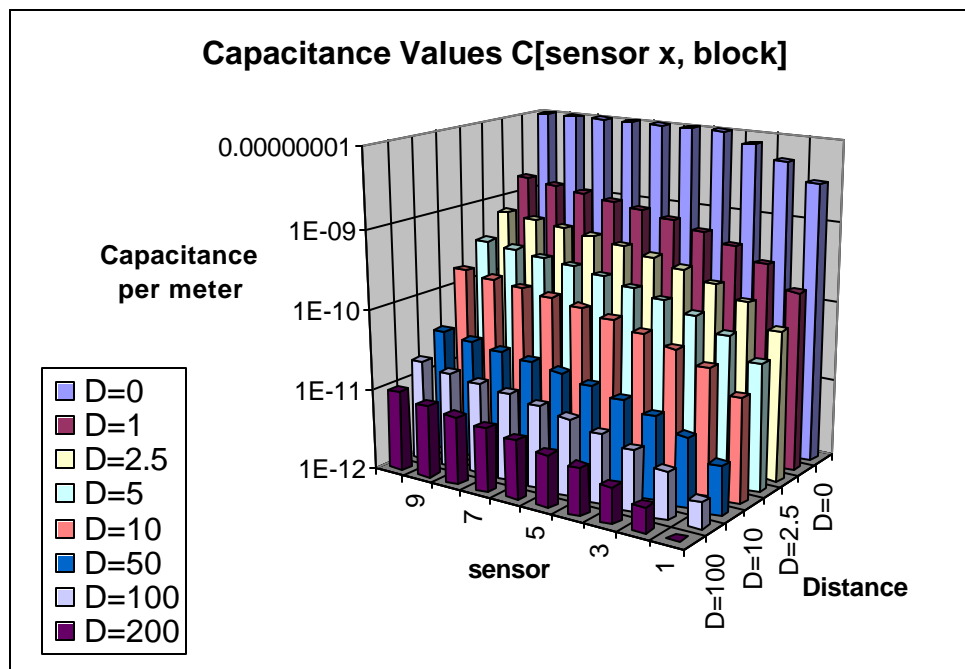


Fig 3.55 Logarithmic Plot for Capacitance values of individual sensors to test object

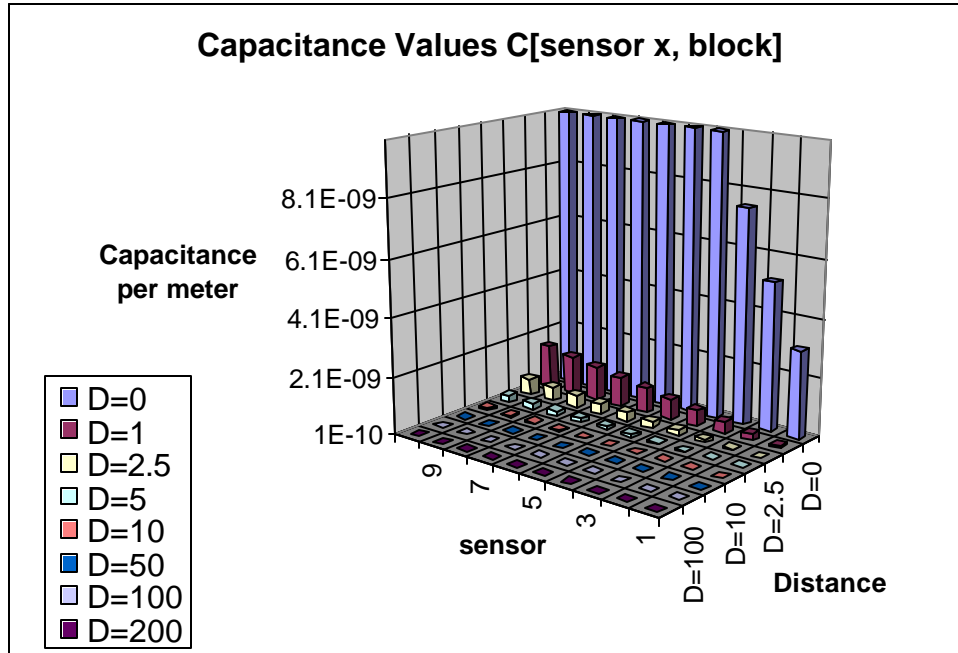


Fig 3.56 Linear Plot for Capacitance values of individual sensors to test object

The capacitance between sensor and test object is increased with increase in sensor plate size, and the performance of this model is better than 50-micron cell size model. But the rise in capacitance with change in sensor factor from 0.1 to 1.0 is found to be less than 10% though overall sensitivity is increased. The total parasitic capacitance is negligible for almost all the sensor factors when the test object is near to the sensor plates and it is coming into picture for higher factors where the sensor plate size is large and the test object is far from sensor plates.

300 micrometer Cell Array:

To see the advantage of large cell size array, 300 micrometer cell size is also tested here expecting still an improvised sensing capacity. The results are plotted in the following Fig 3.57 and 3.58.

The capacitance sensed by sensors is still better in this case and the capacitance for all sensor factors is found to be almost constant as sensor plate size is large enough to sense with even 0.2 or 0.3 factors. The total parasitic capacitance is negligible for all the

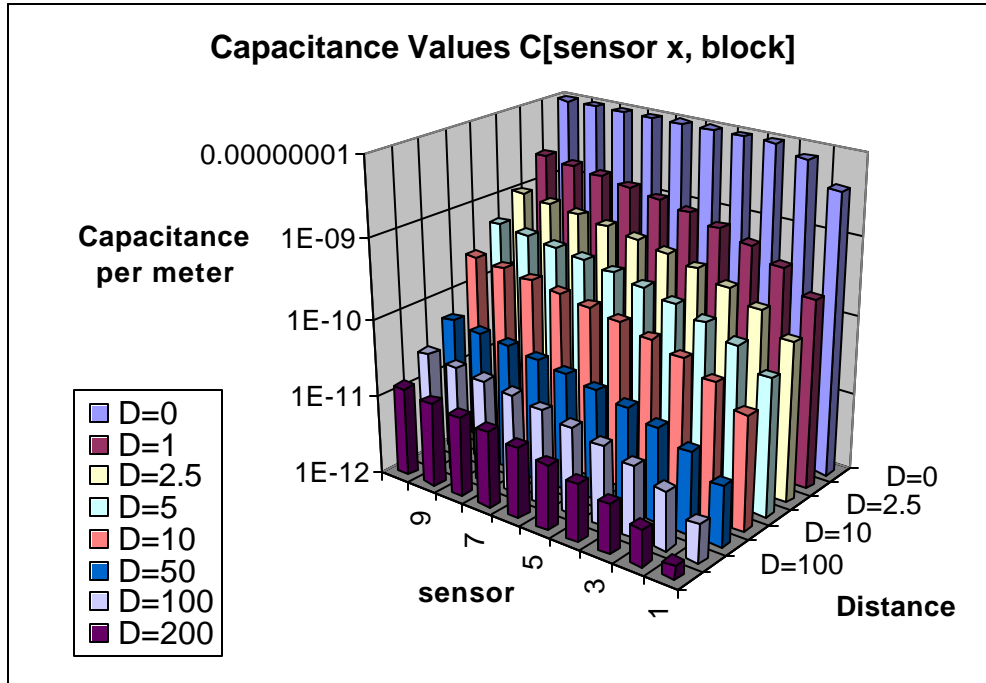


Fig 3.57 Logarithmic Plot for Capacitance values of individual sensors to test object

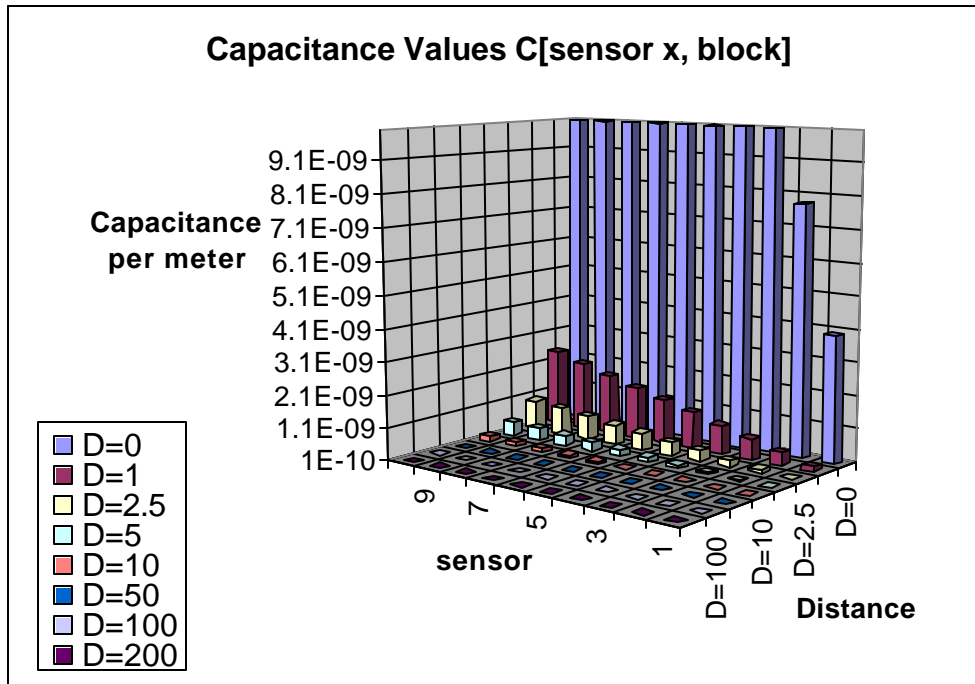


Fig 3.58 Linear Plot for Capacitance values of individual sensors to test object

sensor factors irrespective of test object position except for 1.0 factor when the test object is beyond 100 microns. It seems using 300 micron cell sensor array with sensor factors 0.2 to 0.8 suppress the parasitics below 20% of the test object capacitance.

Conclusions:

Given the constant cell and shield plate size, the shield extending between the variable sized sensors in a "swipe" sensor model can greatly reduce all parasitics, including guard parasitics while enabling different vertical resolutions. Such shielded variable sized designs can be explored further to determine optimum grid spacing for minimum parasitics and maximized capacitance to the object under test.

3.9 Adaptive Arrays

So far we have seen the results of various approaches that have been taken to suppress the total parasitic capacitance of the sensor plate in the model. We realize that, major part of the total parasitics is arises due to neighboring guard grids. In order to reduce this grid capacitance completely while measuring capacitance from a sensor plate in static mode, it might be a good idea if a switched grid system is explored which temporarily turn off regions that are contributing parasitic capacitance and effectively have large sensor plates. At this point, it is useful to see the sensor and grid configuration in the array and how they are electrically connected. Then the model is tested by turning OFF few grids that contribute parasitic capacitance to the sensor plate and making the effective sensor plate area large as explained in this section.

Fig 3.59(a) shows a partial sensor array in which rows are connected to positive supply and columns are connected to ground. Fig 3.59(b) shows how the sensor and grid are connected to supply lines. Each sensor is read by its relative row and column addressing.

The cross sectional view of the model in which grids are switched from ON to OFF state is illustrated in Fig 3.60. In Fig 3.60(a) Sensor 5 has two neighboring grids g5 and g6, which contribute to total parasitic capacitance along with the other elements. When these two grids are made ineffective by switching them OFF the parasitic capacitance might be reduced to some extent as shown in Fig 3.60(b).

This grid switching is tested to see if switching off the neighboring grids reduces the parasitic capacitance of sensor 5. Switching off the grids means assigning them neither to voltage nor to ground in the simulation setup, in other words those grids just float in the model. The capacitance values of sensor 5 with guards shutoff are plotted

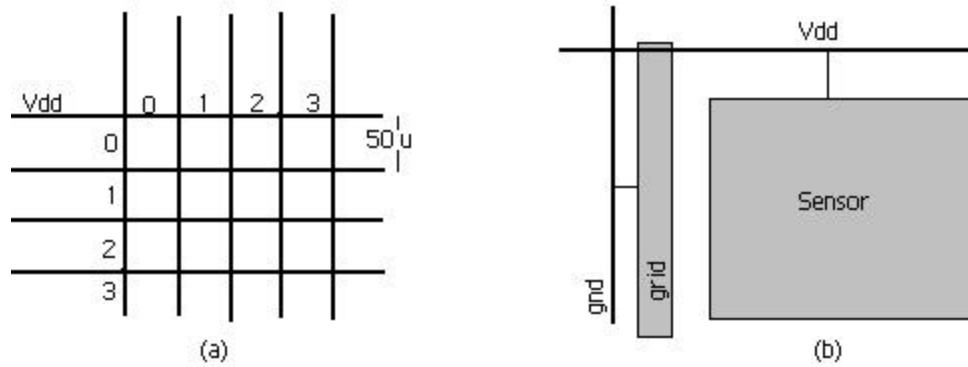


Fig 3.59 Sensor array with row column addressing

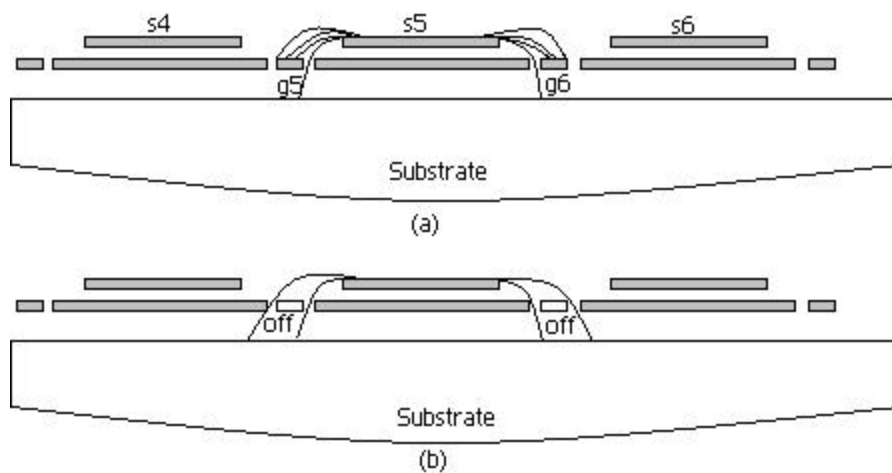


Fig 3.60 Sensor model with guard grid switching

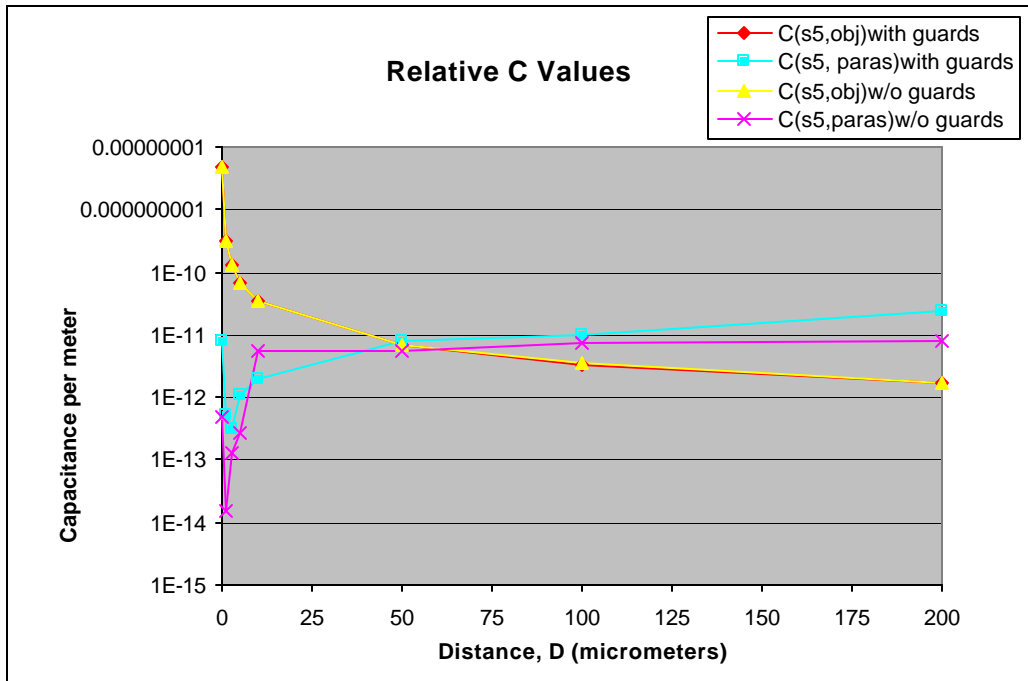


Fig 3.61 Logarithmic plot showing the parasitic capacitance with and without guard grids

$C(s5,paras)$ with guards is Total Parasitic Capacitance with guards = $C \{ (s5,p4) + (s5,p6) + (s5,g4) + (s5,g5) + (s5,g6) + (s5,g7) + (s5, Si) + (s5, s4) + (s5, s6) \}$

$C(s5,paras)$ w/o guards is Total Parasitic Capacitance with guards OFF = $C \{ (s5,p4) + (s5,p6) + (s5,g4) + (s5, Si) + (s5, s4) + (s5, s6) \}$ Guards 5, 6, & 7 are assumed to be OFF.

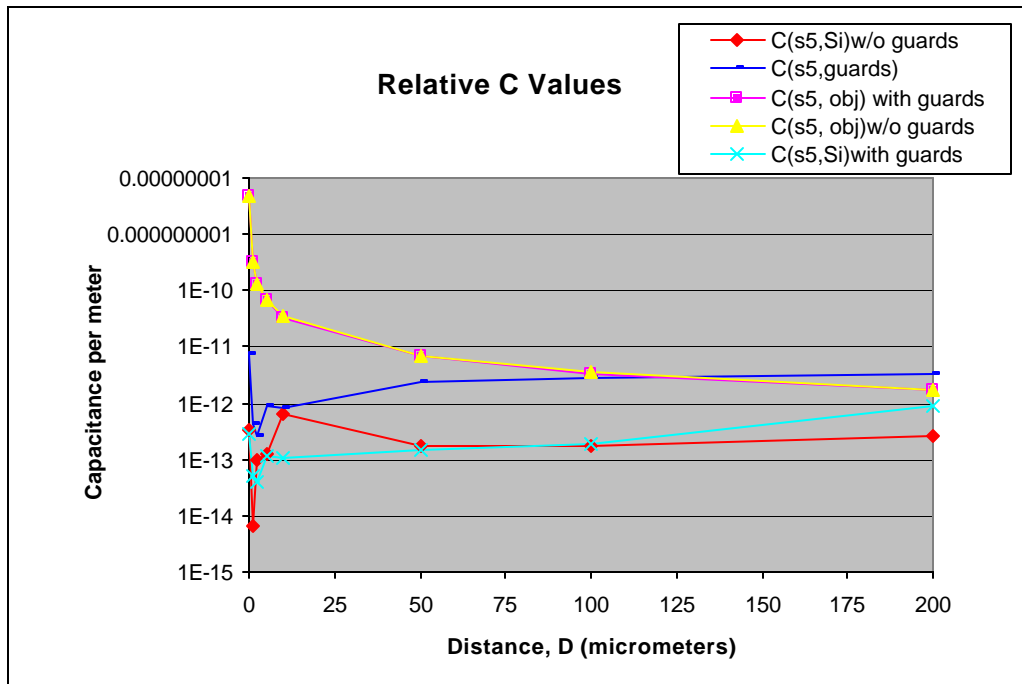


Fig 3.62 Logarithmic plot showing substrate parasitic capacitance with and without guard grids.

and compared with that of the results obtained while guards were present, in Fig 3.61. Both the results are obtained from the model of cell size of 50 micrometers, using the rectangular block as test object.

The plot in Fig 3.62 shows the individual parasitic capacitance values from which it can be observed that parasitic capacitance by the substrate is equal in both the cases when the test object is below 100 micrometers from the sensor plate and then it started to increase. But when guards are present in the model they are contributing 10% more than the substrate capacitance, towards total parasitics. The capacitance between the sensor 5 and test object is equal for any distance in both the cases.

So by this experiment, it is evaluated that this can potentially be a good approach to suppress the parasitic capacitance of a sensor. But by making a grid ineffective, the relative sensor loses not only the circuit ground path but also the internal ESD path. One way to overcome this difficulty is by interconnecting the sensor electrically to the neighboring sensor which has its grid ON. This is illustrated in the next section below.

Adaptive array with grid switching

With the above positive results, the modeling is continued to test the possibility of adapting a 50 micron cell array for large sensing area by electrically interconnecting the consecutive sensor plates with grids switched OFF in between. This is illustrated in the following Fig 3.63. Sensor plates 4, 5, 6, & 7 in a 50 micron cell model are interconnected, which now together equivalent to one 200 micron cell(4x50u). The guards 5, 6, & 7 are switched OFF from the signal line and they float in the model. Now the model is tested to see the capacitance values for this large sized cell array.

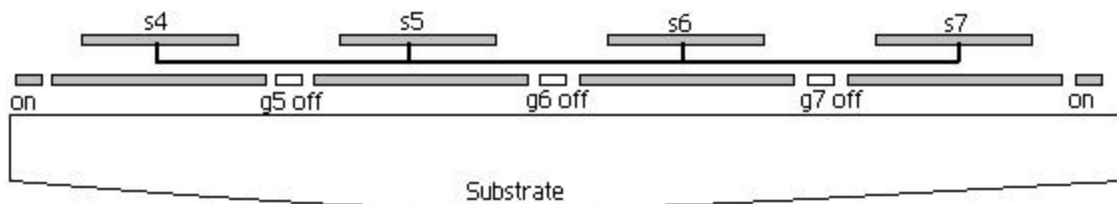


Fig 3.63 Adaptive array model in which few guards are switched off and sensors are interconnected

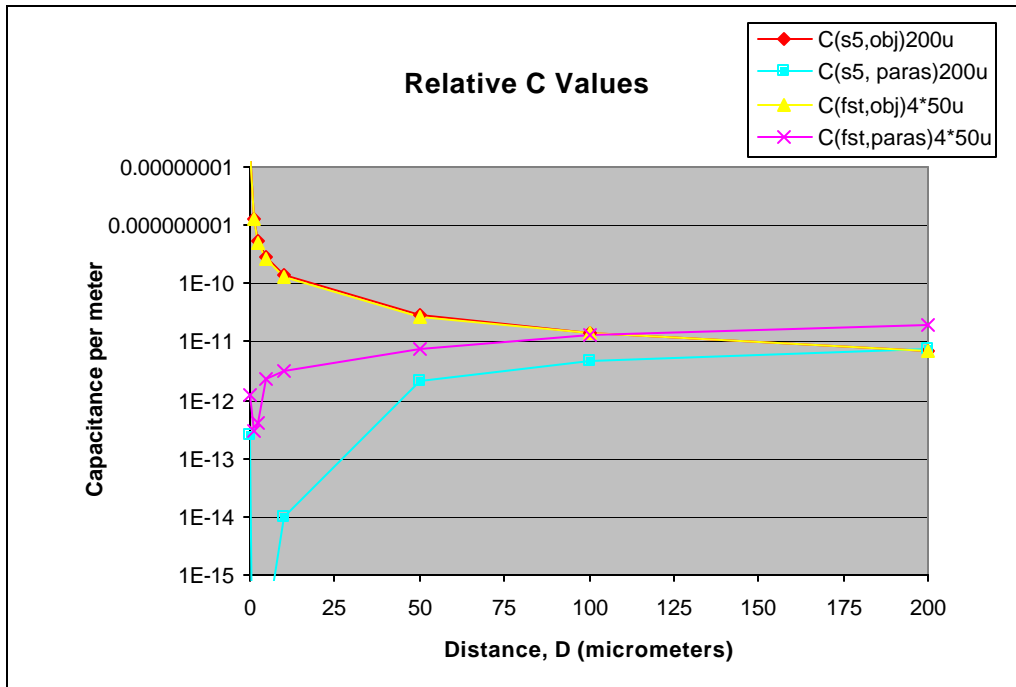


Fig 3.64 Logarithmic plot comparing capacitance values of two types of large size cell array

$C(s5,paras)$ Total Parasitic Capacitance = $C \{(s5,p4) + (s5,p6) + (s5,g4) + (s5,g5) + (s5,g6) + (s5,g7) + (s5, Si) + (s5, s4) + (s5, s6)\}$

$C(fst,paras)$ Total Parasitic Capacitance = $C \{(s4,p3) + (s4,g3) + (s4,g4) + (s4,s3) + (s7,p8) + (s7, g8) + (s7, g9) + (s7, s8) + (s4, Si)\}$

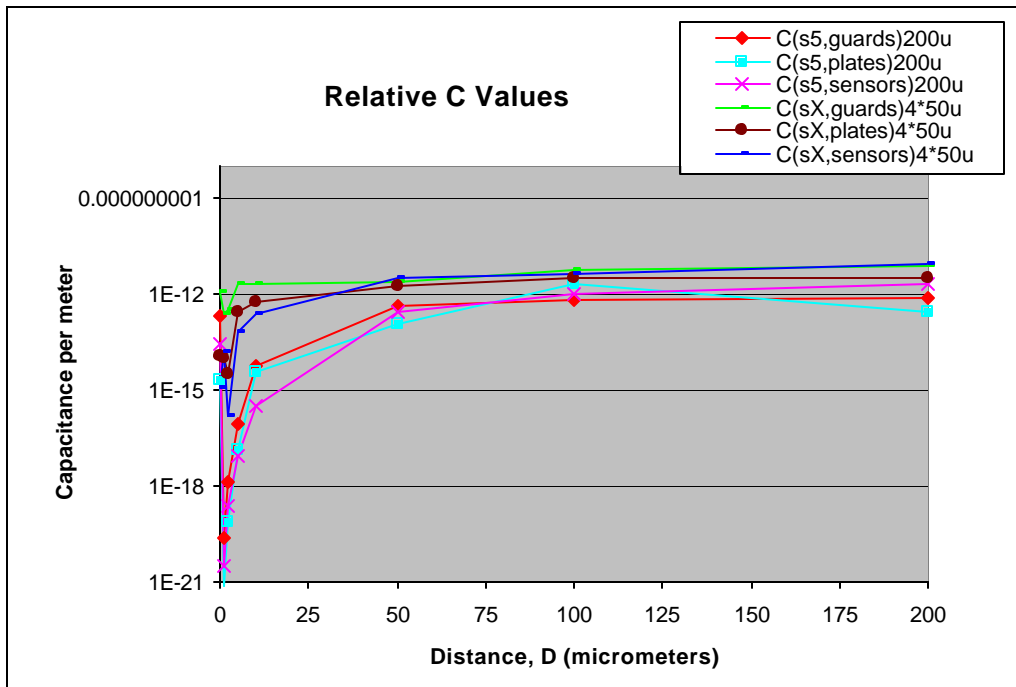


Fig 3.65 Logarithmic plot showing the individual capacitance values of two types of large size cell array

To evaluate this combined 4x50 micrometer cells performance, it is compared with that of one single 200-micrometer cell. It is observed from Fig 3.64 that the capacitance between the sensor and test object is equal for these two types of 200-micrometer cell size. The parasitics for 50 micron sensor plates are so calculated that the four sensors together are continuous and acting just like a single 200 micron sensor. The total parasitic capacitance is significantly higher in the case of 4x50 micrometer cells combined together, than that of a single 200 micrometer cell. This was expected because though some of the grids are switched off the gaps in between these cells have given way to more substrate coupling than in the case of a single large sensor.

The individual parasitic capacitance values are shown in Fig 3.65, which shows that all of the parasitics of 4x50 micrometer cell size are significantly greater than that of 200-micrometer cell. Though guards are turned OFF in between few sensor plates and made the sensor plate area effectively large, the model experienced high parasitic capacitance due to more substrate coupling.

Chapter 4

Conclusions & Future Work

Conclusions

In conclusion, the studies carried out in this work indicate new approaches that may be taken for further improvement of solid-state CMOS fingerprint sensor performance. Given that specific design tradeoff associated with each can be satisfactorily achieved, their incorporation in emerging device generations holds potential. Here, results and discussions from each study are summarized briefly and conclusions drawn.

- ***Sensor Plate and Cell Size Study:***

A sensor plate that is larger than the underlying guard shield is not consistent with extended cell sensing range due to the large substrate parasitic capacitance of the geometry. Decreasing the sensor plate size reduces the absolute capacitance magnitude, however a scale factor of 0.8 (e.g., sensor plate width = 0.8 * shield width) is shown to be a good compromise. Similarly, the mutual capacitance between the sensor and the object under test is found to increase as larger cell sizes are used. Taking cell resolution into account 200 micrometers is found to be a cell size that can be used for which ridges are still resolvable, and vertical resolution is improved.

- ***Vertical Sensitivity and Feature Resolution in Static and Swipe modes:***

It is found that the 200 micrometer sensor cell is able to yield a measurable capacitance even at a valley depth of 200 microns, though it is less in value. In both static and swipe modes with this cell size, the object-sensor capacitance is increased for large size of sensors, but the resolution of the valley sidewall and the ridge structure has been diminished, which was apparent for small sensors. The results of swipe mode are useful for mixed size arrays in which small sensors for maintaining resolution and large sensors for high capacitance measurement ability are used together.

- ***Embedded Sensor Plates:***

The 0.5-micron thick nitride protective coating on the sensor plate structure has little effect on the capacitive modeling relative to a model which has a similarly sized air space

between sensor and test object. Inclusion of the dielectric scales results by a factor on the scale of the dielectric constant.

- ***Well Structure of Underlying Shield Plate:***

For lower sensor plate sizes relative to the underlying well structure shield plate, the total parasitic capacitance is found to be significantly reduced. Incorporation of vertical lips on the shield plate edge is not helpful for larger sensor plates even if the height of the lips is increased. If the sensor plate could be recessed down into the well structure it is expected that parasitics would be better suppressed. Adoption of such an approach must assure that the topography of the device is not affected, and a suitable process to achieve the configuration can be achieved.

- ***External Electrostatic Discharge Ring:***

When the ESD ring is placed 100 micrometers away from the sensing elements on the chip periphery, the ring has very little effect on the parasitics of the peripheral devices in the array, at object distances below 100 microns. When object distance is more than 100 micrometers from chip surface, the ESD ring's contribution to the parasitics is evident and of the order of a guard grid.

- ***Mixed Size Cells and Sensor Plates:***

For linear arrays in which separations are to be made between rows of different sized sensors, it is found that the substrate in these gaps is an added parasitic element. Therefore, instead of making separations between the sensor cells, the underlying shield plate size is held constant for each cell (resulting in the same substrate "exposure") and a different size of sensor plates is used in each row. With small sensor plates used, this model has only small substrate gaps with parasitic capacitance is reduced 20% below the test object capacitance.

- ***Adaptive Arrays with Grid Switching:***

The major contributor to the parasitic capacitance is the neighboring guard grid. To suppress the capacitance arising from these guard grids, the effect of adaptive arrays that

can activate or deactivate the grids are studied. If a guard grid of a sensor plate is able to switch off locally during the sensing cycle for nearby cells, the measured sensor plate capacitance may experience lower parasitics. However, it was found that for the current geometry, shutting one complete or partial column of guard grids off and measuring capacitance from all respective sensor plates interconnected together to simulate the effect of a larger monolithic sensor results in more parasitic capacitance. This is due to the sensor plate field now terminating on the grounded substrate in these regions. Adaptation of the sensor shield factor and cell array layout may remove this barrier, however the increased real estate overhead arising from the needed array switching circuitry may be more problematic.

Future Work

Based on the results of this study, some areas of future investigation are suggested. While not comprehensive, the two areas highlighted below show merit.

Increased isolation of the sensor plate represents a means to achieve improved sensor performance. A 'well structure' for the shield plate was explored in the work. Increasing the height of the vertical lips of the wells combined with recessing the sensor plates into the well represents an area for further investigation. Decreased coupling of the sensor to grid is anticipated, however, issues of thin film deposition and surface topography will need to be addressed.

In the static or non-swipe mode, grid switching can potentially play an important role in suppressing the guard grid parasitic capacitance completely if grids are switched off for neighboring columns of a sensor while the column reader reads the capacitance. This switching scheme is shown in Fig 4.1 below.

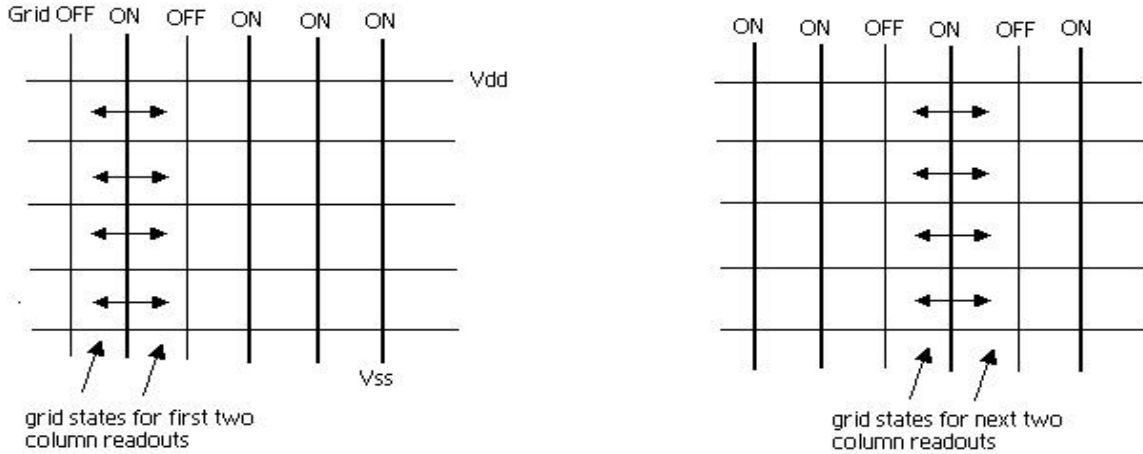


Fig 4.1 Partial sensor array with guard grids shown by columns, which change state by switching.

It is assumed that the two grids present on either side of the switched column ground each sensor plate. For every two column readouts two guard grids will have to change their state as shown in the above figure. With this configuration, for every sensor plate two parasitic elements are reduced at the time of sensor element charging and discharging. Future work would explore and quantify sensor sensitivity benefits as well as the real estate and complexity tradeoffs implied by such an architecture.

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Appendix-A

Specifications of solid-state FPS 100 fingerprint sensor[8], [13].

Features:

- 300 X 300 sensor array
- 500 dpi resolution
- Standard 0.5 μ CMOS process
- 50 μ sensor pitch
- 50 μ X 50 μ sensor element size, more than 60% of this area is occupied by the sensor plate
- 1.5 cm X 1.5 cm array size
- Approx., 1 μ s Sensor integration time
- Approx., 50 μ s Row readout time
- Approx., 60Max. frames per second
- 110 W standby power dissipation at 1.8V, 10 frames/sec
- 250 μ W active power at 60 frames/sec
- < 1 % False Acceptance Ratio
- 8-bit microprocessor interface
- VSPA 80/1 (similar to 24 mm X 24 mm TQFP) or 169 pin, 27 X 27 mm BGA

Absolute Maximum Ratings:

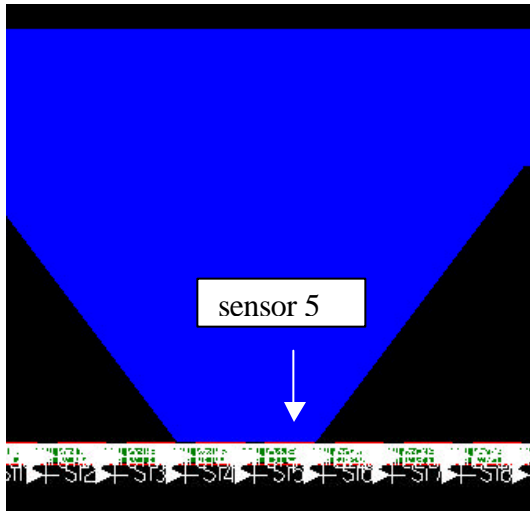
- Storage temperature: -65° to +150°
- DC Voltage Applied to any pin: -5.0 to +7.0V
- ESD Voltage: >2000 V
- Latch up current: > 100 mA

Operating Range:

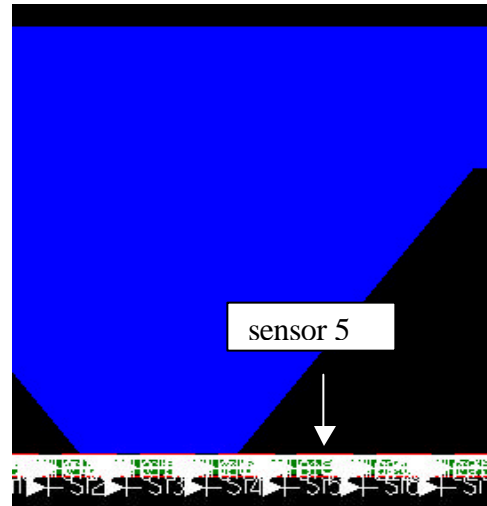
- Ambient temperature: -0° to +70°
- V_{DD} (Digital Supply Voltage): -4.3 to +5.5V
- V_{DDA} (Analog Supply Voltage): -3.0 to + 5.5V
- Oscillator frequency: 10 MHz to 40 M Hz

Appendix - B

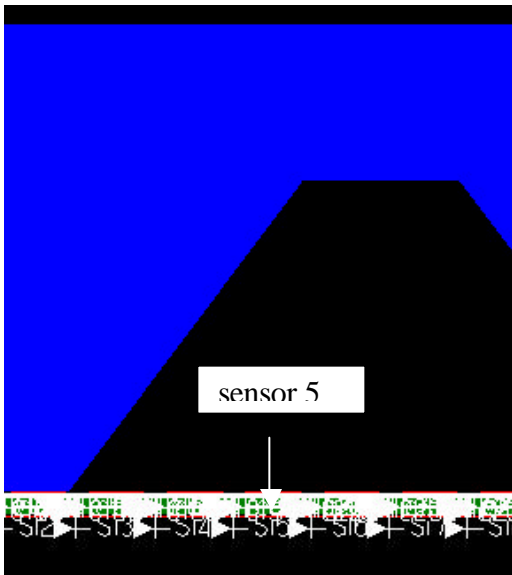
Detailed pictures of specific simulation window geometries



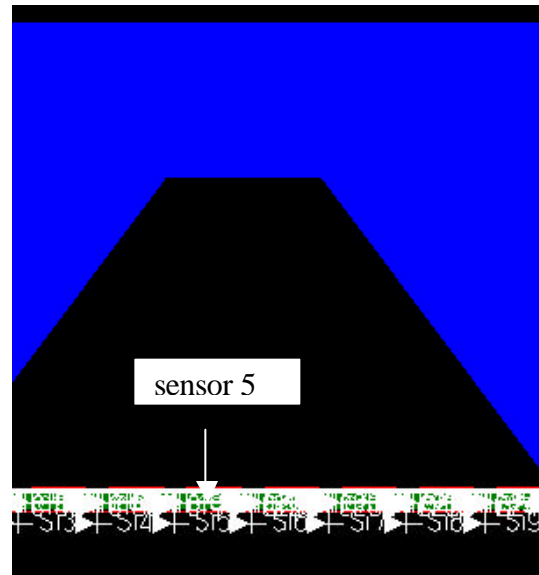
step 1



step2



step3



step 4

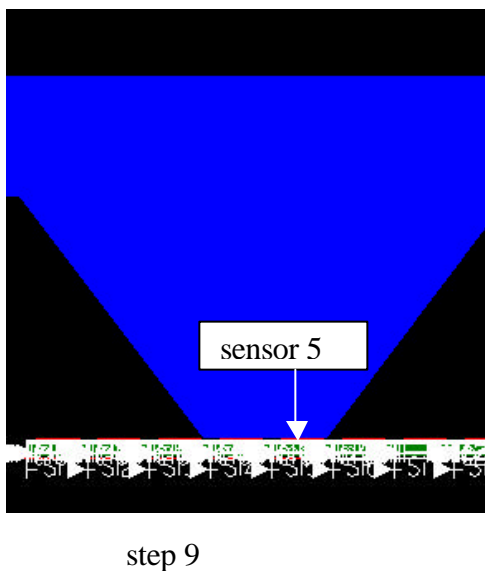
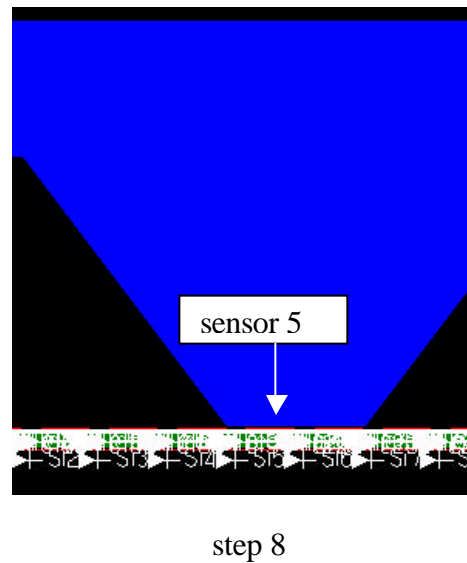
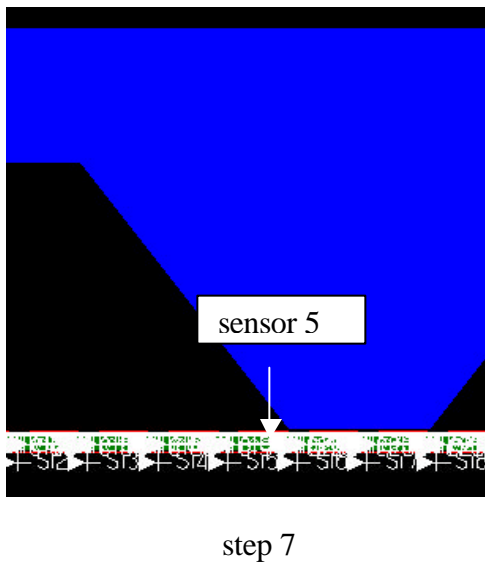
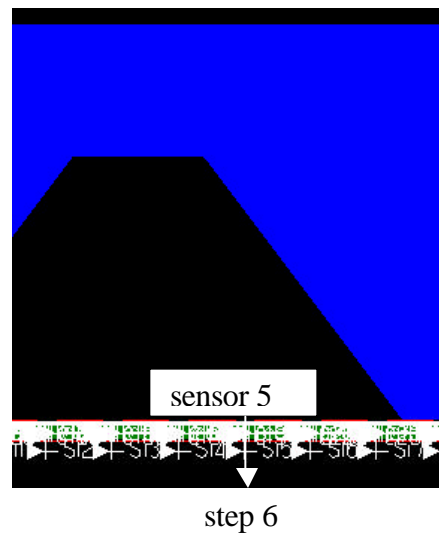
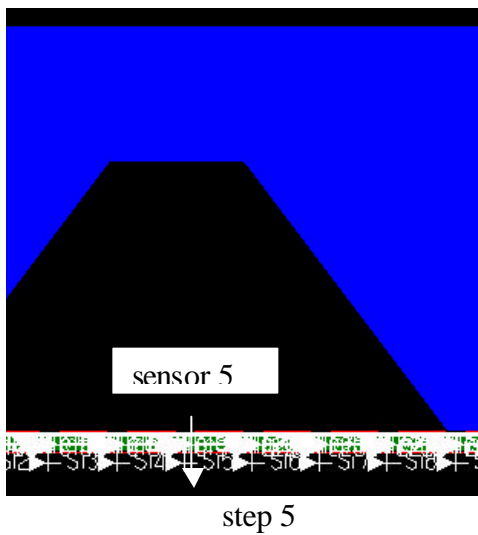
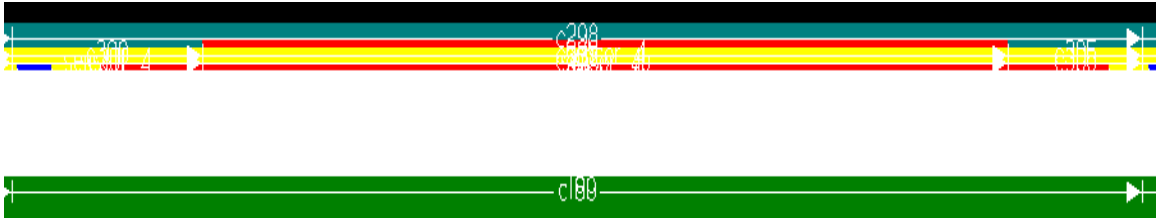
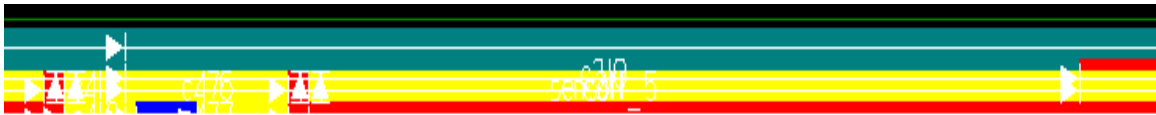


Fig B(1) The above figures shows the positions of the reference sensor5 in one complete cycle of ridge & valley structure when VTO is swiped over the sensor plates with a step size of 75 microns .



Fig(2) Enlarged view of a cell with nitride protective coating on the sensor plate



Fig(3) Vertical lips at the ends of two different shield plates



Fig (4) Mixed cell array with gaps between the cells

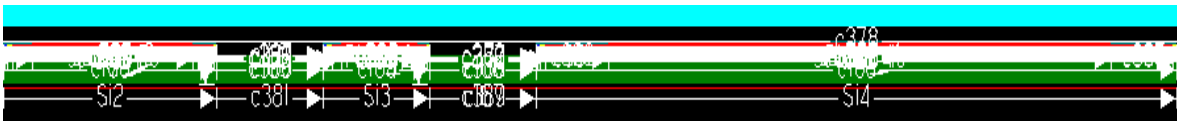


Fig (5) Silicon filled gaps in linear array

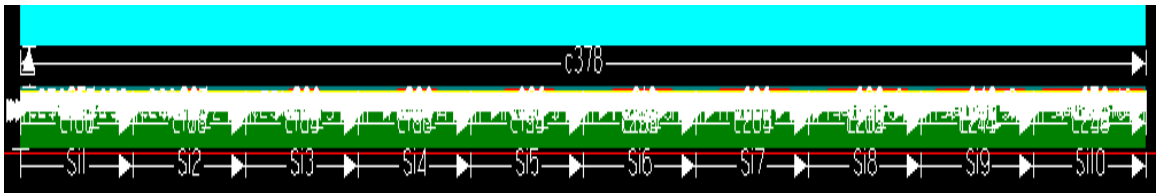


Fig (6) Full Shield Array with variable sized sensor plates

VITA

The author was born on 6th Nov 1976 to Mr. Venkata Swamy and Mrs. Tarakamma in Wanaparthy town of Andhra Pradesh, INDIA. He has a brother Ravi Kumar and two sisters Sucharitha and Kavitha. He completed his schooling in Sri Saraswati Sishu Mandir at Wanaparthy. He was awarded with AP Government Scholarship twice for outstanding performance in the school. He joined in Govt. Polytechnic College with Electronics & Communications Engineering as major and completed with first rank in the year of 1995. In 1999 he awarded with Bachelor of Technology in Electronics & Communications Engineering from Nagarjuna University, INDIA. He came to USA in Aug'1999 to pursue his Masters program in Electrical Engineering. The author worked as Graduate Research Assistant under Dr. L. A. Hornak during Jan'2000 to Dec'2000 and successfully defended this thesis work in the month of Dec'2000. He is going to earn his MS degree in May 2001.