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Low frequency Quadrature detector design, simulation and implementation for use in underground communication

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Low frequency Quadrature detector design, simulation and implementation for use in underground communication

Zenaneh Ashebir Kebede

**Thesis submitted to Benjamin M. Statler college of Engineering and mineral resources
at West Virginia University**

in partial fulfilment of the requirements for the degree of

**Master of Science in
Electrical Engineering**

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David W. Graham, Ph.D**

Lane department of computer science and electrical engineering

**Morgantown, West Virginia
2014**

Key word: Low frequency quadrature detector.

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ABSTRACT

Low frequency Quadrature detector design, simulation and implementation for use in underground communication

Zenaneh Ashebir kebede

The earth does not easily propagate high frequency signals. Low frequency, through the earth, signals would provide better penetration of the earth surface. Extremely low frequency communications has been a challenge for many years because of the underlying limitations such as significant background noise, and large antenna size. This thesis investigates the design of a compact quadrature sampling detector for extremely low frequency through the earth communication. It is hoped that a receiver such as that designed herein could receive signals at frequencies much much less than 10 kHz through the earth. Furthermore, this thesis compares the method of quadrature reception at these extremely low frequencies using simulation and hardware implementation with higher frequencies. This thesis also discusses the design of quadrature sampling detector and performance measurement of the quadrature detector at these extremely low frequencies. The results of the quadrature detection hardware testing show that it is indeed possible to use a quadrature detector at such low frequencies.

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Zenaneh Ashebir Kebede

March, 2014

List of Symbols

- AM - Amplitude modulation
- BPF - Band pass filter
- CLK - Clock
- DC - Direct current
- D-C - direct conversion
- Demux - Demultiplexer
- FET - Field-effect transistor
- FFT - Fast Fourier Transform
- FM - Frequency modulation
- HPSDR - High performance software defined radio
- I - Inphase
- IF - Intermediate frequency
- IC - Integrated circuit
- LO - Local Oscillator
- PCB - Printed circuit board
- PED - Personal emergency device
- PSK - Phase shift Keying
- Q - Quadrature
- QSD - Quadrature sampling detector
- RF - Radio frequency
- SDR - Software defined radio
- SNR - Signal to noise ratio
- TD - Tayloe detector
- TTE - Through the earth

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Chapter-1

1. Introduction

1.1 The need for mining communication

The loss of life in mine disasters has made it apparent that mining communications technology must improve especially post incident. Mine disasters occurred since the dawn of mining for different reasons. Since most of the mine disasters involve explosion, collapse, and fires, it makes it difficult to locate and rescue trapped miners. Most mine disasters can trap miners and destroy infrastructure holding mine communication equipment. Wireless communication is crucial after any significant incident, such as fire or explosion, because of destruction of the fixed communications infrastructure underground.

Most mine disasters which have occurred in the past ten years have shown that a better post disaster communication system is vital for any underground mining operation. Some of the incidents include the Upper Big Branch mine disaster in Mont coal, West Virginia on April 05, 2010 [1] twenty nine miners died. A similar incident in which an explosion occurred at Sago mine near Buckhannon, West Virginia in Feb 2006 [2] in which the life of twelve miners were lost. It is important to mention that the communications between rescue team and surviving miners was impossible and probably contributed to the loss of life in both incidents. The lack of communications between the miners and rescue teams makes the rescue effort very difficult, such communications is extremely time sensitive. For this reason the lives of some miners could possibly have been saved if a better post incident communication technology had been in place. These particular disasters demonstrated emergency mining communication systems are critical for life saving and underground rescue.

The completely wireless operation of radio below the surface of the earth does not yet exist. The main reason for the loss of communication following an underground explosion, the underground communication infrastructure can be destroyed. The penetration of wireless signals below the earth's surface is generally inversely proportional to the frequency of the transmitted signal.

The difficulty of propagation of RF signals through the earth has made it seemingly clear that the one possible effective through the earth, TTE, communication would be to use low frequencies (<10KHz). But there are two major problems associated with communicating with low frequency signals. To be efficient the antennas must be very large to couple at low frequencies (large wavelength). The second issue is that design of the receiver for the low frequency communication system is challenging because of need of extremely narrow bandwidth. The goal of this research is to design a radio receiver that can receive extremely low frequencies and contribute to the mine emergency communication solution.

1.2 Through the earth Propagation problem

The mine Safety and Health Administration have been working to reduce the fatalities related with mines and as the next figure shows the attempt to protect miners have been successful as the fatalities related with mining has declined in recent years. However, a better communication system would even make the death toll even lower. A data is shown on mining fatalities for last 112 years from 1900 to 2012 in the *Fig 1* [21].

A radio system capable of transmitting and receiving a signal through the earth can be used not only for the purpose of the communicating information to/from trapped miners but also to guide the emergency rescue which is a highly time sensitive operation. Moreover, such technology can be used in other areas and application like earth electric field detection in underground, communication in caves, recreational activities to be undertaken in underground, which can create a potential users and business in the discipline.

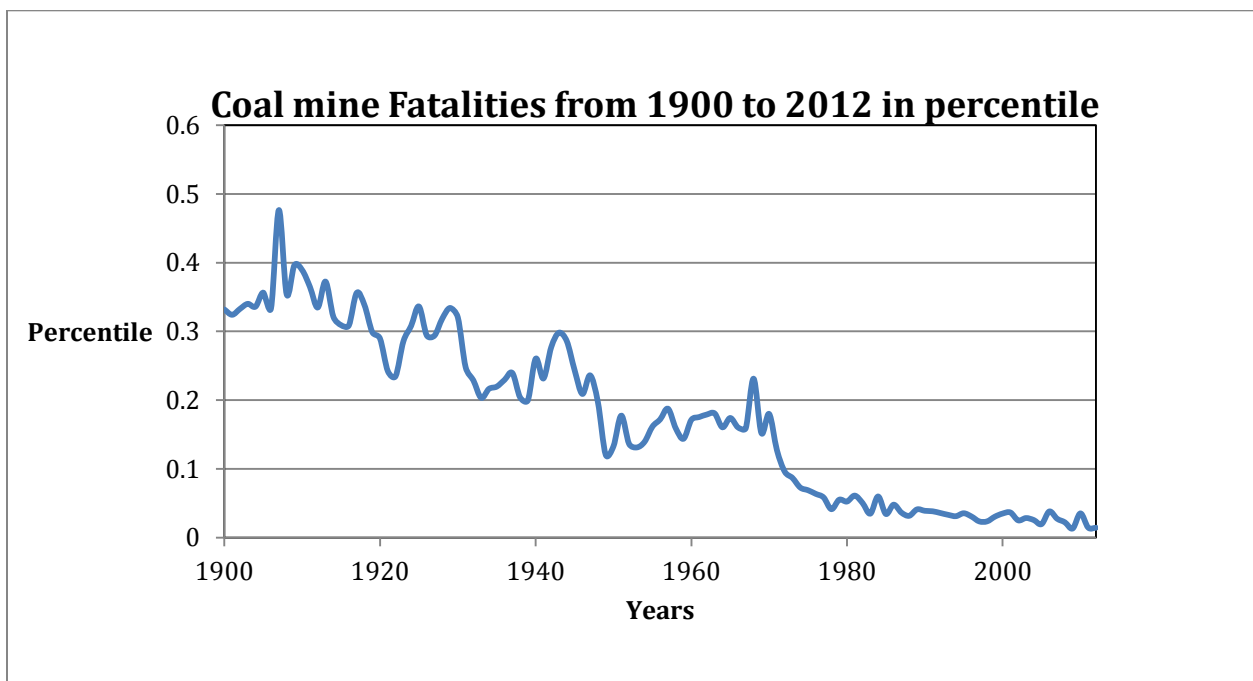


Figure 1: Mining Fatalities

The challenging part for the through the earth communication (TTE) is the propagation of electromagnetic waves through the earth's surface. Long wavelength signals (low-frequency) are very insensitive to obstacles which are smaller than the wavelength of the radiated signal and will therefore scatter less than higher-frequency signals through the Earth's crust. According to previous experiments to characterize the RF characteristics of the Earth, low frequencies are viable carriers for communication, as the Earth is very opaque at higher frequencies. One such Earth characterization experiment states:

“Results indicated an expected 45% probability of detecting a miner’s signal from a depth of 1000ft, a depth which exceeds 90% of the coal mines in the United States and a 90% probability at a depth of 500ft, a depth which exceeds 50% of the mines.” [4]

The penetration of high frequency signals through the earth is small. Thus, this work focuses on building a receiving system for low frequencies. There are two major problems associated with low frequency signals: antenna size and data rate. From basic electromagnetics the relationship between the wavelength which is the distance between two identical points along the propagation wave and the frequency of the signal can be expressed by the equation as shown below.

$$\lambda = \frac{v}{f} \quad (1)$$

Where λ = wavelength, v = speed of light f = frequency

According to the above equation using the speed of light in free space 3×10^8 m/s, it can be seen that the wavelength calculated for 10 KHz is very long, 30 km or nearly five miles in length. Even though an antenna of even quarter wavelength would seem impractical, there are various techniques that can be used to overcome the size problem. Loop antennas are an alternative

$$\lambda = \frac{v}{f} = \frac{3 \times 10^8 \text{ m/s}}{10 \text{ kHz}} = 30 \text{ km}$$

1.3 Current Radio Technologies

A new type of radio, software defined radio, SDR, has become practical since the development of analog to digital converters which has a high processing performance computer cores, fast memories, and fast computing hardware[5]. SDR radio have the ability to capture an entire spectrum, and all the radio functionality including demodulation (recovering of information from the modulated carrier) can be performed in software on all desired portions of the spectrum with the ability to capture an entire spectrum and process the information real time or to save it.

There are several communication systems that are used currently in some underground communications. One that is rare in the United States is personal emergency device (PED) which is a one way text based device from surface to underground communication. Though it can be useful, a major shortcoming is that the product is unable to transmit or transfer data from underground to the surface. Some of the two way communication systems which are currently possible using different technologies include [15].

1. Mine page phones

Mine page phones operate in a very similar manner to landline telephones (two-conductor cable). The most major drawback with this technology is the similarity with leaky feeders – the infrastructure (two-conductor cable) required can be damaged in a mine incident and become inoperable

2. Leaky Feeder systems

Leaky feeder communication allows for communication with parties aboveground and/or belowground via use of radiating coaxial cable, a special type of coaxial cable whose goal is to “leak” a signal to walkie-talkies and receive signal from walkie-talkies along its length. While products utilizing this technology do provide two-way communication, the infrastructure can be damaged and thus rendered useless following an incident.

3. Wireless Mesh Networks

Wireless mesh network type systems that utilize 802.11b protocol at 2.4GHz propagated up to 1500 ft. The signals produced don't turn corner wells [16].

4. Medium frequency Systems

System that use medium frequencies have the potential to provide two way voice and data communication. The signals from a medium frequency radio system was found to couple into existing metallic mine infrastructure and could propagate more than one miles [16]. Medium frequency (MF) communication system typically operate 500kHz [3].

A communication device which is capable of transmitting and receiving not only reduce the time required to find miners trapped underground but also give the psychological strength for miners and the confidence to do their job without being worried if they ever be rescued if some disaster occurred in the mine which give them a sense of assurance that their safety is not compromised and is of a first priority. It is for all this reasons that a Through The Earth communication system built for underground communication could be the heart of the mining operation. To do so it must be compact, low power consuming and meet all standard and safety regulations for underground mines.

1.4 Receivers

Generally there are different types of receivers which are used for radio communications. The type of receiver used practically is selected according to the purpose and performance required by the communication system designed. The most popular types of receivers are Heterodyne receiver, superhetrodyne receivers, direct conversion receivers.

1.4.1 Heterodyne receiver

Heterodyne receiver which is also known as conventional receiver is by far the most commonly used receiver used in area of radio communication. Prior to the heterodyne receiver, radio listeners had to constantly play with a set of knobs on a radio to keep locked on the selected frequency of interest. By tuning the LO frequency, the RF frequency to be received can be tuned. The heterodyne receiver makes it much easier to control the LO frequency and filter out unwanted channels at intermediate frequency (IF) rather than to try to filter out unwanted channels at the RF frequency.

To heterodyne simply means to reduce the incoming signal frequency by mixing. In a radio application the AM or FM signal is centered on the carrier frequency to some intermediate value IF. For practical purposes, the heterodyne receiver always reduces to the same value of IF. Accomplishing this requires one to choose the frequency being mixed with the signal so as to keep the difference the same. A representation of heterodyne receiver looks like that shown below as in *Fig 2*.

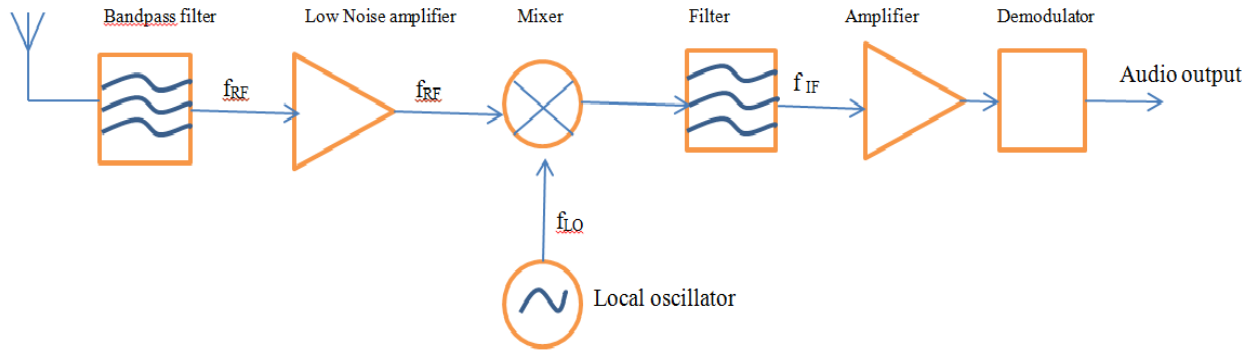


Figure 2 Heterodyne receiver

Conversion of RF signal in to baseband can be done in different ways. In radio communication conversion of an RF signal to baseband requires the use of a mixer to mix the incoming RF signal and change to the Intermediate frequency signal or directly to baseband. An ideal representation of a mixer is shown below where the mixer is shown as a multiplier with two inputs and one output.

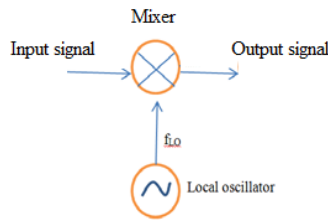


Figure 3 RF mixer and Oscillator

In its simplest application, two signals at frequencies are applied to a mixer and it produces a new signal at the sum and difference frequencies of the original signals. The signal at the output is the vector multiplication of the signals at the two input ports. The first signal is a reference signal and the other input signal is a local oscillator. In practical mixers other frequency components are also produced. Mixers are widely used to shift signal from one frequency range to another. For the convenience of further signal processing the incoming signal can be moved to intermediate frequency or can be directly changed to baseband.

1.4.2 Superhetrodyne receivers

The trade-off between sensitivity (image reject) and selectivity (channel select), can be relaxed by introducing IF to the heterodyne receiver architecture which results in a superhetrodyne receiver. Superhetrodyne receiver also called superheth is by most the popular architecture which allows improved selectivity and higher gain through the use of IF filter and amplifier. At higher frequencies it is often necessary to use two or three IF stages to avoid the local oscillator (LO) stability problem which is to use dual conversion or triple-conversion heterodyne receivers. The structure of the dual conversion Superhetrodyne receiver shown in the Fig 4 includes a second local oscillator and an amplifier to avoid the stability problem of the receiver.

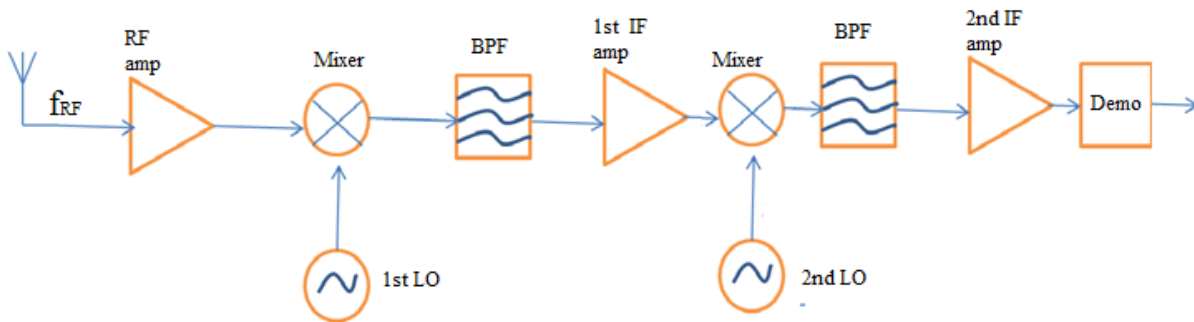


Figure 4 Dual conversion Superhetrodyne receiver

Although superhet receivers are the most popular architecture among most types of receivers used in radio communication, it is not the simplest to build. There are two frequency requirements of the superhet receivers in order to change the incoming RF to a baseband signal. As shown in the figure 4 superhet receivers are used for single sideband reception, it could be either upper side band (USB) or lower side band (LSB). Moreover superhet receivers require a sharp narrow band filter. A pre selector can be used before the superhet receivers for restricting the frequency band that permitted to enter the receiver. The pre low noise amplifier (LNA) components have a direct effect on noise figure, so low-loss is a key characteristic of these parts, because loss adds directly to noise figure. Often, waveguide components are used in front of the LNA because it offers the lowest loss available. The major advantages of superhet receivers can be explained as follows. An obvious advantage is that by reducing a signal from higher to lower frequency, lower frequency components can be used, and in general, cost is proportional to frequency. RF gain at 1 MHz is expensive, while IF gain at 1 KHz is cheaper. The second advantage is in the superior sensitivity of the superhet receivers. Filtering out unwanted signals at IF is a much easier job than filtering them out at RF, because the desired bandwidth is much higher after the signal is mixed down. Further advantage in that many components can be designed for a fixed frequency (and even shared between different receiver designs), which is easier and cheaper than designing wideband components.

An important consideration for superhet receivers on choice of high side LO versus low side LO is in the image frequencies that will be picked up. The choice of high side LO versus low side LO can be made based on the relative quietness of the image band in each case. Also the trade-off between sensitivity (image rejection) and selectivity (channel selection) dictates the choice of the IF in the receiver. High intermediate frequency (IF) selection provides better sensitivity and the image reject filter is easier to implement whereas Low intermediate frequency (IF) gives better selectivity and a channel selection filter is easier to implement. Both the image reject band pass filter and the channel select band pass filter are difficult to implement on a chip, which makes the superhet receivers less attractive. Tunable high-quality factor (Q) filters are difficult and expensive to implement so rather than tuning the BPF center frequency, the LO is changed depending on the desired channel. The superhet receiver relaxes the band pass filter quality factor Q at each stage by having more filter stages. Basically there are three approaches to do channel selection in super-heterodyne receiver, which are Variable LO1 with fixed LO2 which requires very high precision in frequency synthesizer, Fixed LO1 with fixed LO2 which requires very wide tuning range in frequency synthesizer, variable LO1 with variable LO2 which requires both local oscillators to track each other. Since building a filter of high quality factor Q is hard and expensive, it is preferable to build more filters each with lower Q but that requires more mixing in the receive chain which leads to image problems and needs more filters[6].

1.4.3 Direct Conversion (D-C) receiver / detector

A direct conversion receiver is the simplest type of receiver. A local oscillator at the input signal's center frequency f_c creates a mixer output with a frequency of zero at f_c plus and minus

any modulation noise sidebands, and including frequency translated versions of all other signals in addition to noise that are passed by the input filter. Figure 5 show the simple form of direct conversion receiver. The simplicity is obvious, especially when it is compared with the super-heterodyne architecture.

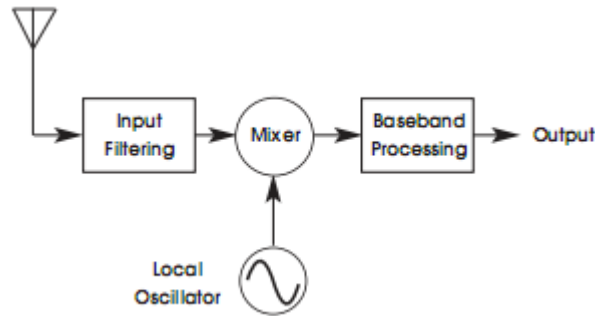


Figure 5 Direct Conversion receiver

The desired signal or information is achieved by processing the signal which is the output of the mixer. All other signal processing functionalities can be applied to the desired signal afterwards. The gain, filtering, limiting and rectification can be performed based on the modulation type which is to be used.

The advantages of D-C receiver are beyond the simplicity of the circuit. The main advantage apart from the simplicity of the D-C receivers starts with the cost. As it can be seen in the figure above the parts count of the receiver has reduced in a significant number in the RF side of D-C radio as compared to superheterodyne receiver. Most of the complexity of D-C receivers is added on the chip when it is manufactured. And the fact that there is no frequency limit when using D-C receiver is another advantage. The D-C receivers operate on any frequency within the bandwidth of the mixer and LO phase splitter. The filter in the front end can be eliminated if necessary. Moreover, the D-C receiver design make it possible to have minimal unwanted responses, which are the result of unwanted mixing products caused by the linearity and imperfect isolation. In D-C only the significant unwanted signals are at the harmonics of the LO, which are far removed from the operating frequency. The architecture of D-C receiver makes it to have high linearity because the distortion is minimized due to a short signaling path as well as the elimination of the narrow IF filter, which usually increases time domain distortion[7].

However the simplicity in the design of the direct conversion receiver is achieved with the limitations. The IF circuitry is a very important in typical superhet. It is where the filtering is implemented where most of the signal path gains are inserted and where the automatic gain controller (AGC) or limiting is added. The front end filter only eliminates frequencies well separated from the f_c , so that an IF usually includes a narrow band filter to separate individual communications channels. In D-C filtering must be done at baseband. If the baseband processing

includes DSP, implementing the necessary filter algorithm is a straight forward matter. The other limitation is Gain distortion. Without an IF, the only options for providing the necessary gain are at the front end and after the detector, at baseband. High gain at the signal frequency is not practical. It is an invitation to oscillation and strong signals can easily exceed the dynamic range of the mixer input. Some amount of front end gain is required, even with a superhet design, to make up for the losses in switching and possible duplexer filters. Providing a lot of gain at baseband is more difficult to D-C. A baseband amplifier must have exceptional power supply isolation and the system must have very low noise on signal, power and ground, such noise is caused by circuit elements such as DC-DC converters, voltage regulators, and digital clocks [7].

The simple D-C circuits use in-phase and quadrature (I-Q) techniques to remove the unwanted image by phase and amplitude balance methods unlike superhet, where one of the frequencies is removed by filtering. Any modulated formats can be recovered using the I-Q technique. With the LO on the operating frequency the input filter will not prevent the LO from passing through to the input. The balance of the mixers becomes controlling factor. An isolator in the input circuitry will further reduce LO feed through [7].

All modulation formats can also be represented using vector techniques, where the signal can be defined in terms of magnitude and angle. Devices using this technique have been developed recently and Software defined radio is one of the devices. To understand the basic principle of inphase (I) and quadrature (Q), it is important to see at first quadrature reception types and techniques.

1.4.4 Software defined receivers

Software defined radio (SDR) technology brings the flexibility, cost efficiency and power to drive the communications forward with wide-reaching benefits. As the processing capabilities of personal computers develop through time more and more functionality of the devices have been transferred to software. This advancement has changed radio communication in recent years as most of the data, voice, video, broadcast, command and control, emergency response communications systems are implemented in software.

The drive to improve the radio communication has led to more dependence on software implementation than on hardware. With the advanced implementation of the software, the popularity of SDR has increased thus avoiding most of the hardware implementation. Most software defined radio use the inphase (I) and quadrature (Q) components of the signal for processing. The processing capabilities will no more be limited by the hardware but by the use of the analog to digital converters like the sound card used in the personal computer.

The digital signal processing performed by software defined radio is dependent on getting the inphase and quadrature component of the signal. Processing two signals rather than one signal has many advantages in software defined radio. Almost all software defined radios including the most zero IF receivers have one thing in common – all of them process two signals containing

the inphase(I) component and quadrature(Q) component of the baseband. It is for this reason a discussion on generation of I and Q signals is important. Moreover the hardware design and implementation used to generate the two signals and how the quadrature generation of the signals is the critical part of the system in the software defined radio will be discussed. An SDR is essentially two direct conversion receivers in one system, see figure 6

As was shown previously, the direct conversion receiver has a band pass filter to ensure that the signal of interest is passed to the mixer. The first signal is generated by mixing the signal of interest and the local oscillator output. Then the output of the mixer is filtered by a low pass filter to get the baseband signal of interest. The processing of the signal is then done on the final received baseband signal. Since this final signal is baseband, the sound card of the personal computer or any analog to digital converter can generally process it into digital format. The second signal is generated from the second local oscillator which is shifted 90 degrees and mixed with signal of interest. In the figure 6 shown below you can see that the second oscillator is shifted by 90 degree from the first local oscillator before passing through the mixer. This is one way of generating the inphase(I) and quadrature (Q) baseband signals. The processing of these two signals is done by software rather than the hardware. There are many ways of generating the inphase(I) and quadrature(Q) components of the signal. The complexity of the circuit also depends up on the method of generating the inphase and quadrature components of the received signal.

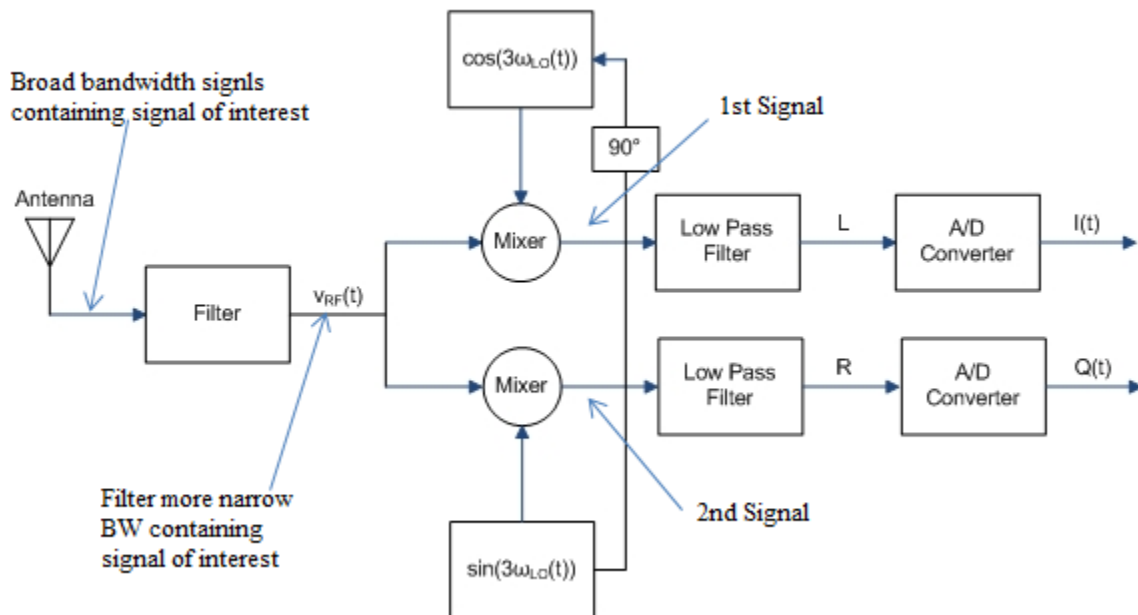


Figure 6 Inphase and Quadrature signal in the SDR front End

The two generated signals can be represented in Cartesian coordinates as in the figure 7 below. And if one were able to see the both the signals in time domain one would see that the signal are phase shifted 90 degrees. There are no strict criteria to classify which one is inphase and which one is shifted 90 degrees (quadrature) but convention has it that the first signal which reached the pick first will be taken as inphase component of the input the signal and second one will be taken as quadrature component.

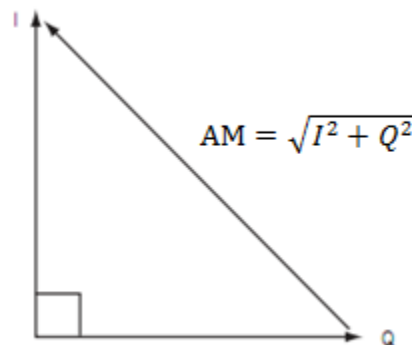


Figure 7 Inphase and quadrature component of an AM modulated signal

The important discussion which may arise at this point is why take the trouble to generate inphase and quadrature signals rather than directly processing the signal we get using typical receivers. The best way to answer this question is that by using the inphase and quadrature component signals one can simply demodulate any kind of modulation being used by using software. The fact that one can demodulate any signal irrespective of the type of the modulation used gives a flexibility and simplification by processing the baseband signal in the software defined radio. The most popular modulation techniques including AM, FM, PSK31 or infact any type of modulation can be demodulated if one has the I and Q components of the signals. Moreover, if we can generate the inphase and quadrature signal we can transmit any type of modulation using the inphase and quadrature components.

A simple illustration for the inphase and quadrature demonstration could be as the example shown above in Fig 7 above. To demodulate an AM signal, after getting I and Q components at the output, simply use the Pythagoras famous theorem about the triangles and take the square root of the sum of I and Q squared. Each of I and Q vectors varies in amplitude with the amplitude modulation on the incoming signal. Hence, the hypotenuse we have formed the I and Q vectors will also vary with modulation. The I and Q signals have passed two low pass filters. Each filter has the same frequency response but the phase of all signals passing through the Q channel is shifted by 90 degree as show in Fig 8 below. If we finally add the two signals we will get single signal with magnitude twice of I and Q for the wanted signal [18].

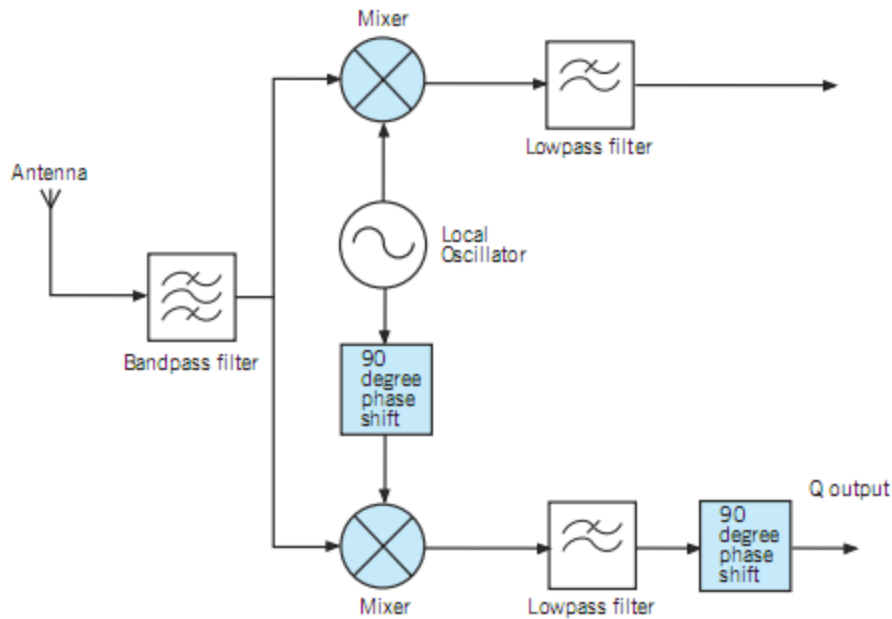


Figure 8 Inphase and quadrature of SDR with Quadrature shifted[18]

For all the above reasons, generating the I and Q signals is important in building any software defined radio. After I and Q are generated the next step will be to process of the received signal. The methods used to generate I and Q may vary depending on the interest of processing the signal. But most radio operators use the famous quadrature sampling detector named “Taylor Detector”.

1.5 Statement of the Problem

This thesis will investigate the use of a Taylor detector at extremely low frequencies. This thesis focuses upon the design, simulation and implementation of this low frequency detector. In this work a Taylor detector for generation of I and Q is designed, simulated and implemented in hardware. The property of Taylor detector is examined by comparing the theoretical design properties with the hardware implementation of the detector.

Chapter-2

2. Tayloe Detector

The power of quadrature signal processing using Inphase(I) and quadrature(Q) signals to receive or transmit using any modulation methods has been explained in chapter 1. Tayloe detector is a simple method of converting a modulated RF signal to baseband so that it can be represented as the inphase and quadrature component. The generated inphase and quadrature components can then be passed to an analog to digital converter (ADC) for further digital signal processing. There are different type of software which are developed by Ham operators to take the inphase and quadrature component as an input and then do further processing of the signal. Since for our application extremely low frequencies are of interest, it is also possible to take advantage of the built in SDR software in low frequency range once the inphase and quadrature components are generated. Efficient detector for getting inphase and quadrature is of extreme importance.

The Tayloe detector is an elegant design used with extremely efficient performance [8]. The design of the detector resembles other types of quadrature signal generations but the high performance with minimal number of components used to build the detector makes it unique. The high performance of the Tayloe detector [14] and its basic properties are discussed in detail so it can be used for comparison of the design, simulation and implementation of the Tayloe detector designed herein.

The Tayloe detector is ultra-low noise, high performance, zero IF quadrature detector. It can also be considered as a preamplifier with unique design which includes the amplification of the signal while deriving the inphase (I) and quadrature (Q) components. The RF signal is connected through a common resistor to one of four sampling capacitors. The multiplexer is commutated at a rate which is four times the frequency of interest for detection. Each capacitor will be tracking the RF carrier amplitude for one quarter of a cycle and will hold the value for the remainder of the cycle as the switch is turning at exactly the RF carrier frequency. The RF carrier will then be sampled at 0, 90, 180 and 270 degrees. The function of the Tayloe detector can be thought of as a rotary switch which has four positions rotating at carrier frequency rate. The setup will allow for each capacitor to see the input signal only for a quarter of a cycle and hold the amplitude for the rest of the cycle. The detection frequency at which the capacitor sees the value of the input signal is the desired detection frequency [9].

The basic product detector is shown in the figure 9 in which F_c and F_s represents the carrier frequency of the signal and the commutating frequency of the rotor respectively [8]. The capacitor voltage sampled will be a DC level which is equal to the average value of the voltage when the carrier frequency and the rotating frequency are exactly inphase. Since the resistor and

the capacitor forms a low pass filter as shown in fig 10 for the quarter of the cycle, each of the sampled signal represents an average voltage during the respective cycle. At the time when the switch rotation frequency is equal to the carrier frequency the differential sum is taken from 0 and 180 degrees sampling capacitors would be a DC output voltage level two times the individually sampled amplitude on each capacitor.

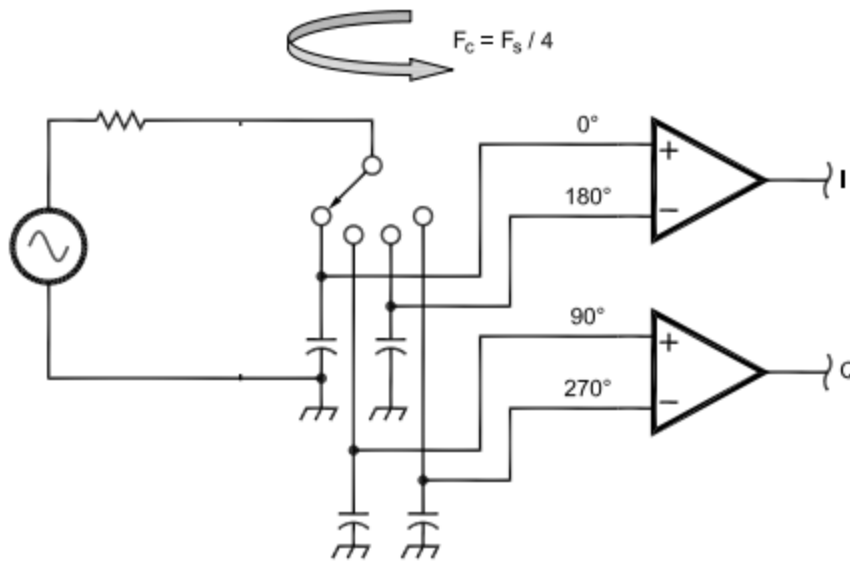


Figure 9 Detector diagram[8]

Conversion loss is a measure of the efficiency of the mixer in providing the translation from the RF input signal to the IF output signal. Conversion loss is defined as the ratio of the RF input power to the IF single sideband output power, expressed as positive in dB. Generally, the output of mixers is the difference and sum frequencies. In most zero IF application since the sum frequency is filtered and the difference frequency is used the typical conversion loss using ideal mixer is at least 3dB with common conversion loss values greater than 3dB. Conversion loss is expressed as

$$\text{conversion loss} = -10\log\left(\frac{P_{RF}}{P_{IF}}\right) \text{ , unit is dB} \quad (2)$$

The Tayloe detector design which is not actually a mixer, the maximum detected voltage will be approximately 0.9 times the peak voltage of the sine wave when integration over the peak quarter cycle of the sine wave is performed. Hence the detection loss is about 0.9dB [14]. The detection voltage on the capacitor will drift with time following the difference frequency

between the incoming signal and the detection frequency of the incoming signal when incoming signal is shifted slightly from being exactly the detection frequency.

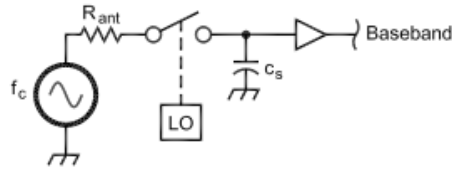


Figure 10 The RC low pass filter formed by the sampling capacitor and resistor

The capacitors acts like a baseband detector where the first capacitance acts as baseband product detector at 0° , the second capacitance detects at 90° and with other capacitors detection at 180° , and 270° degree respectively. The other two capacitors hold information redundant with what has been detected on the first two. If a differential sum is taken on 0° and 180° detections an inphase signal will be produced, likewise the 90° and 270° will also combine to form the quadrature signal. For the purpose of getting lower noise figure (degradation of signal to noise ratio caused by detector components) at low noise gain setting the differential summing can be done using low noise operational amplifier. But also using low noise operational amplifier also has the disadvantage of that that inverting input will be at virtual ground and the non-inverting input will be at high impedance. For this reason an instrumentation amplifier can be used to solve this problem as an option [11].

All signal representations converted to baseband will be accurate if the output frequency will vary accordingly to the beat or the difference frequency between the RF carrier and the switch rotation frequency. So, a shift of the RF carrier away from the sampling frequency will be accompanied with result that the values of the inverting phases not to sum to zero. Though the value of the antenna impedance varies significantly with actual antennas, the input resistance of the op-amp gain is set by the antenna impedance which forms the input resistance to the op-amp. The gain then will take into the effective resistance in the R-C network as the duty cycle of the switch is 25% and doesn't only take a single resistance in the path. Therefore the effective resistance in the network is the antenna impedance multiplied by four in the op-amp gain calculation as shown below [8].

$$G = \frac{R_f}{4 * R_{ant}} \quad (3)$$

Where R_f - feedback resistor to Op-amp, and R_{ant} - antenna impedance

All the components with series resistance must be taken in to consideration for computation of the frequency roll off. The effective resistance is not only the filter input R, but it also includes the system impedance, R_{sys} , and the switch resistance, R_{switch} . The frequency roll off can then is set with selection of the resistance and the capacitance.

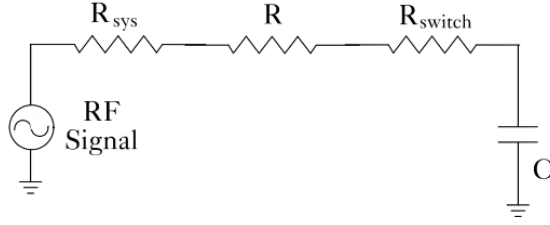


Figure 11 Equivalent input impedance of the Tayloe detector

The detection capacitor sees the effective resistance only for a quarter of a cycle. The effective resistance for calculating the roll off will be four times the sum of all the resistors in series which is $4 \times (R_{sys} + R + R_{switch})$ [14]. The selection of the single signal from all those spread out in the reception spectrum is the main function of the receiver. In order to remove the undesired signals from the signal band of reception a bandpass filtering is usually done on the RF signal at the input of the detector. The bandpass filtering is normally fixed tuned and as such provides no in band protection from signals with the desired frequency.

The selectivity provided by the detector is superior to that provided by band wide bandpass filtering and it is centered about the detection frequency. The selectivity of the detector provide some margin of free selectivity against both adjacent channel and out of band stops.

The Tayloe detector operates as a very high quality factor (Q) tracking filter; it can also be analyzed as a commutating filter. The bandwidth, BW, is dependent on values of n , R_{ant} , C_s where, n is the number of sampling capacitor, R_{ant} is the antenna impedance, C_s is the value of the individual sampling capacitor, Equation (4) below shows how to determine the bandwidth of the detector[8].

$$BW = \frac{1}{n \cdot \pi \cdot R_{ant} \cdot C_s} \quad (4)$$

The figure of merit is measured by the value of the quality factor Q of the filter. The higher value for this figure of merit corresponds to a narrower bandwidth, which is desirable in many applications. More formally, Q is the ratio of the power stored to the power dissipated in the circuit reactance, and resistance respectively.

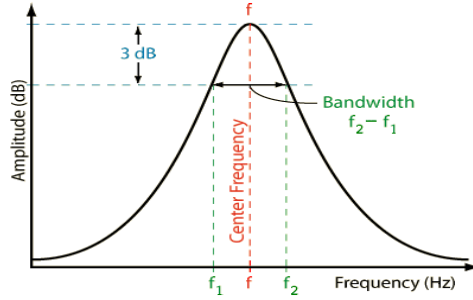


Figure 12 Bandwidth measure for the quality factor

The bandwidth BW of the signal shown in fig 12, would be

$$BW = f_2 - f_1 \quad (5)$$

The quality factor, Q, of the signal using f as the center frequency would be

$$Q = \frac{f}{BW} \quad (6)$$

Typically mixers have a conversion loss 6-7dB. A Tayloe detector has less than 1dB conversion loss [11]. This is because the Tayloe detector is not a mixer but a sampling detector in the form of a quadrature sample and hold. Though it is similar with mixing the sample and hold actually holds the signal in between samples and the output will not go to zero unlike mixers in which the output signal is zero for half of the time because the clock source used is square wave.

Noise Analysis for Tayloe Detector

The system noise at RF input in an Optimum Tayloe detector is expressed as [11]

$$N_{\text{sys}} = -174 + 10 \log(BW) \text{ dbm} \quad (7)$$

$$\text{or } N_{\text{sys}} = \frac{0.45}{\sqrt{\text{Band Width (BW)}}} \text{ nV} \quad (8)$$

Wher: BW is the bandwidth of the receiver in Hz. N_{sys} = System noise

It can be seen that the noise is a function of the bandwidth. At each of the four input of the amplifiers the noise seen is reduced by 0.9 dB which is almost the same as the loss of the detector.

Assuming that both preamplifiers each have the same gain, G and built in noise, Np. At the output of the preamplifier, there will be one noise term for preamplifier and two for system noise as seen by each of the two inputs. For single preamplifier output, this noise will be [14]

$$(\sqrt{((2 * 0.9 * .45)^2 + (Np)^2)})(G\sqrt{BW}) \quad (9)$$

If the both of the preamplifiers are used to create one signal, the composite term will be

$$(\sqrt{((4 * 0.9 * .45)^2 + 2 * (Np)^2)})(G\sqrt{BW}) \quad (10)$$

The sample noise calculation using the noise equation and the signal equation can be expressed as follows. The signal level necessary to produce the output signal equal to the output noise is calculated as [14]

$$0.9 * S * 4 * G = (\sqrt{((4 * 0.9 * .45)^2 + 2 * (Np)^2)})(G\sqrt{BW}) \quad (11)$$

Solving for S in the above equation

$$S = (\sqrt{((4 * 0.9 * .45)^2 + 2 * (Np)^2)})(G\sqrt{BW}) * (\sqrt{\frac{BW}{3.6}}) \quad (12)$$

The reference below shows the signal to noise ratio required to reach the roll off frequency. The table entries demonstrate the importance of a very low noise baseband preamplifier on the overall sensitivity of the receiver. The System noise and signal noise required to reach a 3dB (S+N)/N ratio is as shown in the table below [14].

System Noise @ Bw=1000Hz	Preamplifier Noise (nV/SqrtHz)	Signal level for 3 db S+N/N
14.2 nV / -143.8 dbm	9	113 nV / -125.8 dbm
14.2 nV / -143.8 dbm	4	55.3 nV / -132.0 dbm
14.2 nV / -143.8 dbm	2	34.8 nV / -136.0 dbm
14.2 nV / -143.8 dbm	1	27.3 nV / -138.1 dbm
14.2 nV / -143.8 dbm	0.8	17.3 nV / -142.1 dbm

Table 1 System input noise VS signal noise

Without the use of RF preamp when the detector is coupled with ultra-low noise device such as LT1115 it is practical to build a receiver that can receive a signal with a 3dB signal to noise ratio that is only 1.7dB above the system noise without the use of RF opamp[14].

2.1 Single balanced vs double balanced detector

In addition to the baseband signals the frequency content of output of a mixer also contains the RF carrier frequency and the local oscillator frequency. Mixer types which have no input to output isolation are called unbalanced mixers. Based on the frequency content allowed or blocked mixers can be classified as single balanced and double balanced.

Single balanced mixers are constructed by phasing two unbalanced mixers which allow the cancellation of the input at the output. The RF input is usually chosen as the cancelled output as the local oscillator is just one signal and at a known frequency. Two singly balanced mixers can be phased together to cancel the other input at the output of the mixer. This way, both the local oscillator and RF input are kept from the output. The choice is mainly economic. The mixer that minimizes the total system cost is usually chosen for low cost receivers. This includes the cost of mitigating the effect of the unwanted outputs [17].

The advantage of balanced mixers over single device Mixers are

- Rejection of spurious responses and intermodulation products
- Better LO to RF , RF to IF and LO to IF isolation
- Rejection of modulation noise in the LO

The disadvantage of balanced mixers is their greater LO power requirements. Balanced mixers are often used to separate the RF and the LO ports when their frequency overlaps and filtering is impossible. In practice a perfect double balanced mixer can give 10dB to 30dB isolation without any filtering [17].

Double balanced mixers have higher Conversion loss (or lower gain) than single balanced mixer and lower limiting maximum frequency but have broader bandwidth. The other advantages of a double-balanced mixer over a single balanced mixer are increased linearity, improved suppression of spurious products and the inherent isolation between all ports. The reason for increasing in linearity is easily understood; the incident power is simply shared amongst at least twice as many active components, thus increasing the signal handling capability.

The disadvantages of a double balanced mixer are that they require a higher level LO drive and increased complexity. The conversion gain is sensitive to the unloaded Q of the inductors. The more inductors, the lower the conversions gain (higher insertion loss). The roll off frequency of the inductors affect the conversion gain, if the LO is close or signal is far from RF signal.

The tayloe detector implementation can be done either as single balanced detector or as double balanced detector. Though both implementations are used for generation of the inphase(I) and quadrature(Q) component of a signal, the main difference is the bandwidth selection in addition to other advantages mentioned above.

The tayloe detector the bandwidth is given by

$$BW = \frac{1}{n*\pi*R_{ant}*C_s} \quad (13)$$

The same bandwidth calculation method can be used for both single balanced and double balanced detectors except the value of the total number of sampling capacitors (n) is different in each case. In the case of the single balanced detector, the total number of sampling capacitors is four. In the case of the double balanced detector the value of the total number of sampling capacitors (n) is two because the sampling capacitor is selected twice during each commutation cycle in the double balanced version.

2.2 Tayloe Detector components

The detector simulated and implemented in this paper is a single balanced detector as discussed in the paper [8]. The implementation of the detector can be classified in three main parts. The clock which generates the inphase and quadrature clock for the detector, the detector which is a 1:4 FET demux switch and the amplifier which consists of the low noise op-amps. The first task was to implement the clock required by the detector. The clock source is a 74AC74 dual flip flop which is used as Johnson counter. The 74AC74 is a dual D flip-flop connected back to back and used as a divide-by circuit. The output then is one fourth of the input clock provided to it. An input clock from a local oscillator is thus divided by four giving two phase shifted clock outputs. The phase shifted clocks are identical except for the phase difference. These outputs from the 74AC74 will be used as two phase shifted clocks [CLK1] and [CLK2] for the detector.

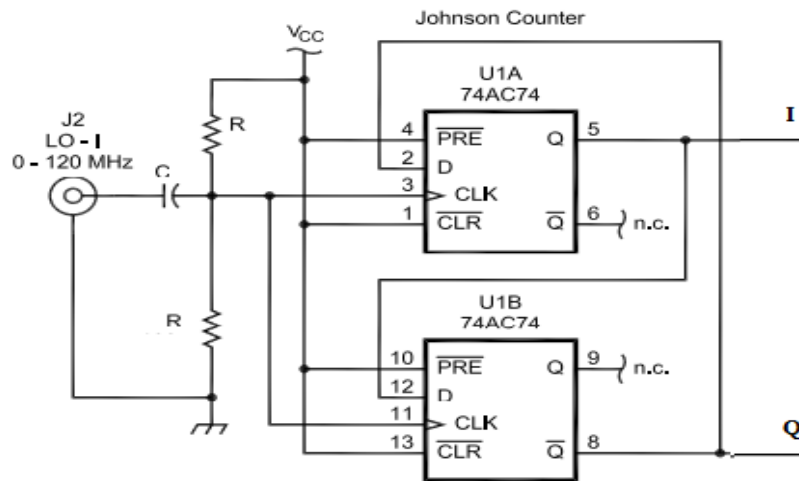


Figure 13 74AC74 clock operation and connection [8]

A Johnson counter is a modified ring counter in which inverted output from the last flip flop is connected to the input of the first flip flop. The outputs cycle through a sequence of bit-patterns. The MOD or the number of unique states of the Johnson counter is $2n$ if n flip-flops are used. The main advantage of the Johnson counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD [10]. The Johnson counter can be

implemented both in D flip flop and J-K flip flop. The 74AC74 is dual D- type positive edge triggered flip flop. The sequence of the output of the counter is 00, 01, 11 and 10 or 00,10,11,01.

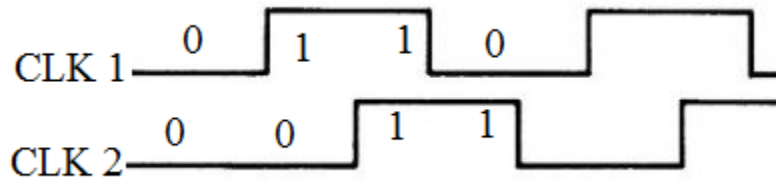


Figure 14 clock sequence input

After the clock is generated, it is connected to the detector IC, the dual 1:4 demux. The dual 1:4 demux is connected to the op-amps last stage of the amplification where the two inputs are summed differentially to give an output of the inphase(I) and quadrature(Q). There are different options of switches to be used as a demux for the detector circuit. The demux used for implementation in this work is Pericom’s PI5V331. The connection of the PI5V331 is as shown in the figure below.

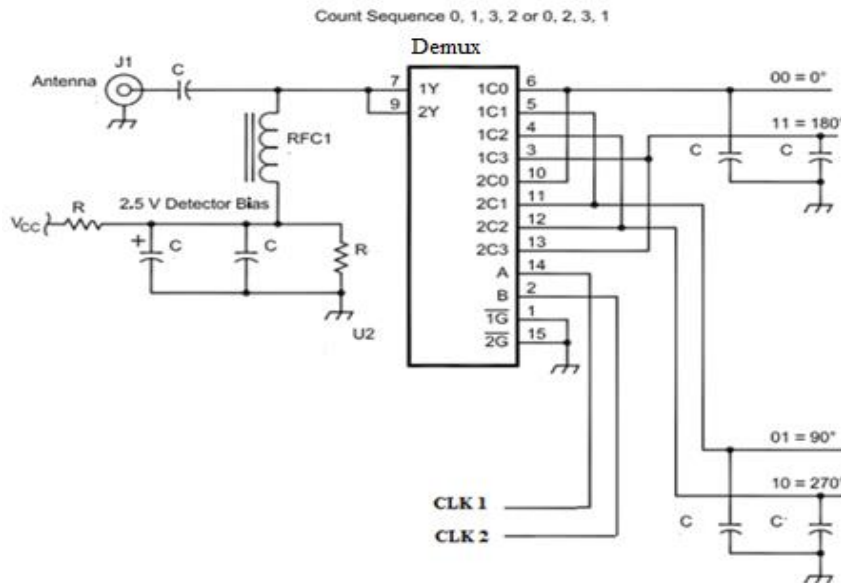


Figure 15 A 1:4 FET Demultiplexer [8]

Another option for a 1:4 FET demultiplexer other than PI5V331 is NXP semiconductor’s FST3253. Many ham operators have built their own version of Tayloe detector with this FET. The PI5V331 was chosen here because of its availability. Both the FST3253 and the PI5V331

are dual 1:4 FET demuxes. The internal layout and operation diagram is shown in the figure below.

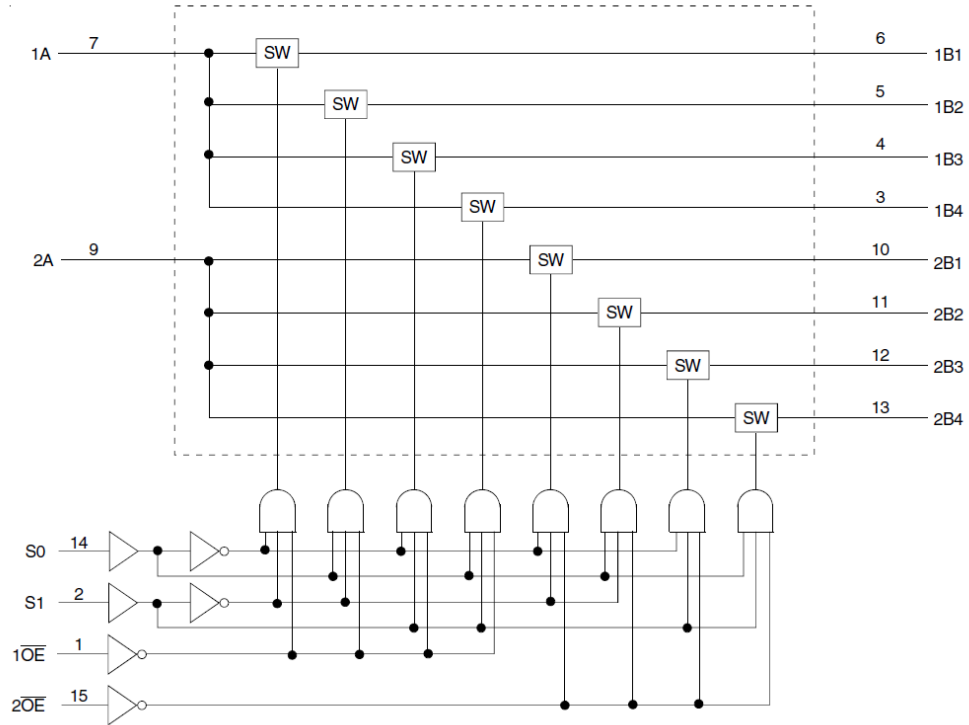


Figure 16 Connection diagram of the FET

Since most of the spice software used for simulation doesn't have either the PI5V331 or the FST3253 as part of their components, the spice simulation of the demux is done according to the connection and functionality diagram shown above. Both pin number 7 and pin number 9 are the input pins. When an input signal is connected to the either of the input pins, according to the selection of the clock on pin number 2 and pin number 14, one of the outputs will be selected from the output pin numbers 1b1 to 4b1 and 1b2 to 4b2 . Though the above connection diagram shows the connection as two input and eight outputs controlled by two clocks , in the design and implementation of the detector the two inputs are shorted and the output are also shorted accordingly.

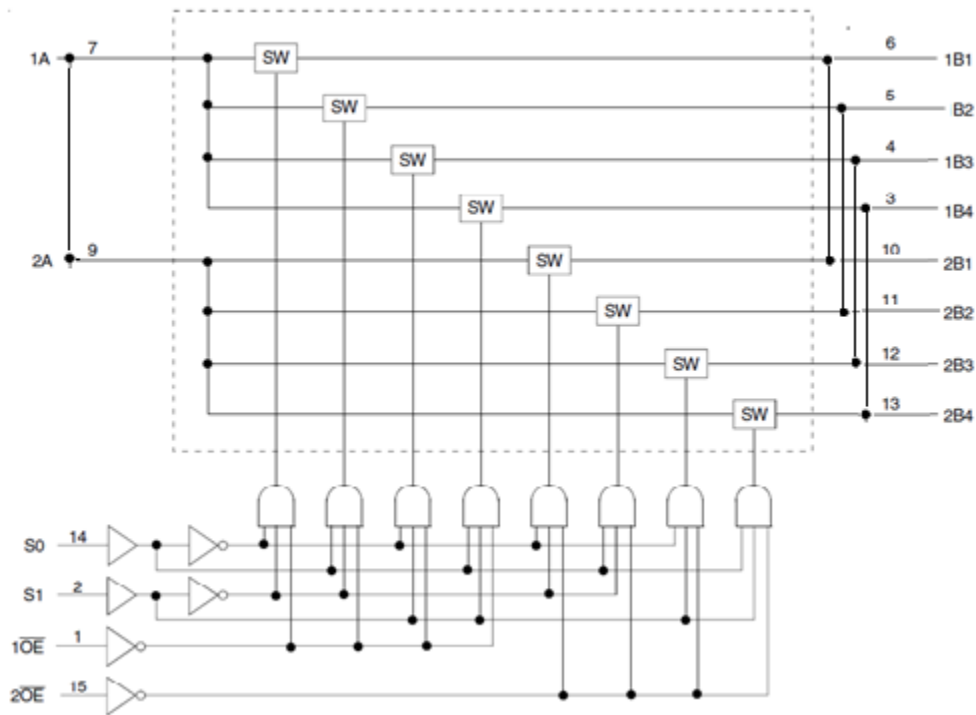


Figure 17 FET connection for the detector

The output of the demux will be then integrated in each of the four capacitors for a quarter of a cycle before being given to the input of the op-amp. The op-amp which is the last part of the detector take the sampled and integrated input in each quarter cycle from the demux and then amplifies differentially the inphase and quadrature components.

The op-amps used are ultra-low noise op-amps that form the I and Q outputs respectively. The antenna forms the input resistance for the op-amp gain so the impedance may vary significantly with the actual antenna. To eliminate the gain variance with the antenna impedance an instrumentation amplifier can be used instead of the low noise op amp. The primary advantage of the low noise op-amp is that it can provide a lower noise figure at the low gain settings. Its disadvantage is that the inverting input of the op-amp will be at virtual ground and the non-inverting input will be high impedance. This means that the sampling capacitor on the inverting input will be loaded differently from the non-inverting input. Thus, the respective passbands of the two inputs will not track one another. This problem is eliminated if an instrumentation amplifier is used. Another advantage of using an instrumentation amplifier as opposed to an op amp is that the antenna impedance is removed from the amplifier gain equation. The single disadvantage of the instrumentation amplifier is that the voltage noise and thus the noise figure increases with decreasing gain [11].

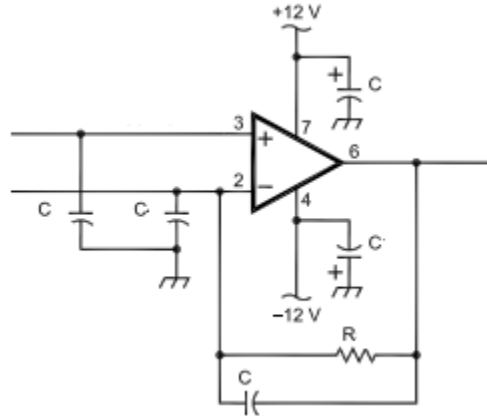


Figure 18 Sampling op-amp inputs

LT1115 op-amps are used for the implementation of the Tayloe detector. The reason for selection is because these op-amps are low noise op-amps. The current state of ultra-low noise amplifiers is typically a noise level in $0.8nV/\sqrt{\text{Hz}}$. This is represented by devices such as the LT1115.

2.3 Design Consideration for Tayloe Detector (QSD)

The quadrature sampling detector is really a direct conversion receiver which gives 90 degree apart inphase(I) and Quadrature(Q) at or near 0Hz . The local oscillator clocks come from the LO divider on CLK1, and CLK2. The quadrature sampling detector takes the “RF” from the bandpass filter stage and down converts to the baseband. The quadrature sampling mixer, actually a commutating switch, clocked by the two clock signals from the dividers outputs the difference of the incoming RF against the clock. The effect is to down convert the incoming RF in to its quadrature analogues at frequencies ranging from 0 to roughly low frequency. These quadrature pairs are then fed to the op-amp stage.

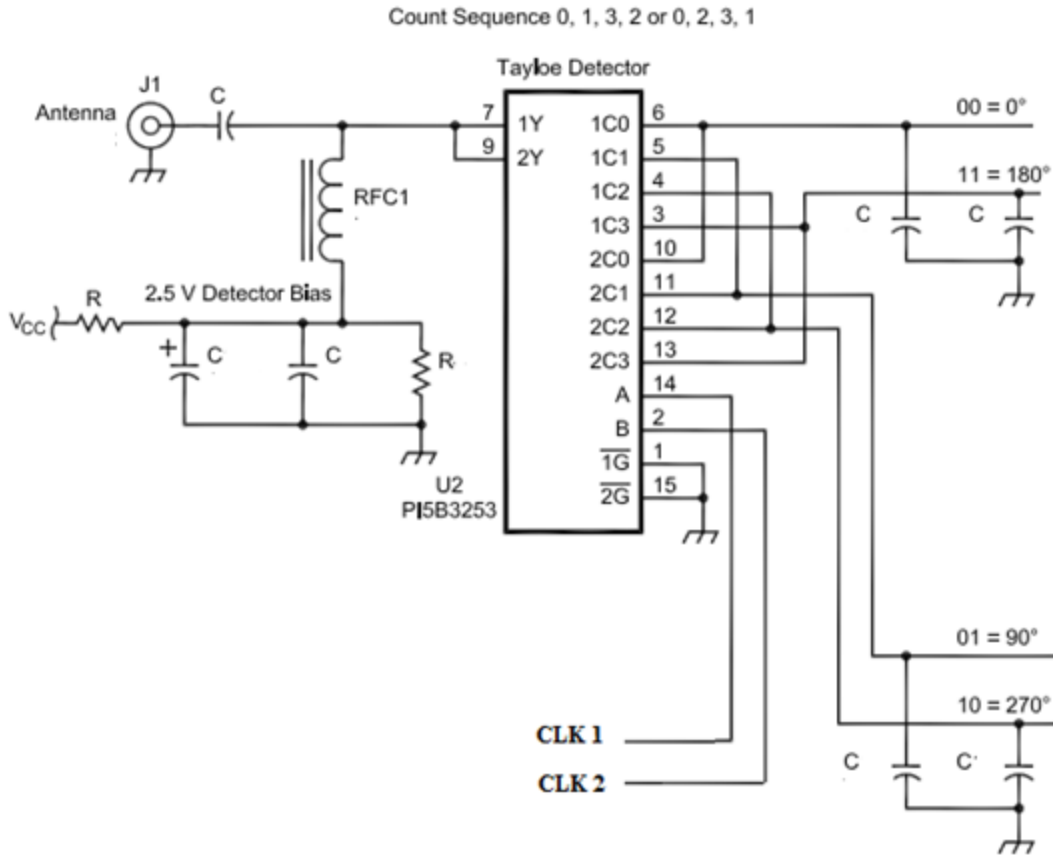


Figure 19 Detector connection

2.3.1 Theory and Design

The QSD is really a sample and hold with each capacitor sampling at $\frac{1}{4}$ of an LO frequency. The conversion loss, bandwidth, the quality factor can be calculated as follows:

- Consider R and C for charging circuit
 - o Smaller $\tau = R \cdot C$ will allow the output to follow the input faster
 - o If τ is too fast, the RF to output frequency ratio increases
 - o If τ is too small, there is a little signal at the output

The equivalent resistor is the sum of three resistors

$$R_{\text{total}} = R_{\text{sys}} + R + R_{\text{switch}} \quad (14)$$

Where R_{sys} = system resistance, R_{switch} = switch resistance

Assuming the resistance of the switch and the series resistor to be zero, the resistor will only be R_{sys} . For maximum power transfer and easier design of the low pass filter and the receiver band pass filter, the impedance the antenna sees taken to be equal to the antenna impedance of 50

ohm. The value of R_{sys} is then taken to be 50 ohm which means that the total resistor (R_{total}) value will be 50 ohm.

Conversion Loss

- Conversion loss of a mixer is equal to the ratio of the IF single sideband output to the RF input level [12].

$$conversion\ loss = 20 \log \left(\frac{V_{IF}}{V_{RF}} \right) , \text{ in dB} \quad (15)$$

- The suggested value of the conversion loss for Tayloe detector is 0.9dB[14]

Bandwidth

Considering the simulation and implementation of the single balanced Tayloe detector, the bandwidth is given as

$$BW = \frac{1}{n * \pi * R_{ant} * C_s} \quad (16)$$

The value of $n=4$ for singly balanced.

As an illustration for 3 KHz bandwidth of a 14MHz receiver. If R_{sys} is 50 ohms, and both R and R_{switch} are assumed to be zero, a detection C of $0.5\mu F$ yields a 3 dB low pass filter bandwidth of 3 KHz.

Quality Factor - The quality factor of the detector is a measure to show how good the detector is getting the desired output signal. It is given as

$$Q = \frac{f}{Bw} \quad (17)$$

For the 3 kHz bandwidth and 14MHz receiver the quality factor would be

$$Q = \frac{14 \times 10^6}{6 \times 10^3} = 2333$$

This shows that the quality factor of the detector is highly affected by the bandwidth of interest to be chosen as a baseband by the detector. The smaller the bandwidth the higher is the quality factor for the filter which means a filter with high quality factor would be more able to receive the signal in the required band. Moreover a filter with higher value of quality factor (Q) will work better with a narrow bandwidth, so the selectivity of the filter is high whereas filter with the lower quality factor would have wider bandwidth and less selectivity.

As it can be seen in the simulation section of this work, building a receiver which has high quality factor and high selectivity is challenging for a receiver which receives a low frequency signal. The other limitation when going to low frequency is the stability of the clock source. The 74AC74 is not able to generate a clean clock and cannot be used as clock source for divider outputs less than 2 KHz.

The design procedure for the low frequency is detailed as follows. To receive a bandwidth of 104 Hz, first we should calculate the value of the capacitor

$$Bw = 104\text{Hz and } R=50\Omega$$

$$C_s = \frac{1}{4*\pi*R*Bw}$$

$$C_s = \frac{1}{4*\pi*50*104}$$

$$C_s = 0.15303 \times 10^{-4}$$

$$C_s = 15\mu\text{F}$$

Since the receiver of the whole detector is built for 2 KHz the oscillator frequency would be $2 \times 4 \text{ kHz} = 8 \text{ kHz}$ and the clock generated from the Johnson counter would be 2 kHz. For the same reception parameters the quality factor of the filter would be

$$Q = \frac{2 \times 10^3}{104} = 19.2$$

It can be seen that the quality factor of the filter drops significantly causing the filter to have low selectivity. A low quality factor filter is only good for operation where a high bandwidth requirement is important. The frequency of interest is low frequency so the option chosen was to use a filter with low quality factor and generate the inphase and quadrature components of the signal. As the frequency limit is going down and down the filter quality factor goes worse and the detection bandwidth also gets smaller and implementation of the detector with hardware is difficult.

Chapter-3

3. Simulation of Tayloe Detector

3.1 Simulation of Tayloe Detector using Matlab

The purpose of the simulation is to do all the functionality of the Tayloe detector by receiving a signal through the sound card or analog to digital converter process and generate the inphase and quadrature components of the detector. The difficulty of getting a stable clock source which can generate a very low frequency clock and the fact that the quality factor of the designed detector goes very low when a test at low frequency is done in hardware leads to more easily implementing the detector in software for comparison. The only challenge for the simulation was to get a large enough signal level for the sound card to pick and process it. For this reason a separate pre-amp was built for the RF carrier to send it to the sound card.

A simulation model for the Tayloe detector can be implemented with different simulation tools. The inphase(I) and quadrature(Q) generated outputs can then be sent to the stereo outputs of the sound card from the digital to analog converter. The tools considered as an option for simulation were C++ and Matlab. C++ was chosen first because it is a compiled language and on the idea that the signal processing should be faster than an interpreted language like Matlab. But the design of filters and integration with the Tayloe detector simulation turned out to be easier in Matlab than doing all the processing and integration with C++. The Simulink is used as part of the Matlab simulation section as most of the components and toolboxes already have built in functionality for filtering and sampling which is needed.

The model used to simulate the detector in Simulink can be viewed as a combination of signal source and sample and hold circuits. A sine wave source and the 90 degree shifted version of the sine wave is given to the sample and hold, while the local oscillator connected to the sample and hold will generate the clock to sample the signal. The output signals will be the difference frequency of the input signal and the clock source. A vector scope is used to see the spectrum of the signal in frequency domain.

The basic idea used to implement the detector in simulation using Matlab is the sampling theorem. The sampling theorem states that the minimum sample rate at which one can completely recover the input signal is called Nyquist rate. This is two times the maximum input frequency. If the sample rate of the sampling switch approaches the input frequency of the signal, mixing behavior will result. For example if a signal is sampled at sample rate of 100Hz and the frequency of the signal being sampled is 110Hz, the frequency that we see at the output of the sampling will be 10 Hz as shown below. The sample and hold using the pulse generator as clock sources samples the signal and a signal having a frequency of the difference between the input and the clock is generated as if a mixing is performed between the two signals.

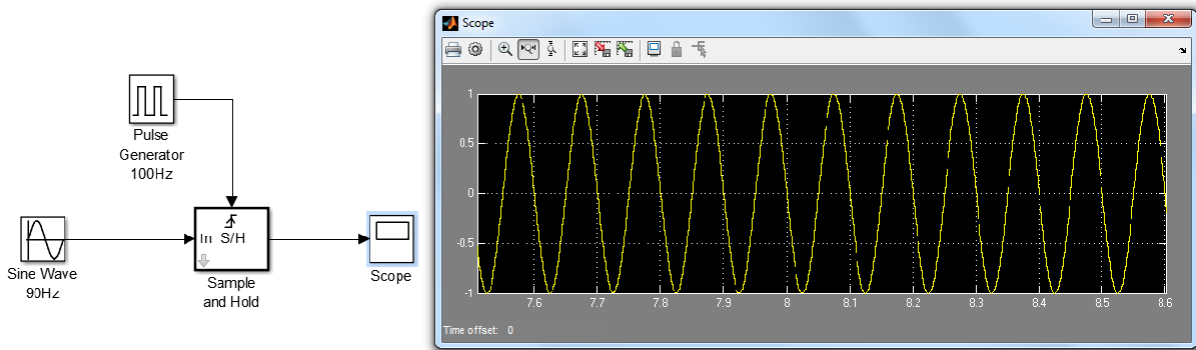


Figure 20 Signal sampled at higher frequency

Similarly if we use the same sampling rate of 100Hz and we sample a signal which has a frequency of 90Hz, the output will be the same 10 Hz signal as shown in the figure below.

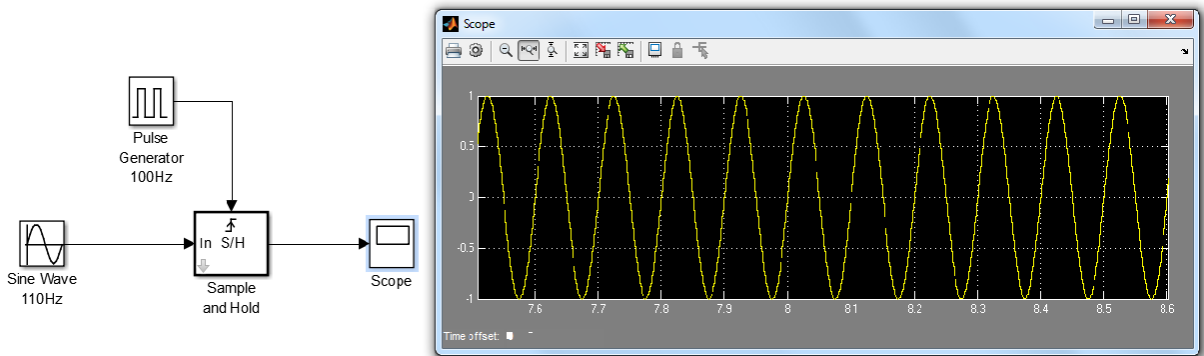


Figure 21 Signal sample at lower frequency

If we see the sampled signal separately it is not possible to tell which signal is shifted which signal is not shifted. But, by looking both outputs in the same scope it can be easily seen that the signal sampled with a sampling rate frequency lower than the input signal is shifted by 180 degree[13]. We can apply the same concept in order to generate the inphase(I) and quadrature(Q) signal. If one has two sample and hold circuits which are shifted in time by 90 degrees, one will have two outputs in which the output which is not shifted by 90^0 will give the inphase and the other output which is shifted by 90^0 will give the quadrature output.

The quadrature sampling detector can be simply represented using blocks from Matlab Simulink. At this stage of the simulation no external signal is taken from outside but a signal which is similar to the RF carrier is generated and modeled using a sine wave block. This signal is used as the RF carrier input to the sample and hold circuit. But when doing the final simulation a signal picked by an antenna will be used as input to the detector circuit rather than a simulated or generated sine wave. The modeled sine wave input and the sample and hold block are connected as shown below

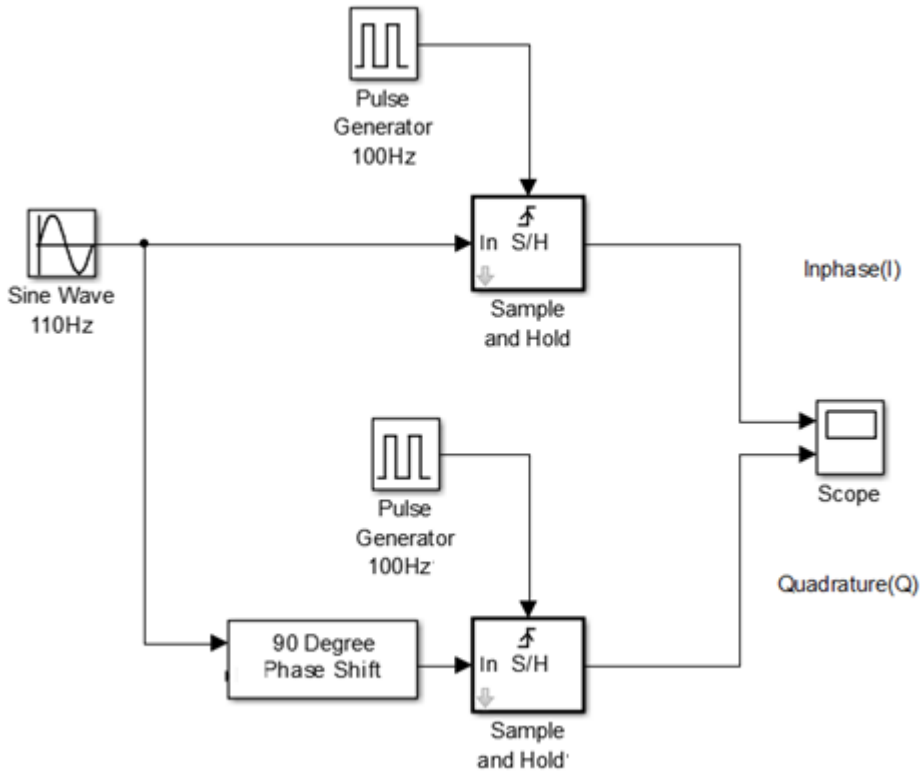


Figure 22 Taylor detector (quadrature sampling detector) Simulink block representation

After generating the inphase(I) and quadrature(Q) components of the signal the next step is to communicate with the sound card to send the generated inphase(I) and quadrature(Q) components of the signal. Before sending the data to the sound card the sampled data must be converted to analog data. A mathematical model for reconstruction of the sampled signal to a continuous signal can be done by using a zero order hold (ZOH) block. A zero-order hold reconstructs a continuous time waveform from a sample of sequence $x[n]$ assuming one sample per period time interval T :

$$x_{ZOH}(t) = \sum_{n=-\infty}^{\infty} x[n] \cdot \text{rect}\left(\frac{t - \frac{T}{2} - nT}{T}\right) \quad (18)$$

Where: $\text{rect}(\)$ is a rectangular function $\text{rect}\left(\frac{t - \frac{T}{2} - nT}{T}\right)$ is time shifted and time scaled rect function

$x_{ZOH}(t)$ is a piecewise constant signal

At the block representation of the detector one of the inputs given to the sample and hold circuit is the phase shifted input to the second sample and hold. In order to create the 90° phase shift for a signal used in Simulink the block used for this purpose is the variable time delay. But using

the variable time delay requires updating the parameter when the simulation is done for different frequencies. The setting of the variable time delay is also dependent on the simulation time and when a simulation is executed the appropriate simulation time and the variable time delay parameter should be selected.

The next part of the communication is connecting the continuous signal to the sound cards. A Simulink block “To Audio Device” is used to communicate with the sound card. The block has an option for the selection of the number of channels used and sampling rate used in each channel connection created. By setting the buffer size appropriately a continuous signal will be sent to the sound card left and right channels. The full Tayloe detector block including the different output display and parameter setting will look as shown below.

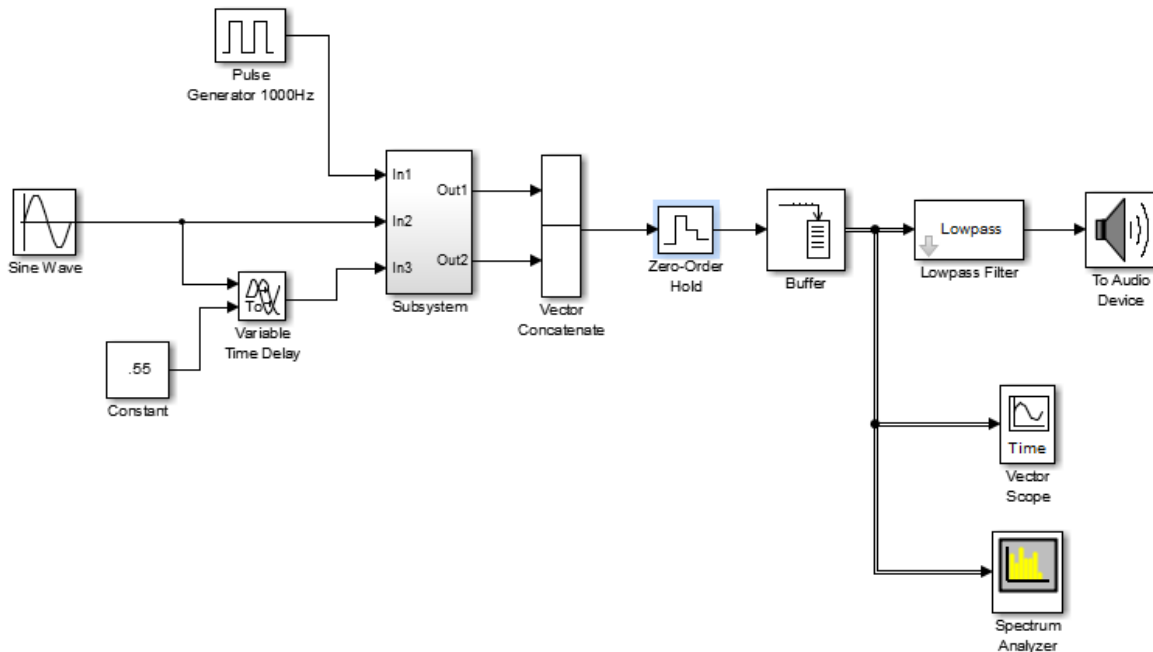


Figure 23 Quadrature sampling detector with sound card communication

The subsystem in the above figure shows the main parts of the Tayloe detector which are the sample and hold connection together with the pulse generator used as clock as show below.

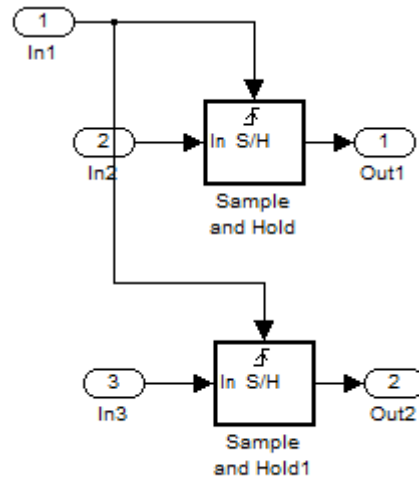


Figure 24 Taylor detector subsystem

A uniform noise is also added with the input during simulation to simulate a better real time environment for the generation of inphase and quadrature components of the input signal. The pulse generator is used as clock source for sampling when the received signal is to be sampled. The final implementation of the simulation also includes notch filter and a preamp section for the received signal before it is given to the detector. A Simulink block “From Audio output” is also used to simulate the reception of the real signal through the soundcard.

The full implementation of the simulation requires two computers at its current configuration. The first computer takes input from the microphone terminal, process, generate, and send the inphase (I) and quadrature (Q) components. The receiving end of the computer will run software defined radio software, HSDR/HPSDR and display the waterfall, spectrum and all other information's of the signal. The HSDR/HPSDR software is the tool which can be downloaded for free and it has been used by many amateur radio operators to receive different high frequency radio signals.

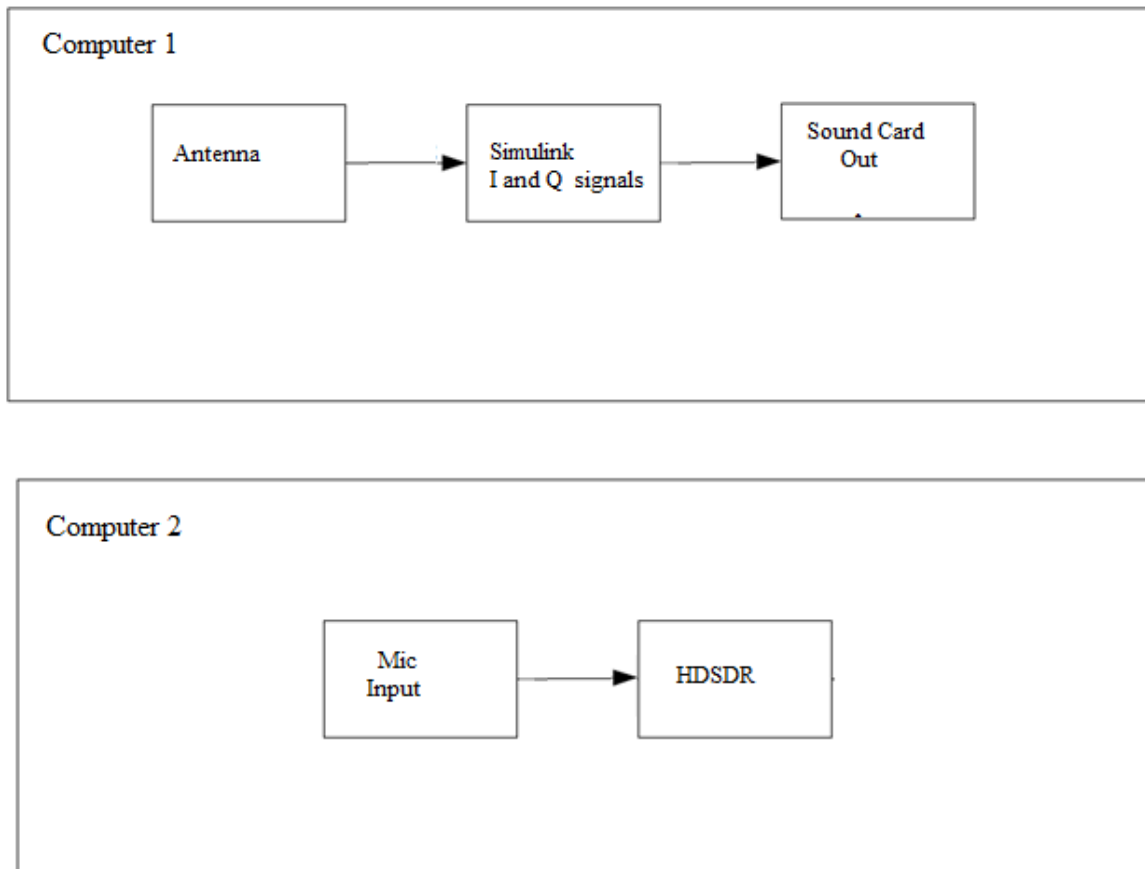


Figure 25 Full system using two computers

The other option is to use one computer for generation of I and Q and use high performance software defined radio (HPSDR) for signal processing. Used by many radio amateur (Hams), HPSDR is a next generation software defined radio where a modular approach of hardware and software integration is used for signal processing. The hardware consists of Magister(Ozy), an FPGA based interface controller card that provides a high speed USB2.0 interface, as well as limited additional I/O lines intended for radio control (e.g. band switching,. The second component of the HPSDR is Mercury board which is used for sampling. The sampling rate of the board is 0-65MHz spectrum. The mercury board contains its own FPGA to undertake digital down conversion to 250kps or less to transfer over the Atlas bus to the USB interface of the OZY board [19].

The functionality of the of the high performance software defined radio with integration of the personal computer is demonstrated for high frequency AM signal. The combined use of the HPSDR with the personal computer to process I and Q of the signal is more efficient because of the high performance analog digital converter and the large spectrum of reception of the board.

The reception of the inphase(I) and quadrature(Q) signal for high frequency is also demonstrated and shown using the HSDR. The demonstration is included in the results section of this paper. The integration and configuration and final simulation of this system is done in a group with two senior students. Without using the detector it is demonstrated that the SDR box can receive amateur radio signals and able to detect the baseband signal with SDR Box.

The high power software defined radio used with personal computer serves as a visual tool for what kind of output we should be expecting from our low frequency simulation and how we can communicate with the hardware for efficient signal processing. The main part to design for using the HPSDR is that it require an antenna design which can pick a small voltage signal. The design of the antenna for the project is ongoing and a group of two senior students are working on it.

The simulation of the inphase quadrature signals using Matlab has shown that building the Tayloe detector for low frequency communication is possible solution for low frequency underground communication apart from the hardware limitation encountered during the demonstration of the system.

3.2 Simulation of Tayloe Detector using Multisim and LTSpice

The simulations done using Matlab both using a generated signal model and a real signal received from outside has shown that the low frequency implementation is possible. After getting the desired output in the simulation the next step for this work was to implement the hardware of the detector. But the first step of the implementation is to verify the functionalities of the all the components using a spice software. LTSpice and Multisim are used for implementation of the simulation in spice model.

As discussed in section 2.2 the parts of the quadrature detection, the first part of the spice simulation is done for the clock source which is used as local oscillator for our circuit. The clock simulation is done both in Multisim and also LTSpice. The output is two phase shifted clocks having a frequency one fourth of the input source. Different frequencies have been used and tested for the simulation. As an example consider the input source frequency given as an input from the function generator in the spice model. The clock circuit connection on Multisim is shown in figure 26.

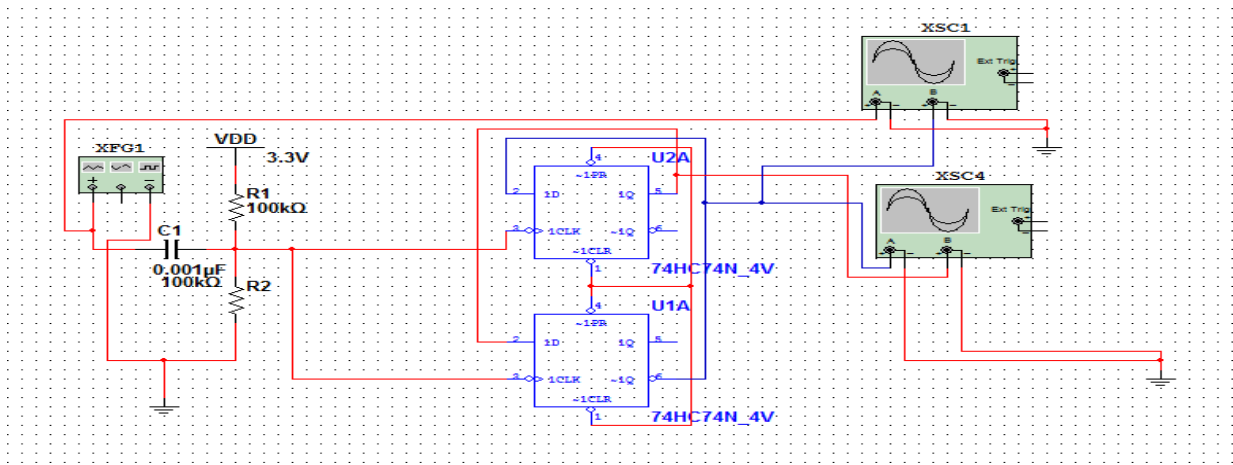


Figure 26 Detector clock drive circuit

The detector clock driver uses a function generator as a clock source and the outputs of the detector are observed with oscilloscope. A comparison of the input and the output clock shows that the output clock is one fourth of the input clock is shown figure 27.

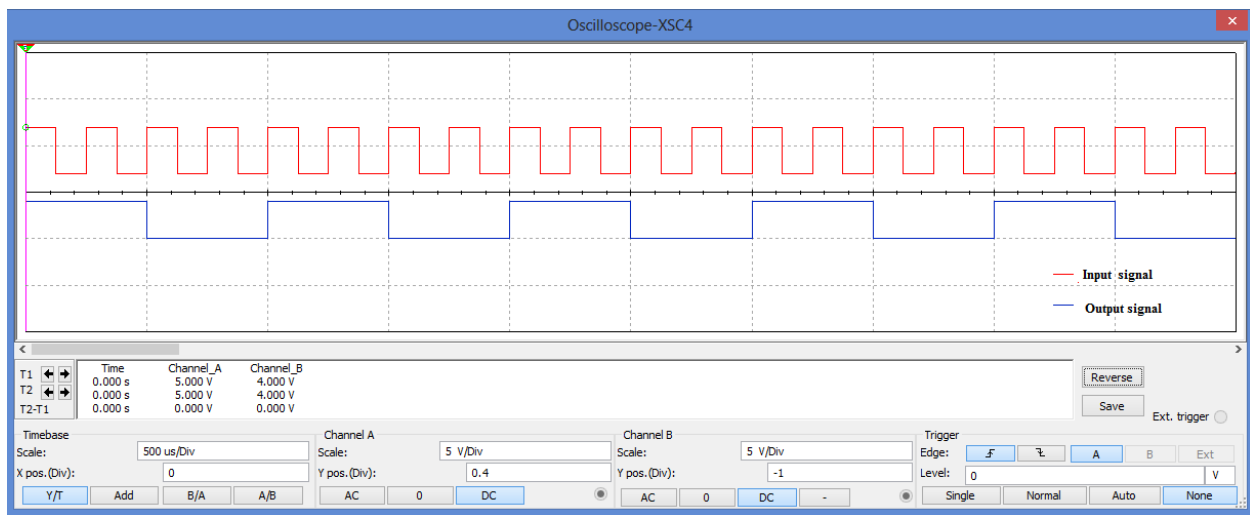


Figure 27 Input Clock and Output clock

The output of the detector driver clock are the phase shifted inphase(I) and quadrature(Q) components of a signal. The 90° phase shifted clock outputs at the output of the detector clock driver look as shown in figure 28.

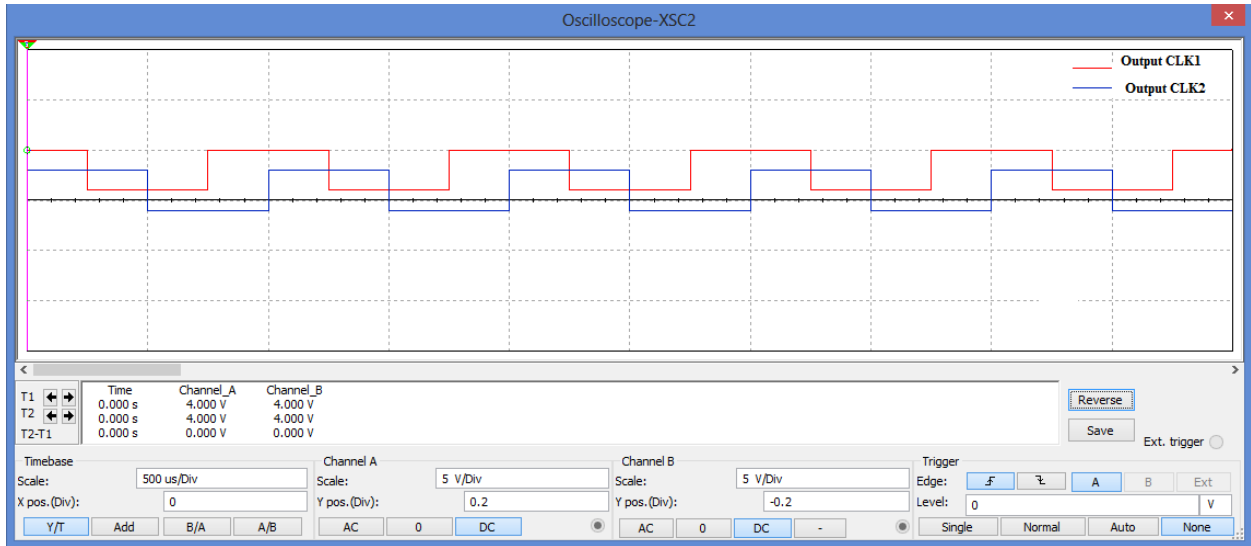


Figure 28 Phase shifted Quadrature clocks

Since the 1:4 FET demux is not included as part of the available components in most of the spice simulation software, it was necessary to design a block and implement the functionality of the detector as a block. For this purpose LTspice software is used for component creation. The free software LTspice was used because integration is simpler compared to other types of spice software.

After the generation of the phase shifted clock is checked by simulation in Multisim the functionality of phase shifted clocks can be represented by square wave voltage sources for simulation. The LTspice simulation which includes all the parts of the detector is shown in fig 29. The main components are the clock driver, the detector FET demux and the low noise op-amps.

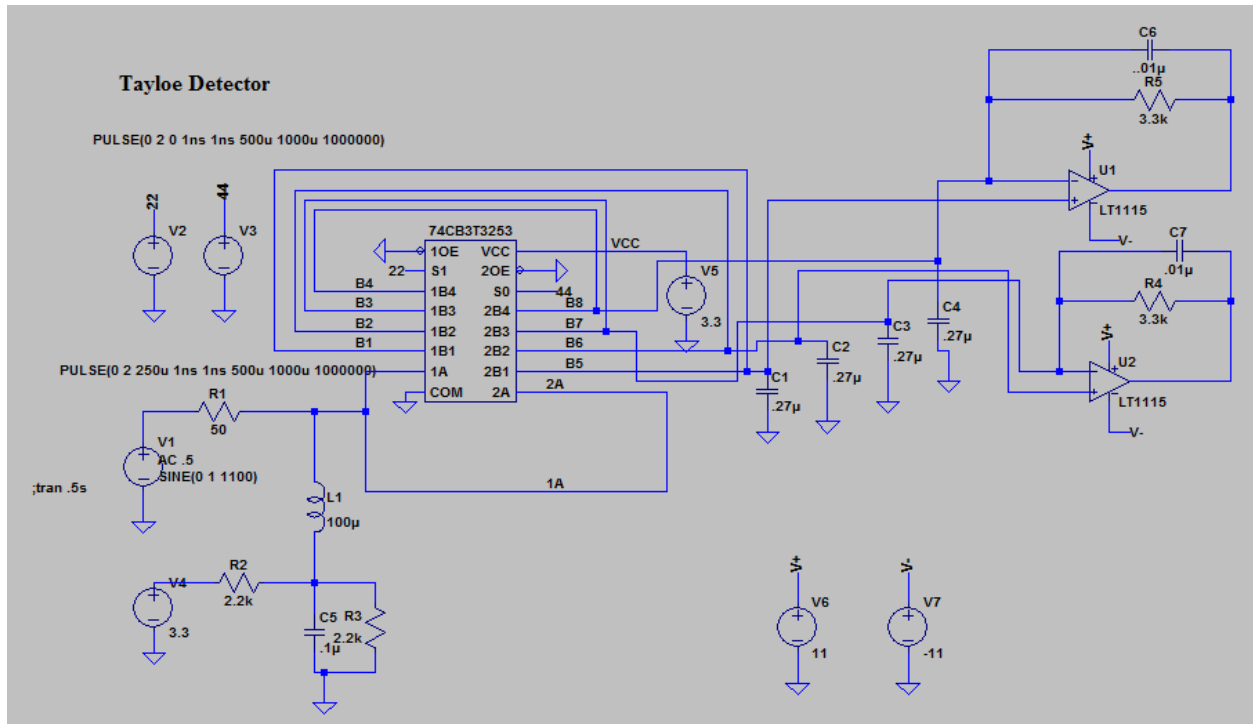


Figure 29 Tayloe Detector simulation connection

In the above figure the 74CB3T3253 block represents the detector IC and the low noise op-amps used are the LT 1115 op-amps. The square wave input sources are V2, and V3 as shown above. For this simulation the input signal level of 500mv is used which is a relatively large input signal level compared to the real RF environment signal. But the simulation is also tested and it works the same for very small level signal as is shown in the results section of this paper. In the above connection the functionality of the Tayloe detector is tested for an input sine wave signal with frequency equal to the baseband signal is achieved and an output of the inphase(I) and quadrature(Q) components of the signal

The simulated input signal, the output I and Q signals of the op-amps can be seen as shown in the figure below. The frequency of the sine wave input signal used in this frequency is 2.104 KHz and the clocks are 2KHz I and Q clocks and accordingly one expects to see as the output, a baseband signal which is the difference between the clock frequencies and the input signals. Detailed simulation results are explained in the simulation result section of this paper section 3.2. Below is the input sine wave signal and the output I and Q signals .

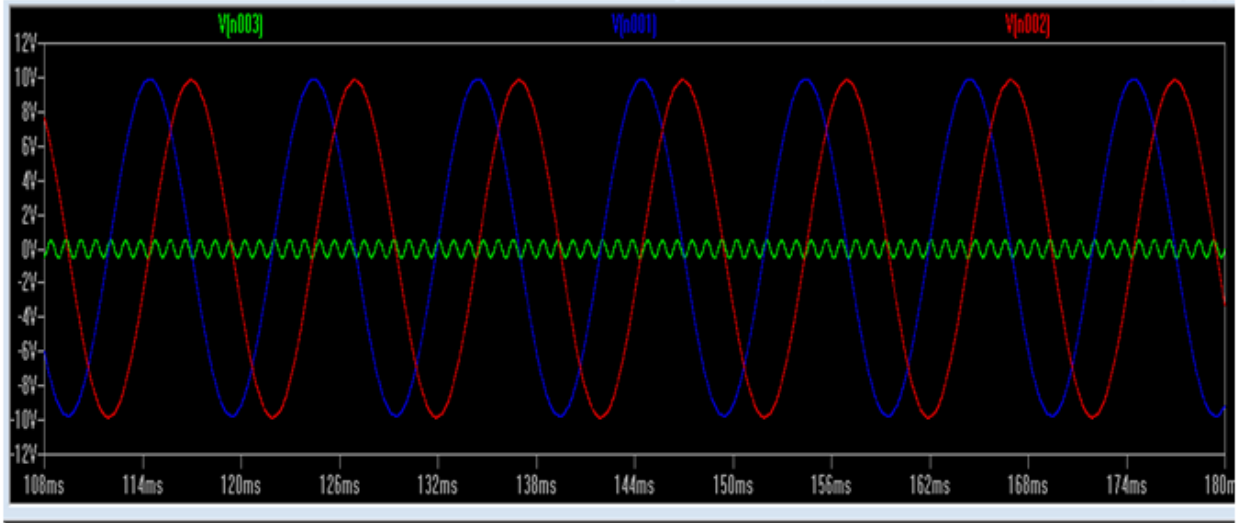


Figure 30 Input signal with output baseband inphase and quadrature components

The LTspice simulation also shows that it is possible to do the detector for a low frequency communication system. The hardware implementation and a comparison with the simulation results is explained in the next section.

Chapter-4

4. Simulation and Hardware Results

4.1 Matlab Simulation Results

This section discusses the simulation results of the detector with Simulink as well as the results achieved from integration of the notch filter with the quadrature detector. The Simulink library components used in the simulation include SimElectronics, SimRF from the DSP system toolbox and the communication systems tool box. The first simulation output is the inphase(I) and quadrature(Q) components outputs from the output of the sample and hold for a sine wave input. At this simulation stage the output of the sample and hold is given to the zero order hold circuit to change the sampled signal to continuous signal. The RF carrier input for the Tayloe detector is simulated as input sine wave signal and the simulation connection looks as follows.

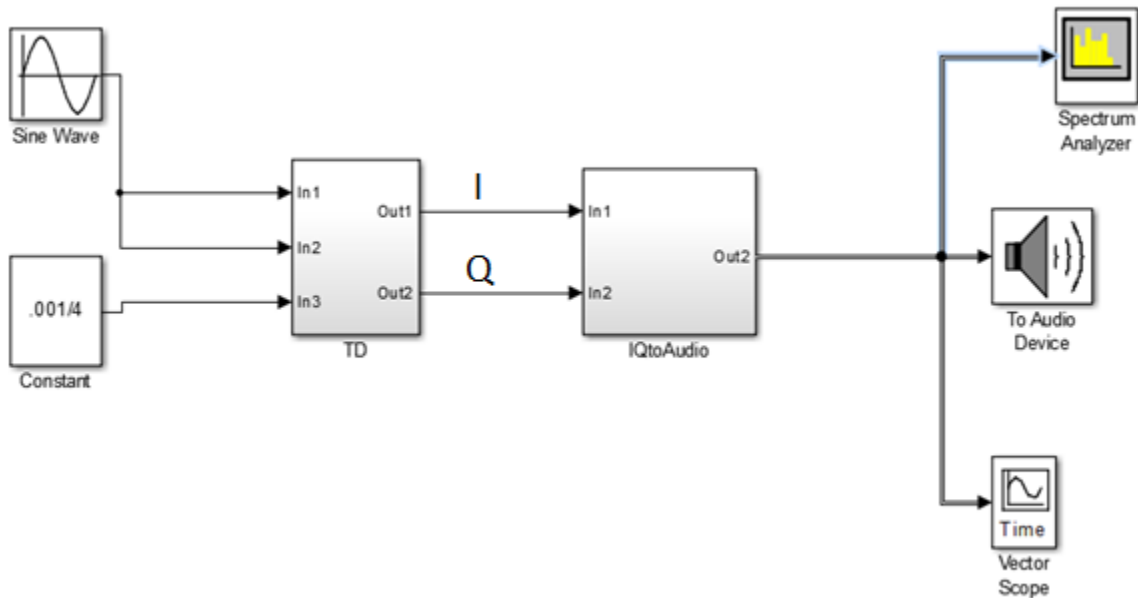


Figure 31 Detector simulation setup

The sine wave input and the delayed sine wave input are given to the sample and hold circuit in the Tayloe detector (TD) block subsystem. The TD block subsystem as shown above consists of the local oscillator for the detector, a sample and hold circuit, and a pulse generator as clock source. The output of the sample and hold is sent to buffer after the zero order hold where a sampled version of the inphase and quadrature components are stored in two columns. The zero

order hold circuit takes the sampled signal and changes the I and Q components to continuous signals to send then to the sound card of the computer. The buffer used after the zero order hold is to store the I and Q component signals for later access and to display using a scope. The concatenate block in the simulation is used to see the combined generated I and Q components together. A low pass filter is used to reduce the high frequency components in the simulation so that the sound card can get a cleaner baseband signal

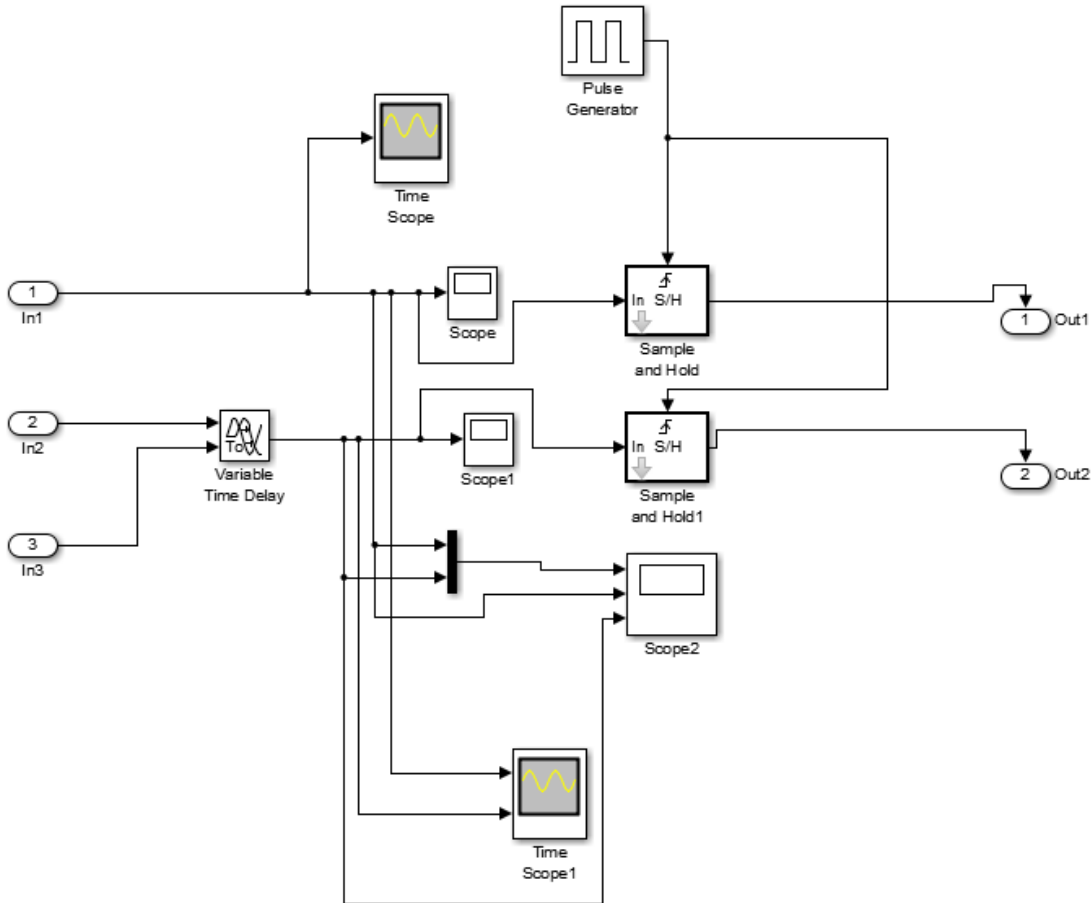


Figure 32 TD functional block representation

The simulation shows that the input RF carrier signal coming to the detector sampled and changed to a baseband signal. In the following simulation result we can see a sine wave of 1.1KHz sampled at a frequency 1KHz giving an output of 100Hz at the end of the detector which is a baseband signal. For simplicity of simulation the input RF signal is a represented as single sine wave. The next simulation result shows the output I and Q baseband outputs sent to

the sound card. It is these inphase(I) and quadrature(Q) signals that are received by the second computer and processed to give the wanted signal.

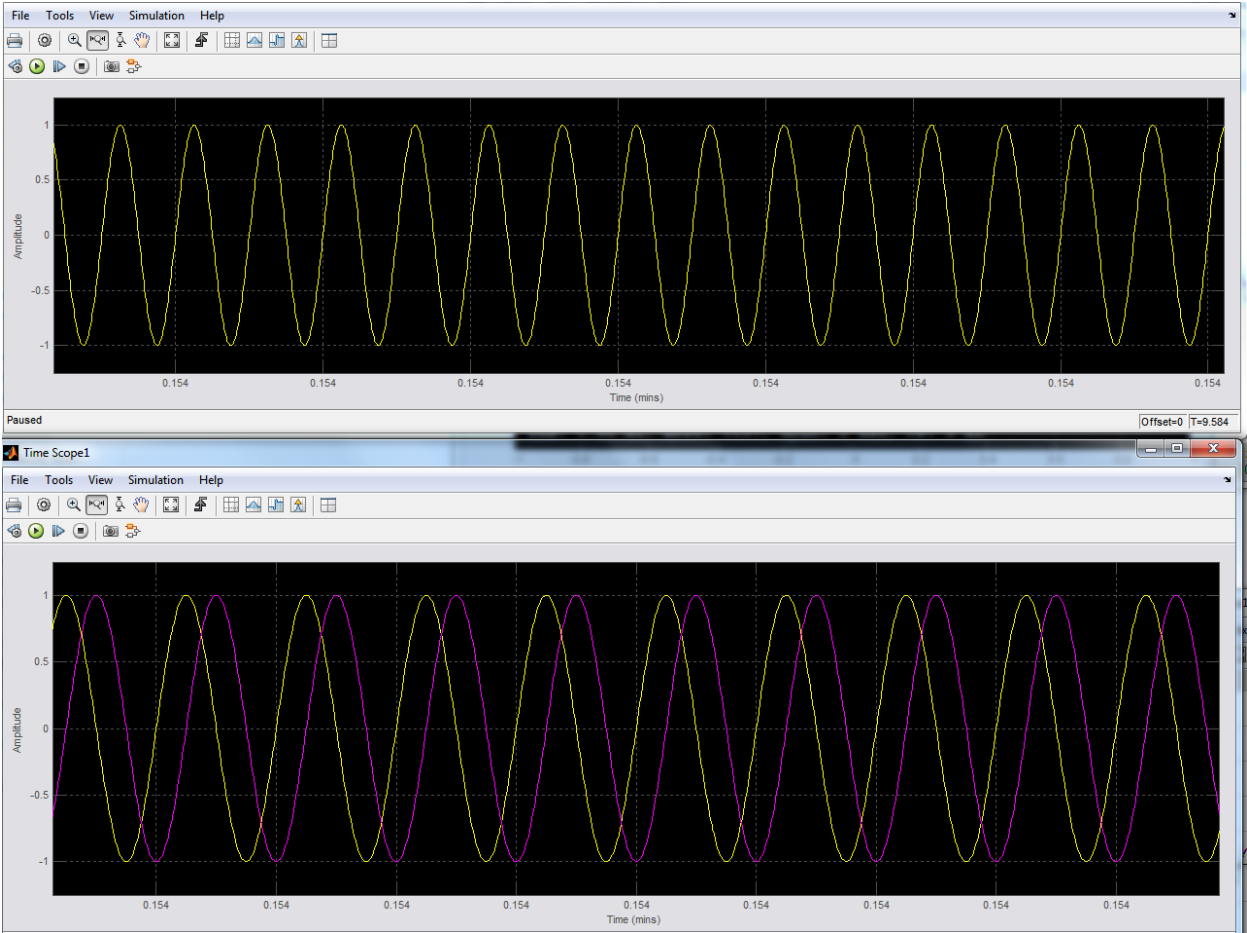


Figure 33 Input RF and baseband I and Q signals

The purpose of generating the inphase and quadrature components is that if one has them, one can demodulate any type of modulation such as AM, FM, PSK and others. After generation of the inphase(I) and quadrature(Q) components if one is interested in single side band processing, one can further extend the built in Tayloe detector for single side band either upper side band or lower side band modulation by adding more processing blocks in Simulink. The inphase and quadrature signals have the same frequency response after passed through the low pass filter. If we further shift the quadrature signal, and add the inphase and quadrature components together, the result will be a signal of double amplitude of I or Q in the case of the wanted signal and zero in the case of the unwanted signal. The generated signals will be added to get the wanted signal. The unwanted signal component is the addition of the inphase and quadrature components in which the second signal is again shifted by the same 90° . In the simulation the same amount of

delay is applied to the signal component to get the delayed version of the same signal. The single side band simulation configuration is as shown below.

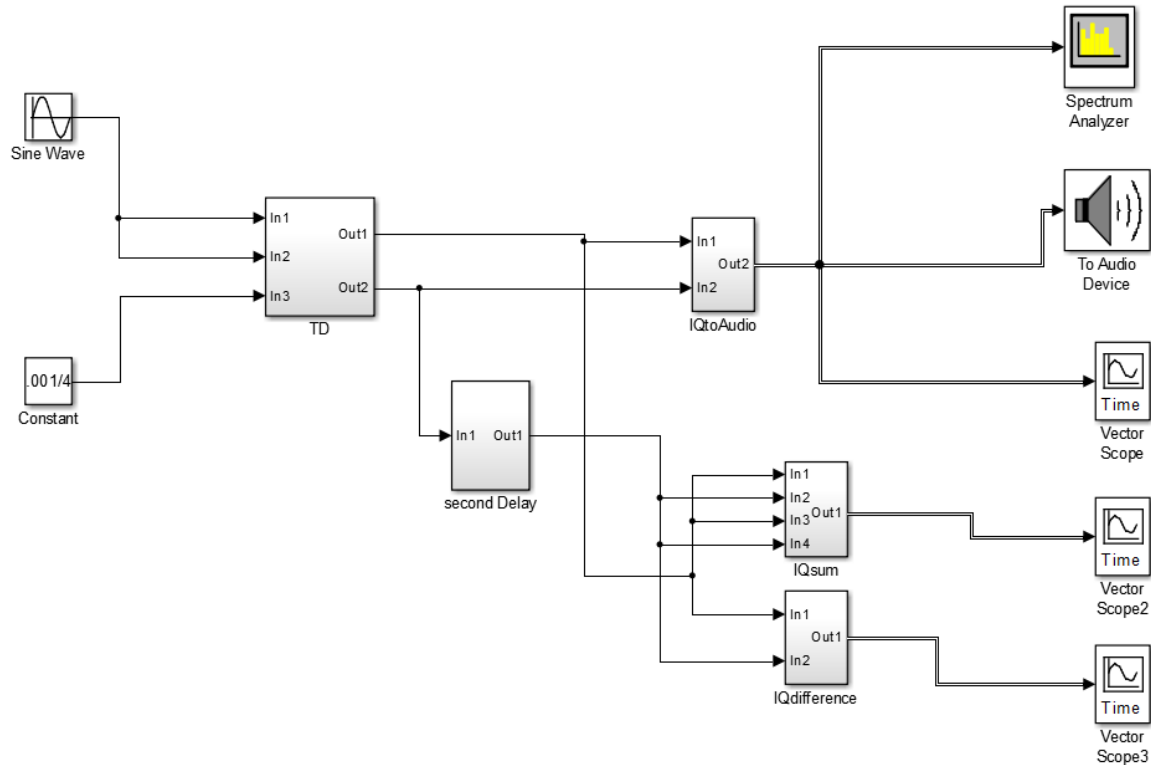


Figure 34 Taylor detector for single side band simulation

The simulation result of the above configuration shows that the 100Hz baseband signals added with the shifted version of its quadrature component. The first result show the same result as amplitude modulated signals where the output is twice in magnitude of each of the signals generated for the wanted signals. And the second simulation result shows that the output for the unwanted signal is zero when inphase signal is subtracted from the shifted version of the quadrature signal. Since time delay block rather than exact 90° phase shift it can be seen that a small amount of signal still exists at the output of the unwanted signal simulation. The first simulation shows the output of the wanted signal and the second simulation shows the difference between the inphase and quadrature components after shifting the second signal for purpose of SSB simulation.

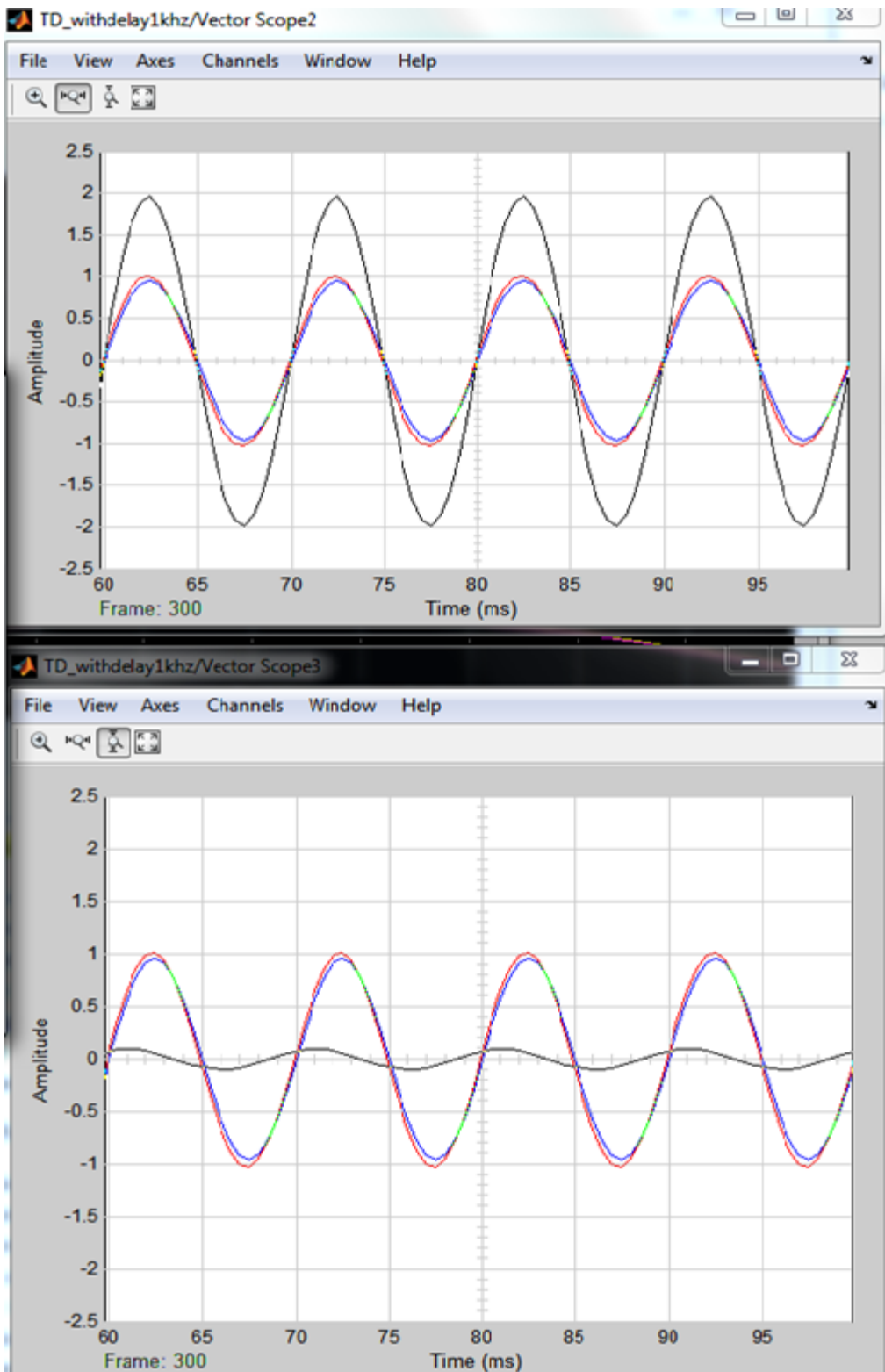


Figure 35 Simulation of Wanted Signal Vs Unwanted Signals for AM

The last part of the simulation for the Tayloe detector is receiving the signal through the microphone inputs of the computer to generate the inphase(I) and quadrature(Q) components to digital. Since the purpose is to use the detector for low frequency communication in underground, one of the challenges is to notch out the 60Hz strong signal during lab testing. The simulation setup for the notch filter integrated with the detector is as shown below and the result of the simulation shows that the 60 Hz notched and the required inphase and quadrature components are generated from the Tayloe detector in baseband

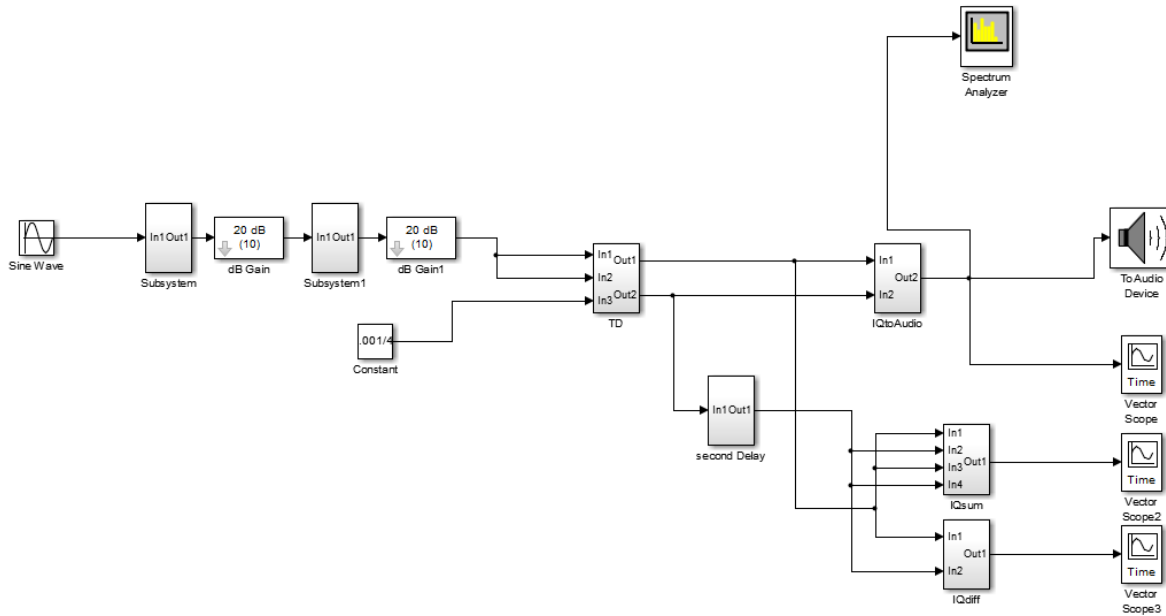


Figure 36 Notch Filter with Tayloe detector

The simulation of the detector in Simulink shows that a low frequency communication can be implemented using the concept of the quadrature detector. The implementation of the detector can be used as an option for generating inphase(I) and quadrature(Q) components of a signal and give a baseband output in conditions when there is hardware limitation in the low frequency quadrature generation.

As part of verification and testing for the operation of the Tayloe detector, simulation of one public rapid transit (PRT) frequency was tested for reception and generation of I and Q. For the purpose of the a test a computer is used as a signal source to generate a tone of 6.1KHz signal. The test result below shows that the detector simulation for generation of I and Q for the PRT frequency under test.

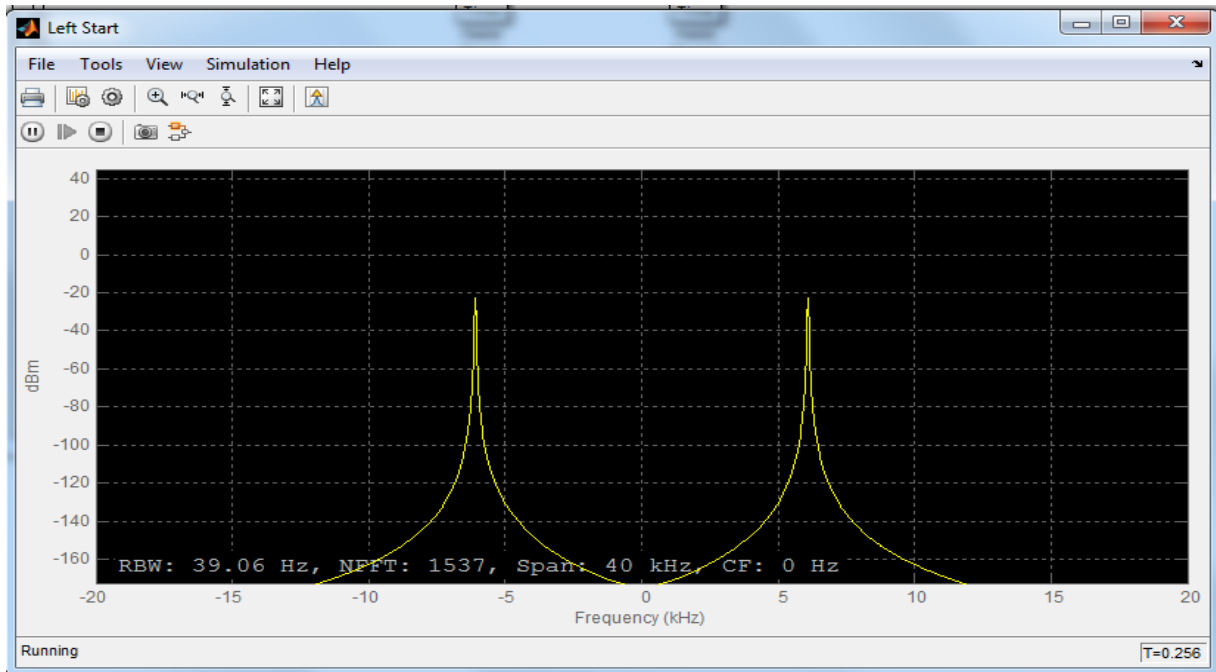


Figure 37 Input spectrum of 6.1kHz signal sent to the detector

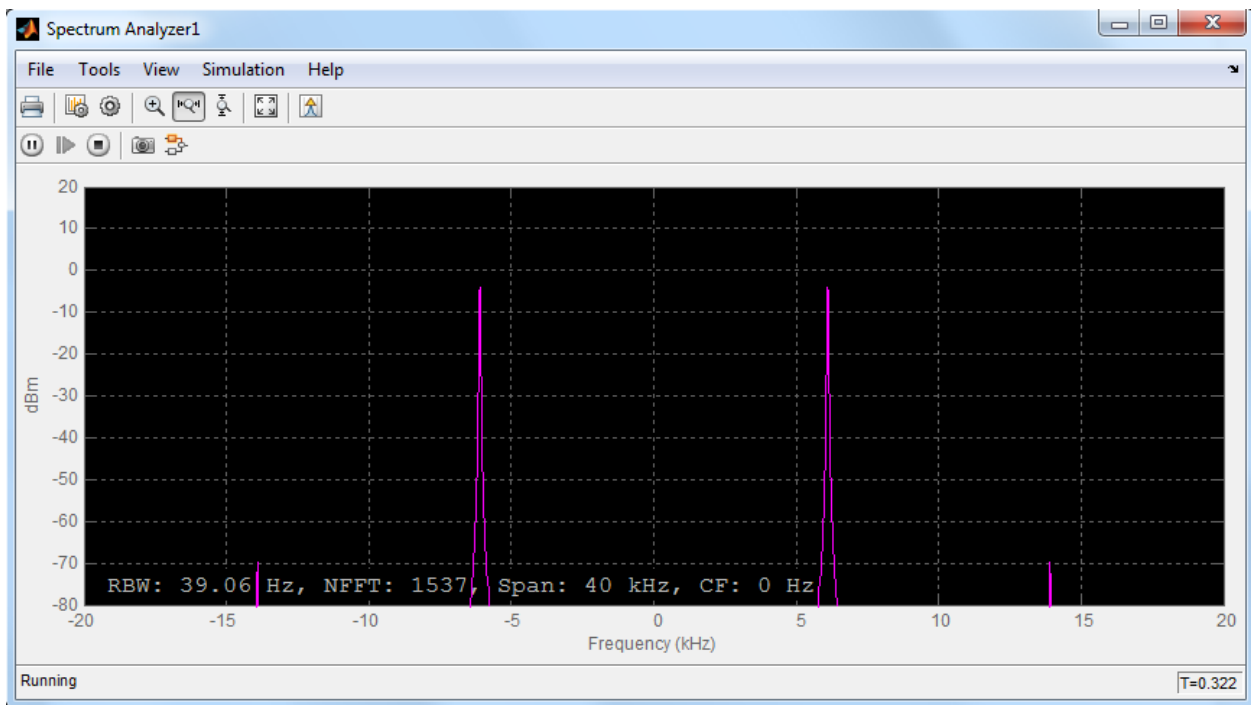


Figure 38 Output Spectrum of the 6.1kHz detected as inphase component

In the next section, the hardware implementation of the detector components and the final detector circuit for low frequency implementation is explained in detail.

4.2 Implementation of Tayloe Detector

The result of the simulation using the Simulink shows the full operation of the inphase(I) and quadrature(Q) generation. The next step for this work is implementation of the detector in hardware. The testing of the hardware for operation and integration with the notch filter for doing the low frequency communication is the main purpose for implementing the detector in hardware.

The first connections and test of the hardware was done on a breadboard. And after the functionality of each part of the detector was tested separately the final implementation of the full circuit was tested as a complete unit. For the purpose of the testing two function generators, oscilloscope, and two power sources were used. The power sources were used as supply voltage for the detector, for clock divider and supply voltage for the op-amps. The first function generator was used as a clock source by generating a square wave input to the detector clock driver and the second function generator was used as antenna input signal. At this stage of the hardware implementation an antenna was not used but rather an input signal from the function generator was used as an RF carrier input to the detector.

4.2.1 Clock Connection and Test

The connection of the clock driver for the detector on hardware to be tested is as shown in the figure 39. An input bias from voltage source and a square wave input from the generator are given to the 74AC74. The expected output of the 74AC74 is two square waves which are shifted by 90 degrees.

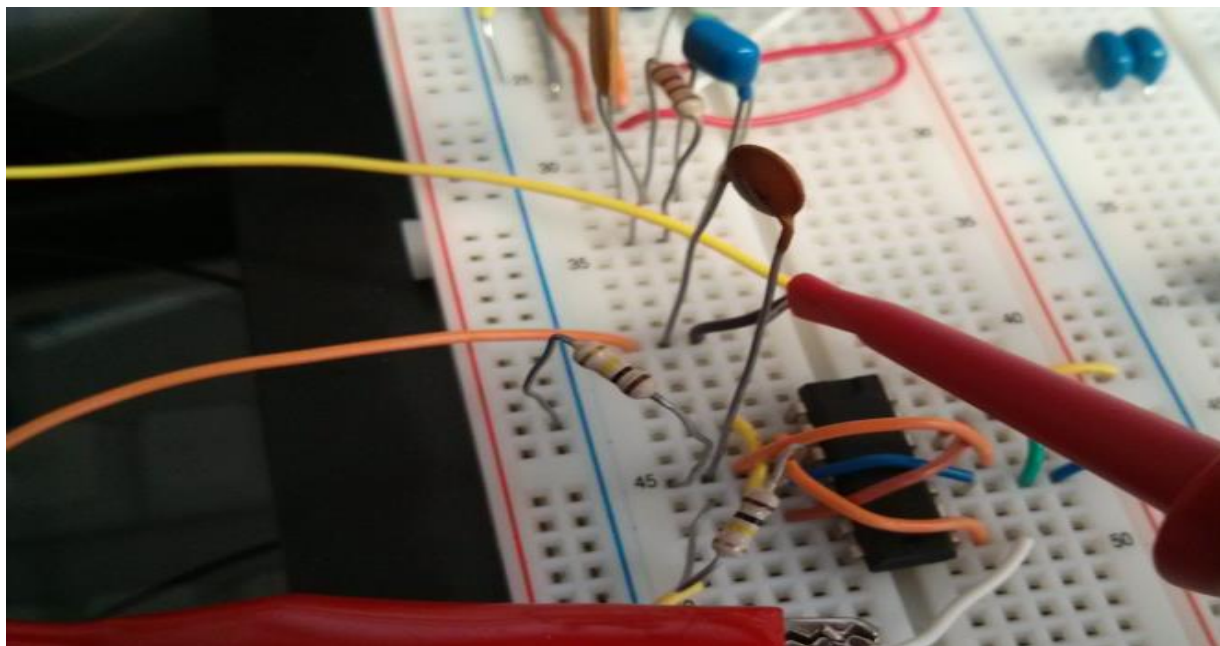


Figure 39 Detector driver clock

The input clock used as local oscillator and one of the outputs from the clock can be seen in the oscilloscope outputs shown below.

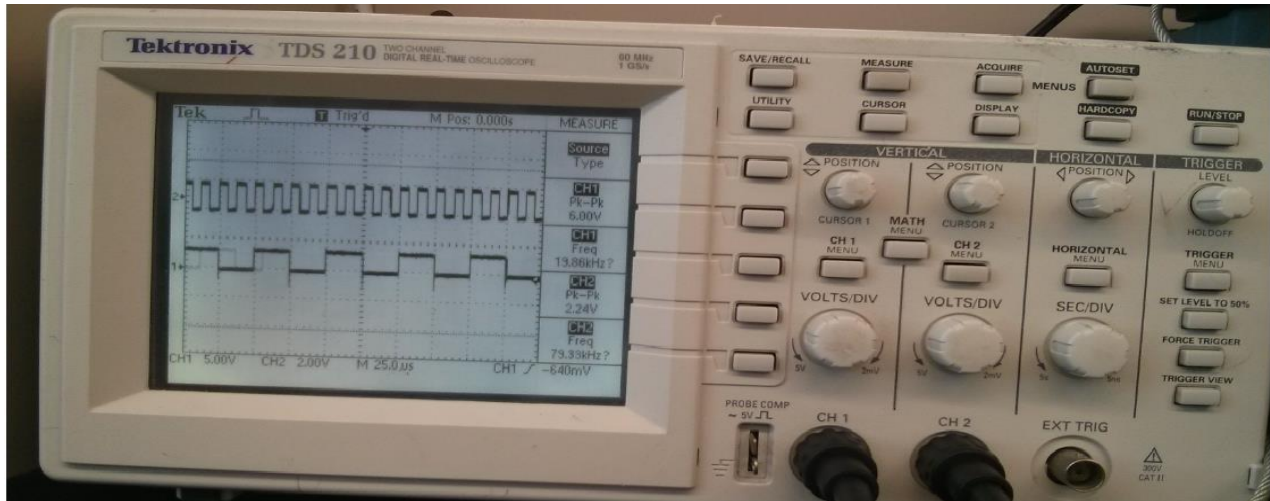


Figure 40 Input local oscillator clock with one of the output clock

The generated and phase shifted clocks which were used as a driver for the detector was taken from pin 8 and pin 5 of the 74AC74. These were the sources of the clock sent to the switch IC. The clock from the pin 8 was connected to Pin 2 of the detector FET switch. The clock from pin 5 of the 74AC74 was connected to pin 14 of the detector FET switch. The shifted clocks at the output of 74AC74 on pin number 8 and pin number 5 are shown in the figure below.

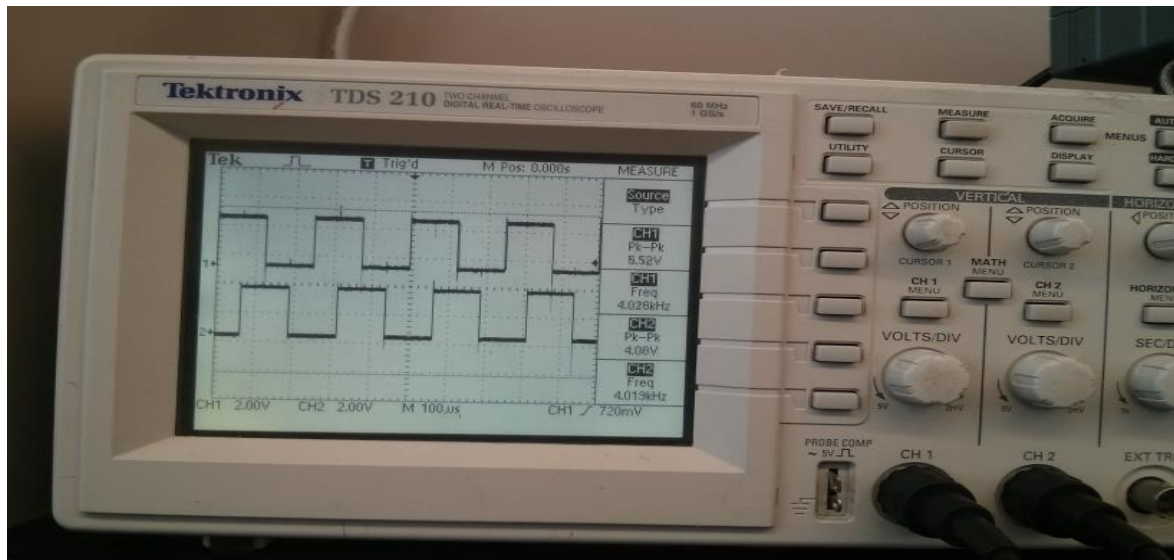


Figure 41 Output clocks from the 74AC74

4.2.2 FET Switch Connection and Test

The switch IC is a dual 1:4 FET demux consisting of two independent demux which can operate separately, but as shown in the component part of the Tayloe detector the detector can be one demux. Instead the corresponding pins of the second demux were paralleled as shown in fig 17

As in the simulator the output selection sequence for the detector is 00,01,11,10 or 00, 10, 11, 01. A test for checking all the outputs of the detector switch can be done by sending these input combinations in pin number 2 and pin number 14 and verifying the input signal is seen at the output. After confirming that all the outputs of the detector are working, the detector switch is combined with the clock source generating the clocks.

When the clock input is given to the detector switch, the output of the detector switch will be identical to the input for one quarter of a cycle and the sampling capacitor will hold this value for the rest of the cycle until the next sampling cycle occurs. The outputs from both capacitors will be sent for differential summing to the op-amps.

The entire connection of the detector on the breadboard is shown in fig 42. The functionality of the connections of the boards is tested and the outputs are checked on the oscilloscope and the inphase and quadrature components have been generated for the input signal from the function generator.

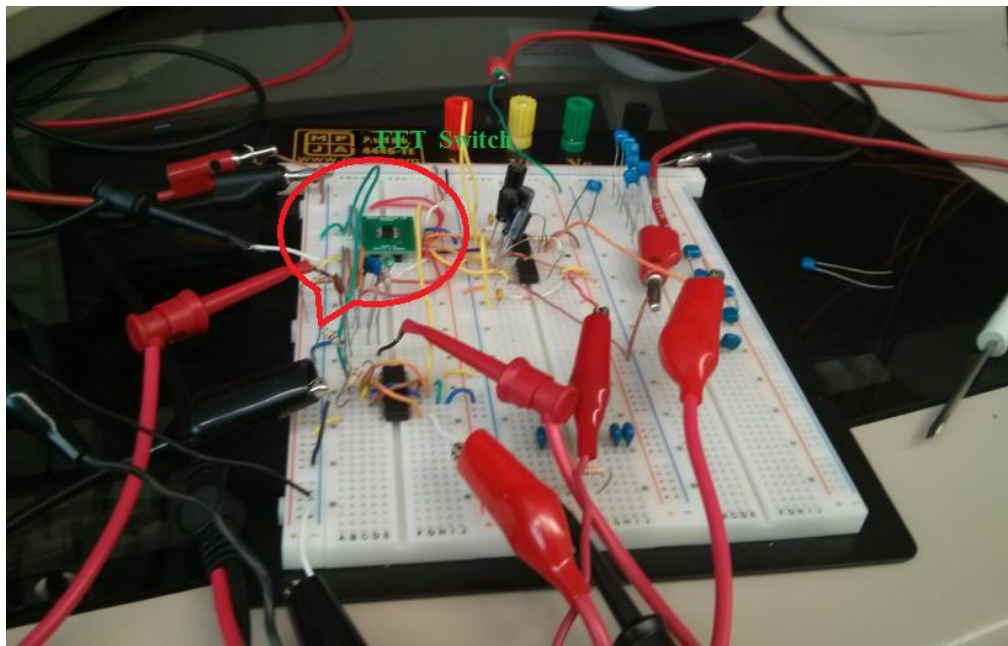


Figure 42 Shifted clock output connection from 74AC74 to the switch

After testing and verifying the functionality of the quadrature detector on the breadboard, the breadboard circuit design was transferred to a printed circuit board. A free software kiCad was used to design the PCB layout for the circuit. The final layout of the PCB layout is shown fig 43.

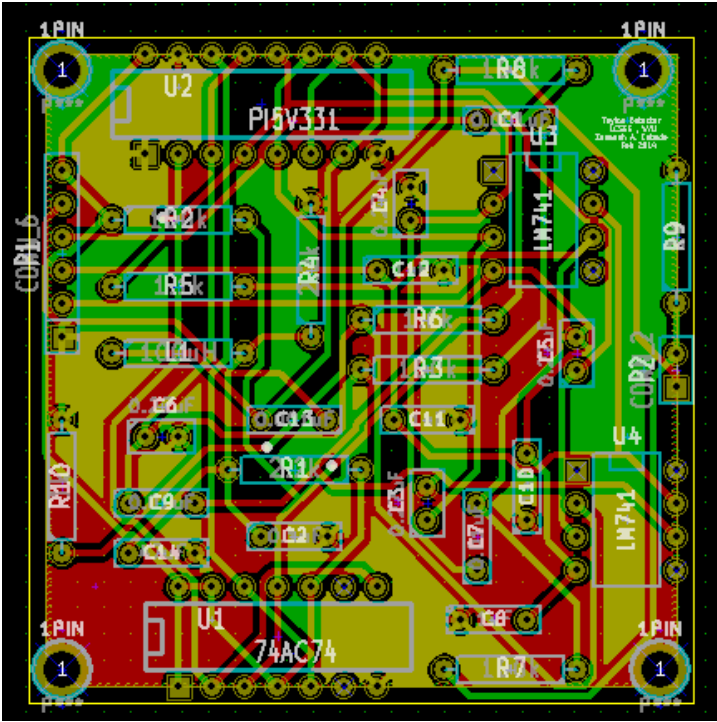


Figure 43 PCB Layout for the detector

The 3D view of the two layer board layout of the detector can be seen in fig 44

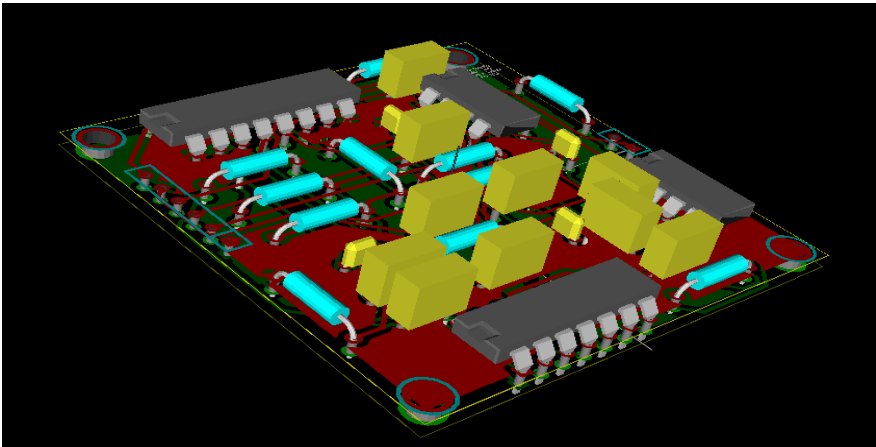


Figure 44 The 3D view of the detector

After the board is fabricated, all the detector components were soldered in the 2 inch by 2 inch board size and the final test was done on the new fabricated board.

c

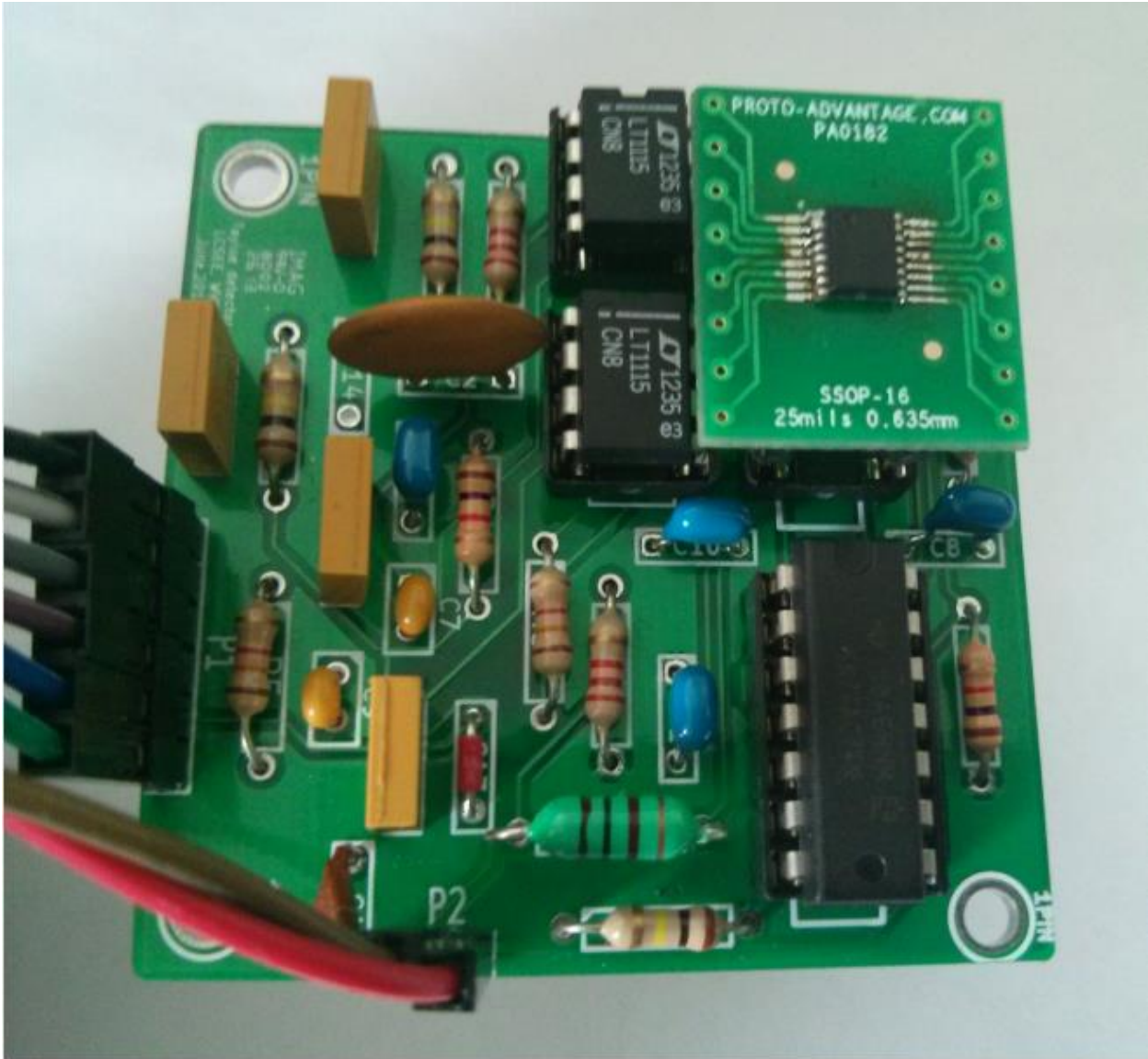


Figure 45 Detector Hardware

The functionality of the PCB mounted detector was then tested for generation of inphase and quadrature baseband components. The following figures show test results of the output of the detector when the sine wave was used as input.

The first detector built was for high frequency in which an input signal of 204.25 kHz was used as an RF carrier. The local oscillator is set to 800 kHz square wave. With this setting the output one expects will be a 4.25 kHz baseband inphase and quadrature components. The following pictures shows the input RF carrier and the outputs inphase and quadrature signals as displayed on the oscilloscope and are 4.25kHz.

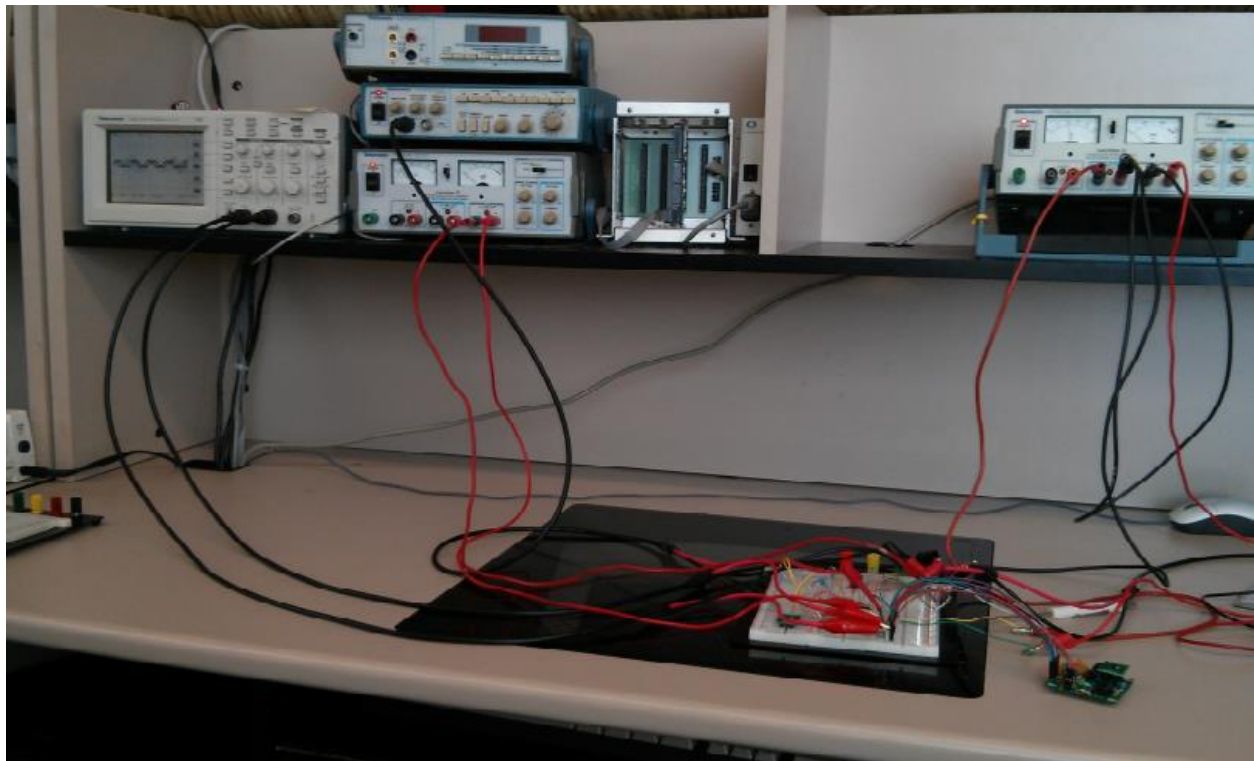


Figure 46 Detector Test connection

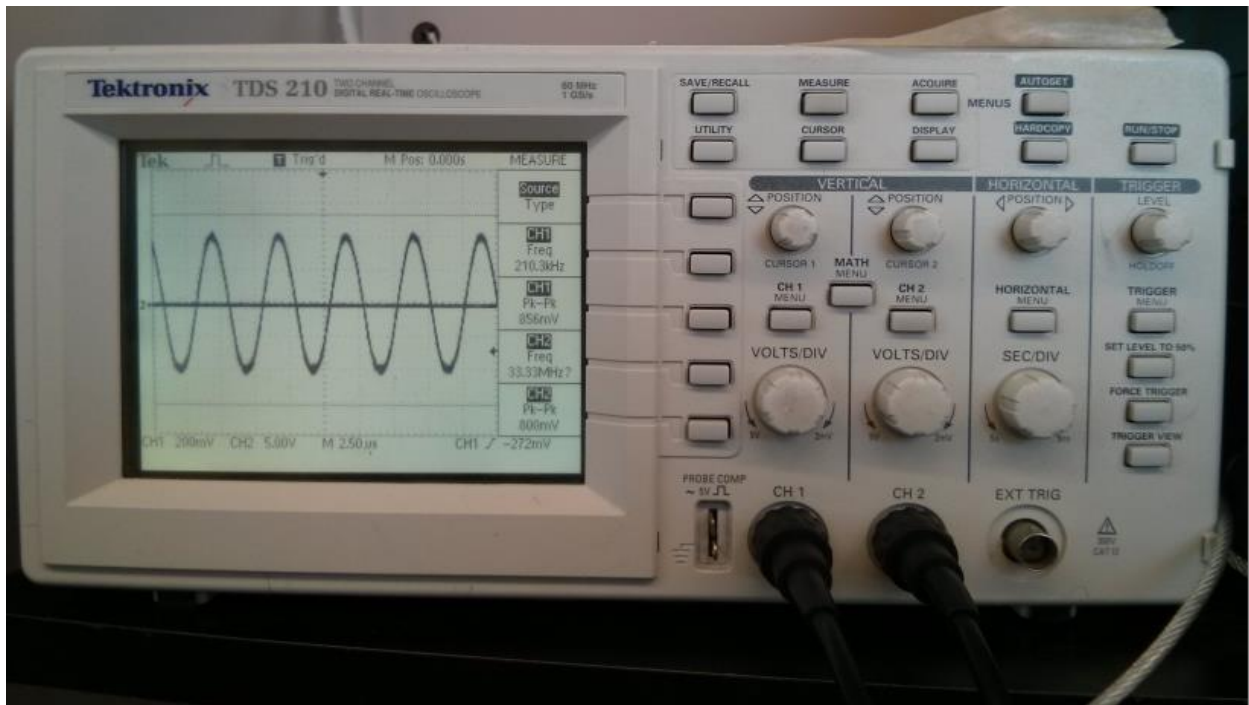


Figure 47 Input for the detector

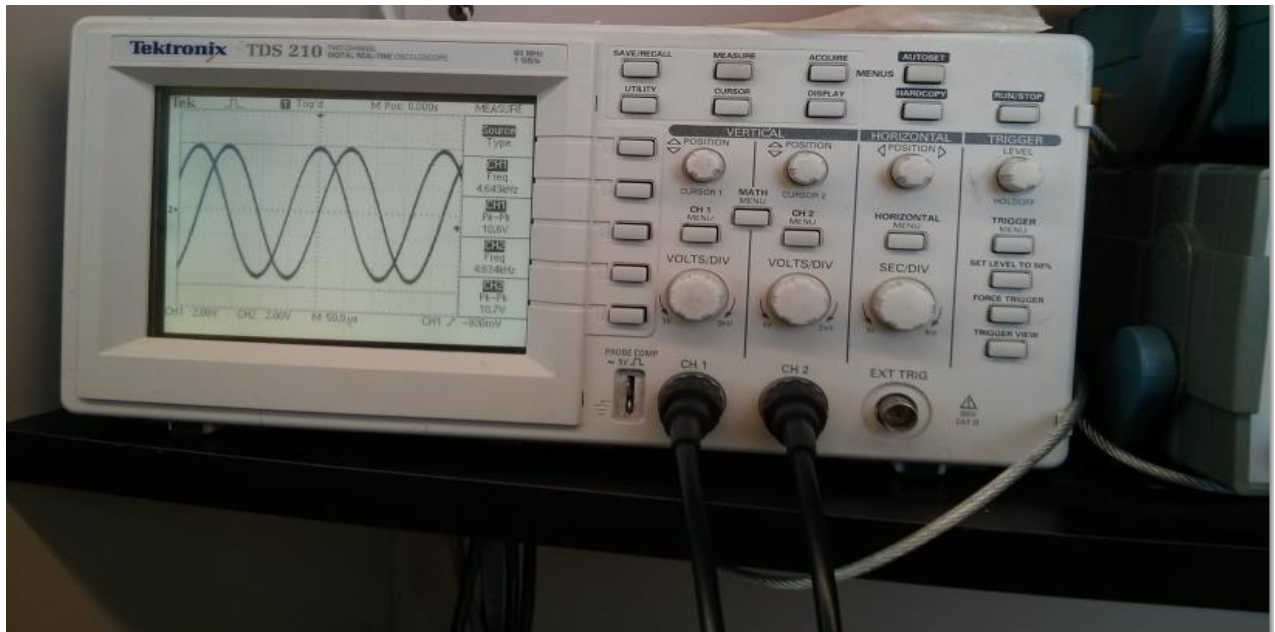


Figure 48 Oscilloscope Output for the detector

The FFT of the output signal for both I and Q can be seen in the PoScope as shown in the figure 49.

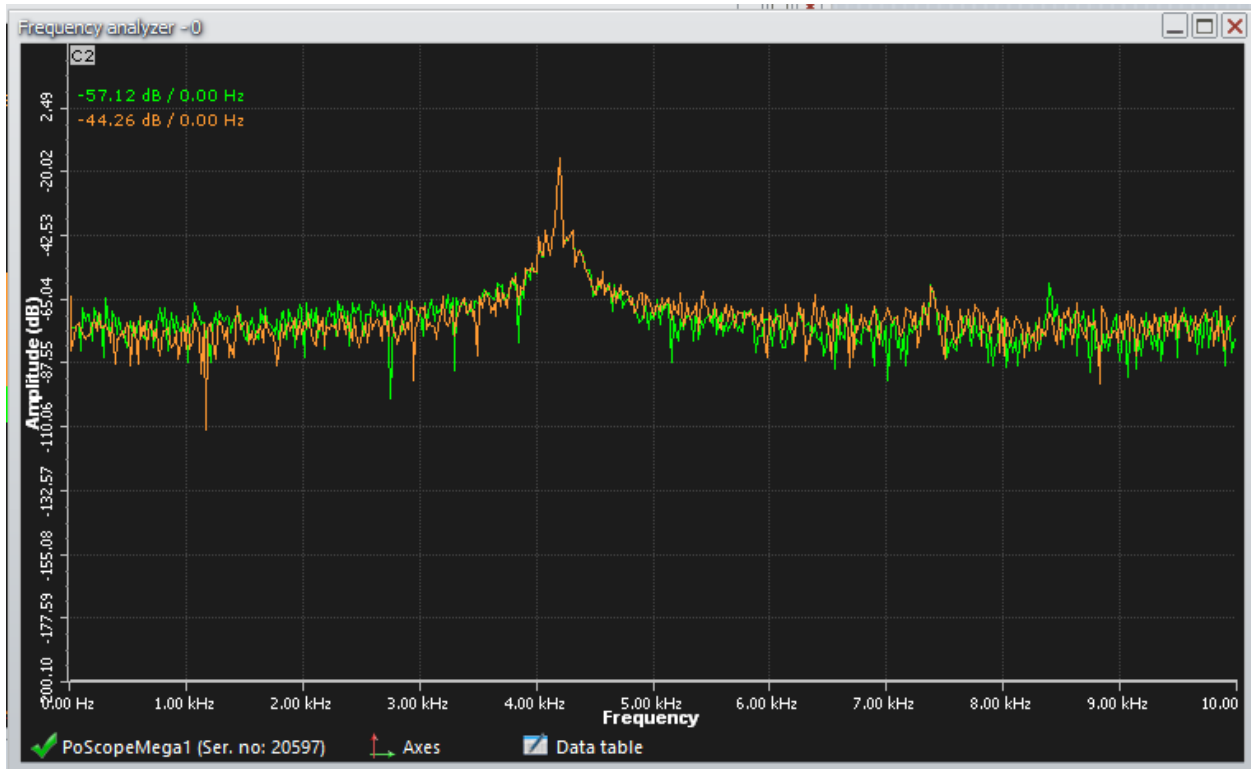


Figure 49 FFT of in phase and quadrature components

The output inphase and quadrature components seen by the Poscope output is as shown below

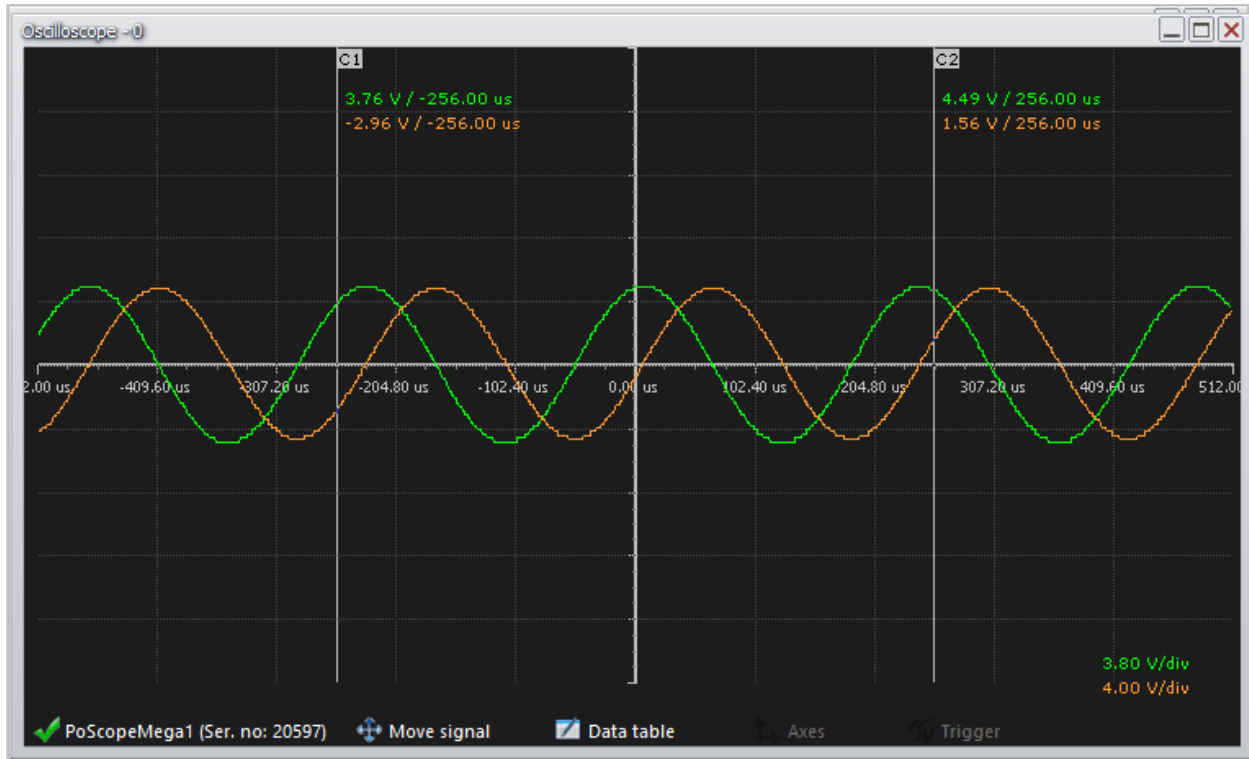


Figure 50 Poscope output of inphase and quadrature components

The second detector was also tested for low frequency range. A test of the detector for frequency of 2.1 KHz input signal was done. The 74AC74 generated two clock sources at frequency of 8 KHz. The laboratory oscilloscope used to see the output of the detector for high frequency and strong signals has become very difficult to use for testing at low frequency due to its precision. For this reason a portable oscilloscope (Poscope) which is connected with personal computer for processing was used to see the outputs of the signal. The Poscope also has a feature of fast Fourier transform(FFT) which enables us to see the frequency content of the strong signal among many other signals and background noise.

The output of the test setup used for demonstrating the low frequency of the detector are shown in the figure below in which the FFT of the signals are shown with the strength of the signal in comparison with the background noises. The input signal strength used as RF carrier is the same as while doing this test. The generated I and Q signals have a frequency content which is the difference of the input signal and the generated clock. Accordingly the expected output for the above signal is a signal with frequency content of 104Hz. The output from the test verifies that two quadrature signals of frequency 104Hz were achieved.



Figure 51 FFT output for low frequency test

The low frequency detector design procedure is the same as that used for high frequencies. The only necessary changes are the values of the sampling capacitors and the feedback resistors for gain of the op-amp. These values are changed because the new operating bandwidth and signal level under test was different from the high frequency. In the laboratory test environment the existence of the other low frequency noise signals can also be seen on the FFT display together with the output of the detector. The results achieved from the hardware implementation have shown that the low frequency receiver can be built and used in small frequency ranges. As one goes to lower and lower frequencies the hardware limitation is seen because of the clock source instability and filter quality factor Q .

Chapter-5

5. Summary and Conclusion

5.1 Summary of Simulation results

The simulation of the Tayloe detector has shown that it is possible to generate low frequency quadrature signals for low frequency through the earth communication. The first simulation of the detector was implemented using Simulink as most of the components required are included as part of Simulink library. All parts of the detector are simulated in a single model using one computer except reception of the input signal which is generated by another computer also running Simulink. Most of the parts of the Simulink used for the simulation require appropriate configuration for getting the desired outputs of the detectors. Real time signal reception by the sound card require to amplify the signal strength as the signal level picked by the sound card is larger than the RF signal picked by the antenna. This is the main reason to build a separate preamp to amplify the RF signal.

In the current configuration the simulation parameters work for a single frequency set up. The parameter must be changed accordingly whenever a different frequency is required to be simulated. This is because there is no exact phase shift generating block in Simulink which can take a continuous real signal. The variable time delay block is used to do the phase shifting during the simulation. The exact delay calculation is done based on the input signal frequency chosen for the test. As shown in the result section of previous chapter, low frequency test is done by taking a tone for I and Q generation. A separate computer is used to generate the tone as an antenna input and the full detection and simulation is done using the built in quadrature detector in Simulink.

In addition to the simulation done in Simulink, an LTspice simulation is also used for simulating the output of the detector to be used as reference for hardware implementation. The inphase and quadrature components are generated and based on the LTspice the simulation results the low frequency detector is implemented in hardware. Since LTSpice doesn't have the FET switch as part of the component the switch is designed according to the functionality the switch.

5.2 Summary of Hardware results

The hardware implementation of the detector was done for two different frequencies. The first implementation is done for high frequency and the second implementation is done for low frequency. The low frequency communication system bandwidth for test around 100Hz while the local oscillator clock generates 8 KHz. The difference frequency between the input and quarter of the local oscillator clock is 104Hz signal as it is seen on the Poscope. The test result of the detector shows that the conversion loss achieved with this hardware implementation is higher than the theoretical value of the detector.

The high frequency hardware test result analysis is shown below

Conversion loss

Given Input voltage 1Vpk-pk, and the output data is tested for the bandwidth with sweep frequency signals and the output voltage is 10.6Vpk-pk.

From the test , for $V_{input}=1V_{pk-pk}$, measured output is , $V_{out} = 10.6V_{pk-pk}$

$$G = \frac{Rf}{4 * Rant} \Rightarrow G = \frac{3300}{4 * 50} = 16.5, \text{ which is equivalent to } 24\text{dB}$$

The differential input yields an additional 6dB gain of the total 30dB [20].

$$\text{Detector loss} = \frac{V_{out}}{V_{input} * \text{Gain}} = \frac{10.6}{1 * 31.6} = 0.335$$

$$\text{Conversion loss} = 20 \log 0.335 = 10\text{dB}$$

The measurements from the hardware are used to plot the output of the detector. The detector output frequency is shown in the figure 52.

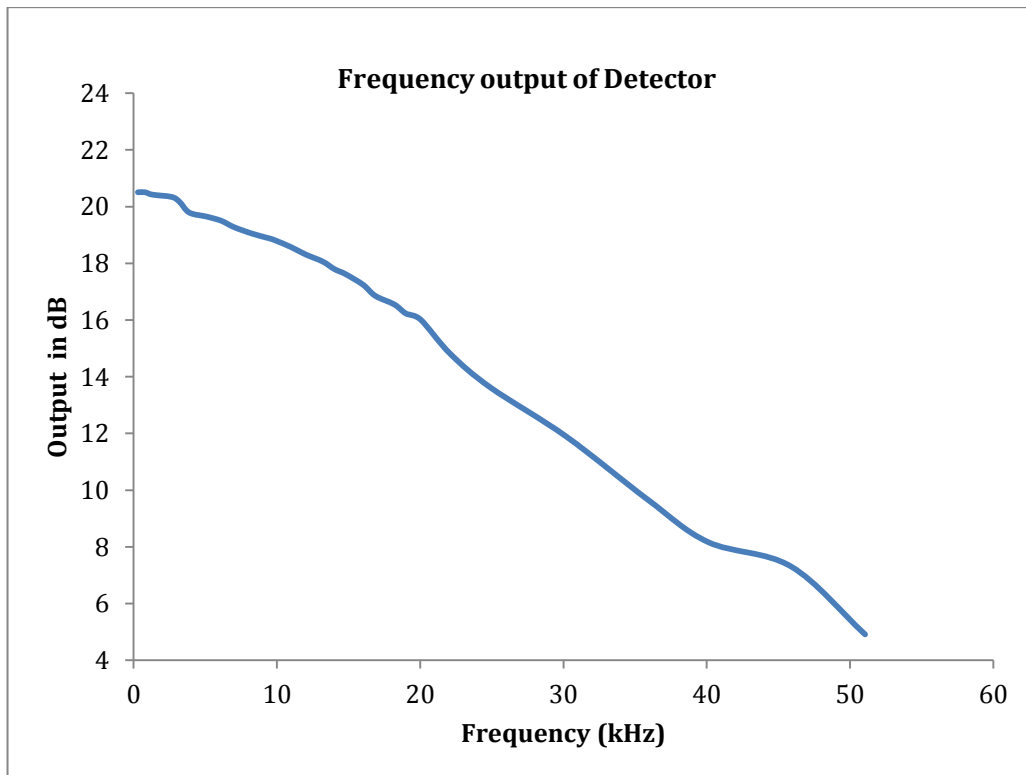


Figure 52 Frequency Output of detector

As it can be seen, the hardware has about 10dB of conversion loss. The input to the detector is also tested to input level as low as 250mV. Since the function generator is used as an RF source, it was not possible to generate stable lower signal levels to do more tests. The important comparisons are shown in the table 2 below.

Table 2 Detector test comparison with Hardware

Taylor Detector	Quality factor(Q)	Conversion loss	Frequency	Bandwidth
Theory	40	0.9dB	200kHz	5KHz
Simulation	25	4dB	200KHz	8KHz
Hardware	14.3	10dB	200KHz	14KHz

For the low frequency hardware test the output of the detector couldn't be seen using the oscilloscope. For this reason a Poscope is used to see the FFT content of the signal. The low frequency hardware has shown that a signal as low as 2 kHz could be received with bandwidth of 200Hz. The low frequency communication hardware implementation was more challenging than that the high frequency implementation because: The roll off frequency of the RC filter is determined by the value of the resistor and the capacitor. The value of the system resistor used for both simulation and hardware implementation is 50Ω. The only component required to design is the value of the capacitor. The capacitor value required for low frequency is large according to the calculation. The need to increase the value of the capacitor for the design reduces the bandwidth of the detector. Moreover since the receiver bandwidth is low, the quality factor will drop significantly which makes the selectivity of the receiver drop. The noise level for low frequency signals is also strong during the test as compared to the high frequency test. It can be easily seen from the noise that as the bandwidth decreases the noise increase [11]. In order to reduce the noise introduced from different sources in the test environment, a low noise op-amp, LT1115, is used. But the output of LT1115 output was not stable for high frequency test so the implementation for the high frequency hardware uses LM741 op-amp. But at low frequency the LM 741 is not as efficient as LT1115 to reduce the noise during the low frequency test.

The most challenging part of the implementing the detector in hardware was getting a stable clock source for low frequency. A function generator is used as local oscillator for a clock source and the Johnson counter was used as a clock driver for the hardware implementation. At high frequency clock generation and the output phase shifted clocks used by the detector work well but for the low frequency clock generation the clock divider could not generate a clock below 2 kHz. Due to lack of generating a stable clock source it was not possible to perform a test for frequencies below 2.1 KHz.

5.3 Conclusion

This thesis describes the concept of using the quadrature detection method for generating the inphase (I) and quadrature (Q) signals for low frequency signals. Furthermore, the thesis discusses simulation and implementation of Tayloe detector. In addition, the results used from the simulation are taken as a model for the hardware implementation. It also discusses the hardware implementation of the detector with tests done on the detector for low frequencies. In the hardware implementation the different performance measures of the detector are measured. And finally the summary of the test results and evaluation of the tests is discussed. The thesis compared the performance of Tayloe detector (also known as quadrature sampling detector (QSD)) used for generating inphase (I) and quadrature (Q) at high frequencies with the hardware implementation of the detector at low frequencies. The results from this work showed that the quadrature sampling detector can be used at such low frequencies.

Chapter-6

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