RESEARCH ARTICLE

A Detailed Study on LDPC Encoding Techniques

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Abstract: This survey deals with LDPC encoding techniques. Different types of error detection and correction codes have been studied. BHC codes, Turbo code, LDPC Codes, Hamming codes are some of the vast classes of codes. Low Decoding complexity and efficient throughput are the achieved by using LDPC codes. Robert G.Gallager introduced this code so LDPC codes are Gallager code. After then Mackay and Neal in 1995 rediscovered LDPC codes because of its bit error performance. It consist of sparse of ones ie., low density of one's because of this property decoding is simple. The major setback in LDPC codes are Encoding Complexity. WLAN (IEEE 802.11n) and MIMO OFDM are some of the applications of code. This code is a class of forward error correction (FEC) technique that exhibits capacity of impending near Shannon's limit. LDPC codes are well identified for their capacity-approaching performance The LDPC codes have been selected as forward error correction in application including digital video broadcasting (DVBS2), 10 Gigabit Ethernet (10GBASE-T) broadband wireless access (Wi-Max), wireless local area network, deep-space communications.

Keywords: LDPC; ALT; FPGA; BER

1. Introduction

Low Density Parity Check (LDPC) codes are a linear error correcting code, a method of transmitting a message over a noisy transmission channel. LDPC codes wereintroduced by Robert G Gallager in his PHD thesis. LDPC encoding is more complex compare to decoding process. LDPC codes have key attention in research community and offered a reliable data transmission. These codes have an outstanding error correcting capability. The name comes from the uniqueness of their parity check matrix which have only a few number of 1's as compared to the number of 0's.There are many algorithms and methods proposed to reduce the number of 1's. Some of the Encoding techniques are Matrix method ie., Straight forward method, Lower triangular Method and Modified Lower triangular method. LDPC codes are characterized by better flexibility; lower decoding complexity as compared with turbo codes; parallel capability which facilitates the hardware implementation; high throughput which promises high-speed decoding. There are two different methods to symbolize LDPC codes. The LDPC codes are represented via matrix and the second method is a graphical representation.

The two most significant advantages of LDPC codes are lack of low-weight code words and iterative decoding of lower complexity. LDPC codes can be straightforwardly constructed so that they do not have such low-weight code words, and they can therefore achieve small bit error rates. Also LDPC codes use a simple parity -check trellis Graph. The graphical way of representingLDPC codes werefundamentally studied and proposed by Tanner. Types of LDPC

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codes are regular and irregular. It was classified based on according to weight on parity-check matrix, H. Regular LDPC codes have identical row weight and same column weight on parity-check matrix, H, and Irregular LDPC codes consist of different row weight and column weight on parity check matrix, H. Binary and non-binary are other classification of LDPC Code. Classifications are according to elements on parity-check matrix, H. Binary LDPC codes are constructed by elements consisting of two elements (0 and 1), and non-binary LDPC codes are constructed from the finite with q elements (denoted $GF(q)$), where $q = 2p$ for some integer p.

2. Literature Review

In a paper presented by Irina E. Bocharova, Boris D. Kudryashov and Rolf Johannesson, in 2016 approach to search for and optimize codes by their sparse parity-check matrices is presented. It was achieved by replacing the nonzero elements of a binary parity-check matrix either by circulants or by companion matrices of elements from a finite field GF(2m), where we obtain quasi-cyclic (QC) LDPC block codes and binary images of non-binary LDPC block codes, respectively. The optimized convolutional LDPC block codes are still superior to their convolutional counter parts if both decoding complexity and coding delay are taken into consideration. They presented a code search technique which appears to be capable for finding good LDPC codes for different applications.The optimization is split into two steps: optimization of the base matrix and optimization of the labeling. They also demonstrate that the important practical restrictions like delay compatibility and low encoding complexity can be easily taken into account [1].

A paper by Yuval Genga, Olayinka Ogundile, Olutayo Oyerinde and Jaco Versfeld presents the construction of asystematic quasi-cyclic (QC) LDPC code. This systematic structureis constructed by a row reduction technique different from theconventional Gaussian elimination method. The advantage of row reduction technique was being easier to implement whencompared to Gaussian row reduction method. The proposed row reduction method maintains the quasi cyclic structure and the sparsity of the QC-LDPC parity check matrix while providing a low complexity approach to the construction of the generator matrix. The proposed construction exhibits an efficient BER performance for high rate codes, while being a less complex encoder. [2]

Yi Hua Chen, Jue Hsuan Hsiao, Zong Yi Siao presented a design of LDPC encoder using approximate lowertriangular code check matrix in IEEE P802.11. LabVIEW programming language was used for writing the matrix. By means of a unified architecture, yielded three sub-block sizes (27, 54, and 81 bits) and four coderates (1/2, 2/3, 3/4, 5/6). Redundancy bits were calculated to generate 12 different codewords as set by the 802.11nwireless standard. A mask matrix design was adopted to find the difference between "0" and spaces in the code check matrix. Finally the accuracy of the codes was obtained by calculating product of code check matrix using transposed code words. Approximate lower triangular encoder was designed based on 12 LDPC approximate lower triangular code check matrices, combining three Z values and four code rates which proved that then coded code words generated by these 12 code check matrices were accurate.[3]

In a paper presented by Dongying Chen, Pingping Chen and Yi Fang utilize encoding operation by a specific structure of LDPC parity matrix to parallelize row and column. An efficient method was also proposed to control memories, which can be reutilized for the LDPC code with different code rates to improve the efficient utilization of hardware resources. The proposed Low Density Parity Check encoder and decoder are implemented on Xilinx. According to simulation results of Model-Sim and MATLAB, they also verify that the proposed method has the advantages of reduced resource consumption, reduction in number of registers, low power and high accuracy. The proposed encoder can attain throughput up to 400 Mbps. they show that the decoding Bit Error Rate can be as low as 10^{-5} at SNR less than 2.5 dB. [4]

Nelson Alves Ferreira Neto, Joaquim Ranyere S. de Oliveira, Wagner Luiz A. de Oliveira and Joao Carlos N. Bittencourt presented two architectures for the Low Density Parity Check (LDPC) encoder, the first one based on a fully serial approach and the second one in a mixed way, as well as their corresponding realizations in ASIC. The

proposed designs are able to operate in 84 combinations of code rate and word size, according to the IEEE 802.22 Wireless Regional Area Network (WRAN) standard, aiming low power and efficient utilization of area. Although the proposed architectures are primarily designed for the mentioned standard, they can be easily modified to other wireless broadband standards. The proposed architectures were proven effective in meeting the requirements of data rate demanded by the 802.22 standard. It was possible to create LDPC encoders compatible with 84 different configurations, consuming smaller area and power inherent in the type of application. [5]

In a paper presented by Jayashree C. Nidagundi and Dr.Siddarama R. Patiltheir proposed work deals with design and implementation of flexible LDPC encoder using general and RU methods in ASIC FPGA. The flexible encoder designed with propagation delay of 5.208ns with 2/5, 3/5 rates of code. Flexible design can be capable of encoding for any rate and length of the parity check matrix. They analyzed the number of SliceLUTS, Number used as logic, Number of fully used LUT_FF, Number of Bonded IOB in ASIC FPGA. The propagation delay (propagation delay of 1.256ns) of encoder with RU method is minimum compared to general method. RU method encoding technique reduced complexity and improved speed. [6]

Yi Hua Chen, Jue Hsuan Hsiao, Jheng Shyuan He, proposed a detailed introduction to the encoding mechanism of the approximate lower triangular method of LDPC Encoding, and completed the implementation and verification of FPGA hardware. Compared with general linear block code encoding techniques, LDPC encoding with lower triangular check matrix and approximate lower triangular check matrix carry out encoding directly by parity check matrix H. LabVIEW FPGA was used to build programming codes in hardware. They completed the approximate lower triangular LDPC encoding circuit and used the orthogonal characteristic of $HX^{T} = 0$ to verify the accuracy of encoder. [7]

3. Survey of LDPC Code in Tabular form

S.No	Title	Publication	Author Name	Pros	Cons
1	Comparison of FPGA implementation of LDPC encoder algorithms	IEEE 2016	Steffy Johnson, Nidhi Gaur	(1) This paper present the straightforward method and the lower triangularapproach, which are the twoencoding schemes for LDPC codes and compares the areautilization of both on ASIC platform (2)LDPC codes are more efficient because ofBER performance. (3) The FPGA implementation is done onSpartan3E board and analysis was done based on device utilization bythe straightforwardmethod compared to that of lower triangular modificationapproach. (4) Reduce the complexity	(1) Utilization of power was not focused in both approach (2) Delay limitation in Lower triangular method was not focused
2	VLSI Implementation of a Rate Decoder for Structural LDPC Channel	Elsevier 2016	Sandeep Kakde, Atish Khobragade	(1) This paper proposes a low complexity LDPC design using message passing algorithm and systolic high throughput architecture.	(1) Implementation of Pipelining will reduce the device utilization in ASIC FPGA.

	Codes			(2) Whole LDPC design was designed simulated and synthesized using Xilinx ISE 13.1 EDA Tool. (3) LDPC codes can attain the close to Shannon limitperformance with the practical decoding complexity like turbo codes on an AWGN channel. (4) Focus on the various levels of obstruction in decoding design (5) Flexible VLSI architecture while efficient utilization of silicon area, latency and dynamic power metrics.	
3	Modified Approximate Lower Triangular Encoding of LDPC Codes	IEEE 2015	ArijitDutta, AnkitaPramanik	(1) New algorithm is proposed to bring any rectangular sparse LDPC matrix into a rectangular part and a square upper triangularpartof the H matrix (2) BERperformance of the new Modified ALT technique is comparedwith the Systematic Approximate Lower Triangularmethod. (3) The proposed algorithm gives improved BER performance.	(1) ASIC FPGA Implementation was not done (2) Performance oriented was not Compared between Modified ALT & Systematic ALT method
4	Flexible Hardware Architecture for LDPC Encoder	IEEE 2016	Jayashree C. Nidagundi, Dr.Siddarama R. Patil	(1) LDPC codes achieve improved performance and lower decoding complexity than Turbo codes (2) RU method encodes with propagation delay of 1.256ns less compare to general method of LDPC Encoder (3) Parameter analyzed are the number of slice LUTS, number used as logic, number of fully used LUT_FF, number of bonded IOB in ASIC FPGA (4) RU method encoding technique reduced complexity and improved speed.	(1) ALT and Modified ALT Methods are not compared which reduce the complexity in LDPC encoding.
5	FPGA Implementation Of Linear LDPC	IJRET, 2013	Chetna N. Kharkar, M. M. Jadhav, A. M.	(1) ASIC Field Programmable Gate Array implementation of linear time LDPC encoder	(1) Utilization of power was not focused in Linear

	Encoder		Sapkal,	(2) Linear Time encoder hardware architecture reduces the Complexity and efficient use of area than generator matrix based encoder techniques	Time Encoder technique (2) Implementation of Pipelining will reduce the device utilization inFPGA

Table 1. Survey of LDPC Code

4. Conclusion

A detailed Survey of above listed paper we concluded the following

The implementation of decoder should be simple compare to encoding. Complexity in encoding refers to number of mathematical operations involved in processing parity check matrix and generator matrix. The regularity and structure of LDPC codes simplifies the implementation of LDPC Code. An LDPC code fulfils error correction and detection codes bit error performance should approach asymptotically the Shanon limit.

In communication SNR (signal to noise ratio) must be high where the noiseless transaction. In LDPC codes improves the SNR, but geometry based design of LDPC codes provides low SNR than turbo structured LDPC code. Pipelined Structure ASIC implementation reduces the utilization of area and provides less delay compared to non-pipelined Structure. Improved Bit Error Rate achieved using new Modified ALT technique is comparedwith the Systematic Approximate Lower Triangularmethod. RU method encodes with propagation delay of 1.256ns less compare to general method of LDPC Encoder.

Major drawback of LDPC codes is its high encoding complexity and also semi parallel LDPC architecture imposes constraints on the code matrix to extract some parallelism to avoid communication conflicts which may be advantageous but drawback of these is memory conflicts and complex control decoding.

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