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State of the Art Computational Ternary Logic Currnent-Mode Circuits Based on CNTFET Technology

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Abstract

Computational operations are considered as a time-consuming and important operation in ALU. These circuits play major role in computational operation in processing unit. This paper presents new computational Ternary Current Mode Circuits including comparator, multiplexer, decoder, and exclusive OR by means of Carbon NanoTube Field Effect Transistors. The new designs rely on three major parts: 1) the input currents which are converted to voltage; 2) threshold detectors; and 3) the output current flow paths to generate the outputs. The designs have been simulated based on 32nm CNFTET using Synopsys Hspice simulator.

Keywords: Current Mode Logic; Ternary Current Mode Comparator; Ternary Current Mode Multiplexer; Ternary Current Mode Decoder; Ternary Current Mode Exclusive OR; CNTFET.

1. Introduction

Traditionally, more than two logical values are utilized in Multiple-Valued Logic (MVL) computations, despite the binary logic. The additional values lead to noticeable merits such as fewer interconnections, pinouts, active devices, less occupied area, and higher parallel and serial communication rates [1, 2]. Great challenges and difficulties in massive amount of wiring congestion inside recent nanoscale chips have addressed circuit and system designers to consider the realization of MVL circuits seriously. several difficulties and restrictions like undesired parasitic effects, high power dissipation, and limitation of routing and placement processes in logical elements can be considered as main drawbacks of the massive amount of interconnections [3, 4]. One solution to overcome these problems is using higher radix number systems.

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In a nutshell, MVL is a mixture design technique of digital and analogue signal processing. It benefits from noise tolerance of a digital signal and the ability of more information processing in the analogue mode [5]. As mentioned in [6] ternary logic, which uses three logical values (‘0’, ‘1’, and ‘2’) introduced by 0 V, Vdd/2, Vdd, is considered as the most effective MVL system.

Among computational and logical operations, comparators, multiplexer, decoder, and exclusive OR are consider as the most important and time-consuming operations inside Arithmetic Logic Unit (ALU) of microprocessors. They include considerable interconnections, and occupied substantial area. Therefore, their improvement is an essential factor in computational units. Each presented Ternary current mode circuit consist of three major parts to perform the required functions [9, 10]. Several peer circuits have been discussed previously [9, 10]

Current mode logic approach brings some advantages when using in MVL such as: i. the ability of making sophisticated circuits by means of different Threshold Detectors (TD) [1]; ii. Less noise sensitivity [9]; iii. Copying, scaling, and duplicating currents by using a simple current mirror circuit [10]; iv. High-speed operation [10]; and v. The slight effects of the fan-out circuits [11]. Although, high static power dissipation and tolerance are considered as the main drawbacks of CML [9- 11].

Traditionally, Current mode circuits are implemented by either bipolar (bipolar CML) or MOS (MCML) devices. However, MCML is preferred for mixed analog-digital signal environments due to high power consumption of bipolar transistors and higher supply noise immunity of MOS devices [12].

This paper presents a novel current-mode computational Ternary Circuits including comparators, multiplexer, decoder, and exclusive OR. Several current-mode ternary peer circuits have been presented previously [7, 8]. However their implementation technique is different and based on MOSFET technology [7, 8]. In this paper, some (TD) are employed in order to produce required logical output levels.

The proposed designs rely on Carbon NanoTube Field Effect of Transistors (CNTFET). For many years, the Bulk Complementary Metal-Oxide-Semiconductor (Bulk-CMOS) has been the main technology for implementing energy-efficient and dense VLSI circuits. Meanwhile, the emerging trend of scaling down the feature size of CMOS technology in nano-ranges leads to various challenges and difficulties [13]. The main demerits include very high leakage currents, high power density, large parametric variations, and decreased gate control, which would affect the suitability of the current technology for nowadays and hereafter high-performance applications, considerably [13, 14]. Many nanometer technologies such as CNTFET [14-16], Single Electron Transistor (SET) [17], and Quantum-dot Cellular Automata (QCA) [18] have been introduced to combat these challenges. Among them, CNTFET is considered as the most promising successor for MOS technology in the near future. This principally originated from the unique specifications of this technology like ballistic transport attribute, the same mobility for both nCNTFET and pCNTFET, and the ability of altering threshold voltage, which is a key feature in MVL circuitry [14-16].

The rest of the paper is organized as follows: In section 2, reviews the CNTFET technology. Section 3 presents the presented CML ternary circuits. Simulation results are presented in Section 4. Finally, Section 5 concludes

the paper.

2. Review of CNTFET Technology

The great trend of scaling down of semiconductor devices and integrated circuits into nanometers in nano-electronics era causes semiconductor industry encounter difficulties and challenges, these challenges include: increased short-channel effects, reduced gate control, exponentially rising leakage currents, severe process variations, and unmanageable power densities [13].

In case being the scaling down of MOSFET technology has progressed rapidly. But, it has to come to an end soon because of increasing short channel effects and power-dissipation constraints [13].

Using Carbon Nano-Tube Field Effect Transistors (CNTFET) is considered as an optimized Nano-scaled device to implement high performance, very dense and low power circuits [14-16].

The base of a CNTFET is made of carbon Nano-tube. CNFETs. Like MOSFETs, they have P-type and N-type devices, and 4 terminals [14- 16]. However, both P-type and N-type CNTFETs with the same device size have the same mobility. This specification leads to significantly simplify the process of transistor sizing, particularly in complex circuits with a large number of transistors [14- 16].

The most common type of CNTFET using for the transistor is Single-Wall Carbon Nano-Tube (SWCNT) which consists of only one cylinder. This type can act as either a conductor or a semiconductor regarding to the angle of the atom arrangement along the tube. This arrangement is so called the Chirality vector. It is represented by the integer pair (n, m) [12]. The diameter of the CNTFET can be calculated as follows [14, 15]:

$$D_{CNT} = \frac{\sqrt{3 \times a_0}}{\pi} \times \sqrt{n^2 + m^2 + n \times m} \quad (1)$$

While, a0 = 0.142nm is the inter-atomic distance between each carbon atom and its neighbor.

The ability of adjusting the required threshold voltage is one of the key superiority of CNTFET in comparison with MOSFET technology. The threshold voltage is defined as the voltage level required to switch on a transistor. This unique feature helps us to set TDs in order to switch correctly. The threshold voltage of the basic CNTFET channel is an inverse function of the diameter [14, 15]:

$$V_{Th} = \frac{0.43}{D_{CNT}(nanometer)} \quad (2)$$

Here, a = 2.49 Å is the carbon to carbon atom distance, Vπ = 3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and DCNT is the CNTFET diameter [14, 15].

3. The Proposed Current Mode Ternary Computational Circuits

Logical circuits, including comparators, multiplexer, decoder, and exclusive OR and OR are considered as the most essential and fundamental operators in digital electronics and logical units.

In this section, new single-digit Ternary comparators, multiplexer, decoder, and exclusive OR circuits are proposed separately. It worth to mention that a ternary digit (trit) includes 1.5 times more information than a binary one. It can take logic values '0', '1', and '2' [12]. The proposed circuits use a technique that converts the input currents to voltage [19]. The switching activity of the related transistors is governed by responsible threshold detectors, which are situated on the output paths. If all of the related transistors are switched on, a unit of current (8μA) flows through each output path represent the logical value of '1'. in addition, if of the output logical value equals to '2', the currents of two different paths are linked together in order to increase the amount of current unit to 16μA.

A single-digit ternary comparator is presented in this paper (Figure 1). The construction of the new design is based on the sum of input currents (Σin), which is converted to voltage by a diode-connected transistor, T1, T6 (Figure 1). Then, the exact value of Σin is realized using threshold detectors. TDs are in fact binary inverters with shifted Voltage Transfer Characteristic (VTC) curves [12]. At last, the p-type transistors in a pull-up network would convert the voltages once again to current. They switch on and produce a unit of current, which is considered to be 8μA in this paper. Three parallel p-type transistors are utilized to show whether the input signals are exact situations of input current (equal, less, greater).

In all proposed designs (Figs.1, 2, 3, 4), the transistors are marked by three values, the diameter of CNTs (DCNT), which indicates threshold voltage (Eq. 1), the number of CNTs (Tube), and Pitch. The latter is the distance between two neighboring CNTs [14-16]. The channel (Lg) and doped CNT source- (Lss) and drain-side (Ldd) extension regions for the diode-connected transistors in all proposed designs, (T1, T6) in for instance Figure1 are lengthened in order to achieve higher resistivity. Despite more resistance, operating speed is not degraded, due to the facts that, these converting transistors are not placed along with the critical path of the cell. The same parameters (Lg, Lss, and Ldd) equal 32nm for the rest of the transistors.

A brief summary is provided to explain the operation of the proposed TCMCOMP (Figure 1):

1. If Σin=0 (a=b), both T1, and T6 convert the input currents to voltage, then T2, and T3 would be turned off and the switched on transistors (T4, T5) provide the output current equal to '1' (8μA) to show the Equal signal.

2. If (a>b), then T1 converts input currents to voltage, T3, T4, and T5 would be turned off and the switched on transistor (T2) provides the output current equal to '1' (8μA) to represent the greater signal.

3. If (b>a), then T6 converts input currents to voltage. T2, T4, and T5 would be turned off and the

switched on transistor (T3) will provide the output current equal to ‘1’ (8µA) to signify the less signal.

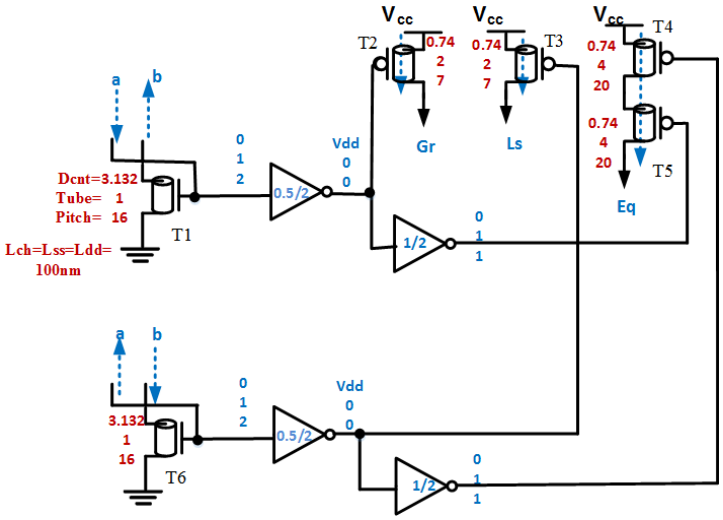

Figure1: the proposed current-mode single-digit ternary current mode comparator (TCMCOMP)

Figure2, depict Ternary current mode multiplexer (TCMMUX) based on mentioned Technology. It`s main functionality is similar to TCMCOMP, as well as using a different parts including the diode connector transistors and two TDs to implant the selector signal.

A brief summary of its operation is reviewed :

1.If S=0 (Selector), then the switched on T4 would active the path to provide the current ternary values of the input signal.

2.While S=1 (Selector), the switched on T8 and T9 would active the path to provide the current values of the input signal.

3.While S=2 (Selector), the switched on T13 would active the path to provide the current values of the input signal.

Ternary current mode Decoder (TCMDEC) based on mentioned Technology is represented in Fig3. It`s main functionality is similar to previous proposed structures.

A brief summary of its operation is discussed:

1. If a=0, then the responsible TDs make T2 switch on, the only active the path would provide the current value equal to ‘1’ (8µA) to represent X0 signal.

2. If a=1, then the responsible TDs make T3, T4 switch on, this active the path would provide the current value equal to ‘1’ (8µA) to represent X1 signal.

3. while a=0, the responsible TDs make T5 switch on, the individual active the path would provide the current value equal to '1' (8μA) to represent X2 signal.

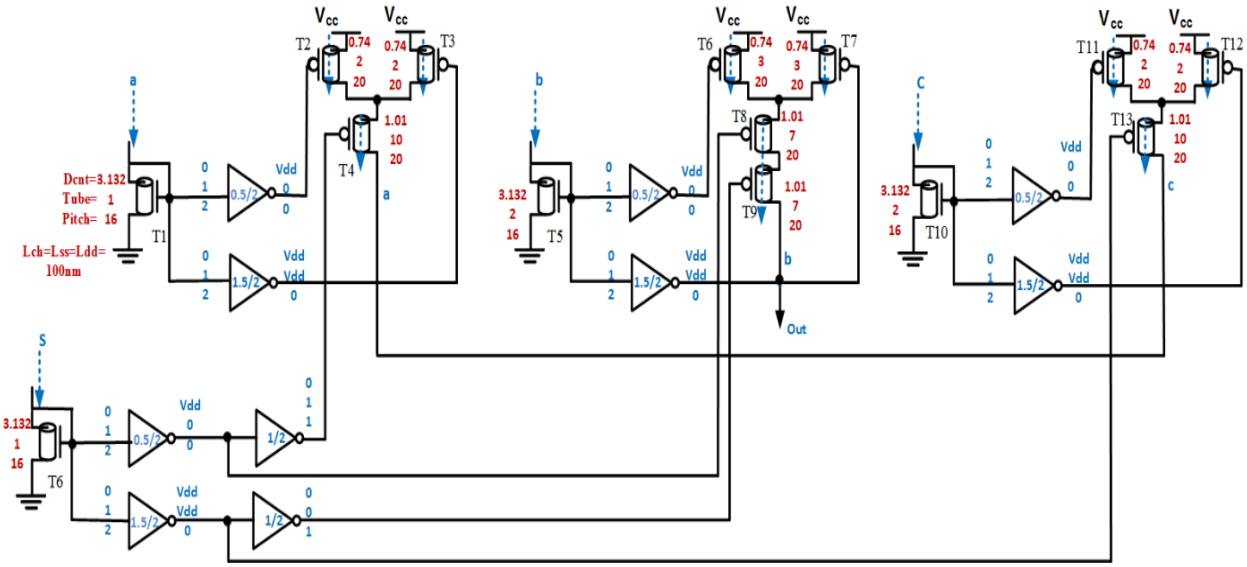

Figure 2: the proposed current-mode single-digit ternary current mode multiplexer (TCMMUX)

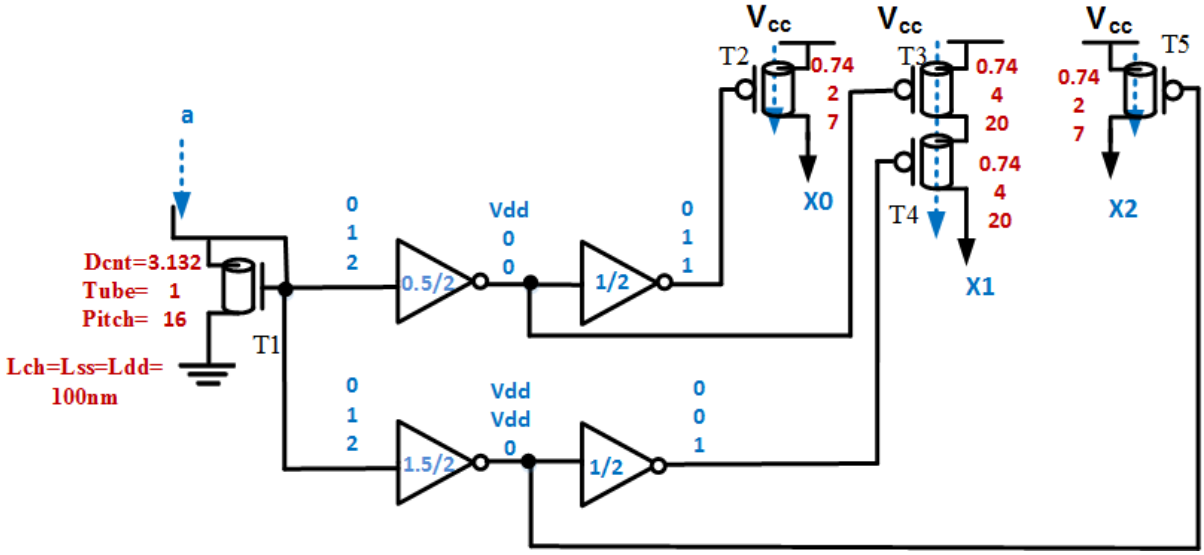

Figure 3: the proposed current-mode single-digit ternary current mode decoder (TCMDEC)

Figure 4 demonstrates, Ternary current mode Exclusive OR (TCMXOR) based on mentioned Technology. It1s function in Ternary logic is shown in Table 1. The input currents (a and b), have to be converted to voltage separately one again. Because, taking branches from the input currents is not possible due to the kirchhoff's current law [12, 19]. In CML, currents must be mirrored whenever another copy is required (Figure 4).

A brief summary of its operation is discussed:

1. If Σin=0, there is not any active path to provide output current. Although T25, T26, and T29 are switched o, but the output signal equals to 0V ‘0’.

2. If Σin=2 (a=2, b=0), then transistors T24, T25, T26 and T27 provide two active paths eachof them equals to ‘1’. Consequently, 16μA of current flows.

3. If Σin=2 (a=0, b=2), then transistors of two parallel paths, including T24, T25, T28 and T29 provide two active paths each equals to ‘1’. Then, the output would be equal to 16μA.

4. If Σin=2 (a=1, b=1), then turned on transistors in the only active path including T24, T25 provide a unit current of 8μA to the output.

5. If Σin=3 (a=1, b=2), then two parallel paths, including T24,T25, T28 and T29 transistors provide two active paths each equals to ‘1’. So, 16μA of current flows in the output.

6. If Σin=3 (a=2, b=1), then the switched on transistors of two parallel paths, including T24,T25, T26 and T27 provide the active paths each equals to ‘1’, finally the output would be 16μA.

7. If Σin=4 (a=2, b=2), there is no active path to convey the output current.

Table 1: Truth table of a single-digit ternary current mode exclusive or function

A	**b**	**Σ(a,b)**	**XOR**
0	0	0	0
0	1	1	1
0	2	2	2
1	0	1	1
1	1	2	1
1	2	3	1
2	0	2	2
2	1	3	1
2	2	4	0

All proposed novel designs benefit from simple design and advantages of CML. Unlike voltage-mode logic, it is possible to combine two different wires in CML [12, 19]. When it applies to a junction, currents with the same direction are summed up. Even the subtraction of the input signals are possible by changing the direction of one of them (Figure1). It is worth mentioning that there is a major difference between the linear summation of currents and the real addition. In addition, the output number set must be the same as input one [9].

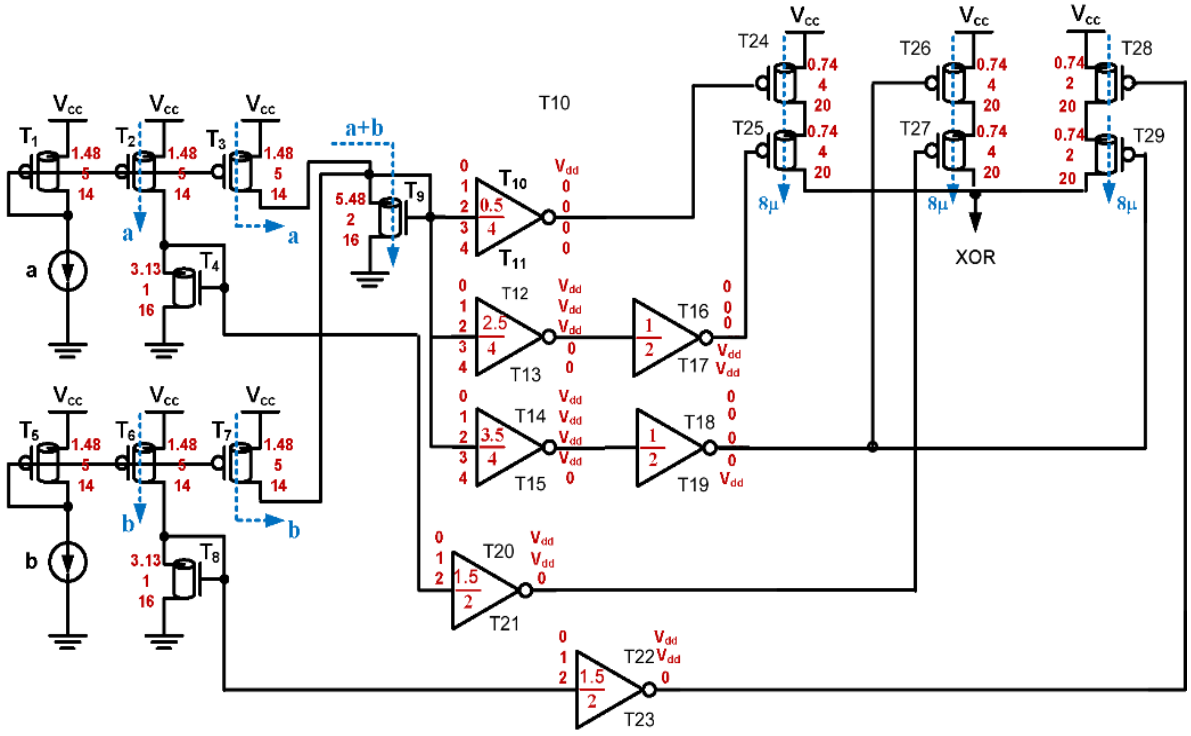

Figure4: the proposed current-mode single-digit ternary current mode exclusive OR (TCMXOR)

4. Simulation Results

All of the proposed designs, including the current mode comparator, multiplexer, decoder and exclusive OR, are simulated by Synopsys HSPICE with 32nm CNTFET technology [14, 15]. Simulations are fulfilled in 1V power supply and 1GHz operating frequency at room temperature, with an 8µA unit of current. Simulation results are reported in Table 2. In order to obtain delay (τ), the complete input pattern, including 72 transitions (Figure5, 6), is fed to the proposed ternary comparator and exclusive OR, whereas random input patterns are applied to the decoder and multiplexer circuits (Fig, 7, 8). The average power consumption during all transitions is also measured. In addition, static power is considerable in CML. Therefore, it is separately measured while the inputs are kept constant. The entire possible input patterns (Tables 1) are individually fed to the circuits to measure stand-by power dissipation. The average amount is also reported in Table 2. Finally, Power-Delay Product (PDP) is an important parameter, which makes a trade-off between the delay and power factors (Eq. 3).

$$PDP = \text{Maximum Delay} \times \text{Average Power} \quad (3)$$

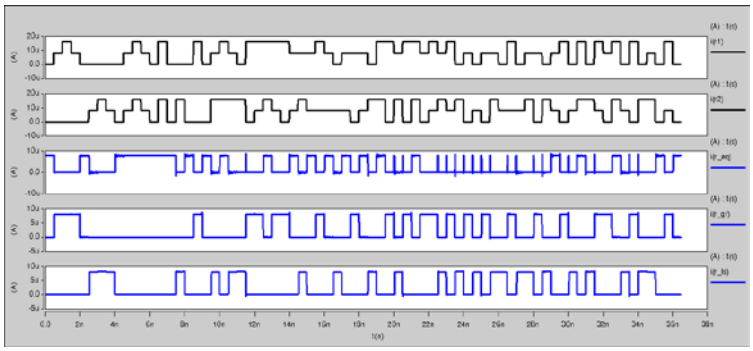

Figure5: Input and output waveforms of the proposed current-mode single-digit ternary comparator (TCMCOMP)

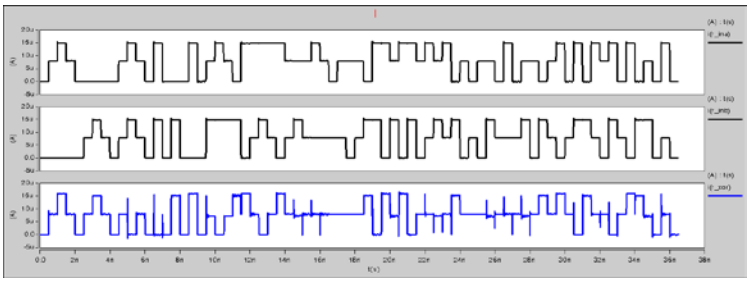

Figure6: Input and output waveforms of the proposed current-mode single-digit ternary exclusive OR (TCMXOR)

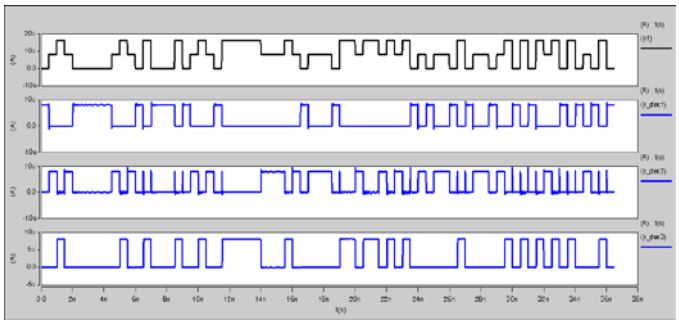

Figure7: Input and output waveforms of the proposed current-mode single-digit ternary decoder (TCMDEC)

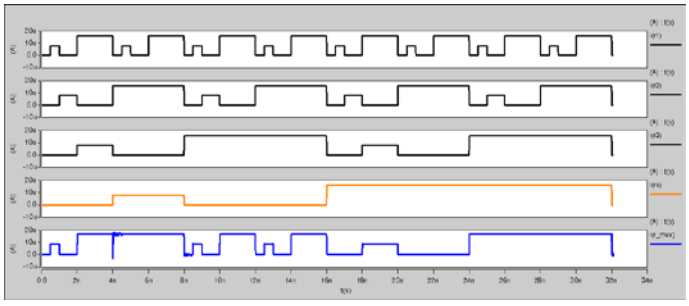

Figure8: Input and output waveforms of the proposed current-mode single-digit ternary multiplexer (TCMMUX)

Table 2: simulation results of the new circuits

Block	Delay (psec)	Power (□W)	PDP (fJ)	Static Power (□W)	#Transistor	#Voltage Levels
TCMCOM	44.501	40.308	1.7937	25.998	14	3
TCMMUX	14.847	40.665	0.60378	30.317	34	3
TCMDEC	32.013	14.062	0.45018	14.138	13	3
TCMXOR	37.239	46.765	1.7415	47.288	29	5

Sensitivity to the variation of temperature is put under examination for the proposed designs. The amount of energy consumption (PDP) versus a wide range of ambient temperatures, from 0 □C to 70□C, is Figure 9. The proposed designs show insignificant sensitivity to temperature variations.

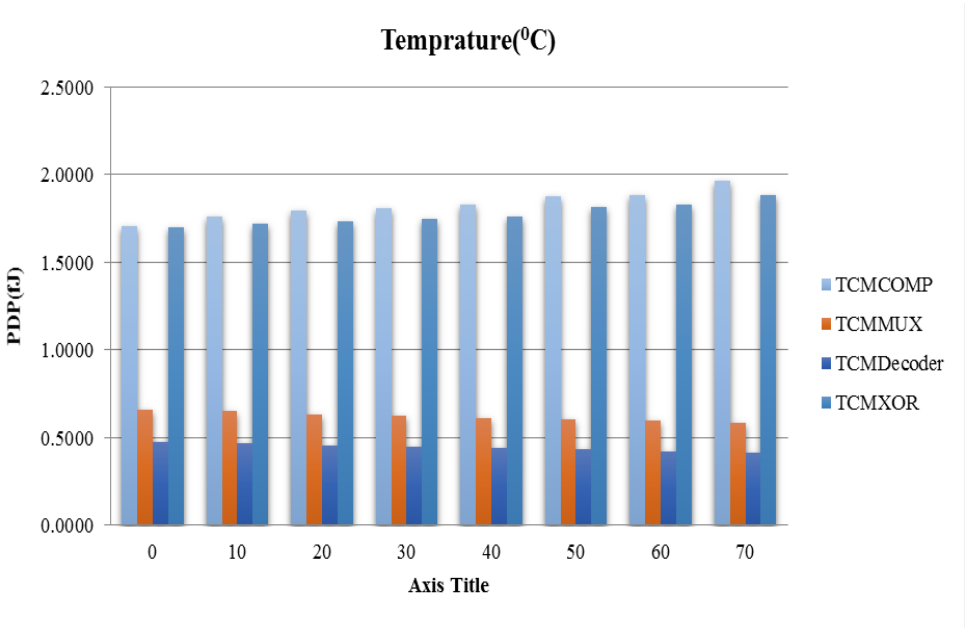

Figure 9: PDP of the proposed designs versus the temperature

Sensitivity to the variation of working frequency in 1GHz, 2GHz, and 4GHz is put under examination for the proposed designs.

The amount of energy consumption (PDP), is presented in Table 3.

One key benefit of CML over VML is that fan-out circuits do not cause speed degradation and performance loss for the current-mode circuits [12]. This mainly originates from the way that fan-out circuits are connected to a current-mode circuit [12]. This capability has been tested by re-simulations [12]. Table 4 exhibits that the existence of the output load transistor and the connection of the fan-out circuits do not rise cell delay. This is

just in contrast with VML in which as the output load increases, voltage-mode circuits operate slower [20, 21].

Table 3: simulation results of the new circuits versus working frequencies

Block	**1GHZ**		
	Delay (psec)	**Power (□W)**	**PDP (fJ)**
TCMCOM	44.501	40.308	1.7937
TCMMUX	14.847	40.665	0.60378
TCMDEC	32.013	14.062	0.45018
TCMXOR	37.239	46.765	1.7415
Block	**2GHZ**		
	Delay (psec)	**Power (□W)**	**PDP (fJ)**
TCMCOM	44.672	39.673	1.7723
TCMMUX	15.479	40.652	0.62927
TCMDEC	30.652	14.054	0.45083
TCMXOR	37.141	46.877	1.7411
Block	**4GHZ**		
	Delay (psec)	**Power (□W)**	**PDP (fJ)**
TCMCOM	44.244	38.407	1.6993
TCMMUX	15.402	40.615	0.62556
TCMDEC	31.951	14.069	0.44954
TCMXOR	37.198	47.112	1.7524

The simulation results express that all the proposed designs in addition to benefiting from CMMVL and CNTFET technology advantages as mentioned before, also present simple and novel design by means of less transistors and TDs. Although as mentioned before the CMMVL designs suffer from high static power dissipation and tolerance as the main disadvantages of CML [9- 11]. In addition adjusting the switching point of TDs to drive the related transistors may be sensitive, however utilizing the CNTFET technology respecting to its

unique characteristics blurs this challenge [15, 16].

Their functionality has been tested in various situations by means of Hspice simulator. Finally, the common parts could be easily integrated in order to combine two different circuits in CML.

Table 4: Delay parameter of the proposed designs versus the output load(s)

Designs	**Without Any Output Loads**	**With The Output Load**	**With The Output Load Transistor and 4 Copies of the Output Current**
	Delay(psec)	**Delay(psec)**	**Delay(psec)**
TCMCOM	44.501	45.066	45.001
TCMMUX	14.847	16.194	16.13
TCMDEC	32.013	32.502	32.453
TCMXOR	37.239	38.475	37.822

5. Conclusion

In this paper, novel designs of current-mode Ternary computational circuits, including comparator, multiplexer, decoder and exclusive OR based on CNTFET technology have been proposed. The new designs rely on mixed current and voltage logics and threshold detectors to switch on or off the related transistors, resulting in the elimination of constant independent current sources. These designs have been simulated in different situations to demonstrate their functionality. The simulation results show that the designs in addition to the simple and novel design perform their functionality in various situations. Meanwhile, despite the VML, fan-out circuits have almost no effect on the delay parameter. Finally, the common parts could be easily integrated in order to combine two different circuits in CML.

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