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A Reduced Size Look Up Table for Sinusoidal Wave Generation in Digital Modulators Applications

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ABSTRACT

Digital Modulators is one of the areas that have received great attention recently due to the tremendous developments in Radio Frequency (RF) frond ends and system on chips (soc) architecture in general. Building any kind of digital modulators using soc type Field Programmable Gate Array (FPGA), like ZYBO, depends heavily on how the carrier signal got generated since it consumes a lot of utilization recourses. This paper presents a new method of generating sinusoidal carrier signal based on Direct Digital Synthesizer (DDS) concept using small size Look Up Table (LUT). 64 samples of a quarter period of the sine wave signal were stored in a fixed point format in small LUT to generate the carrier at the desire frequency. The paper used Very high speed integrated circuit Hardware Descriptive Language (VHDL) without the help of DSP Builder Tools or XILINX System Generator. The suggested method was tested by building simple modulators like On-Off Keying (OOK) and Amplitude Shift Keying (ASK). Low utilization was achieved as compared to other implementation methods.

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1. Introduction

Software Defined Radio (SDR) or simply Software Radio (SR), which was first presented by Joseph Metola in 1990s as a new method of building communication systems [1]-[2], has become a widely used technique of implementing different kinds of communication systems. It has become a well-known method of either augmenting or even replacing the current implemented ones. One of the research areas in SDR-based systems is digital transmitters. Digital transmitters have received great attention recently due to the tremendous development in reconfigurable hardware recourses which represent the backbone of any SDR-based system. The main idea of building any SDR-based digital transmitter is using low cost terminals such as Application Specific Integrated Circuit (ASIC) devices or Field Programmable Gate Array (FPGA) as the base of implementation.

The last few years have seen a great progress in this direction from the implementation of simple modulation schemes such as Frequency Shift Keying(FSK), Amplitude Shift Keying (ASK), and Phase Shift Keying (PSK) and up to the most advanced ones such as Quadrature Amplitude Modulation(QAM) and Quadrature PSK (QPSK)[3]-[5]. Unfortunately, almost all of these papers used MATLAB and either XILINX System Generator or DSP Builder Tools (Co simulation tools) as the main implementation software [5]. Using software like these means higher cost. Not only the high cost is the problem, it also doesn't give the design engineers a direct control on their implemented systems. To solve these issues, several papers have been presented such as the work of Al-safi and Bazuin [6]-[7].Their work used VHDL as the main implementation tool without using any Co simulation tools, or Intellectual Property (IP) blocks.

The main purpose of this paper is to investigate the possibility of reducing the utilization recourses by looking at an alternative solution to reduce the design cost especially the utilization increase caused by carrier generation. ASK, and OOK were used to test the system performance based on the new carrier generation method.
The rest of the paper is organized as follow, section II will present the main research statement, and section III illustrates the currently used implementation methods as well as the suggested one. Section IV presents the obtained implementation results, and finally section V will show the conclusion and recommendations for future work.

2. Problem Statement

The main components in building any FPGA based digital transmitter based on SDR concept are FPGA, Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), and RF mixer. The common software tools that have been used so far are MATLAB with the Co-simulation tools. In these cases, Co-simulation tools have to generate the Hardware Descriptive Language (HDL) based implementation based on the simulated MATLAB model. Co simulation tools usually use available IP blocks to build the simulated models which makes the design cost very high. The other way of building an FPGA based systems is using Very high speed integrated circuit Hardware Descriptive Language (VHDL) or Verilog directly. This kind of implementation means low cost, direct control on the built systems but it might not be efficient as the ones that were built using MATLAB and the Co simulation tools.
To get an optimum design, we have to look for an alternative design solution to reduce the utilization cost and increase the performance efficiency. The high utilization cost usually caused by the carrier wave generation, phase shifting, and multiplication instructions. Al-safi and Bazuin presented several papers that reduced the implementation cost caused by multiplication instructions and phase shifting [6]-[7] by using Feher modulation concept [8].
This research paper presents a new method to reduce the cost generated by carrier wave by using a reduced size Look Up Table (LUT). Carrier wave generation based on LUT, which can give a high resolution signal [9], is the main way of implementing sinusoidal wave carrier in this paper not the COordinate Rotation DIgital Computer CORDIC one [10].

3. The Suggested Implementaation Method

The suggested implementation method use Random Access Memory (RAM) within the FPGA board to store 64 values of the fixed point representation of quarter period of the sinusoidal signal only to generate the whole carrier wave. Let us assume that we generate a full period sine wave signal in a fixed point format using MATLAB. From these 256 samples we can use 64 samples only (quarter wave) to generate the whole wave carrier as shown in the code in Table. 1.

Table 1: MATLAB code for sine wave generation.

```
LUT=zeros(128,1);
LUT2=zeros(256,1);
 for i=1:64
   LUT(i)=Rom(i);
End;
for i=1:64
   LUT(64+i)=Rom(65-i);
end ;
LUT2(1:128)=LUT;
LUT2(129:256)=-1*LUT;
plot(Rom,'k');
hold on;
plot(LUT,'b');
plot(LUT2,'r');
grid on;
```

If we use 256 samples to represent the whole wave then each quarter can be epresented by 64 samples as shown in Table. 2:

Table 2: Quarter location based on the sample number.

Samples range	Quarter location
1-64	first quarter
65-128	second quarter
129- 192	third quarter
193-256	fourth quarter

But quarters 2-4 can be calculated based on the samples available in the first qurter as shown in the MATLAB code in Table. 1. The main idea behind that can be explained by looking at figures 1-3 shown below. Fig.1 represents the 64 samples that we need to store in the LUT to generate half wave as in Fig.2 or the whole wave as in Fig.3 at any desired frequency.

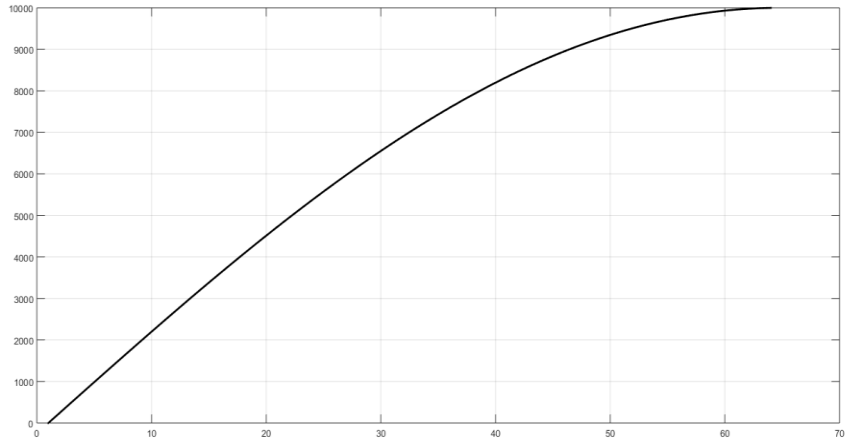

Figure 1: Quarter period of sinusoidal signal.

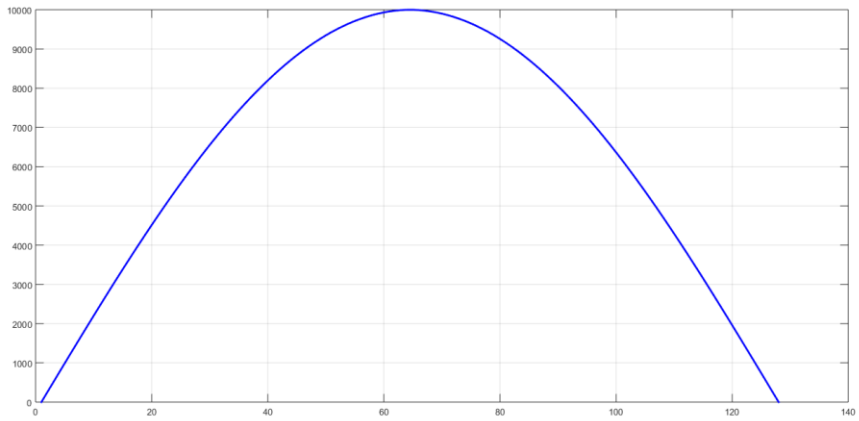

Figure 2: Half period of sinusoidal signal.

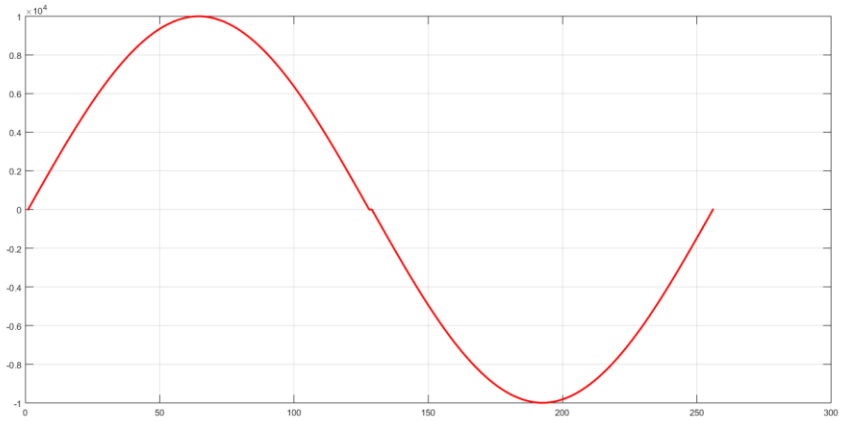

Figure 3: Full period of sinusoidal signal.

This process looks very simple in MATLAB but in VHDL it is a little more complex than that.

4. Implementation and Results

The suggested sine wave generation method using reduced size LUT based on DDS concept presented in section III was used to implement two kinds of digital modulators. The chosen modulators were Binary ASK (BASK) and OOK since OOK and ASK are the easiest modulation schemes as shown in Fig. 4.

For the ASK modulator implementation, an 8-bit phase accumulator working on the rising edge of the clock was used. This accumulator generates the required phases to cover the angles between 0-360. The two most significant bits of the accumulator were used to select in which quarter the angle was located. The rest 6-bits of the accumulator were used to look at the LUT to see the corresponding fixed values of the sine wave for that angle. The obtained sine value must be adjusted to reflect the location of the angle using the same concept presented in the MATLAB code in Table.1. Now the generated sine wave can be used to implement BASK or OOK modulators as shown in Figs. 5-6 respectively. Instead of using 256 samples LUT, this time 64 samples will be enough to generate the carrier wave. The information signal was used as the the MUX circuit selector in as shown in Fig. 5. The inputs to the MUX circuit are two sinusoidal signals while the information signal will work as a selector. These two sine waves can be generated from the same 64 values LUT and the 8-bit accumulator. The generated sine wave signal refers to the message bit "1" while the second signal refers to the message bit "0" is the generated sine wave after dividing its amplitude by two. The best way to do amplitude division in VHDL is by using shift to the right operation as shown in Fig. 5. The widths of the output sine wave and BASK modulated signal were selected to be 16-bit. 8-bit width works also but we are looking for a smoother and a cleaner signal. The message signal that used in the simulation and implementation was generated using simple counter driven by the main board clock.

In OOK modulator, the modulated output signal is either sine wave or zero based on the information signal. Implementing this form of ASK is almost similar to the previous one. The only change that we have to do now will be in the MUX circuit by giving it a ground signal instead of one of the sine wave signals as shown in Fig. 6. The modulated BASK and OOK signals are shown in Figs. 7-8 respectively.

To download the design on the FPGA board (ZYBO), we need to write the .xdc file which explains the used input and output pins. The targeted board for the implementation is ZYBO board from Digilent [11] which is shown in Fig.9. The ZYBO board is an entry level embedded platform which is built around a Xilinx Zynq-7000 (Z-7010) family device. The Z-7010 is based on Xilinx Programmable SoC architecture, integrating a dual-core ARM Cortex-A9 processor with Xilinx 7-eries FPGA. The ZYBO board has a rich set of multimedia and connectivity peripherals, including; video and audio I/O, dual-role USB, on-board memories, Ethernet, and SD slot. Besides these peripherals, it contains six PMOD ports with pins connected to the Xilinx device that can be connected to a range of available devices. Unfortunately, getting a terminal that has 16-bit was not that easy. Hence we used one of JE pmod output which has 8 pins and used the eight most significant bits of the output result just to see the resources utilization reports.

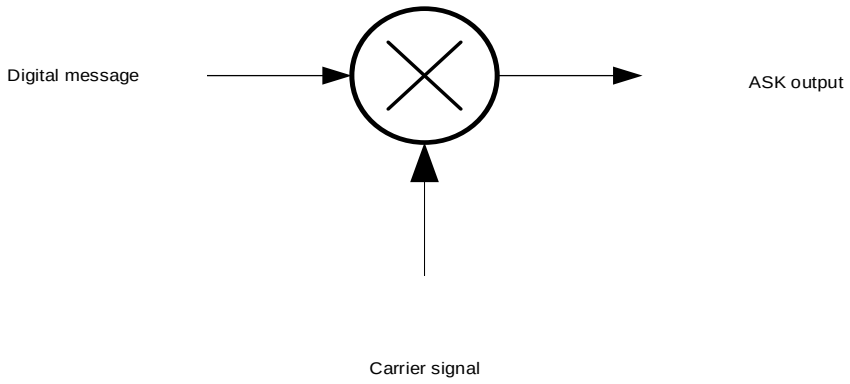

Figure 4: ASK modulator.

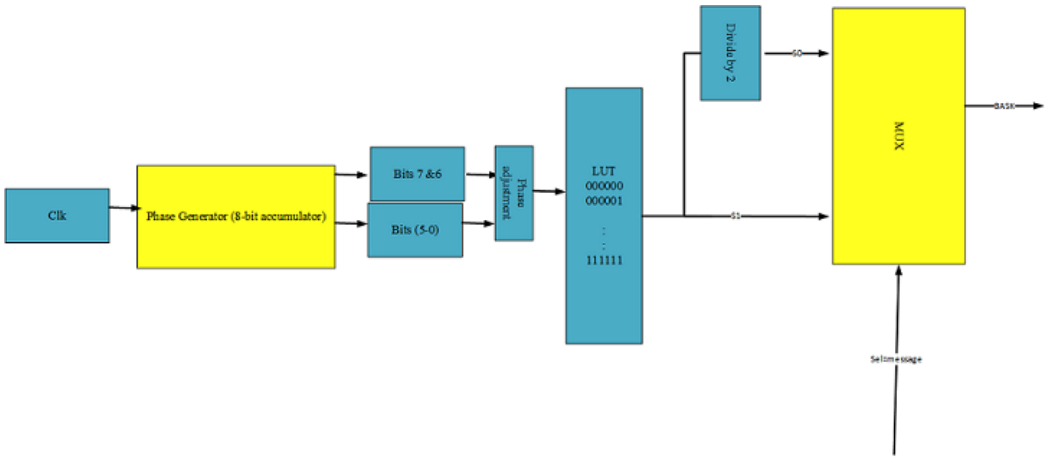

Figure 5: VHDL based ASK modulator.

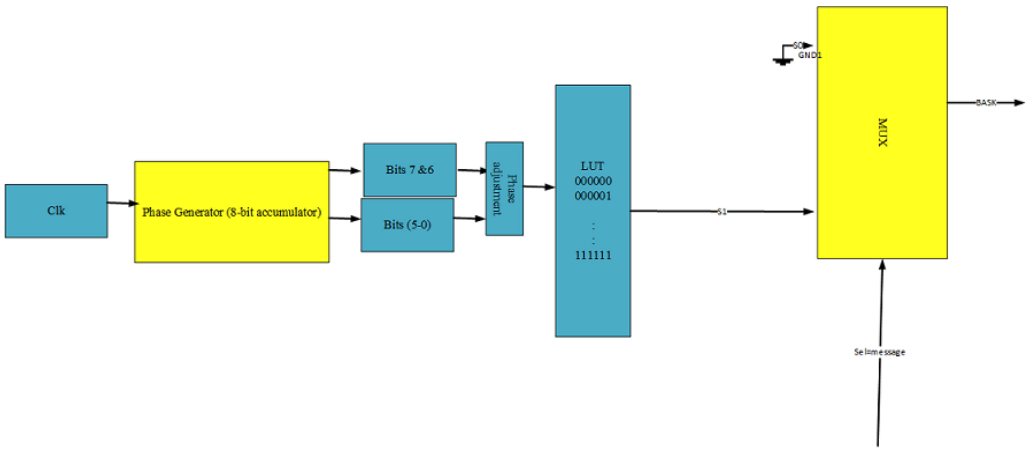

Figure 6: VHDL based ASK(OOK) modulator.

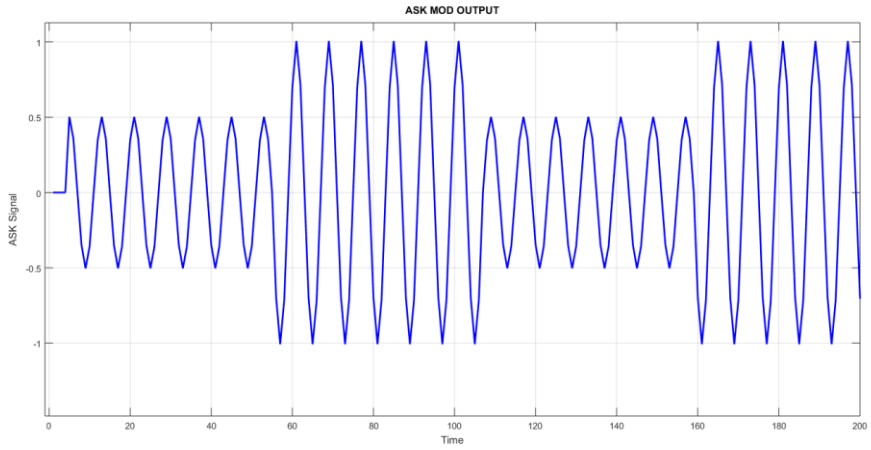

Figure 7: BASK Modulation results.

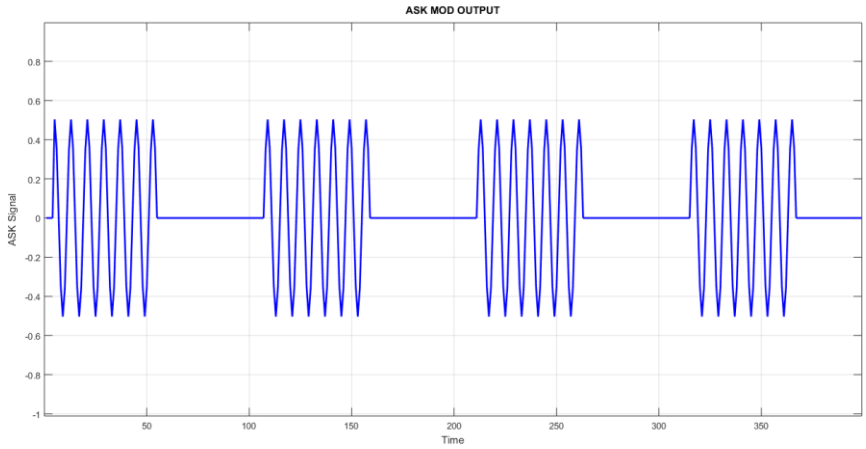

Figure 8: OOK modulation results.

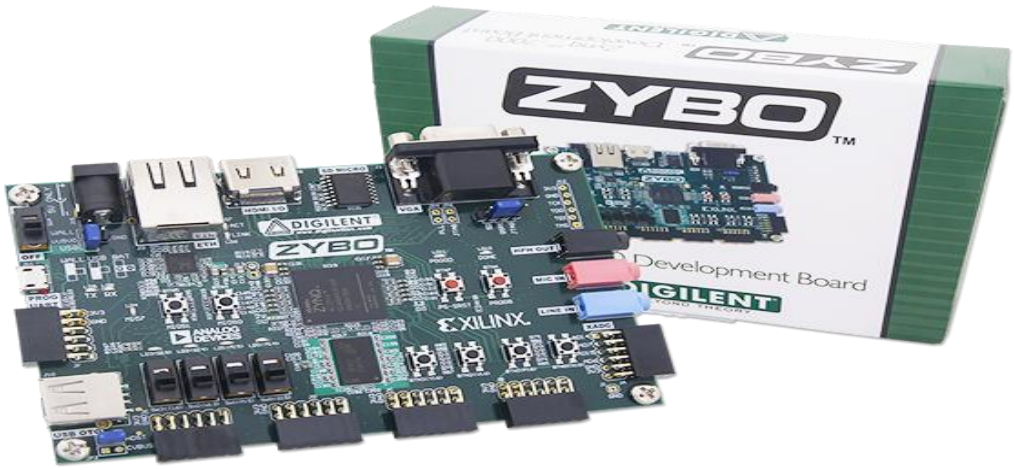

Figure 9: ZYBO board.

After downloading the design on the board we got the project utilization report for the built ASK modulator as shown in Table. 3 which look a little better than utilization recourses based on a full period sine wave as shown in table 4.

Table 3: Device utilization report of the ASK modulator based on the suggested method.

Resource	Utilization	Available	Utilization %
LUT	10	17600	0.06
FF	10	35200	0.03
IO	9	100	9.00
BUFG	1	32	3.13

Table 4: Device utilization report of the ASK modulator based on the old method.

Resource	Utilization	Available	Utilization %
LUT	11	17600	0.06
FF	11	35200	0.03
IO	9	100	9.00
BUFG	1	32	3.13

5. Conclusion and Future Work

A new method of generating sinusoidal carrier wave for digital modulators was presented in this paper. The presented method was tested by implementing simple OOK and ASK modulators. A reduction in recourses utilization was achieved. Even if it may not be so obvious but for big systems design, the recourses utilization reduction will make a huge impact on the overall design. As a future work, the authors suggest the use of the presented method to build other kinds of digital modulators to check their performances and follow Ref.[12] to compare performance of the new implementation method as compared with the old ones especially in term of resources utilization and IP blocks usages.

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