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EMI design of flyover QSFP (FQSFP) connector for 56+ Gbps applications, system level modelling of the Z-directed component (ZDC)

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EMI DESIGN OF FLYOVER QSFP (FQSFP) CONNECTOR FOR 56+ Gbps APPLICATIONS, SYSTEM LEVEL MODELLING OF THE Z- DIRECTED COMPONENT (ZDC)

by

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ABSTRACT

This thesis comprises of two parts. Firstly, the Flyover Quad Small Form Pluggable (FQSFP) approach for 56+ Gbps applications is introduced to overcome the limitations from a large loss on typical QSFP ports with surface mount to Printed Circuit Board (PCB) traces. By replacing the PCB traces to the twinax cables, it is possible to achieve around 7 dB lower insertion loss at 40 GHz for the 12-inch path from the switch IC to connector than that of PCB trace with a low loss substrate. Also, to investigate electromagnetic interference (EMI) aspect of FQSFP approach, a simulation model of FQSFP has been developed which corroborates favorably with measurement profiles of time domain reflectometry (TDR) at FQSFP port and total radiated power (TRP) from FQSFP in a test vehicle. Furthermore, the EMI profile of the FQSFP after integration of the cage has also been studied.

The second portion of the thesis includes the system level implementation of a novel Z-directed component (ZDC) capacitor studied in two phases. Firstly, the ZDC interaction with planes is modelled using full wave 3D simulation and the impedance profile is compared to that of a regular decoupling capacitor, when it is placed far away from the Integrated Circuit (IC). Secondly, utilizing a commercial tool, the ZDC is implemented on a real PCB design where the local decoupling capacitors underneath the IC are replaced with ZDC and their performances are compared. It is shown that the high frequency performance can be significantly improved by reducing the current path inductance, the advantage of using ZDC.

ACKNOWLEDGMENTS

Foremost, I would like to express my sincere gratitude to my advisor Dr. James Drewniak, for an opportunity to carry out my masters' theses under his supervision, for demonstrating patience, inspiration and support despite continued challenges in my journey.

I would like to thank my committee members Dr. Pommerenke and Dr. Hwang for their valuable insights in my research. I am grateful to all the students at EMC Laboratory for encouraging insightful discussions that contributed much to my understanding.

Last but never the least, I would like to praise my Lord for his grace and comfort through his Word. Also, my family members and church friends at both the Rolla Bible Church and Indian Community Church for their never ending support, prayers and love.

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LIST OF ACRONYMS

EMI	ELECTROMAGNETIC INTERFERENCE
PI	POWER INTEGRITY
SI	SIGNAL INTEGRITY
TRP	TOTAL RADIATED POWER
QSFP	QUAD SMALL FORM-FACTOR PLUGGABLE
FQSFP	FLYOVER QUAD SMALL FORM-FACTOR PLUGGABLE
ZDC	Z-DIRECTED COMPONENT
ESL	EQUIVALENT SERIES INDUCTANCE
ESR	EQUIVALENT SERIES RESISTANCE
SEM	SCANNING ELECTRON MICROSCOPE
TDR	TIME DOMAIN REFLECTOMETER
CST	COMPUTER SIMULATION TECHNOLOGY
SMT	SURFACE MOUNTED TECHNOLOGY
PDN	POWER DISTRIBUTION NETWORK
IC	INTEGRATED CIRCUIT
BGA	BALL GRID ARRAY
PPP	PLANE PAIR PEEC
PEEC	PARTIAL ELEMENT EQUIVALENT CIRCUIT

1. INTRODUCTION

It is acclaimed that the data centers are backbone of the networking industry. As the data rates are extending in to 56+ Gbps and beyond, handling the signal integrity of such long/medium reach channels is critical to the successful system design. However, meeting the target requirements at such high speeds with lossy channels can become a daunting challenge to the design engineers. To address this issue, a novel technology known as Flyover QSFP is introduced, wherein the low loss twin-ax cables "fly over" the PCB in contrast to the typical stripline traces (and hence "lossy") from one QSFP connector to the other in the system. The signal integrity benefits of the FQSFP technology compared to the legacy QSFP are detailed in section 2. The primary objective of this research is to evaluate the EMI performance of such novel FQSFP connector. Then, to mimic the realistic implementation of the FQSFP connector, a cage has been integrated and the EMI profile is evaluated. The research documented in sections 2 and 3 is published for DesignCon conference in the year 2016, bearing the title "Design of Flyover QSFP for 56 Gbps applications" [1].

It is a well-known practice in the industry to place the decoupling capacitors as close as possible to the IC in order to keep the inductance of the current path loop from capacitor to the IC small. However, as the switching speeds of the ICs and the component density on the PCB real estate undergo drastic increase, it is challenging to place the capacitors closer to the IC in order to meet the desired target impedance. To address this issue, a novel capacitor known as Z-Directed Component (ZDC) has been introduced which is targeted to be placed under the BGA of the IC.

The research entails studying two aspects of the system level modelling of the ZDC. Firstly, the interaction of the planes with the ZDC is studied and the impedance profile is compared to that of a regular decoupling capacitor for thick and thinner separation of PWR/GND plane pairs. The latter portion of the study is related to the implementation of the ZDC on a PCB design by replacing some of the local decoupling capacitors with ZDC and comparing their performances. The essence of the study is emphasizing the advantage in reducing the high frequency inductance at the system level PDN using ZDC. As a final note, the ZDC can provide a better, promising decoupling solution in near future as the charge can be delivered promptly to the IC with charge reservoir (i.e., ZDC in our case) being embedded right underneath the IC pin, thereby boosting the performance of the system up to very high frequencies.

2. FLYOVER QUAD-FORM FACTOR PLUGGABLE (FQSFP) TECHNOLOGY

IEEE 802.3bs and IEEE 802.3cd are emerging Ethernet standards which aim to increase data transfer rates in networking equipment from 28 Gbps to 56Gbps [2]. This increase in data rate stresses traditional interconnects approaches such as Quad Small Form Factor Pluggable (QSFP). A lower loss interconnects solution has been developed which connects the front panel pluggable module to the switch ASIC using twinax cable. This category of cabled interconnect is referred to as “Flyover” as the high-speed signals “fly over” the lossy PCB traces. Figure 2.1 illustrates the system level implementation of the FQSFP technology.

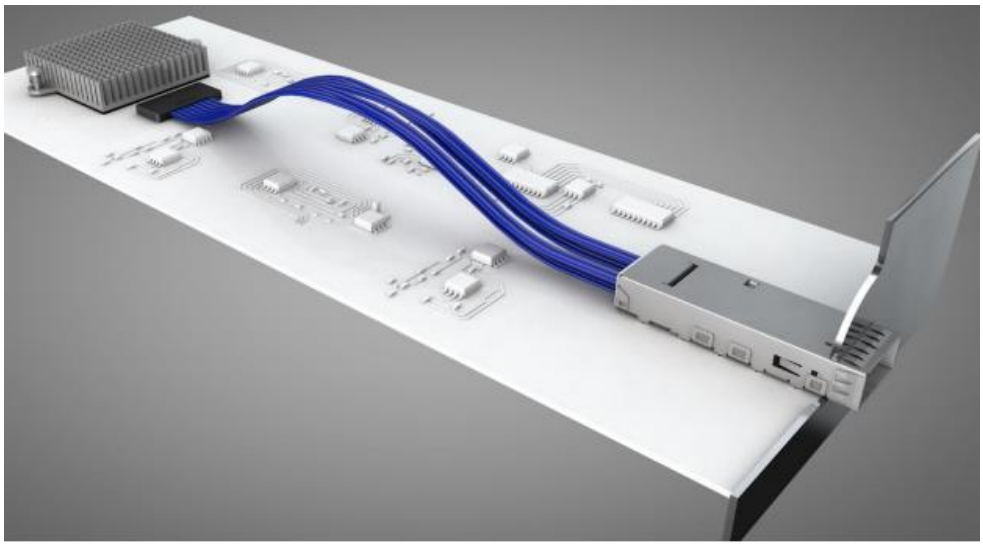


Figure 2.1 Implementation of Flyover QSFP on a Printed Circuit Board

The architecture differences and signal integrity performance comparison between legacy QSFP and FQSFP technologies is discussed briefly in Section 2.1.

2.1. ARCHITECTURE COMPARISON OF QSFP AND FQSFP TECHNOLOGIES

Figure 2.2 highlights the topology differences between the standard legacy QSFP and novel Flyover QSFP (FQSP) technologies. The key to the lower loss FQSFP solution is the use of twinax cable which has a Teflon dielectric.

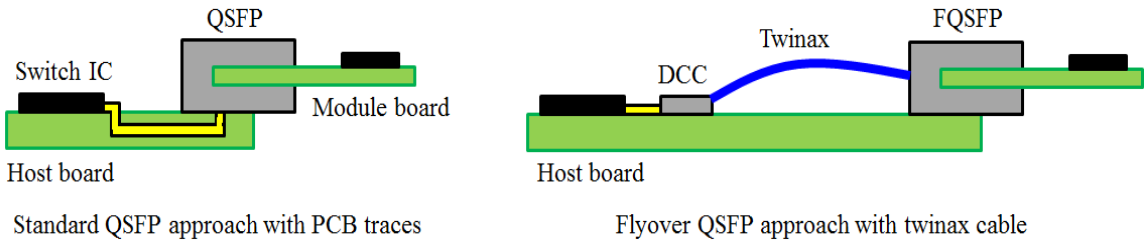


Figure 2.2 Comparison of Standard QSFP and Flyover QSFP (FQSFP) Approaches

Figure 2.3 shows a comparison of the insertion loss characteristics of twinax cable vs PCB traces on a Megtron6 PCB. Around 40 GHz, the insertion loss of 12-inch twinax cable in the FQSFP approach is 7 dB lower than typical 12 inch PCB trace in the low loss dielectric substrate in the standard QSFP approach. This lower loss FQSFP solution gives great advantages in the system design by enabling us to remotely locate the receiver besides much more system design flexibility. It enables us to have the higher density port configuration (multiple stack), reduction of power consumptions by the elimination of re-timers, reduction of thermal dissipation by freeing designers to place ICs in preferred locations, reduction of PCB material costs due to lower layer counts and increased material options without compromising the backward-compatibility to standard QSFP.

2.2. SIGNAL INTEGRITY BENEFITS OF FQSFP OVER LEGACY QSFP

The signal integrity aspects of this design are well predicted using modern full wave simulation tools. Product tradeoffs between SI performance, manufacturing approach and cost are routine in the product development process. What is novel and somewhat unique is the EMI aspect which is the subject of this research. Typical applications in networking equipment may have 10's -100's of QSFP modules which demand a careful engineering solution, assuming the combined emissions from many FQSFP assemblies. We also study the EMI impact of integrating the cage on to the FQSFP connector from both measurements and simulation standpoints and compare the performance to that of the connector itself. However, determining the potential causes of EMI for this connector technology and their mitigation techniques remain beyond the scope of this thesis.

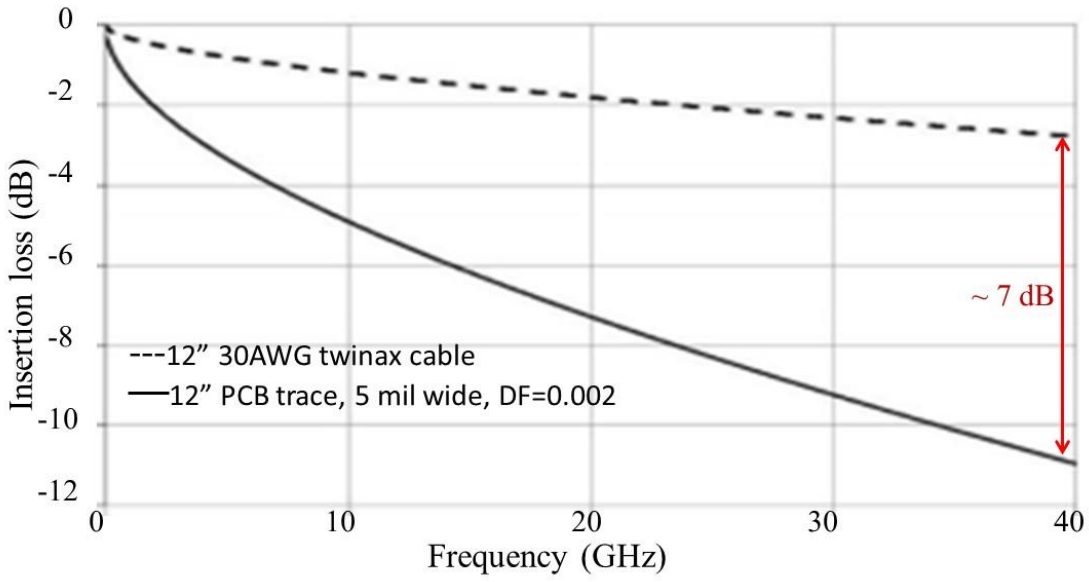


Figure 2.3 Insertion Loss Comparison of Twin ax Cable Compared to Copper Traces on Megtron 6 PCB

3. EMI CHARACTERIZATION OF FLYOVER QSFP (FQSFP)

High-speed channel interconnect includes several impedance discontinuities at their connector and assemblies which act as an effective source of electromagnetic (EM) radiation [3]. Keeping the radiation below FCC regulation with those discontinuities is one of the most critical parts of high-speed channel system design. FQSFP system also has several discontinuities at the interface between a module board and FQSFP connector at host board, FQSFP connector to twinax cable, and twinax cable to DCC connector right before IC. The EMI from those sources should be properly investigated and improved to meet the regulation before we complete the design cycle. In this section, the test vehicle and a measurement correlated simulation model of FQSFP for EMI characterization of FQSFP is discussed. Once the model achieves the correlation with measurement, it enables us to perform simulation based design iterations, which is much more cost and time effective than trial and error on actual test vehicles, for further enhancement of EMI performance.

3.1. DESIGN OF TEST VEHICLE AND SIGNAL INTEGRITY EVALUATION

To accommodate the measurements, a 4-layer PCB test vehicle with FQSFP approach is designed. The test vehicle is fabricated and also modeled in CST microwave studio. Figure 3.1 shows the fabricated 4-layer PCB test vehicle with FQSFP connector and 6-inch long twinax cable. The overall objective of the research is categorized to get a measurement correlated simulation model into two parts, for TDR and for total radiated power (TRP). By doing the correlation work for TDR first, we could quickly screen out

any errors in the signal path transition of the simulation model. These errors are generally difficult to troubleshoot directly from TRP simulation and measurement. Therefore, doing TDR first reduces our design iteration to achieve the measurement correlated simulation model for our EMI characterization of FQSFP.

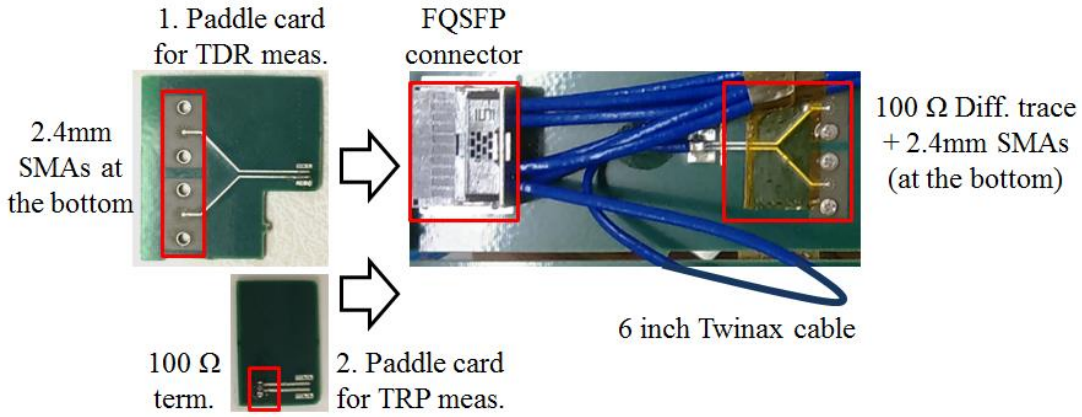


Figure 3.1 Fabricated 4-Layer PCB Test Vehicle with FQSFP Connector and Two Pluggable Paddle Cards (1, 2) are Shown

3.1.1. Overview of Full Wave 3D Simulation Model. The simulation model of the same test vehicle in CST microwave studio as shown in Figure 3.2. The model includes from SMA launch ports in the paddle card to the middle of twinax cable after FQSFP to reduce a simulation time. Therefore, TDR comparison with measurement is only valid till the end of twinax cable. The material properties used are based upon the suggestions from PCB and FQSFP vendors.

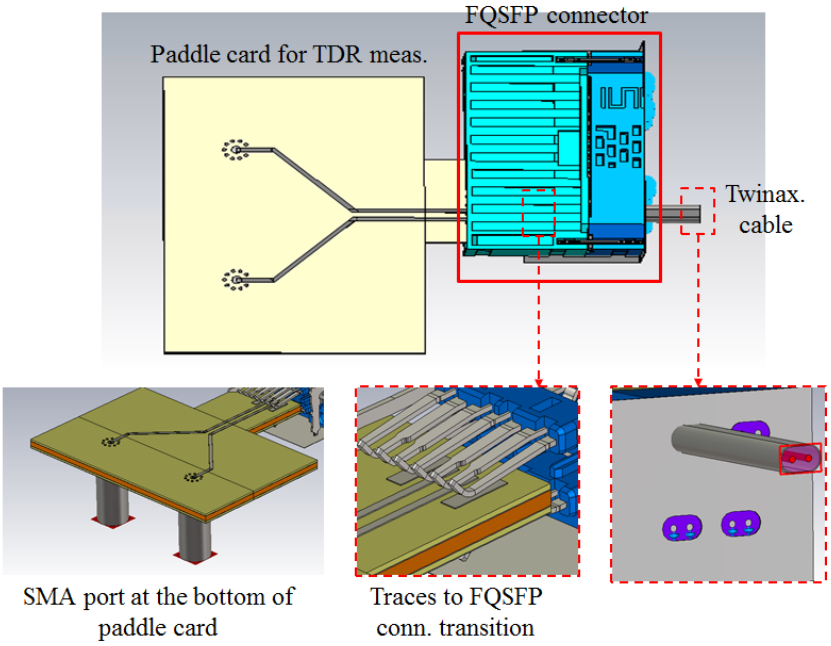
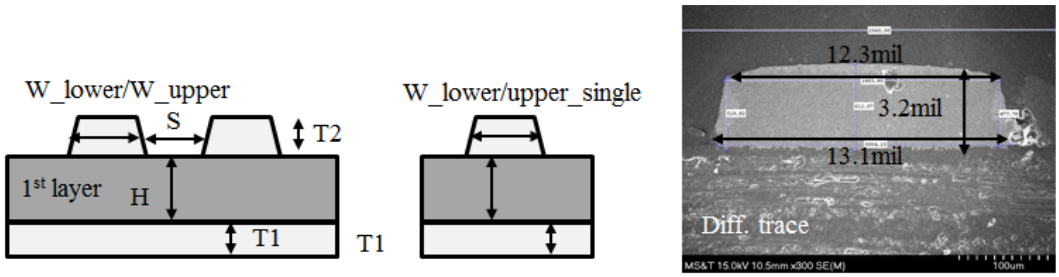


Figure 3.2 Full Wave 3D Simulation Model in CST

Two different type of paddle card 1 and 2 were designed for TDR measurement and TRP measurement, respectively as shown in Figure 3.1. These paddle cards play an important role of the module board in our test vehicle for simplicity purposes. One paddle card (#1) which has SMA ports is designed for TDR and the paddle card (#2) for TRP has 100-ohm termination resistor between differential trace pair. These paddle cards are plugged into FQSFP connector and terminate differential signal pins in FQSFP connector. This channel is connected to 2.4 mm SMA ports at the other end of the host board via 6-inch twinax cable. The simulation time of the model with CST took 3 to 5 hours depending on the resources of simulation machines. The simulation model and test vehicle for TRP will be explained in more detail later in Section-3.2.

3.1.2. Simulation Model Updates from SEM Cross-Sectional Analysis. The PCB traces in the test vehicle were originally designed to have 50 ohms single and 100 ohms differential characteristic impedance. However, the measured impedances at the single and differential traces in Figure 3.2 were 5~7 ohm lower than the design target value (100 ohms). After SEM cross-section analysis on the fabricated test vehicle, we found that the lower impedance was due to the thicker metal traces in the fabricated test vehicle than that of targeted in the design. Figure 3.3 summarizes the result of SEM cross-section analysis. The thickness of the trace was measured as 3.2 mil, which is more than two times larger than targeted value (1.4-mil), while space, width of traces vary within the range of 10% from the targeted value. The measured dimensions of traces are updated in the CST model before S-parameter simulations and then the TDR profile is obtained using FEMAS tool developed by EMC laboratory, Missouri S&T.



	W_lower	W_upper	S	H	T1	T2	W_lower _single	W_upper _single
Designed dimensions	12.5 mil	-	18	7.6	1.2	1.4	13.6	-
Fabricated dimensions	13.1	12.3	20	7.5	1.3	3.2	14.2	13.8

Figure 3.3 Cross Section of the Fabricated Test Vehicle with SEM Analysis

3.1.3. TDR Measurements and Simulation Correlation. Now that simulation model is updated with dimensions recorded from SEM analysis of the test vehicle, we proceed for performing measurements on the test vehicle to corroborate with measurements. The Section 3.1.3 discusses the measurement setup and correlation with simulations.

3.1.3.1. TDR measurement setup. To measure TDR profile of the test vehicle, we used a 50 GHz 4 ports VNA as shown in Figure 3.4. First, we measured 0.01~50 GHz 4 port S-parameter between two SMA ports at the paddle card and the other two SMA ports at the host board. Then, it was converted to Differential TDR profile seen at SMA ports of the paddle card, using FEMAS tool.

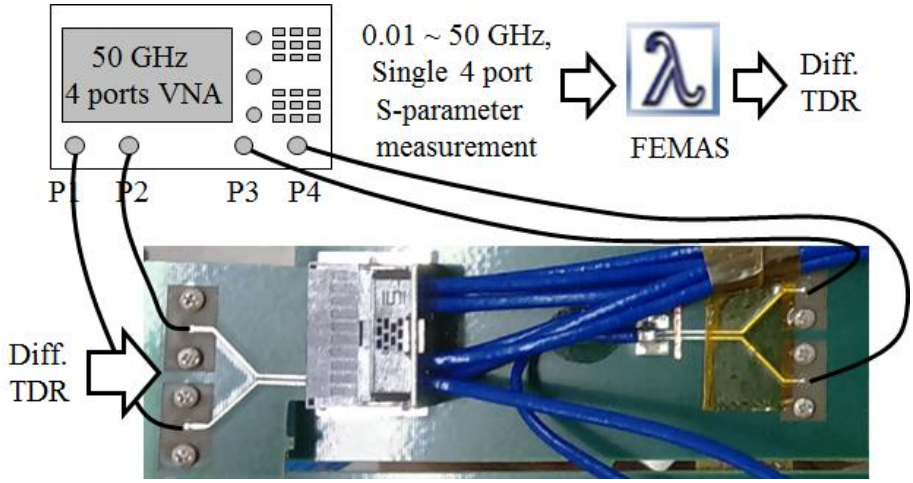


Figure 3.4 TDR Measurement Setup

3.1.3.2. Correlation results and observations. The comparison of TDR in the Figure 3.5 shows good correlation between measurement and simulation. Since the simulation model only models from SMA launch ports in the paddle card to the middle of twinax cable after FQSFP, TDR profile within this range is compared with the

measurement. The differential impedance of the single/differential traces for TDR measurement is lower than 100 ohms because of the fabrication variation in trace thickness as explained earlier in section 3.1.2. By updating the dimensions of traces from SEM analysis to CST model, we achieved the good correlation for this part of the TDR profile. A big capacitive dip at the interface of FQSFP connector and the paddle card is caused by an excessive capacitance due to coupling between the pin structure of FQSFP and PCB traces at the transition. Having a void at a ground plane under the differential traces at the transition point can help to reduce the capacitive dip.

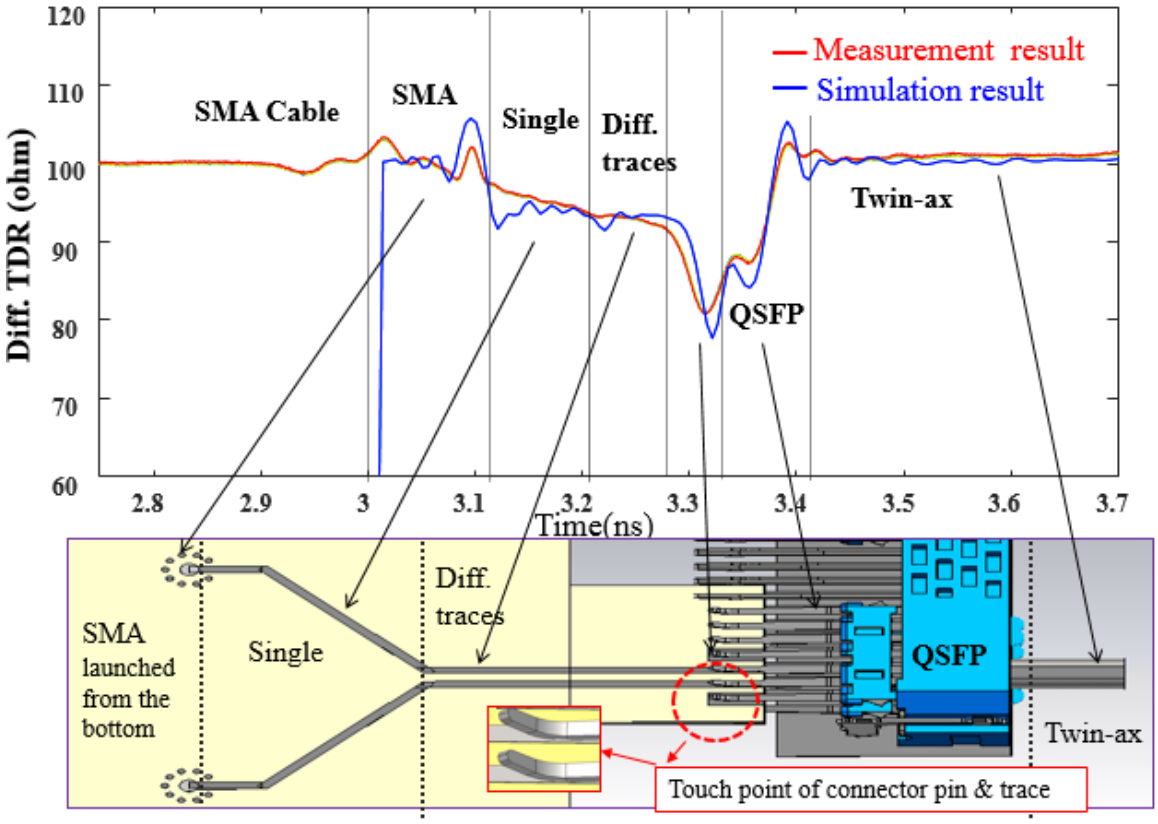


Figure 3.5 Comparison of TDR Measurement and Simulation Results

3.1.4. Redesign Considerations of the Test Vehicle. In order to proceed for EMI investigation, the SI profile of the current test vehicle has to be improved as highlighted in the below curve.

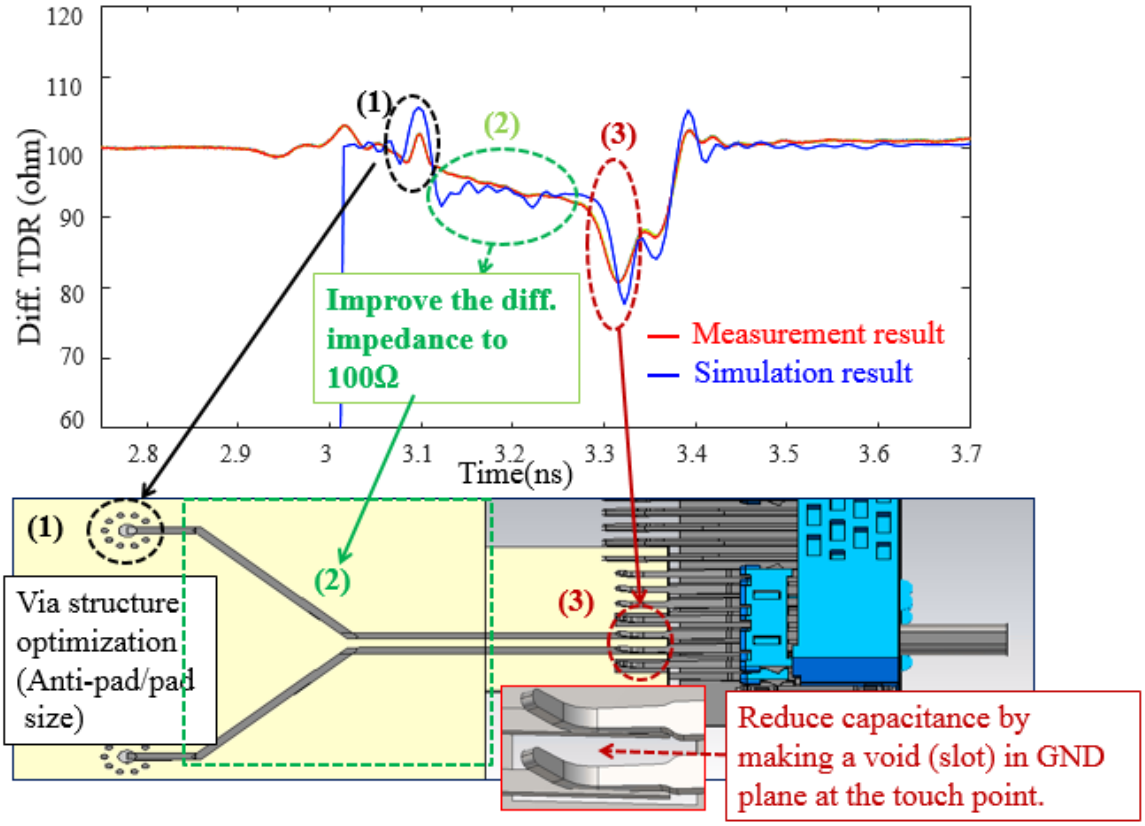


Figure 3.6 Critical Areas Requiring Improvements

For this purpose, redesign considerations have been carried out which focused on three main segments of the TDR curve as shown in Figure 3.6.

(i) The inductive bump at the SMA-pad transition can be optimized by increasing the capacitance through reducing the size of the anti-pad.

(ii) The impedance of the single and differential traces were optimized in the simulation model with the help of calculations from 2D-cross sectional analysis tool in FEMAS.

(iii) The capacitive dip at the touch point is improved through making a rectangular slot in the GND plane.

The corrections targeted in the previous test board (test vehicle-1) were implemented in the new test vehicle (test vehicle-2) and the impedance profiles of measurement and simulation are compared as shown in Figure 3.7.

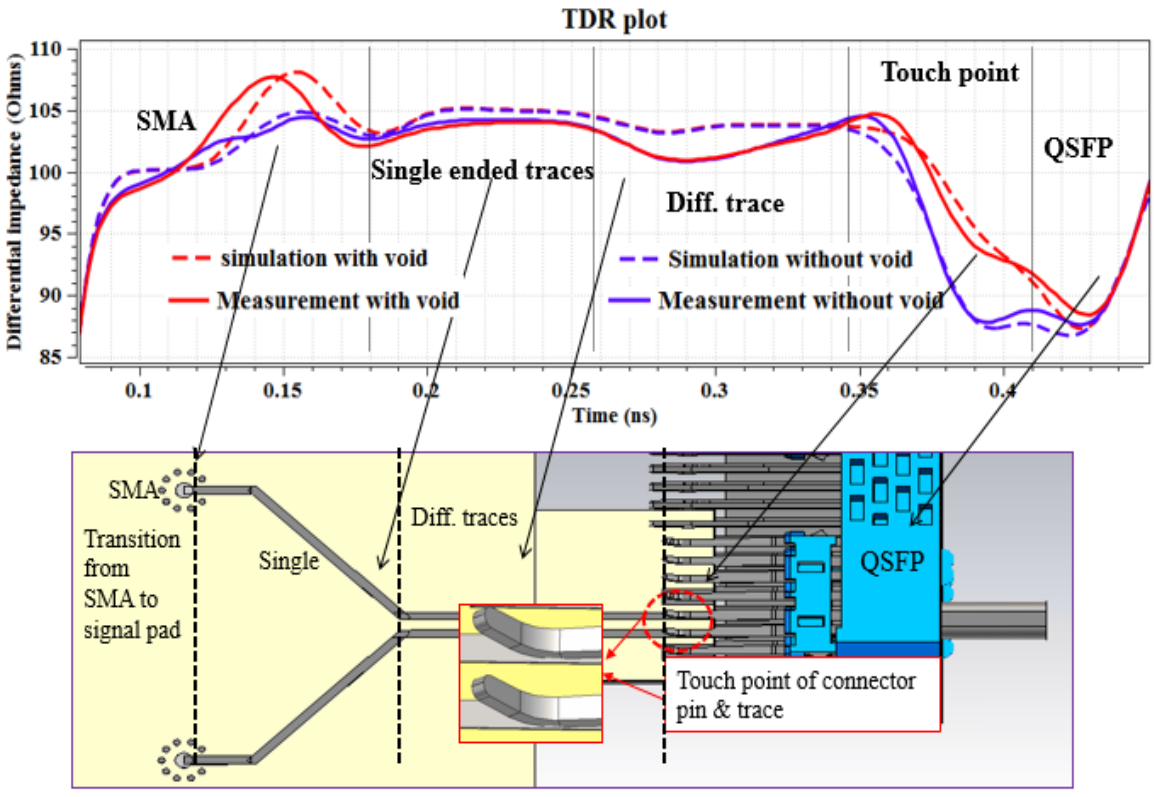


Figure 3.7 Correlation Results of the Redesigned Test Vehicle

Due to manufacturing tolerances, the differential impedance after fabrication was found to be ~103-104 ohms. Similar to the previous case, microscopy was performed and the obtained dimensions were updated in the simulation model and correlation was better than the previous test vehicle. In particular, the extra capacitance at the touch point of connector pin to trace (highlighted in the Figure 3.4) is improved by making a slot underneath the touch point. Thus we see ~5-7 ohms improvement. Now, after such better correlation (<2-3 ohm deviation), we now proceed for EMI investigation, discussed in next section.

3.2. EMI INVESTIGATION OF FLYOVER QSFP (FQSFP)

While SI aspects of the Flyover technology are appealing, the EMI aspects are yet unknown and are to be investigated. The high level system implementation is shown in Figure 3.8. The ultimate goal is to provide a solution for this technology to ensure that the product meets regulatory requirements (Class B).

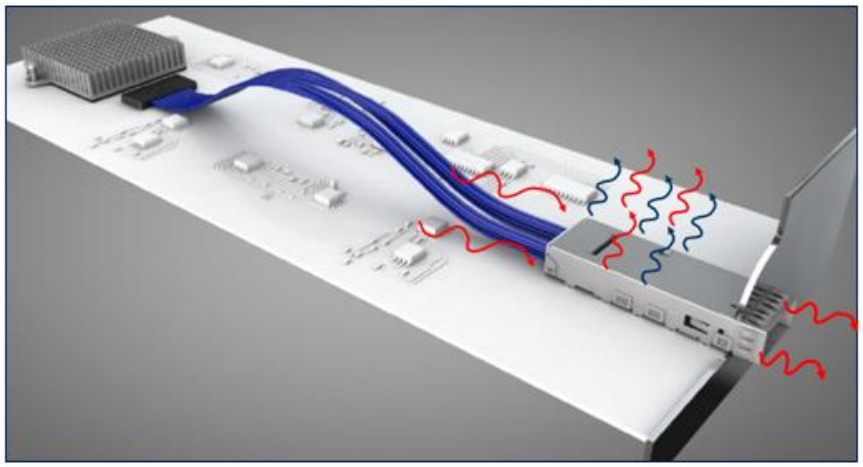


Figure 3.8 High Level Potential EMI Behavior of the Flyover QSFP

3.2.1. Overview of Simulation Model. Once we achieved the measurement correlation for TDR in the previous step, our next step is the correlation work for TRP from the FQSFP connector, which is an initial step to characterize the EMI of whole FQSFP system. To begin with, TRP was investigated from the FQSFP connector, targeting a favorable correlation (~3-5 dB) between the measurements and simulations for both differential and common mode excitations. The simulations were carried out in CST microwave studio. The overview of the simulation model is shown in Figure 3.9.

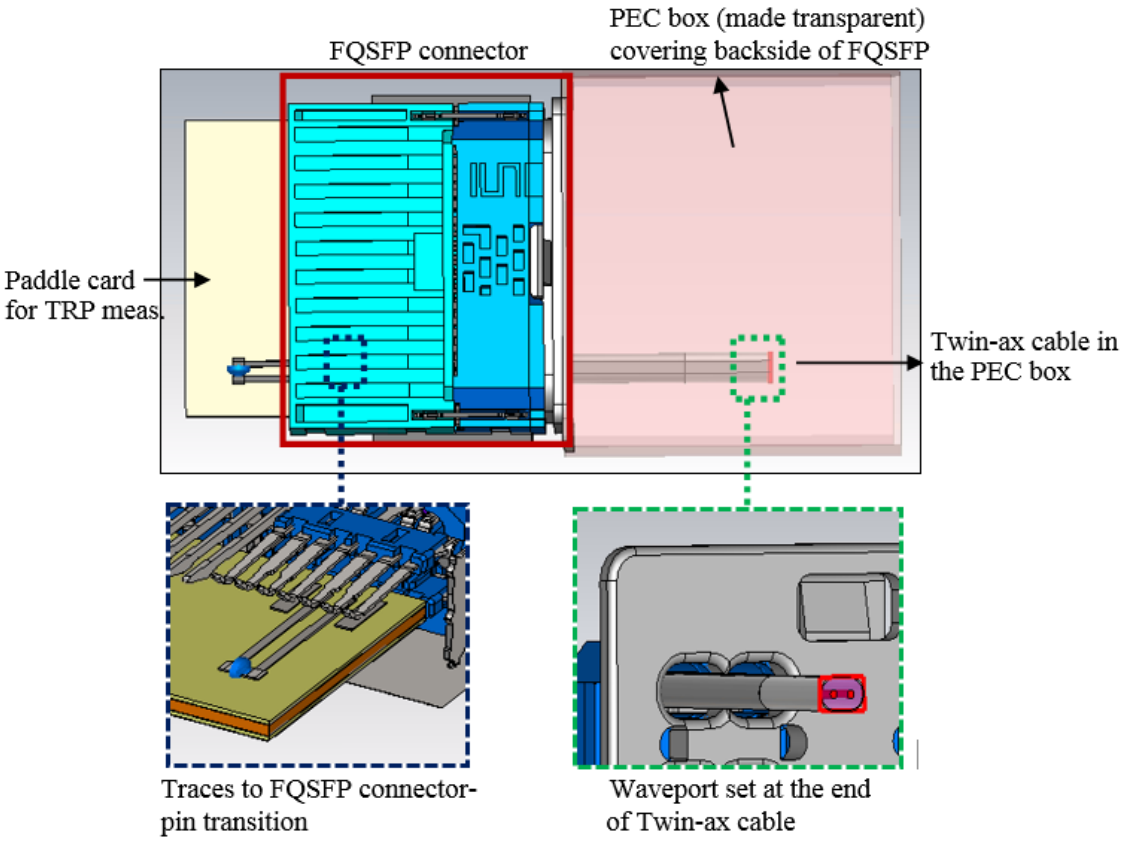


Figure 3.9 CST Simulation Model for TRP

A paddle card plugged into FQSFP is terminated in 100 Ω differential fashion for the differential mode as shown in Figure 3.1 and two-50 Ω single ended fashion for the

common mode. Such termination for common mode was to terminate the traces with defined common mode impedance.

3.2.2. Overview of the TRP Measurement Setup. Besides the simulations, the TRP measurements were carried out up to 18 GHz in a stirred-mode reverberation chamber as setup schematic is depicted in Figure 3.10. The well-known TRP substitution method [3] was used to obtain TRP values.

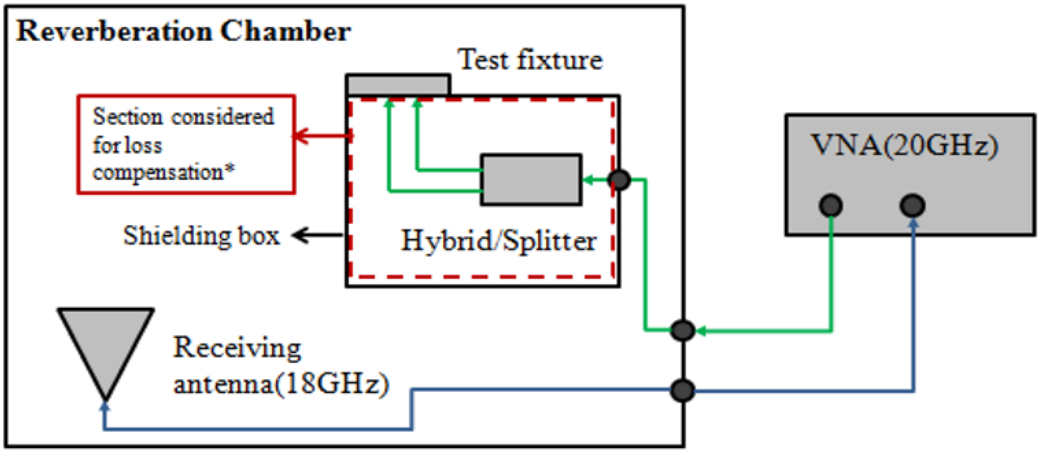


Figure 3.10 TRP Measurement Setup

The receiving antenna limits the frequency band for TRP measurement to be 750 MHz to 18 GHz. A VNA (20 GHz) along with a balun (for differential mode) and splitter (for common mode) was used for the excitation of the test vehicle. In the simulation model, 0.5 W power is directly excited at end of the twinax cable. But in the measurement setup, there is an additional loss incurred due to the SMA cables and balun/splitter, in the highlighted red box in Figure 3.10. To account for these, the insertion loss of the cables and that of balun/splitter (~ 5.5 – 7.5 dB across the frequency range) is compensated on the measured TRP for the comparison with simulated TRP.

The actual measurement setup inside the stirred-mode reverberation chamber is shown in Figure 3.11. In the test vehicle, except the FQSFP connector, everything else was shielded with copper tape as implied in Figure 3.12. This was necessary to capture TRP only from the FQSFP connector. To ensure a reliable contact, the edges of each copper tape are soldered together as depicted in right picture of Figure 3.12.

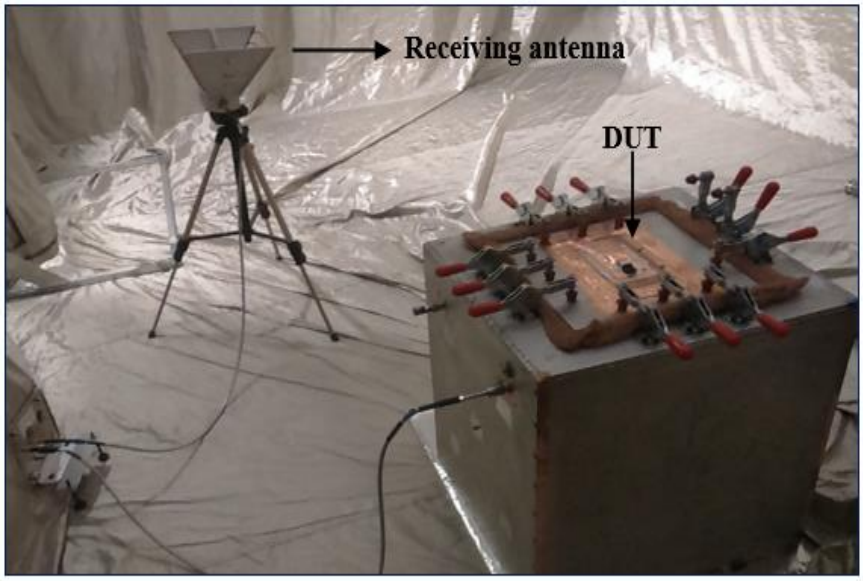


Figure 3.11 Measurement Setup Inside the Reverberation Chamber

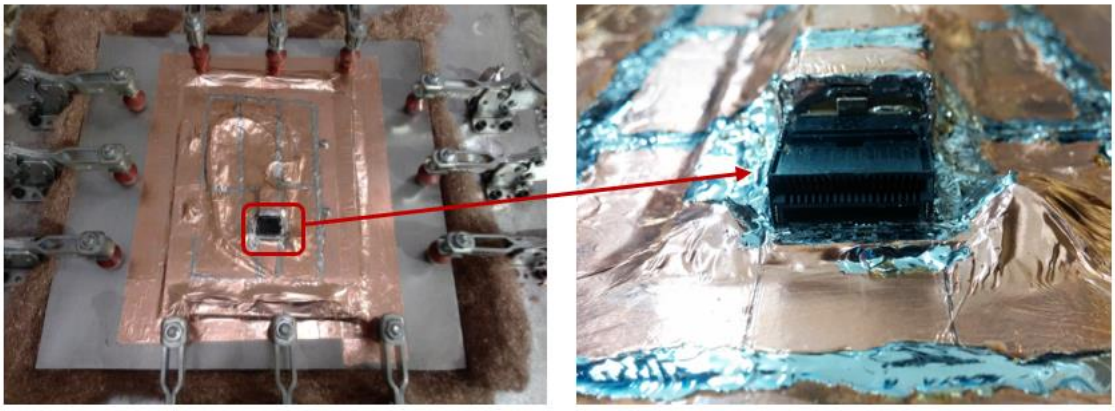


Figure 3.12 A Close View of FQSFP Connector in the Measurement Setup

3.2.3. Correlation Results and Observations. In order to provide the easy eye ball comparison of the total radiated power (TRP) results, the input power to the FQSFP for both the simulated and measured TRP is re-normalized to 1W i.e., 0 dBW. After accounting for all the cables and balun/splitter losses on the measured TRP, the measurement and simulation results are compared in Figure 3.13. A favorable correlation of ~3-5 dB is observed in the case of common mode excitation. However, the differential mode has a significant difference of ~5-10 dB between measurement and simulation. After an investigation, it was found that the cause for such difference is the skew between two imperfect phase matched SMA cables from the balun to FQSFP connector, two green paths in the box in Figure 3.10. Considering the fact of high sensitivity of differential mode in a measurement setup due to phase imbalances along the signal lines, this skew can cause a differential to common mode conversion. Therefore, the measured TRP in differential mode setup is no longer pure differential mode and result in the larger TRP in the measurement than the simulated TRP with the pure differential mode excitation. The skew between the two SMA cables used after balun is measured from the TDR (with 50 GHz BW) and found to be ~7 ps. In order to take account the skew into simulation setup, we set 7 ps skew between two ports in the simulation model, and the port setting was changed from waveguide port to discrete port. After taking account the skew, the new simulated TRP shown in Figure 3.14 is higher than the previous case and hence much reasonable agreement was achieved with the measured TRP. The new correlation between measurement and simulation stands within ~3-5 dB for the differential mode.

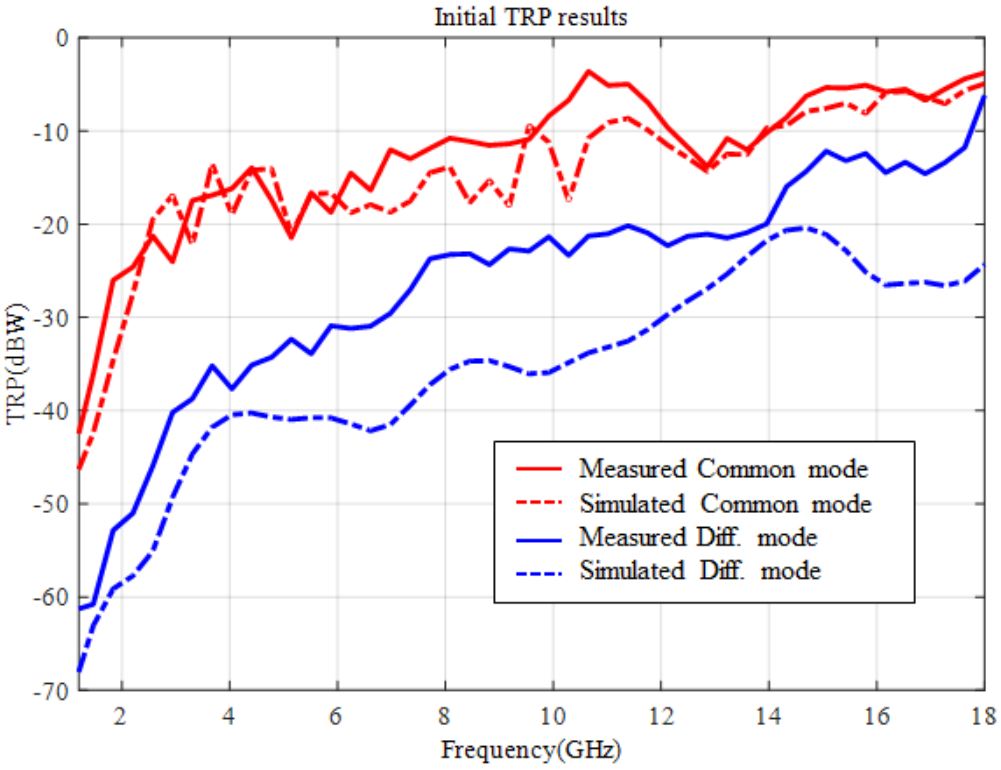


Figure 3.13 Initial TRP Measurement and Simulation Results

As long as reflecting the skew into simulation model give us the good correlation with measured TRP, the simulated TRP without the skew in Figure 3.14 (blue solid curve) gives us an idea to predict a measured TRP with pure differential mode excitation. This amount of favorable correlation for both TDR and TRP profiles of the FQSFP proves that the model is ready to roll for the further simulation based enhancement of EMI design. To summarize the research thus far, the Flyover QSFP approach for 56+ Gbps application is introduced and compared with standard QSFP approach in terms of the insertion loss. Twin ax cables in FQSFP offer about 7 dB lower insertion loss at 40 GHz for 12-inch path than the PCB traces in standard QSFP approach. Beside of the superior signal integrity performance of FQSFP, we have developed a simulation model of FQSFP to investigate

another important aspect, EMI of FQSFP approach. We built a test vehicle to measure TDR and TRP of FQSFP and got a good correlation between the simulation and the measurements for both TDR and TRP from FQSFP. The TRP from FQSFP without a shielding cage is -8 dBW, -12 dBW at 15 GHz from 1 W input power for common-mode and differential-mode, respectively.

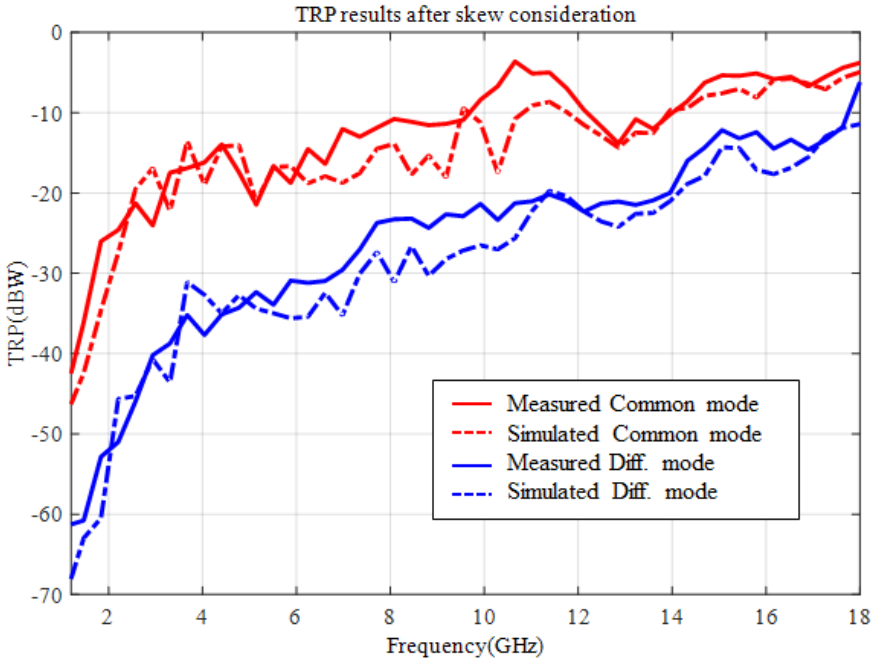


Figure 3.14 TRP Measurement and Simulation Results after Skew Consideration

Once we have achieved the measurement correlated model for simulation, the simulation model facilitates a further simulation based enhancement of EMI design. The ultimate objective is to investigate the EMI for a real case implementation of FQSFP with high-speed data rates such as 28 Gbps, and extended up to 56 Gbps. For this purpose, proceeding to the next level in the EMI design of the FQSFP includes integration of cage,

chassis, and optical module along with the current test vehicle and performing the same set of TRP experiments to corroborate simulations.

3.3. EMI INVESTIGATION OF FLYOVER QSFP ENCLOSED IN A CAGE

The typical FQSFP connectors are enclosed in a cage where an optical module from the other end of the cage is plugged in to the FQSFP connector. The cage is intended to mitigate any electromagnetic radiation escaping the FQSFP connector and the optical module in to the outer world. In this experiment, as a preliminary step, a paddle card is plugged in to the FQSFP connector instead of an optical module.

3.3.1. Overview of the Test Vehicle. Figure 3.15 shows the integration of the cage integrated on to the FQSFP connector.

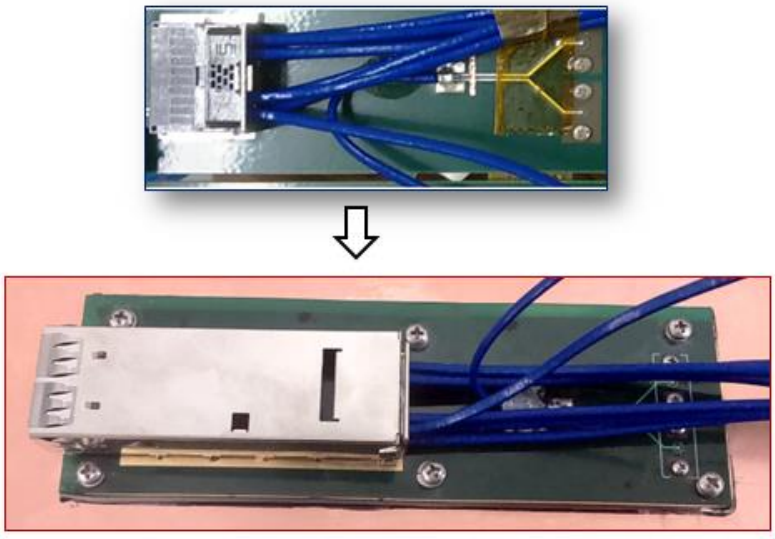


Figure 3.15 Integration of the Cage upon the Flyover QSFP in the Test Vehicle

The pins of the cage are plugged in to the thru holes on the PCB, where the bottom portion of the cage is touching the exposed GND patch on the top of the PCB which ensures the common GND connection between the FQSFP connector, cage and the PCB. The excitation techniques are same as before, using VNA to excite the other end of the twin-ax cable, connected to the SMA and the channel is terminated using the paddle cards which gets plugged in to the FQSFP connector in the cage.

3.3.2. Overview of the Simulation Model. The CST model for the cage with FQSFP connector is except that the cage is connected to the FQSFP connector and the bottom portion of the cage is filled with PEC material to mimic the GND patch on the top layer of the PCB.

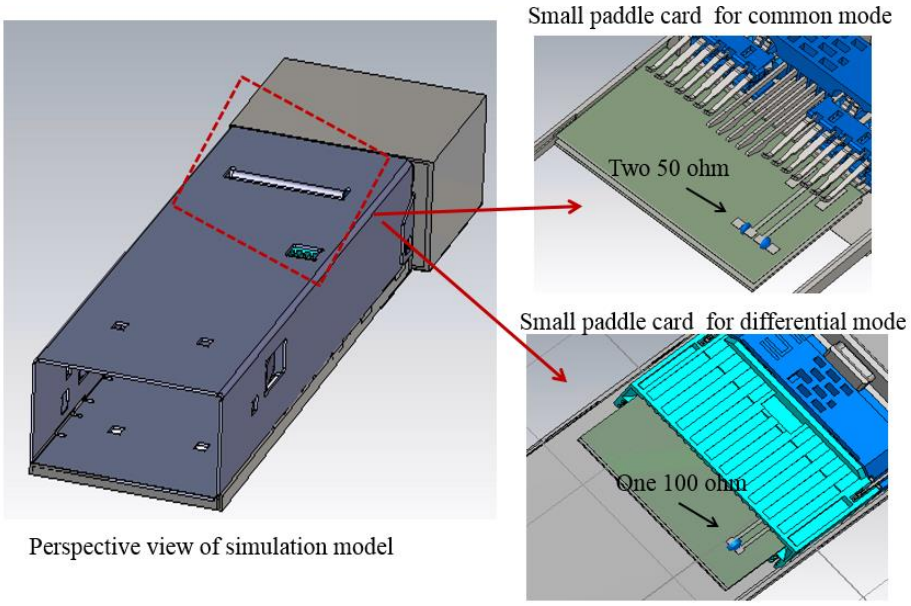


Figure 3.16 CST Simulation Model Integrating the Cage with FQSFP

The paddle cards with well-defined terminations for both differential and common mode excitations are shown in the right section of Figure 3.16.

3.3.3. TRP Measurement Setup after Integration of Cage and FQSFP. As the designed paddle cards are smaller in size compared to the cage, it is difficult for plugging in and out, from the FQSFP connector. Hence, a technique is implemented where a small cut is placed in a plastic to hold the paddle card. The plastic material is held from the other side and paddle card is plugged in to the FQSFP connector in the cage. However, to remove the paddle card from the cage, two holes have been drilled at the bottom of the paddle cards and tied the knot with a thread which accommodates easy plug out facility. Figure 3.17 shows the overview of the technique discussed.

Figure 3.17 Technique Implemented to Plug in/out the Paddle Cards from FQSP in Cage

3.3.4. TRP Measurement Setup. The entire setup and measurement principle of the TRP measurement remains same as discussed in section 3.10, with an exception that the DUT is replaced with test vehicle consisting the FQSFP connector enclosed in a cage. The overview of the test setup is mentioned below in Figure 3.18. Figure 3.19 depicts a

close view of the test vehicle with cage connected to the FQSFP connector. The outer interconnection area of the cage and FQSFP connector is covered with copper tape and soldered to ensure better GND connection of the cage to the back plate of the FQSFP connector and also to avoid any unnecessary escape of the electromagnetic radiation.

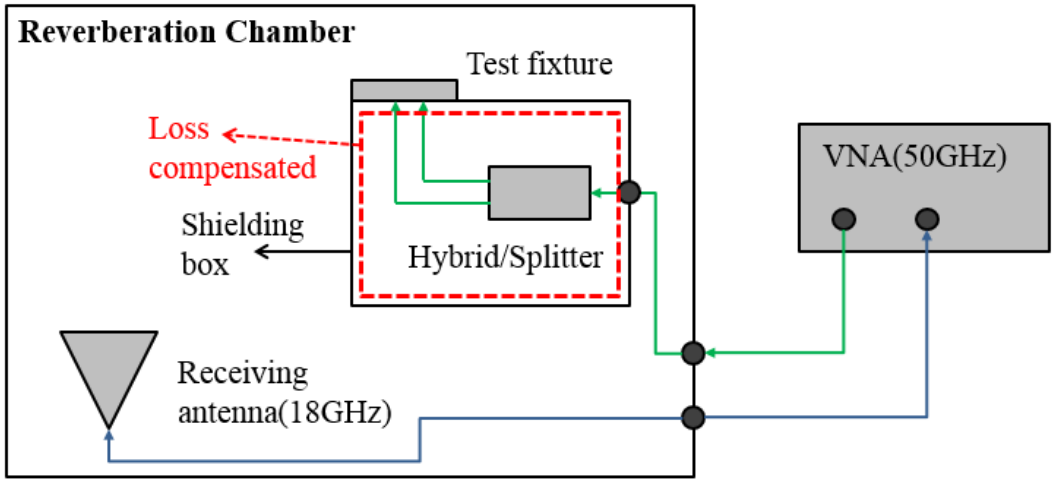


Figure 3.18 TRP Measurement Setup

Figure 3.19 Close View of the Cage Area in the Measurement Setup

3.3.5. Correlation of Simulation and Measurement Results. When compared to the TRP profile of the FQSFP connector alone, integration of the cage shows ~ 10 dB mitigation at 18 GHz, in both differential and common mode excitations. The frequency range is from 750 MHz – 18 GHz, which is the usable frequency band of the horn antenna employed in our test setup.

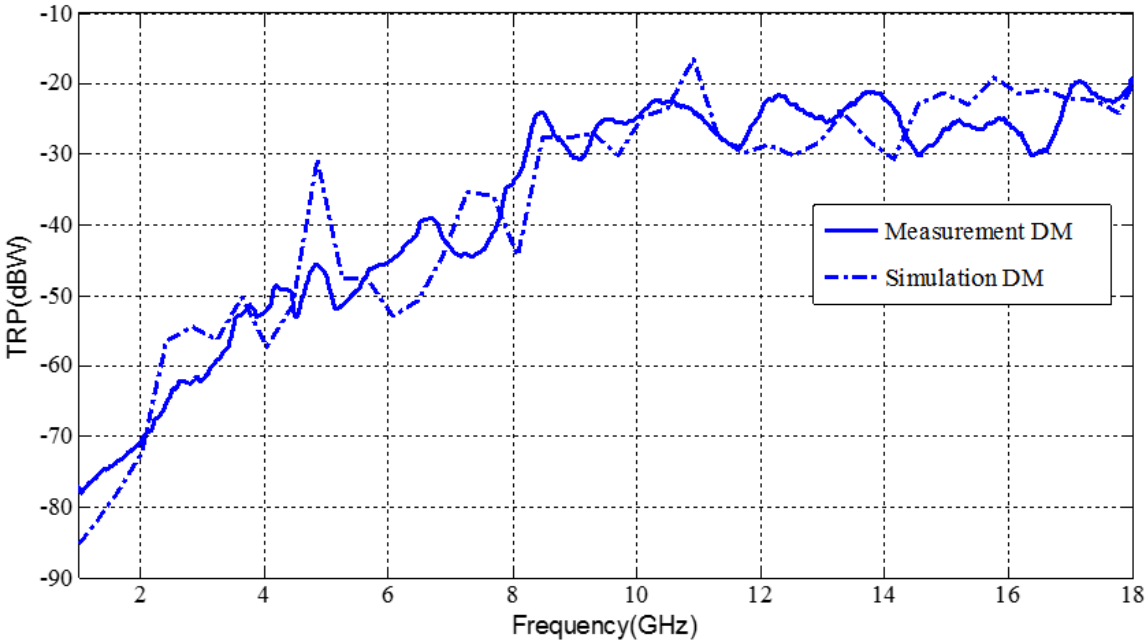


Figure 3.20 Differential Mode Correlation

As shown in Figure 3.20 and Figure 3.21, both the differential and common mode TRP shows favorable correlation between the measurement and simulation. However, the difference in the frequency range of 2-6 GHz, which is more pronounced in common mode than differential excitation has to be further investigated.

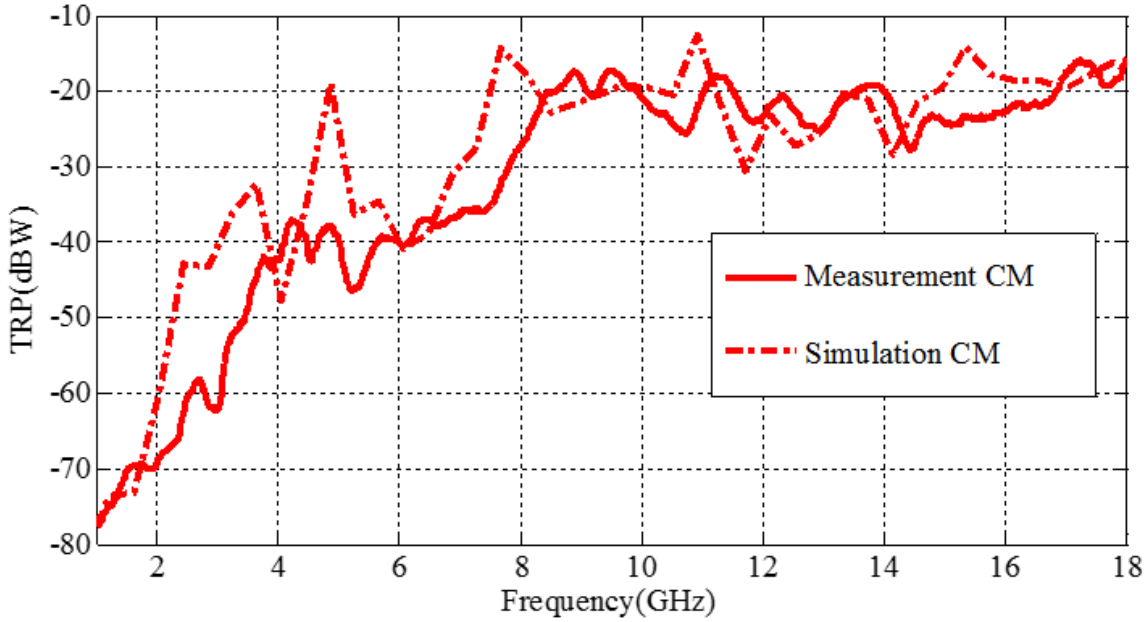


Figure 3.21 Common Mode Correlation

However, the peak at 5 GHz seems to be present both in differential and common mode TRP and will needs to be investigated further.

4. SYSTEM LEVEL MODELLING OF THE Z-DIRECTED COMPONENT (ZDC)

4.1. FUNDAMENTAL BACKGROUND

Any state of art PCB design includes a number of decoupling capacitors placed on the top and bottom layers, as close as possible to the IC. Thus, ensuring proper decoupling is provided within the frequency range of interest such that the target impedance requirements are met and voltage ripple is kept as low as possible to avoid the voltage droop on the power rails. Section 4.1 is a brief excerpt from [4], to provide a proper background for the system level modelling of the ZDC.

Figure 4.1 shows the current paths associated with the PDN in case of a typical SMT decoupling capacitors as a decoupling solution. The current paths include vertical portion, which is from decoupling capacitor to the power net area fill (L_{PCB_decap})_and then an horizontal current path on the power net area fill (L_{PCB_Plane}) and finally the vertical current path from power net area fill to the IC on the top (L_{PCB_IC}).

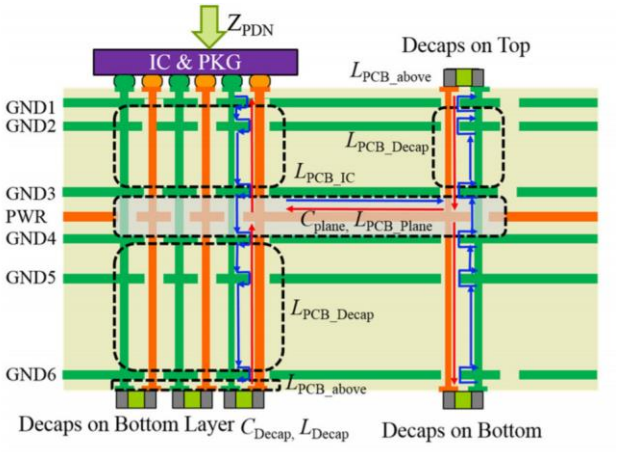


Figure 4.1 Current Path Distribution of a PDN for a Typical SMT Decoupling Capacitor

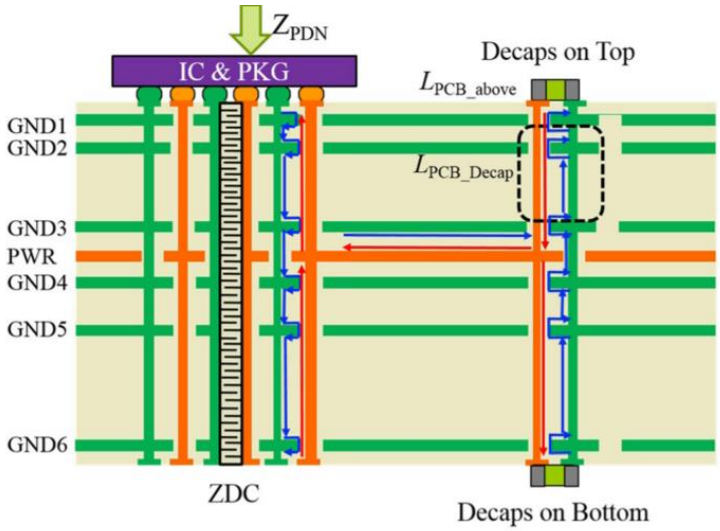


Figure 4.2 Implementation of the ZDC in the PCB

However, Figure 4.2 shows the implementation strategy of the ZDC, where the ZDC capacitor is embedded within the PCB underneath the package ball of the IC, which eliminates the current paths associated with the vertical portions of the L_{PCB_decap} and L_{PCB_IC} and the horizontal portion i.e., L_{PCB_Plane}. The only portion of the inductance would be due to the Equivalent series inductance (ESL) of the ZDC. Thus, ZDC significantly improves the mid-to-high frequency performance of the system as shown in Figure 4.3.

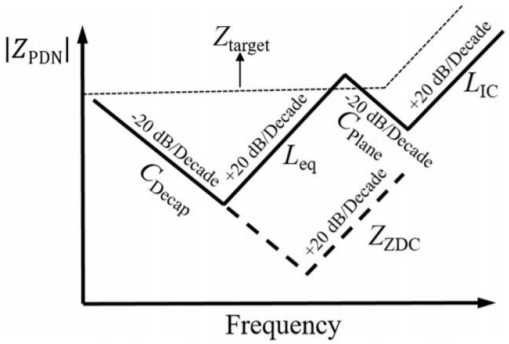


Figure 4.3 Magnitude Approximation of the PDN Looking through IC Package Ball

As mentioned in [4], the published research includes the study of the electromagnetic fields, developing a higher order circuit model of the ZDC and corroboration of the circuit model profile with simulation and measurement. The critical aspect of this theses is an extension of the research on ZDC from component level to the system level implementation.

As discussed earlier in brief, the system level study is carried out in two phases.

(1) ZDC interaction with both widely & narrowly separated PWR/GND planes using full wave 3D simulations and their corresponding impedance profile comparison with that of a typical SMT capacitor.

(2) Implementation of the ZDC in a real world PCB design by replacing some of the local decoupling capacitors with ZDC and comparing the system level solutions using ZDC and SMT capacitors, using a commercial tool.

4.2. ZDC INTERACTION WITH PLANES

Before proceeding to the system level study of ZDC on a real PCB design, the interaction of ZDC with PWR/GND planes is studied and compared to that of a regular 0402 decoupling capacitor using commercial tools.

4.2.1. ZDC in a Widely Separated PWR/GND Pair. The impedance profile of the ZDC when it is embedded under the IC, for a thick PWR/GND separation of 47 mil FR4 is shown in Figure 4.4. The PWR and GND planes connect to the scallops of the ZDC on either side.

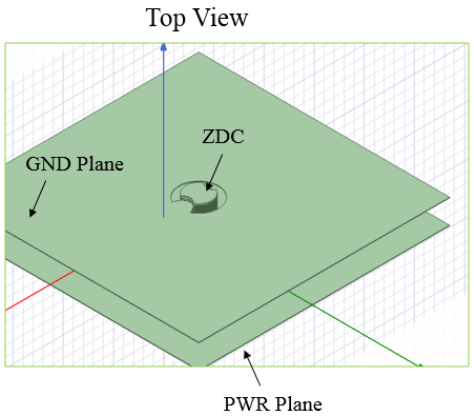


Figure 4.4 ZDC in Thick Dielectric

4.2.2. ZDC Embedded in a Widely Separated Planes Vs. ZDC Itself. Then, the performance of ZDC with planes is compared against the default ZDC simulation model without any planes included. The impedance profiles shown in Figure 4.6 reveal no difference, emphasizing the fact that the planes have negligible effect on the ZDC when it connected to the planes. This is mainly due to the provision of low impedance path within the ZDC through the displacement current between the layers and the ZDC part itself is sufficient for decoupling when placed underneath the IC. In Figure 4.5, the multiple resonances observed after the first self resonance frequency (~30 MHz) are the half wavelength resonances which are due to the open ended transmission line effects of the ZDC. The Q-factor of the resonances is low as both the conductor and dielectric losses are considered in the simulation model.

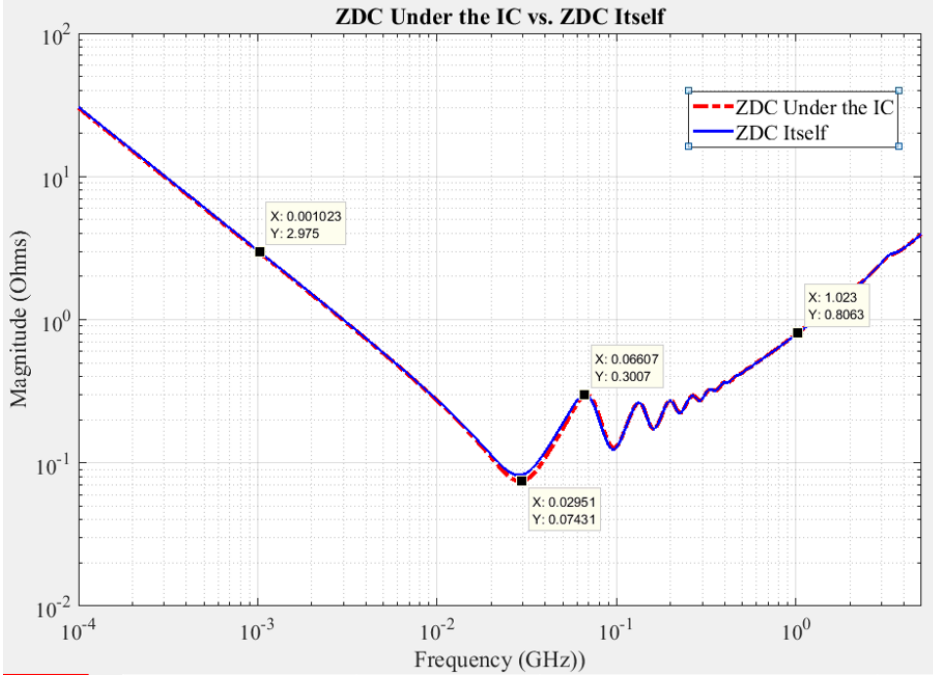


Figure 4.5 Impedance Profile of ZDC in Wide Planes vs. ZDC Itself

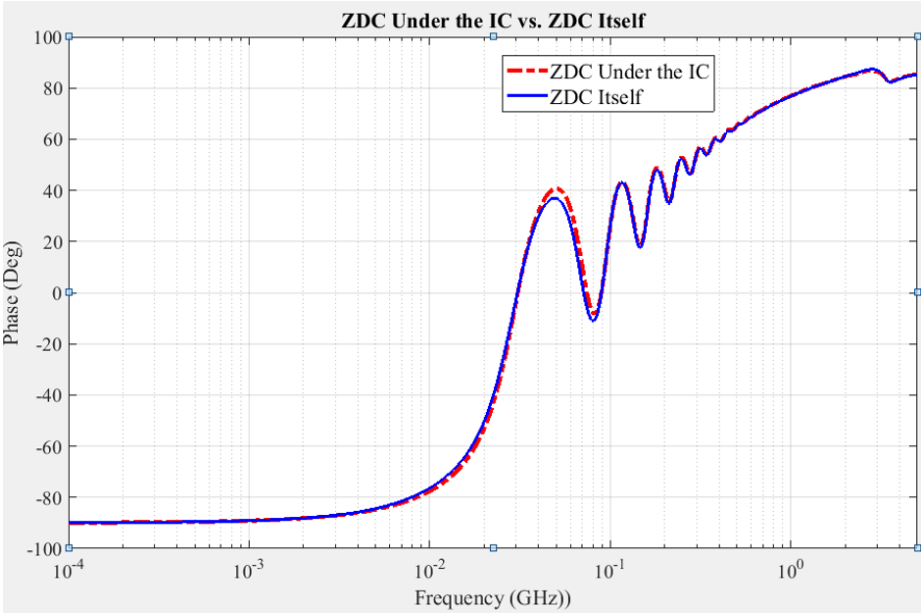


Figure 4.5 Impedance Profile of ZDC in Wide Planes vs. ZDC Itself (Cont'd)

The ESL of the regular 0402 decap is around 0.5nH and the capacitance (C) = 53 nF, which is kept same for both ZDC and 0402. The high frequency inductance in case of the ZDC is purely due the ESL of the capacitor which is around 0.130 nH. However the inductance in case of the regular decoupling capacitor is around 3.10 nH, dominated by the horizontal portion of the current paths, which is the plane inductance due to 47 mil spacing of PWR/GND planes.

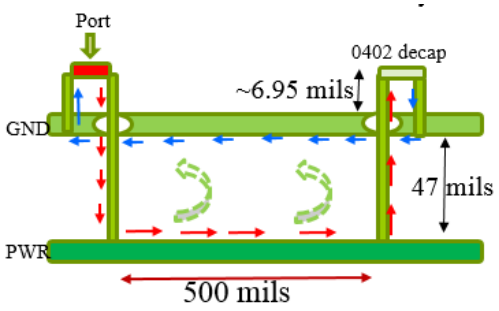


Figure 4.6 Regular Decap Placed 500 mils Away from the IC

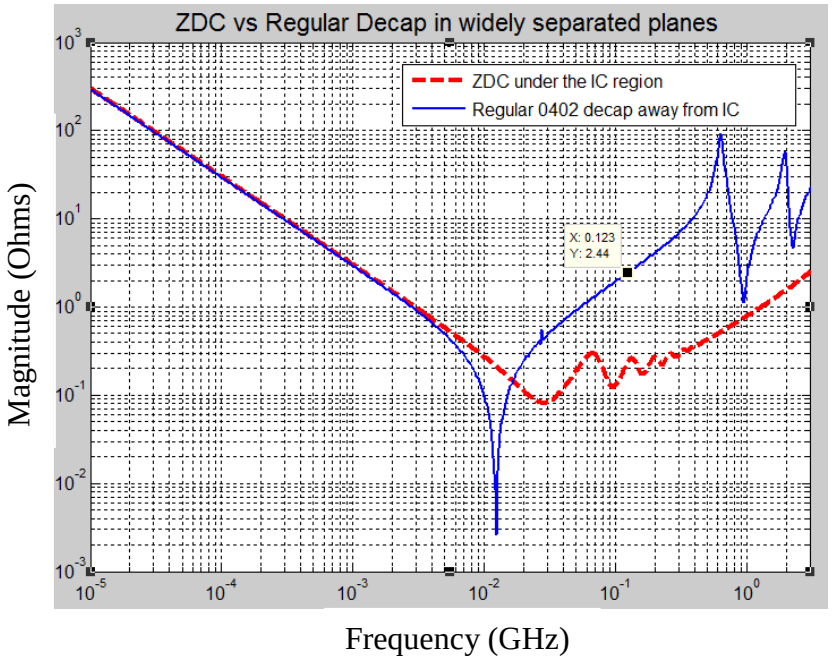


Figure 4.7 ZDC vs. Regular Decap Compared in a Widely Separated PWR/GND Planes

Table 4.1 ZDC vs Regular Decap Compared in a Widely Separated PWR/GND Planes

Simulation model	Capacitance	Inductance
ZDC underneath the IC	~53 nF	~0.130 nH
Regular SMT decap 500mils away from the IC	~53 nF	~3.10 nH

As shown in Figure 4.7 and Table 4.1, utilizing the ZDC as a decoupling solution is promising with 95% better performance at higher frequencies, when compared to the typical placement of the decoupling capacitors for a widely separated PWR/GND plane pairs.

4.2.3. ZDC Embedded in Multiple, Narrow Separated PWR/GND Pairs. It is already shown that the contribution of planes is negligible when using ZDC, proceeding to the next level of study entails performance comparison of the ZDC and regular SMT capacitor, for multiple, narrowly spaced layers.

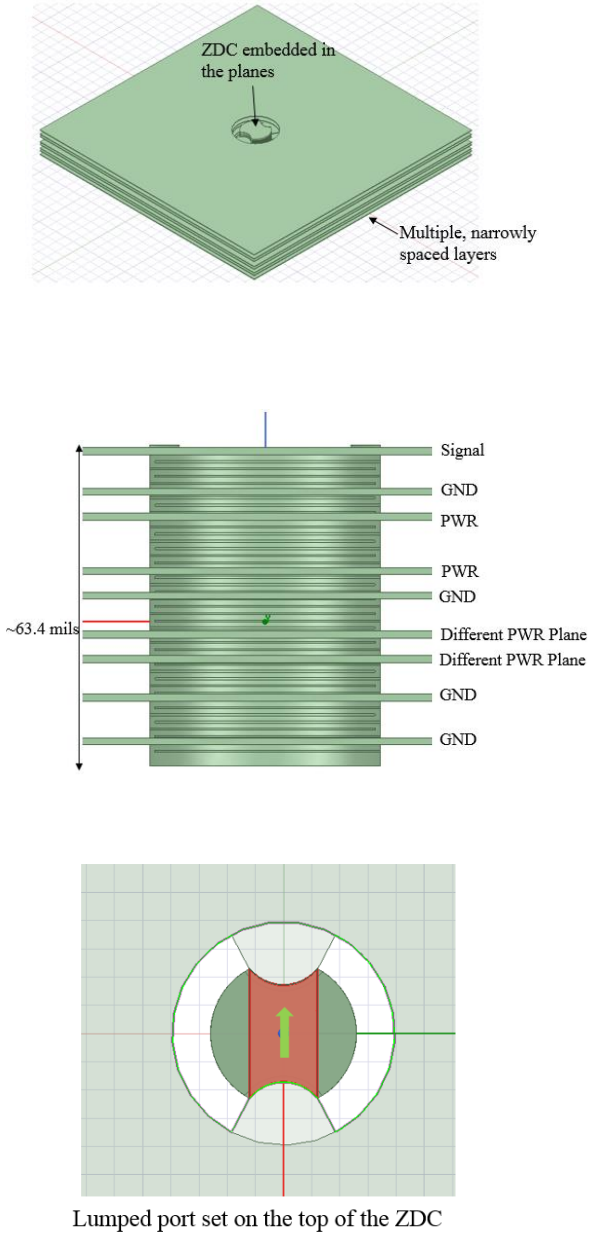


Figure 4.8 ZDC in Multiple, Narrow Planes

The geometrical and material parameters of the ZDC are same as afore mentioned widely separated plane pair case with an exception of placing the ZDC in multiple, narrow layers. The stack up of the planes is leveraged from a real PCB design as shown in Figures 4.8 (b) and 4.9.

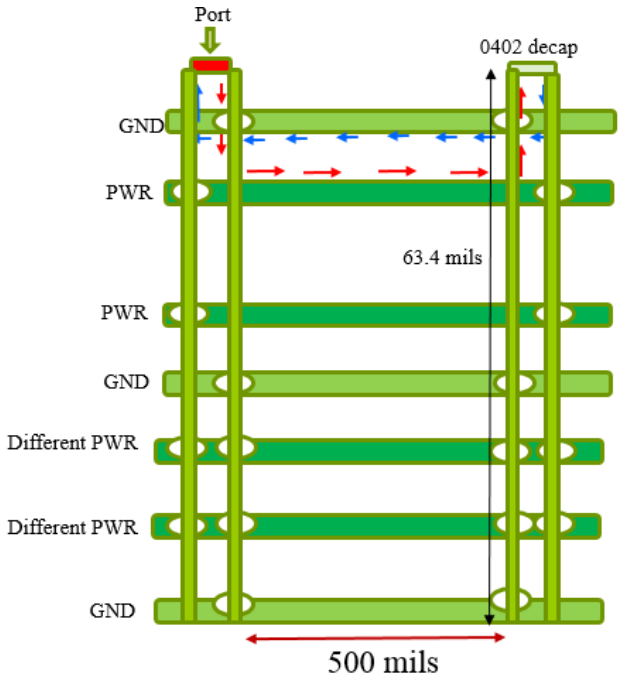


Figure 4.9 Regular Decap 500 mils Away from the Port for Narrow, Multiple Layers

As shown in Figure 4.10 and Table 4.2, utilizing the ZDC as a decoupling solution is promising with 89% better performance at higher frequencies, when compared to the typical placement of the decoupling capacitors for a narrowly separated PWR/GND plane pairs. Since the PWR/GND planes are placed closer to the top in the stackup, the vertical inductances are small. Also, for a thin spacing between the plane pairs, the horizontal plane inductance is also smaller. However, still the benefit can be leveraged from using ZDC for any plane stackup but the advantage is more pronounced in case of a thickly spaced plane pairs, which is a typical scenario in case of lower layer count, cheaper PCB designs.

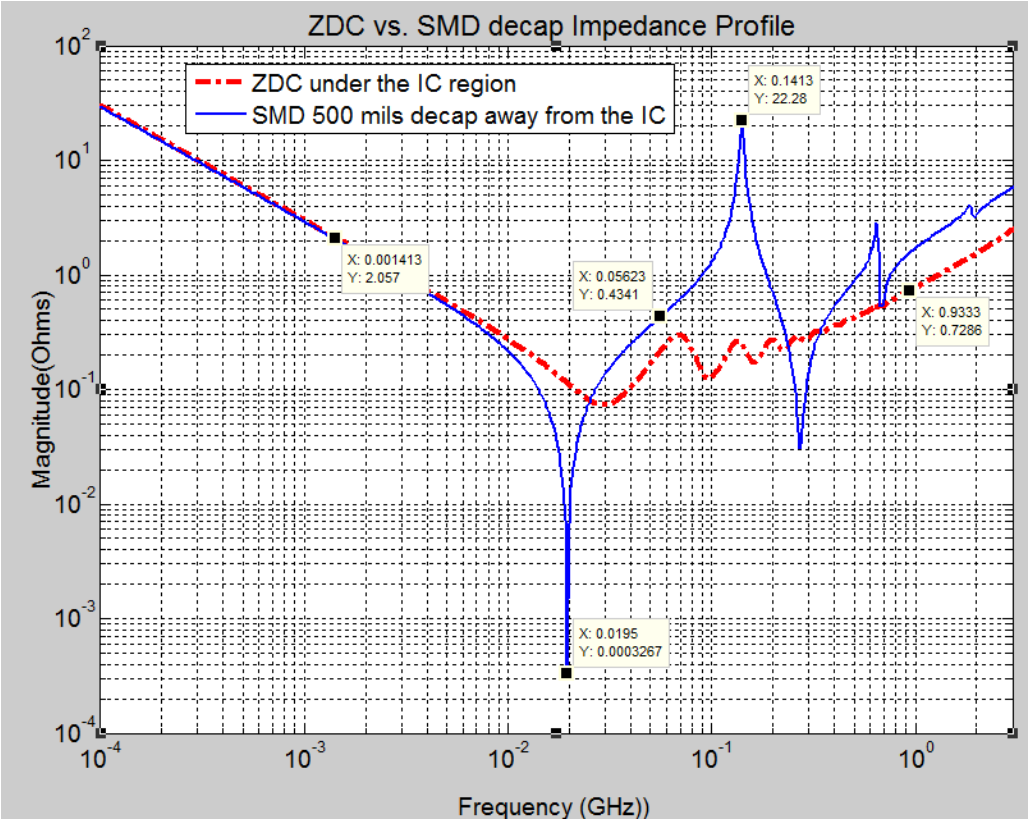


Figure 4.10 ZDC vs Regular Decap Compared in a Narrow, Multiple PWR/GND Planes

Table 4.2 ZDC vs Regular Decap Compared in a Narrow, Multiple PWR/GND Planes

Simulation model	Capacitance	Inductance
ZDC underneath the IC	~53 nF	~0.130 nH
Regular SMT decap 500mils away from the IC	~53 nF	~1.21 nH

4.3. VALIDATION OF SIMULATION TOOL

Before proceeding to the system level implementation of the ZDC, the simulation results of the commercial tool has to be validated in order to reassure the performance

accuracy of the design using the tool. Hence, the simulation tool is validated in two different approaches. Firstly, using two port Vector Network Analyzer (VNA) measurements and then by developing an equivalent circuit model for the PCB design using cavity model techniques.

4.3.1. Overview of the Geometry. The test vehicle utilized is a four layer PCB design with signal layers on top and bottom while second layer is GND and on third layer resides the PWR net of our interest.

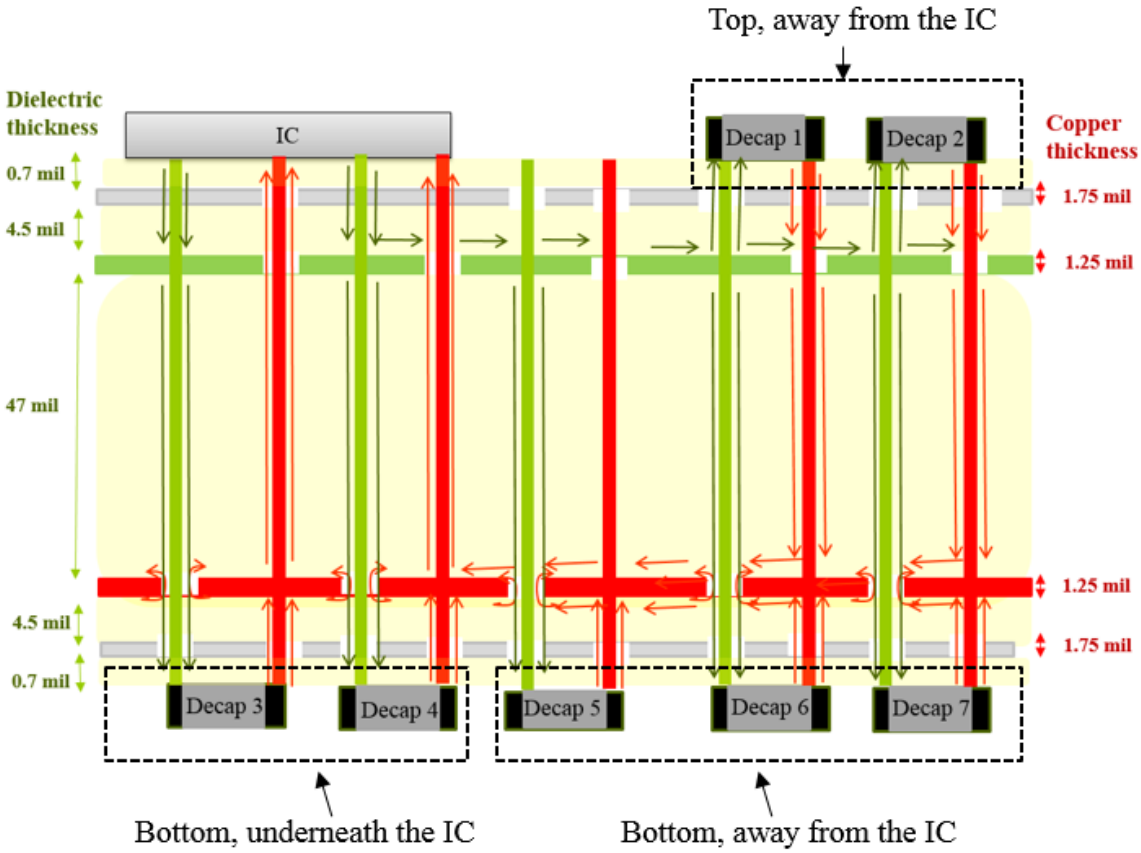


Figure 4.11 PCB Stackup and Current Path Flow

A high level schematic of the geometry given in Figure 4.11 is for representation purpose only. There are total of 33 decaps connected to the PWR net, out of which 6 decaps

are in the bottom layer located exactly underneath the IC region, another 19 decaps on the bottom layer but away from the IC, and 8 decaps on the top layer – away from the IC. In the simulations, the port is set on one of the 6 decaps which are on the bottom layer, underneath the IC region.

4.3.2. Two Port VNA Measurements. It is challenging to ultra-low impedance for PDN using a one port measurement due to the limitation of the parasitics associated with the test fixture used to perform measurements [6].

4.3.2.1. Measurement principle. The two-port measurement technique as shown in Figure 4.12 is used, where the PDN impedance is inherent in the insertion loss of the two port measurement as mentioned in (1). The second order equation mentioned in (1) is suitable for any impedance measurement using two port technique, while the first order impedance calculation is applicable only for ultra-low impedances.

$$Z_{PDN} = 25*S(2, 1)/(1-S(2, 1)) \quad (1)$$

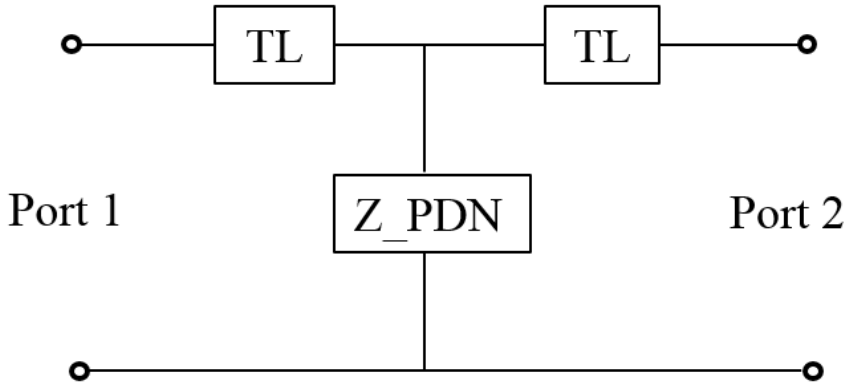


Figure 4.12 Two Port Measurement Principle

4.3.2.2. Measurement setup. Figure 4.13 and Figure 4.14 shows the measurement setup using 1mm S-G probes to perform a two port scattering parameter measurement using Vector Network Analyzer (VNA). The frequency range of the measurement is 100 KHz to 3 GHz.

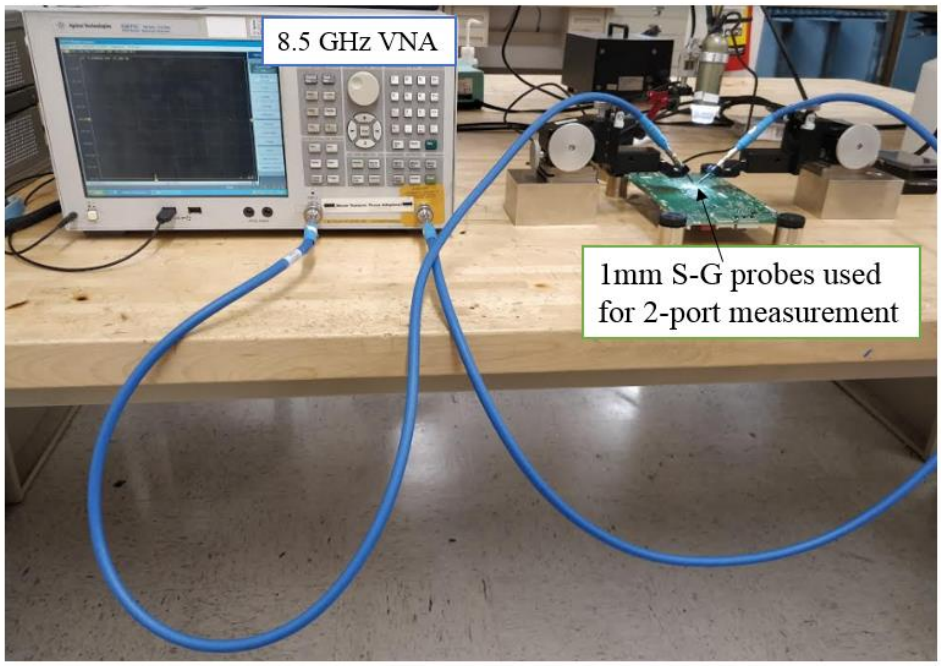


Figure 4.13 Two Port Measurement Setup Using the VNA

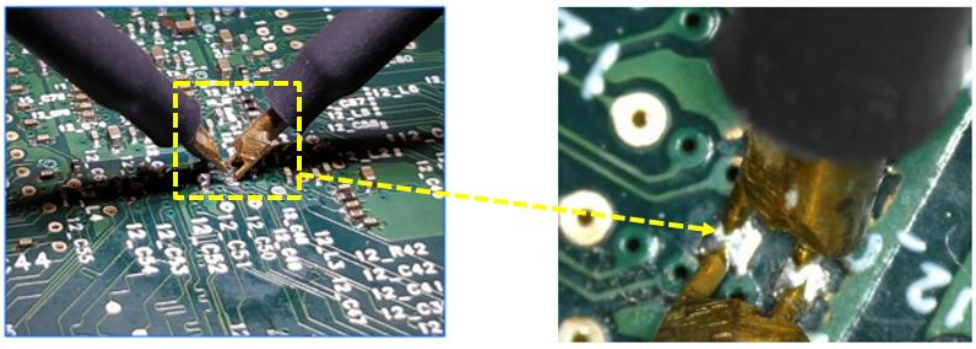


Figure 4.14 Close View of the Two Probes Landing on Pads of a Decoupling Capacitor

Upon recording the thru measurement, the impedance profile has been computed using the formula mentioned in (1). The closer view of the two probes landing on pads of decoupling capacitor on the bottom of the PCB is shown below.

4.3.3. Developing an Equivalent Circuit Model Using Cavity Model. In order to represent the current path physics on the PCB design, an equivalent circuit model is developed using cavity model approach. For simplicity, the decaps which are an inch away from the IC are grouped together depending upon their location and capacitance. The connection inductance associated with pads of decaps to the vias (L_{above}) is calculated using Plane Pair PEEC (PPP).

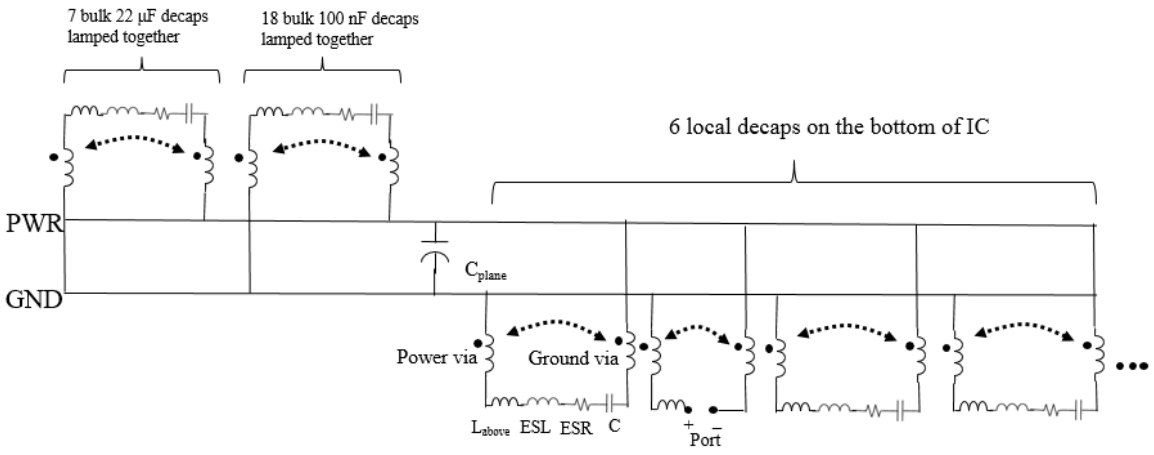


Figure 4.15 Cavity Model Equivalent Circuit

Moreover, the frequency dependent conduction loss of planes and vias is also considered (not shown in the Figure 4.15).

4.3.4. Comparison of Simulation and Measurement Results. The correlation of the simulation and measurements proceeded as a two-step process. Firstly, to evaluate the bare board inductance of the PCB, all the decaps on the board are depopulated and the

decap locations are shorted both in simulation and measurements. Secondly, the decaps are populated back to their corresponding locations and the impedance profiles are evaluated.

4.3.4.1. All decaps shorted. All the decaps are shorted on the board and the impedance profiles are compared in Figure 4.16.

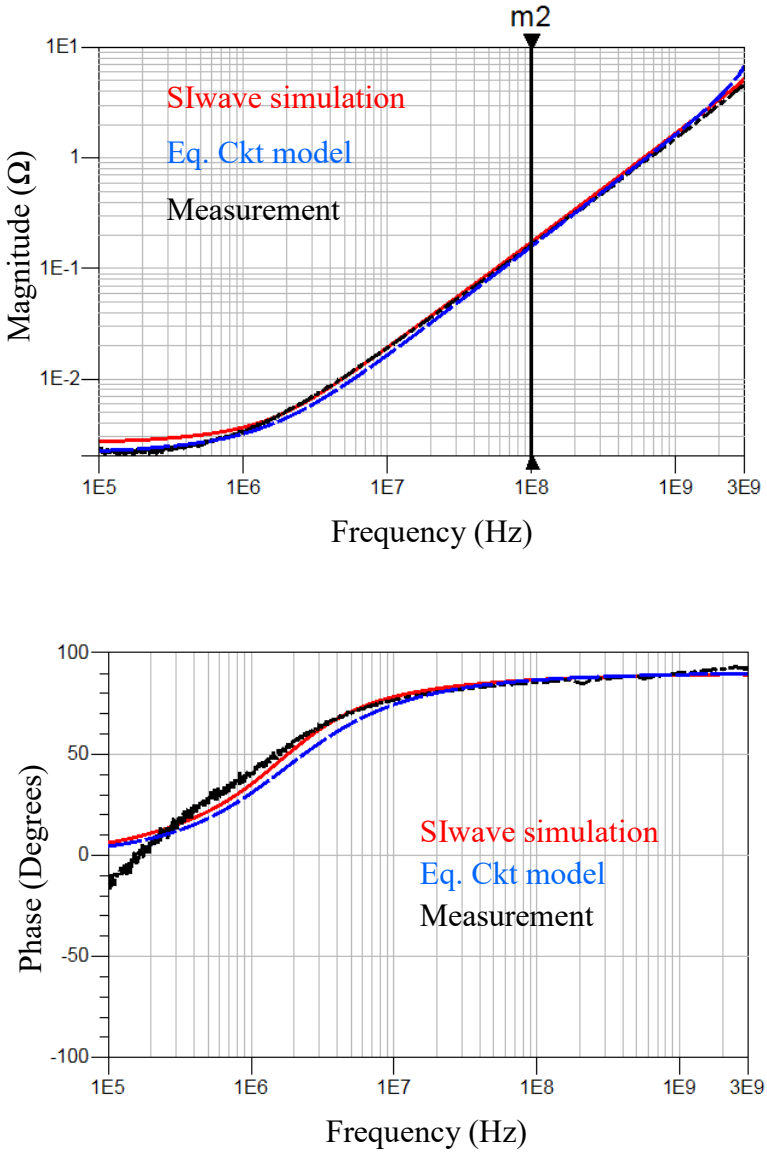


Figure 4.16 All Decaps Shorted on Board

As shown in Table 4.3, a favorable agreement between the simulation and measurements on this bare board reassures that all the simulation parameters in the

simulation tool are sufficient enough to represent the design accurately to that of a real PCB test vehicle.

Table 4.3 Inductance Correlation when All Decaps are Shorted

	Impedance @ 100 MHz	Inductance
Simulation model	~0.174 Ω	~0.276 nH
Measurement	~0.164 Ω	~0.261 nH
Cavity model Eq. Ckt	~0.159 Ω	~0.253 nH

4.3.4.2. All decaps re-populated on the board. Once the bare board inductance is correlated favorably between the simulation and measurements, all the decaps on the board, except the probing location (same as port in simulation) are re-populated and the impedance profile is evaluated.

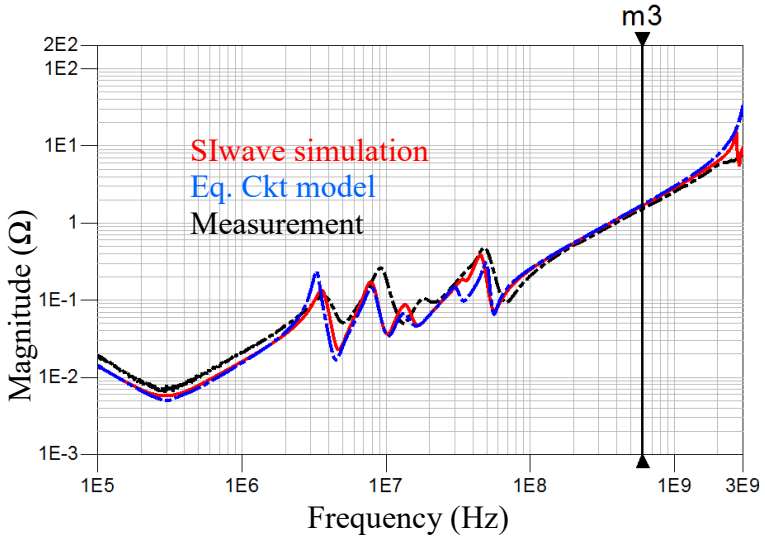


Figure 4.17 All Decaps Populated on the Board

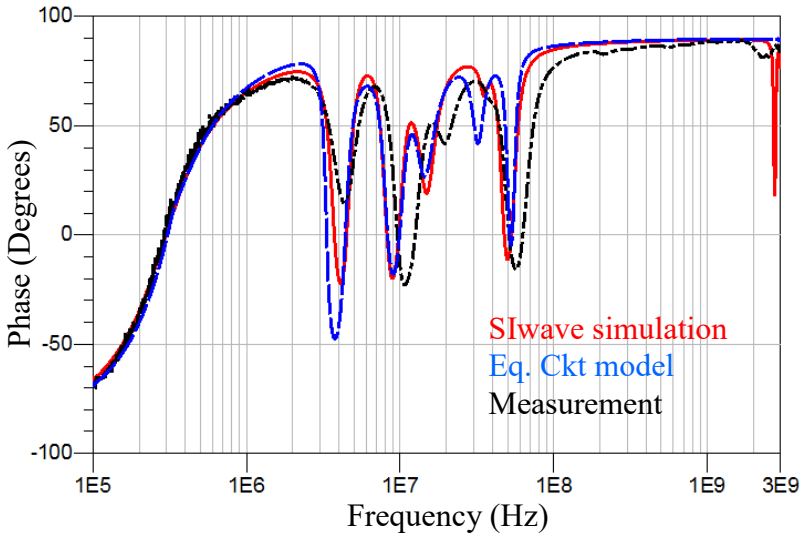


Figure 4.17 All Decaps Populated on the Board (Cont'd)

The impedance profile of the simulation corroborates favorably with the measurements and equivalent circuit model within 8% as shown in Figure 4.17 and Table 4.4, which connotes that the simulation tool is sufficiently good in representing the accuracy of performance of the complicated, real world design. Now that the accuracy of the simulation results using commercial tool is validated, the same commercial tool can be utilized to compare the system level performance of SMT decoupling solution for a real design with ZDC decoupling solution.

Table 4.4 Impedance Correlation When All Decaps Are Populated

	Impedance @ 600 MHz	Inductance
Simulation model	~1.674 Ω	~0.444 nH
Measurement	~1.575 Ω	~0.417 nH
Cavity model Eq. Ckt	~1.722 Ω	~0.456 nH

4.4. SYSTEM LEVEL IMPLEMENTATION OF THE ZDC ON REAL PCB DESIGN

Before proceeding to simulate the system level study of the ZDC, the placement and relevance of the existing capacitors on the real design has to be evaluated over a wide frequency range. As mentioned earlier, the power net of our interest has 33 decaps intended to serve as a decoupling solution for this design. Out of them, 27 decaps are away from the IC (~ 1 - 1.5 inch) and rest of the 6 decaps are exactly underneath the IC, on the bottom layer. Among the 27 decaps which are away from the IC, 8 are on the top layer while 19 of them are on the bottom layer. By intuition, it is a reasonable expectation that the 6 local decaps underneath the IC region are more effective in the mid-high frequency region. This is due to the low impedance path provided through the via inductance connecting the IC and local decaps on the bottom. However, in case of other 27 decaps, the vertical via inductances are dominated by the plane inductance due to the thick separation of PWR/GND plane pair. However, it is prudent to evaluate the contribution from all these capacitors at the mid-high frequency region so that those particular capacitors can be removed and ZDC can be integrated in to the system. Thus, this would pave a way for a valid system level comparison of performance of the ZDC and existing SMT capacitor solution.

Hence, to identify the relevance of the capacitors as per their placement in the design, the evaluation is carried out in a two stage process. Firstly, the 5 out of 6 local decaps are removed (while 1 of them is used for probing/port purposes) and 27 decaps which are away from the IC are shorted. This is to see the contribution of effective inductance of these 27 decaps to the overall effective inductance looking from the port when all the 32 decaps are shorted. Secondly, the 5 out of 6 local decaps are shorted (while

1 of them is used for probing/port purposes) and rest of the 27 decaps are removed. This is to see the effective inductance of local decaps and their contribution to the effective inductance looking from the port when all the 32 decaps are shorted. Lastly, all the 32 decaps are shorted in order to capture the effective interconnect inductance of all the decaps. The simulations are corroborated with measurements, following the same measurement principle and setup mentioned earlier.

4.4.1. Local Decaps Removed and 27 Decaps are Shorted. The inductance is significantly higher compared to the other cases due to the 47 mil thick separation of the PWR/GND plane pair as shown in Figure 4.18 and Table 4.5. The current path associated with the plane inductance dominates the vertical current paths due to the vias connecting decaps to the planes, which is evident in Figure 4.19.

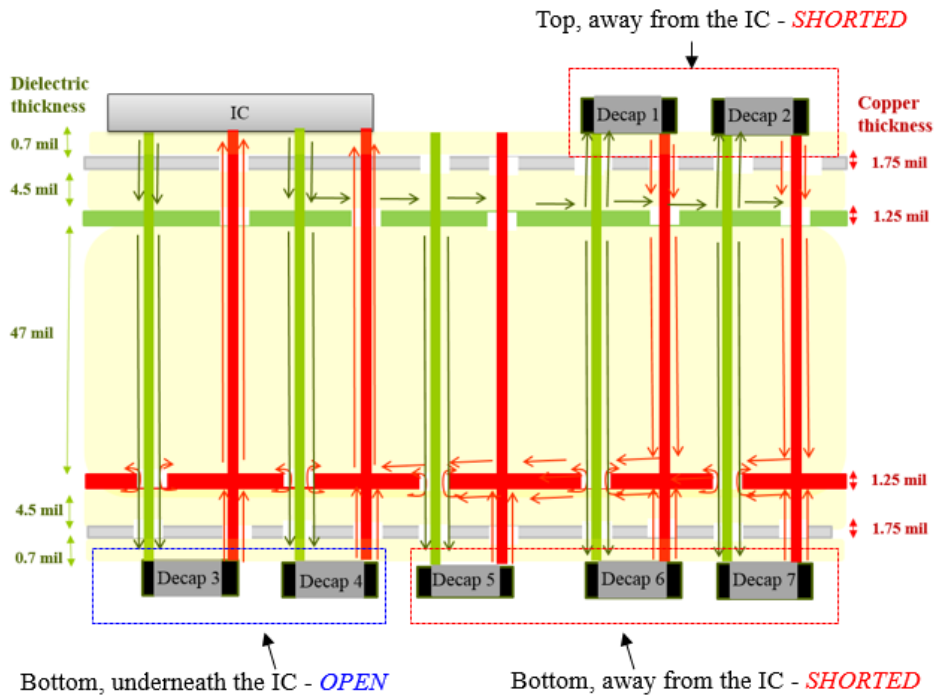


Figure 4.18 Local Decaps are Removed (open) and Rest of the Decaps are Shorted

Table 4.5 Impedance Profile of Local Decaps Open and 27 Decaps Shorted

	Impedance @ 100 MHz	Inductance
Simulation	1 Ω	1.59 nH
Measurement	1.118 Ω	1.77 nH
Cavity Model Eq. Ckt	0.884 Ω	1.41 nH

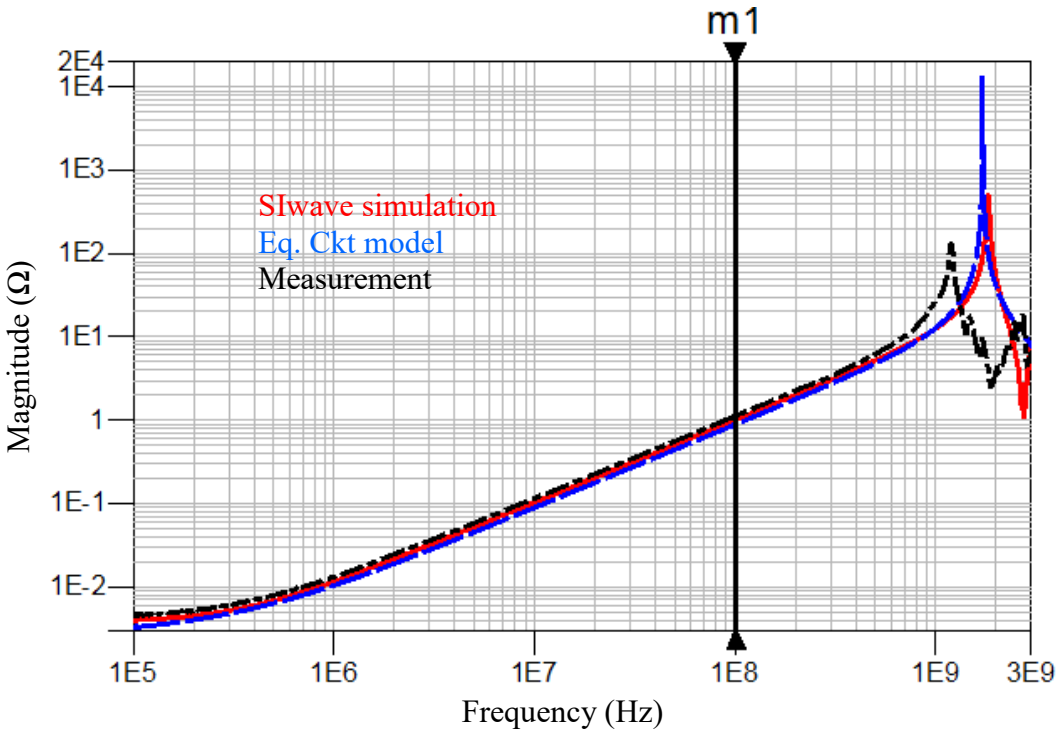


Figure 4.19 Local Decaps Open and 27 Decaps Shorted

4.4.2. Local Decaps Shorted and 27 Decaps are Removed. The impedance profile of the simulation correlates favorably with the measurements within 3.5% as shown in Figure 4.21 and Table 4.6. The geometry is shown in Figure 4.20.

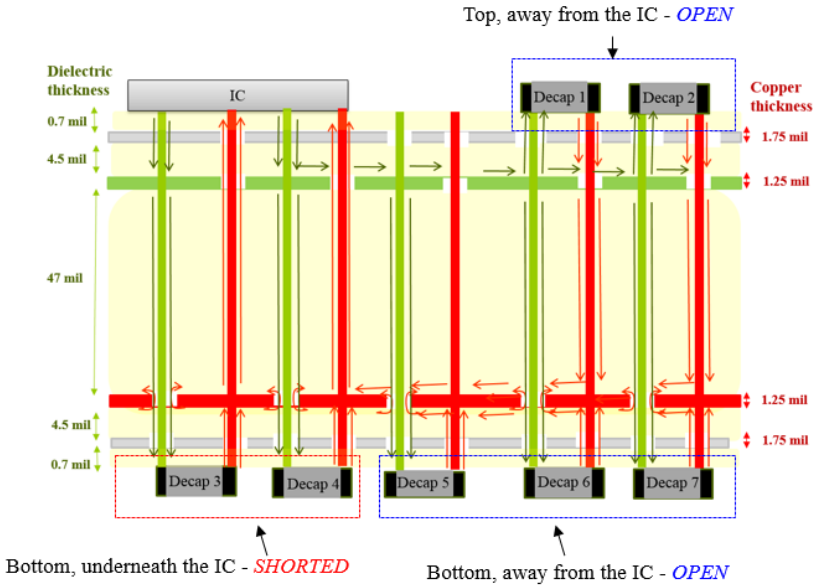


Figure 4.20 Local Decaps are Removed (open) and Rest of the Decaps are Shorted

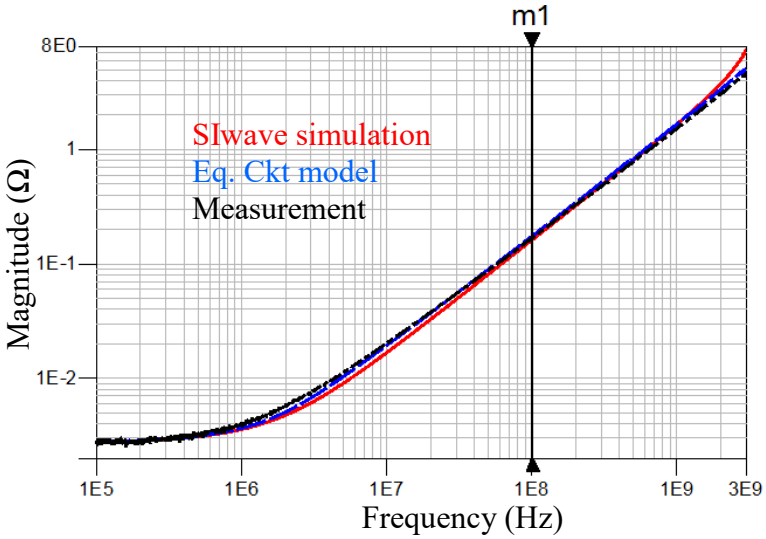


Figure 4.21 Local Decaps Shorted and 27 Decaps are Removed

The impedance is significantly lower in this case compared to the earlier case as mentioned in Table 4.6. This is because of the parallel combination of multiple vias to which the local decaps are connected.

Table 4.6 Impedance Profile of Local Decaps Shorted and 27 Decaps are Removed

	Impedance @ 100 MHz	Inductance
Simulation	0.175 Ω	0.278 nH
Measurement	0.169 Ω	0.268 nH
Cavity Model Eq. Ckt	0.162 Ω	0.257 nH

4.4.3. All the 32 Decaps are Shorted. The impedance profile of the simulation favorably with the measurements within 5.4% as shown in Table 4.6, documented from Figure 4.23. The geometry of the same is shown in Figure 4.22.

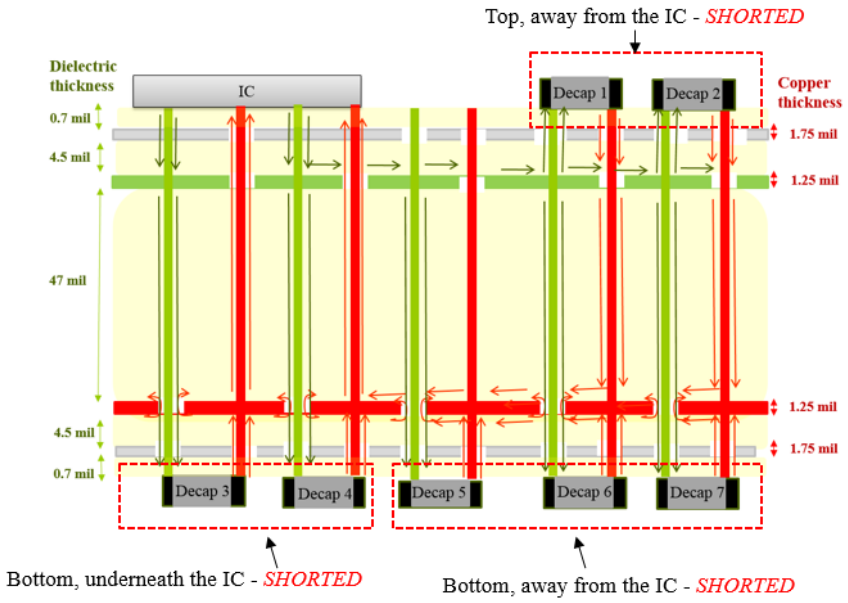


Figure 4.22 All the 32 Decaps are Shorted

When all the 3 different cases covered from sections 4.5.1 to 4.5.3, it can be noticed that the impedance profile reflects no change when all the 32 decaps are shorted or only the local 6 decaps are shorted. This reassures the assertion that only the 6 local decaps

which are under the IC region are effective in high frequency decoupling and the remaining 27 decaps have no influence as shown in Table 4.7.

Table 4.7 Impedance Profile When All the 32 Decaps are Shorted

	Impedance @ 100 MHz	Inductance
Simulation	0.174 Ω	0.276 nH
Measurement	0.164 Ω	0.261 nH
Cavity Model Eq. Ckt	0.159 Ω	0.253 nH

The purpose of using these 27 decaps in the design is two-fold. One is to provide the low frequency decoupling and the other is to serve as stitching capacitors for ensuring proper return path, for all the high speed signals transitioning from the top to bottom layers and vice versa. Such strategy is utilized often in PCBs with such low layer count, where there is shortage in the GND planes (as 1 GND plane in this 4 layer PCB).

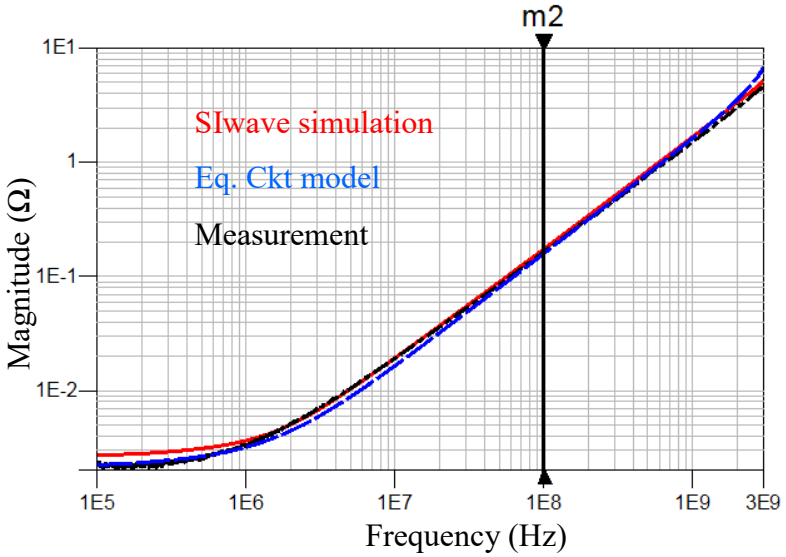


Figure 4.23 All 32 Decaps Shorted

However, as the ZDC is targeted to be placed under the IC package ball, the observation point (port) in our simulations has to be on the IC pins – top layer. Hence, from here on, we will be proceeding to use the commercial tool to evaluate the system level performance of the ZDC by electrically lumping all the IC pins of the power net of our interest. As a sanity check, after the port has been changed from decap on the bottom layer to the IC pins on the top layer, the simulations in sections 4.5.1 to 4.5.3 are repeated – but with port on the IC pins, as mentioned below in section 4.5.4.

4.4.4. Impedance Profile from the IC Standpoint. As expected, there isn't any difference shorting either all the 33 decaps or shorting the local 6 decaps underneath the IC region as shown in Figure 4.24, Figure 4.25 and Table 4.8. The geometry is shown in Figure 4.24. Now, we proceed to replacing these 6 local decaps which are effective decouplers in mid-high frequency with ZDC and compare the performance of the two profiles at the system level.

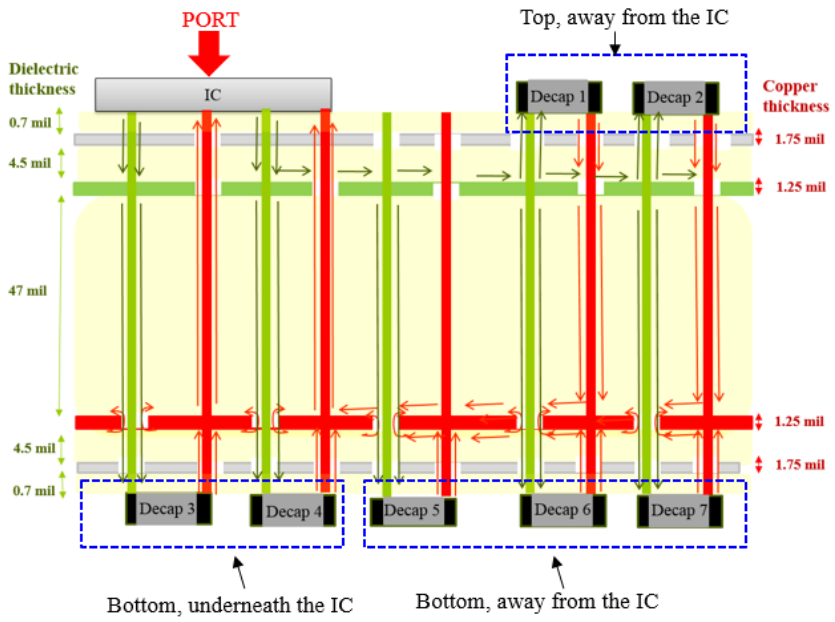


Figure 4.24 Changing the Port to the IC Pins on the Top Layer

Table 4.8 Impedance Profile of All Cases with Port on IC

Simulation Data	Impedance @ 100 MHz	Inductance
All 33 decaps shorted	0.113 Ω	0.179 nH
Only 27 decaps are shorted (6 local decaps removed)	0.581 Ω	0.924 nH
Only 6 local decaps are shorted (27 decaps are removed)	0.119 Ω	0.189 nH

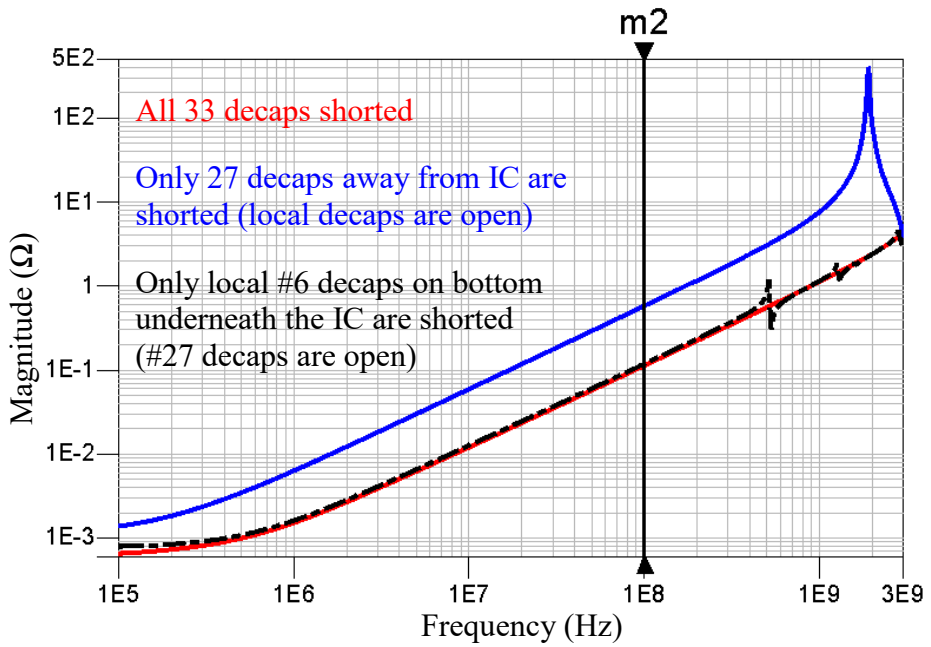


Figure 4.25 Impedance Profile with Each Case of Decaps Shorted

4.4.5. ZDC Integration in to PCB by Replacing Local Decaps. Though there are six local decaps on the bottom layer, underneath the IC, only two of them are shown in the Figure 4.26 just for representation purpose. These local decaps are replaced with the ZDC. Ideally, the ZDC will need to be embedded through the PCB, penetrating the layers

as shown in Figure 4.27. However, since our system level performance evaluation is based on simulations utilizing a commercial tool, the strategy is to assign s-parameters of the ZDC to a capacitor model connected between the IC PWR/GND pin pair in the XY plane on the top. Since the inductance looking through the IC port would include only the ESL of the ZDC, this approach is sufficient to mimic the realistic implementation of the ZDC connected between the IC PWR/GND pin pair. Thus, the six local decaps are replaced with six ZDCs. The six local decaps altogether contribute about 2.2uF capacitance. From the standpoint of utilizing the ZDC simulation model, the same ZDC model mentioned in [4] is used with few exceptions. The original prototype model was designed with 21 nF capacitance.

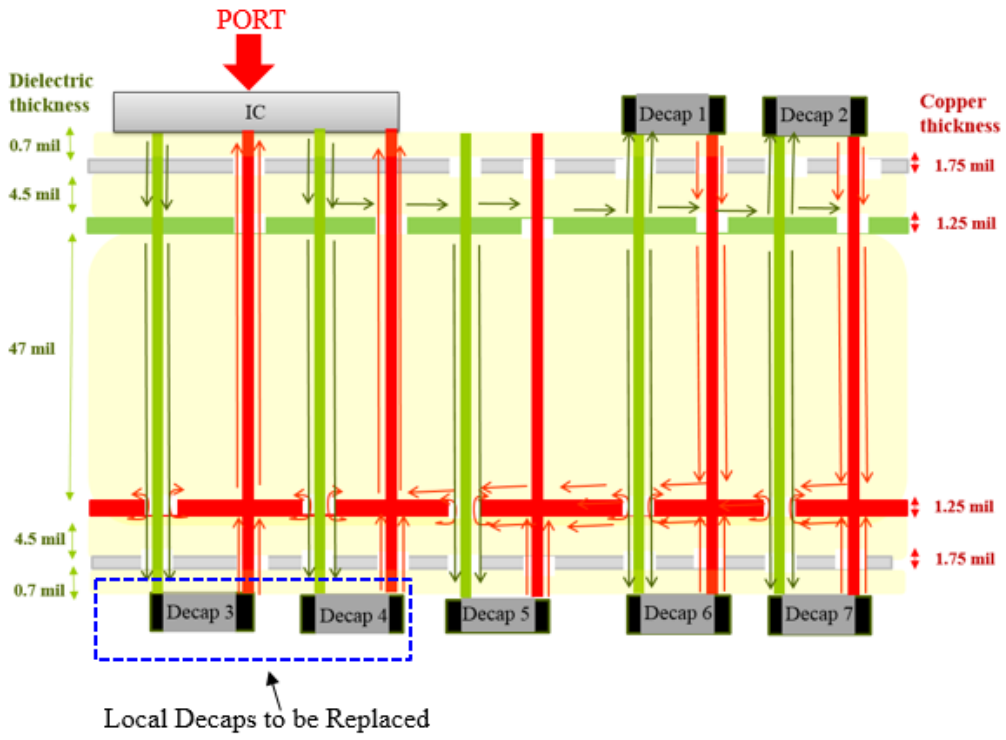


Figure 4.26 Six Local Decaps to be Replaced with Six ZDC

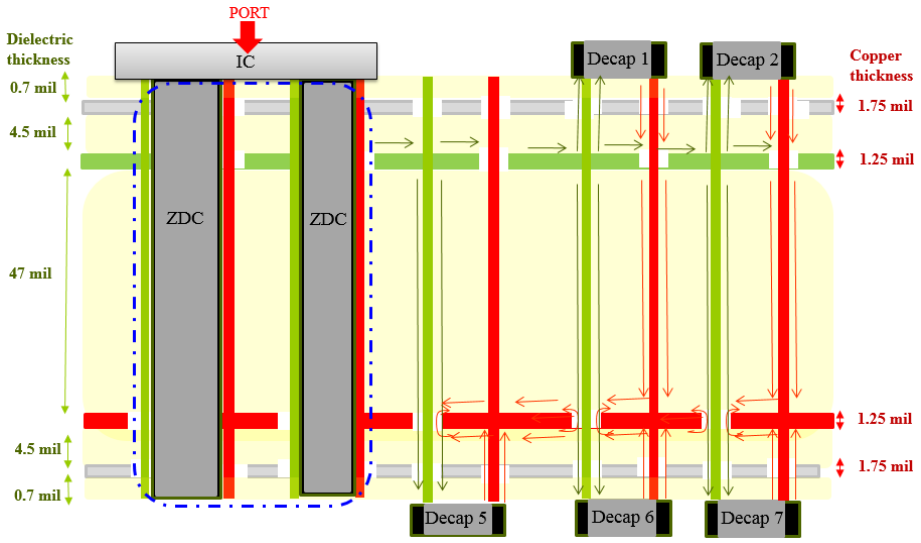


Figure 4.27 Six Local Decaps Replaced with Six ZDC

Hence, the thickness of the ZDC is made sure to be of exact thickness of the PCB stackup and the spacing between each layer has been adjusted in order to accommodate enough capacitance when replacing the existing local decaps and impedance profiles are compared below.

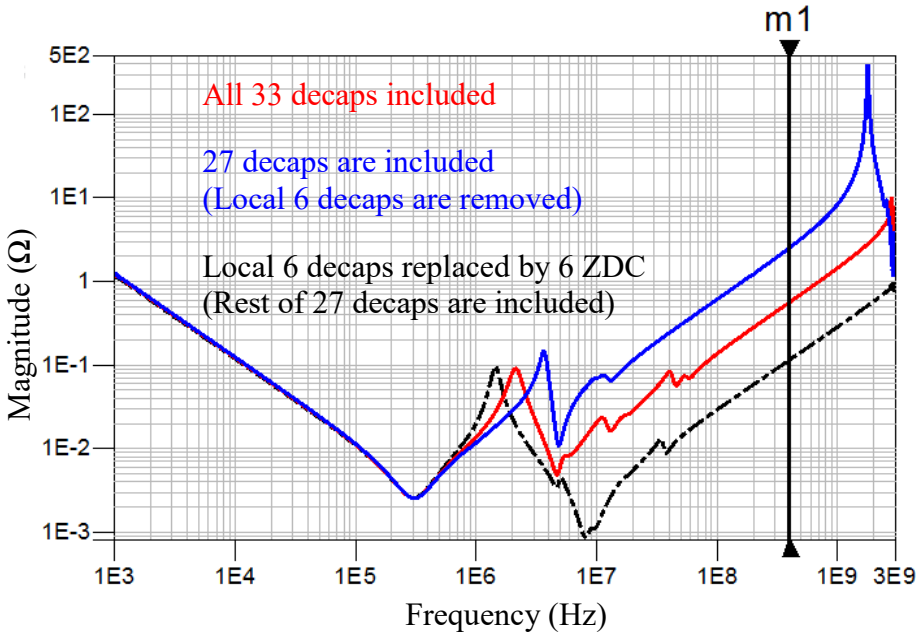


Figure 4.28 Comparison of Existing Design with that of ZDC

The system level impedance profile using ZDC exhibits superior performance when compared to that of the existing design with SMT decaps, above 1 MHz. The high frequency inductance is significantly reduced by 79% using ZDC as shown in Figure 4.28 and Table 4.9. This is due to elimination of the inductance due to the vertical portion of the current paths from IC down to the decaps through multiple vias.

Table 4.9 Comparison of Existing Design with that of ZDC

Simulation Data	Impedance @ 400 MHz	Inductance
All 33 decaps included	0.566 Ω	0.225 nH
Only 27 decaps are included (6 local decaps removed)	2.540 Ω	1.01 nH
6 local decaps replaced by ZDC (27 decaps are included still)	0.115 Ω	0.046 nH

Due to the large volume of the ZDC in the Z-direction, it is possible to accommodate more capacitance when needed (as in this case – each ZDC with 1 uF capacitance provides much better performance). Thus, with boosted high frequency performance, ZDC is a promising decoupling solution for the future PI applications.

5. CONCLUSION

The EMI design of the FQSFP connector is discussed by corroborating both measurements and simulations up to 18 GHz. The mitigation of the radiation by ~ 10 dB at 18 GHz, due to the shielding effect of the cage enclosed on the FQSFP connector is also discussed briefly from both measurements and simulations standpoint. The TRP profiles for both the aforementioned cases indicate that the simulation model is an accurate representation of the realistic design and is ready to roll off for any further improvements.

The system level implementation of the ZDC is discussed in detail. It is shown that the planes do not have any impact on the ZDC due to the port being on the top of the ZDC i.e., at the package ball of the IC. By comparing the performance of the ZDC to that of a regular decap placed 500 mils away from the IC, it is shown that much advantage can be leveraged using the ZDC for widely separated PWR/GND plane pair compared to narrow spaced PWR/GND plane pair. Finally, the effective decaps are identified in the real PCB design and the existing decoupling solution is compared to that of using ZDC. It is shown that ZDC gives new degrees of the freedom such as accommodating the required capacitance due to the large volume in the Z-direction and significantly nullifies the PCB inductance associated with the vias connecting the IC pins to the decaps. Thus, ZDC is endeavoring as a promising decoupling solution for future PI applications.

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