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System level power integrity transient analysis using a physics-based approach

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SYSTEM LEVEL POWER INTEGRITY TRANSIENT ANALYSIS USING A PHYSICS-BASED APPROACH

by

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PUBLICATION THESIS OPTION

This thesis consists of the following three articles, which have been submitted for publication, or will be submitted for publication as follows:

Paper I: Pages 7-38, "System Level Power Integrity Transient Analysis Using Physics-Based Approach and Optimization with Hybrid Target Impedance," is intended for submission to IEEE Symposium on Electromagnetic Compatibility and Signal/Power Integrity (EMCSIPI) 2019.

Paper II: Pages 42-58, "A Survey on Modeling Strategies for High-Speed Differential Via between Two Parallel Plates," published in 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSIPI).

Paper III: Pages 60-72, "Application of Deep Learning for High-speed Differential Via TDR Impedance Fast Prediction," published in 2018 IEEE Symposium on Electromagnetic Compatibility and Signal/Power Integrity (EMCSIPI).

ABSTRACT

With decreasing supply voltage level and massive demanding current on system chipset, power integrity design becomes more and more critical for system stability. The ultimate goal of well-designed power delivery network (PDN) is to deliver desired voltage level from the source to destination, in other words, to minimize voltage noise delivered to digital devices. The thesis is composed of three parts. The first part focuses on-die level power models including simplified chip power model (CPM) for system level analysis and the worst scenario current profile. The second part of this work introduces the physics-based equivalent circuit model to simplify the passive PDN model to RLC circuit netlist, to be compatible with any spice simulators and tremendously boost simulation speed. Then a novel system/chip level end-to-end transient model is proposed, including the die model and passive PDN model discussed in previous two chapters as well as a SIMPLIS based small signal VRM model. In the last part of the thesis, how to model voltage regulator module (VRM) is explicitly discussed. Different linear approximated VRM modeling approaches have been compared with the SIMPLIS small signal VRM model in both frequency domain and time domain. The comparison provides PI engineers a guideline to choose specific VRM model under specific circumstances. Finally yet importantly, a PDN optimization example was given. Other than previous PDN optimization approaches, a novel hybrid target impedance concept was proposed in this thesis, in order to improve system level PDN optimization process.

ACKNOWLEDGMENTS

First, my sincere gratitude and respect go to my advisor, Prof. Jun Fan, for his support and guidance of my master degree study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and finish this thesis. I would like to give my special thanks to Prof. James L. Drewniak for his instruction and support on both my technical and non-technical skills. I would also thank Prof. Chulsoon Hwang for provide his suggestion and hard questions to widen my research from various perspectives.

I would like to thank all my colleagues and friends in the EMC laboratory for their support and cooperation during my master coursework and research. I am very grateful to my parents for their endless love and support throughout these years.

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1. INTRODUCTION

1.1. BACKGROUND

To deliver a reliable power delivery network is a critical design challenge for a Chip-Package-PCB System as shown in figure1.1. As the chip semiconductor integrated process scale down to nano-scale, the chip supply voltage is also continuously decreasing. From International Technology Roadmap for Semiconductors (ITRS) 2015 report as shown in table 1.1, the supply voltage will move from 0.85V to 0.64V at 2022 [1]. At the same time, the current demand for microprocessor unit (MPU) or central processing unit (CPU) is also growing with higher computational ability and power as the arrival of artificial intelligence era, the development of computer-aided engineering, smartphones, robotics and pilotless automobile.

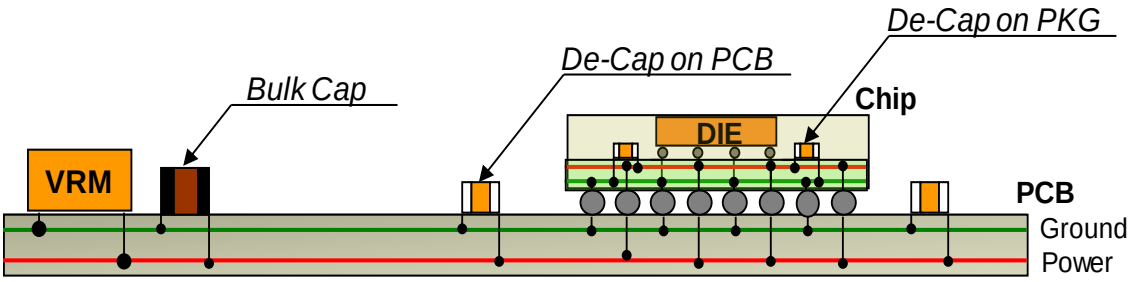


Figure 1.1. Chip-Package-PCB System Full Power Delivery Network (PDN)

The target impedance is a metrics for evaluating the qualification of the power delivery network. From table1.1, target impedance will potentially decrease to 0.315mΩ in future years. That assumed it is calcucated with 2.5% voltage noise tolerance dividing

to 25% current change. This impedance could become less if the chip can only tolerate a smaller voltage noise less than 2.5% or have larger current change than 25%. These would be extremely hard to meet the design target to main a robust system circuit performance.

Table 1.1. 2015 International Technology Roadmap for Semiconductors (ITRS)

Year	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**
Voltage (V)	0.85	0.82	0.80	0.77	0.75	0.73	0.71	0.68	0.66	0.64
Power (W)	149	152	143	130	130	136	133	130	130	130
Current (A)	175	185	179	169	173	186	187	191	197	203
Target Imp (mΩ)	0.486	0.443	0.447	0.456	0.434	0.392	0.380	0.356	0.335	0.315

Therefore, it is important to develop a set of methodology to analyze and optimize the PDN then validate the proposed design for the Chip-Package-PCB system full PDN. The system full PDN represented by simplified circuit elements as shown in figure 1.3. The Chip-Package-PCB system includes voltage regulator module (VRM), printed circuit board (PCB), chip package (PKG), chip die and capacitors (CAP). The resistance of these components would cause dc voltage drop, that decreases nominal voltage to a lower voltage and potentially cause a thermal issue of the system.

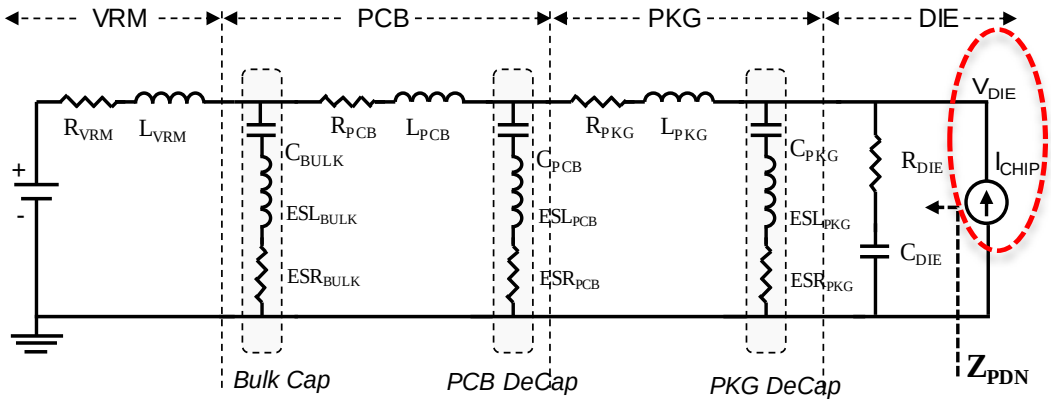


Figure 1.2. Simplified Circuit Representation of System Full PDN

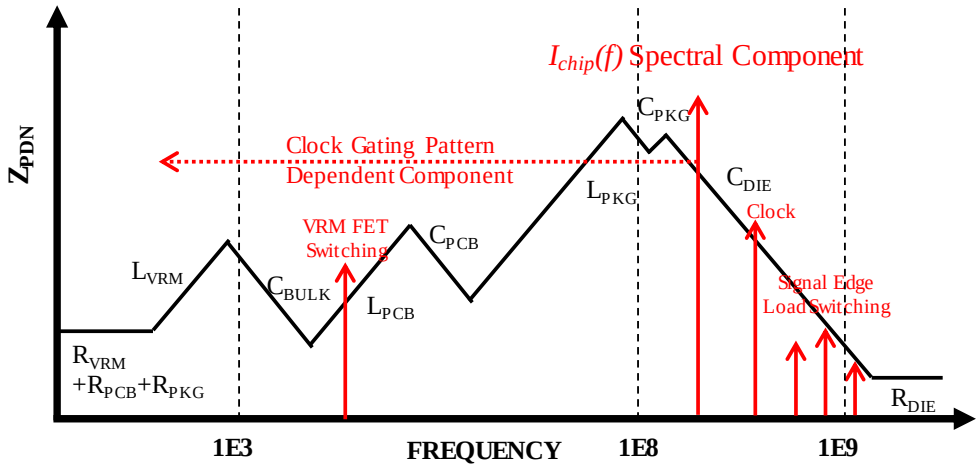


Figure 1.3. Full PDN Impedance and Current Spectral Component on DIE

$$V_{DIE}(f) = Z_{PDN}(f) * I_{chip}(f)$$

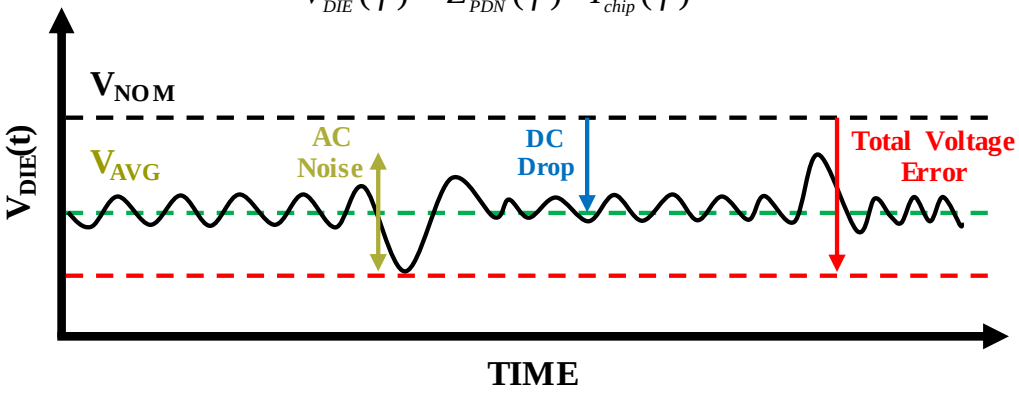


Figure 1.4. Transient Voltage Response on DIE

The PCB and PKG have parasitic inductance, which create anti-resonance with the capacitance in the PDN as shown in the figure 1.3. Especially the resonance peak that cause by package inductance and chip die capacitance would be the highest impedance, which exceed the expected target impedance to make a critical voltage noise to the system chip. From clock gating operation pattern, current spectral components would also vary from a broadband range in middle frequency. These current spectral components multiply with PDN impedance. It would also create an unexpected ac noise droop.

Totally, the DC drop and AC noise of supply voltage will give the total voltage error for the supplied chip. These could cause logic gate error, functional failure, excessive thermal issue and even system chip damage. The well-designed power delivery network from a set of effective methods from system-level is greatly important for maintaining a robust Chip-Package-PCB System.

1.2. MOTIVATION AND CHALLENGE

For system each parts, there are several available models developed for analyzing their behavior and performance as shown in table 1.2. Serval analysis tool and simulators also developed for analyzing each model from different perspectives. The impedance profile could achieve from s-parameter model, spice model, RLC model for frequency domain analysis and optimization to meet the target impedance. The voltage noise could calculate from simulator with these models but the computational time would be very consuming from different tools. How to integrate available models in one compliable simulator for a better approximately accurate simulation, optimization and validation process in a faster way would a critical challenge for system level PI simulation.

Table 1.2. Common Models Comparison for Each Parts in System PI Analysis

	VRM Model	PCB/PKG Model	DECAP Model	Chip Model
Available Models	▪ Small Signal Model ▪ Linear RL Model ▪ Behavior Model	▪ S-parameters Model ▪ Broad-Band Spice Model ▪ Equivalent Circuit Model	▪ S-parameters Model ▪ Spice Netlist Model ▪ RLC Circuit Model	▪ CPM model ▪ Distributed Model ▪ Lumped Model ▪ Vector-aware VCD ▪ Vectorless Profile

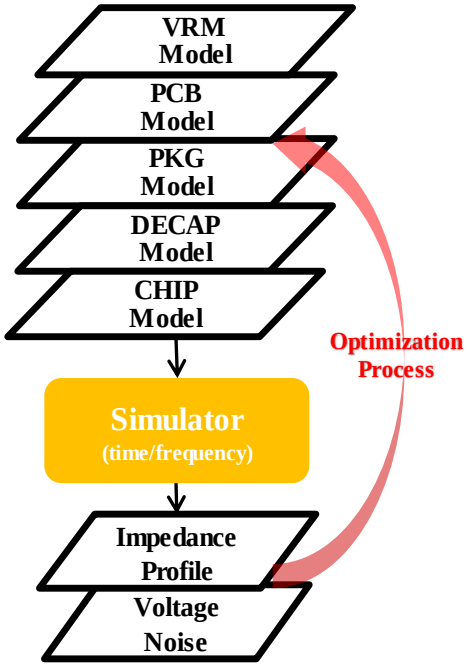


Figure 1.5. System-level Power Integrity Simulation Flow

1.3. RESEARCH LITERATURE REVIEW

Power integrity analysis to power delivery network design are critical topics in both academic and industrial for many years.

About VRM modeling [2]-[4], [L. Smith et al. 1999] four-element model, and [C. Chung et al. 2001] simplified inductor Model were applied for power integrity analysis.

[K.Yao Phd. 2004], [Y.Qiu Phd. 2005] and [S. Baek et al.2012] provided high-frequency modeling and behavior modeling for buck converters.

About chip power modeling [5]-[13], [J. Zheng et al.2007] presented reduced order CPM model by Norton equivalent circuit with Krylov subspace approximation. [A. Waizman et al. 2004] proposed integrated power supply frequency domain impedance meter (IFDIM) method for system full impedance measurement from the die; [S.Sun ea al.2010] gave On-Die Noise and Capacitance Measurement. [X. Zhang et al. 2013], [L. Smith et al. 2012] and [I.Novak et al. 2013] discussed worst-case PDN noise by reverse pulse technique. [K. Koo et al.2015] and [D. Hu et al.2015] extended CPM model for system core power optimization.

About PDN metrics Target Impedance [14]-[15], [L. Smith et al. 1999] proposed a target impedance to be met across a broad frequency range, [J. Kim et al. 2010, 2013] identified improved Target Impedance and IC transient measurement, [O. Dan et al. 2014] presented improved Target Impedance Method for PCB Decoupling of Core Power.

About power delivery network and PCB channel modeling, [16]-[101] provided related studied about power plane, via modeling and via-plane capacitance calculation related research work for passive interconnector electromagnetic (EM) modeling and analysis. The equivalent circuit model for system interconnectors was investigated from [16]-[32] by various methods including the cavity model and parallel plate partial element equivalent circuit (PEEC) methodology. In addition, related mathematical, analytical and experimental methodology from [33]-[101] were investigated by various researchers from different perspectives for the power delivery network (PDN) modeling and interconnectors electromagnetic (EM) performance modeling for the Chip-Package-PCB System.

PAPER

I. SYSTEM LEVEL POWER INTEGRITY TRANSIENT ANALYSIS USING PHYSICS-BASED APPROACH

ABSTRACT

In this section, a methodology for system level end-to-end transient analysis was developed and validated in SIMPLIS tool with current path physics-based equivalent circuit model of board and package, simplified on-die power model and load current profile. Then compared the SIMPLIS small signal VRM model with different linear models of voltage regulator module (VRM) in both frequency domain and time domain, these comparisons and studies present the advantage of this methodology using equivalent circuit model for system level power integrity transient analysis. This thesis work also proposed a method of hybrid target impedance including current profile-based discrete and continuous target impedance. This hybrid target impedance could apply for system level PDN optimization to get a qualified and convergent solution to meet the supply voltage specification of the chip power. The PDN impedance optimization in frequency domain and voltage response validation in time domain are both achieved effectively in this thesis work with the hybrid target impedance and the physics-based equivalent circuit model.

1. ON-CHIP POWER NETWORK AND LOAD TRANSIENTS

1.1. ON-CHIP POWER NETWORK MODEL

Due to the continuous scaling on-die transistors process technology and increasing power consumption of the chips, the voltage noise related on-chip failure has drawn industrial-wide attention in past decades [4]-[6].

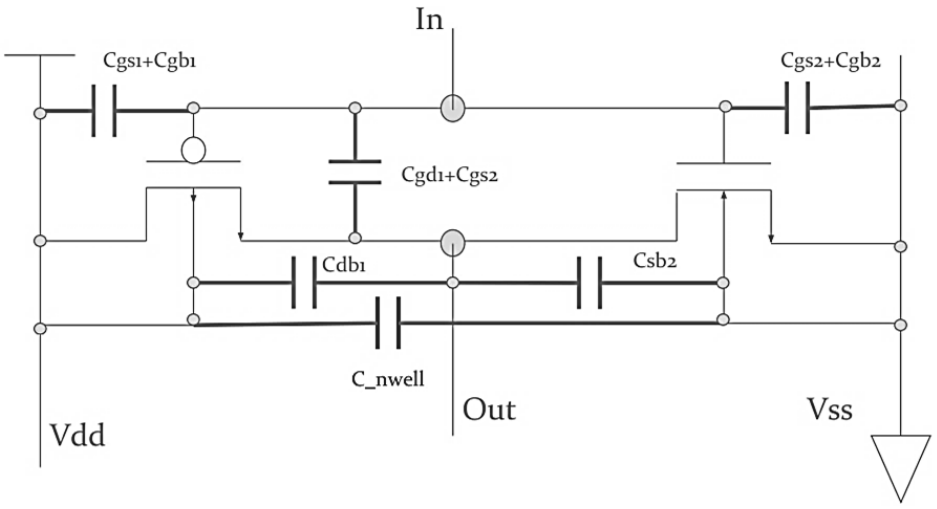


Figure 1. Parasitic Capacitance Circuit Representation of On-Die Transistors

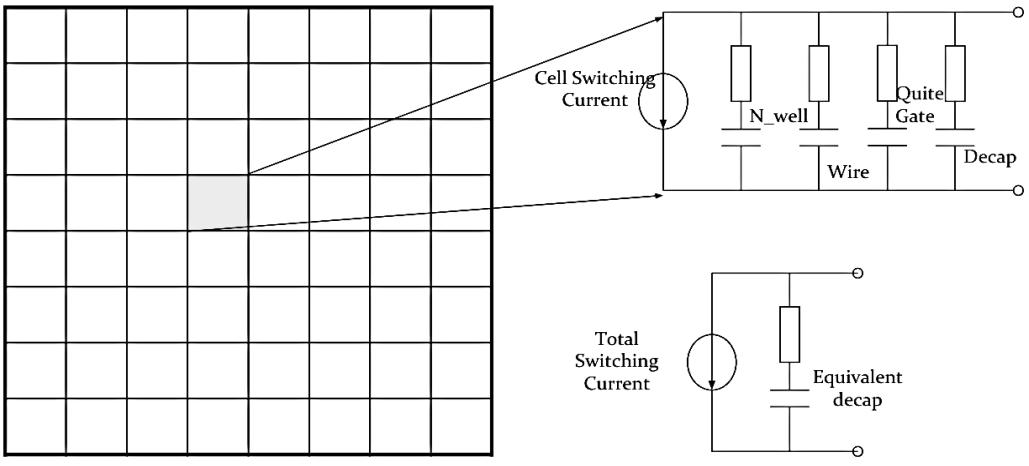


Figure 2. Simplified Lumped Equivalent Chip Power Model

The chip power model (CPM) is a common chip power modeling approaches presented from Apache Design [4] for system level power integrity analysis and optimization. Full-chip switching scenario needs to be determined first in order to build the model of the on-chip power network. Non-switching instances with parasitics are modeled by their lumped RC equivalent circuit [4] as shown in figure 1. Then switching instances are modeled by a linearized macro-model including parametric voltage-dependent current sources as shown in figure 2.

1.1.1. Lumped and Reduced Order Power Model. The passive RC network model includes that the original full-chip power network may contains 100M+ cells. These multiple order power model was reduced to lumped order as shown in figure 3, which might loss high frequency accuracy but could provide approximate voltage response as show in figure 4. Therefore, this reduced order lumped RC circuit model is desirable to employ the CPM model for on-PCB and on-PKG level design optimization.

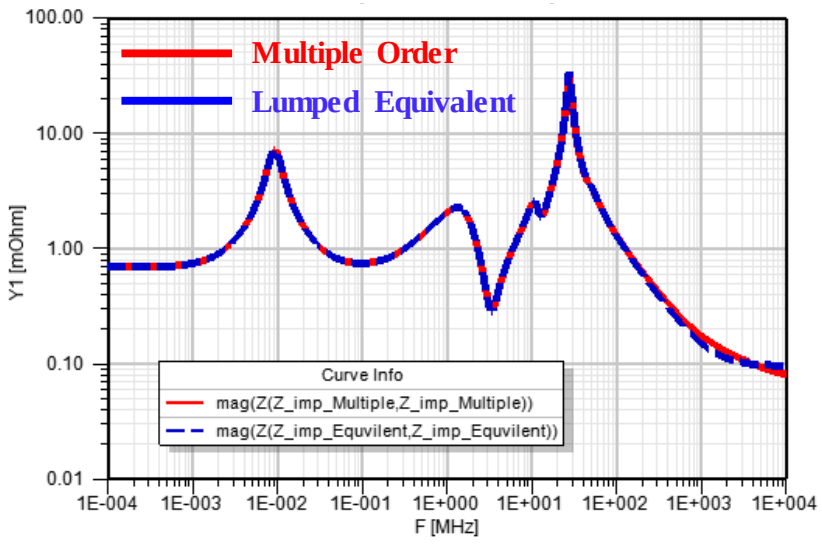


Figure 3. Frequency Domain Comparison between Lumped Equivalent Power Model and Multiple Order Power Model

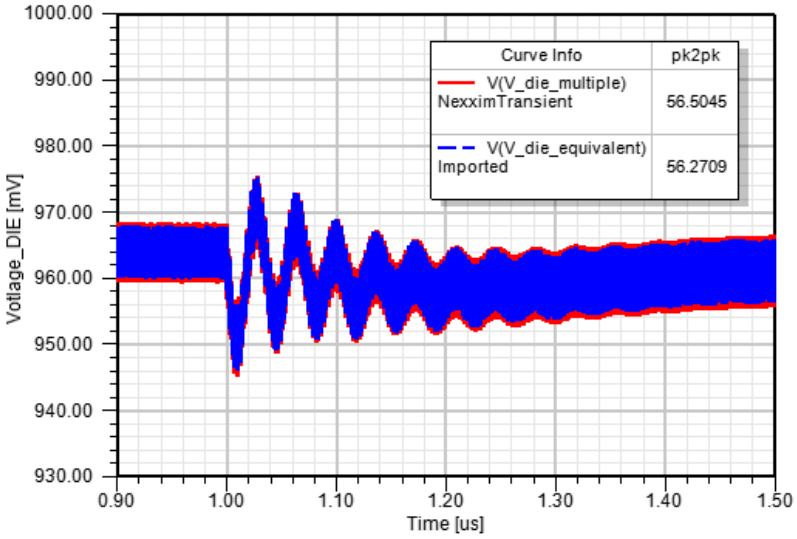


Figure 4. Time Domain Comparison between Lumped Equivalent Power Model and Multiple Order Power Model

1.1.2. Simplified Current Load and Pwl Current Profile. In the CPM model, the switching instance can be modeled by voltage-dependent current sources with piecewise linear (pwl) current profile as show in figure 5. The on-chip low power load operation was categorized from different operation origins [9]-[10] as shown in table 1. The dynamic clock gating is dominating frequency spectral components above clock frequency. The clock gating sequence is the key components to middle-lower frequency range, which need on-PCB and on-PKG DECAP for noise suppression.

This full-chip switching scenario can be determined with only focusing on clock gating sequence operation, categorized with random mode, step model and resonance mode scenario. From comparison in figure 7, the clock gating only scenario presented the similar spectral components at lower frequency to complete profile including pwl current. The higher frequency range above clock frequency cannot be optimized from system level, which can only be improved from on-die power network design and with on-die DECAP.

The clock gating only current profile can also give the same envelop on voltage response as shown in figure 8, which did not consider higher-frequency switching noise along the envelop as shown in figure 9. Therefore, this clock gating only current profile is desirable to employ the CPM model for on-PCB and on-PKG level design optimization.

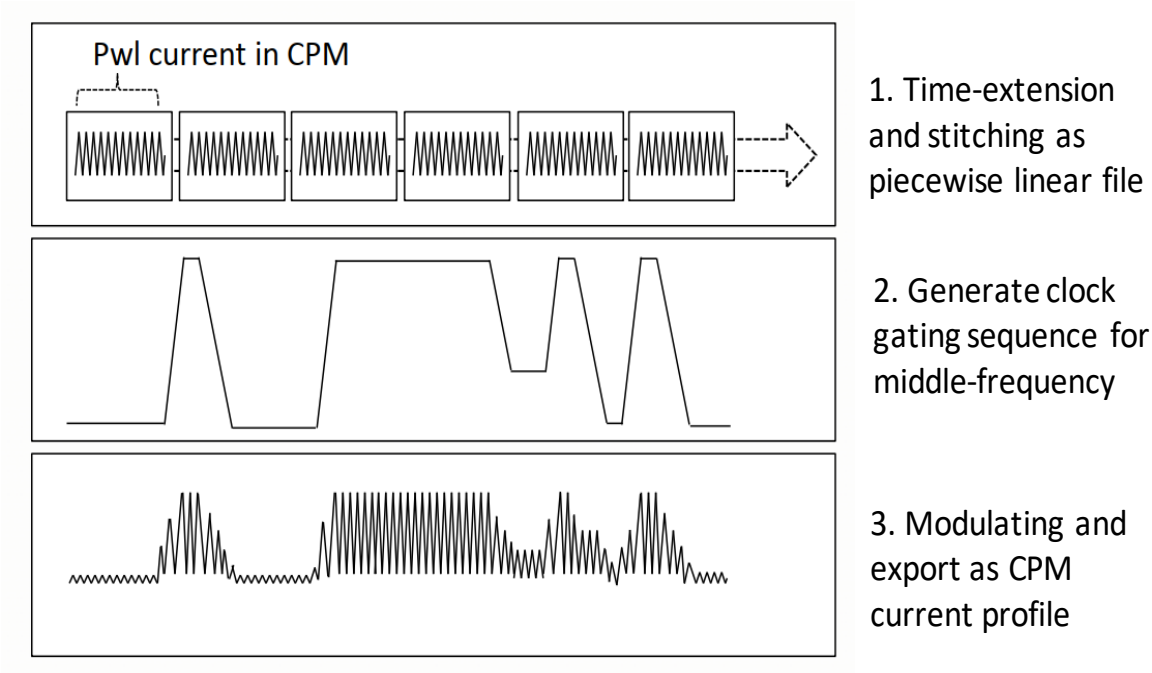


Figure 5. Current Profile Modulation for Load Transients Modeling

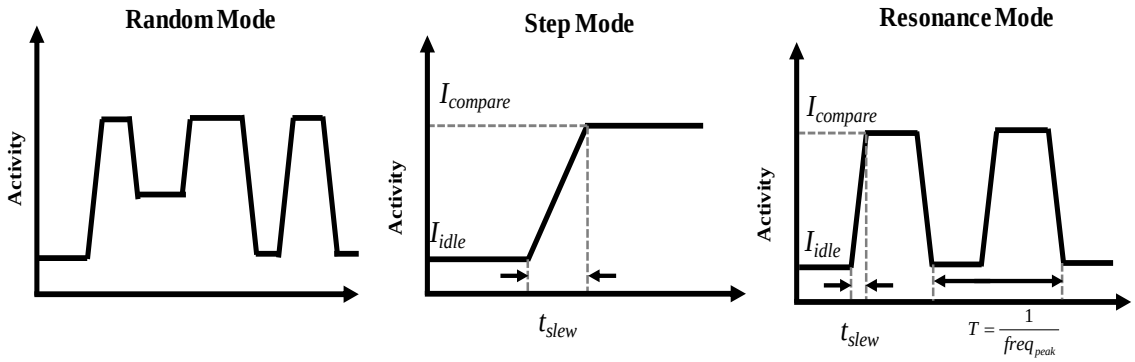


Figure 6. Typical Operating Mode for Clock Gating Sequence

Table 1. On-chip Low Power Load Operation that Possibly Cause Critical Noise

Load Operating Origin	Transition Time	Expected Freq. Spectral Components	Suppression Technique	Consideration for System PI Analysis
DVFS	ms order	< kHz	VDD monitoring by VRM	Not required
Power Gating	us to ms	kHz ~ 0.1Mhz	VDD monitoring by VRM and current control	Not required
Clock Gating	us order	0.1 ~ 100 Mhz	On-PCB Decap, On-PKG Decap	Required
Dynamic Clock Gating	ns order	> 100 Mhz	On-die decap	Not required

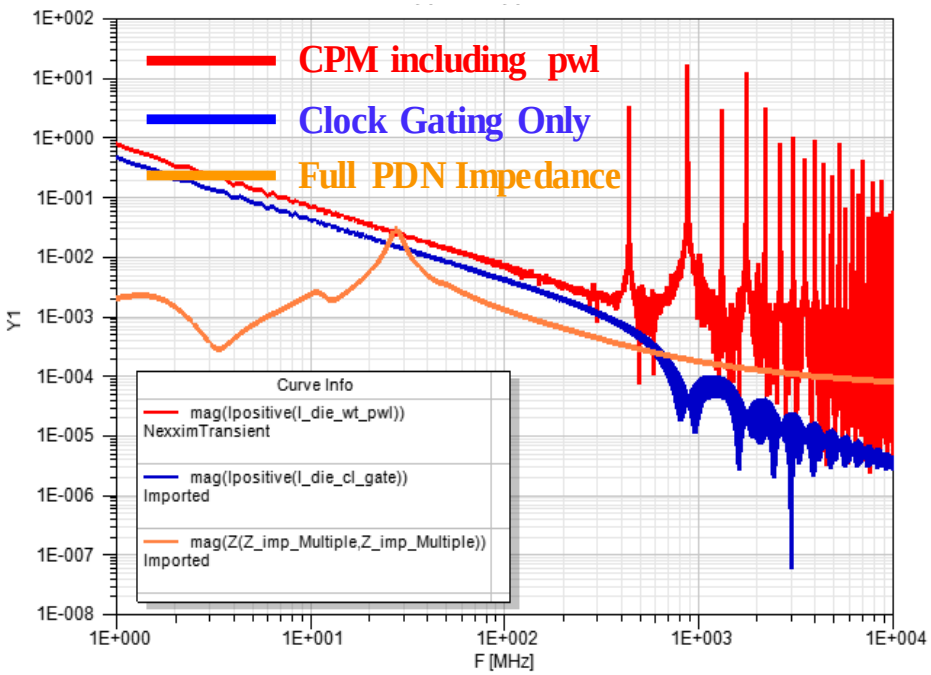


Figure 7. Frequency Domain between Simplified Current Load and Complete Current Load included pwl current profile with Full PDN Impedance Profile

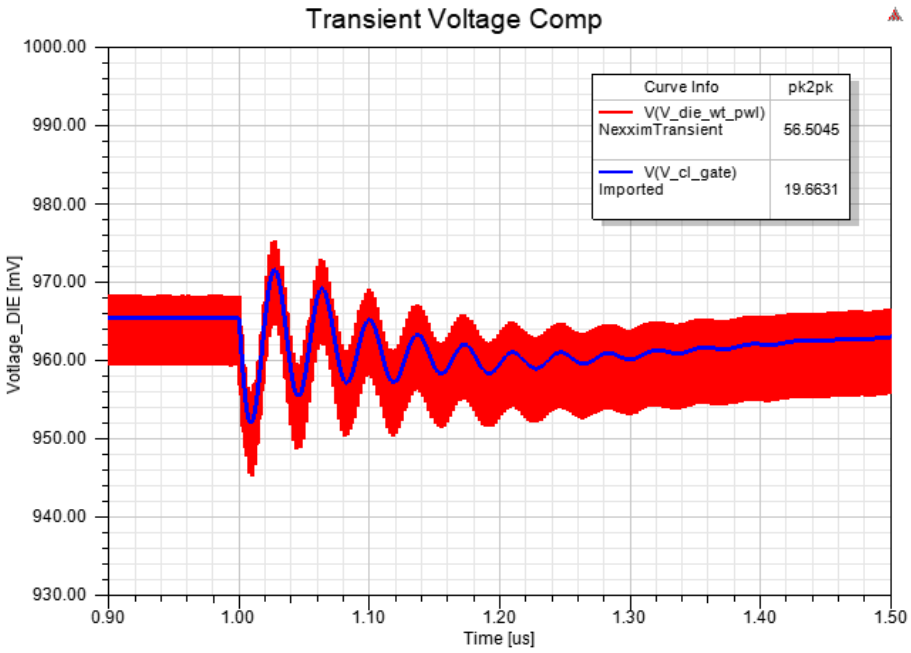


Figure 8. Time Domain Comparison between Simplified Current Load and Complete Current Load included pwl current profile

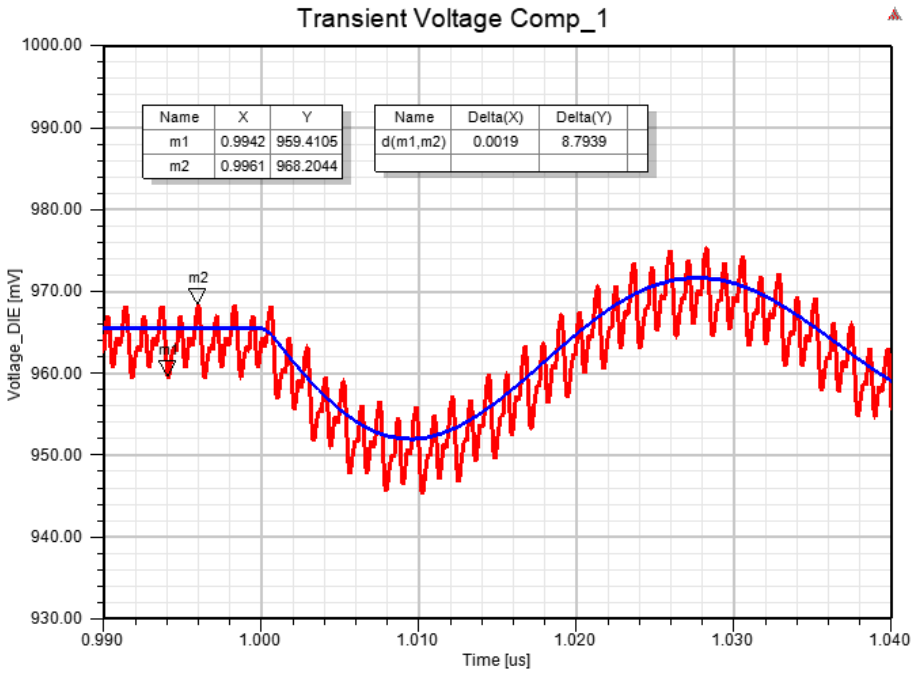


Figure 9. Time Domain Ripple Comparison between Simplified Current Load and Complete Current Load included pwl current profile

1.2. WORST-CASE LOAD SCENARIO TO PDN IMPEDANCE PEAK

To achieve the worst-case current load is an essential part for predicting the maximum voltage noise to supplied chip through the PDN [9]-[12]. When the clock gating sequence is modulating in resonance model with period equal with inverse of the maximum anti-resonance peak, the current spectrum would hit the PDN impedance highest peak as shown in figure 10 to give an enormous voltage noise compared to random mode as shown in figure 11. From comparing to figure 10, random mode have multiple current spectral components, which split the energy from resonance peak at the resonance mode.

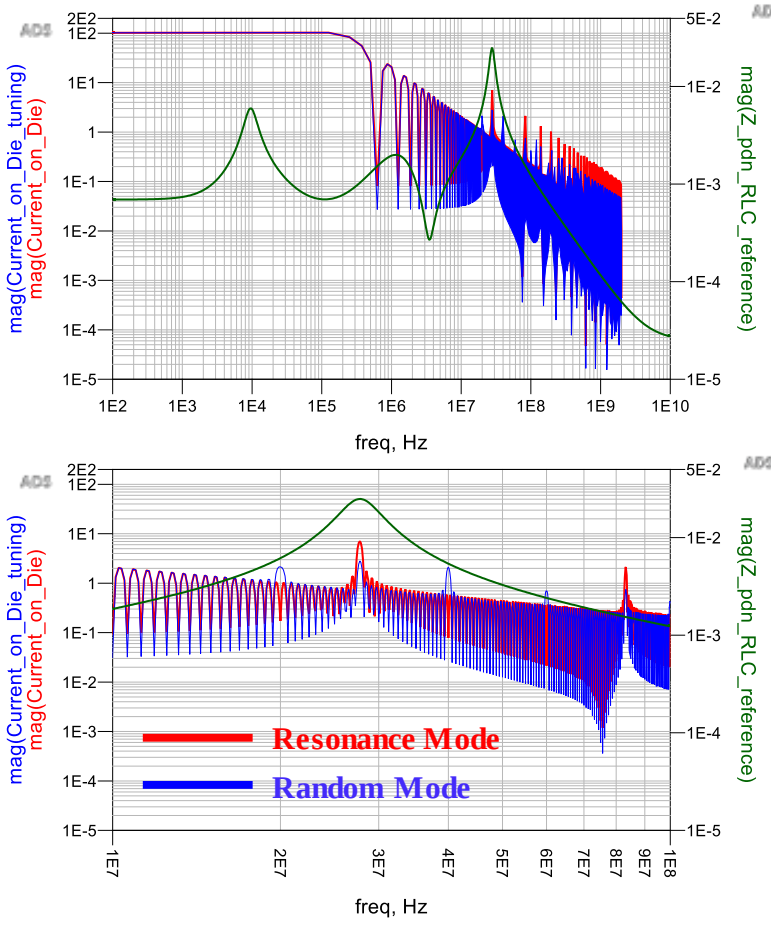


Figure 10. Frequency Domain - Random Mode Current Profile and Resonance Mode Current Profile with Full PDN Impedance Parallel Resonance Peak

Here are the steps for deploying the worst-case to PDN impedance peaks [5]:

1. Cascaded the full PDN impedance and identify the frequency $freq_{peak}$ with the maximum impedance peak;
2. Generate the clock gating current sequence with the period $T_{resonance}$ = 1/ $freq_{peak}$ as resonance model in figure 6;
3. Modulated generated clock gating sequence with time-extended piecewise linear (pwl) current profile together;
4. Exported this worst-case switching pattern CPM profile for noise analysis.

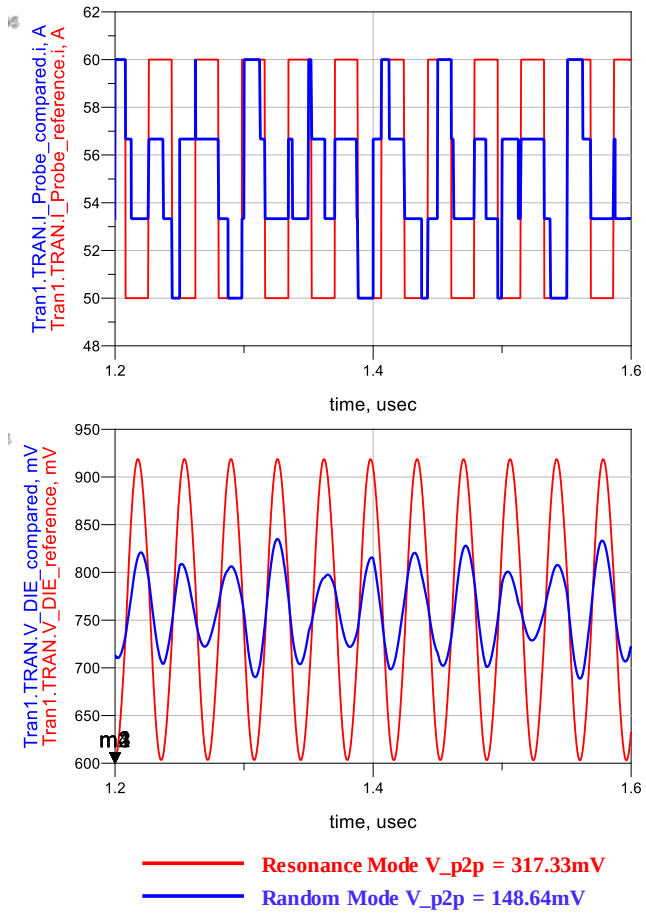


Figure 11. Time Domain - Random Mode and Resonance Mode Current Profile and Voltage Response Comparison

2. PHYSICS-BASED EQUIVALENT CIRCUIT MODEL

2.1. MODELING BASED ON CURRENT PATH PHYSICS

The power delivery network is mainly composed of these interconnecting structures including PCB and PKG to deliver power from VRM supply source to chip destination. The modeling on these passive structures is a critical topic for research for many years [15-21]. Based on the current path physics, the modeling of PCB could be divided into four segmentations as shown in figure 12., including the IC interconnection inductance L_{PCB_IC}, the DECAP interconnection inductance L_{PCB_DECAP}, the inductance of the current crossing the power plane area L_{PCB_PLANE} and the mounting inductance from DECAP attaching to the PCB top plane L_{PCB_IC}. The total equivalent inductance L_{PCB_EQU} is the sum of all segments inductance given by equation (3.1). The specific inductance would be calculated based on the DECAP placement locations.

$$L_{PCB\_EQU} = L_{PCB\_IC} + L_{PCB\_DECAP} + L_{PCB\_Plane} + L_{above} \qquad (3.1)$$

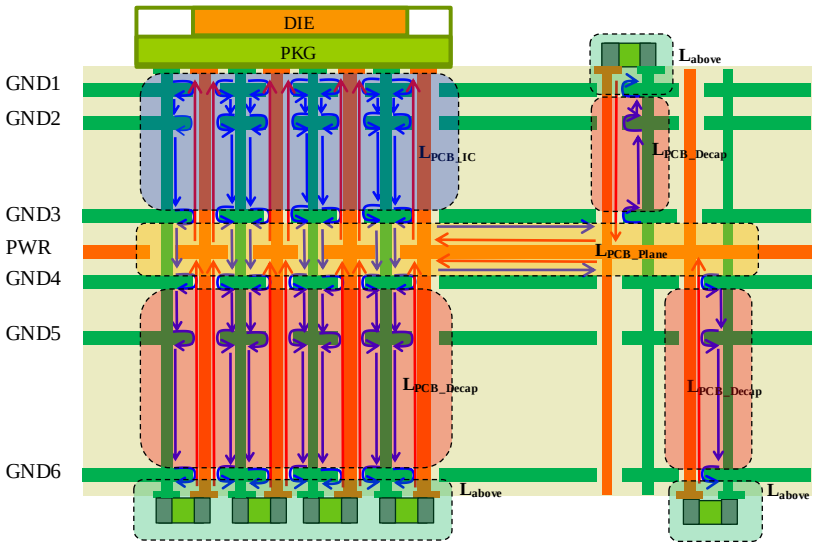


Figure 12. Geometry Segmentation based on Current Path

2.1.1. Modeling of Printed Circuit Board. To decrease the PDN impedance in middle frequency range that dominant by the equivalent inductance L_{PCB_EQU}, the DECAP is the key elements. There are three categories of DECAP based on the DECAP placement locations as shown in figure 13.

1) DECAP on bottom layer and directly under the IC;
2) DECAP on bottom layer but away from the IC;
3) DECAP on top layer and side of the IC.

The equivalent circuit parameters was extracted based on above categories for a specific PCB casa as shown in figure 14, with left ports for connecting to PKG model, DECAP models on bottom and top layers of PCB. The presented circuits could be used in both frequency domain and time domain analysis with fast iteration. Most importantly, these provide flexible ports for DECAP from different location and physical metrics on these geometries. It could be desirable for doing PI margin analysis and design variation analysis from the equivalent circuit model.

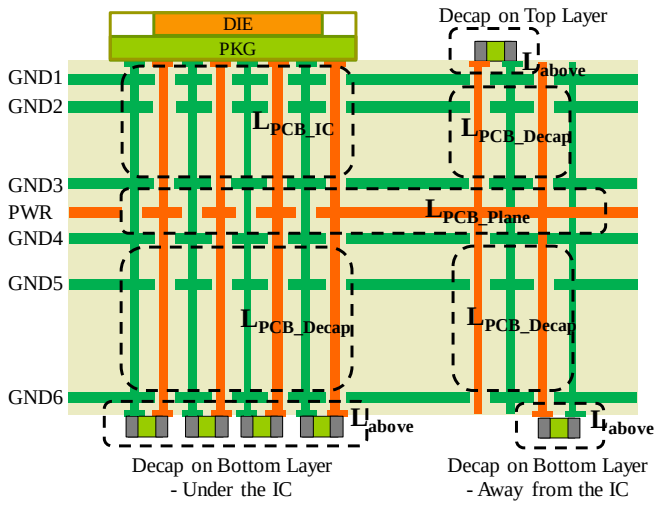


Figure 13. PCB Modeling Based on DECAP Placement Locations

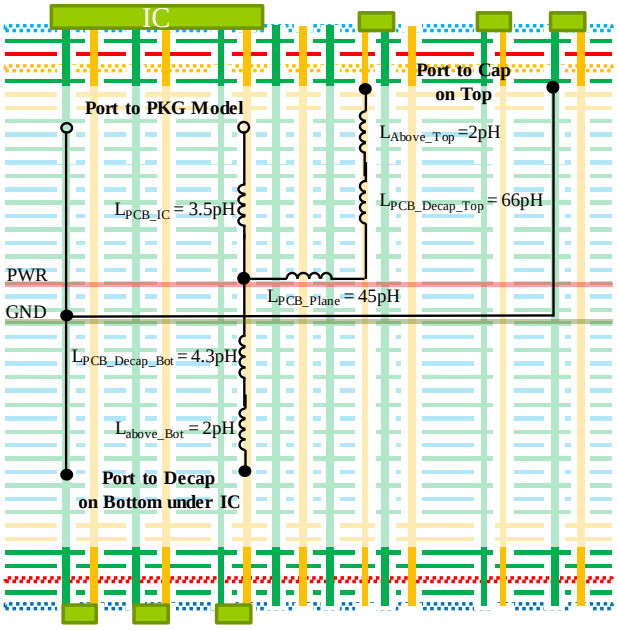


Figure 14. Equivalent Circuit Model Extraction for PCB

2.1.2. Modeling of Chip Package. To decrease the PDN impedance in middle-higher frequency range that dominant by the equivalent inductance of the package, the DECAP on package would be helpful. There are only one DECAP on top layer and side of the DIE as shown in figure 15. The equivalent circuit parameters was extracted for the example case as show in figure 16, the ports are connected to DIE model, PCB model and DECAP model on top layer of package.

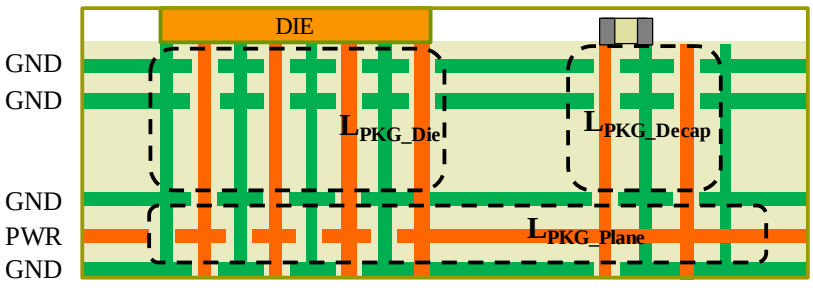


Figure 15. PKG Modeling Based on DECAP Placement Locations

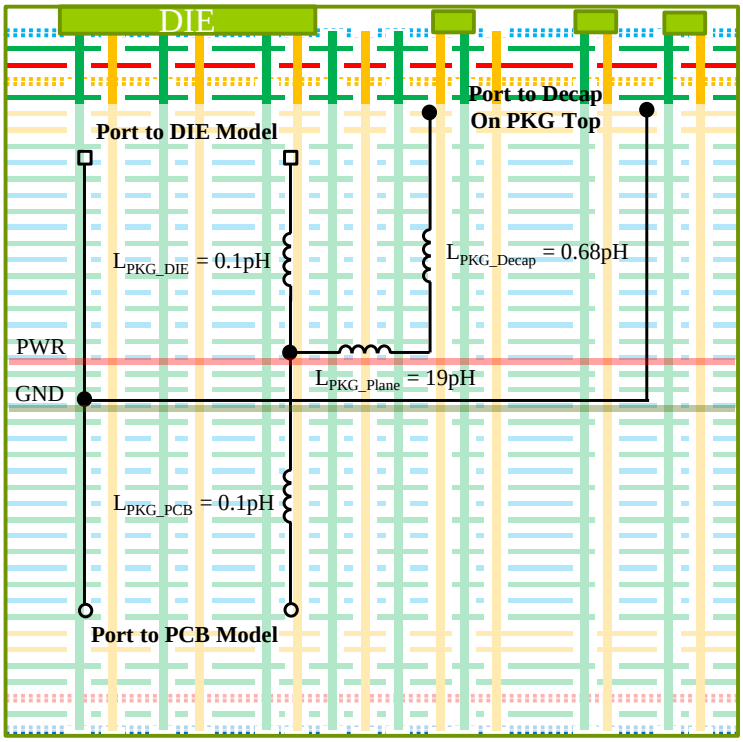


Figure 16. Equivalent Circuit Model Extraction for PKG

2.2. END TO END PDN CASCADED EQUIVALENT CIRCUIT MODEL

With extracted PCB and PKG circuits elements, these can be cascaded to VRM model and CPM model from end to end for modeling the full PDN impedance as shown in figure 17. The impedance from equivalent circuit can be correlated with S-parameter model that was extracted from other commercial tool for full structure extraction as shown in figure 18. These resonance peaks in the impedance are related to the Q factor of RLC tank circuits. The accurate extraction on DC resistance of each segments are also critical for these peak amplitude. Once these equivalent circuit models for PCB and PKG are extracted and validated, they would be available for extending to time domain transient simulation for predicting the voltage noise on-die.

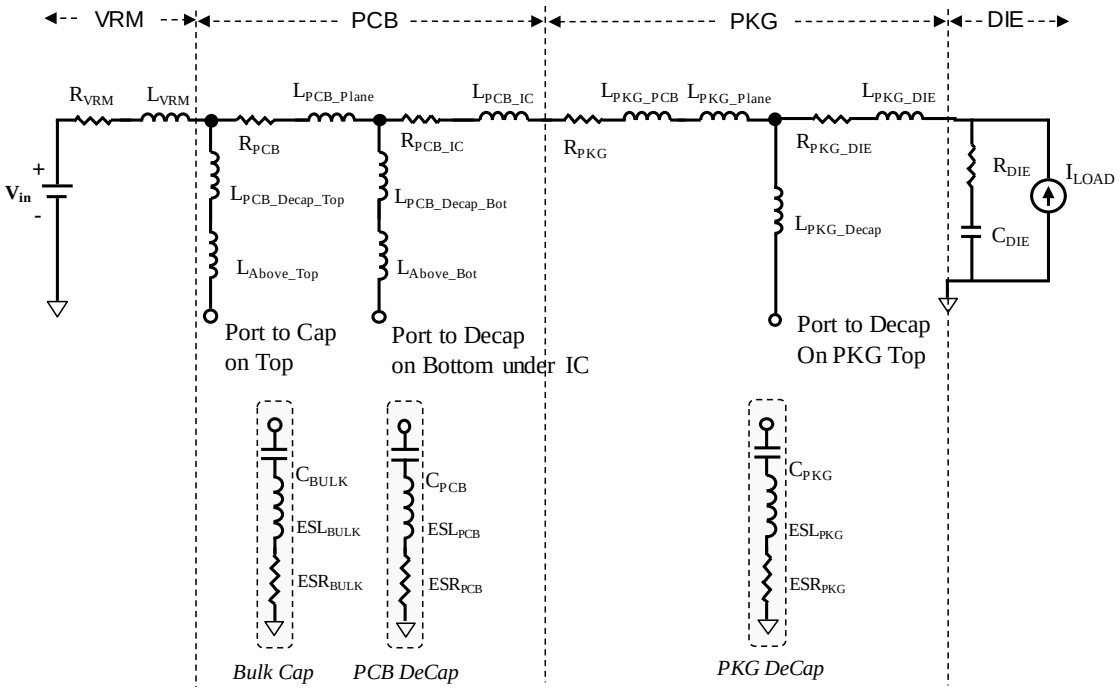


Figure 17. Cascaded Equivalent Circuit Models from End to End

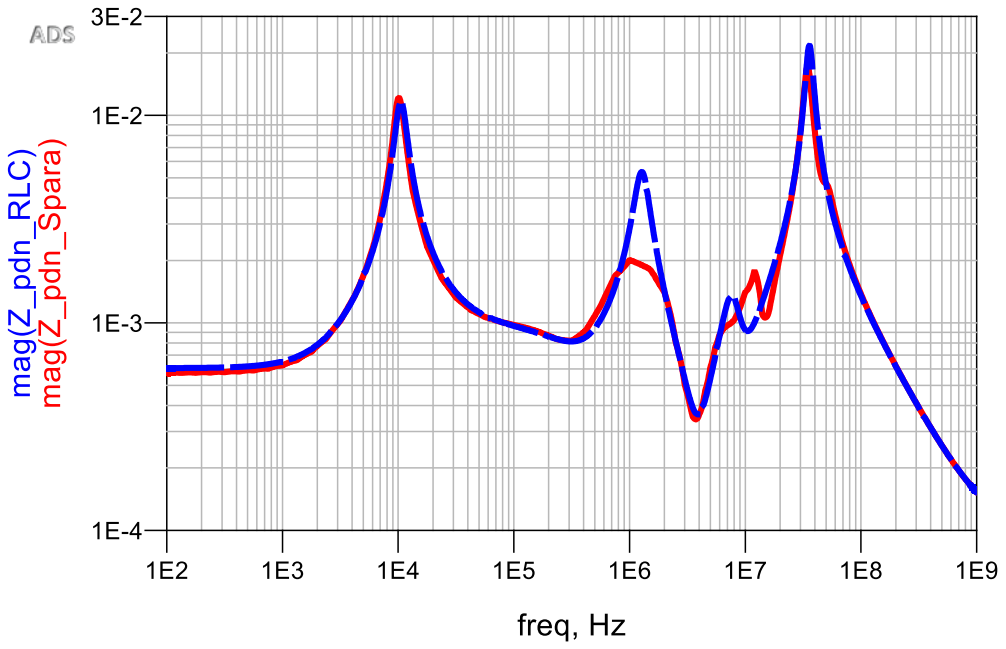


Figure 18. Correlation between S-parameter Model and Equivalent Circuit Model

3. SYSTEM LEVEL TRANSIENT ANALYSIS

3.1. TRANSIENT SIMULATION WITH FULL PDN

As mentioned in the introduction chapter, how to validate the full PDN design in time domain response for voltage noise is the ultimate goal for optimizing the full PDN. For an appropriate transient response prediction, the VRM model is an integral part of transient simulation with end-to-end power delivery network. The role of the VRM model provide not only the supply voltage to the system chip, but also compensation for dc voltage offset and lower frequency current fluctuation. The VRM model accuracy directly decides if predicted voltage response could qualify or fail with the supply design specification.

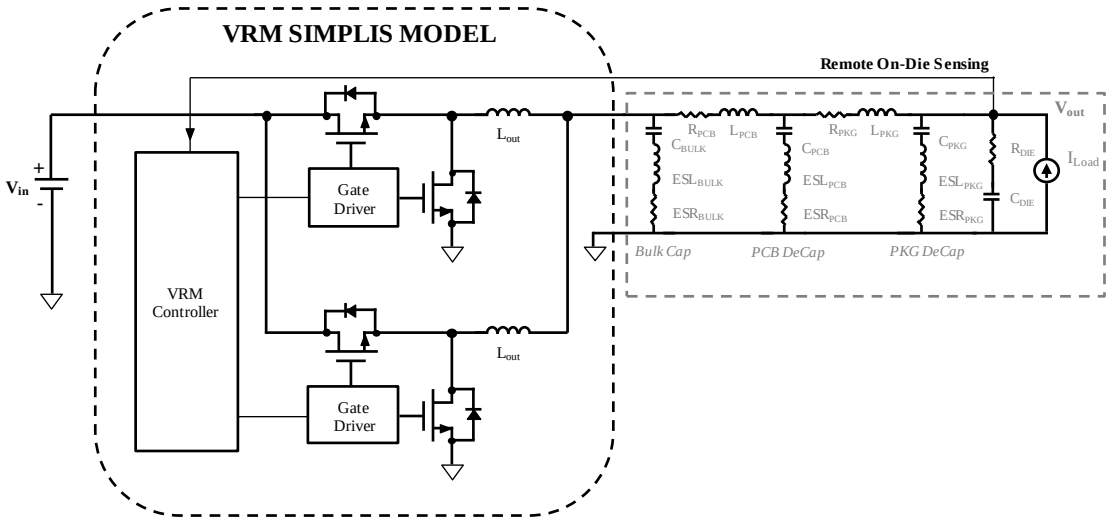


Figure 19. Two-Phase Synchronous Buck Converter Small Signal VRM Model in SIMPLIS with PDN Equivalent Circuits Models and Load Current

The VRM provider in the industry provides well-correlated small signal model in SIMPLIS tool from their product line. This vendor-provided VRM model would be a good choice from system level power integrity transient validation. However, the s-parameter

model or broadband spice model of interconnects networks including PCB and PKG cannot be compliable with small signal model in SIMPLIS tool. The methodology using physics based approach was presented in previous chapter to model interconnects networks by the equivalent circuit models. These equivalent circuit models can be cascaded with small signal model in SIMPLIS tool for transient simulation and validation.

3.1.1. Spike, Droop and Ripple of Voltage Response on DIE. The voltage response of full system PDN that measured at Die is consisted of voltage spike, voltage droop, and voltage ripple as shown in figure 20. These three main ac noise would be the critical transient response, which need to suppress from optimizing physical parameters of the power delivery network. How to minimize these three types of voltage response is the design goal of the full system power integrity.

The identification on these three types of noise presented in table 4.1 from different perspectives of time lasting duration, frequency response range, and dominant capacitor in corresponded frequency range. From understanding in both time domain and frequency domain, the noise peak optimized to meet the design spec for the chip supply voltage.

The first voltage droop refers to voltage spike happens in nanosecond level, which can optimize from higher to middle frequency range by decoupling capacitors. The second voltage droop refers to voltage droop come into microsecond level, which can optimize from middle to lower frequency by bulk capacitors and decoupling capacitors with larger value. The voltage ripple noise caused from load switching and VRM MOSFET switching, the ripple by VRM MOSFET switching will be firstly concerned for system level PDN optimization. The load switching on die would optimize from on-die decoupling capacitors.

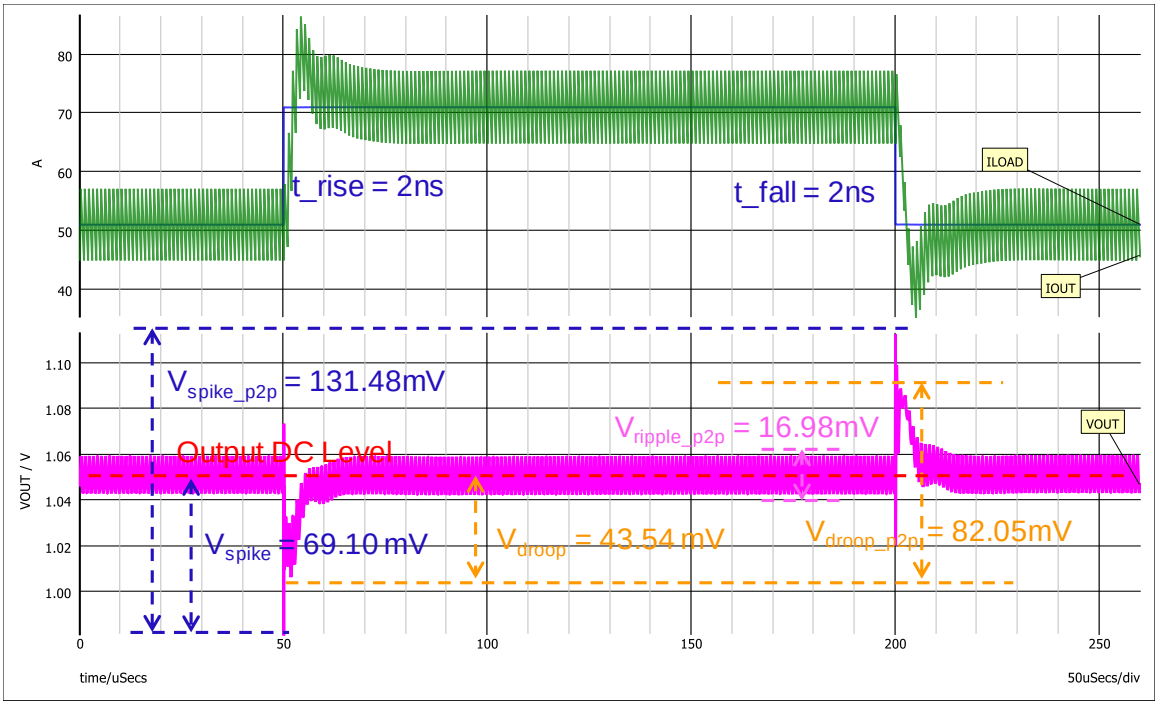


Figure 20. Identify on Spike, Droop and Ripple of Voltage Response on DIE

Table 2. Supply Voltage AC Noise and Design Spec

	V_{Spike}	**V_{Droop}**	**V_{Ripple}**
Time Duration	In nSeconds	In uSeconds	In uSeconds
Response Frequency	Middle Frequency	Lower Frequency	VRM n Phase * Switching Freq
Dominant Capacitors	Decoupling Cap	Bulk Cap and DeCap	Decoupling Cap
Voltage Design Spec	3.0 % 30 mV	3.0 % 30 mV	1.0 % 10.0 mV

3.1.2. Output Impedance of Voltage Regulator Module (VRM). The switching mode power supply is main application for voltage supply to core power of system chip. For example, the synchronous buck converter shown in figure 19 is a common topology for voltage step-down application. When gate driver of the MOSFET switched with different duty cycle, output voltage from VRM provide scaled voltage to supplied chip. When looking from the chip die, the VRM output impedance is dominant at lower frequency impedance from dc to several kHz range of full system PDN impedance as shown in figure 1.3 and figure 21.

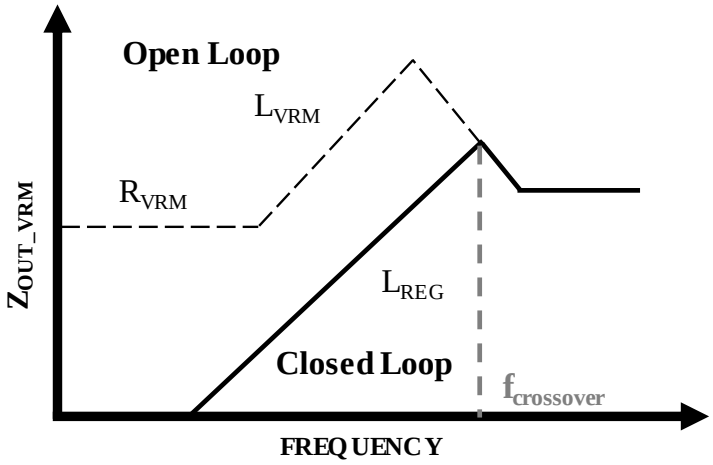


Figure 21. Comparison between OL and CL Output Impedance

The VRM output impedance varies with different working status for different supply to it and transient load on it. The output impedance generally divided into two categories of open loop output impedance and close loop output impedance based on the operation status. The feedback loop of the VRM have limitation to respond on current load change by the bandwidth of operational amplifier circuits in compensator. In fast current load changing, the VRM compensation circuit would not work for suppressing the voltage

noise response. The VRM that seen by PDN and load is directly as MOSFET turn-on resistance R_{DSON} and output inductor of the VRM.

Thus, a two-element linear RL model as below can give VRM output impedance in open loop:

$$Z_{OUT\_OL} = R_{VRM} + j\omega L_{VRM} \tag{4.1}$$

Where, Z_{OUT_OL} is the open loop output impedance of the VRM, R_{VRM} is the equivalent resistance of high-side (HS) and low-side (LS) MOSFET turn-on resistance, L_{VRM} is the can be equivalent inductance of all phase output inductance for the VRM.

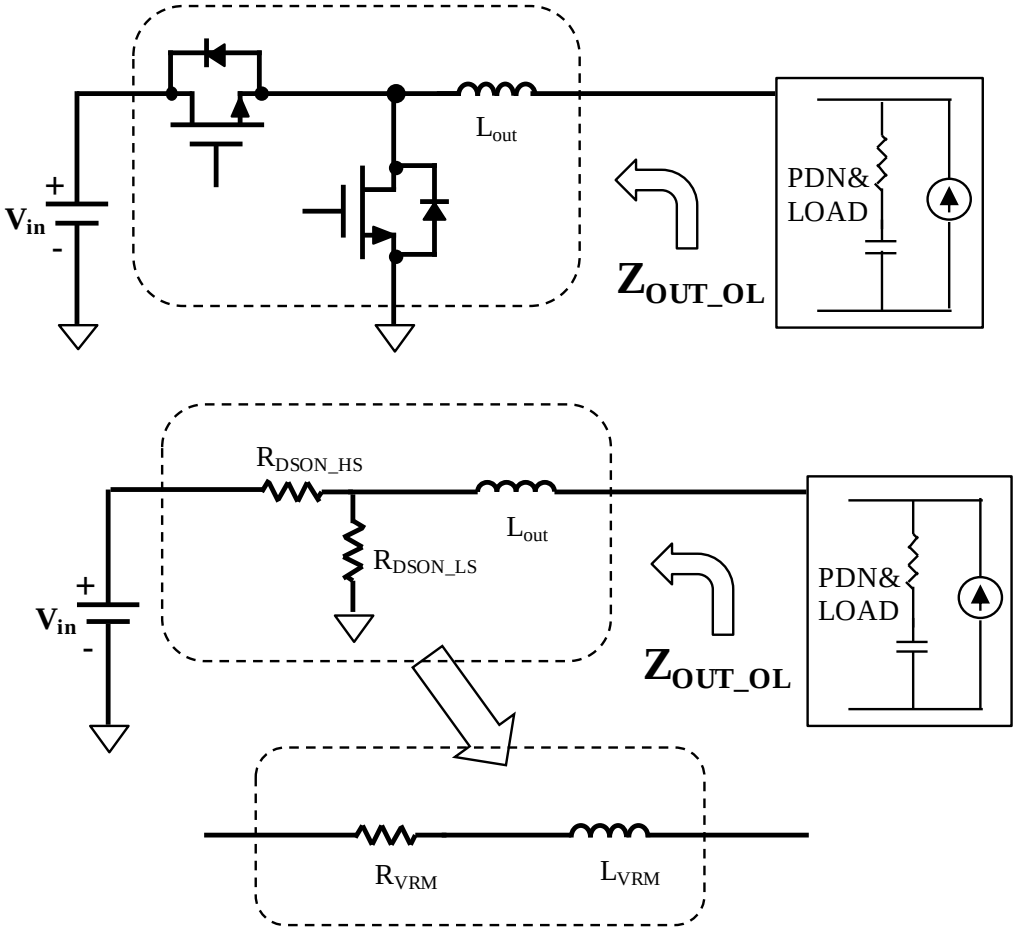


Figure 22. VRM Open loop (OL) Output Impedance

Due to negative feedback, output impedance in close loop responses as inductive behavior to pull down the output impedance of the VRM. The output voltage modulates to lower level voltage response for supplied device [2].

$$Z_{OUT\_CL} = \frac{Z_{OUT\_OL}}{1+G_p(s)*G_c(s)} = sL_{REG} \tag{4.2}$$

Where, $s = j\omega = j \cdot 2\pi f$, Z_{OUT_CL} is the close loop output impedance of the VRM, $G_p(s)$ is the feedforward gain of the VRM, $G_c(s)$ is the gain of feedback circuit, L_{REG} is the approximate equivalent inductance by a simple inductor with the value given by:

$$L_{REG} = \frac{Z_{OUT\_OL}/s}{1+G_p(s)*G_c(s)} \tag{4.3}$$

The close loop impedance would be varying for different conditions with varied supply voltage to load current change. The equivalent inductance L_{REG} would also depend on the approximately extraction method and points frequency. The simple inductor model and extended three elements model discussed in next session.

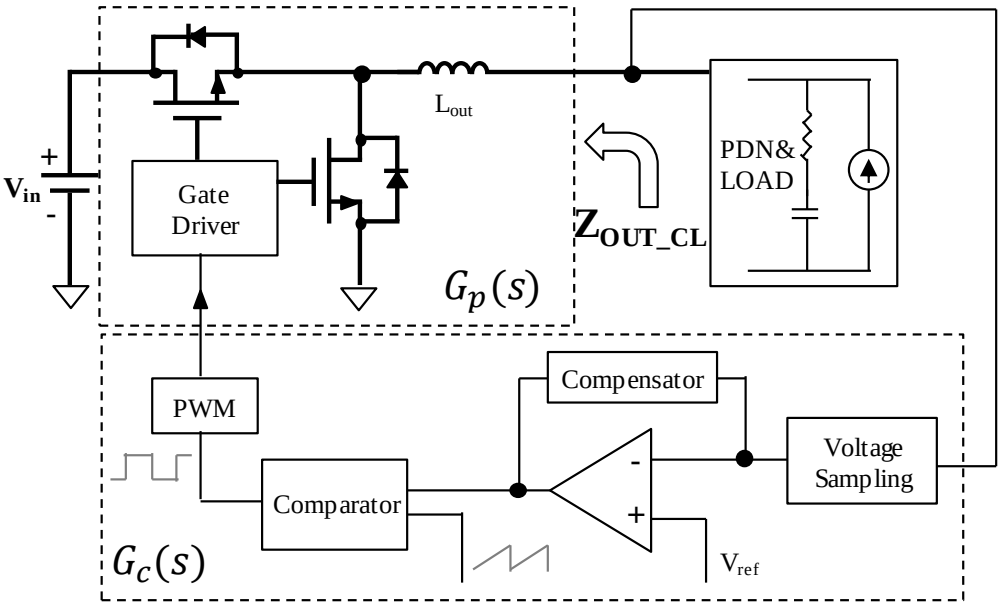


Figure 23. VRM Closed loop (CL) Output Impedance

3.2. VRM MODELS TRADEOFF FOR POWER INTEGRITY ANALYSIS

3.2.1. Various VRM Models Extraction and Response. This session provided comparison between different VRM models including small signal model, two-element RL model for open loop, simple inductor model and three-element for close loop.

The small signal models in SIMPLIS is a common analysis technique for VRM manufacture provider to design the power supply. The correlated and tuned model in encrypted version can be requested from VRM vendor. The SIMPLIS small signal models approximate the behavior of the switching mode power supply containing nonlinear device with linear equations. The small signal models can modeling the nonlinear effects including the discrete sample and hold effect of the switching mode power supply.

Based on the small signal models, the open loop and close loop output impedance could be accurately extracted from the SIMPLIS as shown in figure 24. These output impedance are showing the similar response as shown in figure 21. Other three linear VRM models would be extracted based on the open loop and close loop output impedance then compared their voltage response in the time domain to understand these models.

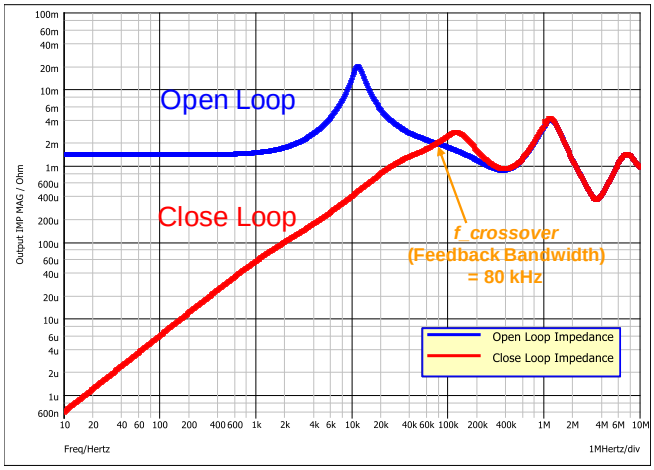


Figure 24. Extracted VRM Output Impedance from SIMPLIS Small Signal Model

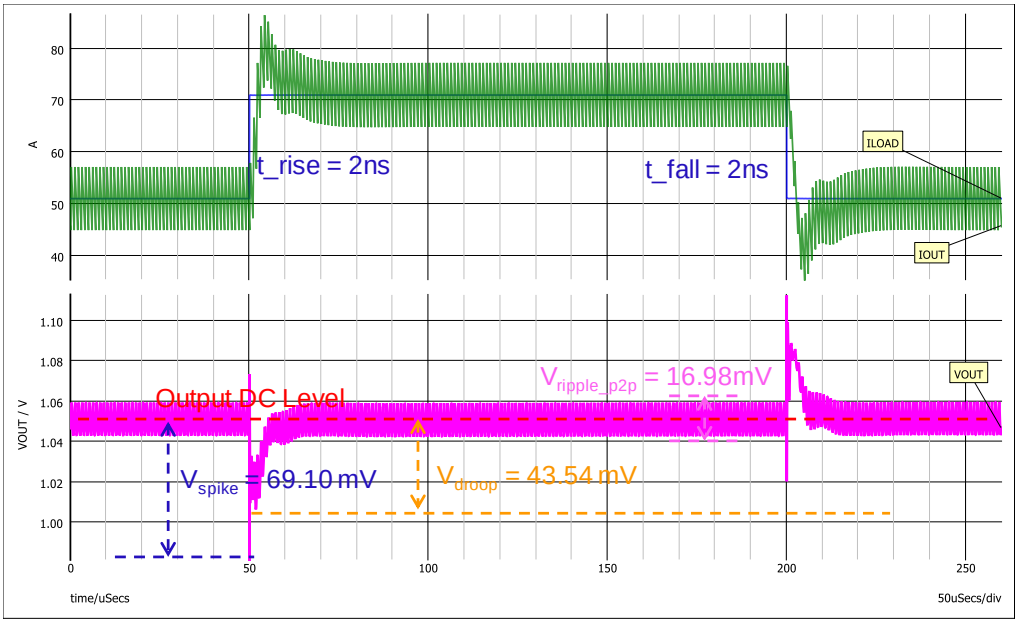
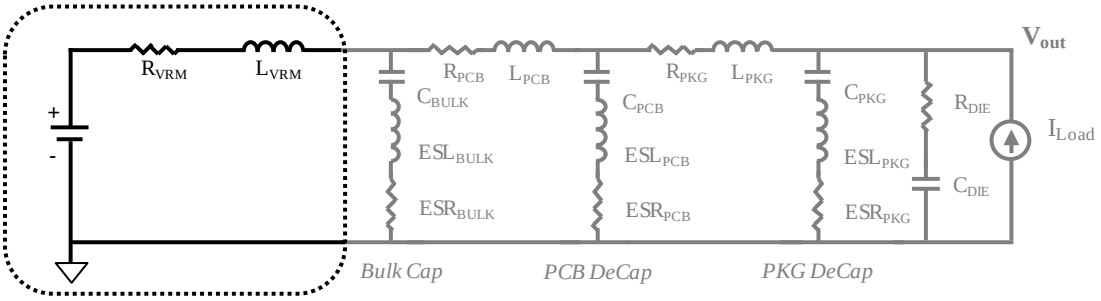


Figure 25. Voltage Response by VRM Small Signal Model

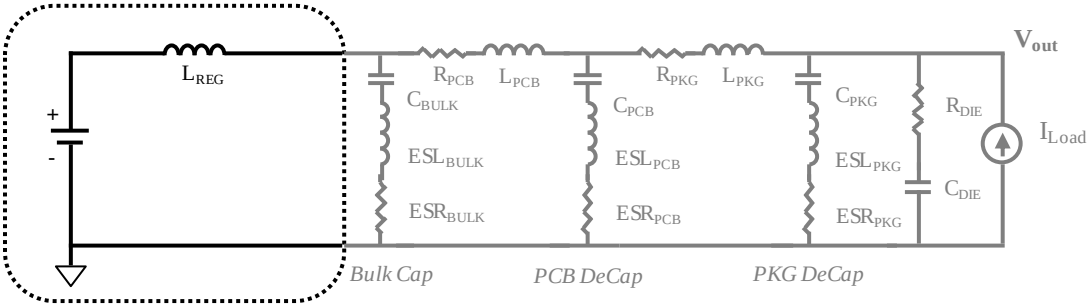
In power integrity analysis, the lumped two-element RL model is a common method to describe the impedance from the VRM as shown in figure 26..(a). From table 4.3, the parameters for the two-element RL model for open loop output impedance is shown as R_{VRM} and L_{VRM}, which parameters can be calculated by following the methods described in equation (4.1) and figure 22. The two-element RL model can be correlated with SIMPLIS extracted model as shown in figure 27. In addition, voltage response presented the approximately same amplitude for the first voltage spike, two-element RL model presented 66.06 mV compared to 69.10mV from voltage spike by small signal model in figure 28.

However, the second voltage droop was over-estimated to 113.84 mV comparing with 43.54 mV from voltage droop by small signal model in figure 25. Therefore, this lumped two-element RL model can predict the first voltage spike that response in higher-middle frequency range, but cannot accurate predict the second voltage droop that response

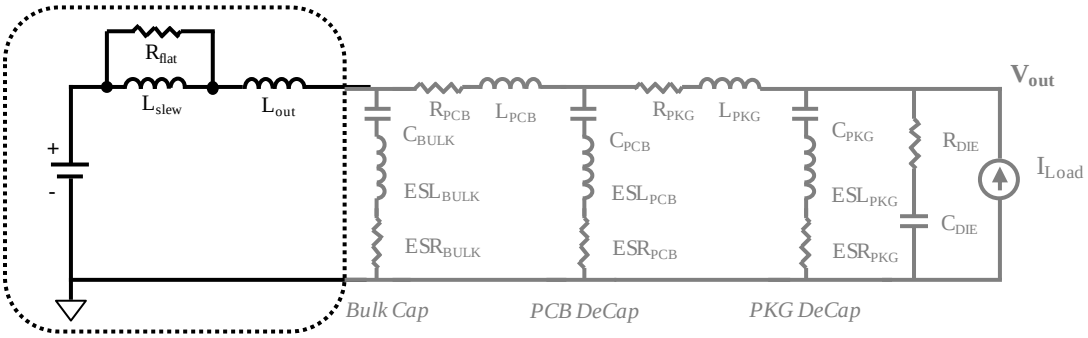
in middle-lower frequency range. Because the VRM model will affect the impedance in lower frequency by feedback loop control to change the PWM pulse width for modulating the output voltage. From frequency impedance perspective, the feedback loop control will change the loop gain to change the VRM output impedance, which refers to close loop impedance.



(a) Two Element RL Model



(b) Simple Inductor Model



(c) Three Element RLL Model

Figure 26. Typical Linear VRM Model

Table 3. Two Element RL Model - Extracted Parameters

Parameters	Value	Units
R_{VRM}	0.825	mOhm
L_{VRM}	75	nH

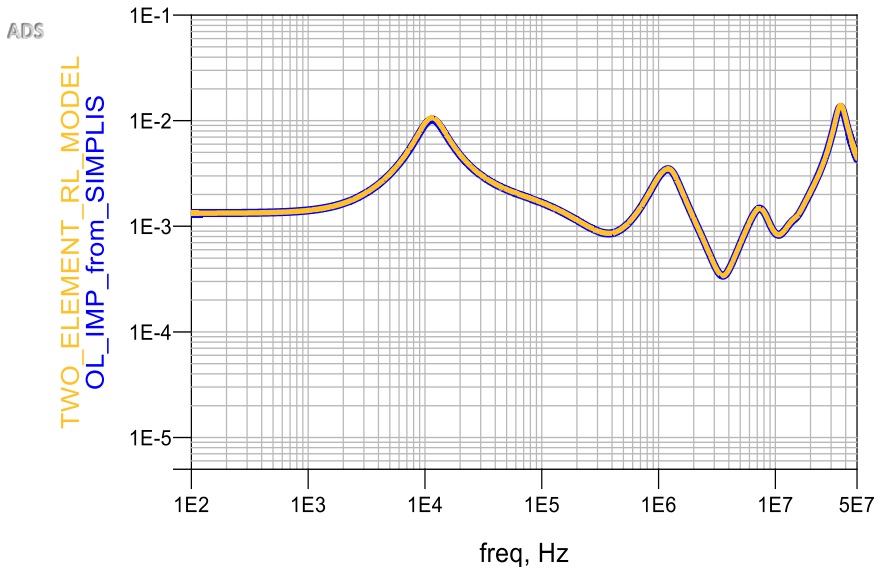


Figure 27. Correlated Model between Two Element RL Model and SIMPLIS Model

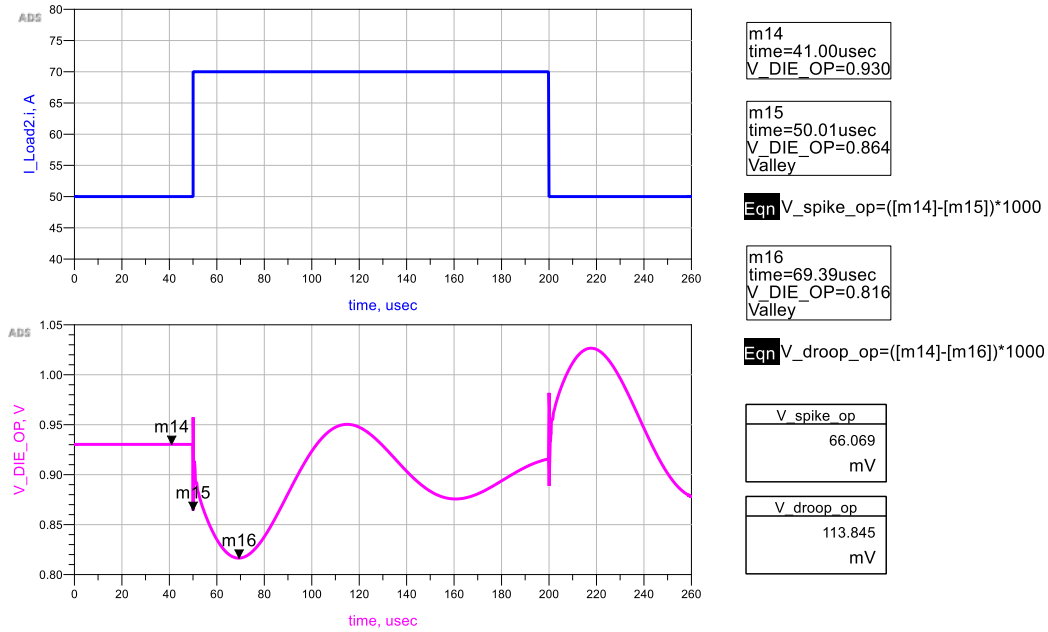


Figure 28. Voltage Response by Extracted Two-Element RL Model

Table 4. Simple Inductor Model - Extracted Parameters

Parameters	Value	Units
L_{REG}	2.8	nH

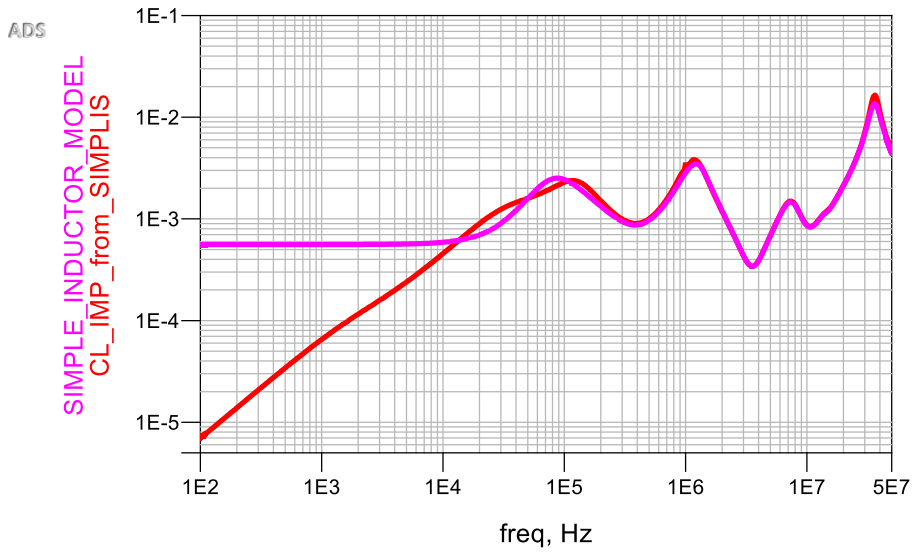


Figure 29. Correlated Model between Simple Inductor Model and SIMPLIS Model

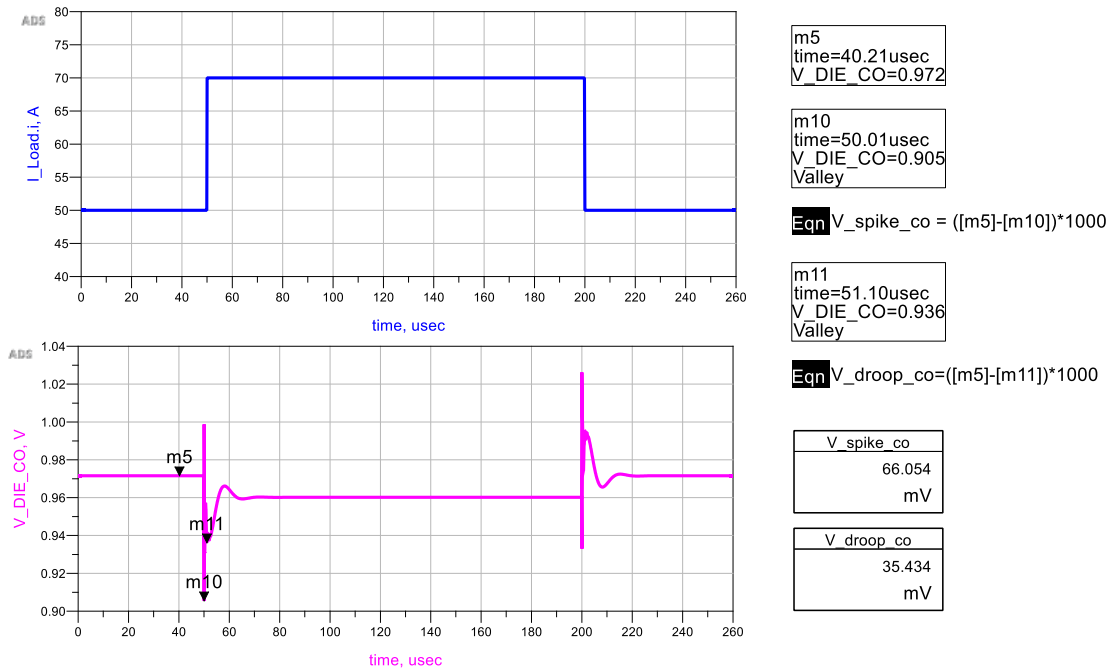


Figure 30. Voltage Response by Extracted Simple Inductor Model

Table 5. Three-Element RLL Model - Extracted Parameters

Parameters	Value	Units
R_{flat}	0.33	mOhm
L_{slew}	2.50	nH
L_{out}	2.50	nH

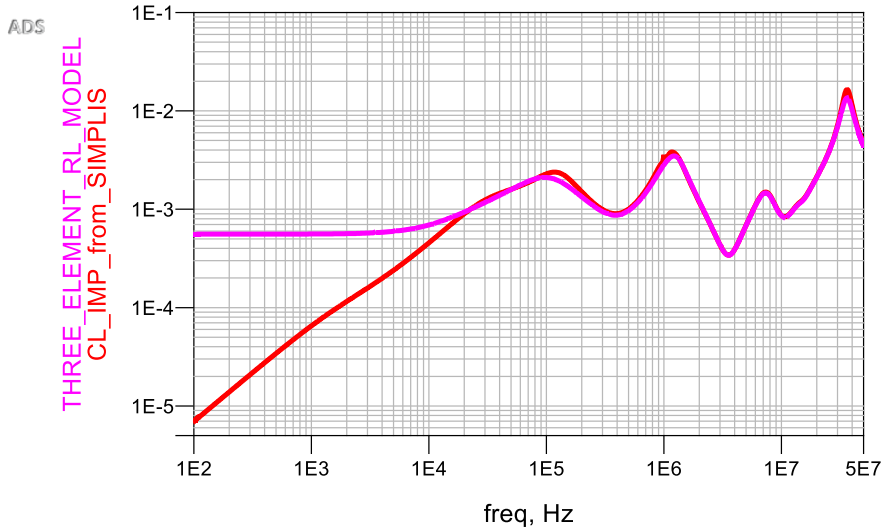


Figure 31. Three-Element RLL Model .vs. SIMPLIS Model

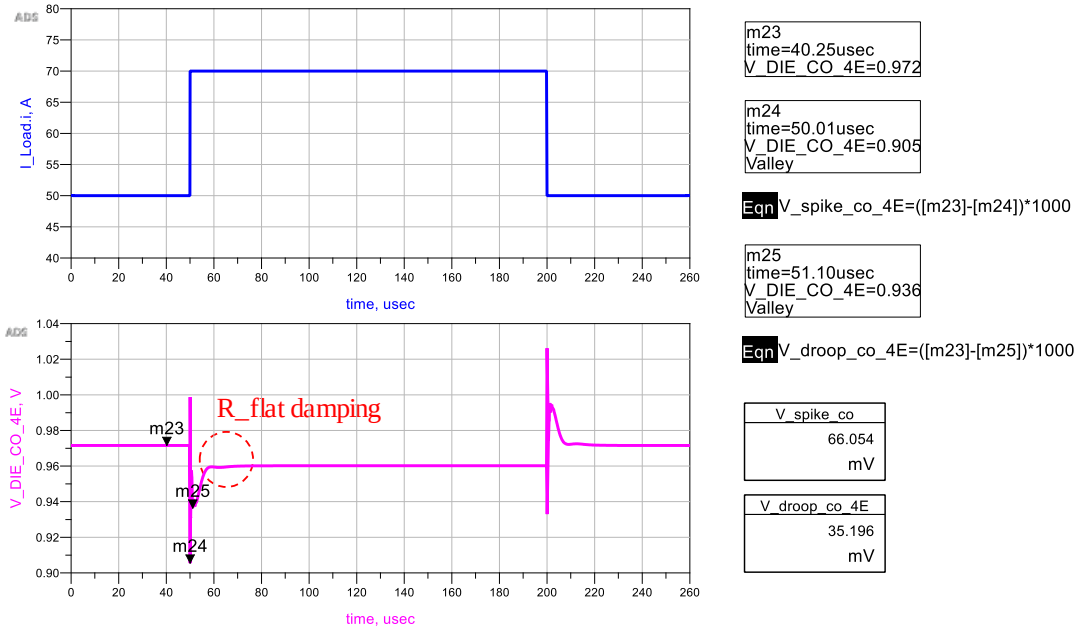


Figure 32. Voltage Response by Extracted Three-Element RLL Model

Table 6. Transient Response Comparison between Four Different VRM Models

	Small Signal Model	2-Element Linear RL	Simple Inductor	3-Element Linear RL
DC Drop	0 mV	70mV	28mV	28mV
$\mathbf{V_{Spike}}$	69.10mV	66.06 mV	66.05mV	66.05mV
$\mathbf{V_{Droop}}$	43.54 mV	113.84 mV	35.43 mV	35.20 mV
$\mathbf{V_{Ripple}}$	16.96 mV	-	-	-

3.2.2. Summary on VRM Model Tradeoff. From these compared results with different VRM models, the tradeoff on different VRM model is discussed in table 7 from different perspectives based on the results for transient response comparison between four different VRM models from table 6. We could also conclude these following guidelines for perform the system-level power integrity analysis:

1. Time domain first response voltage spike is not directly relating to the VRM portion impedance, and these VRM models show the similar results;
2. Time domain second response voltage droop is directly relating to the lower frequency portion VRM impedance. The VRM small signal model can provide the most accurate voltage droop; the simple inductor and three-element RLL model can be approximately predicting the voltage droop.
3. These simplified linear VRM models cannot predict the voltage ripple caused by VRM MOSFET switching, but the small signal model can.
4. The linear model extracted from close loop VRM impedance is a good choice for impedance optimization in frequency domain; the small signal model would be better choice for voltage response validation in time domain.

Table 7. Tradeoff on VRM model for System Level PI Simulation

	Small Signal Model	**2-Element Linear RL**	**Simple Inductor**	**3-Element Linear RLL**
Implementation Complexity	Moderate	Low	Low	High
Applicable Input/Load	Dynamic	Limited	Limited	Limited
VRM Output Impedance	Both OL and CL	Open Loop	Closed Loop	Closed Loop
Gain/Phase Stability Analysis	Supported	No	No	No
FD Impedance Optimization	Limited	Overdesigned	Supported	Supported
TD Response Accuracy	High	Low	Moderate	Moderate

3.3. APPLICATION FOR SYSTEM LEVEL PI OPTIMIZATION

The conventional method to design power delivery network is by controlling the impedance under a metrics called target impedance [1], which assumed to be set as the ratio of the maximum tolerated voltage ripple to current change in the step by applying ohm's law in frequency domain. The example can be calculated for previous case by:

$$Z_{Target} = \frac{Voltage\ Ripple}{Current\ Change} = \frac{1V\ * 3\%}{20A} = 1.5mohm$$

However, this target impedance can no longer be satisfied the broadband frequency for modern process with lower voltage and larger dynamic current. Then many authors

identified improved target impedance with IC transient current [13] and modified target impedance with modeling surging current [14]. The example can be calculated for previous case by:

$$f_{knee} = \frac{0.35}{T_r} = \frac{0.35}{2ns} = 175Mhz, \quad Leq = T_r = 2nH$$

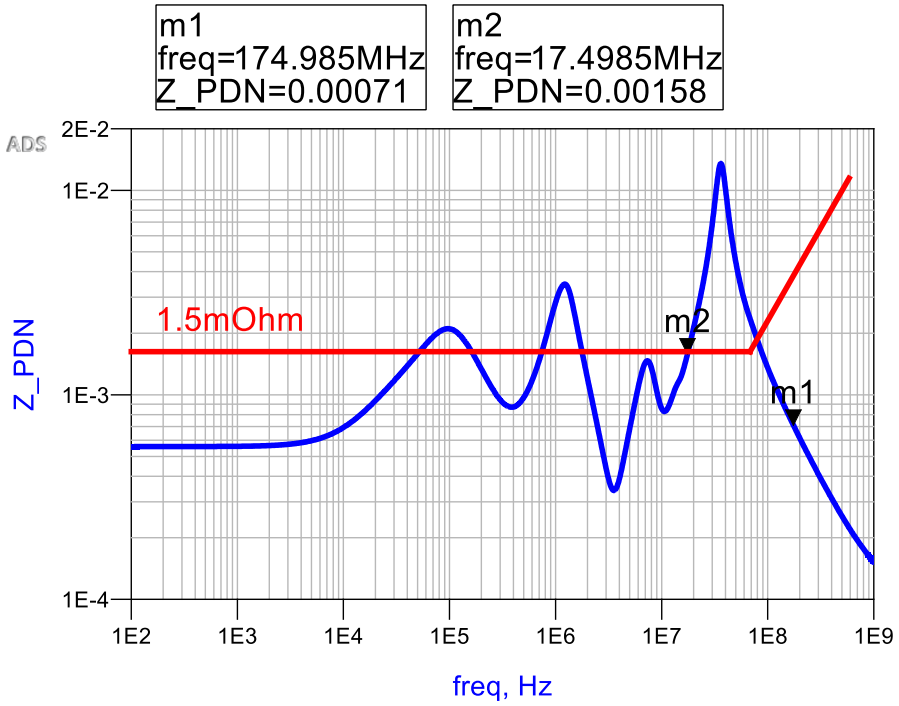


Figure 33. Extremely difficult to meet above target impedance on system level

Nevertheless, these target impedance are extremely difficult to be met by system level optimization as shown in figure 33. The anti-resonance peak caused by package inductance and on-die decoupling capacitor would not be suppressed only with on-PCB and on-PKG decoupling capacitors to meet these target impedance. In addition, these metrics for system level PDN design would provide an over-design solution and even cannot get an achievable solution on system level PDN optimization. How to define better

metrics for PDN design would be critical on avoid these over-design by applying a novel definition on target impedance for system-level achievable solution and considering worst-case current scenario.

3.3.1. Hybrid Target Impedance. For core power of system chip, the current profile spectral components were identified in previous chapter by classifying with operation pattern and dominant frequency range. As show in figure 34, these current profile spectral components were listed with corresponded frequency to the full PDN impedance.

Based identified current components, the continuous target impedance in sectional type can be calculated based on conventional method for lower and middle frequency. Then breakpoint for this continuous target impedance are based on VRM output voltage switching ripple frequency, which usually need a lower impedance for smaller ripple noise as shown in figure 35.

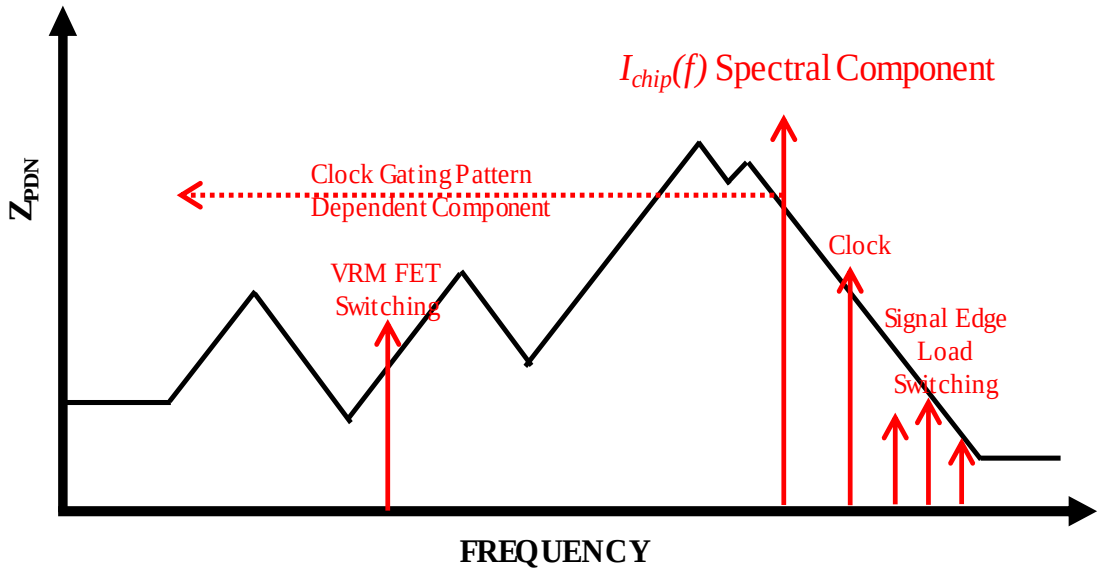


Figure 34. Full PDN Impedance and Current Profile on DIE

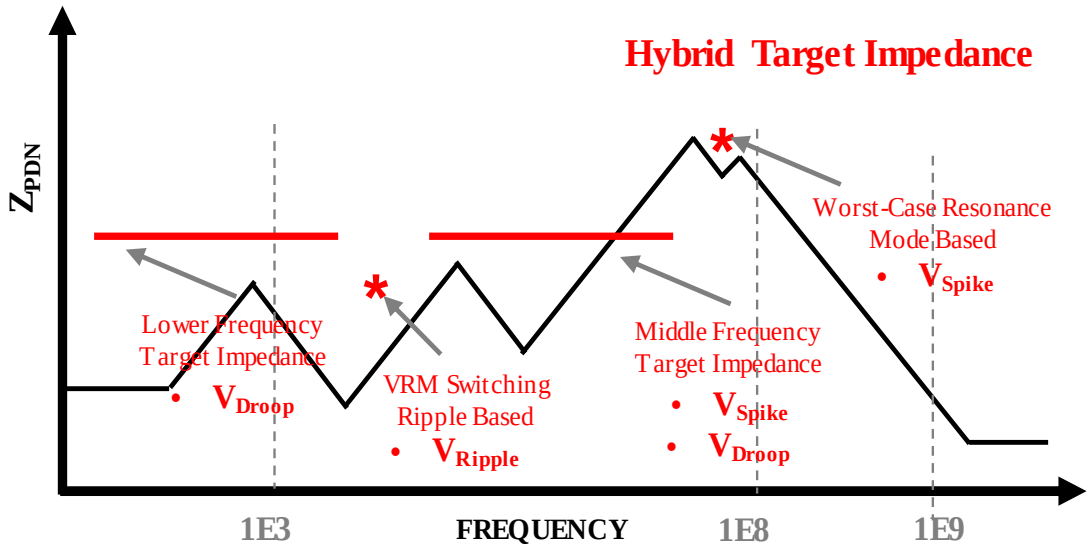


Figure 35. Current Profile-based Discrete and Continuous Target Impedance

Above the middle frequency, that would be limited with another discrete impedance point for considering the worst-case scenario resonance peak. This impedance point would be larger than the continuous target impedance but it can give a limitation on impedance peak based on worst-case current harmonic components. These two discrete impedance points in hybrid target impedance either can be achieved from previous design data for a qualified product, or can be calculated based on the estimation for these current components and requirement to tradeoff between performance and cost.

The hybrid target impedance can help to avoid the over-design problem, and provide specific solutions for each voltage response noise including the voltage spike, voltage droop and voltage spike. Most important, these well-defined hybrid target impedance with continuous target impedance in sectional type and discrete target impedance for specific point would give a reasonable constrain for get an achievable solution in fast convergence.

3.3.1. An Example for FD Optimization and TD Validation. Finally yet importantly, a PDN optimization example was given in this session to apply the hybrid target impedance as constrain, use the linear VRM model for frequency domain optimization, and validate this optimized solution with small signal VRM model in time domain.

From figure 36, the optimized impedance was shown by green curve, which below the provided hybrid target impedance with red points for discrete impedance and red lines for continuous target impedance. From figure 37, the output voltage was provided including voltage spike with 44.80mV, voltage droop with 30.15mV and voltage ripple 10.33mV. Comparing with previous voltage response with the PDN impedance by the blue curve in figure 36, these voltage noises are all improved to lower level for voltage spike by 24.30mV, voltage droop by 13.39 mV and voltage ripple by 6.63mV as shown in table 8.

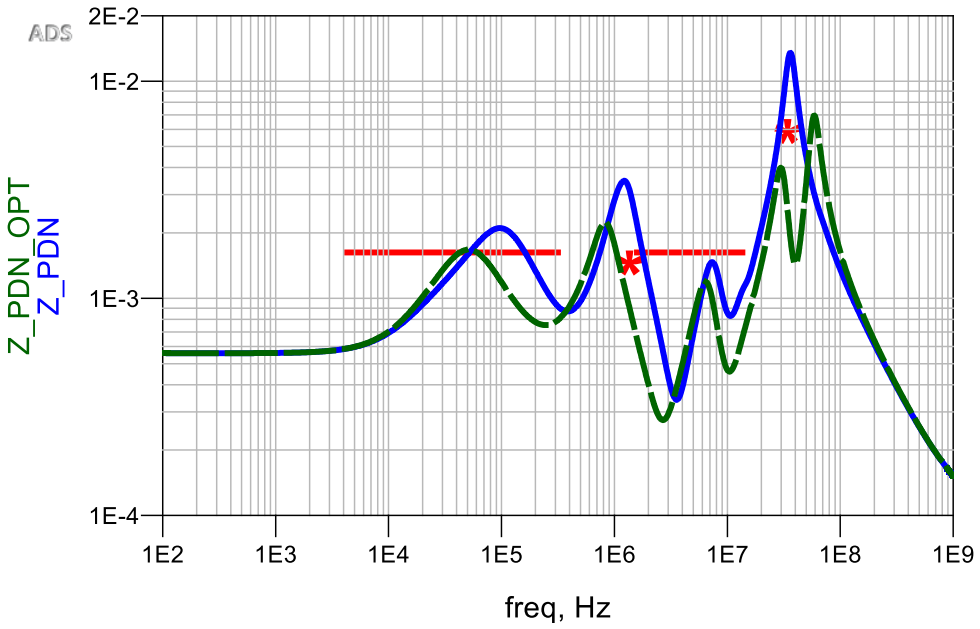


Figure 36. Impedance Optimization based on Hybrid Target Impedance

Table 8. Voltage Response Comparison between Previous and Optimized Case

	Previous	**Optimized**	**Difference**
$\mathbf{V_{Spike}}$	69.10mV	44.80 mV	24.30 mV
$\mathbf{V_{Droop}}$	43.54 mV	30.15 mV	13.39 mV
$\mathbf{V_{Ripple}}$	16.96 mV	10.33 mV	6.63mV

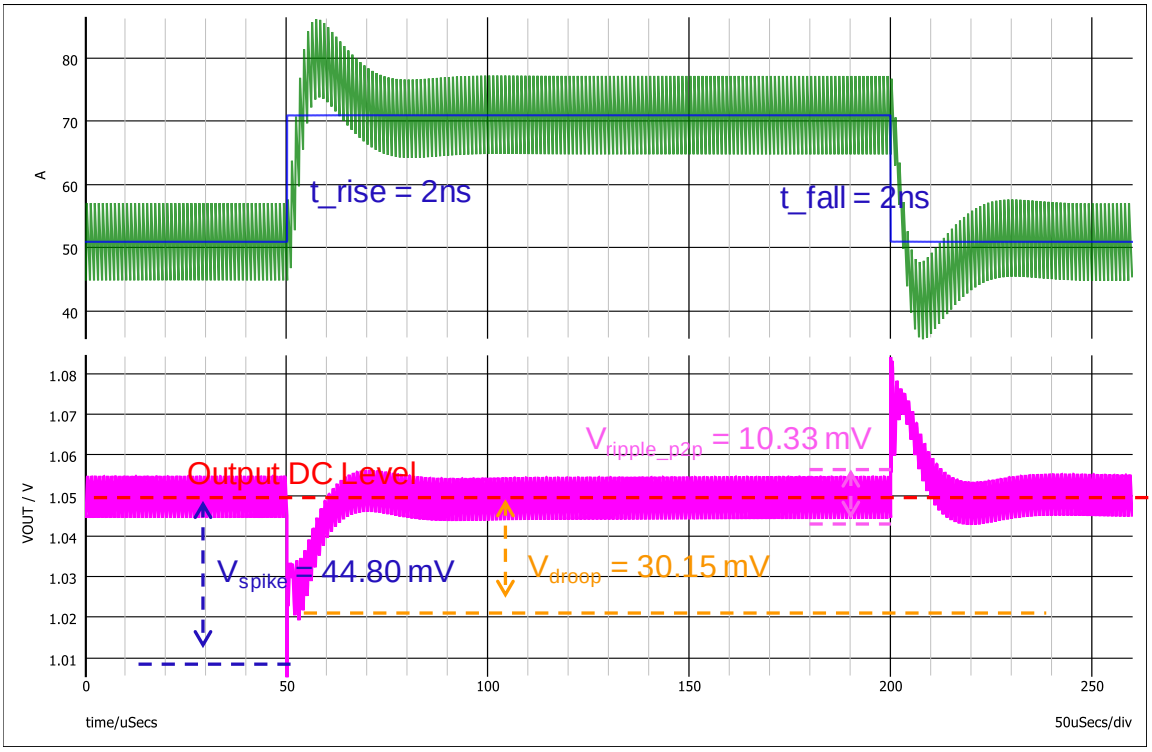


Figure 37. Voltage Response for PDN-Optimized Case

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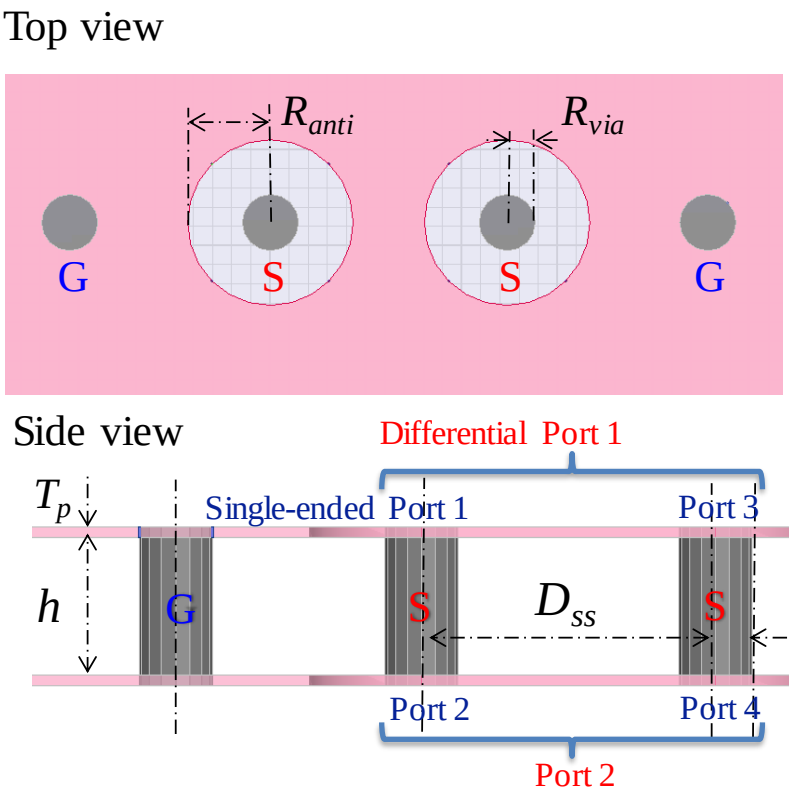
II. A SURVEY ON MODELING STRATEGIES FOR HIGH-SPEED DIFFERENTIAL VIA BETWEEN TWO PARALLEL PLATES

ABSTRACT

This paper presents a survey on physics-based modeling strategies for differential via in high-speed multi-layer printed circuits (PCBs). Driven by the goals of accurate and efficient design, researchers have explored several approaches for differential via modeling, including π-type RLC circuit, differential transmission line with via-plate capacitance/ effective dielectric constant and parallel plate impedance model. This survey provides overviews of these modeling strategies and comparisons by correlating mixed-mode S-parameter from HFSS. In particular, this paper then aims on building a generic parameterized and SPICE-compatible circuit model for designing differential via in a frequency range up to 40GHz.

1. INTRODUCTION OF DIFFERENTIAL VIA

Differential via is a common signal transition in multi-layer printed circuit board (PCB). For high-speed channel with data rates above tens of Gbps, it contributes a critical discontinuity to distort and degrade signal. This paper reviewed four types of differential via modeling strategies. These models can be utilized for the via structure development. An accurate geometry-dependent and SPICE-compatible circuit model is needed for geometrical parameters optimization of an example of the differential via pairs between two parallel plates as shown in figure 1, which is the part II in figure 2 that segmented by the divide-and-conquer method for differential via modeling.



Symbol	Description
R_via	Signal & GND via Radius
R_anti	Anti-pad Radius
D_ss	Signal Via Pitch
D_sg	Air Gap
h	Dielectric Thickness
Tp	Copper Thickness

Figure 1. Geometry of the differential via pairs between planes

There is a lot of research done on via modeling in past years. The work on simple lumped element circuit RLC model did based with some analytical approximation and optimization methods [1-4]. These lumped circuit models are too complicated to understand and extract for their parameters. An equivalent model based on transmission line with via-plate capacitance was applied with space-mapping neural network technique for simplified SPICE-compatible application[5]. However, the model parameter extraction are still complicated and time-consuming. Another simplified and efficient transmission line model proposed with effective dielectric constant calculation in differential mode [6-8]. However, via structure for a practical PCB board is excited by vertical current with

parallel plane waves between two parallel plates. The higher order evanescent modes cannot be involved in above models. The parallel plate impedance model was studied with considering plane effects in many papers [9-19] .

In this paper, these differential via models were studied comparatively and comprehensively for understanding their accuracy, physical meaning, application limitation and design flexibility. This work can help to know how to select a flexible model for a specific application objective. In section II introduce each structure and circuit model of four differential via models. In section III and IV, mixed-mode S-parameters comparison between these models and full-wave simulation reference are presented and analyzed quantitatively with error percentage in linear scale. Based on comparison and studying, an accurate parameterized model for designing differential via is developed.

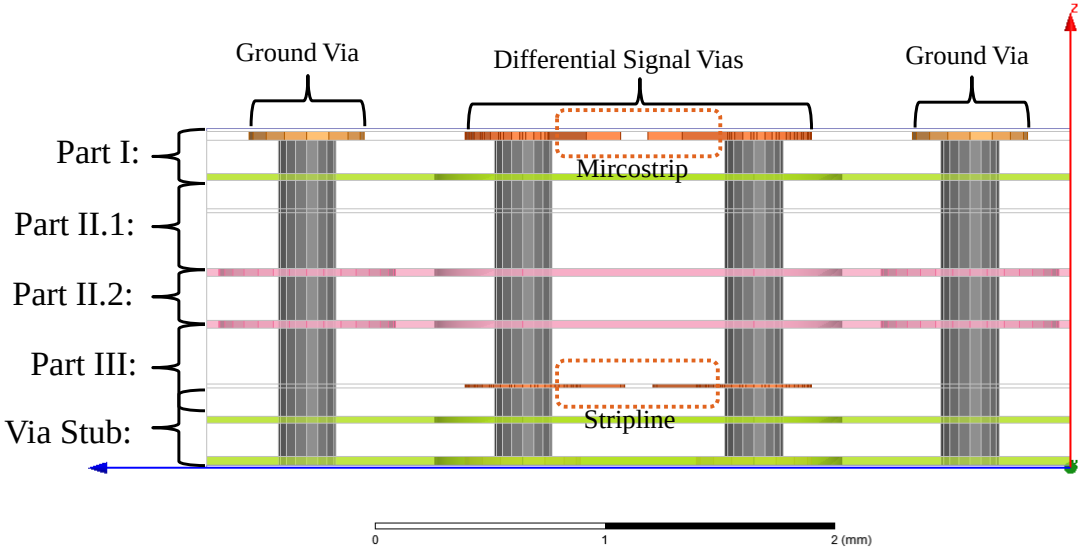


Figure 2. Divide-and-conquer method for differential via modeling

2. SURVEY OF MODELING STRATEGIES

2.1. PHYSICS BASED RLC CIRCUIT MODEL

A physics-based via model can be developed by peeling and partitioning method and analyzing current distributing path through via structure [1, 2]. The displacement current paths are represented by capacitances *Ct* and *Cm*. The partial inductance *Lv* (via barrels part between plates) and the mutual inductance *Lm* (between via barrels) of via barrels must be taken into account as well. The resistance shown in model 1 from figure 3 are frequency dependent and calculated by

$$R(f) = R_t \cdot \sqrt{f} \tag{7.1}$$

where, the R_t are the skin-effect effective resistance with the unit of $\Omega/\sqrt{Hz}$, and f is frequency in Hz.

These RL*C* parameters are extracted from the commercial full-wave HFSS/Q3D tools based on the physical meaning. And these extracted parameter are substituted into the circuit model 1 to calculate the single-ended S-parameter. Then, the mixed-mode S-parameter are converted from these calculated S-parameter for comparing with reference.

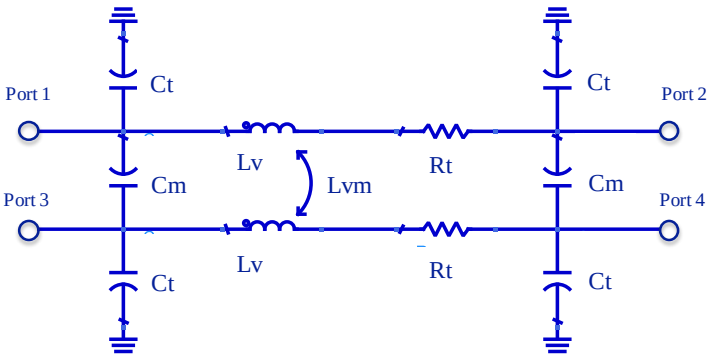


Figure 3. Model 1 - RLC π-type circuit model

2.2. TRANSMISSION LINE MODEL WITH VIA-PLATE CAPACITANCE

A coupled transmission line (TL) model is used to model via barrel part in a lower bandwidth under 20 GHz. The mixed-mode impedance Z_{even} and Z_{odd} were calculated by the Q2D tool by modeling via barrels as the transmission line model. The electrical length EL_{via} in degree is calculated with the physical length of via barrel. The via to plate capacitance C_{t2} and mutual capacitance C_{m2} can be added at terminals of transmission line model for describing an entire via between two plates as shown in figure 4.

The C_{t2} models the coaxial capacitance between via barrel in planes and the reference ground planes. The C_{m2} models the capacitive coupling between via barrels in the planes. These capacitance in this model were trained by some optimization algorithms [5]. However, these capacitance parameters were also extracted from full wave simulation tools for aiming to build the generic parameterized model.

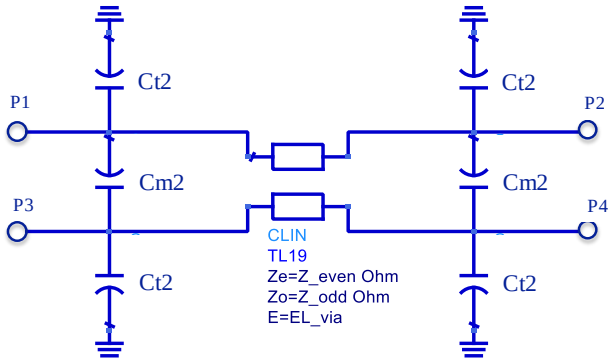


Figure 4. Model 2 - Transmission line model with via-plate capacitance

2.3. TL MODEL WITH EFFECTIVE DIELECTRIC CONSTANT

Another transmission line model was studied in a series of paper [6-8] based on analytical equations for characteristic impedance and effective dielectric constant. By

analyzing differential via holes as a twin-rod transmission line geometry, the differential impedance Z_{diff} and differential effective dielectric constant DK_{eff} are calculated by following equations (2, 3). These two derived parameters were put back into the coupled transmission line model as shown in figure 5.

The differential effective dielectric constant DK_{eff} can also be extracted by HFSS tool or calculated from average effective dielectric constant with a combination of the anisotropic property of dielectric material plus the capacitive loading effect of the anti-pads [6]. These is most important part for this simple circuit model.

$$Z_{diff} = \frac{120}{\sqrt{Dk_{eff}}} \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \tag{7.2}$$

$$Dk_{eff} = Dk_{avg} \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \tag{7.3}$$

Where, s is the signal via to signal via pitch, r is radius of signal via barrel.

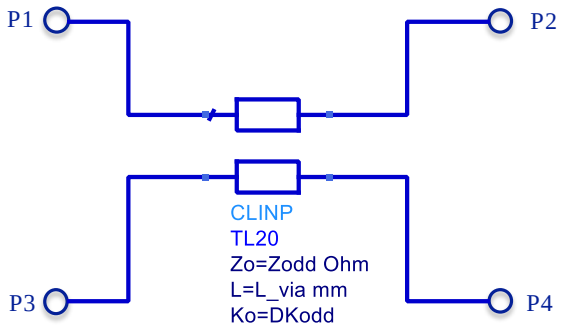


Figure 5. Model 3 - Transmission line model with effective dielectric constant

2.4. PARALLEL PLATES IMPEDANCE ZPP MODEL

To involve the higher order evanescent modes in the model, plane effect must be considered by cavity model with parallel plate impedance that was studied from many

papers [9-19]. This parallel plate impedance matrix *Z* is calculated by analytical equations (4, 5). It is a frequency-dependent table of impedance. The cavity port *i* and *j* for impedance matrix *Z* are cylindrical ports between two plates as shown in figure 6. With corresponded ports connecting as in shown by figure 7, this parallel plate impedance matrix *Z* is substituted into circuit model in figure 8 with capacitance C_p for modeling the entire via between two plates.

$$Z_{ii} = \frac{V_i}{I_i} = \frac{j\omega\mu h}{2\pi k r_i} \cdot \frac{H_0^{(2)}(kr_i)}{H_1^{(2)}(kr_i)} \tag{7.4}$$

$$Z_{ji} = \frac{V_j}{I_i} = \frac{j\omega\mu h}{2\pi k r_i} \cdot \frac{H_0^{(2)}(kr_{ij}) J_0(kr_j)}{H_1^{(2)}(kr_i)} \tag{7.5}$$

$$C_a = \frac{2\pi\varepsilon_r\varepsilon_0 t}{\ln(b/a)} \tag{7.6}$$

$$C_b = \frac{4\pi\varepsilon_r\varepsilon_0 t}{h\ln(b/a)} \sum_{n=1,3,5\ldots}^{2N-1} \frac{(1-\Gamma_a^{(n)}\Gamma_R^{(n)})^{-1}}{k_n^2 H_0^{(2)}(k_n a)} \tag{7.7}$$

$$C_p = C_a + C_b \tag{7.8}$$

Where *a* is the radius of via, *b* is the radius of anti-pad, *t* is the thickness of the reference plate, *h* is the via barrel physical length. ε_r is the relative permittivity of the dielectrics in which the via is embedded. *R* is the outer boundary. *N* is the mode number. k_n is the wavenumber calculated by (4). Γ_a and Γ_R are the reflection coefficients for any TM_{zn} mode with different boundary conditions [11].

The via-plate capacitance C_p is sum of coaxial capacitance C_a and via barrel to plate capacitance C_b that are calculated by analytical equations (6, 8).

This approach is more efficient than the numerical method and can be integrated with SPICE circuit model. Furthermore, these analytical equations are fully geometry-related, which can be utilized for via structure optimization design with a generic model. And it can support a rather higher frequency to 40Ghz and well-correlated with measurement results[9, 10].

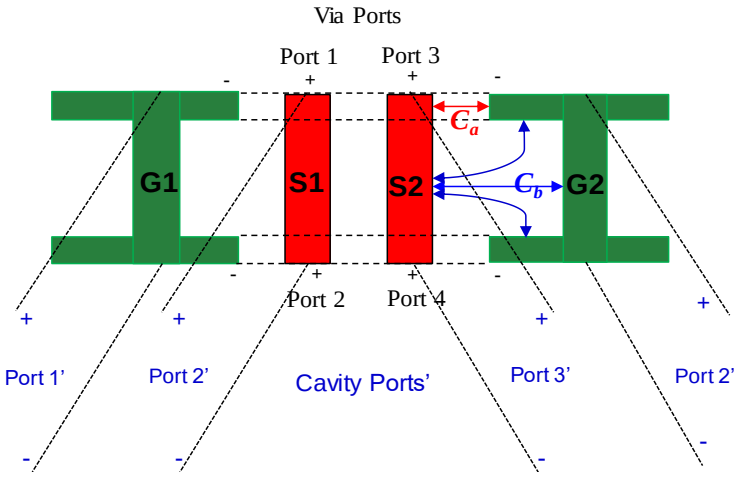


Figure 6. Illustration of four ports between two parallel plates

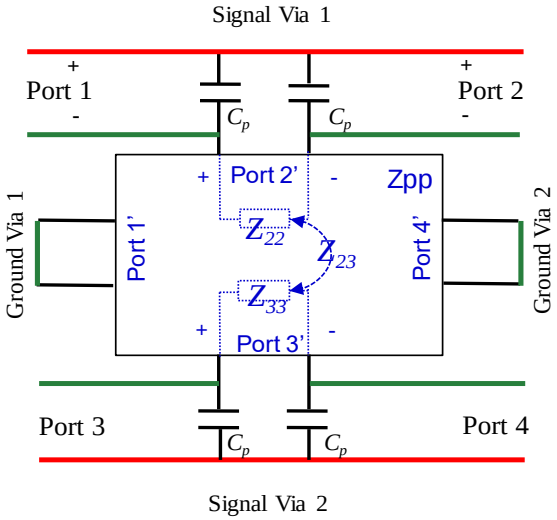


Figure 7. Illustration of circuit model - Parallel plates Impedance Zpp model

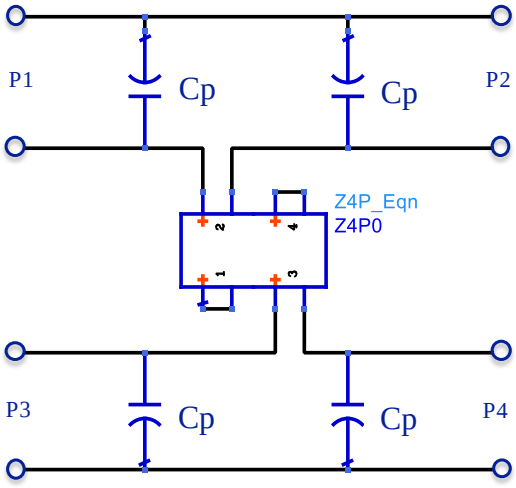


Figure 8. Circuit model for Model 4 - Parallel plates Impedance Zpp model

3. TWO-LAYERS CASE COMPARISON

In this section, above mentioned via models are used to generate S-parameter by SPICE circuit model. The correlation accuracy between these models and reference is presented here and evaluated by linear scale error percentage. The single differential via between 2-layer plates in figure 1 is simulated by a finite element method (FEM) based commercial tool as a reference of the frequency range from 20Mhz to 40Ghz. The geometry parameters for this example are R_{via} = 5mil, R_{anti} = 16mil, D_{ss} = 45mil , D_{sg}= 20mil, h = 10mil , T_p = 0.6mil and *dielectric constant* = 3.68.

The mixed mode S-parameter was obtained from the four methods and reference for comparison in figure 9. Table I and II also provide the linear scale error for SDD12 and SCC12 at three frequency points of 14 Ghz, 28Ghz and 40Ghz. The model 3 only support differential mode, so common mode comparison between model 3 and reference was not included.

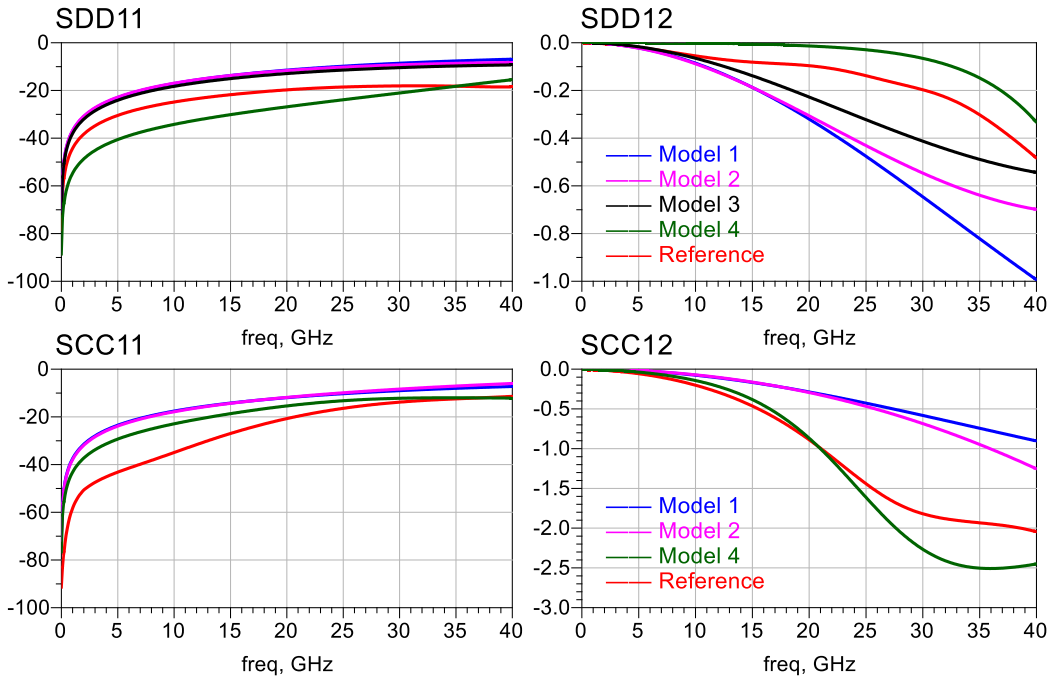


Figure 9. Mixed mode S-parameter comparison for via with 2-layer plates

Table 1. Linear Scale Error for Sdd12 for via with 2-layer plates

Sdd12 2-layer	**% Error between models and reference**			
	Model 1	**Model 2**	**Model 3**	**Model 4**
14Ghz	1.00%	1.01%	0.51%	-0.84%
28Ghz	4.55%	4.55%	2.32%	-1.46%
40Ghz	5.71%	2.45%	0.69%	-1.74%

Table 2. Linear Scale Error for Scc12 for via with 2-layer plates

Scc12 2-layer	**% Error between models and reference**		
	Model 1	**Model 2**	**Model 4**
14Ghz	-2.97%	-3.03%	-0.94%
28Ghz	-14.69%	-13.72%	3.83%
40Ghz	-14.06%	-9.54%	4.56%

4. MULTI-LAYERS CASES COMPARISON

In this section, two cases for multi-layers differential via structure are evaluated for comparison between these models. The cases with 5-layers plates have four in-between via barrels as shown in figure 10. The circuit model by model 1 and model 4 for this case was cascaded by four-stage π-circuits and Zpp blocks as shown in figure 11. The 9-layers case have two times of cascaded in-between via barrels as shown in figure 12, so 8 Zpp blocks will needed for cascaded circuit model.

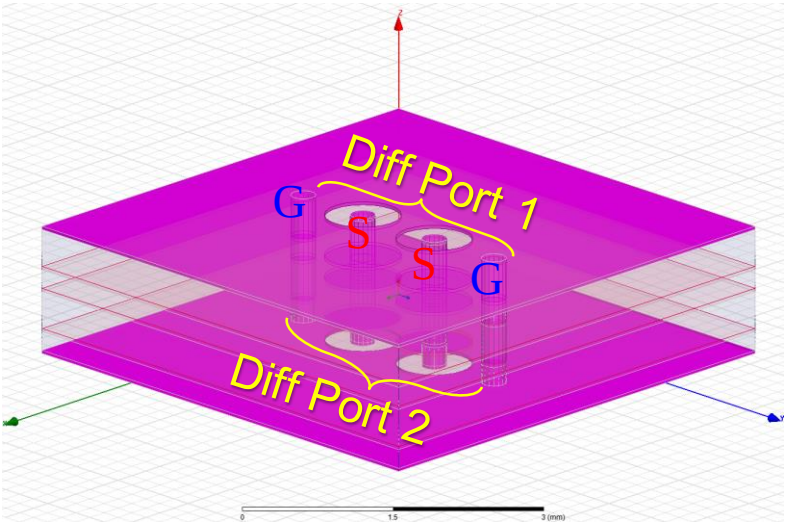


Figure 10. Full-wave models structure for differential via with 5-layers plates

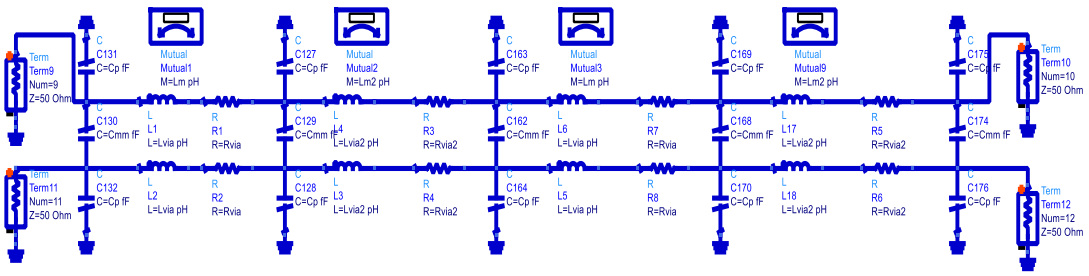


Figure 11. Four-stage π-circuit RLC model for via with 5-layer plates

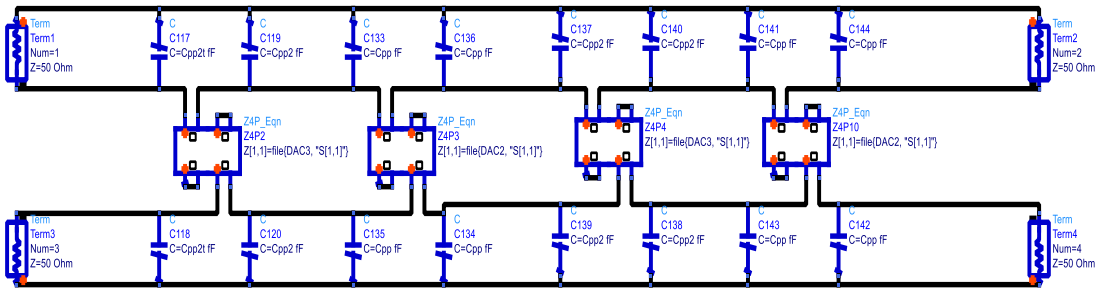


Figure 12. Cascaded Zpp model for via with 5-layer plates

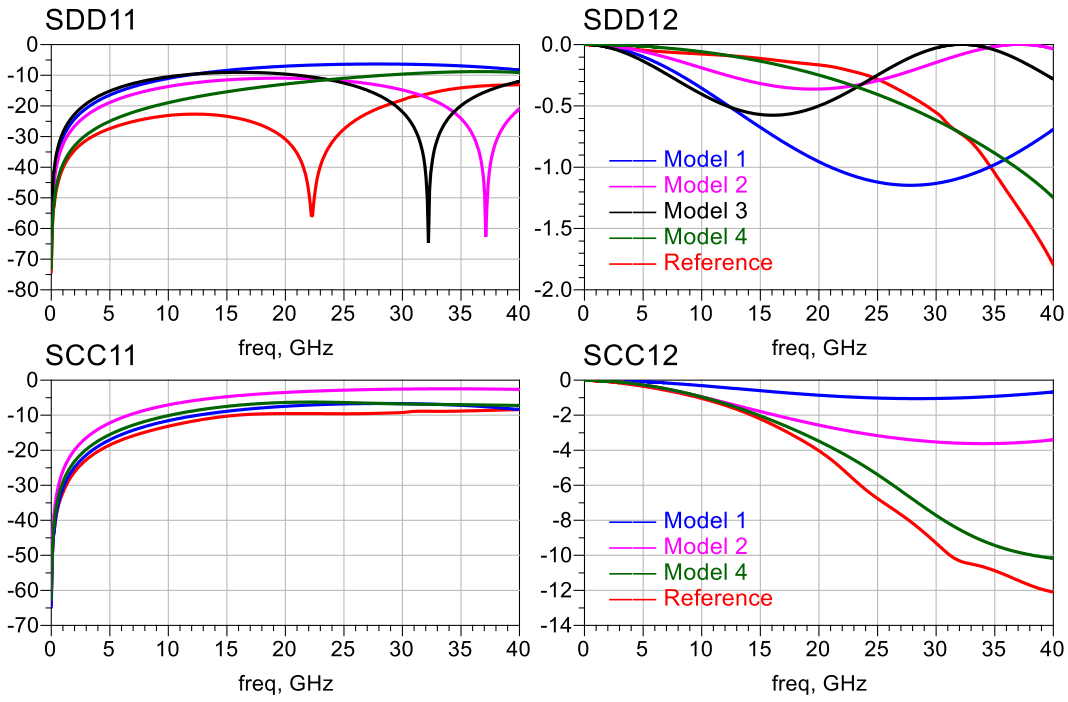


Figure 13. S-parameter Comparison for via with 5-layer plates

Table 3. Linear Scale Error for Sdd12 for via with 5-layer plates

Sdd12 5-layer	**% Error between models and reference**			
	Model 1	**Model 2**	**Model 3**	**Model 4**
14Ghz	5.69%	2.20%	5.06%	0.16%
28Ghz	7.91%	7.91%	-3.95%	1.09%
40Ghz	-13.53%	-22.46%	-19.02%	-6.49%

Table 4. Linear Scale Error for Scc12 for via with 5-layer plates

Scc12 5-layer	**% Error between models and reference**		
	Model 1	**Model 2**	**Model 4**
14Ghz	-17.34%	-3.03%	-1.59%
28Ghz	> 100%	> 100%	-17.14%
40Ghz	> 100%	> 100%	-24.77%

Other Circuit models that made by coupled transmission line model 2 and model 3 for cascaded case is the same with 2-layer case as shown in figure 4 and figure 5. So these two models are simpler for the SPICE circuit simulation comparing with RLC model and Zpp model.

The mixed mode S-parameter comparison between four methods and reference for 5-layers and 9-layer cases are respectively shown in figure 13 and figure 15. Following tables after these S-parameters plots provide the linear scale error for SDD12 and SCC12 for numerical correlation between these models and the full-wave reference.

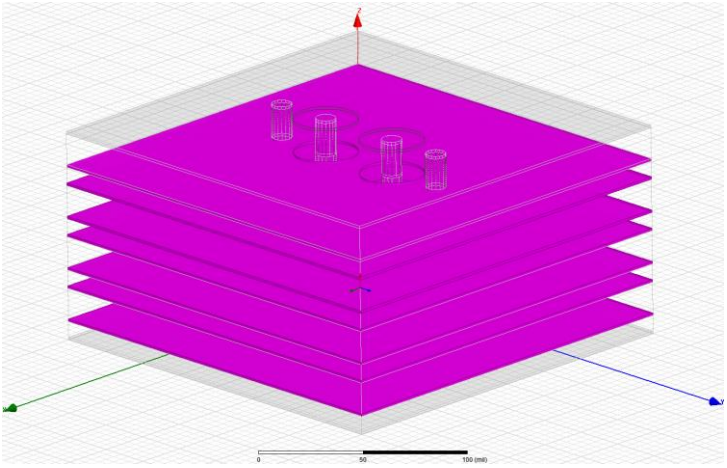


Figure 14. Full-wave models structure for differential via with 9-layers plates

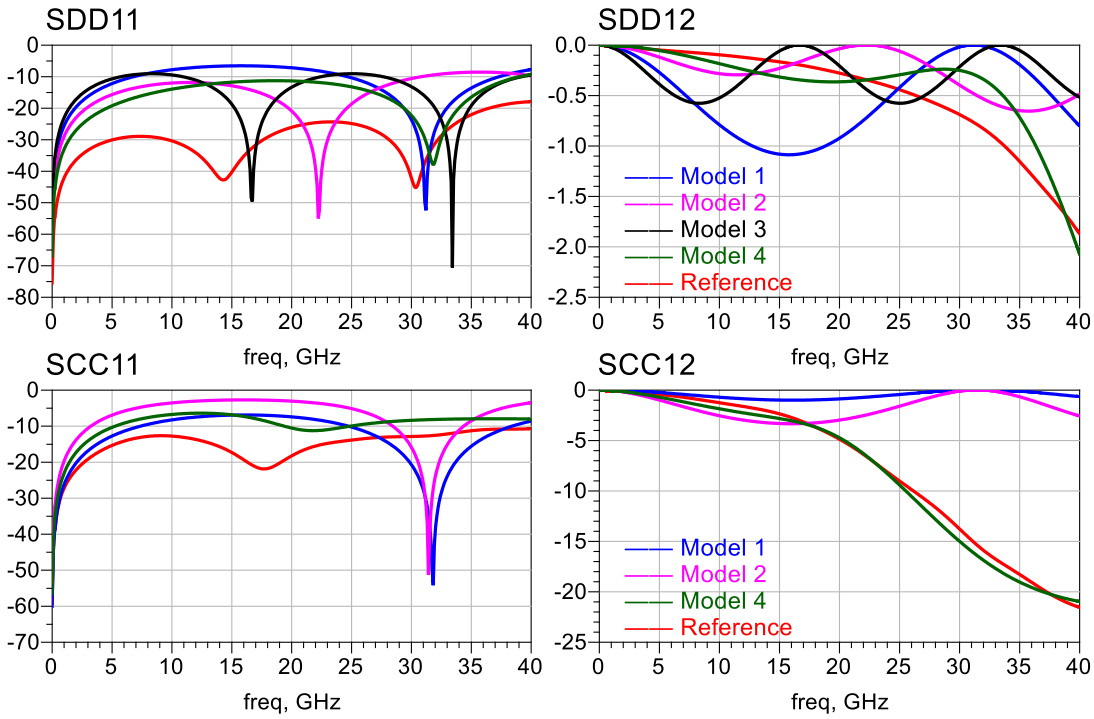


Figure 15. S-parameter Comparison for via with 9-layer plates

Table 5. Linear Scale Error for Sdd12 for via with 9-layer plates

Sdd12 9-layer	**% Error between models and reference**			
	Model 1	**Model 2**	**Model 3**	**Model 4**
14Ghz	9.92%	1.25%	-0.13%	1.64%
28Ghz	-5.34%	-5.34%	-1.83%	-3.97%
40Ghz	-13.09%	2.45%	-16.88%	2.31%

Table 6. Linear Scale Error for Scc12 for via with 9-layer plates

Scc12 9-layer	**% Error between models and reference**		
	Model 1	**Model 2**	**Model 4**
14Ghz	-13.61%	-12.67%	6.27%
28Ghz	>100%	>100%	12.77%
40Ghz	>100%	>100%	-6.91%

5. CONCLUSION

From this survey, the four circuit models for the differential via were compared by mixed-mode S-parameters and corresponded error percentage correlating to the reference. Generally, the model that built by the parallel plates impedance Zpp can have smallest error percentage in both of differential mode and common mode at concerned frequency range. It also have a good agreement for common mode S-parameter in cascaded multi-layers cases. In particularly, the model 4 can be implemented as a geometry information related generic model for parameterized optimization as shown in figure 16.

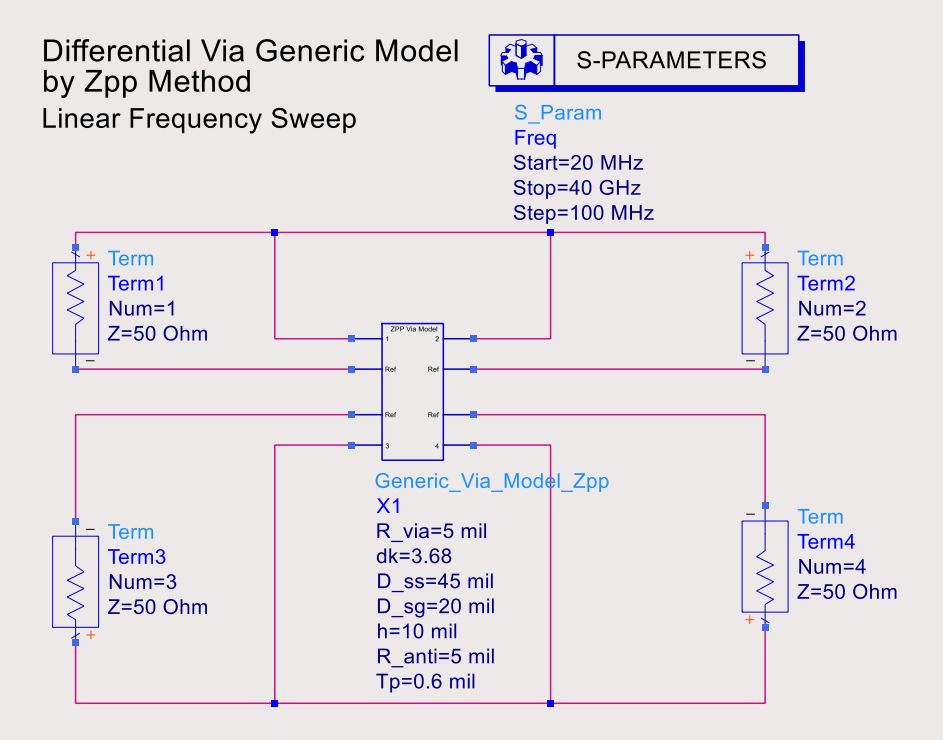


Figure 16. A generic parameterized model using Zpp model for differential via

The transmission line models are more straightforward for implementation in SPICE circuit simulation. However, it supports with lower frequency to 20 GHz. So the via models for application up to 40 GHz, the model 4 by parallel plates Zpp method is preferred. A comparison for these four models of differential via are also concluded in table VII from different aspects of correlation performance, application complexity, applicable frequency range and flexibility for parameterization design and optimization for trade-off in modeling strategies.

Table 7. Comparison of Four Models for differential via

	Model 1 π-type RLC	**Model 2** TL w/ $C_{via\text{-}plate}$	**Model 3** TL w/ DK_{eff}	**Model 4** Zpp Impedance
Correlation Performance	Low	Low	Moderate	High
Implementation Complexity	Low	Moderate	Moderate	High
Applicable Frequency Range	Subject to electrical length	Up to 20GHz	Up to 20GHz	Up to 40GHz
Supported Mixed Mode	Both DM and CM	Both DM and CM	Only DM	Both DM and CM
Parameterized Model Design	No	No	Yes	Yes

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III. APPLICATION OF DEEP LEARNING FOR HIGH-SPEED DIFFERENTIAL VIA TDR IMPEDANCE FAST PREDICTION

ABSTRACT

A deep neural network (DNN) model is developed in this paper for fast prediction of time-domain reflectometer (TDR) impedance for differential vias in high-speed printed circuit boards (PCBs). Unlike traditional empirical linear modeling approaches, the DNN model more accurately maps the nonlinearity between via geometrical parameters and differential impedance. How to select neural network type, training functions and how to select an efficient set of training data are discussed in the paper. Good correlations between the predicted impedances and target values prove the accuracy and reliability of the DNN model. The calculation time for a single data point is reduced to milliseconds, so that the design efficiency of high-speed differential via design is significantly increased.

1. INTRODUCTION OF VIA IMPEDANCE

Differential via is a critical part in designing high-speed channel in multi-layer printed circuit board (PCB). With the increasing of clock rate and data rate above tens of Gbps, transition via contributes a critical discontinuity to distort and degrade signal performance. An accurate geometry-dependent model is needed for geometrical parameters optimization of an example of differential via in the multi-layer board as shown in figure 1. In a practical layout stage, the design parameters for tuning the differential geometry can mainly focus on via drill hole size, signal and ground pad size, anti-pad size and pitches between signal and ground vias.

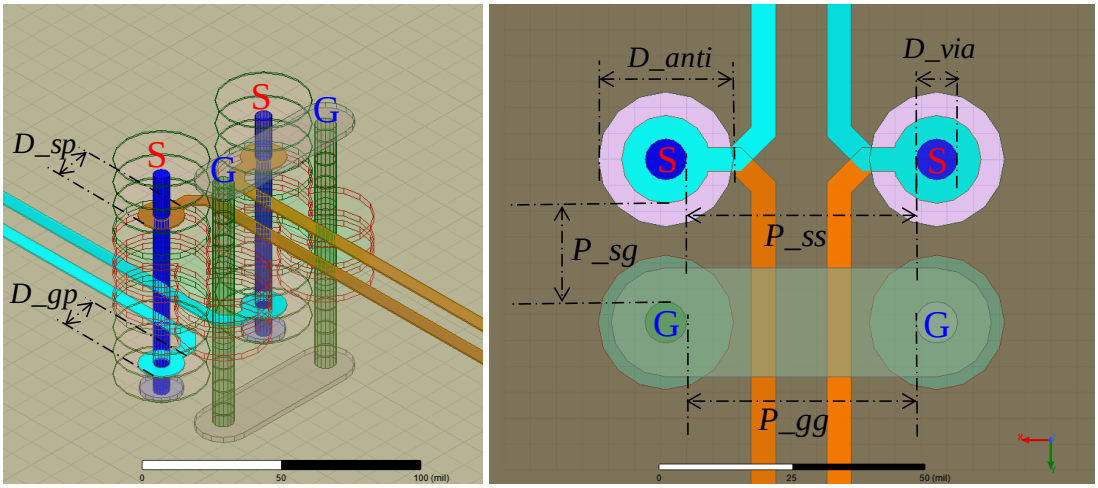


Figure 1. Geometrical parameters of the differential via in multi-layers PCB

Table 1. Via Design Tunable Parameters in Layout Stage

#	Parameters	Description	Range(mils)
1	*D_v*	Via Drill Hole Diameter	4.9 ~ 14.7
2	*D_sp*	Signal via pad Diameter	9.5 ~ 28.5
3	*D_gp*	GND via pad Diameter	10.5 ~ 31.5
4	*D_a*	Anti-pad Diameter	25 ~ 75
5	*P_sg*	Signal-Ground Via Pitch	20 ~ 60
6	*P_ss*	Signal-Signal Via Pitch	26 ~ 78
7	*P_gg*	Ground-Ground Via Pitch	26 ~ 78

In the past years, many approaches were done on via modeling and parameter tuning to optimize TDR impedance, return loss and insertion loss for improving channel performance. There has been some work on simple lumped element circuit RLC model and transmission line model with some analytical approximation and optimization methods. However, via structure for a practical PCB board is excited by vertical current with parallel plane waves between two parallel plates. The higher order evanescent modes cannot be

taken into consideration in the above models. The parallel plate impedance model was studied with considering plane effects [1]. However, these existing modeling strategies lack of fast and flexible parametric modeling ability for multi-layers board differential via in practical design application. A broadband parametric equivalent model space-mapping neural network was applied with transmission line model and via-plate capacitance [2]. Recently, the deep neural network method and machine learning were applied for DDR channel modeling, Eye Height/Width Prediction, Serializer/Deserializer (SerDes) Channel setting tuning and three-dimensional integration for high-speed interconnect system [3-6]. These applications have presented the efficient nonlinear modeling ability of neural network to overcome the limitation of traditional method to speed up the parameter optimization and variations analysis.

In this paper, a deep neural network was proposed for different-via impedance prediction with identified design tunable parameters as inputs and impedance as output. The input parameters include seven geometrical variables of differential via, i.e. via drill hole diameter (D_v), signal via pad diameter (D_{sp}), ground via pad diameter (D_{gp}), anti-pad diameter (D_a), signal via to ground via pitch (P_{sg}), signal via to signal via pitch (P_{ss}) and ground via to ground via pitch (P_{gg}). To get a training data set, an input table is generated by design of experiment (DoE) to select the smallest set of designs in each expected range [7]. Then HFSS full-wave simulations are performed for these training data points. These parameters can cause a wide range of fluctuations for TDR impedance, return loss and insertion loss as shown in figure 2. Then, section II introduces the DNN model method and three different training functions for neural network. In section III, the flow to model

differential via using DDN is demonstrated and correlation between desired data and predicted data is discussed.

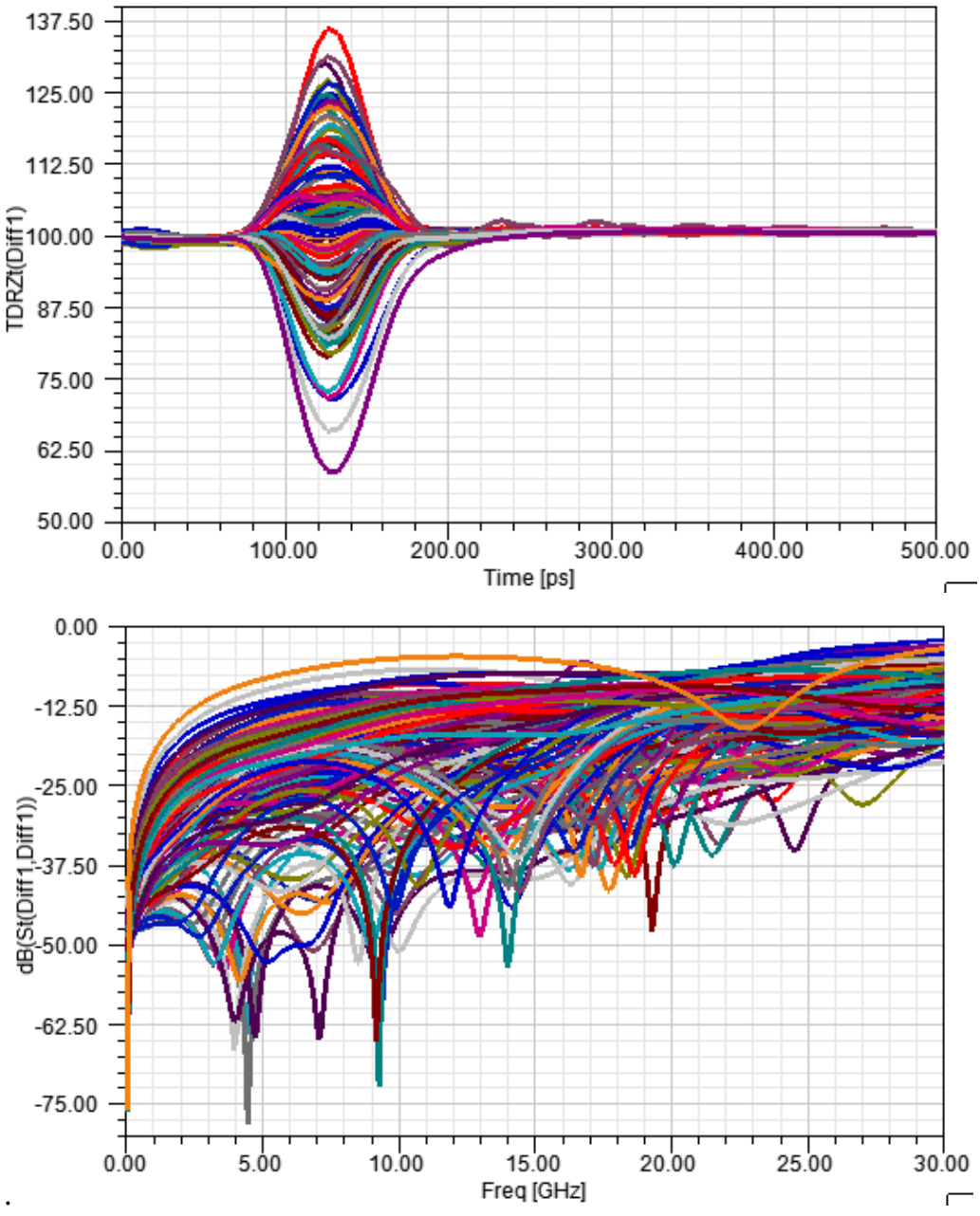


Figure 2. TDR Impedance and Return Loss Variation with Tuning Design Parameters in the Wide Range

2. DEEP LEARNING APPROACH

The structure of the DNN modeling illustrated in figure 3 consists of a neural network with one input layer, one output layer and multiple hidden layers. The DNN model can nonlinearly map the output and input parameters with modified weighted linear combination as shown in figure 3. The mathematical function for each neuron can be given as:

$$. \; y_i = \phi(\sum_j (b_i + w_{ij} x_j)) \tag{12.1}$$

where y is the output value of neuron i, ϕ is the activation function, b_i is the bias of neuron i, w_{ij} is the weight between input neuron j and output i, x_j is the input value for neuron i from the output value of previous neuron j.

The key to design a DNN model is how to select training algorithm and hyper-parameters based on particular input training data. The flow of the DNN model parameter

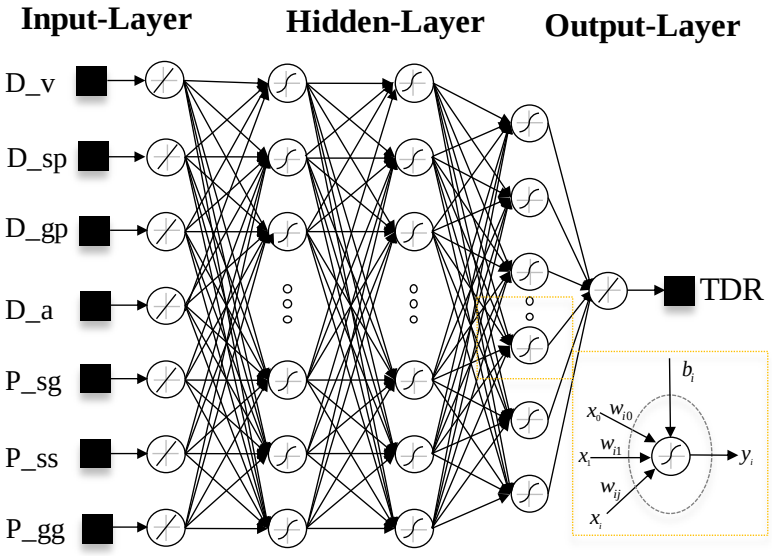


Figure 3. Structure of DNN model with several hidden layers and quadratic mapping at a neural node

selection is shown as figure 4. This flow starts from picking a training algorithm. Then define network hyper-parameters, i.e., numbers of hidden layers, numbers of neurons in each hidden layer, following by defining training parameters such as learning rate, momentum constant and mini-batch size. Then run the defined DNN model and last but not least check performance metric using cost function. If performance meets minimum requirement, save the network. Otherwise, return to step 2 to sweep another set of parameter values.

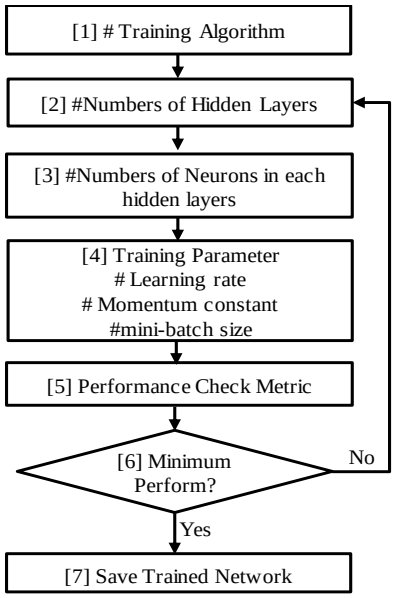


Figure 4. Flow of DNN model hyperparameter selection

For training parameters, learning rate is critical. It is a hyper-parameter that controls convergence speed to adjust the weights in the trained network with respect to loss gradient. If learning rate is large, the training can overstep the minimum points and even diverge. And if learning rate is small, the training will need more iterations of gradient descent which increases the training time. Hence, selecting an appropriate learning rate is critical for training an accurate network model with fast convergence.

Among these DNN network parameters, the number of neurons is important. The number of neurons is determined with training DNN model based on complexity of input parameters mapping and input variable dimension to achieve the target performance. These learning model problems can be summarized as obtaining a network model ***F***, such that

$$\begin{gathered} T = F(x_i) \\ subject.to. \rightarrow J(T, F(x_i)) \le \varepsilon \\ x_i \in [X_L, X_H] \end{gathered} \tag{12.2}$$

Where, x_i is a tunable input parameter to an optimizer in limited range, which used to generate the network ***F*** with minimizing cost function ***J*** to achieve a desired goal ε .

For DNN performance check, cost function usually uses the mean square error (MSE) between expected target data ***T*** and predicted data $F(x_i)$ from trained network ***F***. But square error puts a greater emphasis on larger values especially when difference is larger than 1. Hence, other error measure methods are also mentioned as root mean square error (RMSE), normalized root mean square error (NRMSE), mean absolute error (MAE), minimum absolute error (MIN) and maximum absolute error(MAX) for cost function to check network performance.

$$MSE = \frac{1}{N}\left(\sum_{i=1}^{N}(T_i - F(x_i))^2\right) \tag{12.3}$$

$$RMSE = \sqrt{\frac{1}{N}\left(\sum_{i=1}^{N}(T_i - F(x_i))^2\right)} \tag{12.4}$$

$$NRMSE = \frac{RMSE}{Y_{\max} - Y_{\min}} \tag{12.5}$$

$$MAE = \frac{1}{N}\left(\sum_{i=1}^{N}|T_i - F(x_i)|\right) \tag{12.6}$$

$$MIN = \min(|T_i - F(x_i)|) \tag{12.7}$$

$$MAX = \max(|T_i - F(x_i)|) \tag{12.8}$$

3. MODEL DEVELOPMENT AND VALIDATION

The flow for developing differential via impedance DNN model is shown in figure 5. First, identify seven differential-via geometric variables as discussed in section 1. Then a data set including 150 data points is generated by latin hypercube sampling (LHS) method to achieve a 150*7 matrix dataset. The third step is to use Ansys HFSS to run 3D EM simulation so as to extract TDR and S-parameters. The impedance at the 125ps is extracted for the maximum variation at peak and dip of the TDR as shown in figure 2. Reflection loss and insertion loss are extract at Nyquist frequency 8GHz. Table II listed 6 typical cases. Case 1 and case 2 have two highest via impedance values, while case 149 and case 150 have two lowest impedance values. Case 149 and case 150 correspondingly have more reflection SDD11 and lower insertion loss SDD21, since their impedance values deviate more from 100Ohms. Case 44 and Case 45 have their impedance most close to 100Ohms, leading to the tiniest reflection loss and highest insertion less.

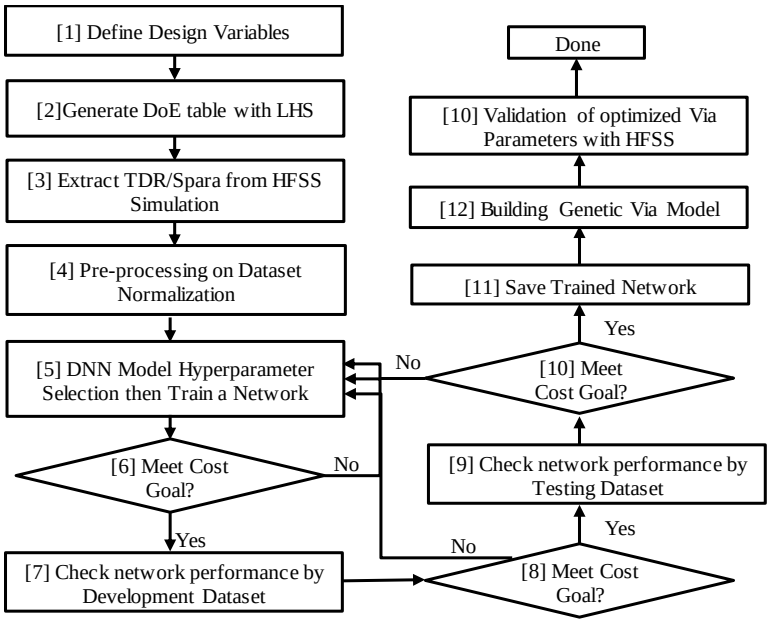


Figure 5. Flow for developing DNN model for designing optimized via

Then this 150 dataset is divided into training set, development set and testing data randomly by ratio of 70%, 15% and 15% each. The development set is used for tuning the DNN model parameters selection. It can provide an unbiased validation of a model fit on the training dataset while tuning the model hyper-parameters.

Step 4 is pre-processing training data. Normalization is applied for rescaling input vectors in (0,1) that can effectively change weights and bias with fast convergence speed.

Step 5 is to select a training algorithm and define training parameters. Three training algorithms are applied for training the network with different layers and optimized neurons based on development dataset validation.

1. Levenberg-Marquardt Backpropagation (LM-BP);

2. Bayesian Regularization (BR);

3. Gradient Descent with Momentum and Adaptive Learning Rate Backpropagation.

Based on DNN hyper-parameter selection flow in section II, the numbers of hidden layers and neurons for each algorithm function are optimized individually. The LM-BP uses single layer with 6 neurons and then the training process converges at 1000 iterations. The BR selects two layers with 6 and 4 neurons at first and second layers, then the training process converges at 245 iterations. The GDX selected three layers with 6-6-4 neurons at each layer, then correspondingly training process cannot converges until 50000 iterations.

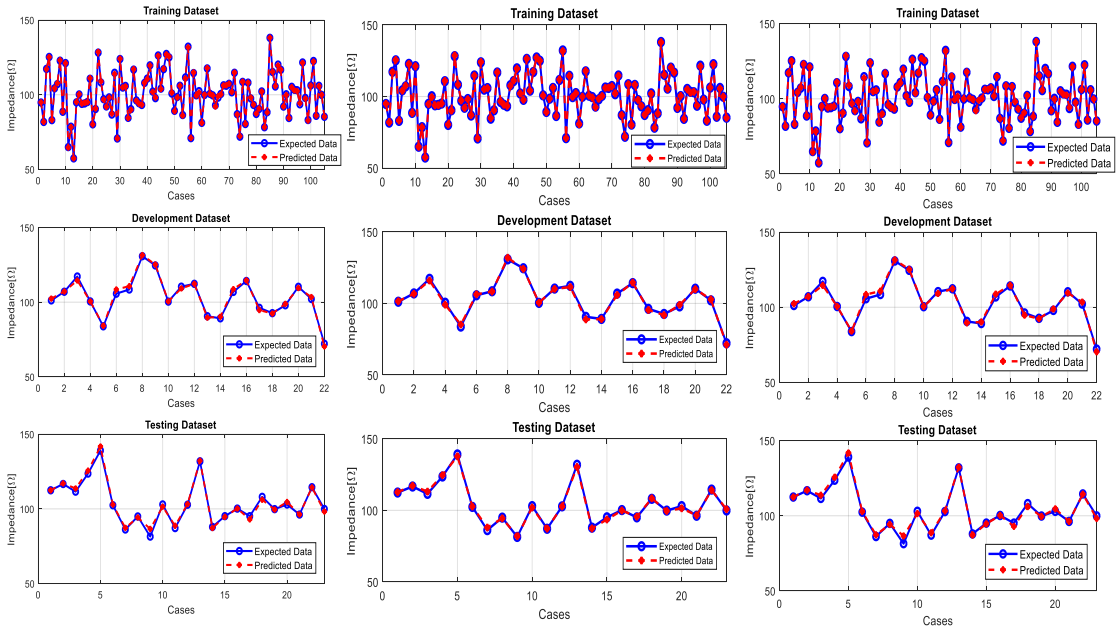
Then step 7 is to apply the trained model to check development dataset by cost goal and testing dataset. If passing, then go to step 9, checking testing dataset by cost goal again. Any failure occurs, the flow goes back to step 5, the DNN model parameter optimization. Once passing testing dataset validation, the model could be saved as a well-trained generic

via model to predict impedance. The impedance calculation time is all most at no cost by using the well-trained model. Thus, it is handy and time-efficient for SI engineers doing differential via design.

Correlation between expected and predicted data trained with development and testing dataset for these three different training algorithms is as shown in figure 6. Overall speaking, all three algorithms correlate well. Table 3 shows Bayesian Regularization (BR) algorithm gave smallest MSE below 1.0 and smaller MAX error compared with other two algorithms. Figure 7 shows BR converges fastest to a low MSE in training process. Consequently, BR is proved to be the best algorithm for this particular case with faster convergence speed and lower prediction cost error.

Table 2. Tabulated Samples of Dataset (150 data points)

#	$D_antipad(mils)	$D_gnd_pad(mils)	$D_trace_pad(mils)	$D_via (mils)	$pitch_gg (mils)	$pitch_sg (mils)	$pitch_ss (mils)	TDR11: (125ps)	dB(SDD11): (8GHz)	dB(SDD12): (8GHz)
01	59.88	16.98	13.73	4.938	57.48	52.34	77.46	138.1	-9.936	-0.9772
02	74.04	24.86	17.74	6.087	41.23	27.03	61.29	132.2	-10.87	-0.8425
…	…	…	…	…	…	…	…	…	…	…
44	37.29	22.23	19.82	6.852	43.67	42.03	59.49	102.1	-30.18	-0.4656
45	61.41	12.88	23.08	10.53	40.42	31.41	39.37	98.23	-43.31	-0.4195
…	…	…	…	…	…	…	…	…	…	…
149	26.19	11.57	27.39	10.07	59.92	54.84	38.29	64.93	-7.672	-1.361
150	28.11	21.57	27.54	14.59	66.42	47.34	40.45	57.36	-5.913	-1.895



(Single Layer 6 with 1000 iterations) (Two Layers 6-4 with 245 iterations) (Three Layers 6-6-4 with 50000 iterations)

(a) Levenberg-Marquardt Backpropgation (b) Bayesian regularizatio (c) Gradient descent w/momentum & adaptive learning rate

Figure 6. Training Data (105 sets-70%), Development Data(22 sets-15%) and Testing Data(23 sets-15%) Correlation between expected and predicted data trained with three different training algorithm for neural network

Table 3. Prediction Cost Metric Value (Ohm) of Performance Evaluation for Different Training Algorithm

Algorithm	Dataset	MSE	RMSE	NRMSE	MAE	MIN	MAX
Levenberg-Marquardt BP	Train Set	0.22	0.46	0.01	0.35	0.00	1.35
	Dev Set	2.43	1.56	0.03	1.19	0.10	4.50
	Test Set	3.10	1.76	0.03	1.34	0.00	3.70
Bayesian Regularization	Train Set	0.06	0.25	0.00	0.20	0.00	0.62
	Dev Set	0.75	0.87	0.01	0.73	0.13	1.78
	Test Set	0.81	0.90	0.02	0.72	0.04	1.78
Gradient Descent W/Momentum & Adaptive Lr	Train Set	0.12	0.35	0.00	0.27	0.00	0.95
	Dev Set	1.72	1.31	0.02	1.04	0.01	2.81
	Test Set	2.78	1.67	0.03	1.20	0.01	5.13

4. CONCLUSION

This paper proposes an idea to apply deep learning algorithm for high-speed differential via design. A DNN model is developed, tested and correlated to predict differential via impedance. The Levenberg-Marquardt Backpropgation (BR) is proved to be the best algorithm with faster convergence speed and lower prediction cost error as shown in figure 7. The model has been proved to be accurate and impedance calculation time is in milliseconds using the DNN model. Therefore, comparing with 30 minutes per model in HFSS 3D EM simulation, it could facilitate engineers to increase via impedance optimization efficiency.

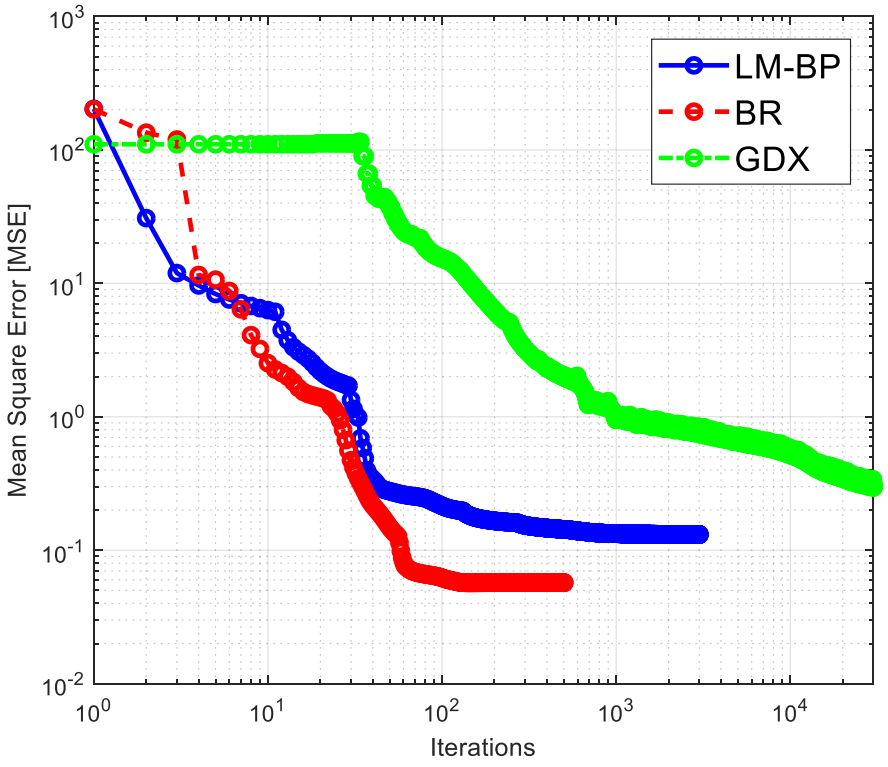


Figure 7. Loss Convergence Comparison between Three Training Algorithm

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SECTION

2. CONCLUSION

2.1. SUMMARY OF CONTRIBUTIONS

A well-designed power delivery network demands a set of efficient and effective modeling methodology for the Chip-Package-PCB System. This thesis work provided and validated the hybrid target impedance for the PDN impedance optimization in frequency domain and the physics-based equivalent circuit model with small signal model for voltage response validation in time domain.

The chip power model simplified with lumped RC equivalent circuit and clock gating only current profile for on-PKG and on-PCB DECAP in fast simulation and optimization. The worst-case load scenario identified by modulating clock gating current profile to hit the PDN impedance resonance peak.

This study compared four different VRM models integrating with the equivalent circuit models for PCB and PKG, which extracted from current path physics-based methods. The three main voltage noise identified as voltage spike, voltage droop and voltage ripple. The VRM model did not contribute to the first voltage spike, but take the key role for second voltage droop. The voltage ripple only predicted by small-signal model with MOSFET switching activity. Compared with linear model, this small-signal model would be a better choice for validation for voltage response in time domain.

The hybrid target impedance defined with current profile-based discrete and continuous target impedance. That provide an effective way to perform system level

optimization to meet voltage specification at critical frequency of current spectral components, and avoid over-designing in the decoupling capacitors optimization.

2.2. FUTURE WORK

As an extension to the methodology described in this thesis work, in the future, we can investigate more on these topics for achieve a well-designed power delivery network. The hybrid target impedance can be further extended with definition that is more theoretical for the bandwidth of continuous target impedance and the amplitude of discrete target impedance. Based on hybrid target impedance, we could develop different optimization strategies for system-level DECAP selection and placement, PCB and PKG layout optimization with considering both performance and cost. The automation on these optimization flow and machine learning based-optimization methodology would be an inevitable trend for power integrity design.

Meanwhile, system-level measurement and simulation correlation is needed from both frequency domain for full PDN impedance and time domain for on-die voltage response. The correlation can help to develop more realistic PDN prediction methods, but need lots of cooperation from different roles and resource. More design parameters would be added in the simulation for realistic PDN prediction design, such as distributed voltage variation on power plane, DECAP derating model, temperature model, and DECAP aging model.

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