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Analysis and mitigation of parallel-plate noise for high-isolation applications

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ANALYSIS AND MITIGATION OF PARALLEL-PLATE NOISE FOR HIGH-ISOLATION APPLICATIONS

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ABSTRACT

Achieving highs levels of isolation between different functionalities in a PCB can be challenging. One of the major issues is that vertically adjacent planes or area fills in a PCB can form a parallel-plate waveguide with no cutoff frequency and serve as an efficient coupling mechanism between interconnects. Due to the finite size of the conductors, reflections off the edges of these parallel-plate cavities can result in the formation of standing-wave patterns with very high field strengths, resulting in high coupling at certain frequencies. This noise coupling mechanism can be suppressed by connecting the parallel plates together with an adequate amount of vias. However, adjacent power and ground conductors can not be conductively connected together because they are at different DC potentials. As a result, there is no way to eliminate the existence of parallel-plate noise in a power/ground cavity. A fundamental understanding of this problem is needed to determine how it can be mitigated.

The first part of the thesis develops a qualitative understanding of the underlying physics of how noise is coupled to the parallel plates from a variety of interconnects and how the noise can spread throughout the design. This discussion is then expanded to more complex geometries that are representative of what could occur in actual designs. Test vehicles are created to study the noise coupling to various interconnects from noise injected into the power distribution network by an amplifier. Parameters affecting the transfer of noise from an amplifier to the power distribution network, such as the addition of capacitors, are then explored. An expression to predict the noise coupling using S-parameter measurements of the PCB and the amplifier is developed. It is demonstrated that results from full-wave electromagnetic simulation can be used to predict the amount of noise coupling before PCB fabrication. General design recommendations are then presented to improve design robustness to the parallel-plate noise.

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1. INTRODUCTION

1.1. MIXED-SIGNAL DESIGN CONSIDERATIONS

Much of the PCB related research is conducted for high-speed digital designs such as server motherboards. Signal integrity considerations, making sure the ones and zeros can be interpreted at the receiver, are the most important for these designs. Due to the routing density of most high-speed digital products, transmission line crosstalk is unavoidable. Although transmission line crosstalk can be pervasive, it is well understood and easy to identify. It drops off predictably with increasing distance. This type of coupling is sometimes referred to as proximity coupling because it is dependent on how close the two transmission line structures are to each other. Analytical equations are available in references such as [1]. However, in signal integrity applications, coupling or crosstalk between nets only becomes important if it is large enough to increase the bit error rate (BER). The coupling has to be fairly high to change the logic level of the signal. Although the susceptibility to noise can increase with lower voltage levels and multi-level signaling such as PAM4.

Mixed-signal designs contain both digital and analog functionalities. For a low level analog signal, a small amount of coupling from a digital signal may completely dominate the desired analog signal. In addition, a design may contain ICs that are sensitive to noise such as a PLL or VCO. As a result, much lower coupling levels are allowable, i.e. greater isolation is needed. Most designers are aware of standard transmission line coupling and can avoid it by placing potential aggressor signals on a different layer or far away from a sensitive analog signal. Furthermore, often in aerospace or test equipment applications, where less of a cost performance trade-off exists, routing density can be decreased with the use of additional PCB layers. In addition, above the board shields can often be afforded

which reduce the coupling between interconnects on the top and bottom layers if properly implemented. For these reasons, it is unlikely that standard transmission line coupling will be an unforeseen issue for these types of high-performance designs.

A common practice in RF PCB design is to place GND area fills to fill all open areas after routing. This practice results in the formation of many parallel-plate cavities throughout the design. Parallel-plate cavities are also formed by power net area fills/planes and neighboring GND fills/planes. It is these parallel-plate cavities that can provide an efficient, but subtle, coupling mechanism between signals in a PCB, even those not in close proximity. A pair of parallel plates is able to propagate a TEM mode with no intrinsic cutoff frequency. Consequently, this coupling mechanism is not associated with higher order waveguide modes that are cutoff before a certain frequency.

Of course, cavities formed by GND area fills should be well connected using vias to prevent the formation of electrically large cavities that can propagate fields. But, if only plated through hole (PTH) vias are used it can be difficult to connect the GND areas adequately due to routing constraints. Further, it is not well defined what the largest allowable spacing between via connections should be to achieve a certain amount of isolation. Parallel-plate cavities formed between PWR and GND obviously cannot be conductively connected so field propagation is unavoidable. The important consideration in this case is to contain the fields to prevent them from coupling through the rest of the design. The parallel-plate noise problem has been occurring for a long time in designs and continues to be an issue. For example, a RF engineer, James Lampen, wrote a poem in the 1990s titled ”Ode to GREENTAPE” which a portion of states “The ground design you generate / Can really, truly, resonate. / Scattering a few vias around/ Should, it seems, suffice for ground” [2]. The author of the poem likely had an unfortunate experience of a LTCC design being ruined due to resonances in parallel-plate cavities. The following subsections will provide the theoretical background necessary for understanding the problem.

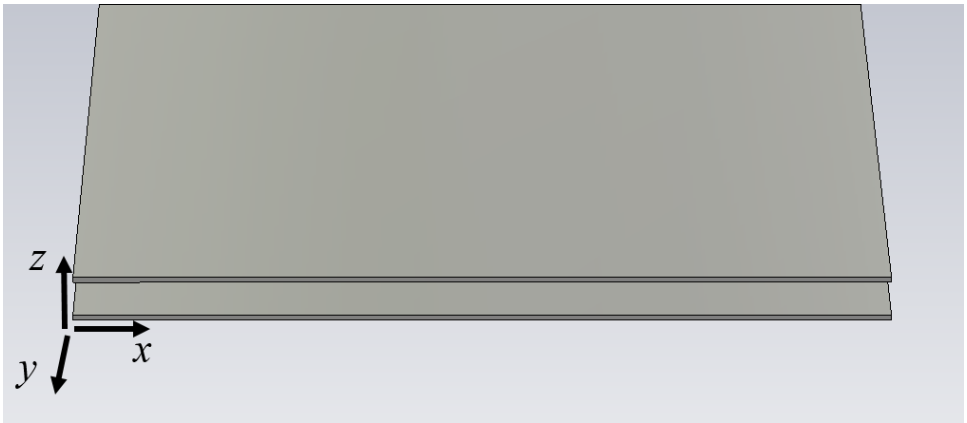

Figure 1.1. A rectangular parallel-plate waveguide.

1.2. PARALLEL-PLATE WAVEGUIDE

Transmission lines are used to guide electromagnetic waves. Transmission lines support a TEM mode where the field distribution is uniform along the cross section with no field components in the direction of the propagation. The transverse fields then satisfy Laplace's equation for electrostatics which means the transverse fields are the same as the static fields [3]. This property allows for well-defined voltages and currents. For instance, in electrostatics the potential on a perfect conductor is the same everywhere so calculating the voltage from the electric field is path independent [3]. In contrast, for higher-order modes, such as the TE_{01} mode of a rectangular waveguide, the electric field varies across the geometry resulting in different voltages depending on the integration path for the electric field. In this case, the voltage is not well-defined. Another consequence of the potential on a perfect conductor being the same everywhere is that two conductors are required for a TEM mode.

A parallel-plate waveguide, shown in Figure 1.1, consists of two conductors so it is capable of transmitting a TEM mode. A parallel-plate waveguide is also capable of supporting higher-order TM and TE modes. The TEM mode solution can be obtained by solving the Helmholtz wave equation or using Laplace's equation. Because it is also

important to have knowledge of at what frequencies the higher-order modes can start to occur, the Helmholtz wave equation will be solved. The following derivation follows from [4]. For a TM solution, there is no magnetic field component in the direction of propagation and a non-zero electric field in the direction of propagation. The direction of propagation is assumed to be in the y-direction. If the width of the parallel plate is much larger than the separation then the x-variation, d/dx, can be approximated as zero. As a result, the problem is reduced to a 2-D problem which can be solved with the 2-D Helmholtz wave equation. The wave equation is solved for E_y and the other field components are obtained by substituting E_y into the Maxwell's equations:

$$\nabla^2 E_y(x,y,z) + k^2 E_y(x,y,z) = 0 \tag{1.1}$$

$$E_y = 0 \; at \; z = 0 \; \& \; z = d \;\; (PEC) \tag{1.2}$$

Separation of variables is used to solve the homogeneous differential equation. Traveling wave solutions are selected for the y-direction and standing-wave solutions are selected for the z-direction resulting in (1.3).

$$E_y(x,y,z) = [A\sin(k_c z) + B\cos(k_c z)][Cexp^{-j\beta y} + Dexp^{+j\beta y}] \tag{1.3}$$

In (1.3), A, B, C, and D are unknown constants. Applying the PEC boundary conditions in (1.2) results in B = 0 and $k_c d = n\pi$ or $k_c = n\pi/d$. There are only outgoing waves which results in D = 0. This results in (1.4), where the constants A and C have been combined.

$$E_y(x,y,z) = A_n \sin(\frac{n\pi z}{d}) \exp^{-j\beta y} \tag{1.4}$$

The remaining field components are obtain by substituting (1.4) back into the Maxwell's equations.

$$E_z = \frac{-j\beta}{k_c} A_n \cos(\frac{n\pi z}{d}) \exp^{-j\beta y} \tag{1.5}$$

$$H_x = \frac{j\omega\varepsilon}{k_c} A_n \cos(\frac{n\pi z}{d}) \exp^{-j\beta y} \tag{1.6}$$

$$E_x = H_z = 0 \tag{1.7}$$

The dispersion relation is (1.8) and the cutoff frequency for the higher order modes can be derived from it and is given in (1.9).

$$k_c = \sqrt{k^2 - \beta^2} \tag{1.8}$$

$$f_c = \frac{k_c}{2\pi\sqrt{\mu\varepsilon}} = \frac{nv_p}{2d} \tag{1.9}$$

Equation (1.9) shows that electrical length of the separation between parallel plates must be greater than $\lambda/2$ for higher order mode propagation. The TEM mode, n = 0, does not have cutoff frequency and only has E_z and H_x components. For the case with a dielectric thickness of 10 mils (254 μm) and ε_r = 4 the cutoff frequency of the first higher-order mode is 295 GHz. As a result, the higher-order modes are not of concern for typical PCB geometries and frequency ranges.

An important result for PCB geometries can be derived by considering a pair of infinite circular plates with a line excitation in the center. This configuration is referred to as a radial waveguide. Obviously no actual PCB geometry has infinite parallel plates, however making this assumption allows for closed-form analytical solutions in the absence of scattering to be obtained. In addition, line excitations are also a mathematical construct, however in PCB geometries the most common excitation is a via that passes through the parallel-plate pair. The size of the via typically much smaller than the parallel plates so the use of a line excitation is reasonable. These closed-form analytical solutions help elucidate the physics of the initial excitation of the parallel plates by a via without becoming too cumbersome. A radial waveguide can support TM_z and TE_z modes. The TM_z modes are of interest in PCB geometries because a TEM mode is possible. The fields of the TMz modes are derived in [5] for the homogeneous differential equation. Equations (1.10-12) are the

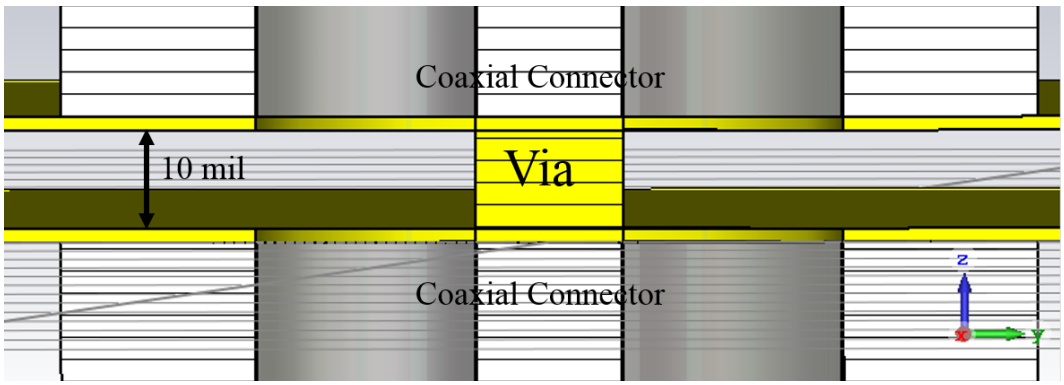

Figure 1.2. Cross-section of a via passing through a parallel-plate pair.

case when n = 0, corresponding to the TM_{z0} mode which is TEM.

$$E_z = -j\frac{\beta_\rho^2 A}{\omega\mu\varepsilon}H_0^{(2)}(\beta_\rho\rho) \tag{1.10}$$

$$H_\phi = -\frac{\beta_\rho A}{\mu}H_0^{(2)'}(\beta_\rho\rho) \tag{1.11}$$

$$E_\phi = E_\rho = H_\rho \tag{1.12}$$

With respect to the parallel-plate surfaces, there is a tangential magnetic field and a normal electric field while the propagation is in the radial direction. Consequently, there are no field components in the direction of propagation and $\vec{E}$ and $\vec{H}$ are perpendicular to each other, illustrating the TEM property of the fields. The higher-order modes are cutoff and the wave impedance for the cutoff modes is capacitive [5].

For comparison with the analytical equations, a simulation model is created in CST Microwave Studio of a pair of parallel plates with a via passing through the plates as shown in Figure 1.2. The time-domain solver is used for the simulation. There are coaxial connectors on the top and bottom with waveguide ports that connect to the via. The dielectric between the two plates is lossless. The model uses dimensions representative of typical PCB geometries with a dielectric thickness of 10 mils, a via diameter of 15 mils, and an

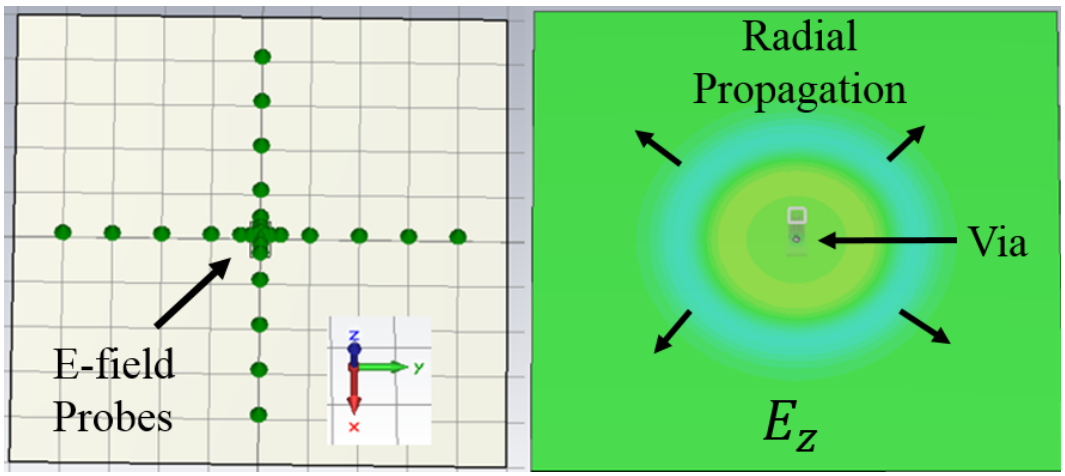

Figure 1.3. E-field probe locations and normal E-field in cavity.

anti-pad diameter of 35 mils. Perfectly Matched Layer (PML) boundary conditions, which absorb the wave incident on the boundary, are used to enforce no scattering (infinite length plates). PML boundary conditions are called "Open" in CST. E-field probes are defined in both the positive and negative x-directions and y-directions as shown in Figure 1.3. The via passing through the parallel plates results in the excitation of a radial wave as seen in the left side of Figure 1.3. As expected from the analytical expressions, the E-field values from the simulation were the same at equidistant points in different directions, indication of the radial propagation. The E-field probe data from the simulation is normalized to one using the E-field value at 50 mils. The simulation data is plotted with the analytical solution to E_z, (1.10), which is also normalized to the value at 50 mils. The two curves agree well as seen in Figure 1.4. The difference could be attributed to not accounting for the finite via radius, the anti-pad, and if the cutoff higher-order modes are not completely decayed at 50 mils. The field strength drops off rapidly initially, but decays much slower at farther distances.

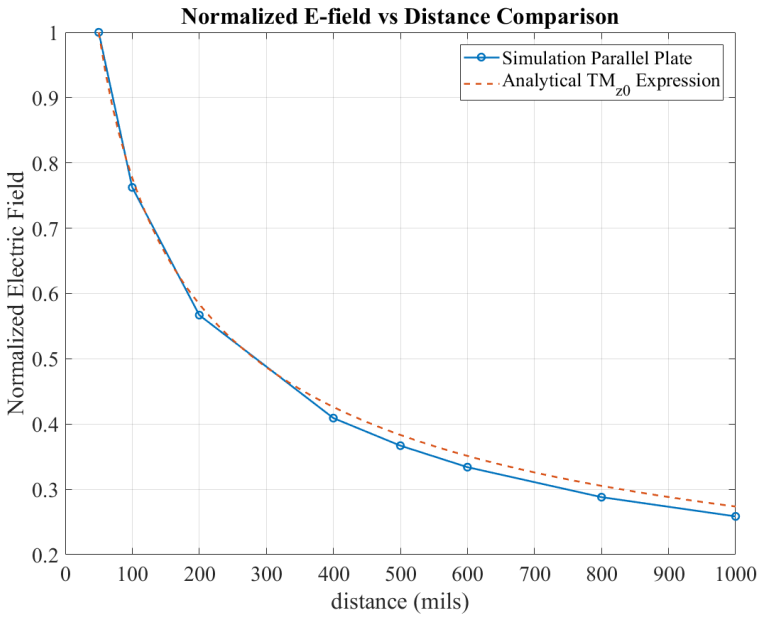

Figure 1.4. Comparison of E_z as a function of distance for simulation and analytical solution.

1.3. PARALLEL-PLATE CAVITY RESONATOR

Assuming infinite parallel plates is important for understanding how the fields of a via can couple to a parallel-plate cavity. By invoking reciprocity, the fields in the parallel-plate cavity can then couple to other vias. However, the scattering of the fields in the parallel-plate cavity needs to be accounted for to determine the field distributions that can be present in the cavity. The waves will scatter when they encounter discontinuities such as apertures in the cavity and the open edges of the cavity. In the frequency domain, the incident and reflected waves can combine constructively and destructively resulting in the formation of standing-wave patterns. The standing-wave patterns are dependent on the boundary conditions, material properties, physical dimensions, and where the excitation occurs. For instance, the dielectric constant of a material will determine the speed that waves propagate through the medium. The speed and physical dimensions will determine

the electrical length of a structure, i.e. how many wavelengths long a structure is. At resonant frequencies, where the waves add constructively, the magnitude of the fields becomes very large which can result in greater coupling.

The cavity model, which was originally developed for analysis of patch antennas, can be used to analyze the standing-wave behavior [6]. More recently the cavity model has been used for the analysis of the power distribution network (PDN) of PCBs [7]. Although the cavities formed in PCB geometries are not completely uniform due to cutouts for anti-pads and vias, discussion of the cavity model can still provide insight to the problem. Complex geometries have been successfully studied with the cavity model by using segmentation techniques [8]. For PCB geometries, the electrical length of the thickness of a cavity is usually much less than a wavelength. As a result, the field variation in the z-direction (along the thickness) can be approximated as zero and the problem simplifies to a 2D problem. The propagating wave solutions, Equations (1.4-1.9), derived earlier in this section were obtained by assuming infinite length plates where scattering was ignored, however for this derivation the standing-wave modes resulting from scattering at the boundary conditions are desired. The boundary conditions on the periphery of the cavity are approximated with perfect magnetic conductor (PMC) boundaries. The 2D Helmholtz wave equation for E_z can be solved and the other field components are obtained by substituting E_z back into the Maxwell's Equations.

$$\nabla^2 E_z(x,y,z) + k^2 E_z(x,y,z) = 0 \tag{1.13}$$

$$H_x = 0 \; at \; y = 0 \; \& \; y = b \;\; (PMC) \tag{1.14}$$

$$H_y = 0 \; at \; x = 0 \; \& \; x = a \;\; (PMC) \tag{1.15}$$

The wave equation is solved through separation of variables. Standing wave-solutions are selected for both the x-direction and the y-direction. The boundary conditions are on $\vec{H}$ which is obtained from E_z using Faraday's Law.

$$E_z(x,y) = [A\cos(k_x x) + B\sin(k_x x)][C\cos(k_y y) + D\sin(k_y y)] \tag{1.16}$$

$$H_x(x,y) = \frac{j}{\omega\mu}[A\cos(k_x x) + B\sin(k_x x)][-Ck_y\cos(k_y y) + Dk_y\sin(k_y y)] \tag{1.17}$$

$$H_y(x,y) = \frac{-j}{\omega\mu}[-Ak_x\cos(k_x x) + Bk_x\sin(k_x x)][C\cos(k_y y) + D\sin(k_y y)] \tag{1.18}$$

Applying the PMC boundary conditions at y = 0 and y = b (1.14) results in D = 0 and $k_y = n\pi/b$, respectively. Applying the PMC boundary conditions at x = 0 and x = a (1.15) results in B = 0 and $k_x = m\pi/a$ respectively. The remaining constants A and C can be consolidated into a single constant A_{mn}. The resulting fields are given in (1.19-1.21).

$$E_z(x,y) = A_{mn}\cos(\frac{m\pi x}{a})\cos(\frac{n\pi y}{b}) \tag{1.19}$$

$$H_y(x,y) = \frac{jA_{mn}}{\omega\mu}\frac{m\pi}{a}\sin(\frac{m\pi x}{a})\cos(\frac{n\pi y}{b}) \tag{1.20}$$

$$H_x(x,y) = \frac{-jA_{mn}}{\omega\mu}\frac{n\pi}{b}\cos(\frac{m\pi x}{a})\sin(\frac{n\pi y}{b}) \tag{1.21}$$

The dispersion relation is (1.22) and can be rearranged to obtain an expression for the resonant frequencies of the cavities (1.23).

$$k^2 = k_x^2 + k_y^2 = \omega^2\mu\varepsilon = (\frac{m\pi}{a})^2 + (\frac{n\pi}{b})^2 \tag{1.22}$$

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{(\frac{m\pi}{a})^2 + (\frac{n\pi}{b})^2} \tag{1.23}$$

Equation (1.23) for the resonant frequencies can be used to determine when the first resonance occurs based on the geometry and material properties. If the highest frequency of interest in a design is greater than the first resonant frequency of the cavity, the resonances of the cavity need to be considered. The derivation of the cavity model contained here solves the homogeneous differential equation, but does not solve the inhomogeneous differential equation with the excitation. A Green's function of the 2-D Helmholtz equation can be used to solve the inhomogeneous differential equation. In [7], the inhomogeneous differential equations is solved to obtain the impedance matrix where finite length ports can be placed at different locations. An important result is that the impedance looking into the cavity varies with position, i.e. what modes are excited and how strongly they are excited is position dependent. Conductor and dielectric loss is accounted for with a complex propagation constant that uses the standard low-loss approximation.

The parallel-plate PWR/GND cavity has the same structure as a microstrip-patch antenna which is why the cavity model works well for its analysis. It follows that noise coupled to the parallel-plate cavity can excite resonances and result in radiation [9]. This radiation is primarily an EMC radiated emissions issue, i.e., causes the product to exceed the field strength limit for radiated emissions in EMC compliance testing. But the radiation could cause an inter-system interference issue as well. This radiation is typically mitigated by stitching the sides of PCBs with vias and edge plating [10]. Because this work is concerned with coupling mechanisms within a PCB, the radiation from the PCB edges will not be discussed further in this work.

An important concept with dealing with resonant structures is the quality factor or Q. The Q is a measure of the loss of a resonant circuit and is obtained by dividing the stored energy with the power loss. A high Q corresponds to low loss which results in very high field strength at resonance for a cavity resonator. For unintended resonances, loss is desirable to dampen the resonance or lower the Q. Analytical expressions for the Q of a parallel-plate cavity can be derived from the fields obtained using the cavity model. The

conductor loss is obtained by calculating the power dissipated in the finite resistance of the top and bottom plates where the surface current density is obtained from $\vec{J}_s = \hat{n} \times \vec{H}$, by approximating the conductor as a PEC. The dielectric loss is obtained by performing the volume integral of $\frac{1}{2}\omega\varepsilon''|\vec{E}|^2$ over the structure. The stored magnetic and electric energy are obtained by performing the volume integral of $\frac{1}{4}\mu|\vec{H}|^2$ and $\frac{1}{4}\varepsilon|\vec{E}|^2$ over the structure. From the stored energy and the loss of the cavity, equations for the Q can be obtained (1.24-26).

$$Q_{conductor} = \frac{d}{\delta_s} \tag{1.24}$$

$$Q_{dielectric} = \frac{1}{\tan\delta} \tag{1.25}$$

$$\frac{1}{Q_{total}} = \frac{1}{Q_{conductor}} + \frac{1}{Q_{dielectric}} \tag{1.26}$$

The PMC boundary conditions used in the cavity model do not account for the radiation loss which also impacts the overall Q. However, previous research has shown in general for PCB geometries the radiation loss is much less than conductor and dielectric loss [11]. From (1.24) and (1.25) it is clear that two design parameters impact the Q: the $\tan\delta$ of the dielectric material and the thickness, d, of the dielectric material. The skin depth, δ_s, of the metal is essentially fixed as only copper is used in standard PCB fabrication. The dielectric thickness is dependent on the number of layers, the desired finish board thickness, and the standard thicknesses of a dielectric material available from the manufacturer. The designer in some cases may have some control in selecting a dielectric thickness between two layers. More often, the dielectric material is a key design parameter. For applications where signal attenuation needs to be minimized, such as in RF designs or high-data rate digital designs, a lower-loss dielectric material is used instead of low-cost FR-4. Low-loss dielectric substrates such as Rogers RO4000 series or Megtron 6 have a much lower $\tan\delta$ resulting in an increase in Q. To provide an illustration, the simulated coupling in linear scale between two vias for a 2"x 2" cavity with FR-4 dielectric ($\tan\delta = 0.025$), and a 2"x 2"

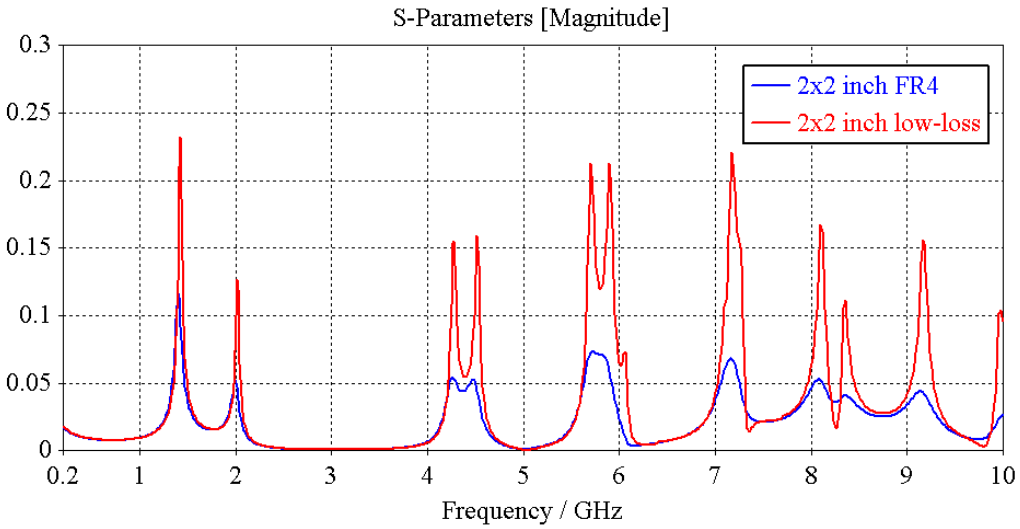

Figure 1.5. Comparison of simulated coupling between vias in a cavity for lossy (FR-4) and low-loss dielectric material.

cavity with a tan δ of 0.003 is shown in Figure 1.5. The coupling magnitude of the low-loss dielectric cavity is 2-3 times greater at resonant frequencies than the FR-4 cavity coupling magnitude. Therefore, the parallel-plate coupling mechanisms are much more severe in PCBs that use low-loss dielectric materials. In addition, in [12] it was shown that smaller sized cavities resonate stronger. The low-loss materials used in some IC packages can result in even larger Q-factors. For instance, a glass interposer used for 2.5D IC integration resulted in very strong coupling at resonant frequencies due to the very low loss of the glass material [13].

1.4. PARALLEL-PLATE NOISE IN THE LITERATURE

Sometimes, this form of coupling is called parasitic coupling to distinguish it from proximity coupling as it is the result of electromagnetic wave propagation on waveguide structures that were not intentionally designed to do so [14]. This type of coupling related to the PWR/GND structures is often referred to in the literature as simultaneous switching

noise. Simultaneous switching noise is referencing when multiple transistors are switching simultaneously which injects multiple noise sources into a PWR/GND structure. Another related term is ground bounce which is referencing the fact that due to the field distributions that can occur in a cavity there can be locations where the voltage (E_z) is no longer zero as assumed in circuit theory analysis. Still, these names do not entirely elucidate the physics of how noise is coupled to the cavity and how the fields in the cavity couple to traces or vias. Further, some of the papers discussing this topic do not explicitly explain the physics of these phenomenon. There are still papers that explicitly reference the physics which will be referenced throughout. A review of the relevant literature is included throughout Section 2.

Overall, there is very little literature on obtaining high isolation in PCB designs. Searching the IEEE database for "noise isolation" primarily yields a paper discussing the use of via fences around striplines and microstrips for isolation in RF multi-chip packages [15]. This practice is primarily aimed at minimizing transmission line crosstalk, but also helps suppress parallel-plate cavity noise. Despite the lack of literature for achieving high levels of isolation, there is some literature for how to suppress parallel-plate cavity noise which is often critical for achieving high isolation. However, a majority of the recent literature in this area discusses using Electromagnetic Bandgap (EBG) structures for suppressing parallel-plate noise such as [16]. For EBG structures, one of the planes is patterned with narrowly connected patches in such a way to suppress the propagating waves in the parallel-plate cavity which creates a stopband for a range of frequencies. Utilizing more complex EBG patterns can yield stopband bandwidths around 4 GHz and stopband attenuation of about 40 dB [17]. Still, the EBG structures have not been used much in industry for several reasons. For example, the patterning essentially prevents the planes from being used as a reference plane for transmission lines because of the gaps. Consequently, the use of EBGs will likely necessitate an increase in the layer count of a PCB. In addition, the narrow connections may have IR-drop or thermal consequences in high-power applications such as the power net

area fill for a power amplifier. Another reason for the lack of adoption is that in most designs the parallel-plate cavity noise is created by switching digital circuits which is broadband noise while the EBG bandwidth is finite. Despite the implementation issues, EBGs may be a potential solution for achieving higher isolation in some applications. There are many topologies and permutations of EBGs which has resulted in numerous publications, dominating the more recent literature on parallel-plate noise. Placement of capacitors is another mitigation strategy that has been studied and suggested in the past for dampening the resonances [18]. The mounting inductance of SMT capacitors typically limits their efficacy at higher frequencies. The effect of capacitors is discussed extensively in Section 4.

1.5. OVERVIEW OF THE REMAINING SECTIONS

Understanding the noise coupling mechanisms related to the parallel-plate cavities is often critical for obtaining high isolation in RF & mixed signal PCB and package designs. Noise coupling in complex PCB designs can be better understood by breaking up the overall coupling mechanism into smaller portions. For example, a via can couple to a cavity, and then the first cavity can couple to another cavity where a via in that second cavity can be coupled to. This work will first discuss basic coupling mechanisms in Section 2 and then will analyze more complex test vehicles in Section 3. The focus will be on qualitatively understanding the physics underlying the coupling mechanisms. This knowledge can then be exploited in the full-wave EM simulation tools for proper identification and mitigation of this noise coupling mechanism. Section 4 will analyze how the active and passive components influence the coupling and how the coupling can be predicted in the final PCB assembly. Section 5 will provide design recommendations for minimizing the parallel-plate noise in mixed-signal designs.

2. BASIC PARALLEL-PLATE COUPLING MECHANSIMS

2.1. ELECTRIC FIELD AND MAGNETIC FIELD COUPLING

It is important to develop a fundamental understanding of electric field coupling and magnetic field coupling in order to diagnose coupling mechanisms in PCB geometries. The Maxwell equations are linear if the constitutive parameters, μ and ϵ, are assumed to be linear. For linear systems, superposition applies which allows for the coupling to be analyzed in the absence of other fields. The coupled fields can then be added to the original fields to obtain the final field distribution. Another important principle in the analysis of coupling mechanisms in PCB geometries is that there is typically no field penetration through conductors. At the frequencies of interest, the skin depth of copper is much less than the thickness of the copper layer in a PCB thus there is negligible field penetration through conductors. For example, at 100 MHz the skin depth of copper is about 0.25 mil As a result, a conductor will have two distinct surfaces with two distinct surface currents. To simplify analytical analysis, good conductors such as copper are modeled as Perfect Electrical Conductors (PECs) at high frequencies. For a PEC, free electrical charges are contained in an infinitesimally thin layer on the surface of the conductor.

Electric field coupling is derived from the Ampere-Maxwell law where a changing electric field or a conduction current induces a circulating magnetic field. For instance, consider the case where a changing electric field is applied to the middle of a stripline as shown in Figure 2.1. The changing electric field produces a circulating magnetic field where the magnetic field is in different directions on each side of the electric field. If the conductor is approximated as a PEC, the $\vec{J}_s = \hat{n} \times \vec{H}$ boundary condition can be used find the current density which shows that the current density is traveling in opposite directions from the changing electric field as seen in Figure 2.2. The electric field is in the same direction

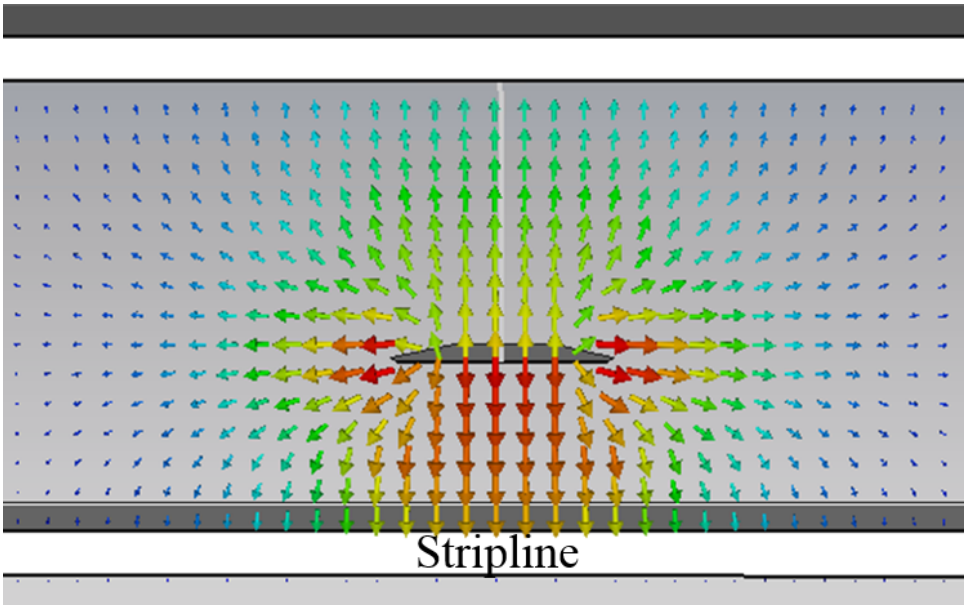

Figure 2.1. Electric field source coupling to stripline.

on both sides while the magnetic field is in opposite directions. Therefore, by the Poynting vector energy is flowing in opposite directions. As a result, two propagating TEM waves travelling in opposite directions are being guided on the stripline. Because the electric field is in the same direction the voltage will have the same polarity at both ends of the stripline. If a closed contour was place between the stripline and the reference plane and symmetric about the electric field injection point, the net magnetic flux density through the surface formed by the contour would be zero because the magnetic field is circulating.

Magnetic field coupling is derived from Faraday's Law which states that a time changing magnetic field induces a circulating electric field. For example, consider the case where a small current loop next to a stripline is excited. The current loop produces a magnetic field with a portion of the magnetic field wrapping the conductor. Consider a closed contour defined between the stripline and the top reference plane. The magnetic field penetrates the surface created by the contour and circulate back on themselves by passing between the bottom of the stripline and the bottom reference plane. As a result,

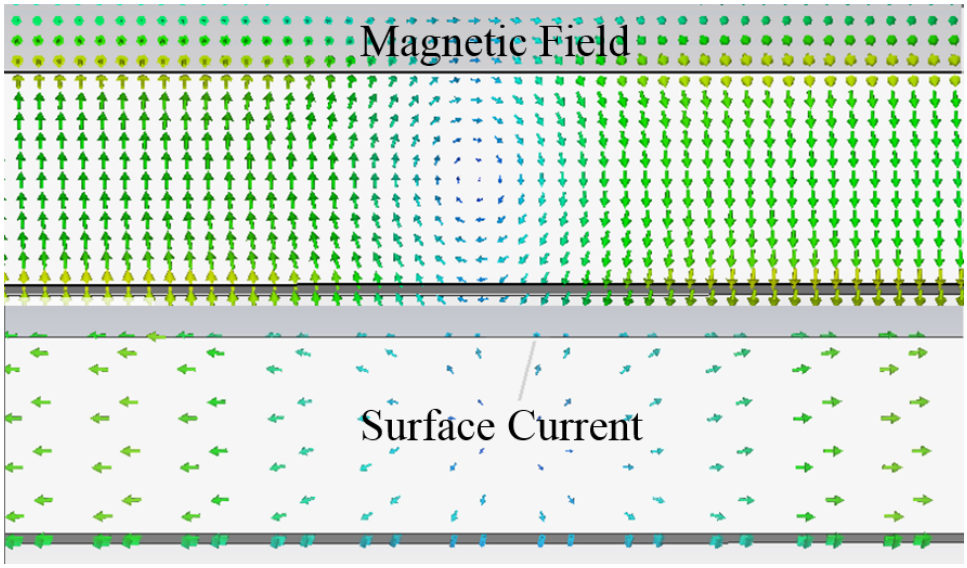

Figure 2.2. Magnetic field and surface current density on electric field coupled stripline.

there is a time changing magnetic flux density that produces an electric field. Electric fields produced by the time changing magnetic fields must circulate back on themselves. For actual conductors with finite conductivity, there will be a portion of the electric field parallel to the conductor that drives conduction current (emf). The direction of the electric field circulation is such to drive a conduction current to oppose the changing magnetic flux density. If the conductor is modeled as a PEC, the tangential electric field at the conductor surface must be zero. The vertical electric fields on each side of the magnetic field are in opposite directions as seen in Figure 2.4. If the $\hat{n} \bullet \vec{D} = \rho_s$ boundary condition is applied, the surface charge density on the conductor at the two locations will have opposite polarities showing a difference in potential. The magnetic field is in the same direction while the electric field is in opposite directions. Because the magnetic field is in the same direction the surface current is in the same direction. Applying the Poynting vector, power flow is opposite for the fields on each side of the excitation. The polarity of the voltage drop at each end of the transmission line is opposite. Two propagating TEM waves travelling in opposite directions are being guided on the stripline.

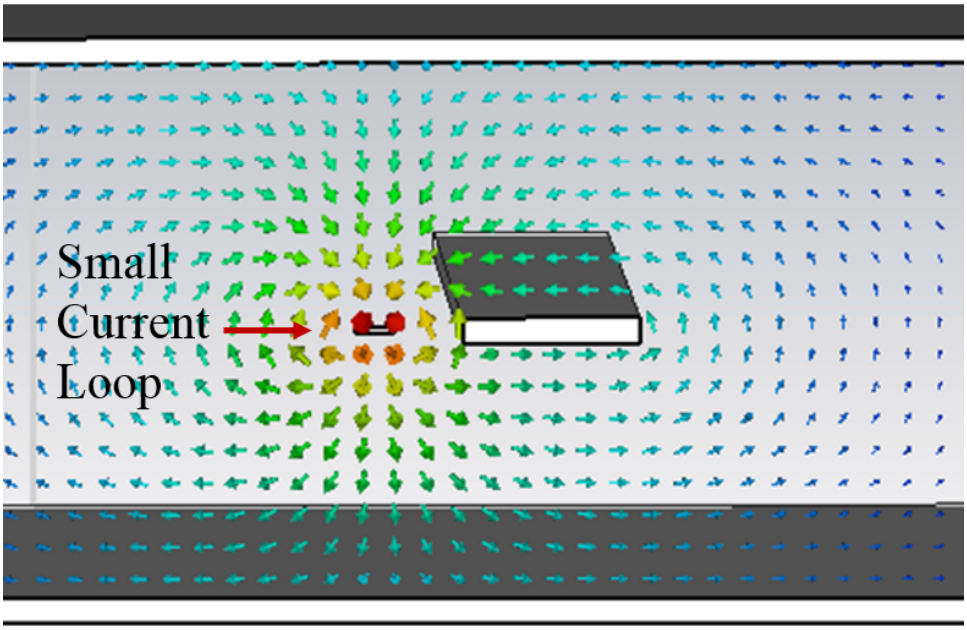

Figure 2.3. Magnetic field source coupling to stripline.

Circuit parameters are more intuitive to most engineers and easier to work with so transmission lines are typically modeled using distributed lumped circuit elements. The transmission line telegrapher's equations solve the wave equation with voltage and current rather than fields. The magnetic field is represented with an inductance and the electric field is represented with a capacitance. As a result of the TEM field structure of a transmission line, these lumped element models can be developed from the Maxwell's equations directly. Another important result of the TEM fields is that static solvers can be used to obtain the capacitance and inductance. Using the lumped element models, electric field coupling is replaced with capacitive coupling where current is injected in to the victim line through the mutual capacitance. If the transmission line structure is uniform, the current will see an equal impedance in both directions so half the current will travel forwards and the other half of the current will travel backwards. This property will result in the same polarity voltage drop across the termination on each end of the structure which as expected agrees with the result from analyzing the fields directly. Magnetic field coupling is replaced with

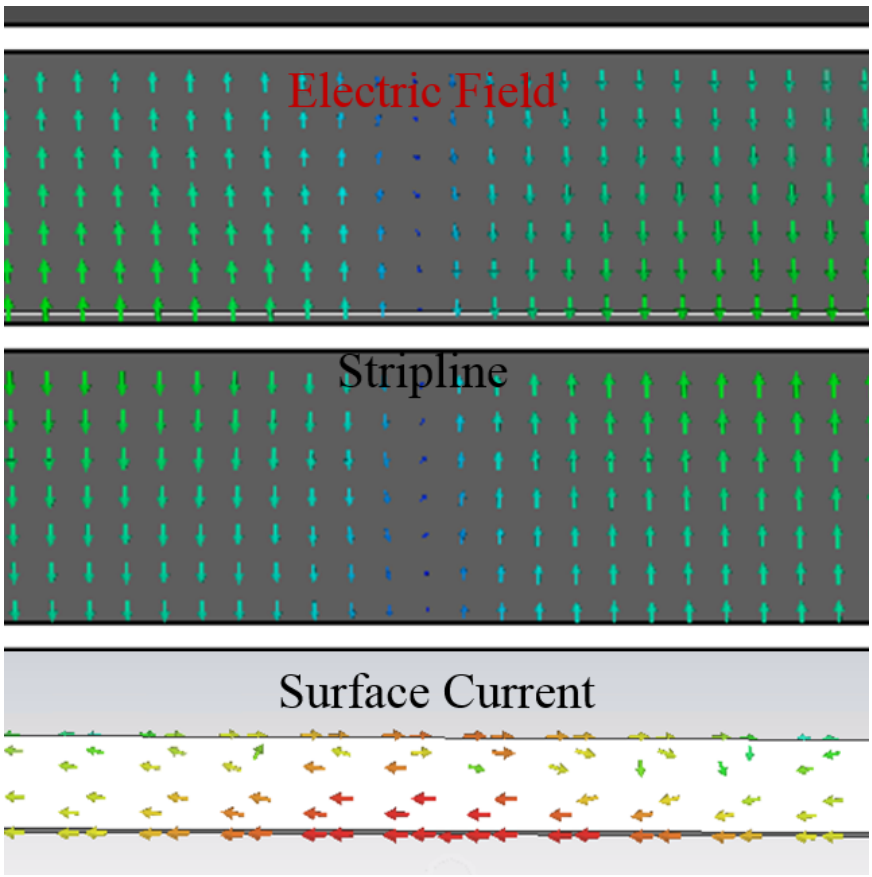

Figure 2.4. Magnetic field source coupling to stripline.

inductive coupling where a time-changing current induces an emf or series voltage source in the victim. A current will be driven by this series voltage which results in current flowing in one direction. As a result, the polarity of the voltage drop across the termination of each end of a structure will be opposite. This result again agrees with the fields where two waves are propagating with magnetic fields in the same direction and with normal electric fields in opposite directions. The above results can be used to analyze the coupling response to determine if the magnetic field (inductive) coupling or electric field (capacitive) coupling is the dominant coupling mechanism. For instance, if inductive coupling dominates the polarity of the voltage drop at the measurement port on each side of the transmission line will be opposite. In the frequency-domain, the phase of the voltage will be opposite. When

the terminations of the transmission line are not matched the coupling response becomes more complicated. This mismatch will introduce reflected waves to satisfy the boundary conditions. At frequencies where the geometry is electrically small, transmission line effects can be neglected and the analysis of the effect of a termination simplifies. For example, for a high impedance termination even a small noise current can create a large voltage drop across the high impedance. Capacitive coupling is then more of an issue for high impedance terminations. In comparison, a series voltage induced by inductive coupling will not drive much current in a high impedance circuit.

For transmission lines in a homogeneous medium, such as a stripline, the inductive coupling and capacitive coupling are equal. Near end cross talk (NEXT) and far end cross talk (FEXT) are used to describe the crosstalk for coupled transmission lines. Because the phase is opposite for the inductive coupling and capacitive coupling they cancel each other out at the far end and add together at the near end where they are in phase. The physics that describe crosstalk are the same physics used to design directional couplers which is why transmission line couplers are reverse couplers (near end is the coupled port). A microstrip is not a homogenous medium as some of the fields travel in air and some travel in the dielectric so the inductive coupling and capacitive coupling do not cancel each other out. The fields travelling in air have a different velocity than the fields traveling in the dielectric which is why there is not cancellation. The fields of the microstrip on the edges fringe out farther compared to the fields of a stripline which are more contained because of the second reference plane. As a result of the fringing fields for the microstrip, the microstrip coupling drops off slower than stripline coupling. These two reasons are why stripline routing is regarded as superior for minimizing crosstalk. Extensive treatment of transmission line coupling can be found in [1] and [3].

2.2. VIA TO VIA COUPLING WITHIN A PARALLEL-PLATE CAVITY

In the introduction section, it was demonstrated that a via penetrating a pair of parallel plates excites a radial TEM wave. By reciprocity, because the vias are able to excite the cavities they are also able to be coupled to by fields in the cavity. Analytical solutions for a radial waveguide or radial transmission line were published in electromagnetics textbooks long before it became an issue for PCB geometries [19]. Publications regarding coupling to the parallel plates and their consequences for PCBs began to appear in the early 1990s. There are many publications covering via coupling and this background is not comprehensive listing of all of them. In 1993, a paper illustrated that at higher frequencies the parallel plates used for power distribution needed to be modeled as a parallel-plate waveguiding system for accurate prediction of "Delta-I noise" [20]. Previously, only inductive effects had been considered. This "Delta-I noise" is another name for the "Simultaneous Switching Noise" (SSN) mentioned in the introduction. The first analytical method for calculating coupling between vias used admittance matrices to describe the parallel-plate modes responsible for the coupling, but was restricted to infinitely large parallel plates as edge reflection was not considered [21]. In 1995, [22] presented field plots from full-wave simulation showing the excitation of the radial TEM waves at a via transition and created a circuit model with dependent sources to capture the mode conversion. Coupling of energy to an undesired mode can be referred to as mode conversion. In [23], analytical expressions for via coupling were developed from radial transmission line theory that accounted for reflections from finite boundaries and time-domain plots were presented to show reflections off the finite boundaries. In [24], analytical expressions were derived that incorporated multiple scattering from other vias in the cavity using the Foldy-Lax equations, although only circular cavities could be used. An excellent analytical treatment of the via and parallel plate geometry is available in [25]. The paper solves the inhomogeneous differential equation using the Green's function and accounts for the finite via radius and incorporates different boundary conditions. The goal of the paper was to obtain analytical formulas for the via

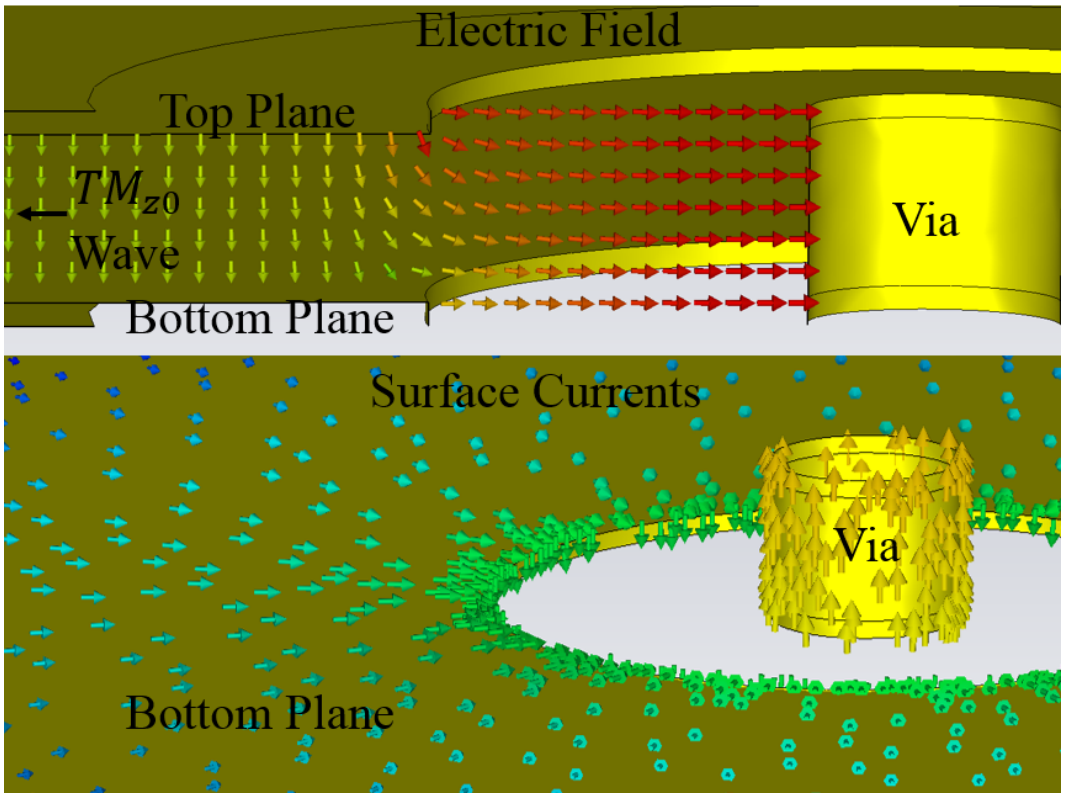

Figure 2.5. Electric field and surface currents for via passing through cavity with absorbing boundary conditions to prevent standing-wave patterns.

plate capacitance that is dependent on the higher order modes. More recently, a physics-based via circuit models with the via plate capacitance from [25] and impedance matrices for the parallel-plate pair was used to study the effect of different dielectric thicknesses and ground via patterning on the via crosstalk [26]. The parallel-plate impedance matrices captures the coupling between vias due to the dominant TM_{z0} propagating mode. In [27], the accuracy of the physics-based circuit model was evaluated and found that coupling due to the higher order TM_z modes only needs to be considered for very closed spaced vias such as those closer than 30 mils for typical dielectric thicknesses. In [28], the intrinsic circuit model for multiple vias was presented which extends the the physics-based via circuit model to accurately model field effects of the higher-order modes for vias in close proximity.

The radial waveguide equations in [5] are derived from the z-component of the vector potential $\vec{A}$, assuming a line current source in the z-direction. Therefore, the existence of a current on the via excites the TM_z fields in the cavity. Alternatively, the fields in the parallel-plate cavity can be obtained from equivalent, fictitious magnetic currents in the coaxial via/antipad aperture, which are dependent on the electric field [25]. The electric field in the coaxial aperture is also an excitation for the TM_z fields in the cavity. Another way to look at the coupling is in terms of mode conversion: the TEM coaxial mode in the anti-pad aperture is converted into TM_z modes in the parallel-plate cavity and then converted back into a TEM coaxial mode in the antipad aperture in the next plane [25]. The impedance of the higher-order TM_z modes that are cutoff is capacitive, representing stored electrical energy [5]. The stored energy associated with the higher-order modes is then converted back to a coaxial TEM mode in the antipad aperture, but some energy is lost as a result of the propagating TM_{z0} mode. The reason for this excitation is also sometimes explained as a return current path discontinuity [29]. For TEM or quasi-TEM transmission lines, the return current (an image current) flows on the reference plane next to the signal conductor. Figure 2.5 shows the electric field around the via passing through a pair of parallel plates and the surface currents on the via and the bottom plate. The surface currents inside the anti-pad plane aperture are in the opposite direction of the currents on the via. At a via transition (through at least one plate pair), the return current needs to change reference planes and does not have a well-defined conduction current path to do so in most cases. In order to satisfy Maxwell's continuity equation (KCL that includes displacement current), a displacement current must exist between the two plates. Therefore, the existence of the radial wave seen in Figure 2.5 is required to satisfy the continuity of current and is said to be the return current path for the via currents.

There are multiple factors that influence the strength of the coupling, many of which are clearly illustrated in the background literature. For instance, analytical expressions in [23] show that the magnitude of the coupled TM_{z0} wave is directly proportional to the

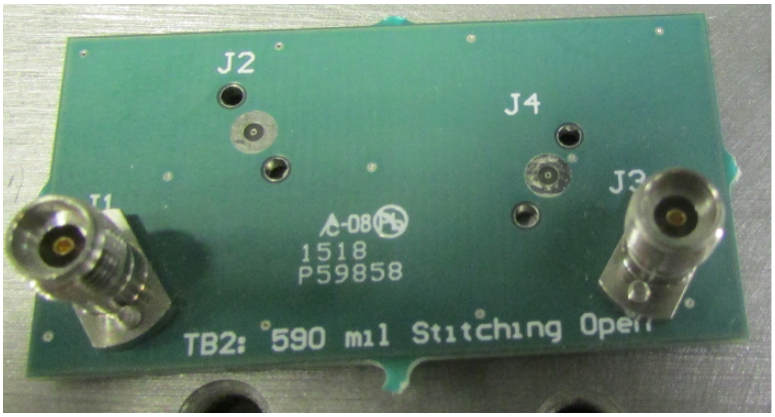

Figure 2.6. Test board for measuring coupling between two vias in a cavity.

height of the parallel-plate cavity, i.e. the dielectric thickness. Parametric studies in [26] agree with the analytical expressions and show the coupling is directly proportional to the dielectric thickness. As shown in the introduction, the dielectric loss affects the magnitude of the field strength at resonant frequencies and is an important factor in the coupling. Basic test vehicles were created to study the coupling among vias in a single parallel-plate cavity. Figure 2.6 shows an example of one of the test vehicles. A 2-layer PCB stack-up is used with a dielectric thickness of 62 mils which is much larger than the typical 5-10 mil dielectric layer thickness of most PCBs. Still, the dielectric thickness is electrically small (less than $\lambda/10$) until about 10 GHz and only the fundamental TM_{z0} mode is propagating. Because of the larger thickness, the cutoff modes may not be fully decayed until a greater distance compared to a thinner cavity. Overall, the structure of the fields will be the same as a thinner cavity. The measured coupling between one excitation via and two other vias is shown in Figure 2.7. For the blue curve, the victim via is 570 mils away from the excitation and the distance is 1500 mils for the red curve. The coupling to each via is on the same order of magnitude despite the varying distances between the excitation via. The coupling clearly exhibits resonant behavior as there are peaks in the coupling. The modal resonances of the cavity will result in coupling maxima if the excitation via excites that resonance and

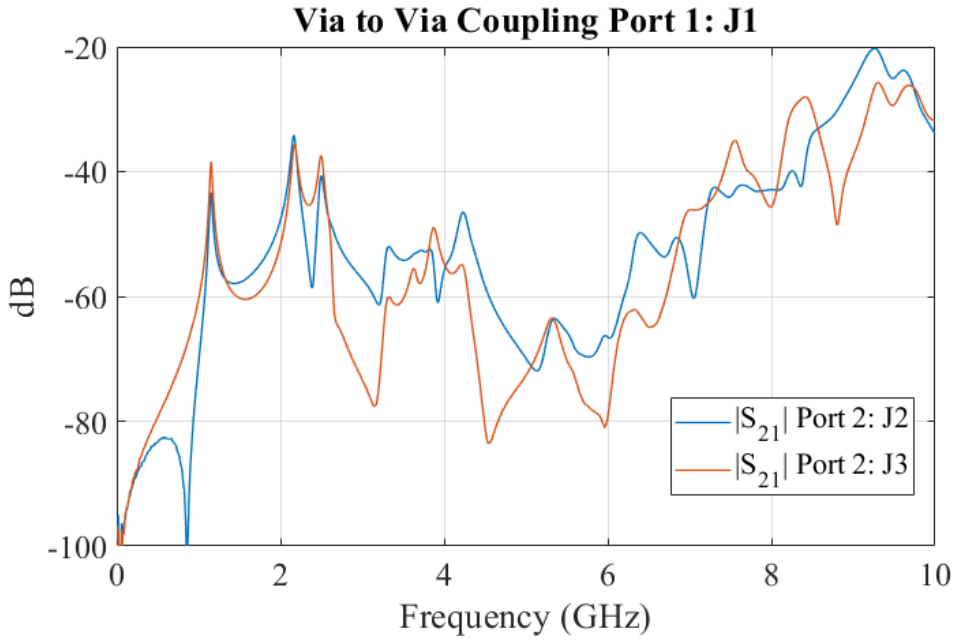

Figure 2.7. Measured coupling between vias in 62 mil thick parallel-plate cavity.

the victim via is not located close to a null in the field distribution of that resonance. As a result, when the cavity is electrically large the position of the two vias relative to the modal field distribution is the most important factor for the amount of coupling. To further illustrate this, two full-wave simulation models of the parallel-plate cavity with vias are created: one with absorbing PML boundary conditions and another with PMC boundary conditions that result in total reflection at the open edges. Figure 2.8 shows a comparison of the simulated coupling of the two models. If the resonances are eliminated, as with the PML boundary conditions, the coupling is much lower. Figure 2.9 shows the measurement of a cavity with 590 mil GND via spacing with different termination for the vias that form the measurement ports. In one configuration the vias are not connected to the cavity, in another configuration the vias are shorted to the bottom plane, and in the final configuration the vias are connected to the bottom plane through two 0201 100 ohm resistors to form a 50 ohm termination. The shorted configuration results in the greatest coupling and the open configuration the least coupling. The parallel plate is excited by the current on the

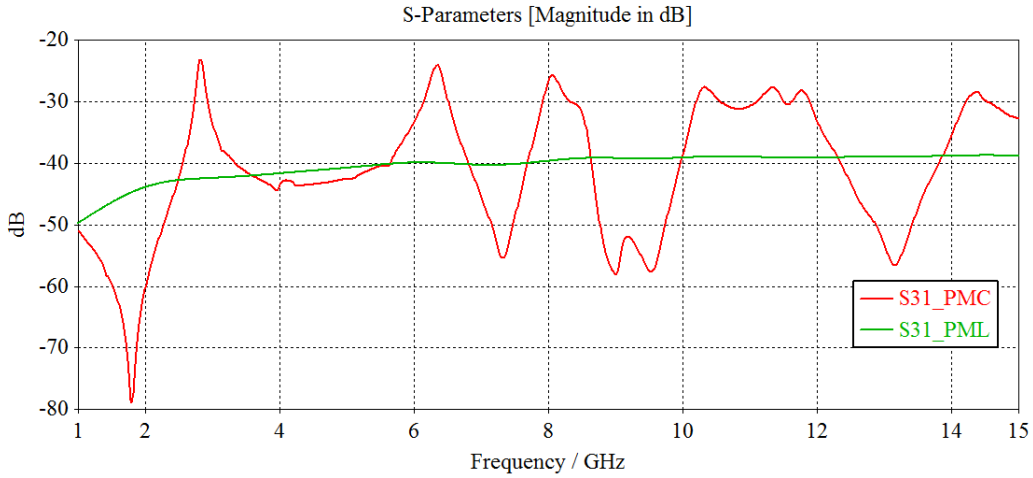

Figure 2.8. Simulated coupling comparison between vias in parallel-plate cavity with PML B.C. and PMC B.C.

via so it is expected that the strength of the excitation and thus the coupling increases with increasing current. At a PEC, the tangential electric field must go to zero so a scattered field must be produced to cancel out the incident electric field. This scattered field results in an increase in the total magnetic field around the via and thus current. The terminated via configuration is most representative of actual geometries as a via is typically connected to a transmission line or IC on where most of the energy is delivered. The vias shorted in the plane is representative of the stronger excitation that occurs for a PWR/GND cavity. Another important consideration in the coupling is how various scatterers, e.g. shorting vias and apertures, within a cavity influence the coupling. Full-wave simulation can be used to analyze the coupling in a specific geometry, but more insight is desired for design guidelines. For the case of parallel-plate cavities formed by two GND area fills, stitching vias can be used to limit the excitation of the cavity. Via stitching is investigated further in Section 5.

It can also be relevant to understand the coupling between vias in the absence of modal resonances. For example, if the frequency of the noise exciting the parallel-plate cavity is below the first resonant frequency of the cavity. As long as the vias are not very

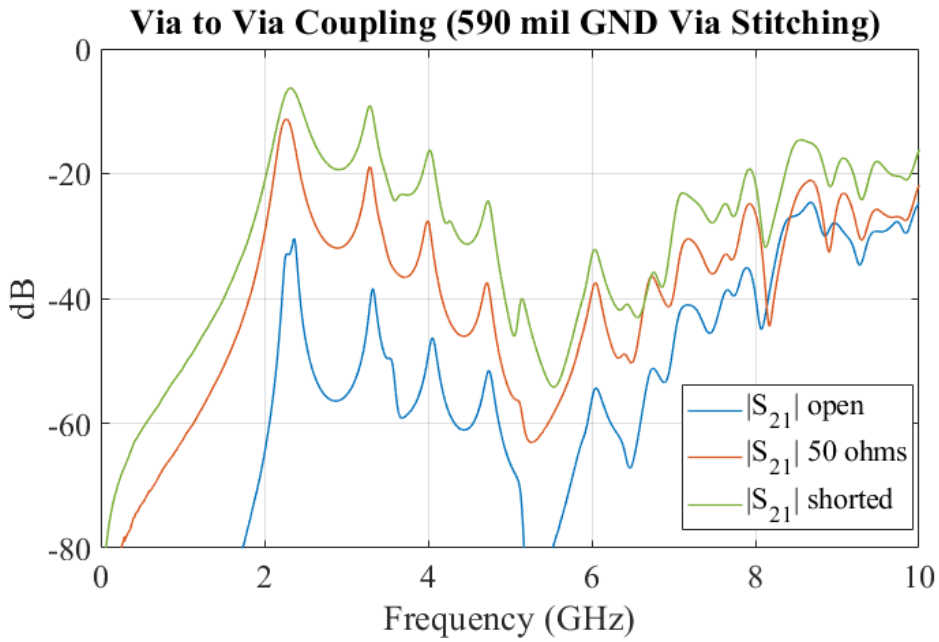

Figure 2.9. Measured coupling between vias: short, open, 50 ohm comparison.

closely spaced, e.g. 30 mils or less depending on the dielectric thickness, the coupling is only due to the propagating TM_{z0} mode. A simulation model was created to simulate the coupling between two vias at varying distances with scattering off the cavity edges removed via absorbing PML boundary conditions. Figure 2.10 plots the simulated coupling in linear scale for vias with a 100 mil separation, a 500 mil separation, and a 900 mil separation. The coupling for the 100 mil case is about twice the 500 mil case while the reduction in coupling between the 500 mil case and 900 mil case is even less. Overall, the coupling between vias is not strongly dependent on the distance between the two vias. The reason for this is the field strength of the propagating TM_{z0} fields is dependent on the Hankel function of the 2nd kind which decreases quickly initially, but then decreases at approximately a $1/\sqrt{x}$ rate subsequently. Figure 2.11 plots the magnitude of the E-field and H-field as a function of distance, where the field strength has been normalized to 1 at 50 mils. As a result, after the quick initial decrease the coupling is only weakly dependent on distance.

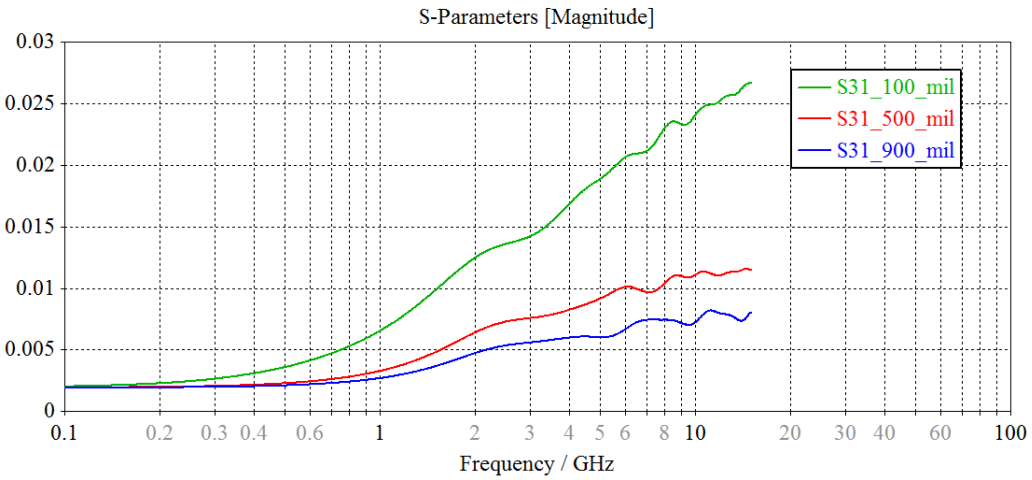

Figure 2.10. Simulated coupling distance comparison between vias in parallel-plate cavity with PML boundary conditions.

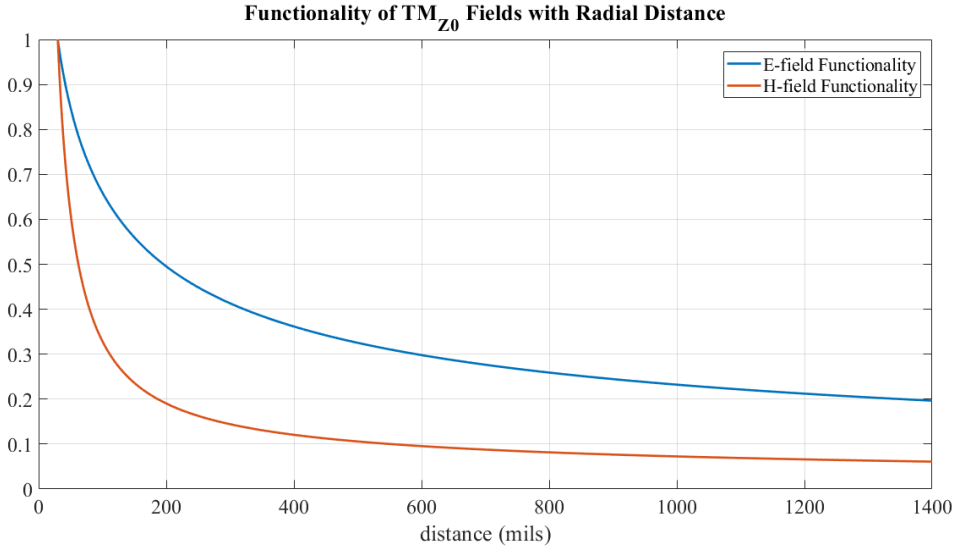

Figure 2.11. Magnitude of TM_{z0} fields as a function of distance.

2.3. PARALLEL-PLATE CAVITY COUPLING TO CBCPW

A conductor-backed coplanar waveguide (CBCPW) is a transmission line structure that occurs commonly in RF PCBs where GND area fills are often placed on the outer layers. The CBCPW transmission line mode is a combination of a microstrip mode and a CPW mode. CBCPW is also common in MMIC designs and can also be created when a MMIC with no ground plane with coplanar waveguide (CPW) transmission lines is mounted on a metal base. CBCPW is sometimes referred to as ground-backed coplanar waveguide (GBCPW) as well. Coupling or power leakage between a CBCPW and a parallel-plate cavity was first mentioned in the literature in 1986 [30]. Although, the paper did not provide any quantification of the amount of coupling or mitigation strategies. Subsequent papers by other authors elaborated on the coupling mechanism between the CBCPW and the parallel plates including [31]. [32] contains an analysis of using shorting vias as a suppression technique by deriving analytical expressions to evaluate the leakage loss as a function of different design parameters such as the shorting via spacing. Modes that lose energy due to coupling into the substrate are sometimes referred to leaky modes. The use of this term is contingent on the parallel plates being assumed to be infinite. [32] was primarily concerned with minimizing the power leakage loss to the parallel plates and did not incorporate scattering effects from the edges of finite size parallel plates. Other papers considered the effect of the finite size of the parallel plates and its consequences. [33] used test vehicle measurements to demonstrate the efficacy of different via stitching strategies for suppressing resonances associated with finite size of the cavity and showed that the resonances can be predicted analytically by the cavity model. These resonances result in dips or dropouts in the insertion loss.

Although it is known that stitching vias can minimize the coupling to parallel-plate modes, to understand the excitation of the parallel plates it is best to analyze the case without vias. As mentioned previously, a CBCPW mode is a combination of the CPW mode and microstrip mode as can be seen in Figure 2.12. Some of the electric field lines terminate

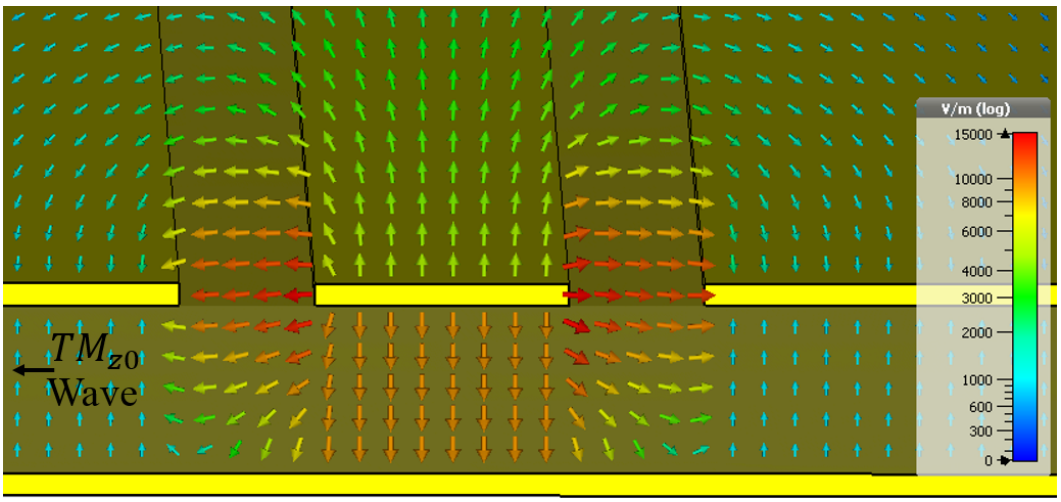

Figure 2.12. Electric field cross-section of CBCPW in logarithmic scale.

on the top reference plane and some terminate on the bottom reference plane. A potential difference between the bottom side of the top reference conductor and the top side of the bottom reference conductor is created. Modeling the conductors as PECs and applying the $\hat{n} \bullet \vec{D} = \rho_s$ boundary condition yields a difference in surface charge density between the two conductors. Because of the potential difference there will be a normal electric field. As a result, the parallel-plate TM_{z0} mode is excited. The physics are clearer when the reciprocal case of the cavity coupling to the CBCPW is considered. The cavity is excited which results in the normal electric field between the two planes. At the gap between the CBCPW signal conductor and top reference conductor the electric field fringes out and terminates on the side of the top reference conductor as seen in Figure 2.13. As a result, a potential difference is formed between the signal conductor and top reference conductor, exciting a slotline mode. Coupling to only one side of the CBCPW primarily excites a slotline mode rather than the complete CBCPW mode. This coupling mechanism or mode conversion is very similar to the case of a microstrip crossing a gap in the reference plane which results in some mode conversion to the slotline mode. A detailed description of the physics of the microstrip to slotline mode conversion from a gap crossing can be found in [34]. The

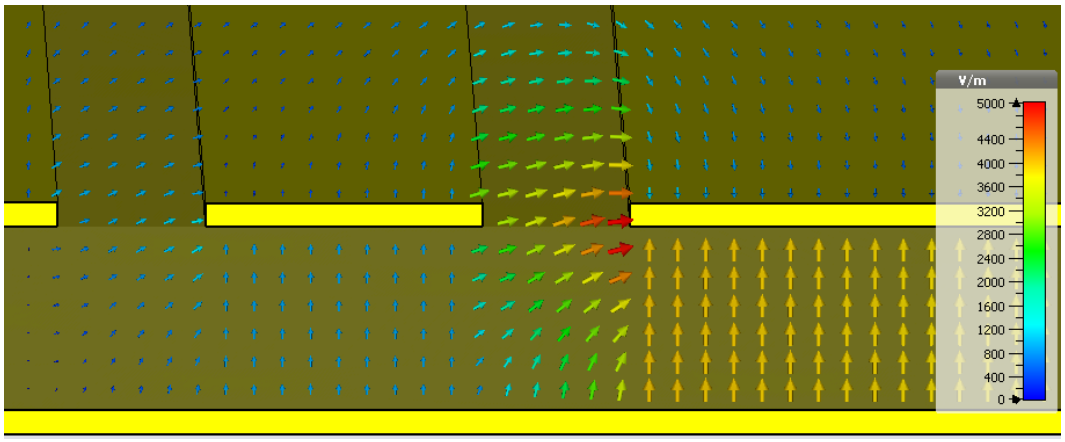

Figure 2.13. Electric field showing parallel-plate mode coupling to CBCPW.

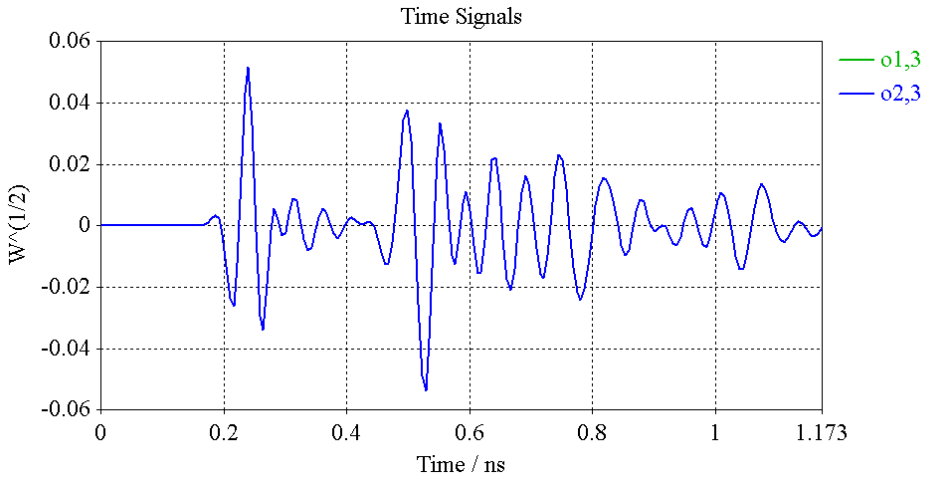

Figure 2.14. Coupled time-domain signals measured at CBCPW ports showing equal magnitude and phase.

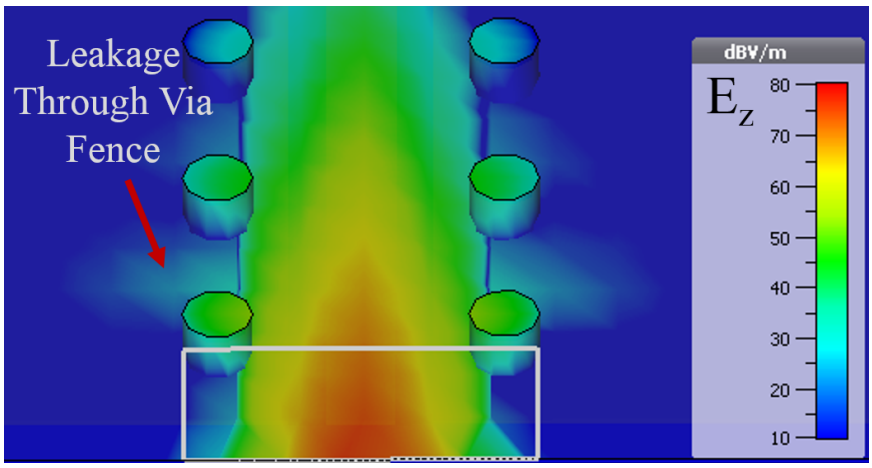

Figure 2.15. E_z around CBCPW showing small field leakage through via fence.

coupling is due to the electric field and is therefore capacitive coupling. A simulation model is created with a discrete port defined between the two reference conductors to excite the parallel plate cavity. The discrete port is located at a point that is along the center of the CBCPW's length so each of the two CBCPW waveguide ports are equidistant from the cavity excitation. The time domain signals at each of the CBCPW ports are the same as seen in Figure 2.14. The same polarity of the signals indicates that capacitive coupling is dominant. In the frequency domain, the coupling has equal phase and magnitude.

A common practice is to use a via fence on each side of the signal conductor to connect the top and bottom reference conductors together. The electric field of the parallel-plate mode is tangential to the surface of the via. If the via is modeled as a PEC, currents are induced on the via to produce a reflected wave to satisfy the boundary condition that tangential electric field must go to zero at the surface of a PEC. As a result, the vias cancel out a portion of the incident electric field that excites the parallel plates thus minimizing the propagation of the parallel-plate mode. This design practice results in the elimination of dips in the insertion loss caused by the parallel-plate resonances provided the via spacing is adequate. However, because the via fence does not form a continuous conductor wall there is still field leakage through the via fence as seen in Figure 2.15 (note the scale is dBV/m).

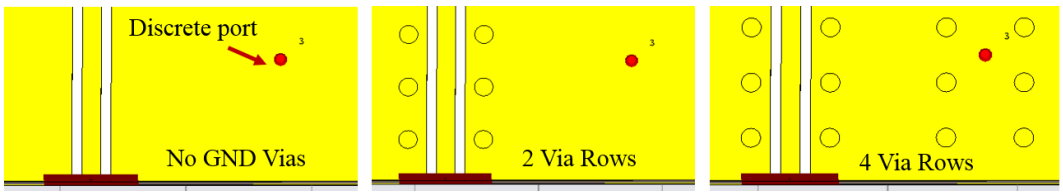

Figure 2.16. Geometry comparison of different amount of GND vias for simulation model.

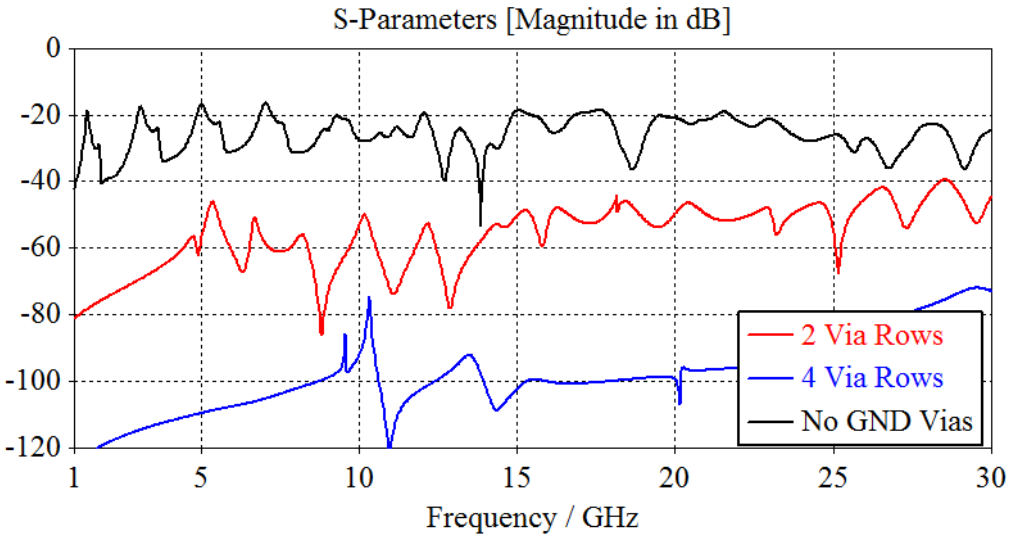

Figure 2.17. Comparison of simulated coupling for different amount of GND vias.

The spacing and size of the vias and their electrical length at the frequency of interest will determine the amount of field leakage. A more recent paper explored the impact different via fences and their spacing had on the insertion loss of CBCPWs [35]. Because the literature is focused on the insertion loss, it is hard to ascertain how much energy is being coupled to the parallel plate cavity, even when employing via stitching, and if this coupling can result in significant crosstalk when the energy is then transferred to other interconnects. A simulation model was created to measure the coupling between the CBCPW and the cavity when differing amounts of GND vias are used. The coupling was simulated for the case with no via stitching, the case with a row of stitching vias on each side of the CBCPW signal trace, and the case with a row of stitching vias surrounding the cavity discrete port in

addition to the the vias around the CBCPW as seen in Figure 2.16. The simulated coupling for the different configurations is shown in Figure 2.17. When no stitching vias are used, the coupling between the CBCPW and the parallel-plate is about -20 dB at resonant frequencies. The addition of the rows of the vias next to the CBCPW reduce the coupling by 50 dB at lower frequencies and by about a 30 dB at higher frequencies. Adding the rows of vias around the discrete port results in about another 40 dB improvement.

Recent research has been conducted to analyze the crosstalk between different types of transmission lines including CBCPW for high-isolation applications [36]. For the majority of the test vehicles studied in this paper, such as CBCPW to microstrip coupling, standard proximity coupling is the dominant coupling mechanism. However, one test vehicle that measured the coupling between a CBCPW and a stripline was not subject to standard proximity coupling because the stripline is enclosed by two reference planes on a separate layer. Via fences were used around the stripline and the CBCPW. Still, the coupling was around -80 dB in the low GHz range and increased to -60 dB at around 20 GHz. The edge-edge via spacing was 30 mils and adequate in terms of transmission as the insertion loss exhibited only smooth loss. This test vehicle shows that even following good standard design practices may not produce very large levels of isolation at high frequencies. A simulation model of the CBCPW to stripline coupling from [36] was created to understand the decrease in isolation at higher frequencies. From previous analysis, it is known that a CBCPW couples to the parallel-plate cavity and the fields of a parallel-plate cavity can couple to a via. This is one of the significant coupling mechanisms for this test vehicle. Simulations were created to illustrate and quantify this coupling mechanism. A field plot of the normal electric field between Layer 1 and Layer 2 at 15 GHz is shown in Figure 2.18. The scale is in dBV/m to show very small field levels. It is important to consider these small field strengths when trying to achieve very high levels of isolation. In between the via fences standing-wave modes can still be excited, although weakly. In the simulation model, additional vias were added around the via transitioning to the stripline which improved the isolation by roughly

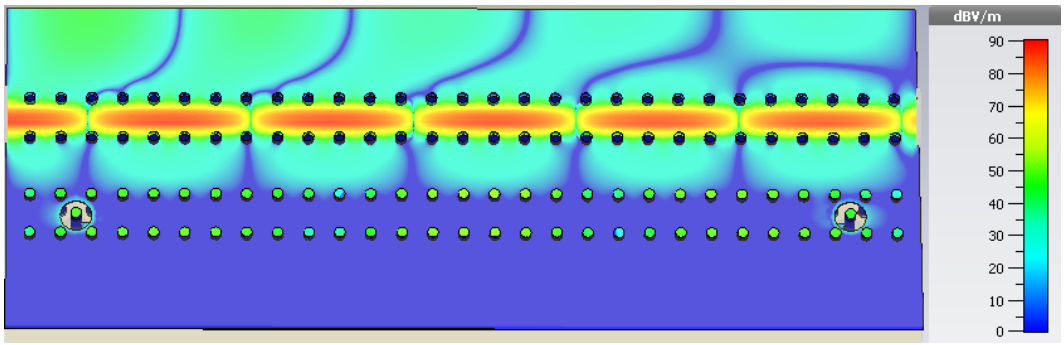

Figure 2.18. E_z between Layers 1 and 2 at 15 GHz of test vehicle.

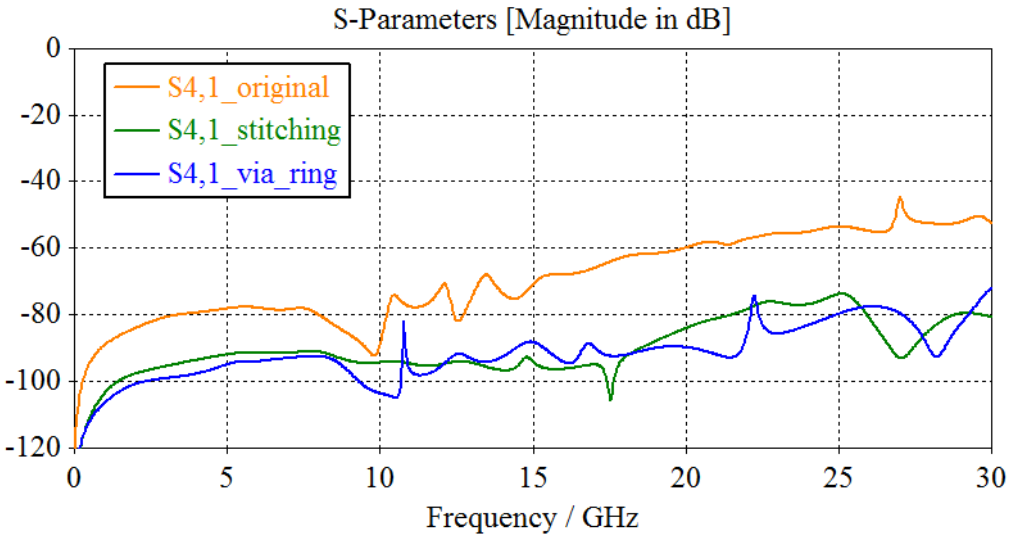

Figure 2.19. Simulated coupling comparison of test vehicle with additional stitching and GND via ring.

20 dB over most of the frequency range as shown in Figure 2.19, indicating that these fields coupling to the via is the primary coupling mechanism. Alternatively, a roughly 20 dB improvement was also achieved in simulation by adding additional stitching vias throughout. Via stitching will be discussed in more detail in Section 5.

2.4. PARALLEL-PLATE CAVITY COUPLING TO STRIPLINE

A via is always required to transition to a stripline. Consequently, a stripline will be subject to coupling from the parallel-plate cavity due to the via. Some papers have focused on the coupling to the via used in the stripline transition such as [37] and [38]. Will this portion dominate the total coupling or can there be significant coupling to the stripline portion of the interconnect? The field distributions of the TEM mode of the stripline and the TM_{z0} mode around a stripline are shown in Figure 2.20. The electric field and magnetic field in the parallel-plate cavity are uniform in the normal direction for typically PCB dielectric thicknesses. The currents induced on each side of the strip from the electric field would be equal and opposite and thus will cancel each other out. Similarly, the currents induced from the magnetic field will also be equal and opposite. As a result, a stripline within a uniform cavity will have negligible coupling to it. In [39], the cavity model is used to obtain the electric and magnetic fields in the cavity and equivalent magnetic current densities are placed on the stripline and via interconnects to obtain the scattered electromagnetic fields induced on them. This analytical approach demonstrated that the scattered fields on a stripline within a cavity were orthogonal to the TEM mode and thus did not lead to noise coupling [39]. This more analytically rigorous approach confirms the conceptual approach above. However, variations in the dielectric material in a cavity, e.g. two different dielectric materials used for consecutive layers, will result in the fields in the normal direction not being completely uniform. Such an asymmetry could result in a small amount of coupling to the stripline. In [40], it was shown mathematically that there is capacitive coupling between

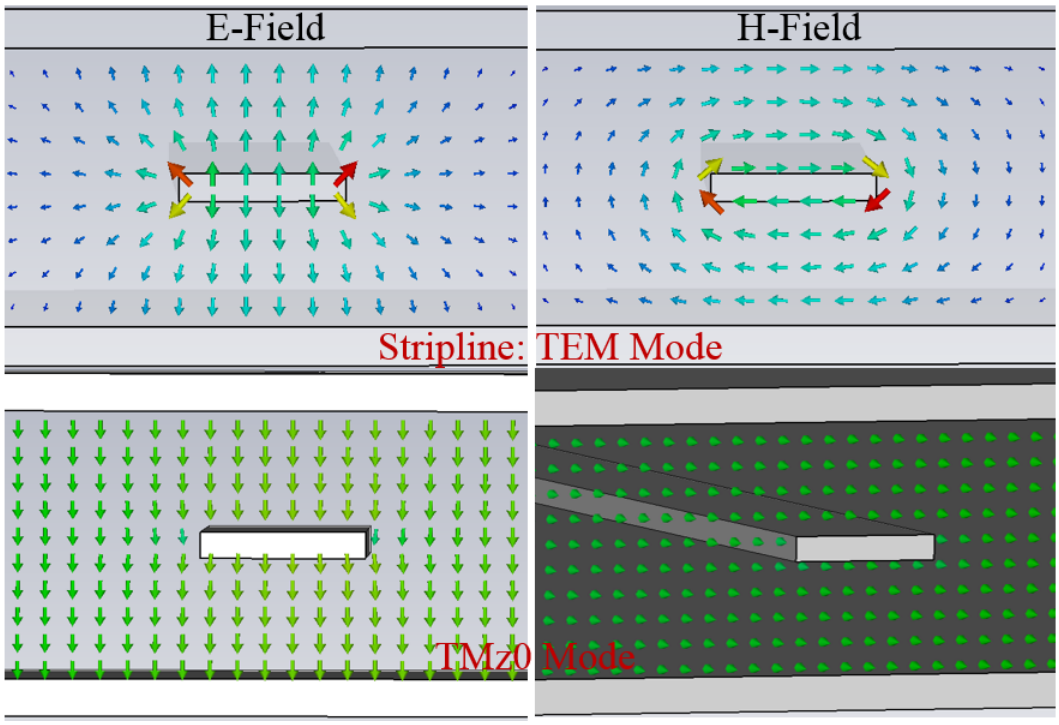

Figure 2.20. TEM mode of stripline and stripline surrounded by TM_{z0} fields in cavity.

the stripline and parallel-plate mode when the dielectric medium is inhomogeneous. Also, in [41] it was reported that an air gap above the stripline would result in leakage of energy to the parallel-plate mode.

The above discussion is relevant for a stripline within a uniform cavity. However, when GND area fills are used throughout a design the situation changes. Now multiple cavities are formed around the stripline. These cavities can have have fields with different magnitudes and phase. As a result of the asymmetry of the fields around the stripline, the induced currents will no longer cancel each other out entirely and there can be significant coupling. Section 3 contains analysis of the coupling mechanisms for victim interconnects, including striplines surrounded by different cavities, in a test board created for the research. Additional analysis will be left for Section 3 of the thesis.

2.5. COUPLING BETWEEN CAVITIES

Additional cavities can be excited from another cavity through a variety of mechanisms. The previous subsections explained how a cavity can be excited by a via or a CBCPW, however there are many other ways to excite a cavity. Still, these two excitations demonstrate fundamentally that both a vertical current source and a vertical electric field are equivalent. This equivalence is stated in the Maxwell-Ampere equation. The only potential for coupling between cavities via a current source is for one cavity to couple to a via and that same via passes through another cavity, resulting in coupling to it. Coupling to another cavity via electromagnetic fields can occur at a discontinuity such as a cutout in the plane or at the edge of the plane. Various researchers have applied electromagnetic theory or microwave theory to develop analytical approaches for calculating the coupling between cavities in PCBs. Much of the research is targeted at coupling from the power distribution network to other cavities formed throughout a design. Coupling can occur at split planes where a small clearance gap is placed between area fills of different DC potentials. Different approaches have been taken to calculate the coupling between these cavities. However, in most of these methods such as [42] , the cavity model is used to calculate the impedance matrix of the cavities and distributed capacitance and inductance elements calculated from the slotline/gap are used to account for the coupling between the two cavities. In [43], the cavity model was used to calculate the impedance matrix for a cavity and electrically small ports are defined to connect the cavities together both through horizontal and vertical connections where continuity of voltage and current are applied. The geometry is divided up into smaller cavities using the segmentation method based on the equivalence principle in order to handle complex geometries [43]. There have also been analytical approaches focused on studying the vertical coupling between cavities, i.e. coupling to a vertically adjacent cavity through a cutout in a shared conductor. In [44], the cavity model was used to obtain the electromagnetic fields within a cavity and a small aperture is replaced with equivalent magnetic and electric currents using Bethe's small aperture coupling theory

which are then used to obtain the fields in the second cavity. In [45], the equivalence principle is used to replace the original fields and aperture with a PEC with discretized equivalent magnetic currents and voltages. The cavity model is then used to calculate the coupling between ports defined in each cavity [45]. These analytical approaches are useful for understanding the coupling, but are not typically practical to implement with full-wave simulation no longer being time prohibitive with current computing power.

One basic geometry relevant for the analysis of coupling between cavities is shown in Figure 2.21. This type of gap occurs when power net area fills or traces are surrounded by a GND area fill or when multiple power area fills are used on a single layer. Time-domain fields will be used for the analysis as they can show cause and effect as opposed to steady-state frequency domain where all transients have decayed. The cavity in the upper left-hand corner is excited with a discrete port, resulting in a propagating wave with a normal electric field and a tangential magnetic field. Figure 2.21 shows the electric field at two instants in time with dBV/m scale. At the gap, the electric field fringes out and a slotline mode is excited. The portion of the fringing electric field and slotline electric fields in the normal direction excites the TM_z modes in the parallel plates. Around the interface, there are higher order modes associated with stored energy, but at some distance from the interface these cutoff modes are decayed and only the fundamental TM_{z0} mode exists. The excited electric fields in the two bottom cavities are of opposite polarity. If only the slot and bottom two cavities are considered, this mechanism is essentially the same as a E-plane tee junction or the E-arm of a magic tee junction as shown in Figure 2.22 [46]. The coupling can also potentially be viewed as a parallel-plate to slotline mode conversion and then slotline to parallel-plate mode conversion for the other cavities.

If there is a larger gap in one of the planes the field distributions will be different. Figure 2.23 shows the electric field for a larger gap at two instances of time. In this case, the upper left-hand cavity is first excited. The fringing fields at the interface excite the bottom cavity and the taller cavity. In the same way as the previous geometry, at the interface

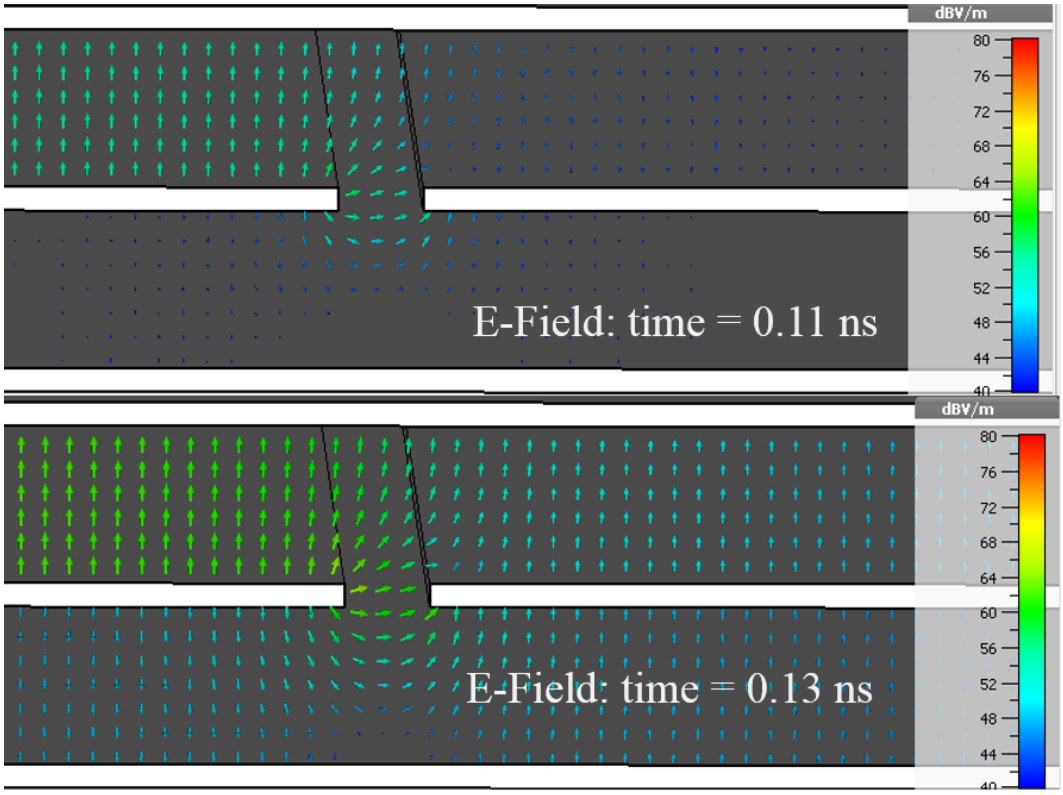

Figure 2.21. Time-domain $\vec{E}$ of gapped plane showing excitation of bordering cavities.

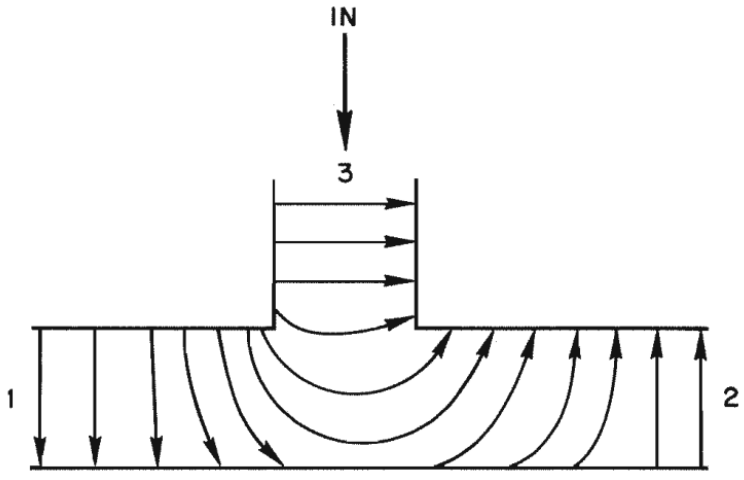

Figure 2.22. Electric field lines for a waveguide E-plane tee.

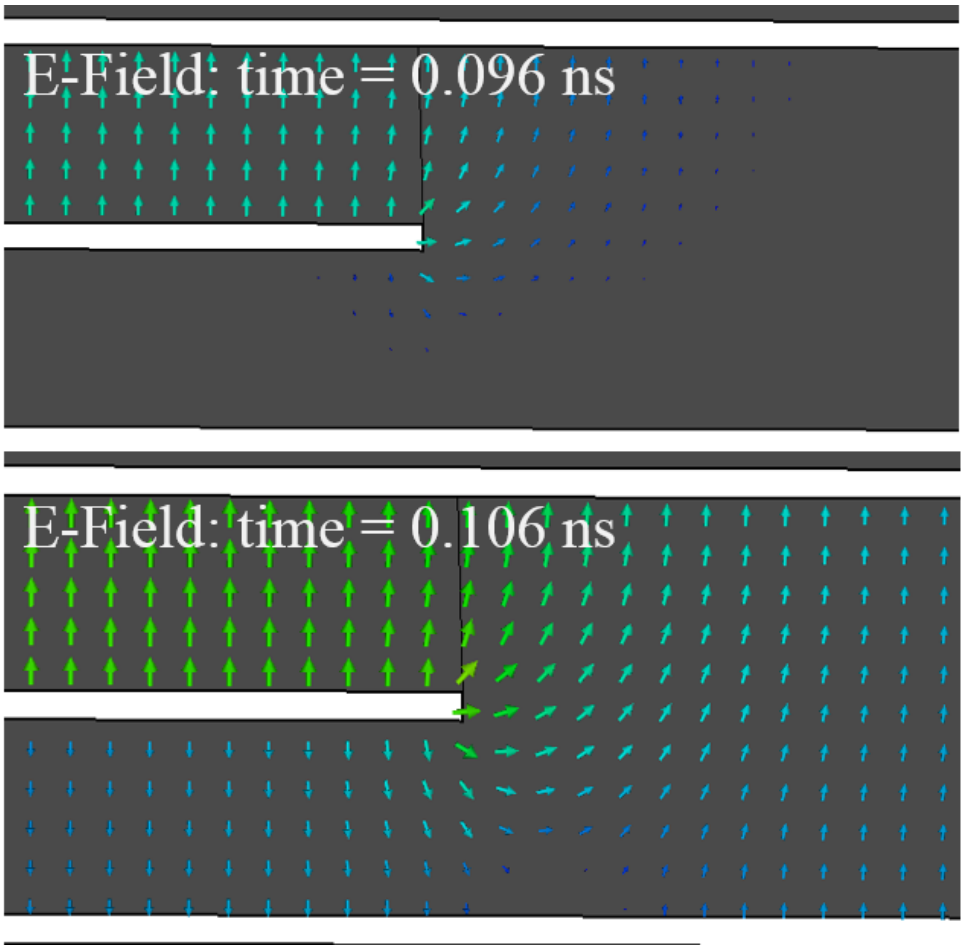

Figure 2.23. Time-domain $\vec{E}$ at plane edge showing excitation of bordering cavities.

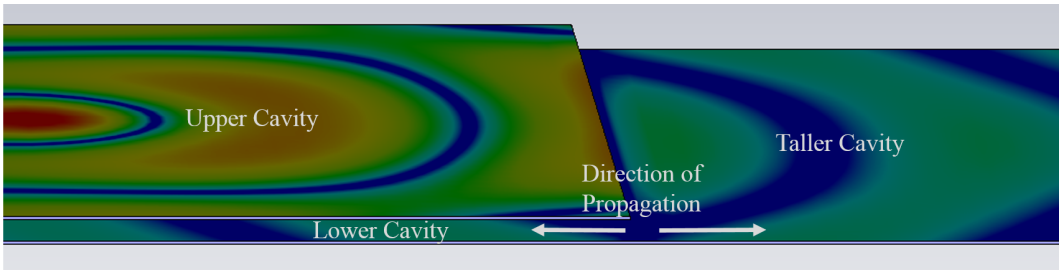

Figure 2.24. Propagation of TM_{z0} waves in two cavities that are excited at the edge of a bordering cavity.

higher order modes exist, but at a certain distance from the interface only the fundamental TM_{z0} mode exists. Essentially, some of the fields in the first cavity will be transmitted into the taller cavity formed by the top and bottom planes and into the lower cavity. Some of the incident fields will also be reflected back at the interface. Absorbing boundary conditions can also be used to eliminate reflections off the open PCB sidewalls. This allows the field behavior to be analyzed in the absence of scattering from the sidewalls. Figure 2.24 shows the normal electric field in the cavity at 20 GHz with absorbing boundary conditions. The fields from the upper cavity result in transmitted propagating waves in the lower cavity and the tall cavity. The brief analysis in this subsection illustrates that is very easy for parallel-plate noise excited in one cavity to spread throughout the rest of the PCB.

3. TEST VEHICLE COUPLING ANALYSIS

3.1. OVERVIEW OF TEST VEHICLES

A set of test boards, shown in Figure 3.1, were designed to study the coupling between the power distribution network and the various interconnects. Each test board is 2" x 2" with a 6-layer 0.062" FR-4 stack-up that is shown in Figure 3.3. One variation of the test board was built with Rogers RO4350B and Rogers 4450F material with a 8 mil thickness for the prepreg layers compared to the 9 mil of the FR-4 stack-up. A power net area fill is located on Layer 3. There are reference planes above and below the power net area fill resulting in the formation of a cavity between the power net and the reference layer. After routing, GND area fills were placed on all layers aside from Layer 1 resulting in the formation of additional cavities throughout the design. There are incremental changes between the five test board configurations that allow for determination of how various changes impact the coupling. The test boards were designed for both passive and active measurements. The PWR/GND cavity can be excited by a compression mount connector via that connects to the power net area fill. In addition, a Qorvo TGA2597-SM, a 2-6 GHz GaN driver amplifier in a QFN package, can be installed on the board to excite the cavity. The power net area fill provides the drain voltage for the amplifier while a trace on Layer 1 supplies the gate voltage. Active measurements and the integration of components are discussed in Section 5.

Various victim interconnects are included in the test board design as shown in Figure 3.2. Compression mount connectors are used to interface with the victim interconnects for ease of measurement and repeatability. There are three victim striplines and three victim vias. The victim striplines include a stripline routed next to the edge of the power net area fill on the same layer, a stripline that is partially routed above the power net area fill (referenced

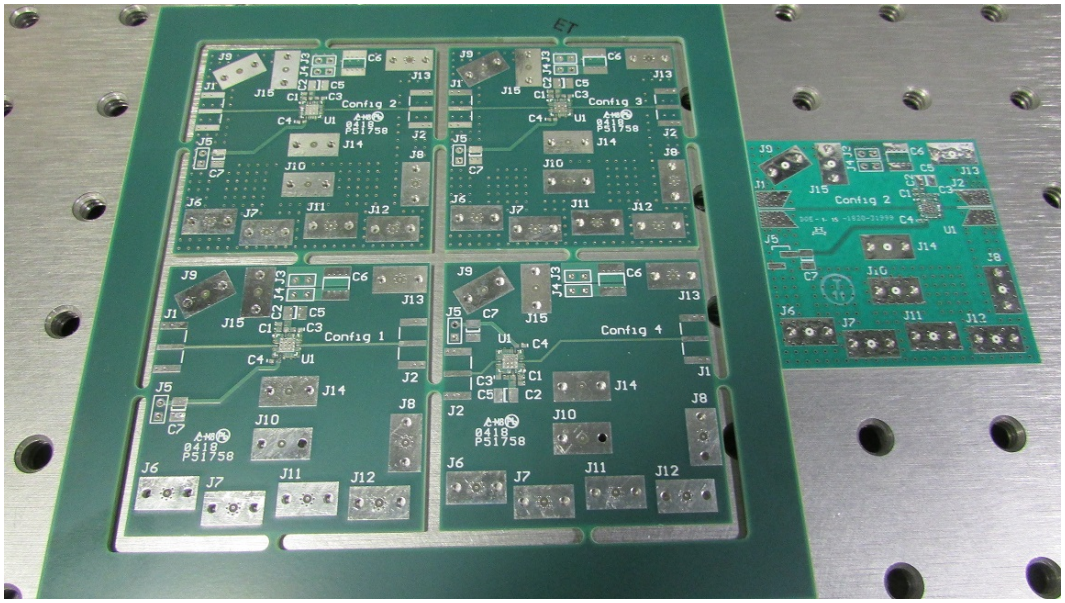

Figure 3.1. Picture of the five different configurations of the test vehicle.

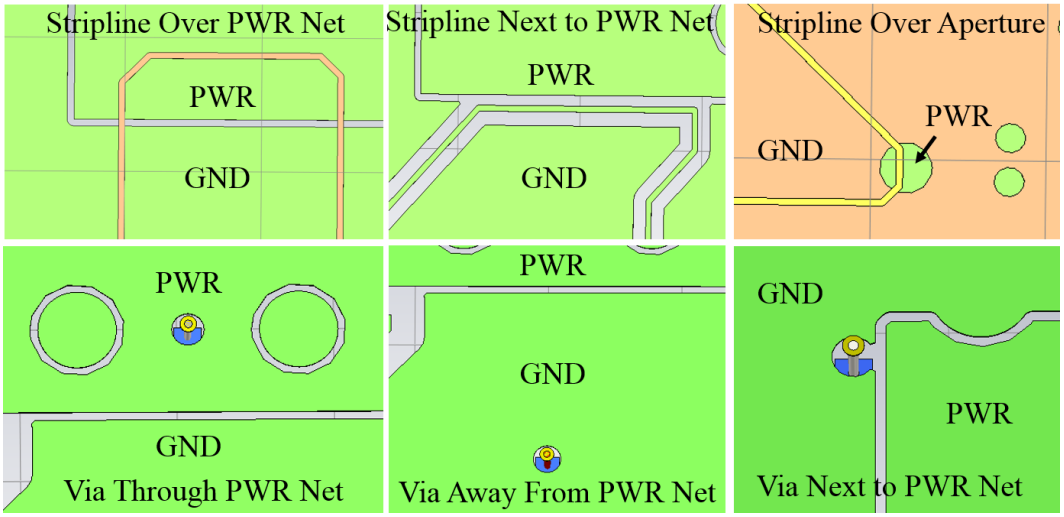

Figure 3.2. An overview of the victim interconnects included in the test vehicles.

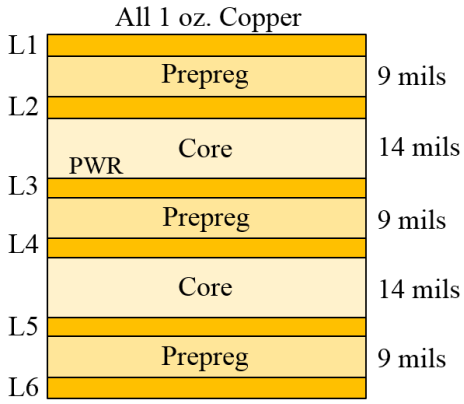

Figure 3.3. Stack-up of 6 Layer FR-4 for configurations 1-4.

to the power net), and a stripline that is routed on Layer 5 above a small aperture in Layer 4 (opening of the cavity). The signal vias that connect to the stripline have a ring of GND vias around them to reduce fields from the various cavities coupling to the via in order to ensure the coupling to the stripline portion of the interconnect is the dominant mechanism. The victim vias include a via that passes through the power net area fill, a via that is located next to the edge of the power net area fill, and a via that is located away from the power net area fill. The coupling mechanism between each victim interconnect and the power net cavity is analyzed in the following subsections. Configuration 1 has intermittent vias connecting the various GND planes together. The Configuration 2 test board adds stitching vias with 75 mil center to center spacing between the GND planes. Although, only through hole vias are used in the design so it not possible to stitch the region of the PCB where the power net area fill is located. Configuration 3 also includes the via stitching along with the removal of the Layer 5 aperture, increased separation between the stripline next to the power net area fill, and additional GND vias added next to victim vias. Configuration 4 is the same as Configuration 1 except for the PA IC is moved from the middle of power net cavity to the corner of the power net cavity. The Rogers material test board is a modified version of Configuration 2 that includes additional stitching vias and the IC is located near the edge of the power net cavity. Network analyzer measurements were performed to measure the

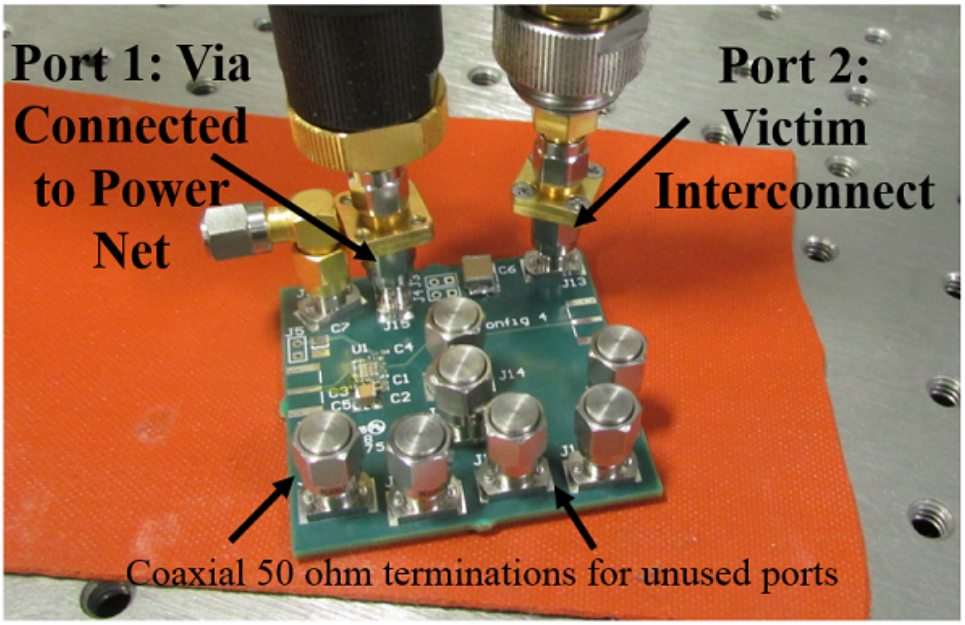

Figure 3.4. Set-up for passive coupling network analyzer measurement.

coupling between the power net and the various victim interconnects. The measurement set-up is shown in Figure 3.4. Port 1 was connected to the compression mount connector that connects with a via attached to the power net area fill and Port 2 was connected to the compression mount connector for one of the victim interconnects. The IC and passive components were not installed for this measurement. All other ports were terminated with a 50 ohm coaxial termination. A frequency range of 10 MHz to 10 GHz was used. The measurement settings were selected to maximize dynamic range so very small amounts of coupling could be measured. For instance, the port output power was set to 10 dBm and the IFBW set to 100 Hz. If the coupling for a certain measurement was not very low, the IFBW was increased for a shorter sweep time. For a few of the measurements with very low coupling, sweep averaging was also used. A Maury Microwave 8050CK 3.5 mm SOLT calibration kit was used for the calibration.

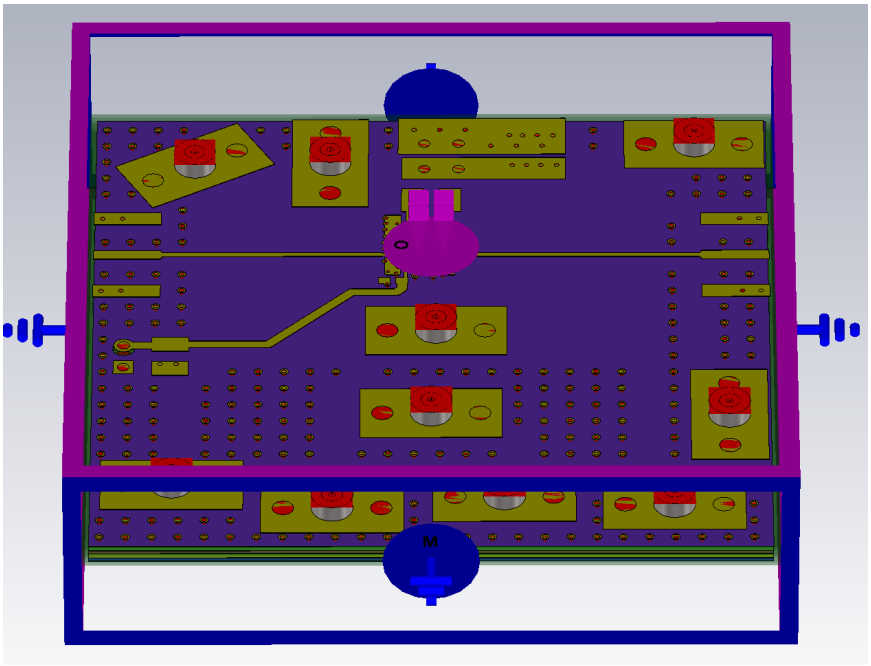

Figure 3.5. Microwave CST simulation model of Configuration 2 test vehicle.

3.2. FULL-WAVE EM SIMULATION MODEL

With the computing power today, it is more feasible to perform EM simulation on entire PCBs. In the past, only certain sections of a PCB may have been simulated which may not capture some coupling paths such as coupling through a parallel-plate cavity. Ideally simulation can be used to identify and correct issues before fabrication. Full-wave EM simulation tools allow for the user to define field monitors at different frequencies or in the time-domain that allow visualization of the fields. Being able to visualize the fields facilitates analysis and understanding of the underlying physics. Also, changes can be made to the simulation model to verify proposed fixes or to help identify the main coupling path. However, it is important to have measurements to validate the simulation models. There are many things that can be set up incorrectly in a simulation that will lead to incorrect results. Still, when simulating certain geometries the user will gain understanding of the common pitfalls that can occur for that type of geometry. Microwave CST's time-domain solver is

used for the PCB EM simulations. Figure 3.5 shows an image of the simulation model. ODB++ files are imported into CST through their EDA import tool. Coaxial connectors are added to the simulation model and coaxial waveguide ports are defined. With moderate mesh density, the simulation model has about 1.5 million mesh cells. A 100 mils of vacuum background material is added in the x and y-directions and 250 mils in the z-direction. Open (PML) boundary conditions are used in the positive and negative z-direction and PMC boundary conditions are used in the positive and negative x and y-directions. Overall, the simulation results had good agreement with the measured results, validating the models. The simulation result will be included in some of the plots in the following subsections, but extensive comparison of the measurements and simulation results is not included for brevity. Field plots from and modifications of the simulation model will be used throughout this section to demonstrate the coupling mechanisms. The simulation time for exciting the via connected to the power net area fill is about 20 minutes for -50 dB accuracy running on a 2x Intel Xeon 128 GB RAM workstation with GPU (GP100) acceleration enabled. Because the PWR/GND cavity is a resonant structure the energy decay is slow, leading to longer simulation times then a simulation model with comparable number of mesh cells and smallest time step.

3.3. EXCITATION AND FIELDS OF POWER NET CAVITY

It is worthwhile to first discuss how the cavity is initially excited by a via. As discussed in the prior sections, a cavity supports a propagating TM_{z0} wave with a tangential magnetic field and a normal electric field with respect to the surface of the conductors. Higher-order TM_z modes are possible, but they will be evanescent modes at the frequencies of interest in standard PCB geometries. For the portion of the geometry where the via is passing through the anti-pad in the conductor, the fields are coaxial TEM mode. The magnetic field is tangential to the via and the electric field is radial. For the portion of the geometry where the via passes through the parallel plates the field distribution changes.

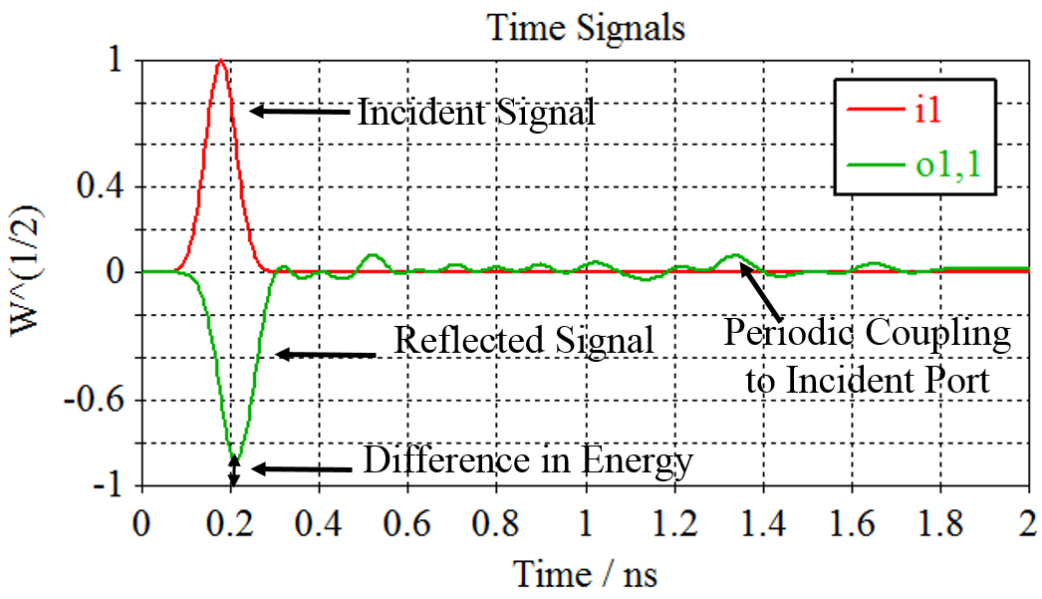

Figure 3.6. Simulated time signals of port exciting the PWR/GND cavity.

The magnetic field remains tangential, however the electric field now contains components in the normal direction in addition to the radial direction. The fields in the cavity consist in the superposition of TM_z modes including the TM_{z0} which is propagating. The excitation will first be discussed in the time-domain where the cause and effect are evident as opposed to the steady-state conditions of the frequency domain. At the connection between the via and the power net area fill the fields encounter essentially a PEC boundary condition. This results in a scattered wave to enforce the condition that the tangential electric field at the surface must goes to zero. The direction of the magnetic field of the scattered wave is the same as the incident wave so the magnitude of the magnetic field increases. The scattered wave is converted back to a coaxial TEM field distribution where it is measured at the port. As can be seen from the time signals in Figure 3.6, most of the energy of the original signal is reflected back to the port. The difference in energy consists of energy remaining in the structure and energy dissipated due to loss. The fields in the cavity show a propagating wave in the radial direction away from the excitation via as shown in Figure 3.7. The radial wave encounters discontinuities such as the open edge of the cavity which result in scattering.

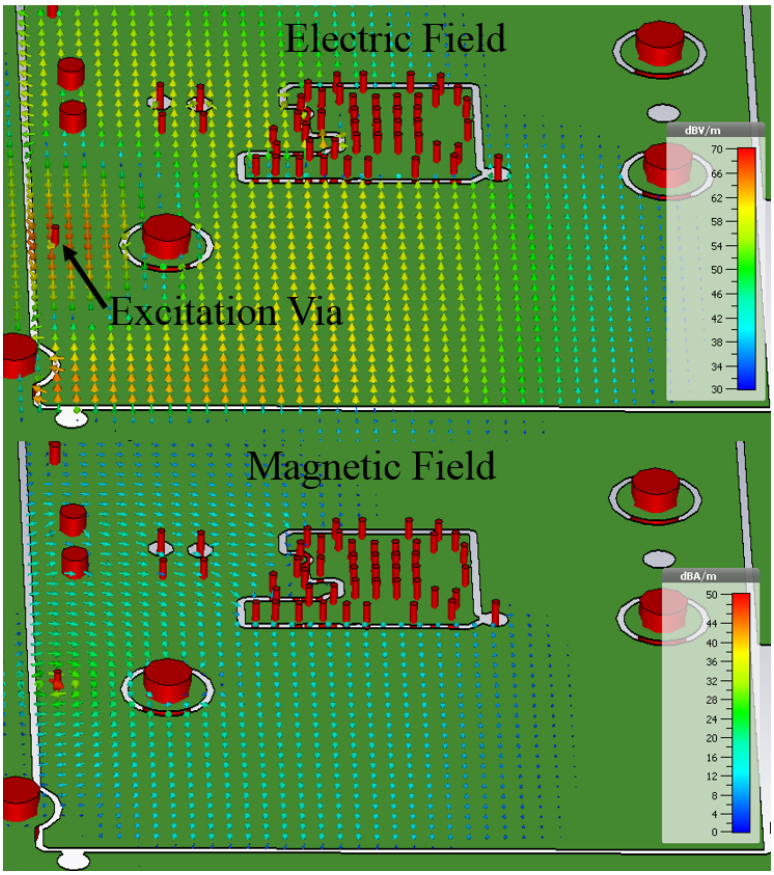

Figure 3.7. Fields in the PWR/GND cavity excited by via.

The waves will bounce back and forth off the open boundary conditions at the edge of the planes resulting in ringing in the time domain waveforms as the waves periodically couple to the via of the excitation port. The periodicity of the ringing in the time-domain corresponds to certain resonant frequencies. In the frequency domain, the incident and reflected waves can combine constructively and destructively resulting in the formation of standing-wave patterns. The standing-wave patterns are dependent on the boundary conditions, material properties, physical dimensions, and where the excitation occurs. For instance, the dielectric constant of a material will determine the speed that waves propagate through the medium. The speed and physical dimensions will determine the electrical length of a structure, i.e., how many wavelengths long a structure is. Using transmission line analysis, a resonant

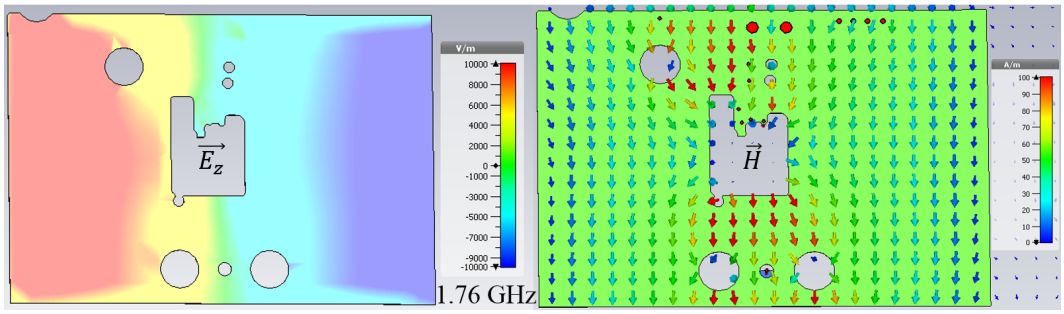

Figure 3.8. E_z and $\vec{H}$ in PWR/GND cavity at 1.76 GHz.

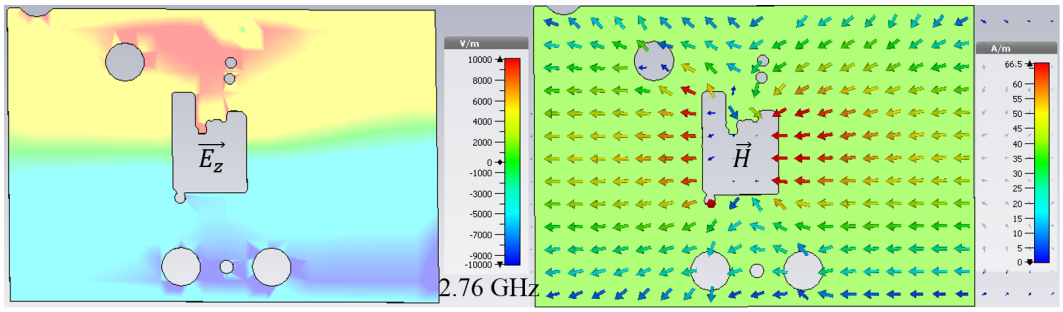

Figure 3.9. E_z and $\vec{H}$ in PWR/GND cavity at 2.76 GHz.

frequency will occur at an electrical length of $\lambda/2$ for an open-circuited transmission line. At resonant frequencies, the fields add constructively which results in high field strengths and thus greater coupling. The first seven resonant modes excited by the via in the upper left-hand corner of the power net cavity are shown in Figures 3.8-3.14. The electric field in the z-direction is on the left and the magnetic field is on the right. The electric fields are captured at a phase of 0 degrees and the magnetic fields at a phase of 90 degrees. More resonant modes may exist, but are not strongly excited from the excitation location. For the first two modes, TM_{10} and TM_{01}, the electric field has a maxima where the magnetic field has a minima and vice versa. These modal patterns will be referenced in the following subsections when analyzing the coupling to the victim interconnects.

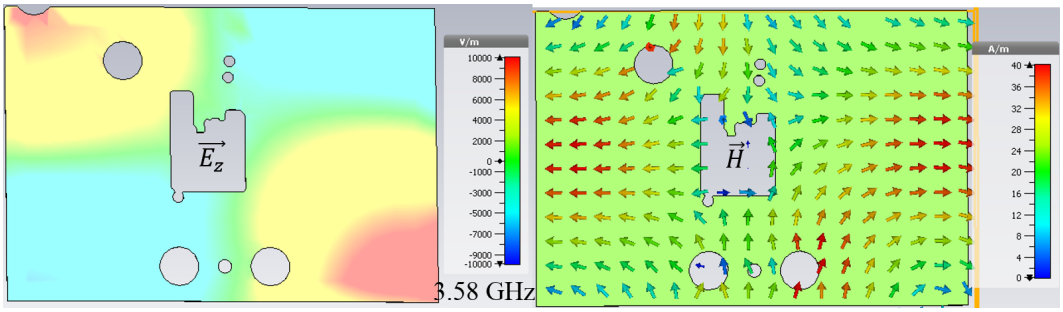

Figure 3.10. E_z and $\vec{H}$ in PWR/GND cavity at 3.58 GHz.

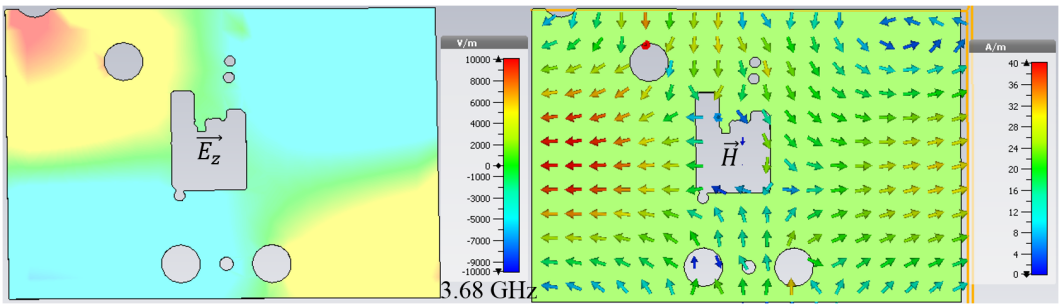

Figure 3.11. E_z and $\vec{H}$ in PWR/GND cavity at 3.68 GHz.

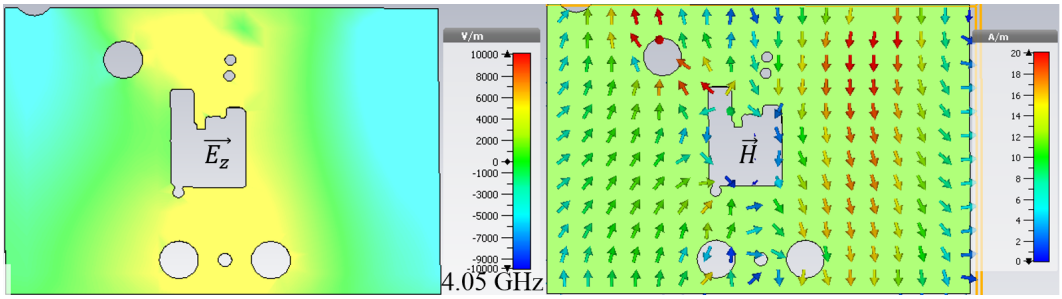

Figure 3.12. E_z and $\vec{H}$ in PWR/GND cavity at 4.05 GHz.

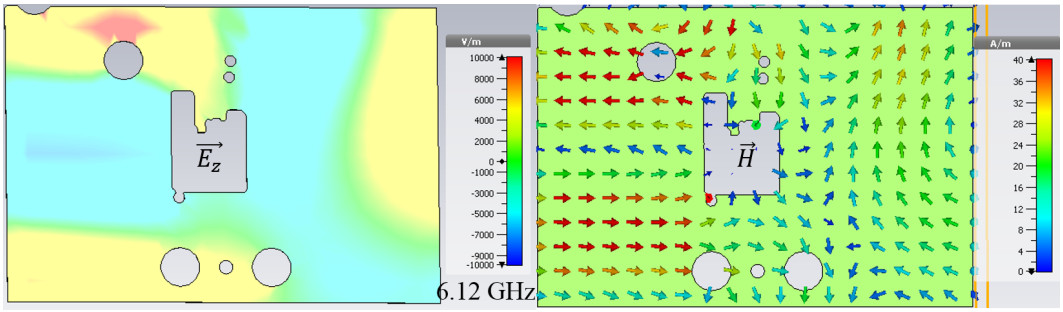

Figure 3.13. E_z and $\vec{H}$ in PWR/GND cavity at 6.12 GHz.

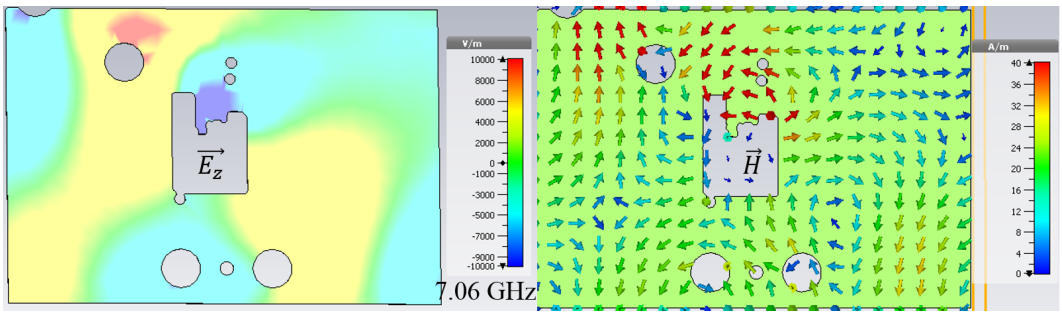

Figure 3.14. E_z and $\vec{H}$ in PWR/GND cavity at 7.06 GHz.

3.4. EXCITATION OF ADDITIONAL CAVITIES THROUGHOUT THE PCB

The electromagnetic waves in the PWR/GND cavity can couple to other cavities and excite them. Some basic analysis of the coupling between cavities was discussed in Section 2. These other cavities can then serve as the coupling path between the PWR/GND cavity and the various victim interconnects. In these test boards, the additional cavities are formed between GND conductors, but other designs may contain multiple PWR/GND cavities. These GND cavities are electrically connected together with vias, but it is not straightforward to know if these intermittent connections will be adequate to minimize the propagation of undesired electromagnetic waves. Because these other cavities may constitute an important component in the coupling path, they will be analyzed prior to the individual victim interconnects. There are four other cavities formed in the six layer PCB stack-up. A cavity between the Layers 5 and 6 GND conductors, a cavity between the Layers 4 and 5 GND conductors, a cavity between the Layers 2 and 3 GND conductors (there is a GND area fill around the power net area fill on Layer 3), and a cavity between the Layers 3 and 4 GND conductors. In addition to the frequency-domain fields, transient time-domain fields can be useful to analyze as they show cause and effect that is not readily apparent in the steady-state frequency domain. Analysis of time-domain fields are used to help determine the primary excitation mechanisms of each cavities. First, the excitation of the cavities that are horizontally adjacent to the PWR/GND cavities will be discussed. A slotline mode is

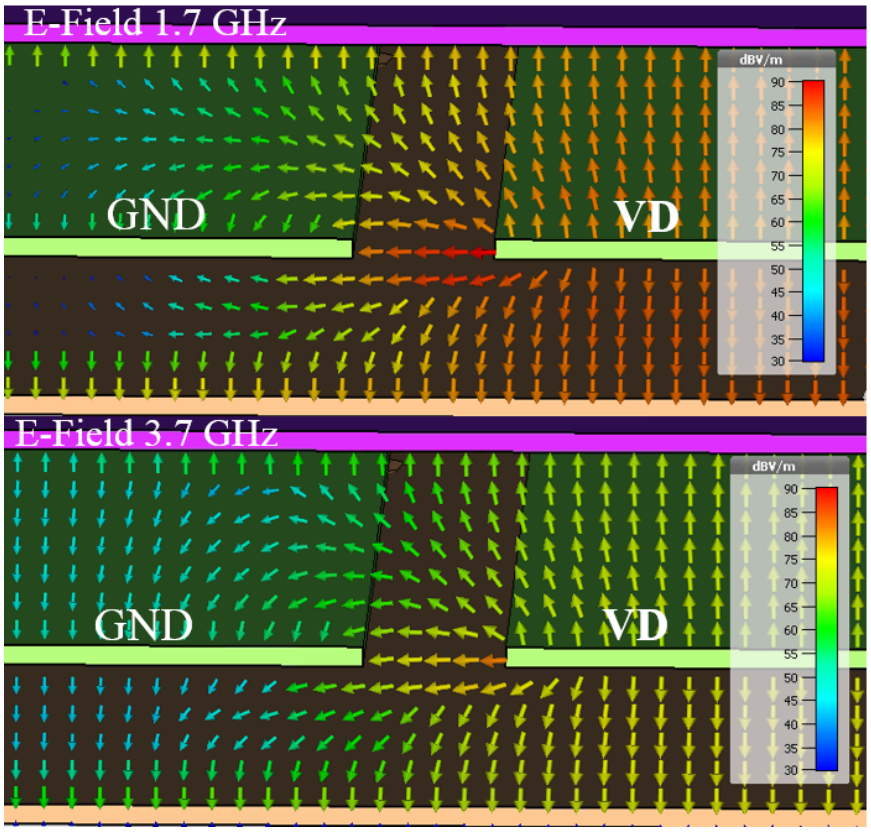

Figure 3.15. $\vec{E}$ at gap between PWR and GND area fills.

created between the edge of the power net area fill and the edge of the outer GND area fill. Figure 3.15 shows the fields between the VD (PWR) and GND conductors at 1.7 GHz and 3.7 GHz. The electric field that starts on the power conductor and terminates on the GND conductor creates a potential difference between the two GND conductors which can excite the cavity. This excitation mechanism was discussed in greater detail in Section 2.5. This excitation may be minimized with vias connecting the two GND conductors. Currents will be induced on GND vias to generate an electric field with opposite polarity as the incident field. If the GND via is too far away from the excitation, i.e. the distance is electrically large, then the field cancellation from the induced currents on the via is no longer effective (the phase of the incident and scattered waves is no longer approximately equal and opposite). The vias can also be viewed as imposing new boundary conditions.

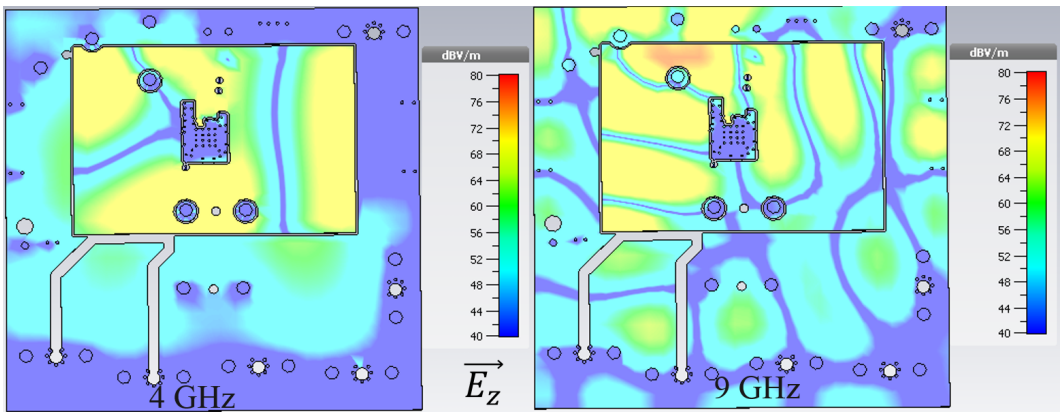

Figure 3.16. Electric field distributions in Layer 2-3 GND cavity at 4 GHz and 9 GHz.

At 1.7 GHz, there is not a normal electric field throughout the cavity, i.e. the cavity is not excited. At 3.7 GHz, there is a normal electric field throughout the cavity indicating that the cavity is excited. At these frequencies, the GND vias are no longer effective at preventing the cavity excitation. The field distributions that occur in these cavities formed by GND conductors will be dependent on the electrical length, boundary conditions (GND vias throughout), excitations, etc. The electric field distributions for the Layer 2-3 GND cavity are shown at two frequencies in Figure 3.16 in dB scale. At lower frequencies, the areas of the cavity that do not have stitching vias are excited. At higher frequencies, there is much greater variation in the standing-wave patterns. Areas within the cavity are becoming electrically longer. For instance, in the 9 GHz E-field distribution there are electric field maxima that occur between stitching vias. These areas between multiple GND vias can be crudely approximated as a cavity resonator with PEC walls. There is an electric field minima at the shorting via and the electric field maxima will occur $\lambda/4$ away from this minima.

The Layer 4-5 cavity is primarily excited by the clearance gap in Layer 4 that exists because of the routing of the stripline on Layer 4. Figure 3.17 shows a cross-section of the time-domain electric fields at the gap. The electric field of the PWR/GND cavity (red

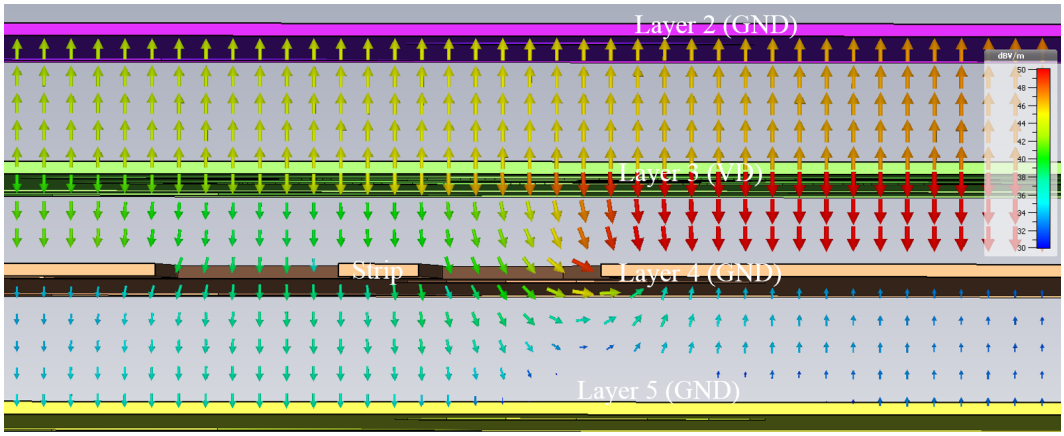

Figure 3.17. $\vec{E}$ at gap in Layer 4 showing the excitation of the Layer 4-5 cavity.

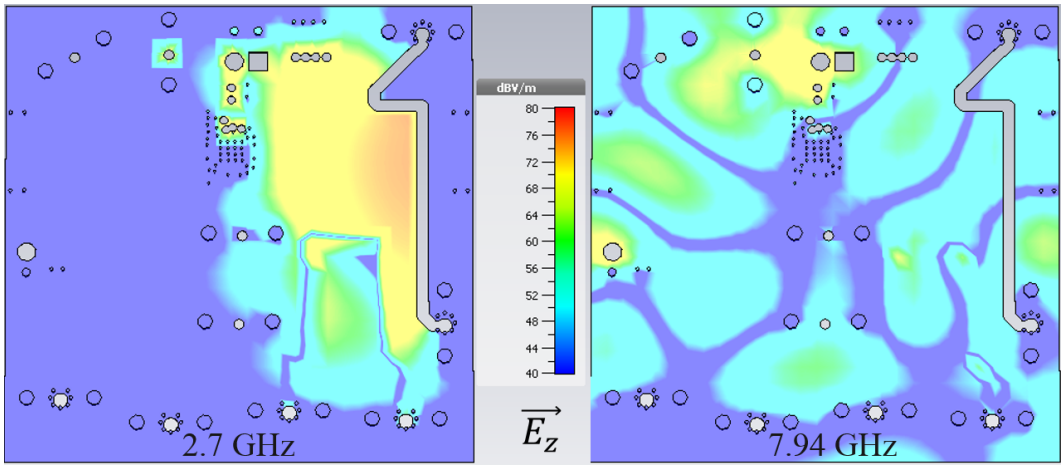

Figure 3.18. Electric field distributions in Layer 2-3 GND cavity at 2.7 GHz and 7.94 GHz.

arrows) encounter a discontinuity at the gap. The electric fields at the edge fringe out and excite the cavity formed in the gap between Layers 3 and 5 and the Layer 4-5 cavity on the bottom right. The fields in the Layer 3-5 cavity can then excite the Layer 4-5 cavity on the bottom right. The Layer 3-4 GND cavity on the other side of the gap is also excited at the power net area fill clearance gap and can subsequently excite the Layer 4-5 GND cavity. Figure 3.18 shows the Layer 4-5 cavity electric field in the z-direction at two different frequencies. At 2.7 GHz, the fields in the Layer 4-5 cavity are constrained to the area around

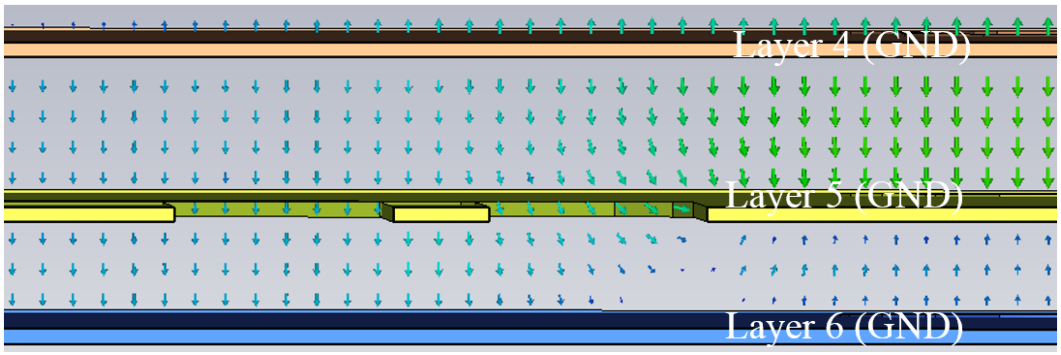

Figure 3.19. $\vec{E}$ at gap in Layer 5 showing the excitation of the Layer 5-6 cavity.

the clearance gap in Layer 4-5 in the large area where there are no vias connecting the GND conductors. At 7.94 GHz, the electric field is spread throughout the entire Layer 4-5 cavity.

The Layer 5-6 cavity is primarily excited from the gap in Layer 5 that exists because of the routing of the stripline on Layer 5. The Layer 5-6 cavity is excited by the Layer 4-5 cavity rather than directly from the PWR/GND cavity. As a result, reducing the excitation of the Layer 4-5 cavity should reduce the excitation of the Layer 5-6 cavity. Figure 3.19 shows a cross-section of the time-domain electric fields at the gap. This excitation mechanism is the same as the excitation of the Layer 4-5 cavity through the stripline clearance gap. There is a small aperture in Layer 4 that overlaps with the gap in Layer 5. However, this gap is electrically small over the frequency range of analysis compared to the electrically large clearance cut-outs, so its contribution to the excitation will be much less than the stripline clearance gap in Layer 5.

The coupling to the different cavities can be quantified in simulation by placing a vertical discrete port between the two GND conductors. The coupling to one single location within the cavity will obviously not capture all functionality, but can demonstrate overall trends. The x and y coordinates of the discrete port were kept the same for each cavity and the location of the vertical discrete ports is shown in Figure 3.20. By comparing

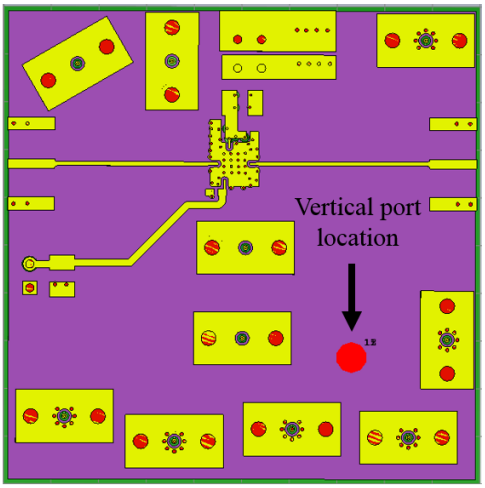

Figure 3.20. Location of vertical discrete port for cavity coupling simulation.

the simulated coupling to each cavity for different versions of the simulation model, the proposed primary excitation mechanisms can be validated. First, the stripline on Layer 4 is deleted and the cutout in Layer 4 is filled with copper. This change should eliminate the primary excitation mechanism of the Layer 4-5 cavity and thus reduce the excitation of the Layer 5-6 cavity. The simulated coupling is shown in Figure 3.21 with the modified simulation model results plotted with dashed lines. It is clear from the results that the clearance gaps in the planes are the dominant coupling mechanism in the first half of the frequency range. The coupling to the two cavities is greatly reduced before 5 GHz. However, in the second half of the frequency range the coupling is on the same order as the original model. Now further changes to the simulation model can be made to determine other significant excitation mechanisms. The PCBs created for this research are all through-hole designs. As a result, the vias that connect to the power net area fill on Layer 3 continue across the entire stack-up, penetrating through the other GND cavities. These vias may serve as another possible excitation mechanism for the other cavities. To evaluate the via's effect, the vias were changed to blind vias that only spanned from Layer 1 to Layer 3 in the simulation model. Figure 3.22 shows the simulated coupling comparison with the via stubs

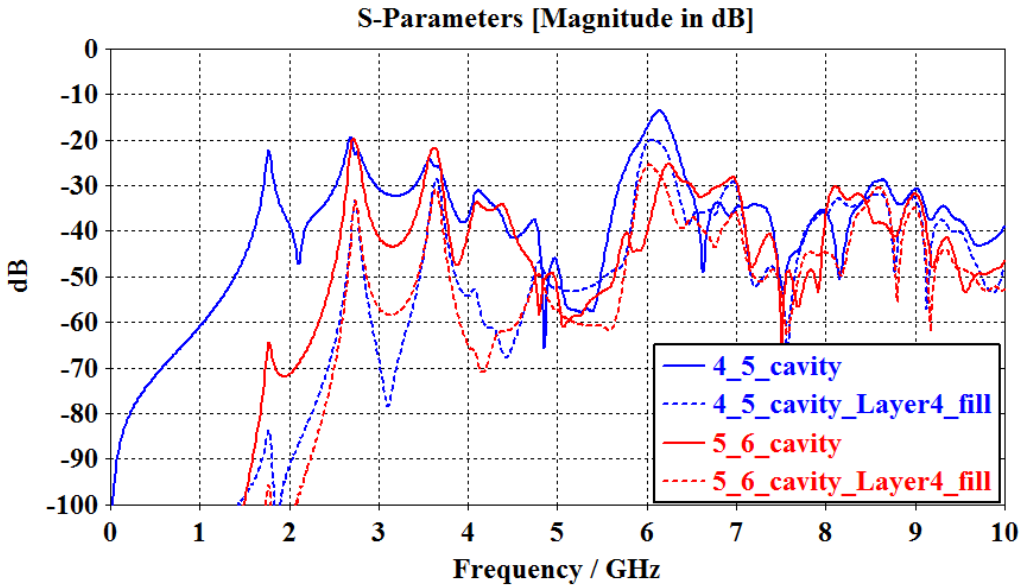

Figure 3.21. Simulated cavity coupling comparison with Layer 4 cutout removed.

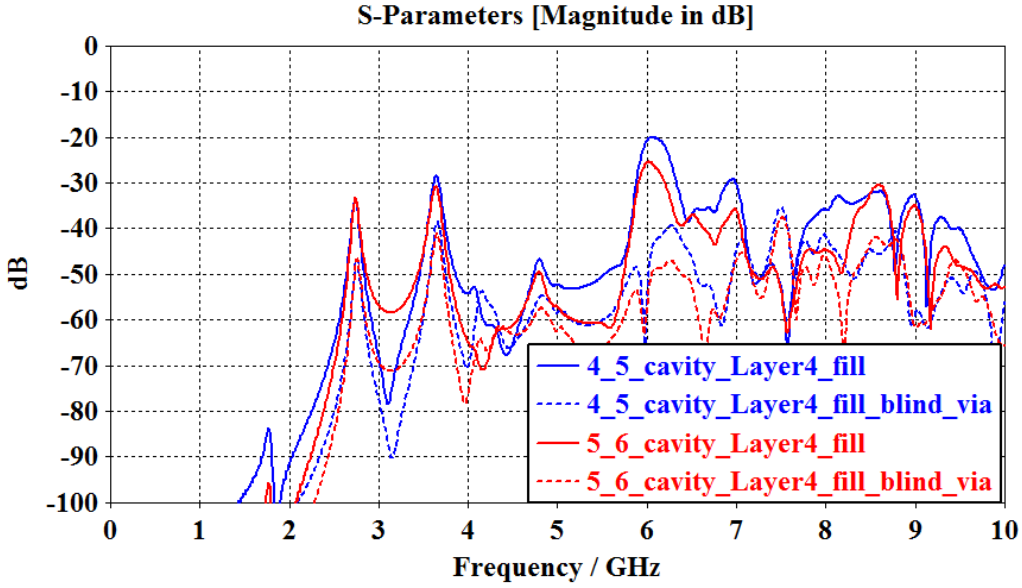

Figure 3.22. Simulated cavity coupling comparison with PWR via stubs removed.

removed. The solid lines are the coupling for the Layer 4 modification model while the dashed lines are the coupling for the additional modification of the removal of PWR net via stubs. Based on the simulation results, the via stubs do contribute to the excitations of other cavities. Although the excitations through gaps can be more significant, especially at lower frequencies. These findings suggest that use of blind/buried vias or backdrilling can limit the spread of PWR noise throughout the design if other significant excitation mechanisms are controlled. After these two modifications, the coupling maximas are around -40 dB compared to -20 dB for the original mode. There are still other excitation mechanisms that exist. Some other potential mechanisms are excitation from signal/PWR vias that are coupled to in other cavities and fringing fields around the periphery of the PCB.

3.5. COUPLING TO VIA IN THE POWER CAVITY

Figure 3.23 plots the coupling ($|S_{21}|$) to the via in the power cavity for the different configurations. The simulation result is plotted with a dashed line and shows good agreement with the measurement. With reference to Figures 3.8-3.9, the via is in an electric field minima for the first mode at 1.7 GHz and is in an electric field maxima for the second mode at 2.7 GHz. At 1.7 GHz the via is in a magnetic field maxima as seen in Figure 3.8. The coupling contains a maxima at 2.7 GHz and a small dip at 1.7 GHz. The modes at 3.58 GHz and 3.68 GHz, which are shown in Figures 3.10-3.11 are slightly different. At 3.58 GHz there is another dip in the coupling that corresponds to via being located close to a minima of the electric field pattern. While at 3.68 GHz there is a local maxima in the coupling as the electric field pattern is slightly different and the via is no longer located in a null. For these two modes the magnetic field around the via is about the same. These observations indicate that a large electric field in the vicinity of the via will result in coupling to the via while a large magnetic field does not. Analysis of the fields will illustrate why this is the case. For many of the modal patterns, in the area around the via the magnetic field will be approximately uniform. This is true, if the via is small compared to the variation of

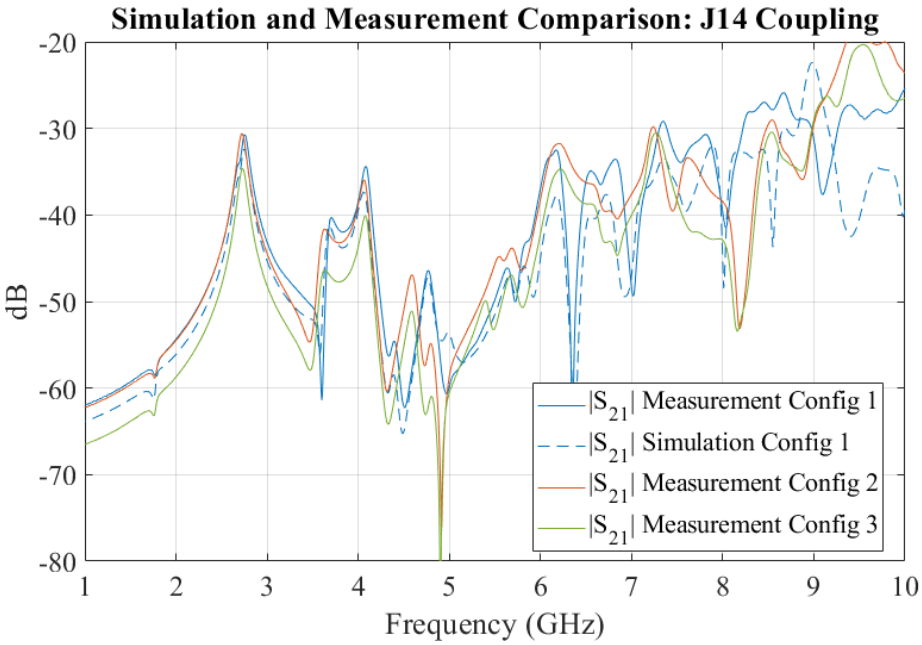

Figure 3.23. Measured and simulated coupling to the via in the power cavity.

the modal patterns. The magnetic field will be tangential to the surface of the via at some location and normal to the surface at others. The outward normal for the via is pointing radially outwards. Applying $J_s = \hat{n}x\vec{H}$ to the two sides of the via where the magnetic field is tangential to the surface will result in surface currents with opposite polarity: one is in positive z-direction and the other in negative z-direction as shown in Figure 3.24. As a result, the net current is essentially zero, resulting in the measured net coupling being very low. Next, consider the via within a portion of the cavity with an approximately uniform electric field. At the anti-pad aperture there is a discontinuity. The electric field fringes out at the edge. The portion of the fringing field normal to the via surface is in the same direction as the coaxial TEM mode as shown in Figure 3.25, resulting in excitation of the coaxial TEM mode. The direction of the fringing electric field in the aperture in the top plate is opposite the direction of the fringing electric field in the aperture in the bottom plate. This results in the opposite polarity electric field within the top and the bottom apertures, which could be incorrectly interpreted as inductive coupling based on the polarity. Essentially, for strong

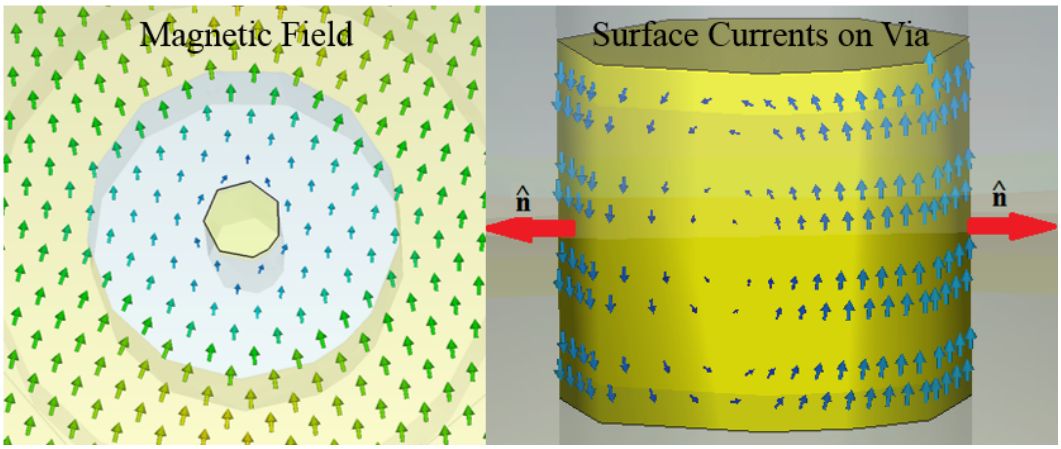

Figure 3.24. Uniform magnetic field around via and corresponding surface currents.

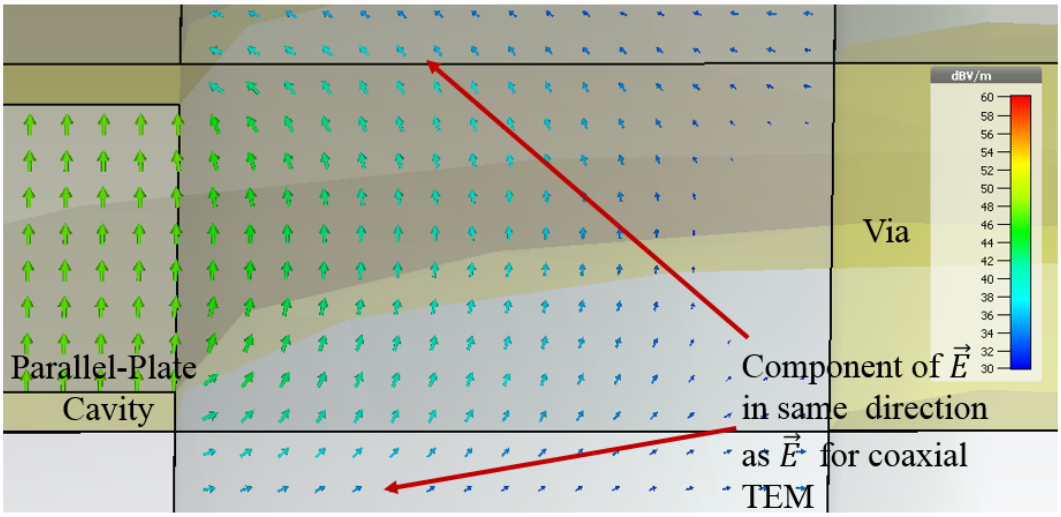

Figure 3.25. Cross-section of the electric field at the via anti-pad.

coupling to the via, the fields in the cavity need to have a strong modal excitation of the coaxial TEM mode in the aperture. In cylindrical coordinates this mode has a radial electric field and a circulating magnetic field in the azimuthal direction. A uniform magnetic field in the same direction is essentially orthogonal to this coaxial TEM mode while the electric field in the aperture is not orthogonal to the mode.

Referencing Figure 3.23, there are only small changes between the coupling for Configuration 1 and Configuration 2 as the stitching vias throughout have little effect because the coupling is dominated by direct coupling from the PWR/GND cavity. Configuration 3 has a larger anti-pad size than Configuration 2. This change results in decreased coupling for Configuration 3 compared to Configuration 2. Analysis of the fields showed that the coaxial mode is excited by the fringing fields in the aperture. Increasing the separation results in a decrease in the coaxial capacitance between the via and the finite plate thickness which then results in less coupling.

3.6. COUPLING TO VIA LOCATED NEXT TO THE POWER CAVITY

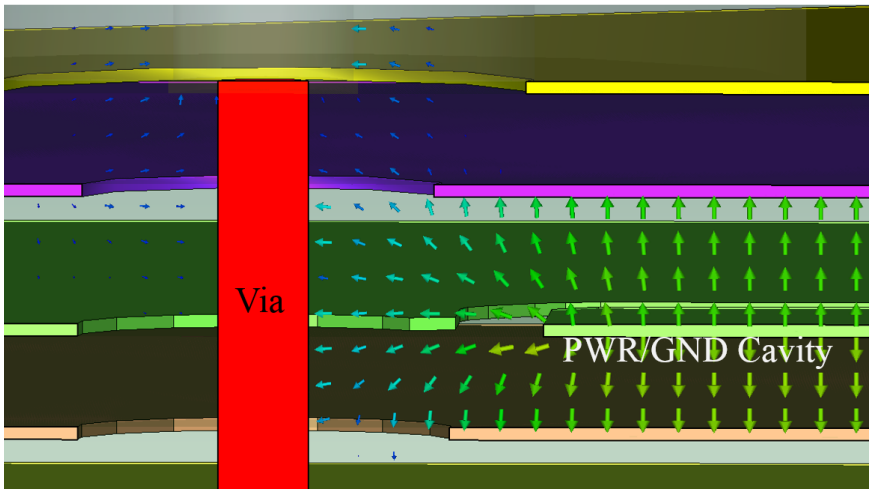

Figure 3.26. Electric field from PWR/GND cavity coupling to via next to cavity.

Figure 3.26 shows a cross-section of the electric field between the via and the PWR/GND cavity. The via is in close enough proximity to the power net, so that the fringing electric field at the edge of the cavity can terminate on the via. The fields at the edge of the cavity are different than the fields within the cavity. The fields in the gap are essentially slotline mode fields: the magnetic field in the gap is in the z-direction while the electric field is in the x-direction. A magnetic field in the z-direction is orthogonal to the azimuthal magnetic field of the via/via coaxial anti-pad aperture. The magnetic field will result in surface currents in the azimuthal direction on the via. However, the electric field in the slot is in the right direction to excite the coaxial anti-pad aperture.

It can be instructive to examine how changes in the geometry affect the coupling. As seen in Figure 3.27, Configuration 2 adds more stitching vias throughout the design and Configuration 3 adds in two more stitching vias in close proximity to the victim via in addition to the other stitching vias. Figure 3.28 compares the coupling to the via next to the power cavity (J9) for three of the different configurations. The additional stitching vias do not affect coupling maxima before 4 GHz. The first three coupling maxima are associated with the first three PWR/GND cavity resonances while some of the later coupling maxima do not occur at a strong cavity resonance. Excitation of the cavities formed between GND area fills/planes is occurring. The excitation of these other cavities was discussed in Section 3.4. When stitching vias are added throughout it prevents standing-wave patterns from forming in these other cavities until higher frequencies. The via is not at the edge of these other cavities, so the coupling mechanism from these cavities will be the same as the coupling to the via in the PWR/GND cavity. The addition of stitching vias in Configuration 2 improves the coupling from 4 GHz to 6.5 GHz. It is around these frequencies where standing-wave patterns develop in the Layer 2-3 GND cavity and Layer 3-4 GND cavity. For instance, at 5 GHz there is relatively strong normal electric field within the area of the Layer 2-3 cavity where the via is located as shown in Figure 3.29. The stitching vias added in Configuration 2 help minimize these standing-wave patterns and thus reduce the

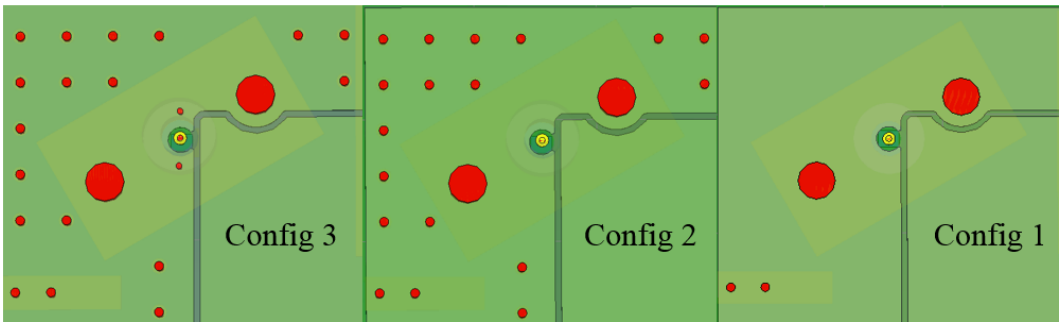

Figure 3.27. Comparison of the number of GND vias around the via for the different configurations.

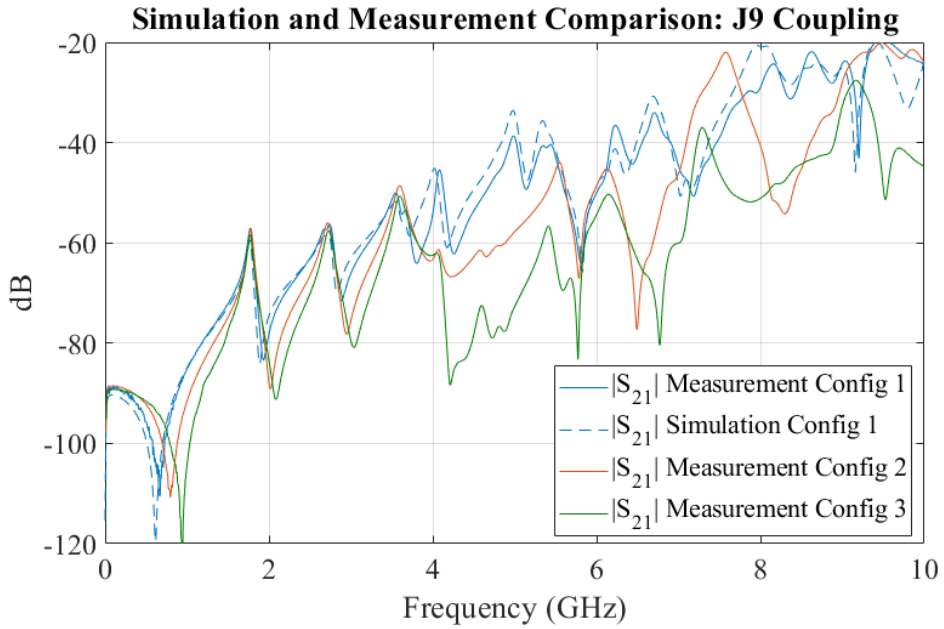

Figure 3.28. Measured and simulated coupling to the via next to the power cavity.

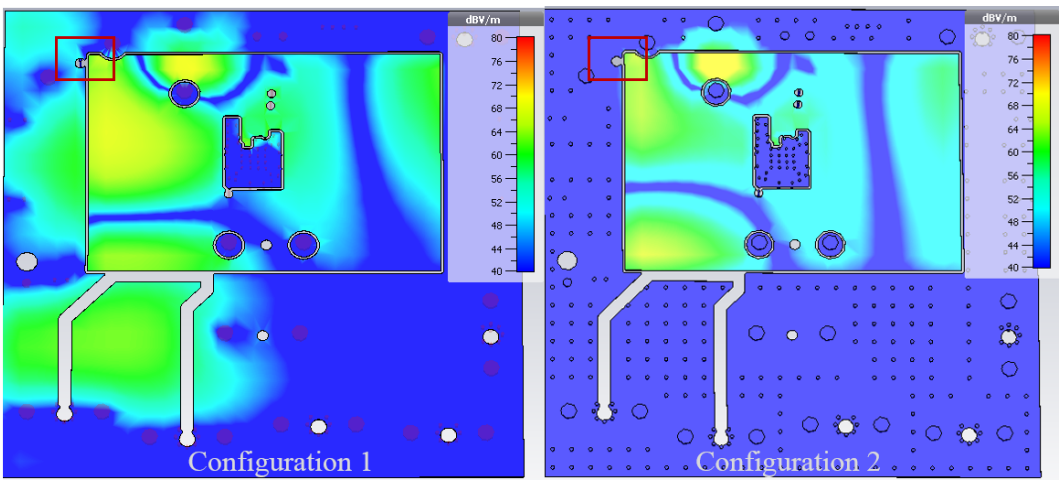

Figure 3.29. Comparison of the Layer 2-3 cavity electric field distribution at 5 GHz between Configuration 1 and 2.

coupling. Standing-wave patterns with electric field maxima in the vicinity of the via occur at other frequencies as well. There are additional improvements in the coupling when two additional stitching vias are added in close proximity to the victim via in Configuration 3. These vias provide additional incident field cancellation and help dampen resonances by the via to higher frequencies because of their close proximity to the victim via.

3.7. COUPLING TO VIA AWAY FROM THE POWER CAVITY

Figure 3.30 plots the measured and simulated coupling to the via away from the PWR/GND cavity for the different configurations. The via is too far away to be coupled to directly from the PWR/GND cavity like the other two victim vias. As a result, the coupling is very low in the lower frequency range. However, as discussed in the previous sections other cavities are coupled to/excited by the PWR/GND cavity. This provides the effective coupling mechanism in the higher frequency range, resulting in an increase in the measured coupling with increasing frequency. Different amounts of stitching vias were placed around the victim via in the three configurations shown in Figure 3.31. For Configuration 2, the

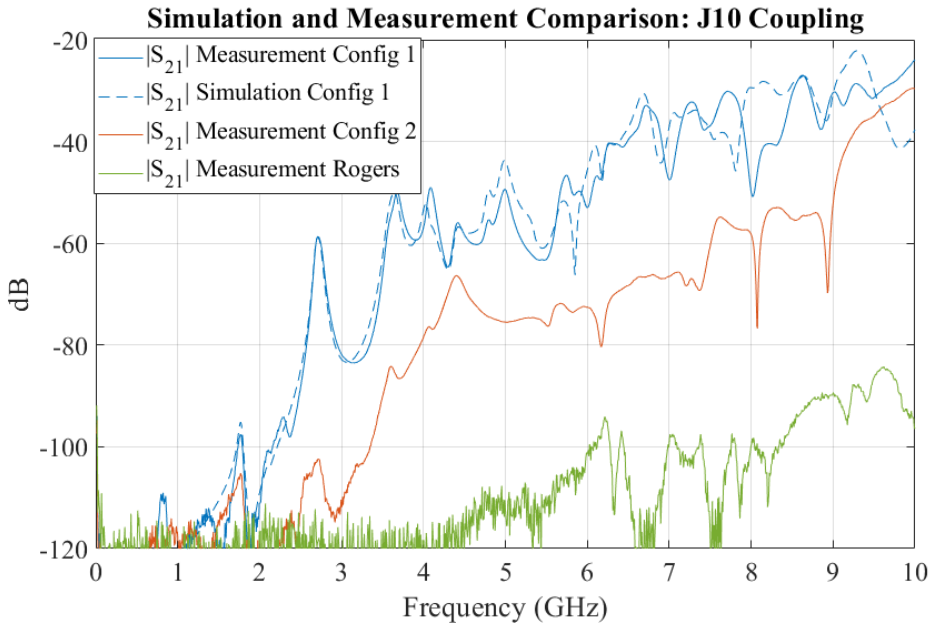

Figure 3.30. Measured and simulated coupling to the via away from the power cavity.

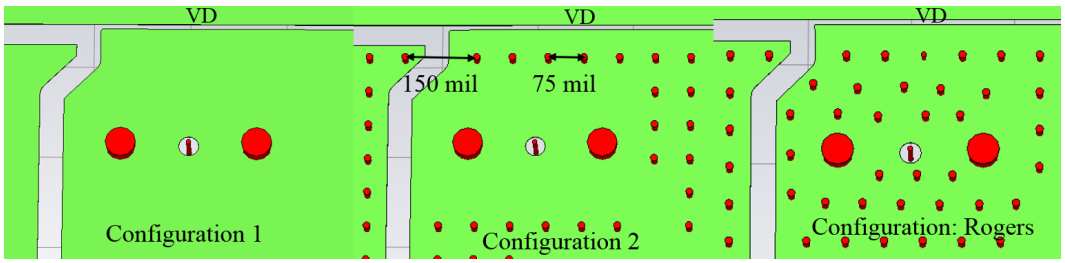

Figure 3.31. Configuration comparison of the number of GND vias around the via.

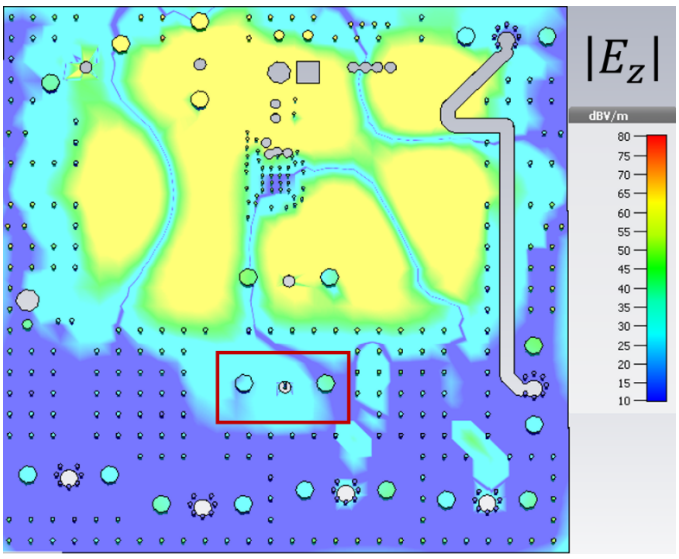

Figure 3.32. Electric field in Layer 4-5 cavity at 10 GHz for Configuration 2.

coupling is lower than -80 dB until about 4 GHz and rises to about -30 dB at 10 GHz. In contrast, for the Rogers Configuration the coupling is below -100 dB until 6 GHz and remains under -80 dB for the entire measured frequency range. In Configuration 2, there are stitching vias that surround the area around the signal via, but they are located about 200 mils away. The row of stitching vias placed closed to the power net area fill clearance gap should greatly reduce the excitation of the horizontally adjacent GND cavities. The vias do not form a solid conductor wall, so there is expected to be some transmitted field through the via row. The amount of leakage through the via fence will increase with increasing frequency as the separation between adjacent vias becomes electrically longer. In Configuration 2, the center to center spacing between vias is 75 mils, but there are some places where a via was not placed due to a clearance constraint, resulting in a larger 150 mil spacing. At 10 GHz, a 150 mil spacing in FR-4 is about an electrical length of $\lambda/4$, so the spacing between those vias is no longer electrically small. Figure 3.32 shows the normal

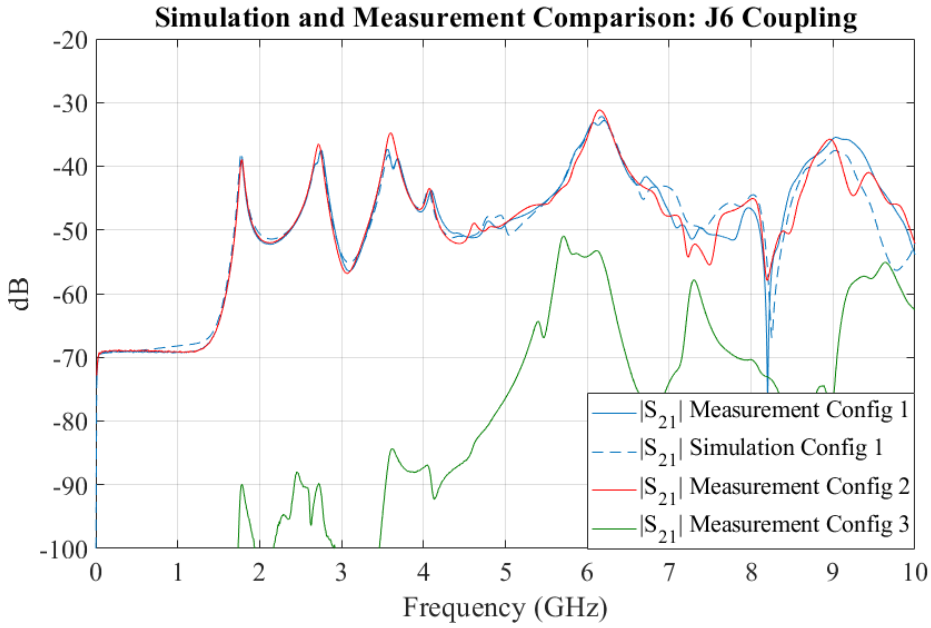

Figure 3.33. Measured and simulated coupling to the stripline next to the power cavity.

electric field in the Layer 4-5 cavity at 10 GHz plotted in dBV/m. The vias are no longer effective at preventing the area around the victim from being excited. Additional study of stitching vias will be presented in Section 5.

3.8. COUPLING TO STRIPLINE ON SAME LAYER AS POWER NET

Figure 3.33 shows the comparison of the coupling to the stripline routed next to the power net area fill for the different configurations. The measurement agrees well with the simulation results. There is little change in the coupling between Configuration 1 and Configuration 2, indicating that direct coupling from the PWR/GND cavity is the dominant coupling mechanism as the stitching vias throughout the GND cavities have little effect. In Configuration 3, the stripline is moved from 15 mils to 45 mils away from the power net area fill. In addition, there is now a small strip of GND conductor between the power net area fill and the stripline. This change greatly reduces the coupling, although there is a local coupling maxima around 6 GHz. Figure 3.34 shows the normal electric field at 5.9 GHz

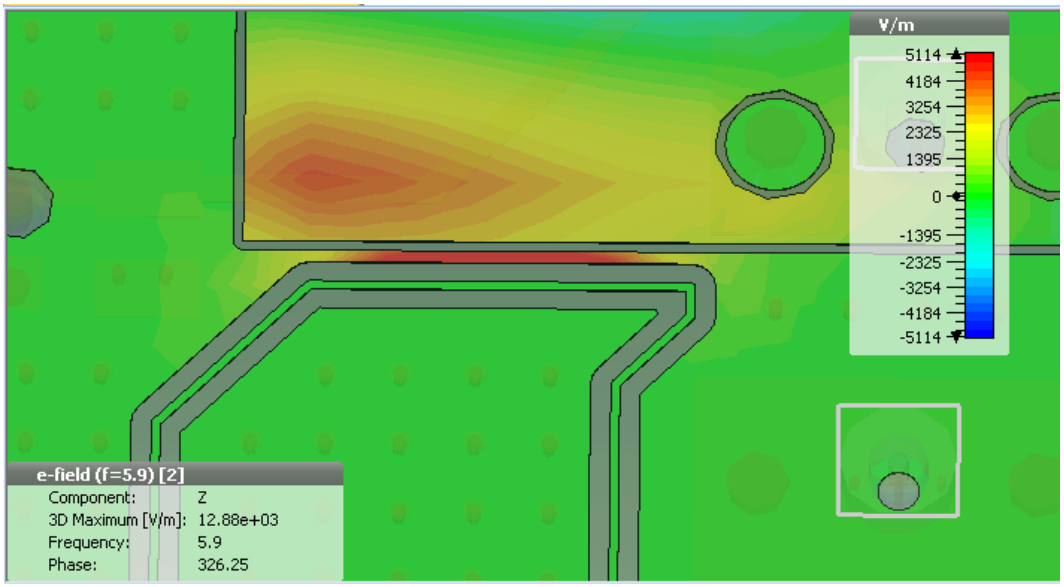

Figure 3.34. Electric field at 5.9 GHz for Configuration 3 showing resonant GND segment.

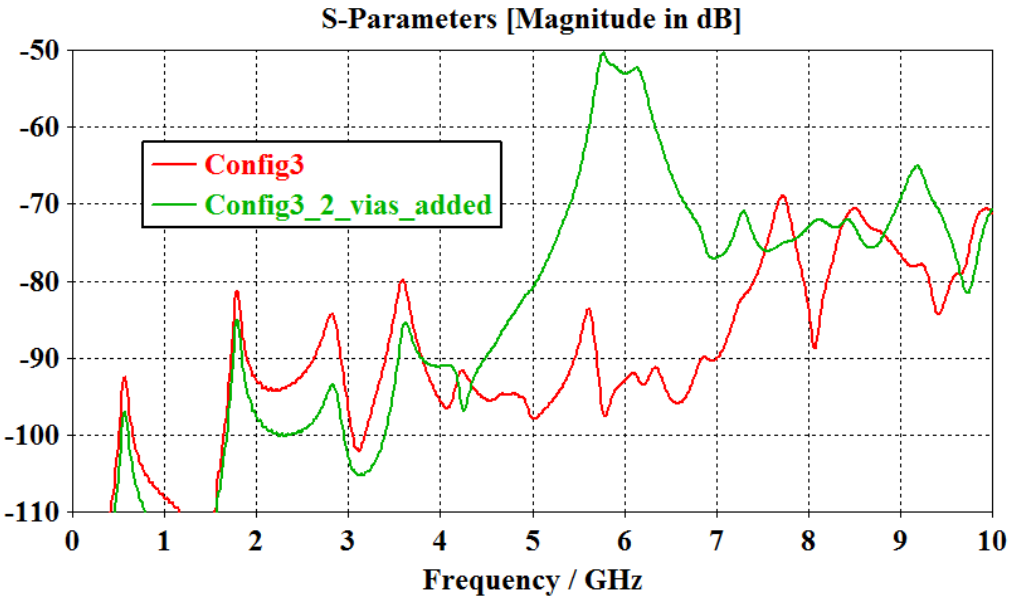

Figure 3.35. Configuration 3 simulated coupling comparison for via modification.

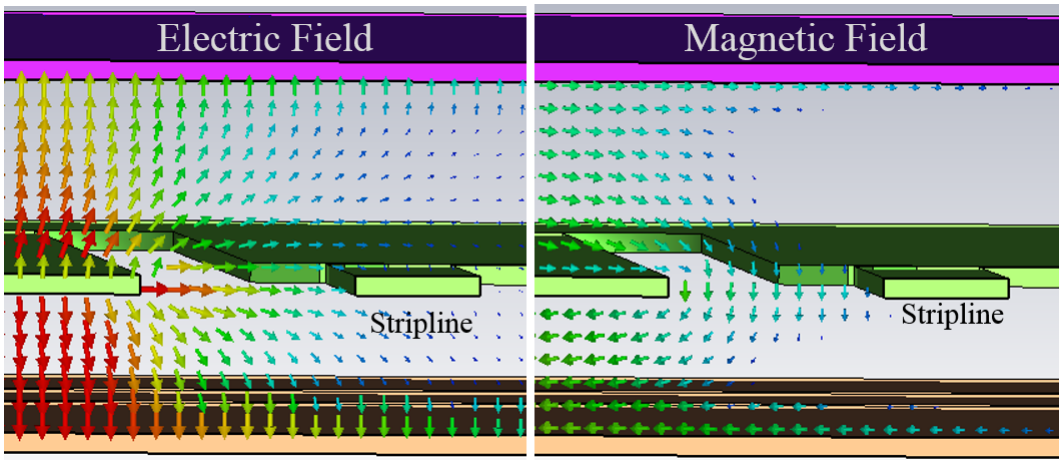

Figure 3.36. Fields of PWR/GND cavity next to stripline on same layer.

for Configuration 3 which show a large electric field on the narrow strip. It appears that a resonator is formed for the narrow strip as there are GND vias on both side of the narrow strip. The distance between the GND vias at either side of this narrow GND conductor is about 17 mm, somewhat close to the $\lambda/2$ electrical length in FR-4 of 24 mm. This resonant section of the GND area fill can then couple to the victim stripline. Adding two stitching vias to the simulation model at the narrow portion of the GND conductor eliminates this coupling mechanism as seen in Figure 3.35. Overall, these results suggest that traces can be routed on the same layer as a resonant cavity, provided they are not in close proximity. The fields between the cavity and the stripline are essentially slotline mode fields as shown in Figure 3.36. At the edge of the cavity the electric field lines fringe out. Some of the field lines terminate on the neighboring reference planes while some electric field lines terminate on the stripline conductor, primarily on the edge of the strip. The magnetic field lines are oriented in the z-direction and do not wrap the stripline. This observation aligns with expectations based on the knowledge that the magnetic field is in the x-y plane (tangential to the surface of the parallel plates) as the magnetic field would need to be in the z-y plane to wrap the stripline. From observing the field distributions, electric field coupling appears to be dominant for this case. It is possible to analyze the resulting field distribution on the

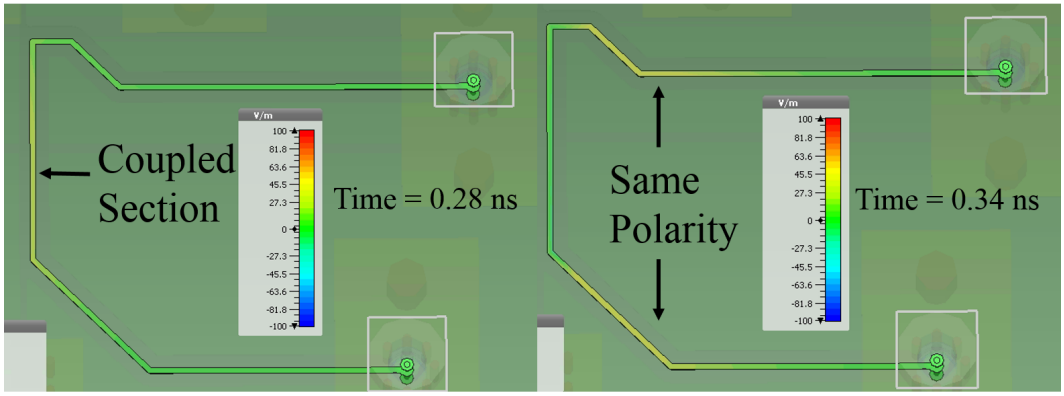

Figure 3.37. Normal electric field of stripline at two instances in time.

stripline to validate this theory. Figure 3.37 shows the normal electric field of the stripline at two instances of time. The middle section of the stripline is where some of the electric field lines from the power net area fill terminate. At the second point in time it can be seen that there are waves propagating towards the vias on both sides of the stripline with both waves having electric fields of the same polarity, indicating capacitive coupling. It also may be helpful to think as the electric field as resulting in a voltage between the stripline and the reference plane. The TEM mode of a stripline has a normal electric field, so this energy excites the propagating TEM mode on the stripline.

3.9. COUPLING TO STRIPLINE ROUTED BELOW CIRCULAR APERTURE

Figure 3.38 shows the comparison of the coupling to the stripline routed over an aperture of the PWR/GND cavity for the different configurations. The addition of stitching vias in Configuration 2 has little effect on the coupling prior to 5 GHz and actually increases the coupling after at some higher frequencies. In Configuration 3 the aperture is removed. This change results in a large decrease in the coupling, demonstrating that the direct coupling through the aperture is the dominant coupling mechanism. Figure 3.39 shows a cross-section of the time-domain electric fields at the aperture. The normal electric field from the

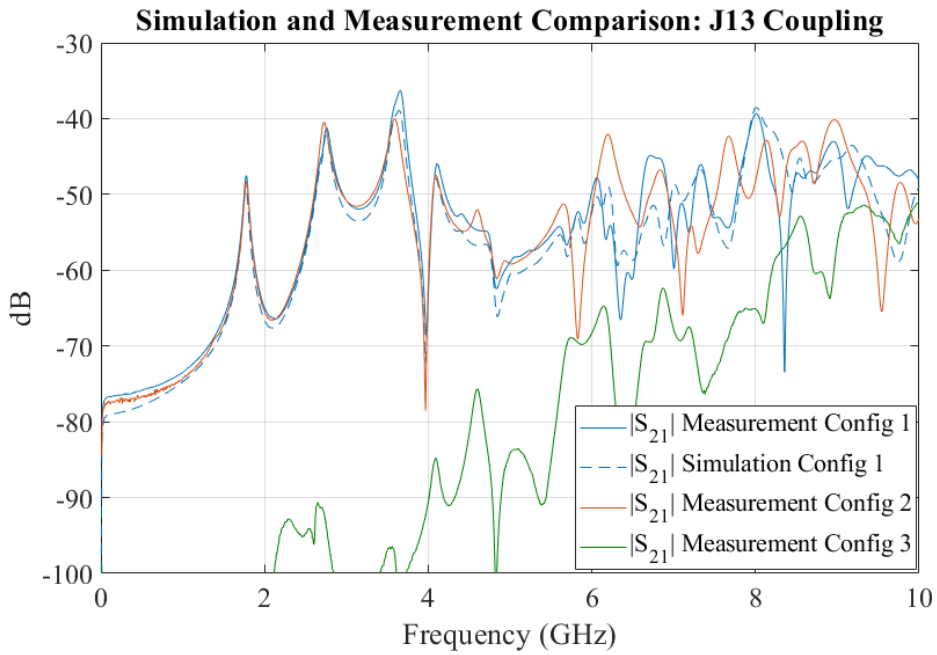

Figure 3.38. Measured and simulated coupling to the stripline routed below an aperture in the power cavity.

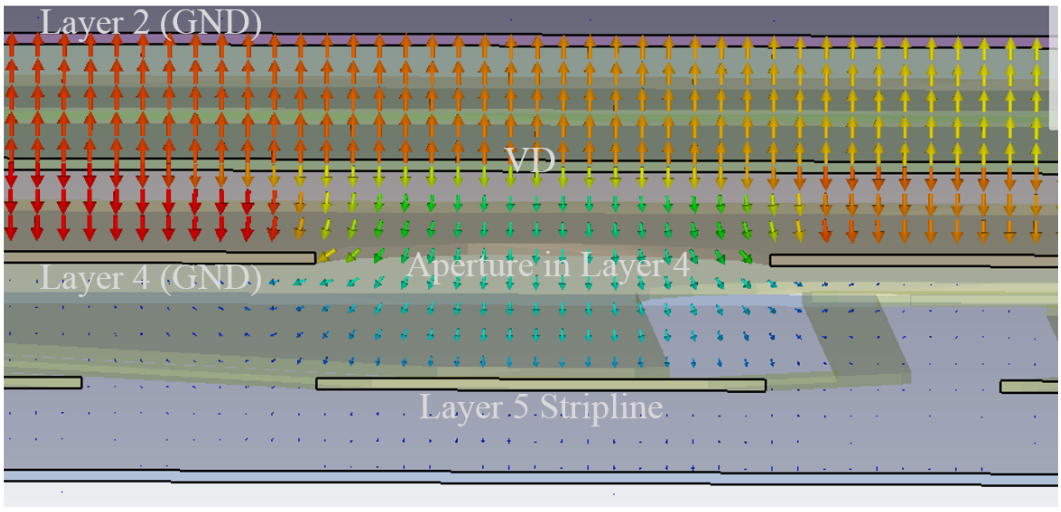

Figure 3.39. Electric field coupling to the stripline through aperture.

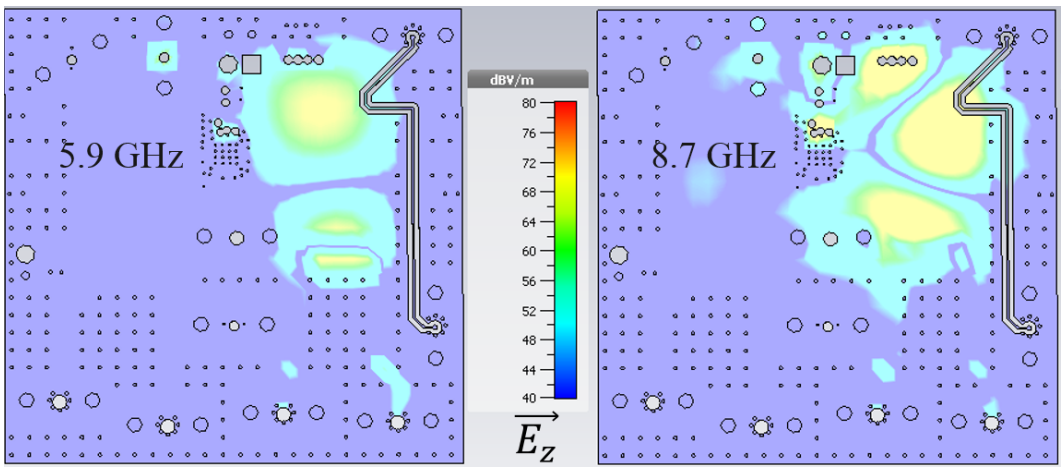

Figure 3.40. Electric field distributions in Layer 4-5 cavity at 5.9 GHz and 8.7 GHz for Configuration 3.

PWR/GND cavity terminates on the stripline, exciting the stripline TEM mode. When the electric field is large in the area around the aperture for a certain modal pattern, the coupling will be high. The magnetic field that fringes around the aperture is orthogonal to the stripline TEM mode and does not contribute to the coupling. Therefore, this coupling mechanism is electric field coupling only. This coupling mechanism is essentially the reciprocal case of an aperture coupled microstrip patch antenna. With the aperture removed, the direct coupling from the PWR/GND cavity is eliminated. Now, the dominant coupling mechanism is from the Layer 4-5 and Layer 5-6 cavities. The ring of GND vias around the signal via should eliminate significant GND cavity coupling to the vias that connect to the stripline. Because only through hole vias were used in these designs, the GND cavities formed underneath the power net area fill are not stitched. As a result, standing-wave patterns develop in these areas in the two cavities as shown in Figure 3.40 for 5.9 GHz and 8.7 GHz. There are local maxima in the Configuration 3 coupling at these frequencies. These fields can couple to the stripline in the same manner as the stripline next to the power cavity.

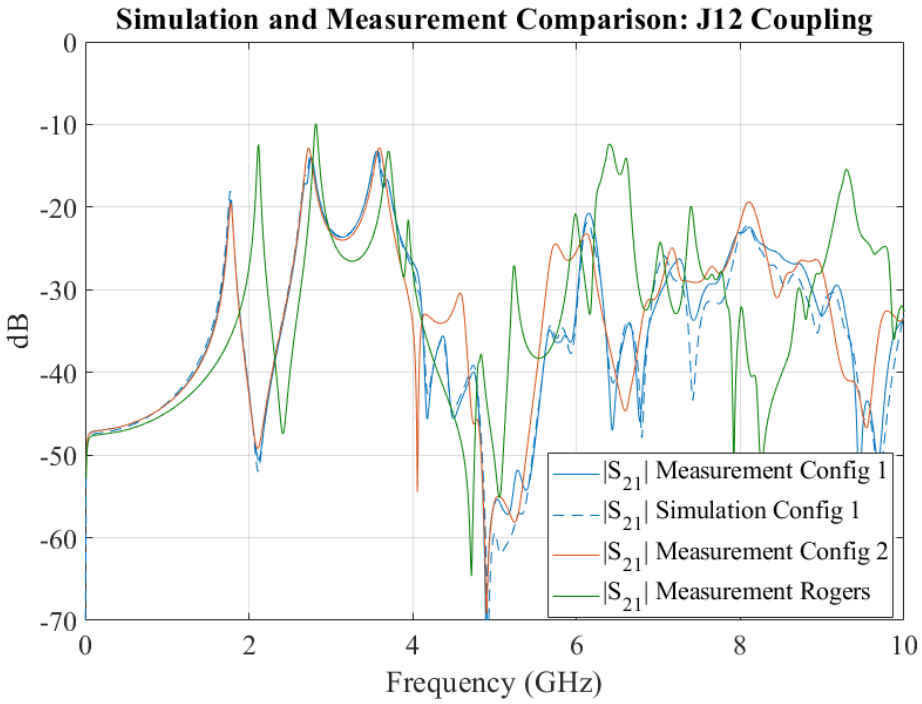

Figure 3.41. Measured and simulated coupling to the stripline referenced to power net area fill.

3.10. COUPLING TO STRIPLINE REFERENCED TO POWER NET AREA FILL

Figure 3.41 compares the coupling to the stripline partially referenced to the power net area fill for some of the different configurations. The coupling to this stripline is the largest out of all the victim interconnects in these test vehicles. This stripline is routed over two clearance gaps that occur between the power net area fill and GND area fill on Layer 3 as seen in the left side of Figure 3.42. One of the most common design guidelines for EMC and signal integrity is to avoid routing microstrip or stripline transmission lines over gaps in the reference plane. The discontinuity results in energy lost to the slotline mode of the gap which can then couple elsewhere through the PCB or, if the slot is electrically long, the slot can radiate, causing external EMI. Figure 3.43 shows a cross-section of the time-domain electric field where the stripline crosses the gap on the left side and a cross-section of the electric field 100 mils away from the gap crossing on the right side. Although the concern

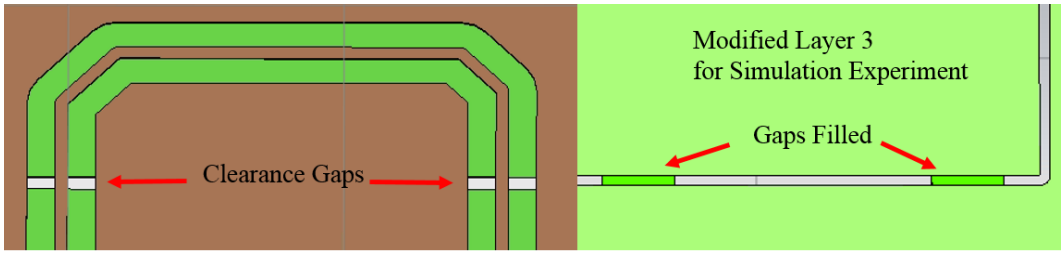

Figure 3.42. Stripline routed over clearance gap between power and GND area fills.

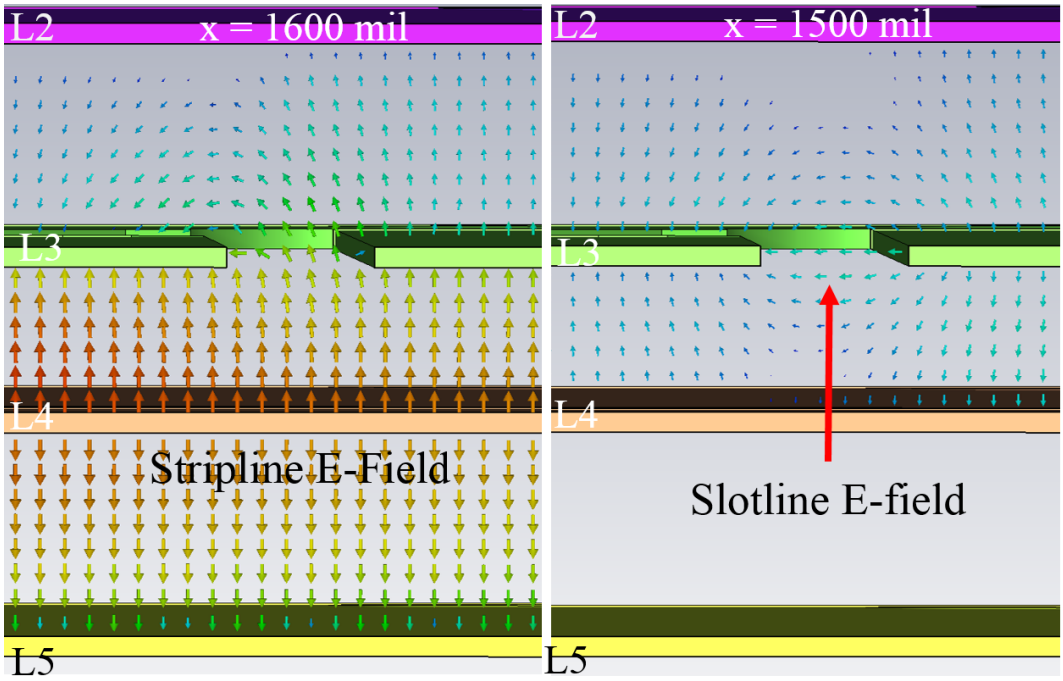

Figure 3.43. Electric field cross-sections showing the stripline crossing the gap excite a slotline mode.

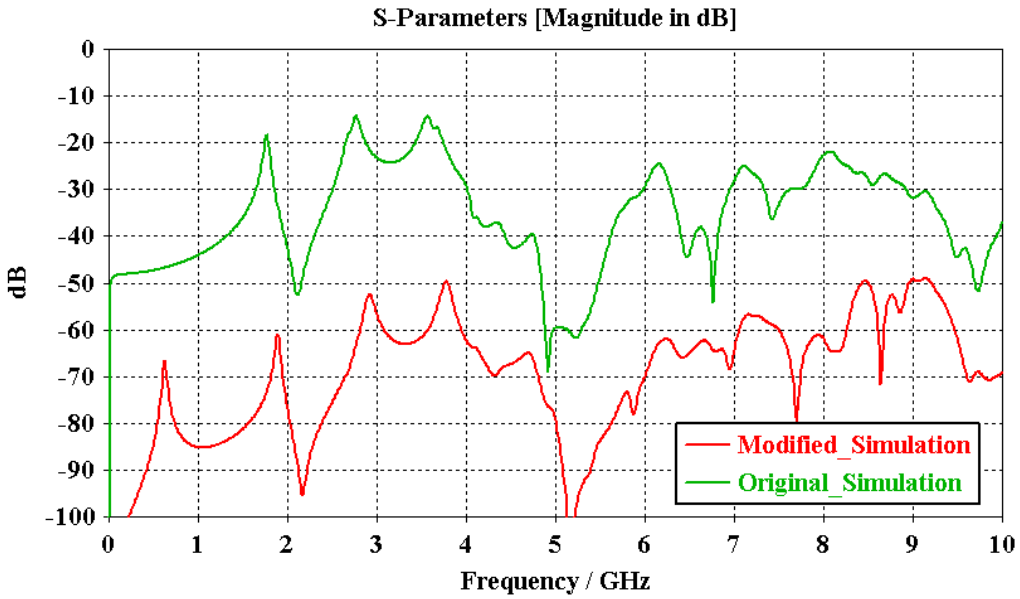

Figure 3.44. Electric field cross-sections showing the stripline crossing the gap excite a slotline mode.

here is the reciprocal case where the cavity couples to the transmission line, reciprocity applies and the coupling mechanism is clearer when analyzed in this way. In the right side of Figure 3.43 it can be seen that there is a normal electric field in the upper cavities, showing they have been excited by the stripline. At a 100 mil distance away from the stripline, the propagating slotline mode excited by the stripline can be clearly seen. The slotline fields excite the cavities bordering the slot. By reciprocity, if there are strong fields in one of the cavities the slotline mode can be excited by those fields and then couple to the stripline. There is little change in the coupling from Configuration 1 to Configuration 2 as the stitching vias have little effect on this coupling mechanism. The coupling maxima for the Rogers Configuration are higher because of the higher Q of the cavity that results from the low-loss dielectric. The resonant frequencies are also shifted to higher frequencies because the Rogers material has a lower dielectric constant than FR-4, decreasing the electrical length. The simulation model was modified by placing narrow connections between the GND area fill and the power net area fill to maintain a continuous reference for the stripline as shown

in the right side of Figure 3.42. The simulated coupling between the two simulation models is shown in Figure 3.44. Eliminating the gap greatly reduces the coupling to the stripline, demonstrating that it is the primary coupling mechanism. Connecting the two area fills together to provide a solid reference is not a solution to the problem as both conductors then have the same DC potential. The modification was done to demonstrate that the crossing of the gap is the primary coupling mechanism for this interconnect. Stitching capacitors across the gap have been used to partially mitigate this discontinuity, but this fix loses effectiveness at higher frequencies because of the high inductance associated with the discrete capacitor connection [47]. Also, if instead the entire plane was the power net rather than being a split plane then the via transitioning to the stripline would be within the PWR/GND cavity. Referencing a stripline to a power net will result in a via being in the PWR/GND cavity or the stripline crossing the clearance gap between the two area fills. As a result, a discontinuity that leads to coupling to the interconnect will exist either way when a stripline is referenced to the power net.

3.11. COUPLING FROM EDGE LAUNCH COAXIAL CONNECTORS

There can also be coupling paths from the RFIN and RFOUT microstrips to the various victim interconnects. For this research it is important to characterize these coupling paths to check if they are larger than the coupling from the power noise injected into the PWR/GND cavity. The amplifier output signal will be at a much higher power level than the noise coupled into the system from the IC's power pin. Fringing electric fields from the microstrip can terminate on the other planes and excite the TM_{z0} propagating mode in the other cavities throughout the design. Once the cavities are excited coupling can occur through the various mechanisms discussed in this section. External fields from other sources can also couple into the PCB in the same way. The use of an edge launch SMA connector will greatly increase the edge excitation of the cavities throughout the PCB. The standard, low-cost edge launch SMA connectors are not matched well to multi-layer

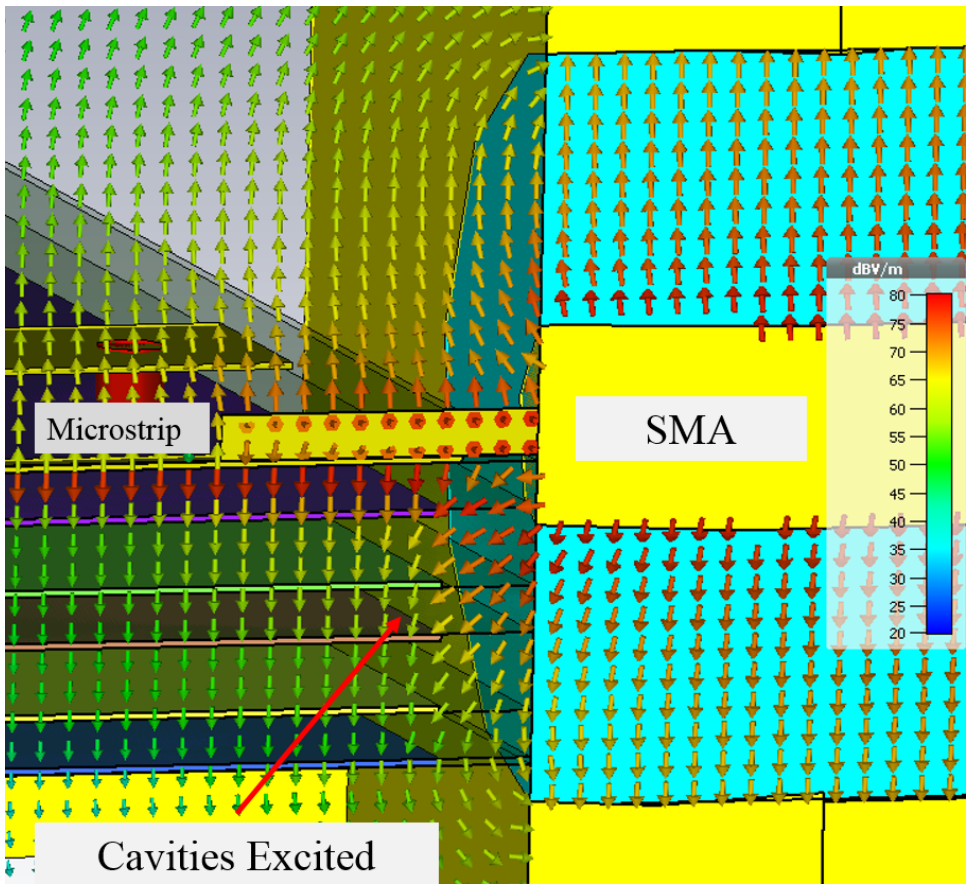

Figure 3.45. Electric field of coaxial connector exciting PCB cavities.

PCBs: the dimensions of the coaxial portion is much larger than the dimensions of the microstrip. In addition to leading to poor transmission performance, it also can result in efficient coupling to the cavities. The SMA edge launch connector was added to the simulation model in Microwave CST. Figure 3.45 shows the cross section of the electric fields plotted in dBV/m at the board edge. The radial electric field of the TEM coaxial mode is in the right orientation to excite the TM_{z0} mode of the cavity. As a result, the cavities will be much more strongly excited than the microstrip only case. Figure 3.46 shows a comparison of the geometry for the SMA launch section of the PCB for three of the different configurations. In Configuration 1, there are only four GND vias around the SMA. In Configuration 2, many additional stitching vias are added around the SMA SMT

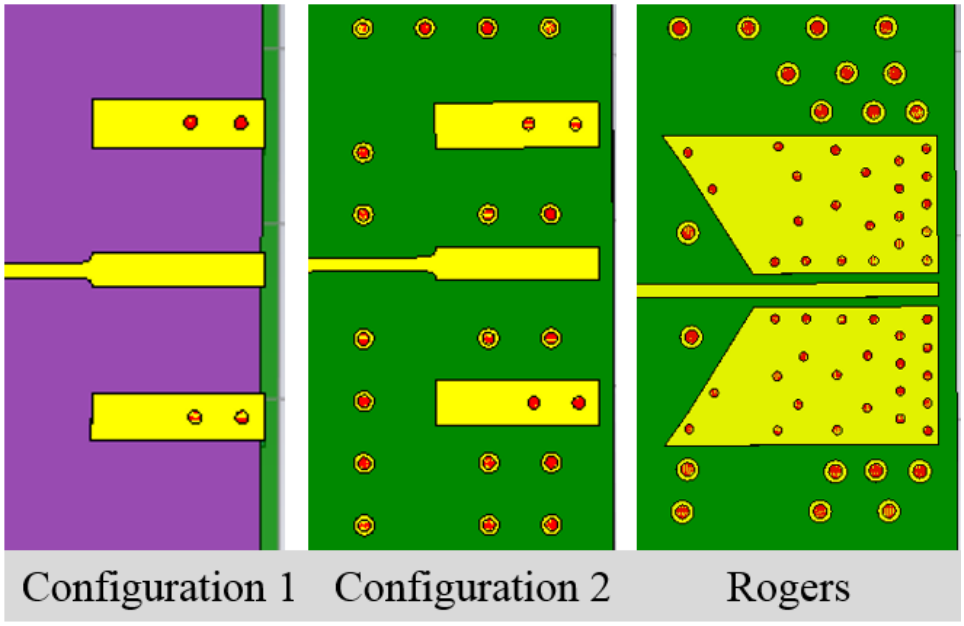

Figure 3.46. SMA end launch structure comparison for the different configurations.

pads, which help reduce the excitation of the cavities from the coaxial fields. In the Rogers Configuration, more stitching vias were added and the SMA connector used was changed to one that transitioned to a smaller coaxial diameter. Network analyzer measurements were performed on each of the configurations to compare the performance. To terminate the microstrip, a 0201 50 ohm resistor was soldered between the microstrip and the IC GND paddle SMT pad. Port 1 was connected to the SMA edge launch connector and Port 2 was connected to one of the various victim interconnects. Figure 3.47 compares the measured and simulated coupling to the victim via in the PWR/GND cavity for the different PCB configurations. For the simulated results, the coupling is much greater when the microstrip is excited with the SMA connector rather than a discrete port, demonstrating that the primary coupling mechanism is from the SMA connector. For Configuration 1, the measured coupling is very large as the sparse amount of GND vias around the SMA are not effective at minimizing the cavity excitation at higher frequencies. Adding many more stitching vias greatly reduces the coupling by around 30 dB for much of the frequency

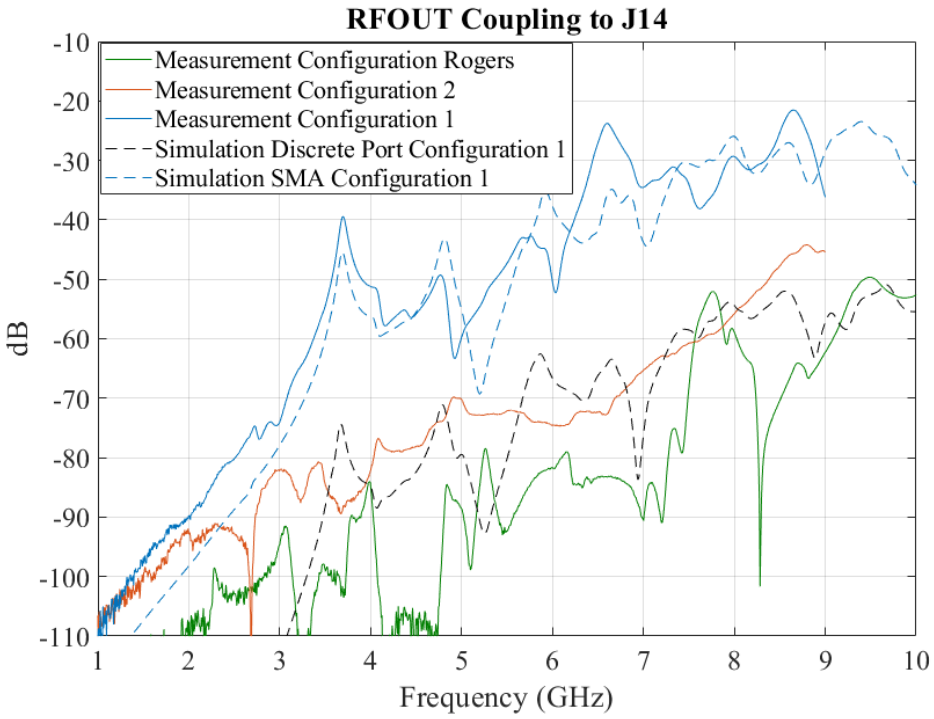

Figure 3.47. Measured and simulated coupling from RFOUT to via in PWR/GND cavity.

range as seen in the measured coupling for Configuration 2. For the Rogers Configuration the SMA edge launch connector was changed to one that transitions to a smaller diameter, so that the fields are more contained. This change as well as adding more stitching vias results in even more reduction of the coupling as seen by the measured coupling for the Rogers Configuration. The SMA connector used in the Rogers Configuration also greatly improves the return loss measurement. Studies have been performed to optimize the SMA end launch structure on the PCB for transmission performance at high frequencies such as [48]. Often improvements for transmission performance also help with noise isolation. For instance, if strong resonances are occurring in the PCB they often manifest themselves with dips in the insertion loss.

4. INTEGRATION OF ACTIVE AND PASSIVE COMPONENTS

4.1. NOISE COUPLING FROM IC THROUGH THE PDN

This section is concerned with predicting the coupling to interconnects from the power distribution network (PDN) due to noise injected from the IC's power pin into the PDN. Section 3 analyzed the coupling mechansims between the PWR/GND cavity and various interconnects. By reciprocity, if an interconnect can be coupled to by a cavity it can also excite the cavity. For instance, multiple signal vias transitioning through a cavity can couple to the cavity, resulting in the build-up of noise in the cavity. This type of noise generation is not present in these test vehicles. In this study the IC used is an amplifier. There will be some amount of RF leakage on the IC's power pin which is then injected into the PDN and can then couple efficiently through the mechanisms analyzed in Section 2 and Section 3. Figure 4.1 shows a simplified diagram of the noise coupling mechanism. This section will develop a method to predict the amount of noise that is coupled via this mechanism.

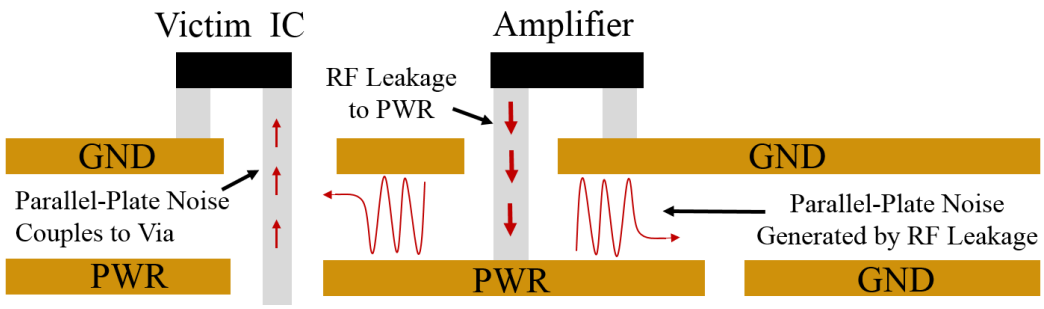

Figure 4.1. Simplified diagram of the noise coupling mechanism studied in this section.

One of the main approaches that has been used for calculating the noise coupling from a PDN is to use Z-parameters (the transfer impedance) [11]. This approach assumes that the impedance of the source is much larger than the PCB which allows the source to be modeled as a current source. Z-parameters are proportionality constants that relate an input current to an output voltage. Because the input, the IC, can be modeled as a current source the Z-parameters are well suited for the calculation as input currents are used to calculate output voltages. Z-parameters can be obtained from S-parameters and thus network analyzer measurements, using network parameter conversion equations available in many microwave theory texts [4]. However, the assumption that allows the IC to be modeled as a current source is typically only valid in the MHz frequency range. For instance, for the test vehicle used in this research the impedance of the IC is only much larger than the impedance of the PCB until about 200 MHz as seen in Figure 4.2. Using the transfer impedance for noise voltage prediction at higher frequencies will likely produce erroneous results. Consequently, another approach is needed to calculate the noise coupling at higher frequencies.

4.2. INPUT IMPEDANCE OF PCB PDN SEEN BY IC

In this research, a circuit model of the IC was not available so measurements were performed to determine the RF to VD isolation and are covered in the Appendix. Amplifiers are designed with biasing networks to block RF to the DC bias, but there is still some RF leakage through these bias networks. A simplified diagram of the RF leakage in the amplifier to the VD net is shown in Figure 4.3. These measurements were performed using test equipment with 50 ohm port impedances. However, the power distribution network (PDN) is not a 50 ohm system so the power transferred to the PDN will be different than the power transferred to a 50 ohm system. To determine the power transfer to the PDN, the input impedance of the PDN needs to be known. This is the impedance looking into the IC PWR/GND SMT pads that the IC will see as shown in Figure 4.4. This input

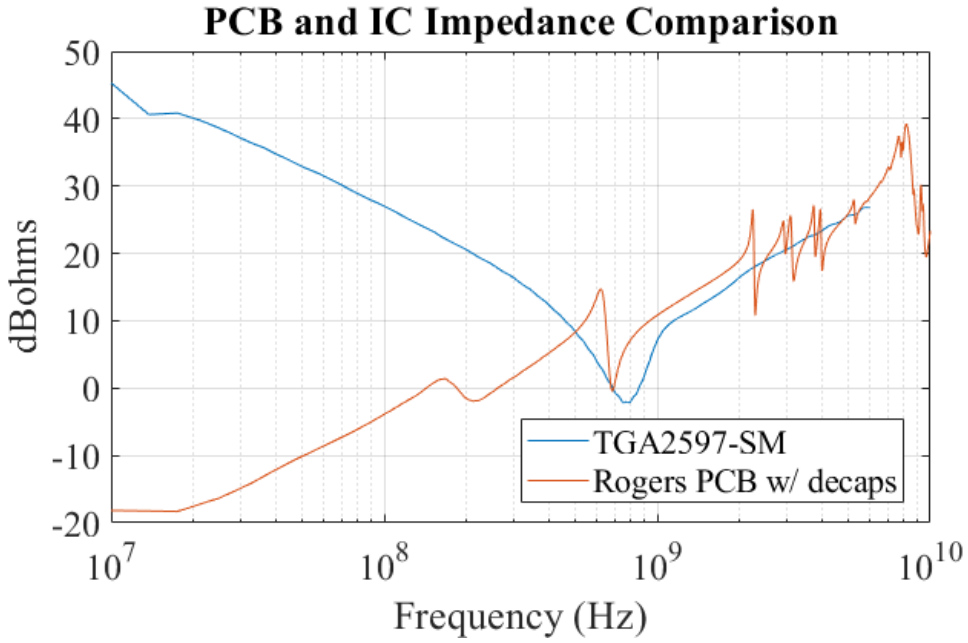

Figure 4.2. Comparison of input impedance of IC and PCB in log scale.

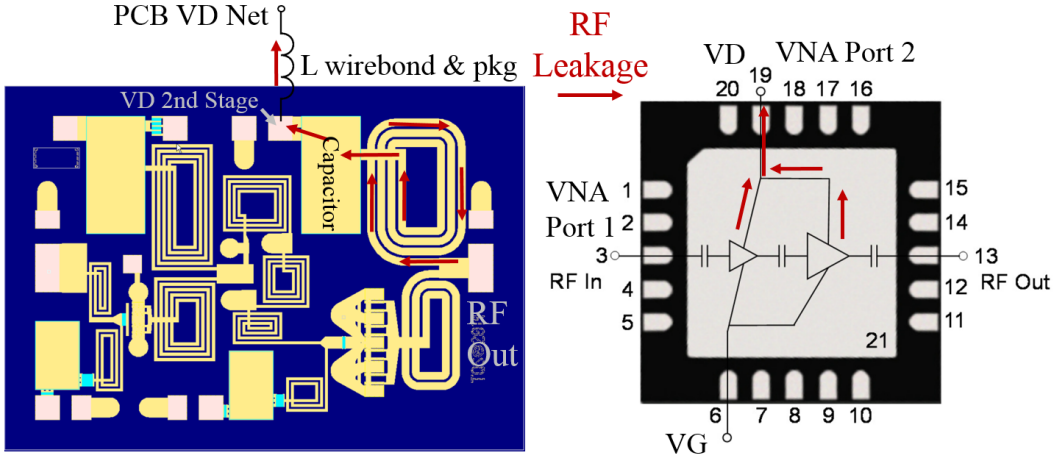

Figure 4.3. Simplified diagram showing the RF leakage to VD in the amplifier.

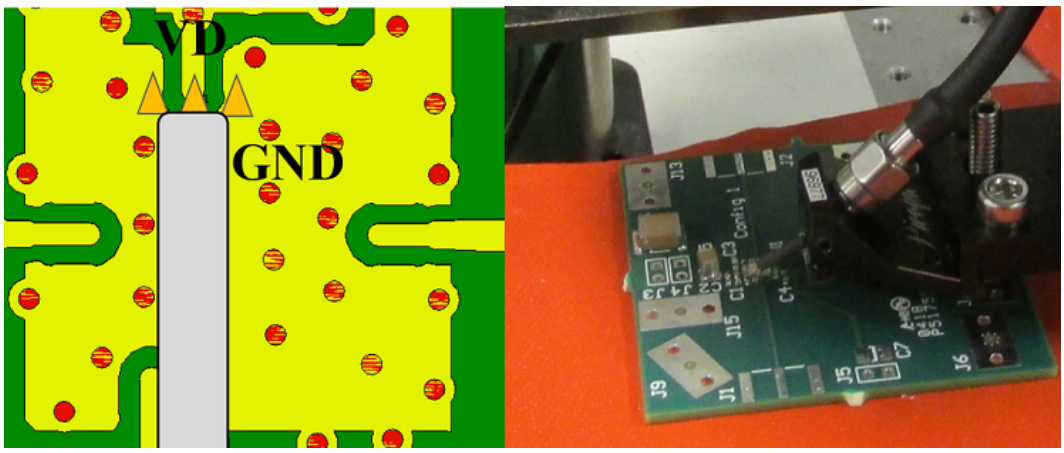

Figure 4.4. Impedance is measured where the IC's VD pin is located once the IC is installed.

impedance can be measured or obtained from a full-wave electromagnetic simulation. In addition, the input impedance looking into the IC pin must be known as well to determine the power transfer. Typically for PDN measurements in the MHz range, a 2-port impedance measurement technique is used that has good dynamic range for very small impedances and was first proposed in [49]. However, in the GHz range the PDN impedance is no longer small. As a result, the 1-port reflect impedance measurement is best suited because it has good dynamic range for impedances around 50 ohms. The impedance of the IC was also obtained using this method and is described in the Appendix. The impedance is obtained from S_{11} using (4.1) where Z_0 is the port impedance which is 50 ohms for most network analyzers.

$$Z_{in} = Z_0\left(\frac{1 + S_{11}}{1 - S_{11}}\right) \tag{4.1}$$

For the PCB impedance measurement, a Picoprobe 40A-GSG-520-DP (520 μm pitch) probe was used and a SOL calibration was performed using the Picoprobe CS-9 calibration substrate to move the reference plane to the probe tips. The measurement frequency range was 10 MHz to 12 GHz, the IFBW was set to 500 Hz, and the power was

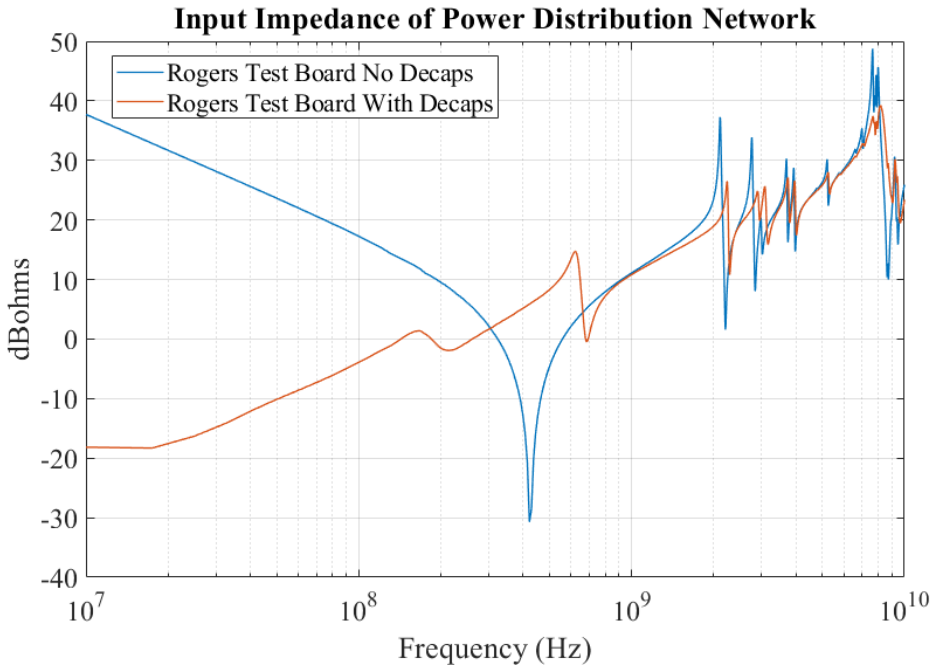

Figure 4.5. Input impedance looking into the PDN with and without decoupling capacitors.

set to 0 dBm. The measurement was performed with and without the decoupling capacitors installed. In addition, the measurement was performed with different variations of the PCB that each had the PA IC at different locations. One of the test board variations used Rogers material RO4350 for the dielectric while the others used a FR-4 dielectric. Figure 4.5 shows the input impedance of the power distribution network in log scale for the Rogers test board with and without decoupling capacitors installed. This is the impedance the IC sees looking into the PCB. For power integrity purposes, the input impedance should be kept as low as possible. A larger impedance results in a larger noise voltage which can lead to jitter or functional failures [50]. As a result, power distribution networks are typically designed to not exceed a certain target impedance to ensure the noise voltage does not exceed requirements for the IC. At lower frequencies, the decoupling capacitors are effective at lowering the

impedance looking into the PDN as seen in Figure 4.5. However, after about 200 MHz the impedances of the two cases are comparable except for the PCB with decoupling capacitors has a much lower impedance at frequencies with a cavity resonance.

For digital ICs, it is important to note that after a certain frequency the PCB impedance does not affect the impedance the on-die transistors see [50]. When looking into the IC from the PCB at higher frequencies, the impedance is dominated by the inductance associated with the package and wirebond connections. Conversely, a transistor on an IC is looking out towards the PCB: it sees the on-die capacitance in parallel with the wirebond/package inductance connected to the PCB input impedance. Comparatively the on-die capacitance is much smaller than the capacitance of a typical SMT capacitor. Although, the on-die capacitance has much less connection inductance so it retains its capacitive behavior to higher frequencies. At higher frequencies, the impedance of the on-die capacitance will be smaller than the impedance associated with the inductance of the wirebond/package/PCB impedance. Consequently, at higher frequencies, the on-die capacitance dominates the impedance seen by the transistors on the IC, i.e. the on-die capacitance supplies charge to the on-die switching circuits. A simplified equivalent circuit can illustrate this. The impedance seen by a device on die is simulated with the simple equivalent circuit model of Figure 4.6. The use of 1 A source in the SPICE simulation results in a voltage that equals the impedance. The PCB impedance was set to 0.1 ohms for one case and to 1 Mohm for the second case. As can be seen in the simulated result in Figure 4.7, the PCB impedance has a negligible effect at higher frequencies as the two simulation models converge. This high frequency range impedance only depends on the value of the on-die capacitance and its associated inductance. The PCB impedance is critical at lower frequencies where typically decoupling SMT capacitors are still effective. Another way to describe this, would be that the package/wiredbond inductance acts as a low-pass filter, blocking high frequency noise on the PCB from reaching the IC.

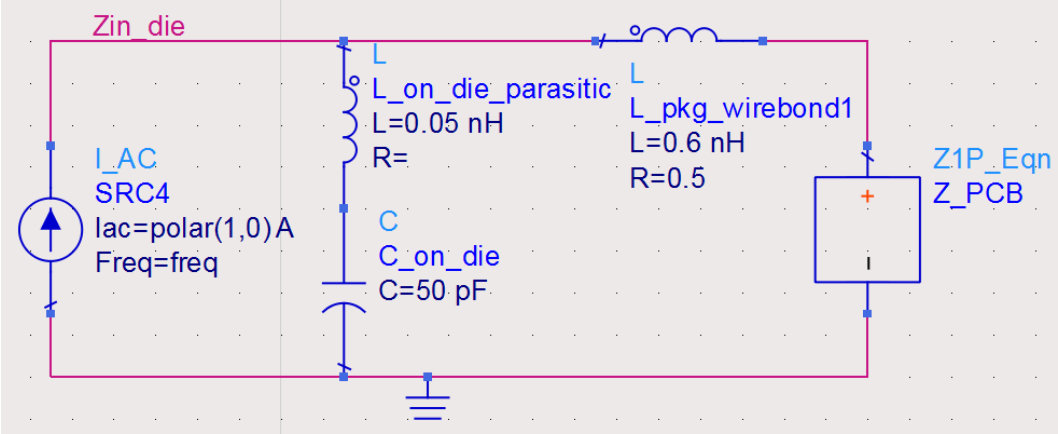

Figure 4.6. Simplified equivalent circuit model of impedance seen by on-die devices.

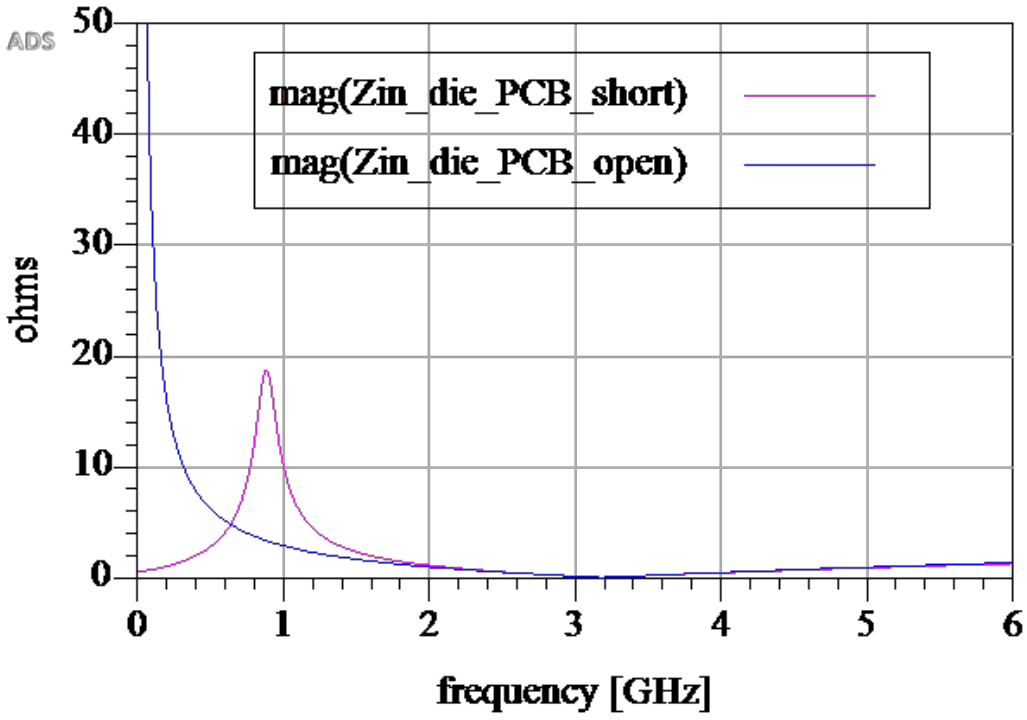

Figure 4.7. Comparison of simulated results of impedance seen by on-die capacitance.

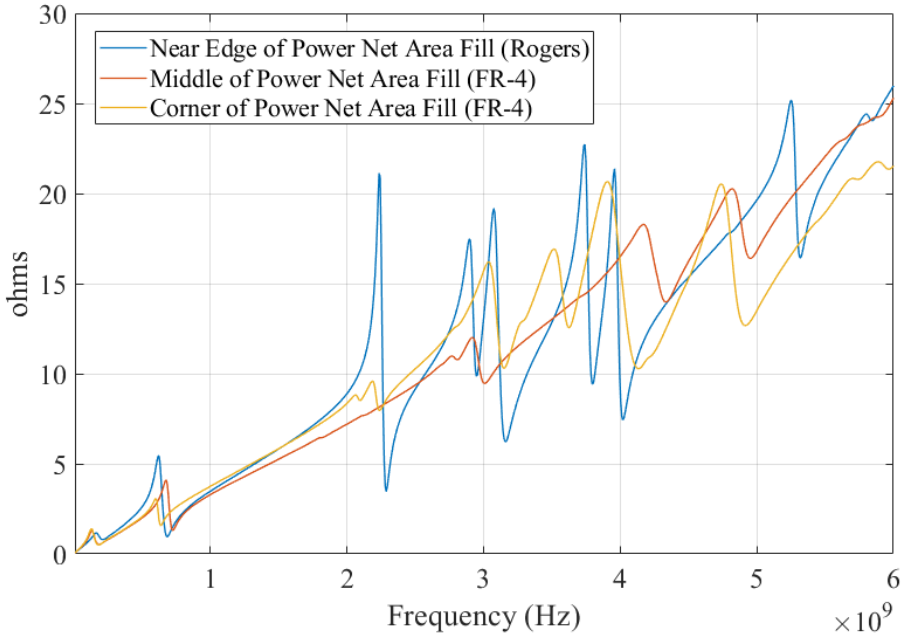

Figure 4.8. Input impedance comparison of different configurations where the IC is at different locations.

Because the PDN impedance no longer affects the impedance seen by the devices on the IC at higher frequencies, it is no longer a true power integrity problem. Still, the PCB impedance is relevant to the noise coupling problem. Another potential consequence of the resonant power distribution network is the creation of undesired feedback paths. If the feedback path is significant it could result in amplifier instability, i.e. the amplifier becomes an oscillator [33]. The TGA2597-SM datasheet [51] recommends that 10 ohm resistors be placed in series with capacitors for VG and VD biasing. Datasheets for similar amplifiers produced by Qorvo contain similar recommendations. However, these datasheets do not include any information on why the resistors are needed. It is likely these resistors are recommended to introduce additional loss to dampen or lower the Q of the PCB resonances. Dampening the resonances should reduce the strength of undesired feedback paths, lowering the risk of amplifier instability. The effect of these series resistors will be examined later in the next section.

Figure 4.8 shows the PCB input impedance for different test boards with the IC located at different locations. Decoupling capacitors were installed on each of the test boards. Each of the impedance curves follow a similar overall trend, but the impedance values at cavity resonant frequencies are different. The location of the excitation will determine how strongly a certain mode is excited. This is captured in the analytical equations for a cavity and has been proposed as a noise mitigation strategy in the literature [7]. For instance, the input impedance of the PCB with the IC located in the middle of the power net area fill has the least amount of impedance peaks. The field distributions for most of the modes contain nulls towards the middle of the cavity so those modes are not excited very well when the source is placed in the middle. When the IC or excitation source is located in the corner or on the edge as in the other two cases, more resonances are excited as seen by the multiple impedance peaks. This is because the field distributions of the modes often contain maxima at the edges or corners of the cavity. The test board with Rogers material has the largest impedance peaks which are also more peaked, i.e. a higher Q. As discussed previously, the smaller dielectric loss of the Rogers dielectric material results in a higher Q.

4.3. EFFECT OF PASSIVE COMPONENTS ON THE PCB PDN INPUT IMPEDANCE

It can be more insightful to examine the impedance in its complex form. Figure 4.9 plots the real part of the input impedance in the top subplot and the imaginary part of the input impedance in the bottom subplot for the Rogers PCB without decoupling capacitors installed, with decoupling capacitors installed, and with decoupling capacitors with 10 ohm resistors in series. At resonant frequencies of the cavity, the real part of the input impedance grows very large while it is close to zero at other frequencies. This large resistance at resonant frequencies is from power being delivered from the cavity to somewhere else. For antennas this is called the radiation resistance and represents power lost to radiation. It is an effective resistance. In this case, there is radiation, but there is also power delivered throughout the

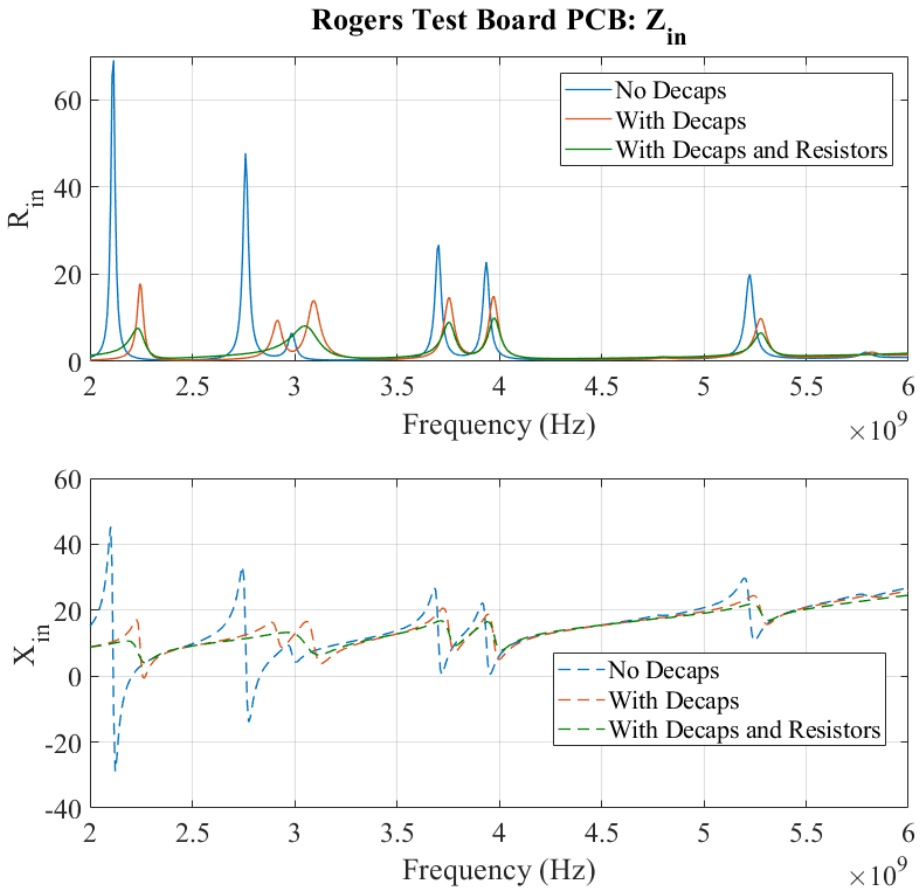

Figure 4.9. Input impedance for the Rogers test board in complex form.

PCB through near-field coupling mechanisms. The addition of the decoupling capacitors greatly reduces the real part of the input impedance at resonant frequencies. The imaginary part of the input impedance is primarily positive, i.e. an inductive reactance. However at resonant frequencies, the imaginary part is negative, i.e. a capacitive reactance. The addition of the decoupling capacitors also greatly reduces the magnitude of the imaginary part of the input impedance at resonant frequencies. The capacitors do introduce some additional loss that contributes to the dampening the cavity resonances. However, the primary damping mechanism is the loading of the cavity with an impedance that will change the input impedance. For the simple case of a two-port network an impedance, Z_L,

connected at port 2 will change the impedance looking into port 1 as shown in (4.2).

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_L} \tag{4.2}$$

In it was [18] shown analytically that at the series resonant frequency of a capacitor, where the inductive reactance and capacitive reactance cancel, the capacitor is most effective at dampening the resonances. The series resonant frequency for a SMT decoupling capacitor is typically on the order of 100s of MHz which is below the GHz range of concern for this work. Additional studies of the effect of decoupling capacitors in the GHz range were performed in [52] and found that in general the dampening was not very significant in the GHz range. Although the measurements in this work show the capacitors do not eliminate the modes, they do reduce the real input impedance by at least half. However, the studies in [52] were performed on high layer count (24 layers) PCBs representative of high-performance server boards where the power planes were approximately in the middle of the stack-up. One possible explanation for the discrepancy is that the test boards for this work are only 6 layer boards and the power net area fill is on Layer 3 which may result in less associated connection inductance. Additionally, the test boards in this work contain conductors on the top layer that directly connect the GND pad of the IC to the GND of the decoupling capacitor and the VD pad of the IC to the decoupling capacitor. These conductors allow for a slotline mode to propagate, adding another connection path in parallel. These top layer conductors were removed in simulation and found to only decrease the input impedance by a few ohms compared to the case where the capacitor SMT pads are only connected with vias.

The decoupling capacitors also result in the resonant frequencies being shifted to slightly higher frequencies. This result can be explained with perturbation theory [4]. Resonances occurs when the stored magnetic energy and stored electric energy are equal. Slightly altering the system such as adding a capacitor may change the stored electric or

magnetic energy, causing the resonant frequency to shift. Perturbation theory assumes that these small changes do not significantly alter the original fields. For a small perturbation, the fractional change in resonant frequency is equal to [4]:

$$\frac{\omega - \omega_0}{\omega_0} = \frac{\Delta W_m - \Delta W_e}{W_m + W_e} \tag{4.3}$$

An increase in the stored magnetic energy or a decrease in the stored electric energy will result in a positive shift of the resonant frequency. In the GHz range, the impedance of SMT capacitors will be primarily inductive. It is then expected that the addition of the capacitors will increase the stored magnetic energy of the system. Increasing the stored magnetic energy will result in a positive shift of the resonant frequencies that is seen in the measurements.

The addition of resistors in series with the capacitors further reduces the impedance by introducing additional loss that provides greater dampening of the cavity resonances. Examining the real input impedance at a frequency away from a resonance frequency will give the baseline resistive loss due to dielectric, conductor, and SMT component losses. For instance, at 4.5 GHz the resistance is 0.43 ohms for the case with no SMT components, 0.53 ohms for the case with decoupling capacitors only, and 0.72 ohms for the case with decoupling capacitors and series resistors. The use of series resistors is clearly effective at adding additional loss and dampening the resonances. As discussed earlier, the on-die capacitance will dominate the impedance seen by on-die devices at higher frequencies so increasing the PCB impedance does not affect the power integrity. Digital ICs or other devices with signal bandwidth at lower frequencies (kHz-MHz) require a very small PCB impedance at lower frequencies for power integrity considerations. For these devices, the addition of the series resistors may increase the PCB impedance too much to be acceptable.

4.4. POWER TRANSFER FROM IC TO PCB PDN

Power transfer can be understood using transmission line theory. The source or generator can be modeled with a Thevenin equivalent circuit that contains a voltage source in series with an impedance. The source is connected to a transmission line or network with a certain input impedance. Circuit theory can be applied at the connection between the source and network to obtain an equation for the power delivered [4].

$$P_{abs} = \frac{1}{2}|V_g|^2 \frac{Re(Z_{in})}{|Z_g + Z_{in}|^2} \tag{4.4}$$

In (4.4), Z_{in} is the input impedance to the network and Z_g is the impedance of the source. The numerator only depends on the real part of the input impedance. The denominator depends on the square of the magnitude of the two complex impedances added together. Examining the input impedances of both the IC and PCB together will illustrate how the power transfer varies. Figure 4.10 compares the real and imaginary parts of the input impedance for the IC and the PCB. The IC impedance is dominated by the inductive reactance with a small resistance. At frequencies where the cavity is not resonant, the resistance looking into the PCB is very small. At these frequencies, the impedances of both the IC and PCB will be dominated by inductive reactance. Because the magnitude of the reactance is much greater than the PCB input resistance, the denominator of (4.4) will be much larger than the numerator resulting in a small delivered power. At resonant frequencies, the real part of the PCB impedance is very large and the imaginary part of the PCB impedance decreases. The numerator is greatly increased from the increase in the real part of the PCB impedance and the denominator, although increased overall from the real part of the PCB impedance, is decreased relatively due to the decrease in the imaginary part of the PCB impedance resulting in a much higher delivered power. Maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance. In this case, the two reactances add to zero and the value of the denominator is minimized. The maximum

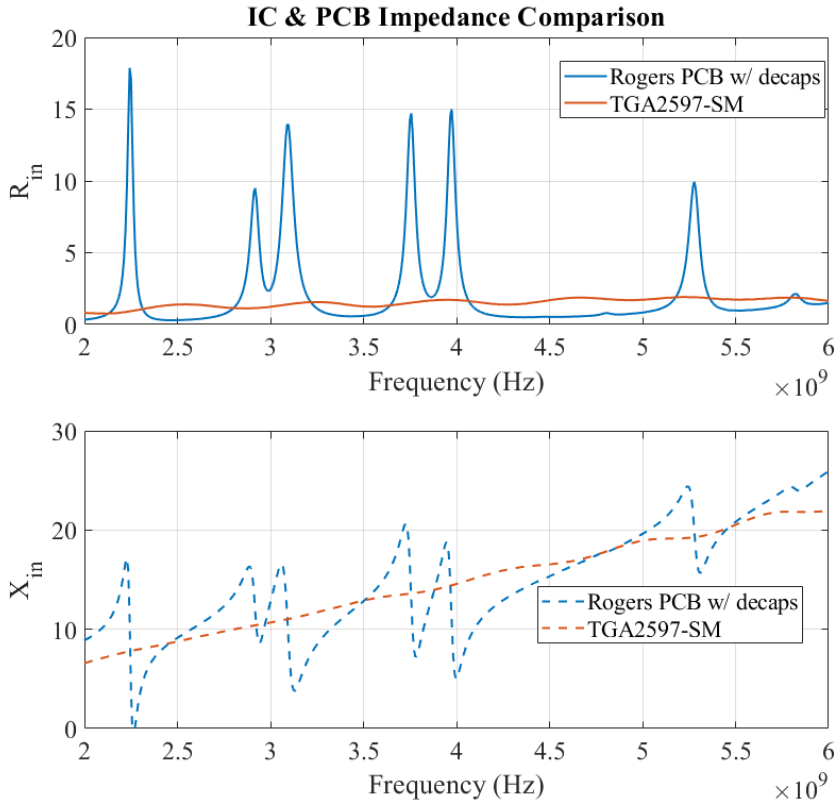

Figure 4.10. Comparison of the IC impedance and PCB impedance in complex form.

power that can be delivered is equal to:

$$P_{abs} = \frac{1}{2}|V_g|^2 \frac{1}{4Re(Z_g)} \tag{4.5}$$

The delivered power expressed as a percentage of the maximum power transfer (conjugate match) is plotted in Figure 4.11 for the case with decoupling capacitors, the case without decoupling capacitors, and the case with a series resistor with the capacitors. Very little power is delivered at frequencies where the PWR/GND cavity is not resonant. There is much greater power transfer at resonant frequencies due to the increase in the real part of the input impedance of the PCB. The decoupling capacitors are effective at decreasing the power transfer, especially for the first two resonant frequencies. The addition of the series resistor with the capacitor further decreases the power transfer. This decrease is due to a

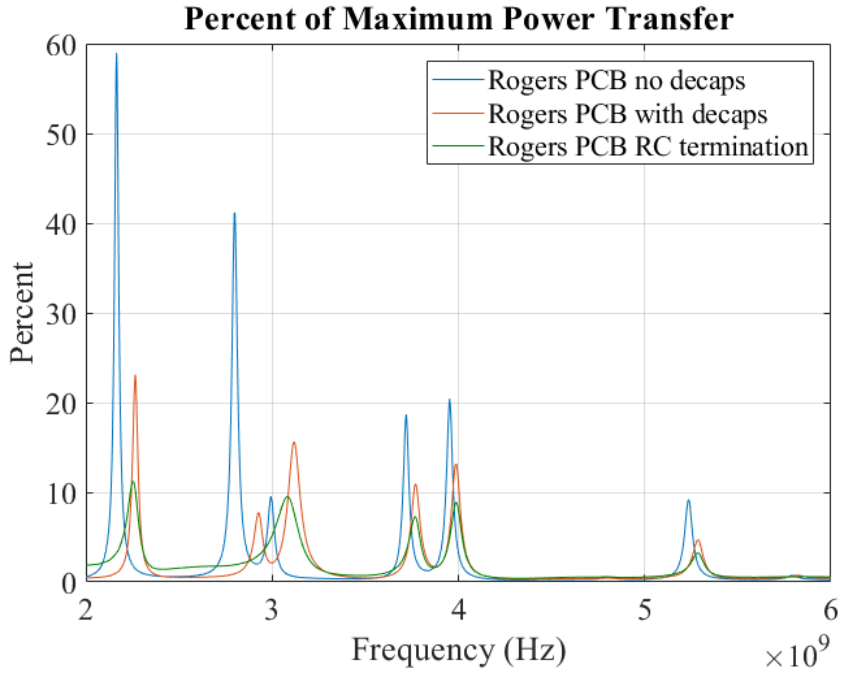

Figure 4.11. Power transfer between IC and PCB PDN expressed as percentage of the maximum power transfer possible.

decrease in the input resistance at resonant frequencies which is decreased by dampening the resonance. Because of the larger input resistance at non-resonant frequencies for the RC termination case, the power transfer is slightly increased at frequencies away from resonant frequencies. There is also a trend of the power transfer decreasing with increasing frequency. For instance, the input resistance is about the same at 2.8 GHz and 5.25 GHz, but the power transfer is lower at 5.25 GHz. This trend is because the inductive reactance of the IC and the PCB is increasing with frequency, resulting in a larger denominator in the power transfer equation.

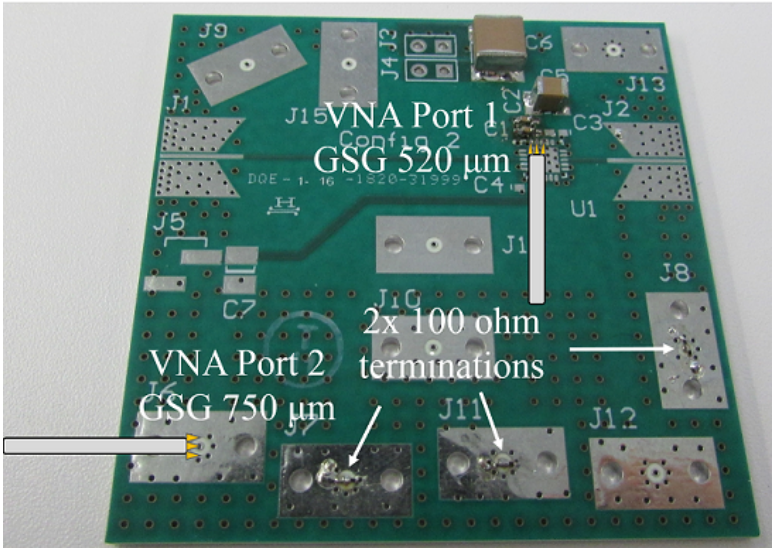

Figure 4.12. Measurement set-up for obtaining S-parameters between the IC location and victim interconnect with the measurement reference plane at the IC SMT pads.

4.5. COUPLING PREDICTION WITH S-PARAMETERS

In Section 3, measurements were made by exciting a via connected to the edge of the power net area fill. For the test board with the IC installed, the IC is now the excitation and it is at a different location than the via used in the previous measurements. As discussed previously, the location of the excitation will determine how strongly each mode is excited. Consequently, measurements are needed with the excitation port placed where the IC is to be installed to obtain S_{21} for the coupling prediction. The set-up for this measurement is shown in Figure 4.12. GSG probes are used to perform this measurement. Unfortunately, two different pitch sizes were required: 520 μm for the IC SMT pads and 750 μm for the coaxial pad of the victim signals. A SOLT calibration was performed using a Picoprobe CS-10 calibration substrate. Because the S_{11} looking into the PCB is important for the coupling prediction, the calibration coefficients were used for the 520 μm probe. The compression mount connectors with coaxial 50 ohm terminations obstruct the landing of the probes and are not used. Instead, two 0201 100 ohm resistors are used to terminate J7, J11, and J8.

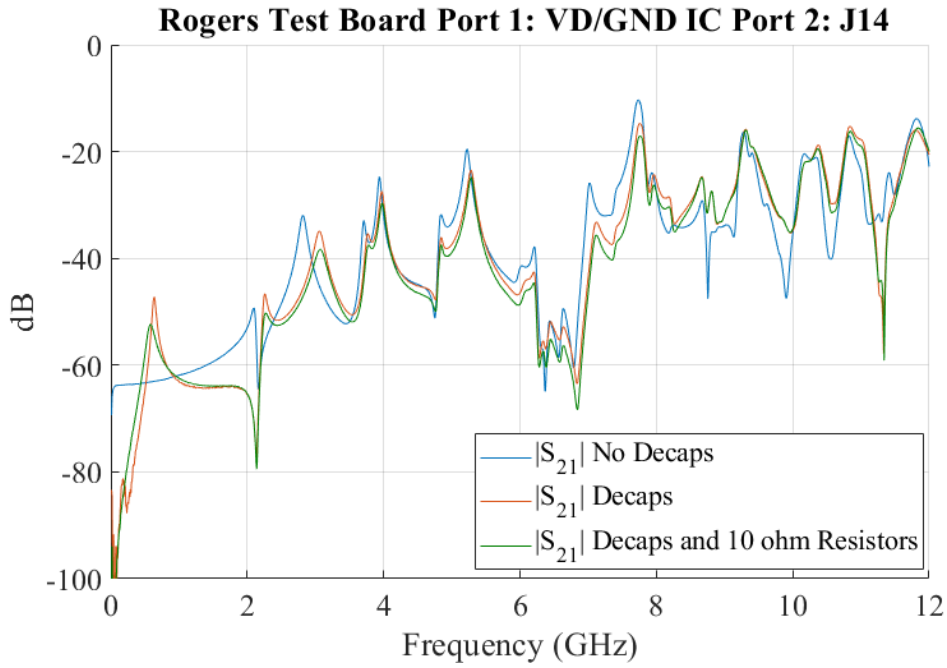

Figure 4.13. Measured $|S_{21}|$ comparison with and without passive components for port 1 excitation at IC PCB pads.

Measurements were performed with no decoupling capacitors installed, with decoupling capacitors installed, and with decoupling capacitors and series resistors. Figure 4.13 shows a plot of $|S_{21}|$ for J14, a victim via passing through the power net, for the three different cases. In general, the measured $|S_{21}|$ decreases by a couple dB with the addition of decoupling capacitors and further decreases by another couple dB when the series resistors are added. The peaks in the coupling are slightly shifted to higher frequencies with the addition of the capacitors. From 10 MHz to about 300 MHz the capacitors are very effective at decreasing the coupling. A new coupling maxima is created at about 600 MHz. This coupling maxima is the result of a resonance of the power net cavity capacitance and the inductance associated with current loop between the SMT capacitors and the IC. At frequencies greater than 8 GHz, there are some instances where the coupling is increased with the addition of SMT components. However, S_{21} cannot be used alone to predict the changes in the coupling. The power transfer between the IC and the PCB must also be taken into account. The change in

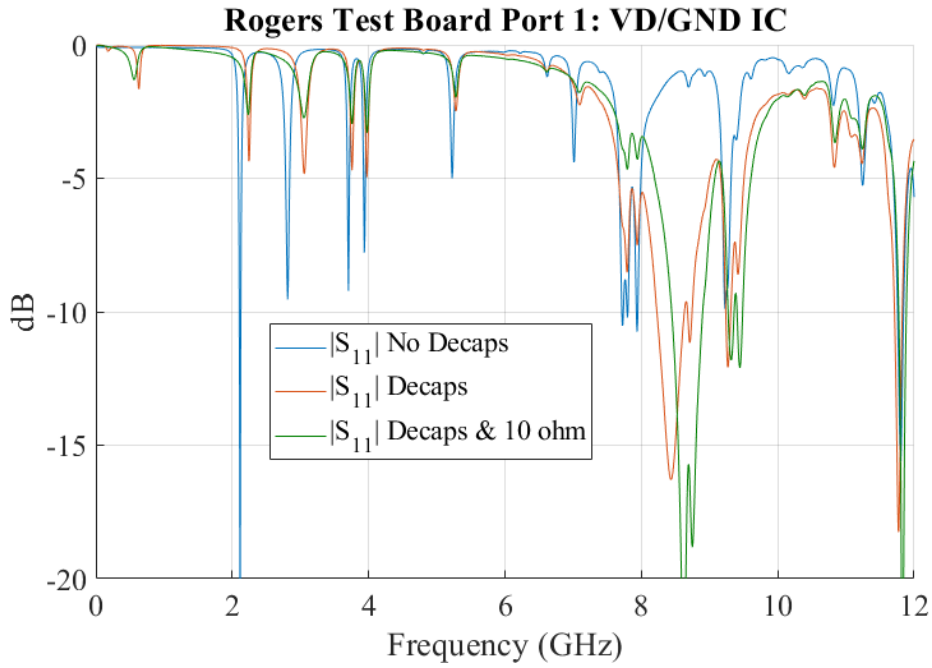

Figure 4.14. Measured $|S_{11}|$ comparison with and without passive components for port 1 excitation at IC PCB pads.

PCB input impedance will affect the power delivered to the PCB from the network analyzer. This functionality is captured with S_{11} and is plotted for the three cases in Figure 4.14. Less power is delivered as more SMT components and thus loss are added to the system. The same trend was evident when calculating power transfer from the IC source impedance in the last section.

In the Appendix, S-parameter measurements of the RFIN to VD coupling of the IC were obtained. The goal is to use these measurements with the measurements of the coupling between the VD/GND IC SMT pads and the victim signals to predict the coupling once the PA IC and PCB are integrated together. When dealing with S-parameters for networks that do not have ports matched to 50 ohms, the S_{21} for each stage cannot simply be multiplied together (or dB values added together) to determine the overall transfer function. The impedance mismatch between each stage needs to be considered which will create multiple feedback paths. S-parameter blocks can be used in many circuit simulators such as

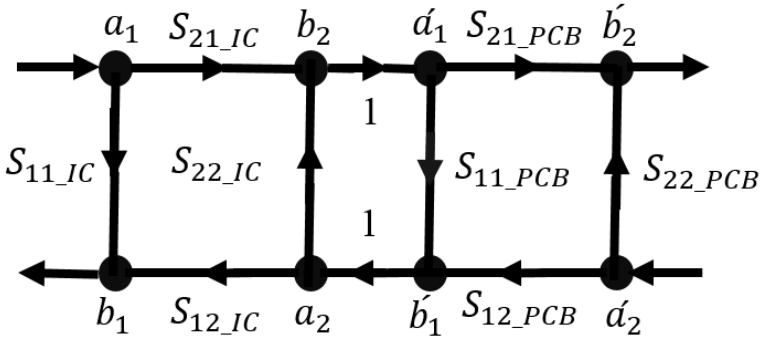

Figure 4.15. Signal flow graph of two cascaded two-port networks.

Keysight Advanced Design Studio (ADS) [53]. These simulators can cascade S-parameter blocks together and will calculate everything correctly without the user needing to know the necessary math. Before the proliferation of CAD software, network analysis was often performed with signal flow graphs. The use of the signal flow graphs can be still useful today to provide insight to a problem. Figure 4.15 shows the signal flow graph for two two-port networks cascaded. Mason's rule can be used to determine b_2'/a_1 or the overall transmission for the system. This rule is sometimes referred to the nontouching-loop rule [46]. The overall gain is (4.6).

$$\frac{b_2}{a_2} = \frac{S_{21IC}S_{21PCB}}{1 - S_{21IC}S_{21PCB}} \tag{4.6}$$

Figure 4.16 plots the linear magnitude of $1/(1S_{22IC}S_{11PCB})$ using the S-parameter data from the 1-port measurements of the IC and the PCB (with and without decoupling capacitors). This equation has the same functionality as the power transfer calculated with the impedances in Figure 4.11 and thus captures the power transfer between the two devices. The equation is greater than one for much of the frequency range, but drops below one after 4 GHz. Overall, neglecting the $S_{22IC}S_{11PCB}$ term will lead to larger errors at resonant frequencies of the PCB cavity. The error will be smaller away from the resonant frequencies. If the IC and PCB were well matched to the 50 ohm reference impedance

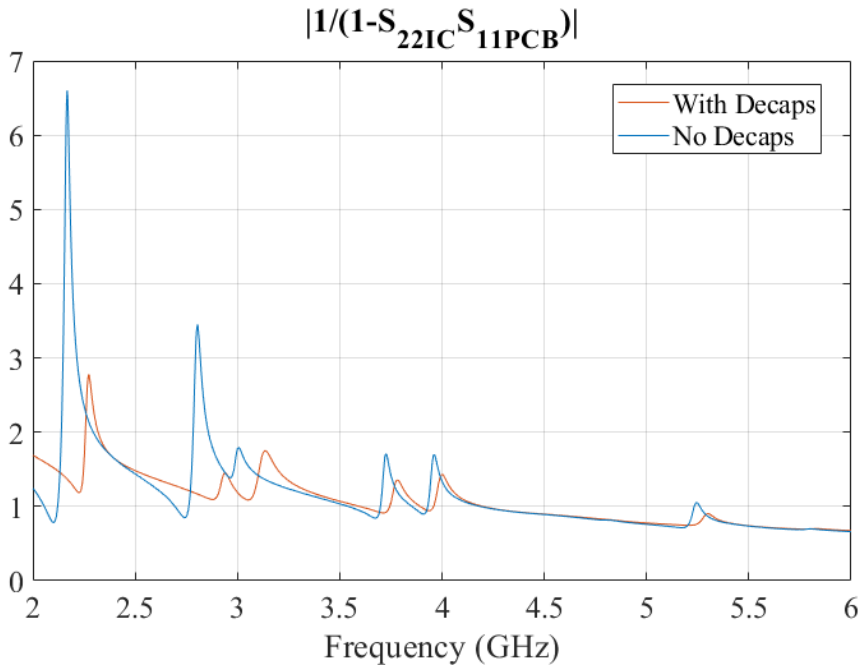

Figure 4.16. Magnitude plot of the S-parameter terms that capture the power transfer.

of the network analyzer, the $S_{22IC}S_{11PCB}$ term would be negligible. Figure 4.17 plots the calculated coupling using the expression, ADS, and multiplication of the S_{21} values of the two measurements. The signal flow graph expression and result from ADS are essentially the same, validating that the expression obtained from the signal flow graph is correct. It is important to note that for accurate reflection coefficient measurements the reference plane needs to be right at the terminals of the device under test. An electrical length between the measurement reference plane and the device under test will change the measured reflection coefficient. This requirement can make it difficult to obtain good reflection coefficient measurements. Use of microprobes with a calibration substrate allows the reference plane to be place at the end of the probe tips which can then be placed directly on the terminals of the device under test. However, for measurements with coaxial connectors the measurement reference plane is placed at the coaxial connectors of the VNA cable after calibration. 2-x Thru de-embedding patterns or TRL calibration patterns could be used to de-embed the

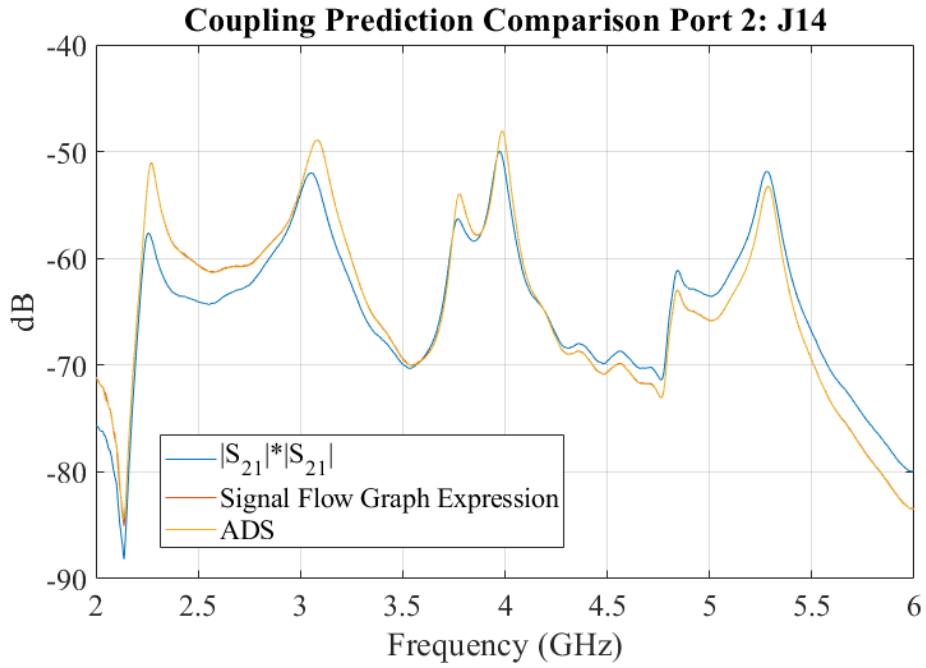

Figure 4.17. Comparison of the signal flow graph method and ADS for the coupling prediction.

measurement or shift the reference plane, but this require patterns be added to the design. Port extensions can be used to try to compensate for the phase shift to move the measurement reference plane, but uncertainty is involved which impacts the accuracy of the measurements. The measurements of the RF to VD coupling internal to the IC did not have the measurement reference plane moved to the terminals of the IC. To account for this, the S_{22} for the S-parameter block used in ADS was replaced with the S_{11} obtained from the GS probe measurement at the package terminals described in the Appendix.

To check the validity of the predicted coupling, network analyzer measurements were performed with port 1 connected to the input of the powered amplifier and port 2 connected to the various victims. Figure 4.18 shows the set-up for this measurement. These measurements are called the ”active coupling” measurement in this work. The output of an amplifier was connected to a power meter. Because the gain of the amplifier is not constant with varying power, a power level of 0 dBm was used for all measurements. The

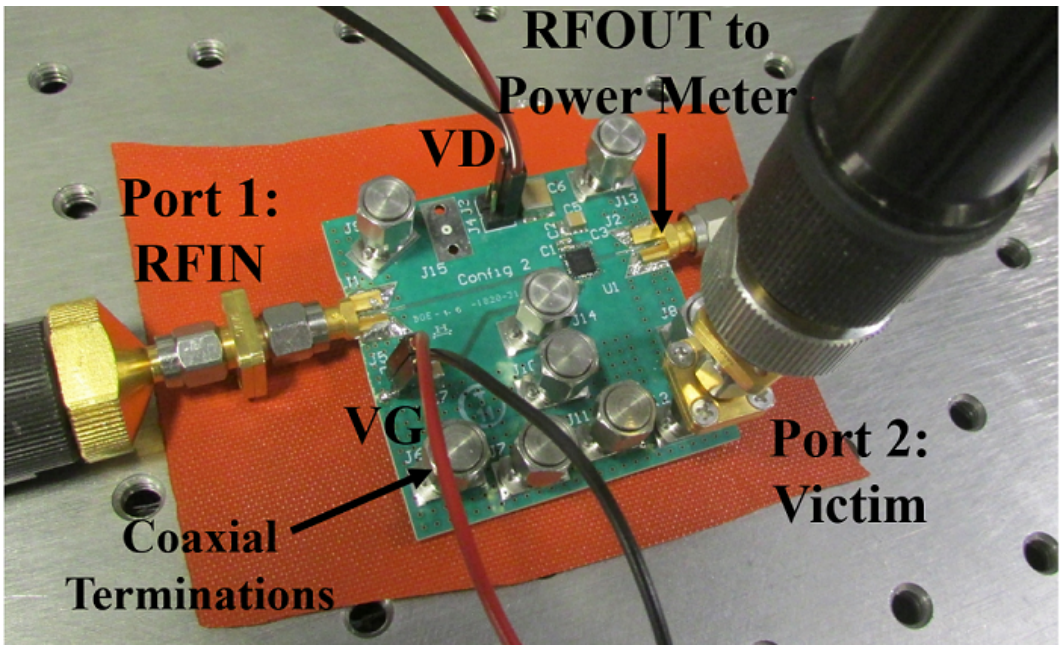

Figure 4.18. Active coupling measurement set-up.

amplifier's gate bias voltage was set such that the drain current was 40 mA with no RF power applied. These measurements were performed on PCBs with and without capacitors installed. Victims not being measured were terminated with 50 ohm coaxial terminations. For the validation, only the coupling due to noise injection through VD of the amplifier is desired. Although efforts were made to minimize the coupling between the victims and the RFIN/RFOUT, this coupling is non-negligible. It is especially difficult to have enough isolation between the victim and the RFOUT as it is 20 dB up from the input RF signal. As a result, at some frequencies the coupling from RFOUT or RFIN may dominate the total coupling measured at the victim. For brevity, only the results for J14, victim via in power net, and J13, victim stripline aperture coupled to the power net, will be considered.

Figure 4.19 and Figure 4.20 compare the active coupling (with decoupling capacitors), passive coupling from RFOUT scaled up by 20 dB, and passive coupling for RFIN for J14 and J13 respectively. The measurement set-up for these measurements was discussed in Section 3.11. The active coupling to J14 should be dominated by the amplifier VD noise

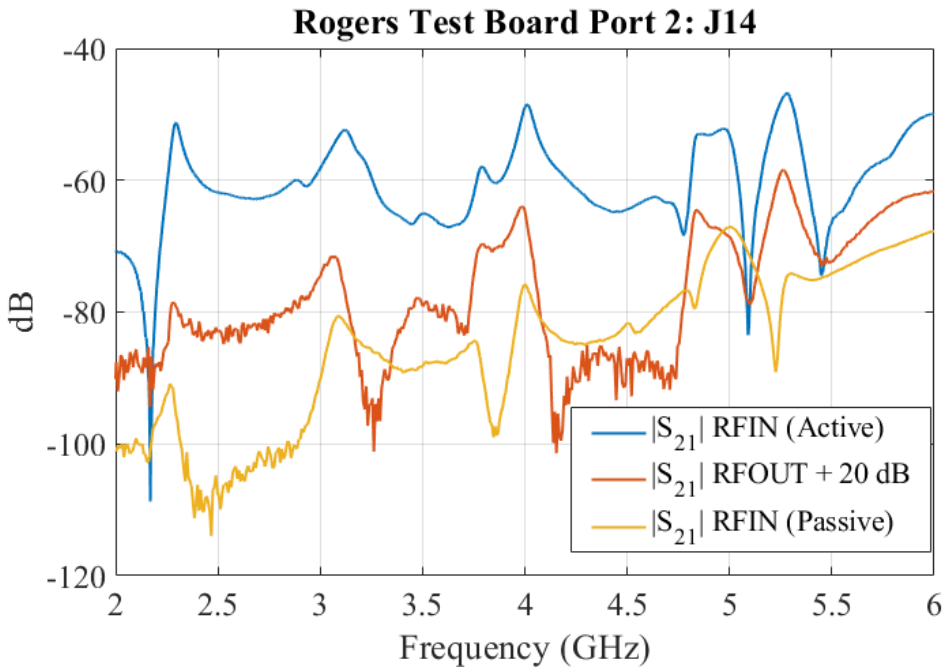

Figure 4.19. J14 active coupling comparison with RFIN and RFOUT coupling.

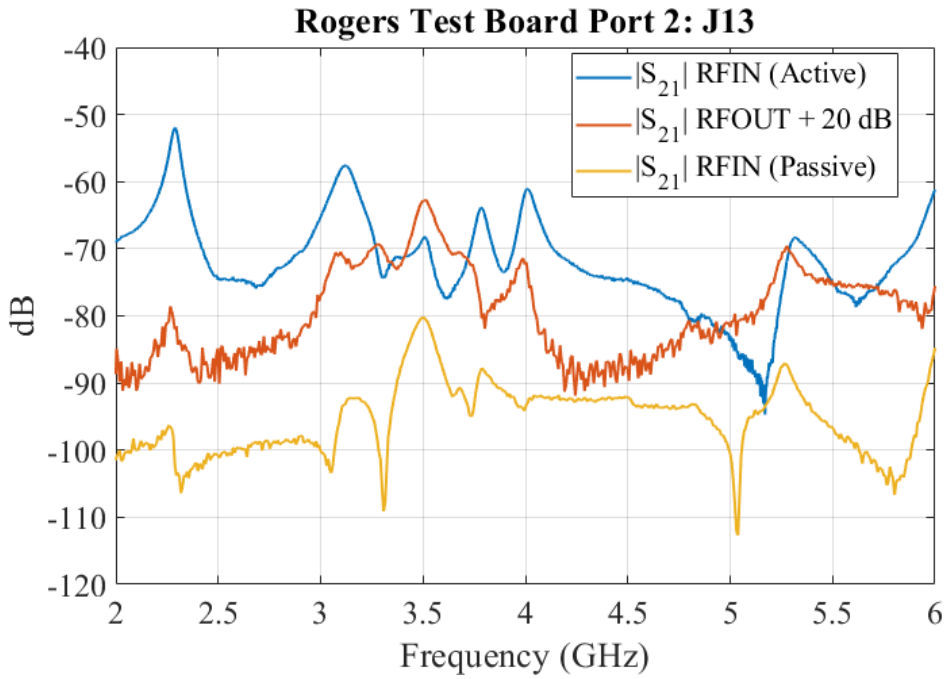

Figure 4.20. J13 active coupling comparison with RFIN and RFOUT coupling.

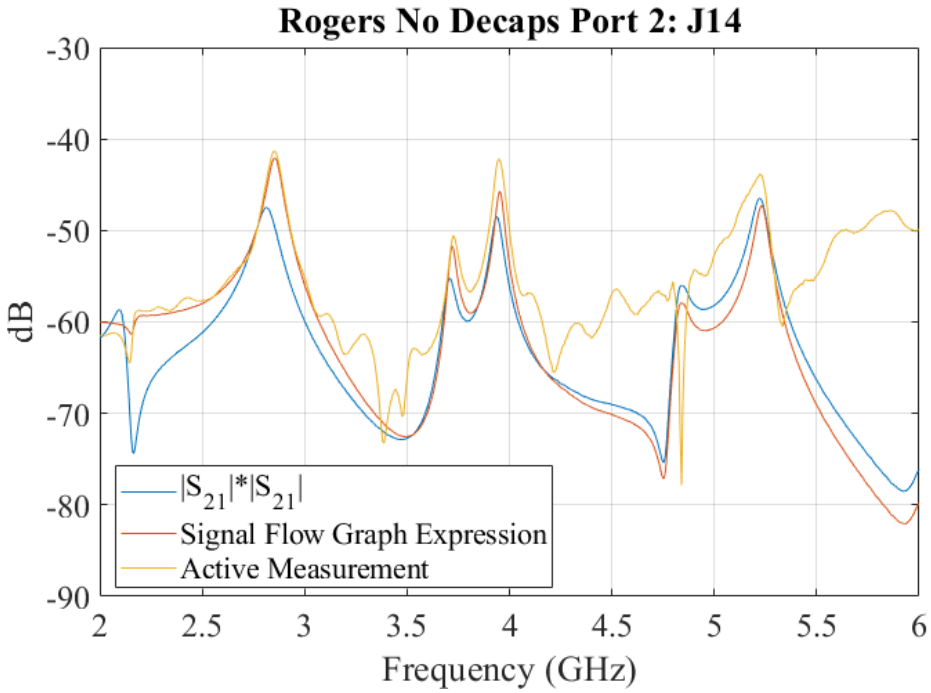

Figure 4.21. J14 active coupling measurement with no capacitors compared with prediction.

injection until about 4.7 GHz where the RFIN/RFOUT coupling may significantly affect the total coupling. The active coupling to J13 is lower than the coupling to J14. The coupling from RFOUT will impact the total coupling to J13 from 3-4 GHz and 4.7-6 GHz. However, the majority of the coupling peaks should not be greatly influenced by the RFOUT coupling. As a result of the minimal contributions of the RFIN/RFOUT coupling, the active coupling measurements for J14 and J13 can be used to validate the coupling prediction calculations.

Figures 4.21-4.24 plot the active coupling with the predicted coupling calculation for J13 and J14 for the cases with and without capacitors. The coupling calculation has a good match with measured active coupling at resonant frequencies, although the match is not as good away from the resonant frequencies. However, the coupling at resonant frequencies is of primary concern as the coupling is largest at these frequencies. The peaks in the active coupling are greater when capacitors are not installed as a result of the larger power transfer. The passive S_{21} measurement between the IC SMT pads and the victim

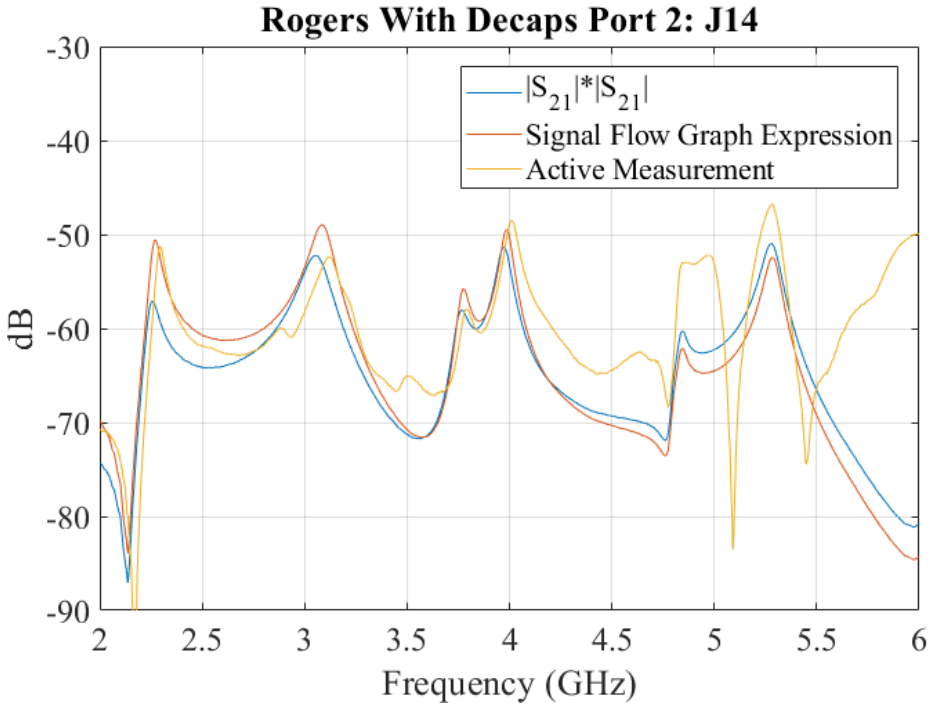

Figure 4.22. J14 active coupling measurement with capacitors compared with prediction.

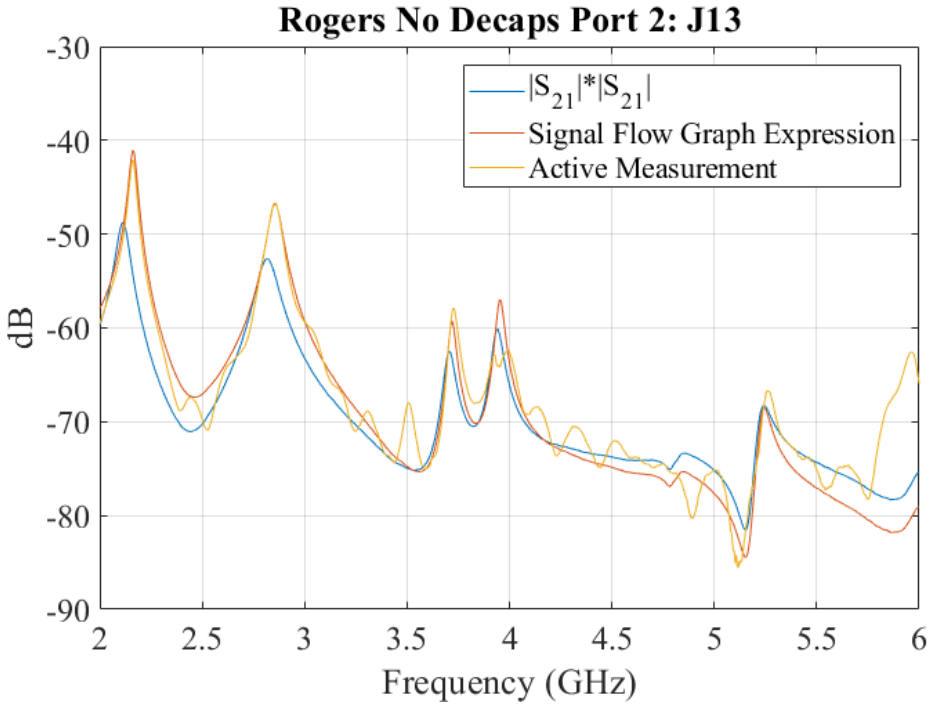

Figure 4.23. J13 active coupling measurement with no capacitors compared with prediction.

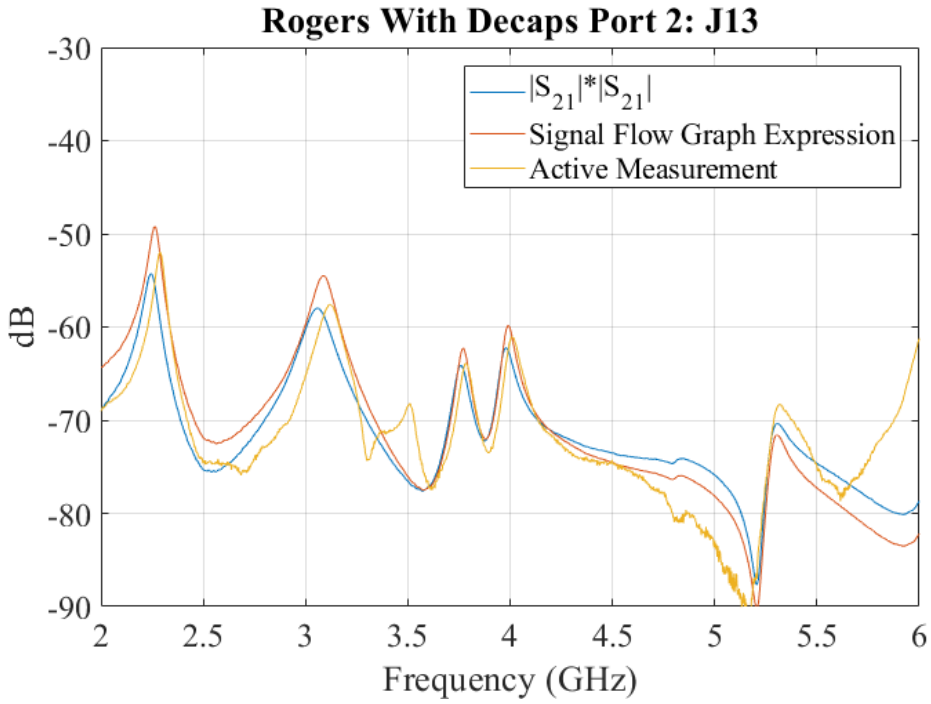

Figure 4.24. J13 active coupling measurement with capacitors compared with prediction.

signal does not capture the entire effect of the capacitors. Simply multiplying the S_{21} values underestimates the coupling at resonant frequencies where there is a large power transfer between the IC and the PCB. For instance, for the first resonant frequencies the S_{21} multiplication is off by around 6 dB for the case of no decoupling capacitors.

4.6. COUPLING PREDICTION WITH FULL-WAVE SIMULATION RESULTS

Results from full-wave EM simulation can be used to predict the coupling during the PCB design phase. One caveat is that the IC input impedance and noise transfer function is needed. For a narrowband device, it is more straightforward to obtain this transfer function compared to a digital device as it can be obtained from a network analyzer or function generator and spectrum analyzer. PCB design files can be imported directly into CST Studio and a variety of formats are supported [54]. Altium Designer is used for the PCB

design for this research which supports export to ODB++ format. The ODB++ format includes netlist, copper thickness, and dielectric thickness data making the model import an efficient process.

The addition of capacitors and resistors greatly impacted the power transfer, necessitating that these components be accounted for in the simulation model. It is not typically feasible to model the actual geometry of a multi-layered ceramic capacitors (MLCC) in simulation. MLCCs contain many ceramic and metal electrode layers to achieve very high capacitance values. Properly meshing these geometries would result in very small mesh cells, thus lowering the smallest time step and greatly increasing the overall simulation time. An alternative approach is to model the SMT components with lumped elements. Microwave CST allows for lumped elements to be added to the simulation. Series RLC and parallel RLC circuits are supported. The lumped elements can be defined between two points and are connected in series with a perfectly conducting (PEC) wire between the two points. Alternatively, a face lumped element can be defined between two edges and the lumped element is distributed through the edge. The face lumped element has a much smaller self-inductance as a result of the distributed connection [55]. A simple simulation model was created to determine how much inductance the PEC wire connection contributes. A short length of microstrip excited by a waveguide port is connected to a grounded rectangular post through a face lumped element or discrete wire lumped element. In the RLC model, R and L are set to 0 and C is set 1000 pF. The gap between the microstrip and rectangular post is 15 mils which is representative of 0402 SMT pads. The inductance is calculated from the impedance at 1 GHz using $L = |Z|/2\pi f$ from the results shown in Figure 4.25. Inductance is defined for complete current loops so the total inductance is associated with the contributions of the fixture current path and the lumped element current path. Use of the discrete edge connection increases the inductance by 800 pH, a larger value than the typical MLCC equivalent series inductance value of 500 pH provided by manufacturers. As a result, for obtaining the input impedance for noise coupling prediction

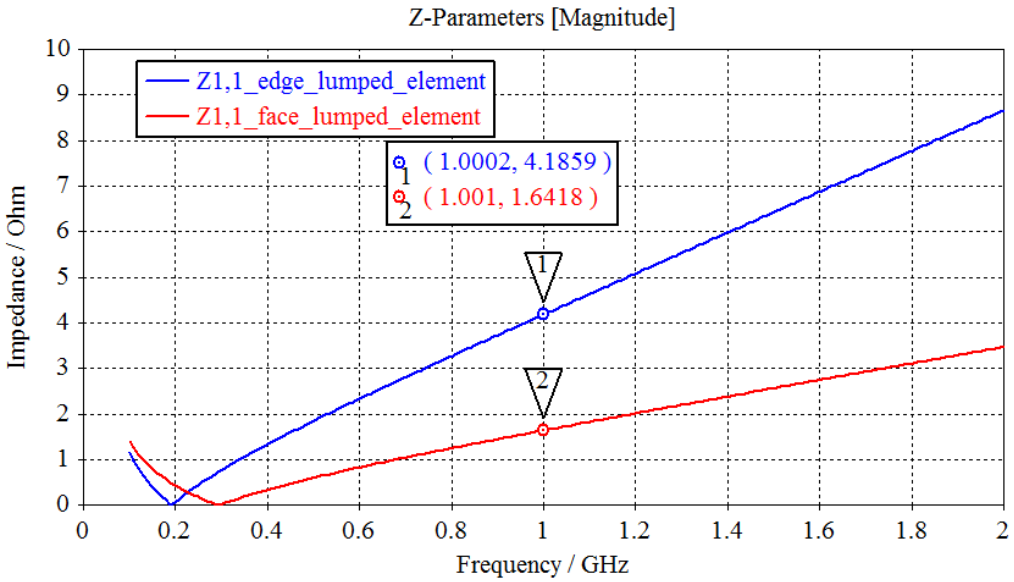

Figure 4.25. Impedance comparison of face lumped element and discrete wire lumped element.

a face connection should be used because the inductance is critical. A MLCC, because of its many metal layers, is a complex structure from an electromagnetics standpoint. A simple series RLC circuit model is typically only completely valid in the MHz range so transmission line equivalent circuit models have been developed with higher bandwidths [56]. However, the inductive behavior of a capacitor will dominate the impedance in the GHz frequency range. Even though it is not completely accurate, the first order RLC circuit model should be able to predict the general result of adding capacitors.

Simulated S-parameters are obtained from the model both with lumped element models for the capacitors and without. These S-parameters will be used in conjunction with the IC measurements to predict the noise coupling. For the 0402 packages a 500 pH value is used for the ESL and for the 1210 packages a 1000 pH values is used. These values are based on those provided by manufacturers [57]. Face lumped elements are used to minimize the inductance associated with the lumped element connection. Constant tan δ models are used for the dielectric permittivity. Moderate mesh density is used which results in a size of about

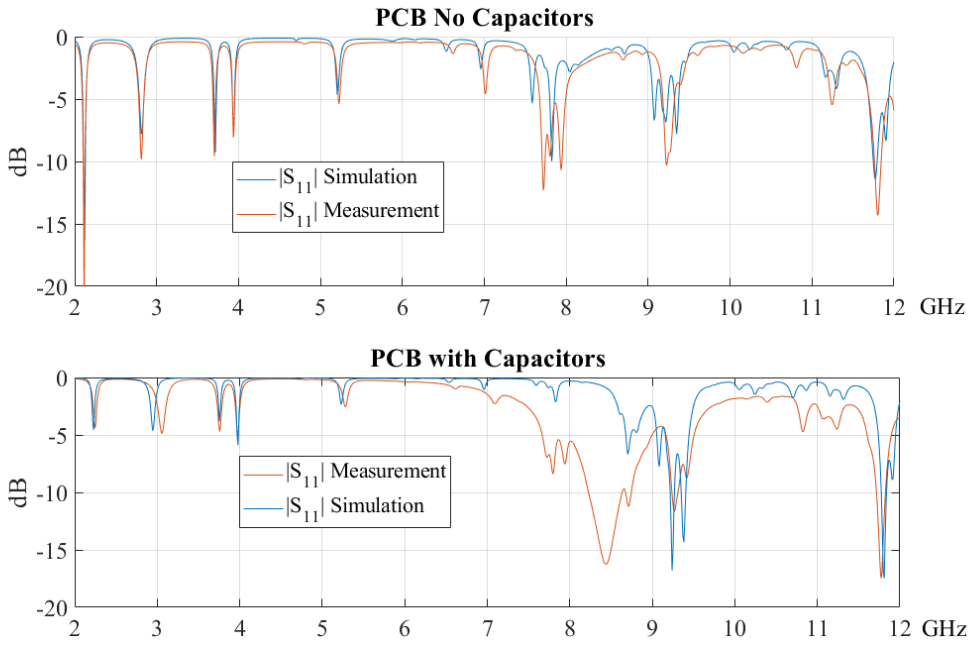

Figure 4.26. $|S_{11}|$ comparison of measurement and simulation results for Rogers test PCB.

2 million mesh cells. The numerous vias throughout the design increase the amount of mesh cells needed. The simulation time is 1 hour and 30 minutes for -60 dB accuracy running on a 2x Intel Xeon 128 GB RAM workstation with GPU (GP100) acceleration enabled. The relatively long simulation time, compared to models with comparable number of mesh cells and smallest mesh cell size, is due to the slow energy decay of the resonant structure in the time-domain. Figure 4.26 shows the $|S_{11}|$ comparison of the measurement and simulation results. For the case of the PCB only, the S-parameters obtained from simulation are in good agreement with the measured S-parameters. At higher frequencies, outside of the amplifier's frequency range, the agreement is not as good. The addition of the capacitor RLC lumped element models shifts the resonant frequencies and reduces the impedance at resonant frequencies, exhibiting the same trends as the measurement. However, the shift in frequency and impedance of the simulation results does not completely match the measured results. Furthermore, the simulation results match poorly to measurement from 7-9 GHz which is relevant if the device operated at a higher frequency range or for higher-order

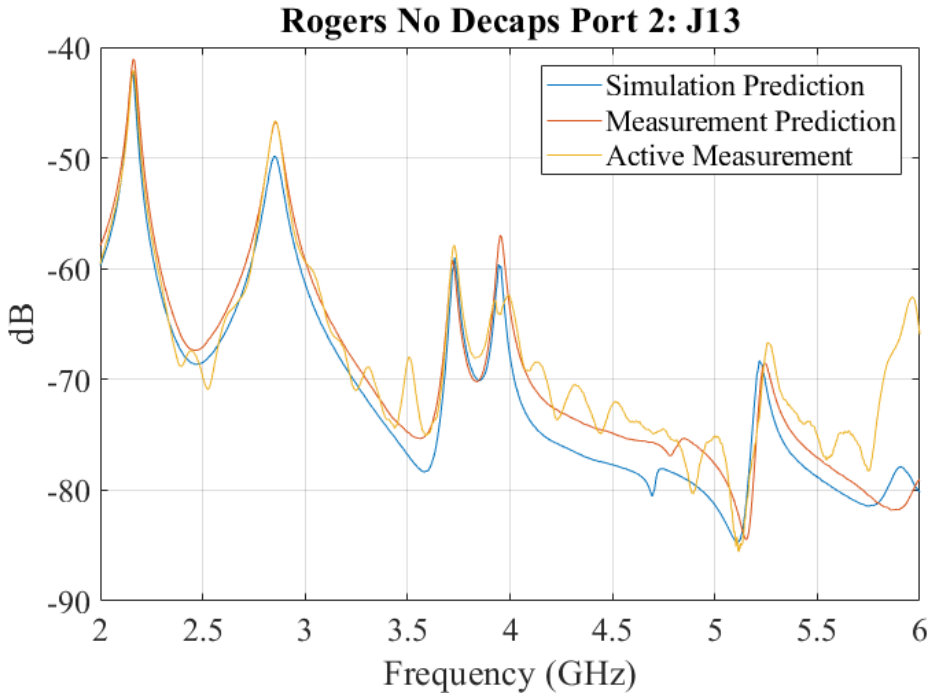

Figure 4.27. Comparison between measurement and coupling prediction from simulation results for PCB with no capacitors.

harmonic coupling prediction. Still, the agreement is acceptable in the frequency range of the amplifier which is the portion needed for the fundamental harmonic noise coupling prediction. The 1st order RLC model is able to predict the general trends, but a more complex model is needed for higher frequencies (7 GHz and greater). The passive $|S_{21}|$ comparisons are not shown in a separate figures for brevity, but their agreement is captured in the simulation prediction figures.

The simulation results were used to predict the noise coupling to the victims and are compared to the active measurement and prediction from measurement. For brevity, only the coupling to J13, the aperture coupled stripline is shown. Figure 4.27 shows the comparison for the case with no capacitors and the agreement is good as expected from the agreement of the S-parameters. The simulation model without lumped elements is more straightforward and should have good agreement with the measurements. Still, there

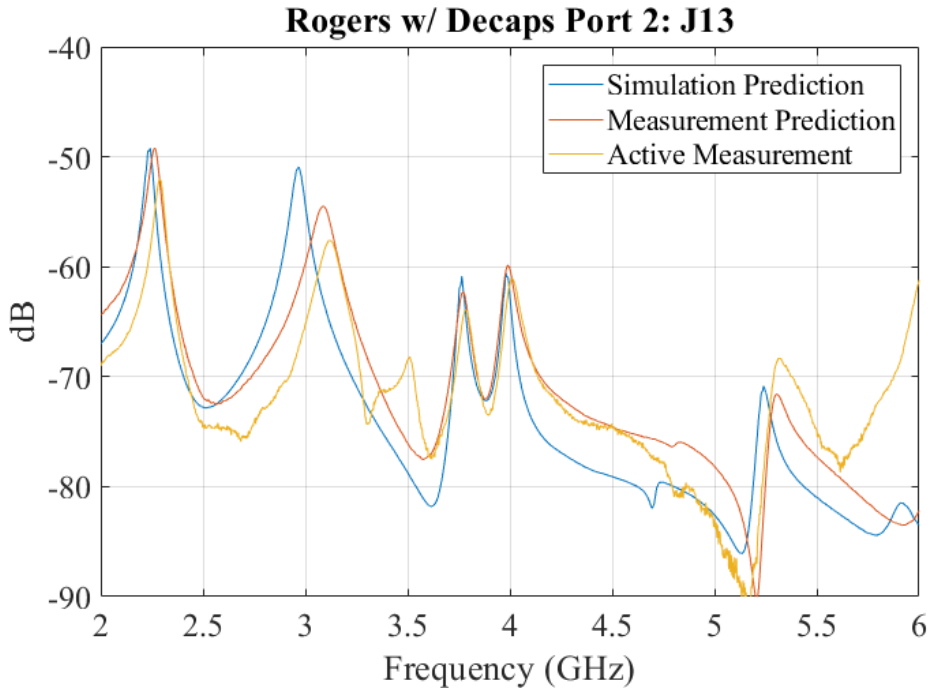

Figure 4.28. Comparison between measurement and coupling prediction from simulation results for PCB with capacitors.

are many ways the simulation model can go wrong, especially for a novice user, such as incorrect permittivity models, inadequate mesh density, and incorrect choice of boundary conditions. Figure 4.28 shows the comparison for the case with capacitors. The biggest discrepancy is the coupling maxima around 3 GHz where the simulation is off by 150 MHz and 6 dB. However, the general trend of a reduction in coupling due to the capacitors is captured in the simulation model. Small variations in the permittivity of a dielectric material can shift resonant frequencies and will exist due to manufacturing variance and even moisture content of the material. Also, a design may need to use a slightly different dielectric material if the original material is not currently available from the PCB vendor. Therefore, even if the prediction is off by over 100 MHz, a coupling maxima close to the

system frequency range should still warrant corrective action in case of shift of the material parameters. Overall, the agreement is not as good with lumped element models added, but is still reasonable and useful for pre-fabrication analysis.

4.7. EFFECT OF UNTERMINATED INTERCONNECTS

Another important consideration is how the terminations of the victim lines affect the coupling. Will having open transmission lines in the PCB, i.e. transmission line resonators, drastically change the coupling levels? It is cumbersome to add lumped elements to properly terminate each line in simulation. Further analysis is warranted to determine if these terminations can safely be omitted or are critical for accurate coupling prediction. Of course not terminating one side of a transmission line will change the signal measured on the other side of the transmission line. A termination will minimize reflections and standing-wave patterns on the transmission lines. This effect is obvious and will not be considered. One potential effect of the victim terminations is a change in the input impedance of the PCB. This change would affect the power delivery to the PCB. Resistive terminations will dissipate the power delivered to them and thus may lower the overall Q factor of the system. Figure 4.29 plots the measured input impedance with none of the victims terminated and with all of the victims terminated. For the first two resonances there is a larger decrease in the input impedance and a smaller decrease for the later resonances. This decrease can also be explained with network theory. Z-parameters are calculated with all ports aside from the excitation being open-circuited. In a system where other ports have loads, Z_{in} is no longer Z_{11}. Z_{in} for the simple case of a two-port network was given in (4.2) and shows the input impedance will decrease when the other ports are loaded. However, if Z_{12}, the transfer impedance, is small this decrease will be very small. Because the coupling to the victims, which is proportional to Z_{12}, is relatively small the subtraction term will be small. Active coupling measurements were initially made with all unused ports terminated in coaxial terminations. Measurements were repeated with unused ports left open. If the victim was

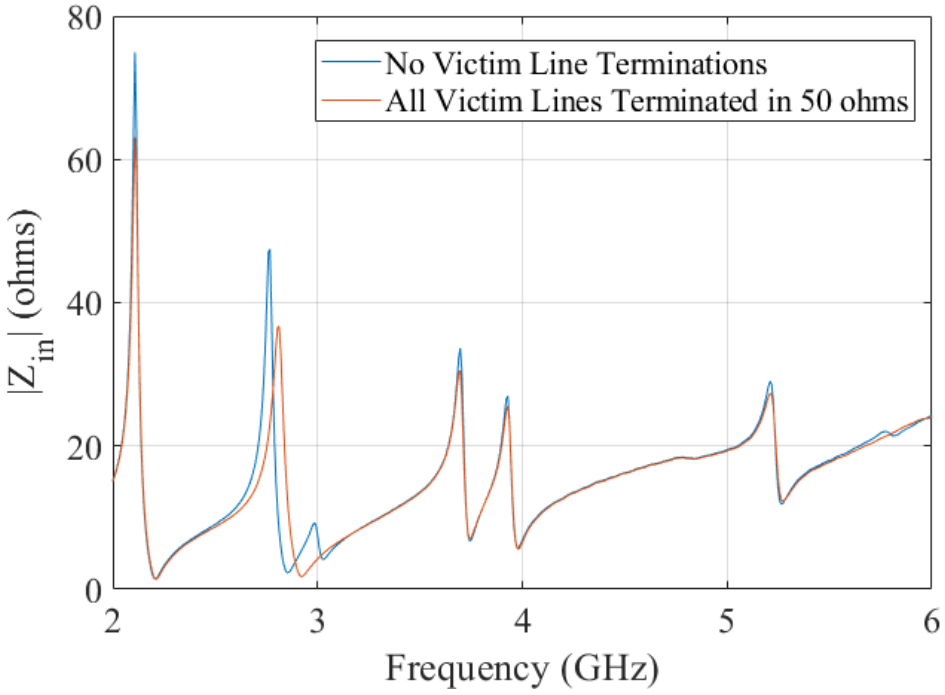

Figure 4.29. Change in the PCB PDN input impedance when all victim interconnects are terminated in 50 ohms.

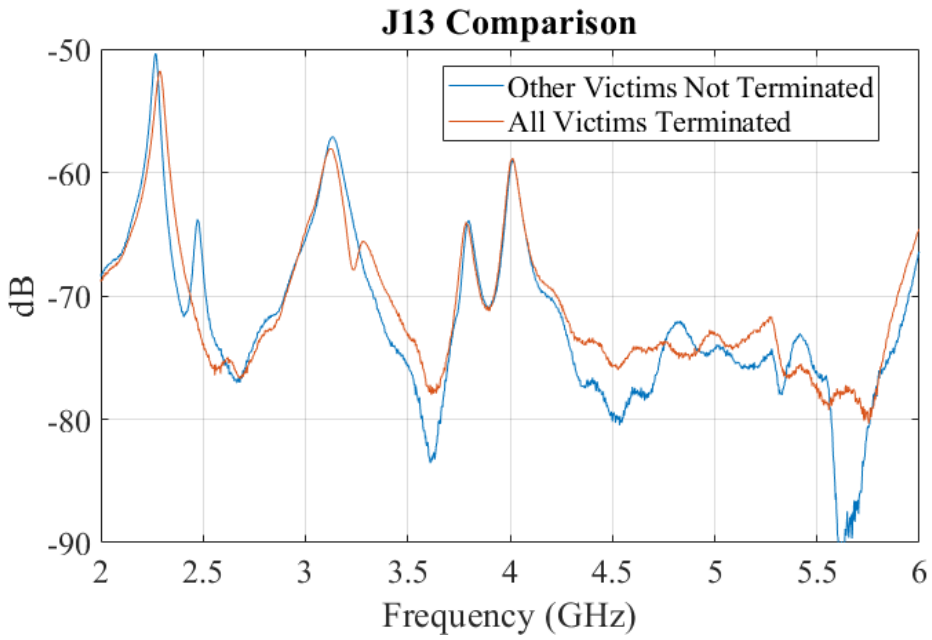

Figure 4.30. Active coupling to J13 measurement comparison with and without termination on other victim interconnects.

a stripline, the other side of the stripline was terminated. Figure 4.30 the comparison of the two cases for J13. The coupling is slightly increased for the first two resonances as expected from the increased input impedance with no victim terminations. There are small differences in the coupling, but overall the maxima in the coupling are consistent. Plots of comparisons for other victim signals were omitted for brevity, but show similar trends. Overall, for this test vehicle the termination of other victim lines does not significantly change the coupling to each victim. In this test vehicle, none of the victims are routed in closed proximity where they could be tightly coupled. Having victims that are tightly coupled together may make the victim terminations more impactful. The terminations do have a slight impact on the input impedance. Yet, the changes from the addition of SMT components were more significant. Proper modeling of the SMT component is a more significant factor coupling prediction than the victim terminations.

5. DESIGN RECOMMENDATIONS

5.1. OVERVIEW

In this section, design recommendations will be presented based on the findings in the previous sections. These recommendations are aimed at high performance mixed signal designs where high isolation is necessary between certain circuit blocks. The recommendations should in general be applicable to PWR/GND noise excited by wideband digital ICs and analog devices such as an amplifier. The first subsection will make recommendations for the power distribution network design. These recommendations are geared towards noise isolation/EMI considerations rather than power integrity considerations. The next subsection will make recommendations for suppressing the spread of parallel-plate noise throughout the rest of the design. The effectiveness of different strategies of via stitching and different stitching via spacing will be explored in this subsection. In the final subsection, recommendations for routing sensitive signals will be provided.

5.2. POWER DISTRIBUTION NETWORK DESIGN RECOMMENDATIONS

The main considerations for minimizing the parallel-plate noise related to the power distribution network include damping of the resonances, minimizing noise power transfer to the PWR/GND cavity, and preventing the spread of the parallel-plate noise throughout the rest of the design. The power distribution network and rest of the PCB can be designed to address these considerations. Dampening the resonances will decrease the field strengths at resonant frequencies and thus lower the coupling. To dampen the resonances, loss needs to be added to the system. The most desirable methods for dampening the resonances are those that do not add additional cost or require significant design effort.

5.2.1. Use of Higher-Loss Dielectric Material for PWR/GND Cavity. One straightforward way to do this is to use a higher-loss dielectric for the dielectric material that borders the power net area fill. According to the analytical expressions, the dielectric Q for a parallel plate cavity is inversely proportional to the loss tangent. A dielectric material with a higher loss tangent will have a lower Q. The measured results in this work showed a higher real input resistance and greater coupling for the test vehicle using Rogers material compared to the test vehicles with FR-4. The use of different dielectric materials is a common practice in PCB design as low-loss dielectric materials are much more expensive than standard higher-loss FR-4 material. Low-loss dielectric material such as Rogers RO4000 series and Panasonic Megtron 6 are compatible with standard FR-4 PCB fabrication processes. The power distribution network on the PCB only provides charge to supply the dynamic current draw in the MHz range and lower, so the dielectric loss at higher frequencies is inconsequential. If the bordering copper layer does not have RF signals or high-speed digital signals, the low dielectric loss has no functional benefit. It has been recently reported that many high-volume PCB vendors have the capabilities to manufacturer these stack-ups with both FR-4 and low-loss dielectric [58]. Overall, this recommendation does not take any significant effort to implement and should lower the cost of the PCB as well.

5.2.2. Use of Thin Dielectric Layer for PWR/GND Cavity. Another potential method for dampening the cavity resonances is to use thinner dielectric layers for the power distribution network. This method was first suggested and investigated in [59] and showed good suppression of plane resonances for 0.3 mil and 1.6 mil substrates. According to the analytical expressions for the conductor Q for a parallel plate cavity, the Q increases with increasing cavity thickness. This relationship is known in microstrip patch antenna design as very thin substrates are known to greatly decrease the radiation resistance, making them unsuitable for patch antenna design [60]. Using a very thin dielectric layer is more difficult to implement than use of higher loss dielectric. Often the dielectric thicknesses are set by a standard PCB stack-up. Still, there are relatively thin dielectric layers available for standard

FR-4 processes that should not add cost to the design, beyond the increased cost of using a custom stack-up rather than a standard stack-up. For instance, Isola glass style 106 pre-preg material (FR-4) has a thickness of 1.7 mils and should have a much lower Q than a 5-10 mil thick dielectric layer.

5.2.3. Use of Passive SMT Components. Other methods for dampening the resonances require the use of additional components or layout space that add cost. In [18], capacitors placed at an optimal location (by a modal peak) were shown to be effective at dampening the resonances in the 100s of MHz range. In Section 4.3, it was demonstrated that the addition of capacitors close by the excitation decreased the input impedance and thus lowered the power transfer. Adding resistors in series with the capacitors further decreased the input impedance and lowered the power transfer even more. Datasheets for many RF amplifiers advise to include these RC terminations likely with the purpose of minimizing feedback mechanisms that may make the amplifier instable. Overall, capacitors or RC terminations should be placed in as close proximity in possible to the IC PWR pin to help minimize the high frequency noise power transfer between the IC and the PWR/GND cavity. To increase the efficacy of these components at higher frequencies, these SMT components should be connected such that the associated connection inductance is minimized.

5.2.4. Elimination of Power Net Area Fill/Power Plane. Another potential solution when the aggressor is a high frequency narrowband device is not use power plane or power net area fill. This would eliminate the resonant cavity and thus the mechanism for the efficient coupling of PWR noise throughout a design. In Section 4, it was illustrated that the impedance of the PCB PDN does not significantly affect the power integrity in the GHz range as the on-die capacitance is the main source for charge delivery to on-die devices in that frequency range. A digital device will have dynamic current draw with spectral content in the kHz-MHz frequency range and the PCB PDN will have an impact on the power integrity. In some cases, the power net area fill or plane may be needed for routing considerations if the IC has multiple power pins. Also, the plane may be needed for DC

IR drop or thermal considerations. If these considerations are not needed, then it may be practical to eliminate the power net area fill. Traces on the outer layer could be used instead. There has also been some research to suggest elimination of the PWR/GND cavity may be possible for some digital applications as well. Researchers at Georgia Tech have proposed a new method called power transmission line signaling to eliminate the power planes and thus simultaneous switching noise for digital high-speed buffers [61].

5.2.5. Minimizing Cut-outs and Apertures Above and Below Power Net. It is also important to design the power distribution network to contain the parallel-plate noise and prevent its spread as much as possible. Electrically large gaps in the reference conductors that enclose the power net area fill will result in efficient coupling between the PWR/GND cavity and neighboring cavities. As a result, the amount of the cutouts and their size should be limited as much as possible. The routing of traces surrounded by GND area fill on the bordering layers to the power net area fill should be avoided as this creates many electrically large gaps. Another example of an electrically large aperture would be the anti-pads of multiple vias adding together to form a larger aperture. Ideally, the portion of the reference planes directly above the power net area fill should be mostly solid. In consumer electronics, this design recommendation is not reasonable. However, in high performance designs there is less of a cost and performance trade-off.

5.2.6. Optimal Location of IC on Power Net for Minimizing Noise Transfer. As discussed previously, the location of the source excitation, i.e. location of IC injecting power noise, will determine how strongly a certain cavity mode is excited. Many papers have suggested placement of the excitation or victim at locations in the cavity where a certain mode is not excited or is very weak [7],[37]. In an actual design, it is not likely very practical to select the location based on how strongly certain modes of concern are excited. However, many modes have nulls towards the middle of the cavity. Placing the IC

towards the middle of the PWR/GND cavity should then minimize the excitation of many of the modes. As a result, a good practice would be to locate the IC towards the center of the power net area fill.

5.2.7. Brief Review of More Complex PWR/GND Noise Suppression Methods. More exotic solutions such as Electromagnetic Bandgap (EBG) structures have also been proposed to suppress the parallel-plate noise [16]. These structures have implementation issues that were discussed in the introduction section and have not been adopted in industry. Dissipative edge terminations to absorb the waves at the edge of the cavity have also been proposed and showed effective damping of the resonances [62]. However, if a split plane is used the cavity edge might not be on the outside periphery of the PCB and there aren't standard processes for installing components on the edge of a PCB.

5.3. SUPPRESSION OF PARALLEL-PLATE NOISE IN GND CAVITIES

Parallel-plate noise from the PWR/GND cavity can couple to other cavities throughout a design. This noise needs to be suppressed to maintain high isolation between different functionalities in a PCB. To suppress the excitation of cavities formed between two GND conductors, stitching vias can be used throughout the design.

5.3.1. Use of Stitching Vias Throughout the Entire PCB. One strategy is to place stitching vias throughout the entire design for parallel-plate noise suppression. There is some guidance in the literature for the spacing needed between stitching vias. An EDN article suggested a rule of thumb of $\lambda/8$ because it is half the electrical length of $\lambda/4$ where a stub can begin to resonate [63]. In [50], Bogatin and Smith proposed $\lambda/6$ based on the analyzing the impedance of a cavity with a different via spacing in a 3D EM solver and selecting the spacing such that the resonances would be suppressed. These are good rules of thumb, but the analysis behind them wasn't directly targeted at achieving a certain amount of isolation. The test vehicles shown in Figure 5.1 were fabricated and measured to quantify the isolation provided by different global stitching via spacing. The test boards contain

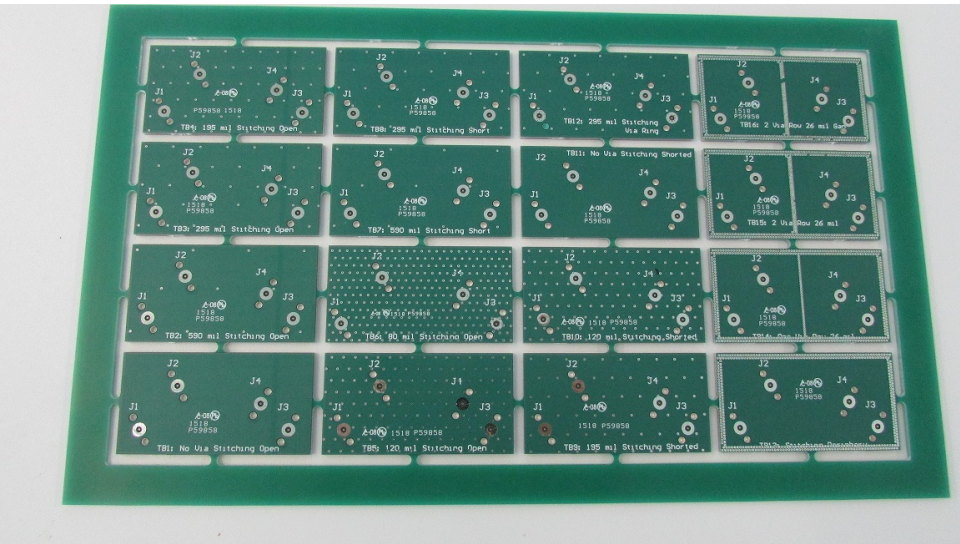

Figure 5.1. Picture of via stitching test vehicle which includes test boards for measuring isolation of global stitching, via fences, and via rings.

different stitching via spacing and include compression mount connectors to measure the coupling between vias. A 2-layer PCB stack-up is used with a dielectric thickness of 62 mils which is much larger than the typical 5-10 mil dielectric layer thickness of most PCBs. Still, the dielectric thickness is electrically small (less than $\lambda/10$) until about 10 GHz and only the fundamental TM_{z0} mode is propagating. Overall, the structure of the fields will be the same as a thinner cavity. Some of the test boards have the vias shorted to the bottom conductor so the impedance looking into the cavity can be measured. There are also a few test boards designed to assess the suppression provided by a row of vias.

Figure 5.2 plots the coupling between two vias in a parallel-plate cavity with different stitching via spacing. The electrical length of the via spacing was calculated at the frequency where the coupling reached approximately -80 dB. For the stitching spacings of 590 mil, 295 mil, and 195 mil the electrical length was roughly $\lambda/6$. This result agrees with the design rule suggested by [50]. But, for the 120 mil spacing the electrical length was larger at about $\lambda/4$. The 120 mil spacing test board has 145 stitching vias which is about 3 times the amount of stitching vias in the 195 mil spacing test board. There might not be a

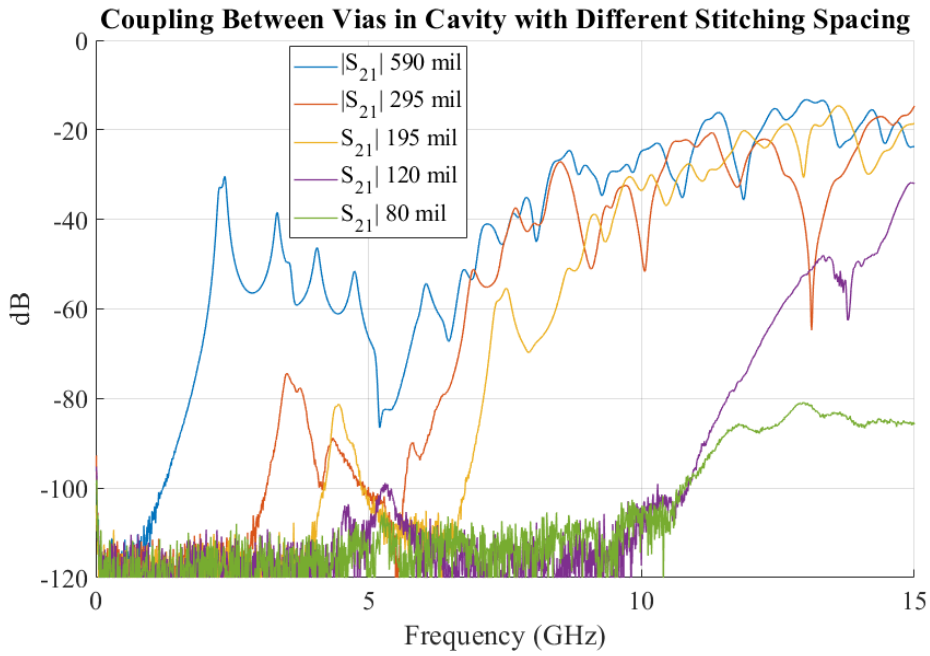

Figure 5.2. Comparison of the coupling between two vias in a cavity with different stitching via spacing.

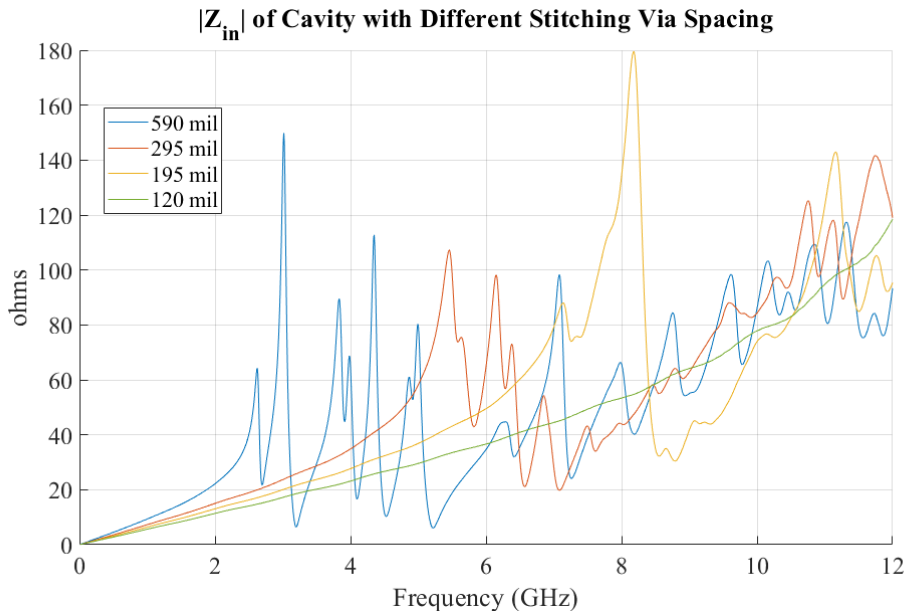

Figure 5.3. Comparison of the input impedance of a cavity with different stitching via spacing.

straightforward design rule when the cavity is loaded with many vias. More work is needed to come to a satisfactory conclusion. Still, the $\lambda/6$ appears to be a good spacing to target, although it may be conservative when the via stitching is dense. The impedance of the test boards with the signal via shorted to the bottom conductor was measured with a GSG probe calibrated to the probe tips. Figure 5.3 shows the input impedance looking into the cavity for different via stitching spacings. Comparison of Figure 5.2 and Figure 5.3 shows that the first coupling peaks occur before the cavity looks resonant from the impedance measurement of the shorted signal via test boards.

5.3.2. Use of Via Fence for Suppressing Parallel-Plate Noise between Two Regions. As a substitute or in addition to global stitching vias, rows of stitching vias can be used to provide isolation between two areas. In [64], design curves were provided with the amount of suppression obtained from a via fence based on the number of rows and set via spacing. Test vehicles were also fabricated to assess the isolation provided by rows of vias. In order to prevent coupling around the via fence, the periphery of the PCB was stitched with two rows of staggered vias. Stitching the periphery also greatly limits the radiation from the board and by reciprocity it also limits the external EMI that can couple into the planes [10]. Now, the boundary conditions on the periphery of the PCB are changed from open (approximated with PMC) to PEC. The change in boundary conditions will change the modal patterns in the cavity, but the cavity is still a resonator. In addition, there is no longer significant energy lost to radiation from that edge, so all that energy remains in the system potentially making the internal coupling greater. As shown in Figure 5.4, a single row of 20 mil diameter vias with 16 mil edge to edge hole spacing decreases the coupling by about 50 dB at lower frequencies and 40 dB at higher frequencies. These results show that tightly spaced via fences are very effective at suppressing the propagation of the parallel-plate noise within a cavity and providing high isolation. However, if gaps need to be added to the via fence for routing signals through the fence then the amount of suppression will decrease.

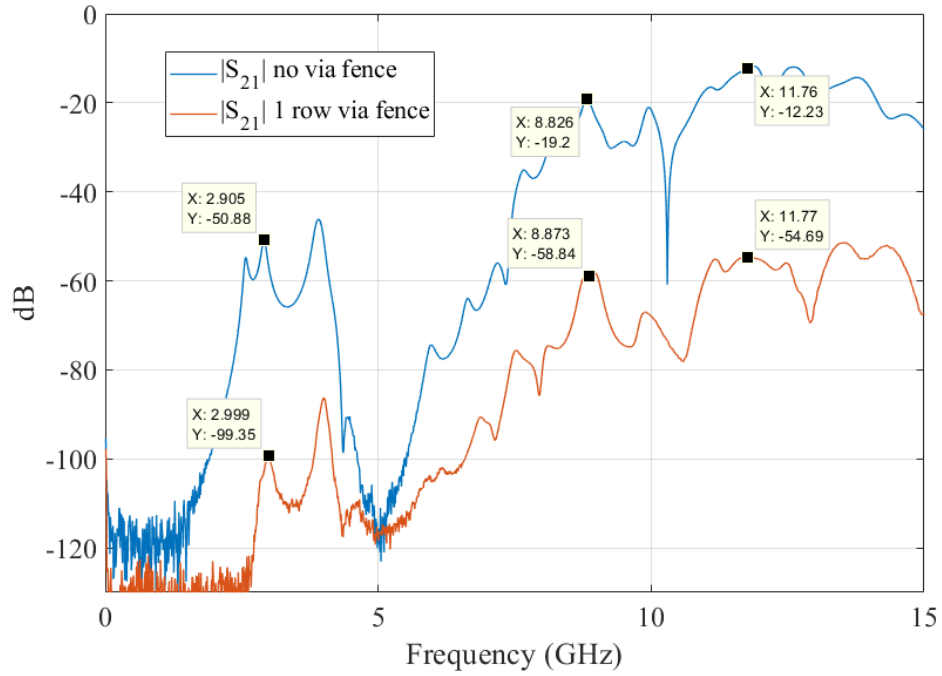

Figure 5.4. Comparison of the coupling between vias with and without a via fence.

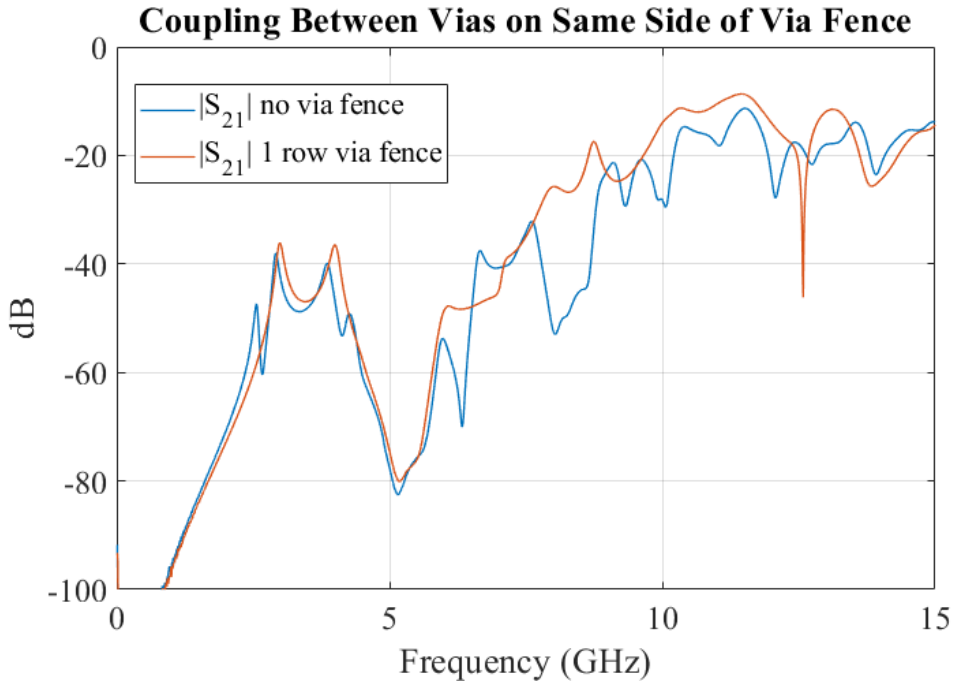

Figure 5.5. Comparison of the coupling between two vias on the same side of the via fence with and without a via fence.

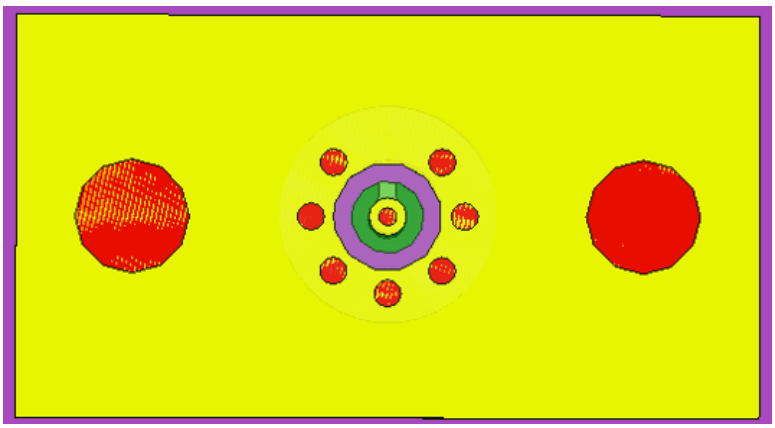

Figure 5.6. GND vias added around signal via to minimize coupling to the parallel plates.

It is important to note that the via fences do not improve the coupling between vias on the same side of the fence. The two vias on the same side of the via fence are still in a resonant cavity just one with new boundary conditions. Figure 5.5 shows that there is actually a slight increase in coupling between the two vias when the via fence is added.

5.3.3. Use of Via Ring Around Signal Via for Suppressing Parallel-Plate Noise Transfer. Another strategy is to selectively place stitching vias around signal via transitions such as in Figure 5.6. Sensitive signals or potential aggressor signals should have a well-controlled via transition by placing multiple GND vias around the signal via. This practice minimizes the coupling between the parallel-plate mode and the via which leads to much higher isolation. Placing a ring of stitching vias around a signal via is a standard practice in signal integrity test board design. Several papers have investigated different parameters associated with the use of GND vias around a signal via such as [26] and [65]. A variation of the 295 mil stitching test board was fabricated that included a ring of GND vias around the signal via. The measured coupling is compared in Figure 5.7 between the two cases. The use of the GND via ring improves the isolation by about 40 dB at higher frequencies, where the coupling is large for the case without the via ring.

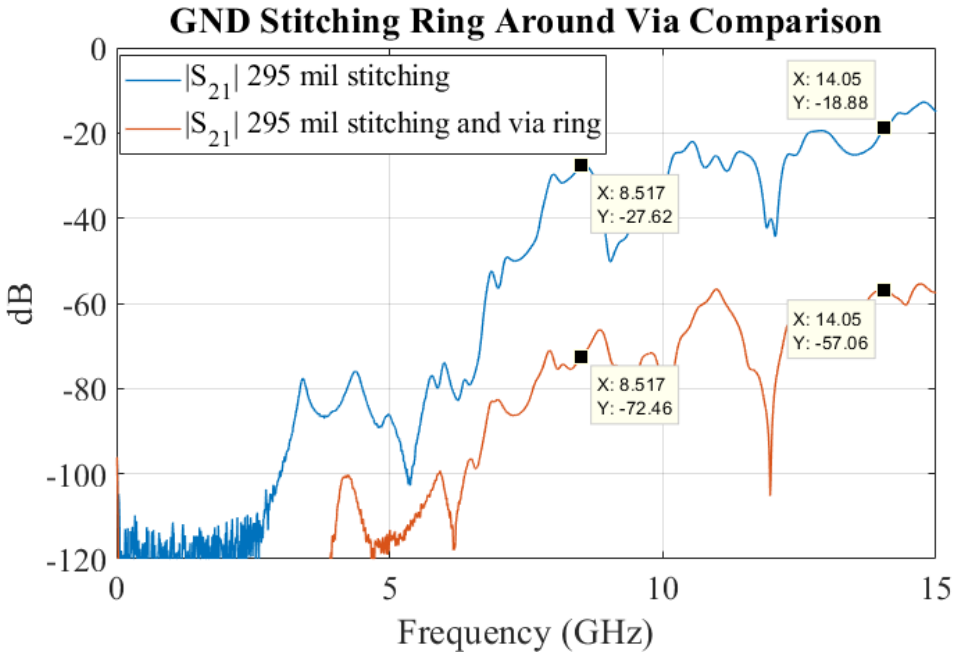

Figure 5.7. Coupling comparison with and without ring of GND vias around the signal via.

5.4. ROUTING OF SENSITIVE SIGNALS

Recommendations will be provided for routing sensitive signals to minimize parallel-plate noise coupling to various interconnects. Other traditional design practices such as not routing striplines or microstrips over gaps should still be followed.

5.4.1. Avoidance of Referencing Transmission Line to Power Net. Transmission lines carrying sensitive signals should not be referenced to a power layer or power net area fill. Although there is very little direct coupling between the stripline and the cavity, the coupling occurs at different discontinuities. In the case of split planes, the routing of the stripline over the gap between two area fills will result in large coupling. Alternatively, if the stripline is not routed over a gap a via is still required to transition to the stripline and the cavity can couple efficiently to the via. There is too much inductance associated with

capacitors to provide a low impedance return path across a gap at higher frequencies. SMT capacitors used in a design are only effective at keeping the impedance between PWR and GND low at lower frequencies.

5.4.2. Avoidance of Via Placement Through PWR/GND Cavity for Sensitive Nets. Vias for sensitive signal should not pass through or nearby a power plane cavity used by a circuit that has potential to inject significant noise into the system such as a power amplifier or digital IC. Resonances in a power cavity can not be completely mitigated in the GHz frequency range. The fields in the cavity at resonance can result in very high coupling to the via. Ideally, a via should only transition through as many layers as necessary. Advanced PCB fabrication techniques such as blind and buried vias and back-drilling can be used to limit the number of cavities the via passes through. These practices all add significant cost to the PCB fabrication and these additional costs need to be weighed against the performance benefits.

5.4.3. Differential Signaling Increased Robustness to Parallel-Plate Noise. Differential signaling can be used to minimize the coupling/mode conversion that occurs at discontinuities. For instance, a differential pair routed over a gap in the reference plane loses less energy to the slotline mode than a single-ended transmission line [66]. Also, differential signals couple less energy to the parallel-plate mode at a via transition than single-ended signals [24], [67]. These properties make differential signaling attractive as they are less susceptible to noise coupling. Still, the same noise coupling mechanisms that exist for single-ended signals can affect differential signals, they are just less severe.

APPENDIX

AMPLIFIER CHARACTERIZATION

TGA2597-SM OVERVIEW

The TGA2597-SM is a 2-6 GHz driver amplifier with a 32 dBm output power and is a commercially available part from Qorvo (Formerly a TriQuint part). The amplifier is a MMIC that uses GaN on SiC process. GaN is well suited for power amplifiers because of its much higher power density than GaS or silicon. The amplifier is packaged in a 4x4 mm plastic QFN package. There are two stages to the amplifier and the V_D and V_G nets for each stage are connected together in the packaging. The transistor used is a n-type depletion mode MESFET where the channel is fully formed with no gate voltage applied and a negative V_{GS} voltage is needed to pinchoff the channel for proper biasing. As a result, power on and power down voltage sequencing is needed to prevent damage to the amplifier. Qorvo also offers the unpackaged die (TGA2597) for this part and the datasheet includes an image of the MMIC shown in Figure A.1 [68]. The image of the MMIC allows for the topology of the amplifier to be identified. A schematic is created of the amplifier from the MMIC image and is shown in Figure A.2. The amplifier topology is a two-stage cascaded common-source amplifier. There are DC blocking capacitors at the input and output of the MMIC. There are input and output matching networks as well as a inter-stage matching network. Inductors between V_D/V_G and the FET's drain/gate are used as RF chokes to allow the DC bias to pass while greatly attenuating higher frequencies. V_D and V_G both contain on-die capacitors after the inductors.

The amplifier MMIC is analyzed to determine two important factors in the V_D power net to victim interconnect coupling. First, the isolation between the RFIN and V_D needs to be evaluated to determine how much noise will be injected into the PCB. The impedance

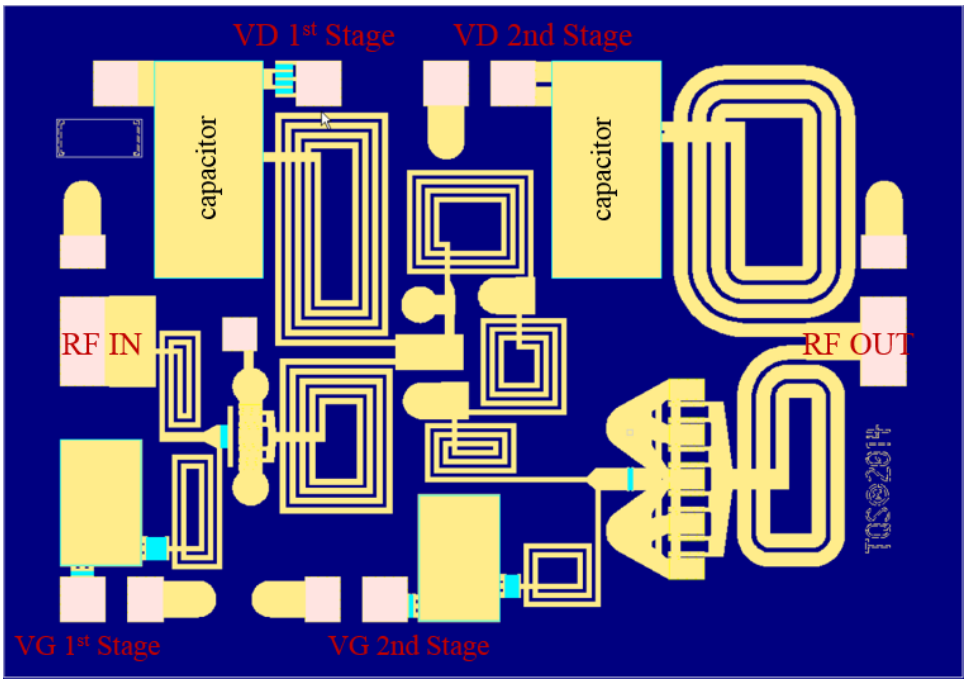

Figure A.1. Image of TGA2597 die with net labels added.

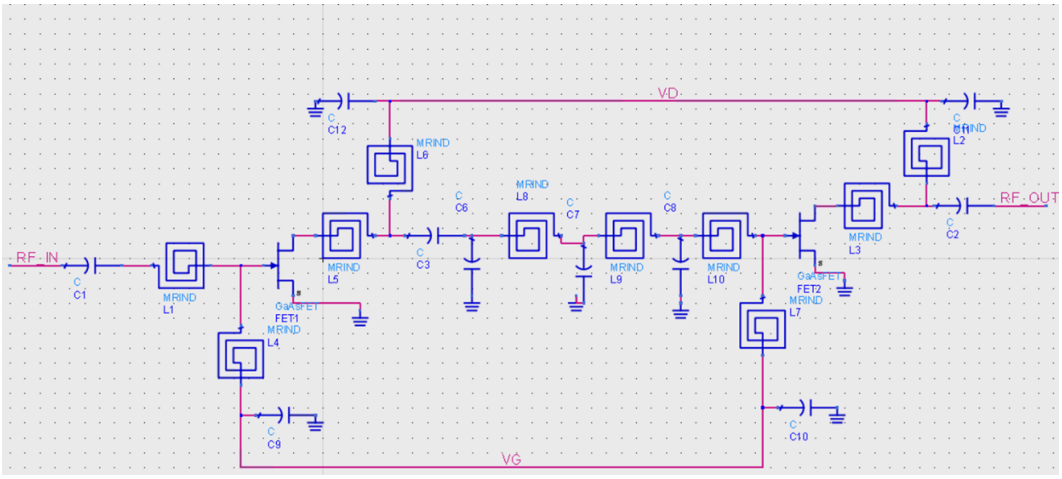

Figure A.2. Schematic of TGA2597 die.

looking into the IC will need to be known as well to determine the power transfer between the IC and the PCB. Secondly, it is important to know how the addition of the amplifier IC will shift the passive network parameters measured or obtained from simulation that does not include the amplifier IC. The measurement of the input impedance of the amplifier IC will be covered first.

INPUT IMPEDANCE OF THE VD PIN OF THE AMPLIFIER

Network parameter measurements are used as a transfer function to predict the coupling between V_D and the various victim interconnects. To determine the effect of the installation of the PA IC, the impedance looking in from the PCB into the PA IC needs to be determined. The 1-port reflect impedance measurement is suitable for obtaining the impedance looking into the amplifier's V_D net. The 1-port reflect method calculates the impedance from the reflection coefficient and has the greatest sensitivity when the DUT impedance is close to 50 ohms. The method has issues measuring very small or very large impedances. However, the frequency range of interest is 2-12 GHz (1st and 2nd harmonics of 2-6 GHz) where the wirebond and package inductance will dominate the impedance resulting in a impedance of at least several ohms. Figure A.3 shows the measurement set-up used to measure the impedance. Keysight PNA-X Network Analyzer, Model N5242A, was used for the measurement. A Picoprobe 450 μm GS probe (40A-GS-450-DP) is used for the measurement. Mini-Circuits ZFBT-6G-FT+ bias-tee is used to bias the amplifier and block DC to the VNA port. The reference plane for the measurement is moved to the end of the probe tips by performing a 1-port SOL calibration with the Picoprobe CS-11 calibration substrate. VG bias is provided by a DC positioner. The impedance was measured with three different gate bias voltages: -5 V (cut-off), -2.5 V (bias for nominal amplifier operation), and 0 V (channel completely formed). The measurement frequency range was 10 MHz to 6 GHz, the IFBW was set to 500 Hz, and the power was set to 0 dBm. Figure A.4 shows the measured impedance with V_G set to -5 V corresponding to a cutoff channel. The measured

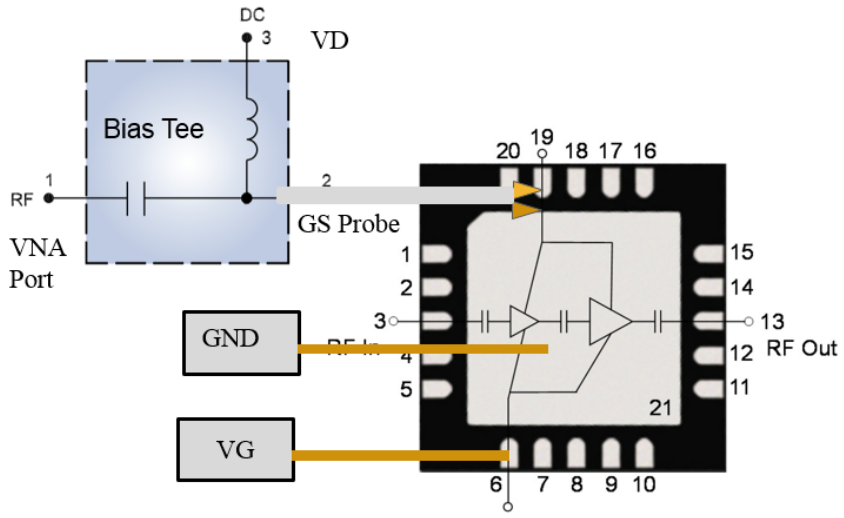

Figure A.3. Test set-up of 1-port reflect impedance measurement for IC.

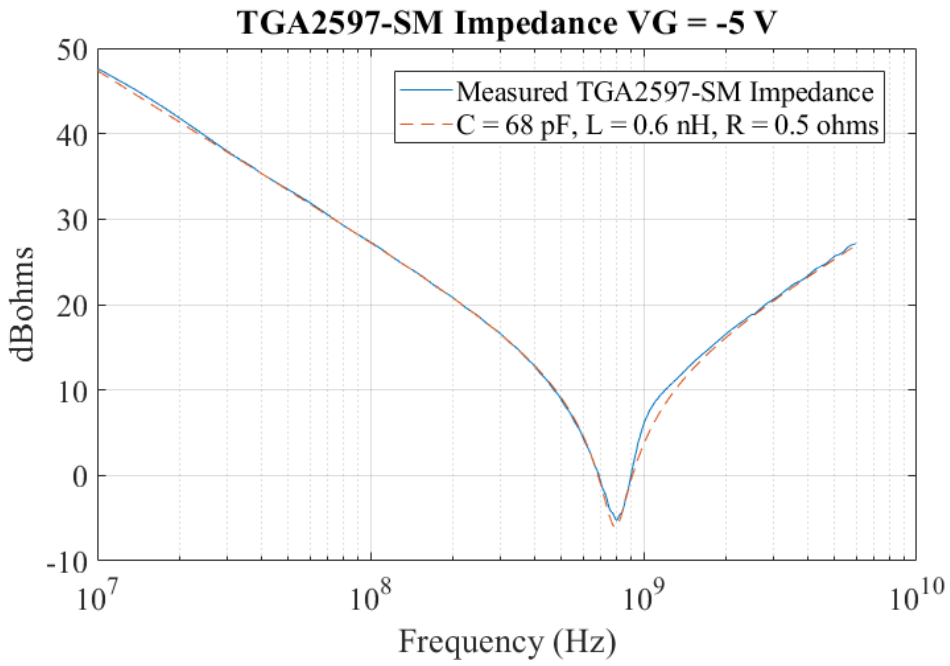

Figure A.4. Measured TGA2597-SM VD impedance plotted with equivalent RLC model.

impedance has the response of a series RLC circuit. At lower frequencies the impedance decreases by 20 dB/decade indicating the impedance is dominated by capacitance. In the GHz range, the impedance is increasing by 20 dB per decade indicating that the impedance is dominated by the inductance. Values for the capacitance and inductance are determined by data points in the linear regions. The resistance is determined by the impedance at the self-resonant frequency where the impedance of the capacitance and impedance of inductance are equal in magnitude and opposite in sign and thus cancel each other out. An inductance of 0.6 nH, a capacitance of 68 pF, and a resistance of 0.5 ohms are the extracted values from the measurement. The extracted lumped element model is plotted in the dashed red line and shows good agreement. For this measurement, the FETs are cutoff so the drain to source impedance is very high. Although, there is parasitic capacitance between the drain and source this is much smaller than the on-die capacitance as Pozar gives a typical value of 0.12 pF [4]. As a result, the capacitance looking in includes the two on-die capacitors at the V_D wirebond locations for each stage. The inductance is associated with the wirebonds and the package. The case where the gate voltage is zero is also considered and measured. Figure A.5 shows the measured impedance with different gate voltages. The measured impedance for the -2.5 V amplifier bias gate voltage is only slightly different than the -5 V cutoff case at lower frequencies. When no gate voltage is applied the channel is fully formed. For this case, the FET's drain to source impedance is lower than the impedance of the on-die capacitance. The V_G = 0 V case could be relevant if network parameters measurements are measured when the PA IC is installed on the PCB, but not powered on. However, in the GHz frequency range the inductance still dominates the impedance and the impedance is the same in this frequency range for all gate voltages. As a result, in the GHz frequency range the network parameters characterizing the PCB assembly can be measured without needing to power on the PA IC.

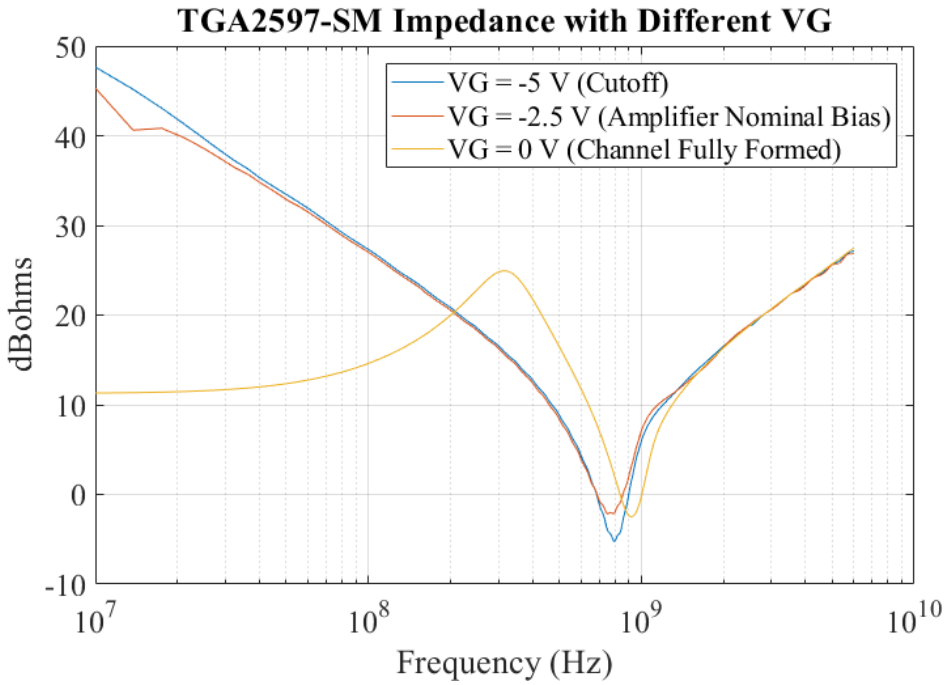

Figure A.5. Measured TGA2597-SM VD impedance with different gate voltages.

ISOLATION BETWEEN RF AND VD

The internal bias tee/RF choke greatly attenuates the RF signal before it reaches the V_D pin on the package. However, this attenuation does not necessarily make the RF signal negligible for noise coupling considerations. The isolation between the RF and V_D needs to be characterized to understand how much noise is injected into the power distribution network. The MMIC designer could use EM simulation or equivalent circuit model to quantify the performance of the bias tee section of the IC, but the consumer does not have access to the design files. The isolation provided by the internal bias tee is often not provided by the manufacturer. This is the case for the TGA2597-SM amplifier used on the test boards. A measurement method is needed to quantify the on-die and package isolation between the RF and V_D for commercial devices.

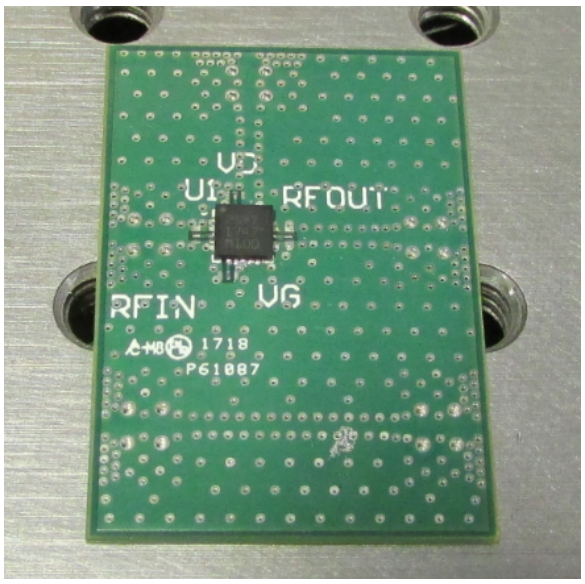

Figure A.6. PCB for RF to VD isolation measurement.

The performance of a bias tee is typically measured using a network analyzer. The insertion loss between the RF port and RF and DC port and the isolation between the RF port and the DC port are the typical measurements for assessing performance. Network analysis is applicable for linear devices, i.e. devices that do not produce additional harmonics. In this case, the bias tee is integrated on die with non-linear transistors and cannot be measured alone. Harmonics are produced because a transistor is a non-linear device. A network analyzer measurement can still be used, but it will ignore the higher order harmonics produced by the amplifier. A spectrum analyzer can be used to measure the higher order harmonics as well as the fundamental harmonic. An additional test board was designed for the measurement of the RF to V_D isolation and is shown in Figure A.6. It was difficult to probe the QFN package directly because three GS/SG probes were needed because the RFOUT also needs to be terminated for this measurement. With the probes and probe holders available, it was not possible to land all three probes. A 0201 50 ohm resistor could be soldered between the RFOUT and the QFN GND paddle to provide a termination, but it would not have adequate power rating. The additional test board was needed as a result of these difficulties. The test board is a 4 layer FR-4 PCB with a thickness of 31 mils.

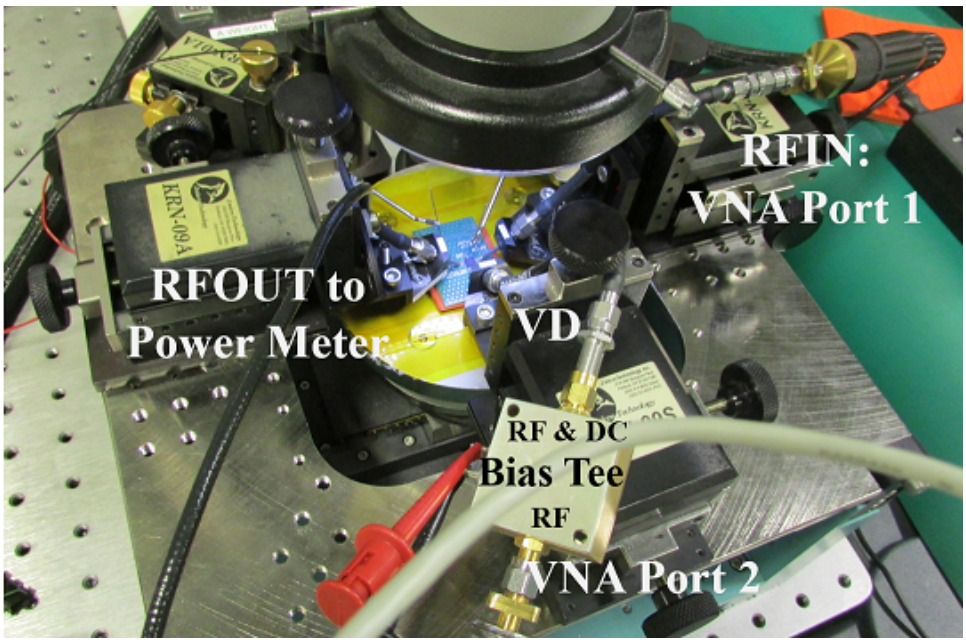

Figure A.7. Test set-up for RF to VD isolation measurement.

The two inner layers are solid reference (GND) planes. One side of the board contains SMT pads for the PA IC along with GSG pads for probing. The other side of the board contains SMT pads for the PA IC with CBCPW traces to edge launch SMA connectors. On this side of the board, a 2x-Thru is also available for loss normalization or de-embedding if needed. The 31 mil stack-up was chosen for the small 6 mil thickness of the top and bottom dielectrics. This thickness allowed for a small width signal trace for a 50 ohm characteristic impedance, which eliminated the need for a transition to a larger trace width from the IC SMT pads. Using this test board, both spectrum analyzer measurements and network analyzer measurements were performed. These measurements were performed with GSG probes and also with the end launch SMA connectors. The test set-up is shown in Figure A.7. Port 1 of the VNA is connected to the RFIN of the amplifier. Mini-Circuits ZFBT-6G-FT+ bias-tee is used to provide V_D bias to the amplifier and block DC to port 2 of the VNA. The RFOUT is terminated into a power meter to monitor the output power and a 20 dB attenuator is placed before the power meter so its max power limit is not exceeded. A DC positioner is used to provide the V_G bias to the amplifier. The bias tee upper frequency

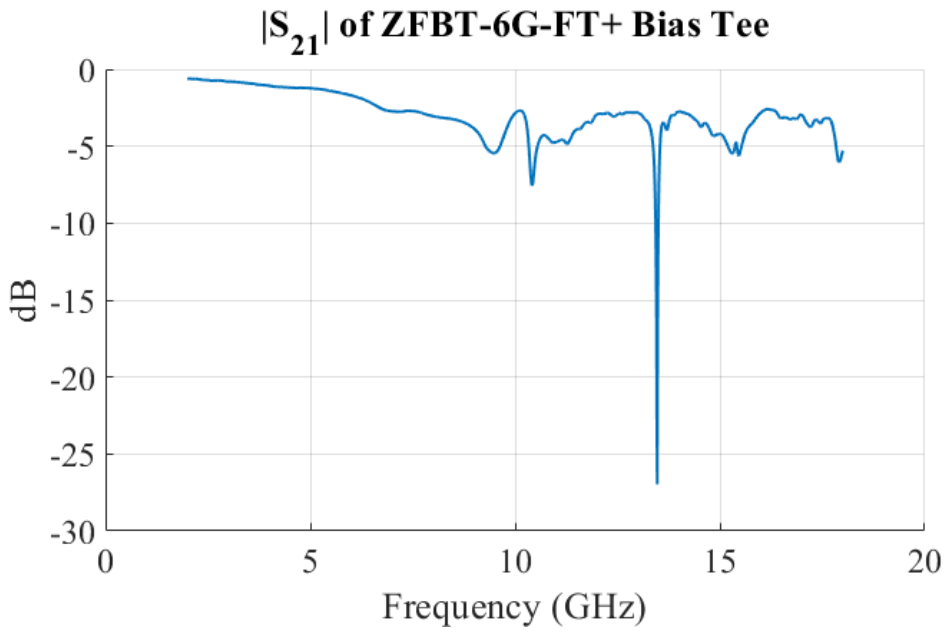

Figure A.8. $|S_{21}|$ of Mini-Circuits ZFBT-6G-FT+ bias-tee.

range is 6 GHz as the insertion loss is no longer smooth past 9 GHz as shown in Figure A.8. This frequency range is adequate for the 1st harmonic, and thus the VNA measurements that only capture the 1st harmonic. For the GSG Probe measurements, Picoprobe 40A-GSG-520-DP (520 μm pitch) probes were used and a SOLT calibration was performed using Picoprobe CS-9 calibration substrate to shift the measurement reference plane to the probe tips. For the SMA end launch measurement, the e-cal module was used to perform a SOLT calibration to shift the measurement reference plane to the connectors at the end of the VNA cable. The 2x-Thru was measured to account for the loss associated with the CBCPW and end launch connectors. A Keysight PNA-X Network Analyzer, Model N5242A, was used for the measurements. The measurement was performed at three different VNA port output powers: -10 dBm, 0 dBm, and 10 dBm. The RFIN to V_D measurement varies based on the VNA output power. The amplifier is a non-linear device and the gain will decrease with increasing input power. Each of the RFIN to V_D measurements were normalized to the gain measurement at that power level so that is referenced to the output power of the amplifier. The result is shown in Figure A.9. When the measurement is normalized to

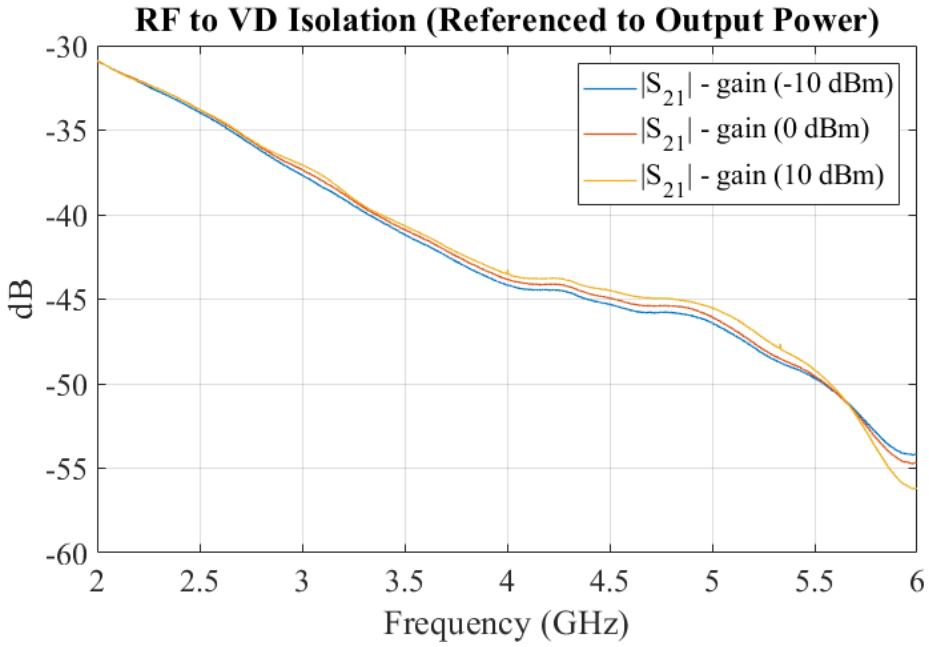

Figure A.9. RF to VD isolation with respect to the amplifier output power.

the output power it is shown to be independent of the input power as expected for the bias network that consists of passive devices. The isolation improves with increasing frequency. If the amplifier was driven such that it was outputting its max power (32 dBm), then the RF leakage to V_D would be at 0 dBm at 2 GHz.

HIGHER ORDER HARMONICS OF AMPLIFIER

Before discussing the harmonics present at V_D, it is important to first understand the harmonics present at the amplifier output. Harmonic distortion is typically expressed as a power ratio in dBc where the harmonic distortion is equal to the dB difference between the fundamental harmonic and the higher-order harmonic. Harmonic distortion data is typically included in datasheets, but it was desirable to obtain the data for the same test set-up as the other measurements. These measurements will allow for the performance of the internal bias tee to be assessed for the higher-order harmonics outside of the amplifier's operating frequency range. A Keysight EXA Signal Analyzer N9010A (10 Hz - 26.5 GHz) and a

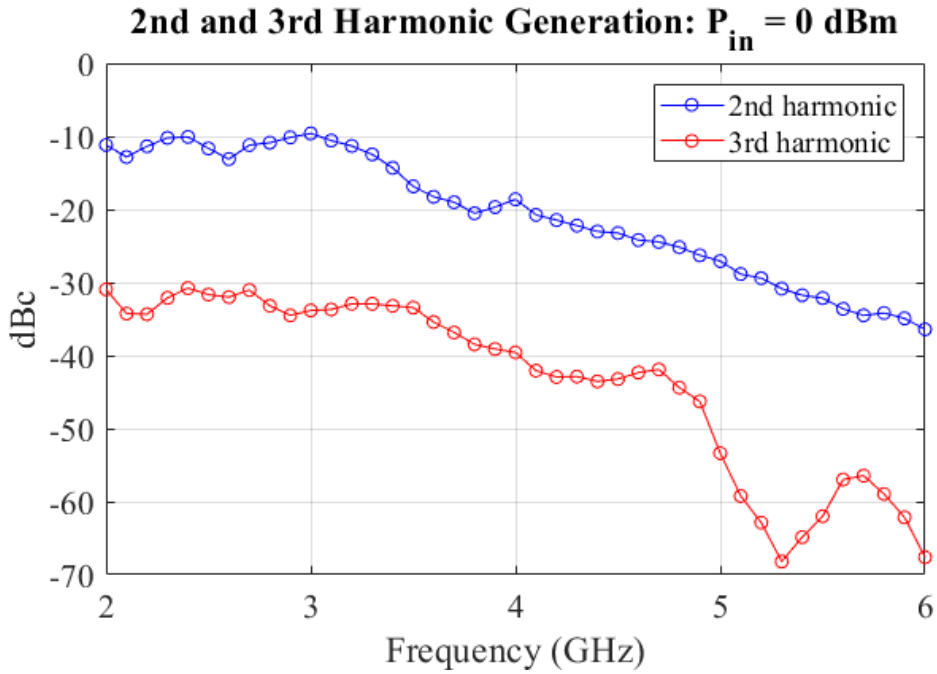

Figure A.10. TGA2597-SM 2nd and 3rd harmonic generation as a function of frequency.

Keysight E4438C function generator (250 kHz - 6 GHz) were used for the measurement. A 2 W 20 dB attenuator was placed at the input of the spectrum analyzer so that the maximum power rating would not be exceeded. The output spectrum was recorded for an input power of 0 dBm and 10 dBm. The measured values were scaled up by a thru measurement that included the cables and the 20 dB attenuator to account for the loss.

Figure A.10 shows the 2nd and 3rd harmonic generation as a function of frequency for an input power of 0 dBm. At this input power, the output power is roughly 20 dBm. At the low end of the frequency range for a 20 dbm output power, the 2nd harmonic power is roughly 10 dBm and the 3rd harmonic power is roughly -10 dbm. The harmonic generation decreases with increasing frequency for this amplifier. One possible explanation for this behavior is that the matching networks are attenuating the transistor gain in the lower frequency range while the higher-order harmonics at higher frequencies are not as attenuated. The gain of the individual transistors is not flat with frequency. For wideband amplifiers, the matching networks are typically designed to sacrifice gain at some frequencies to obtain a flat gain

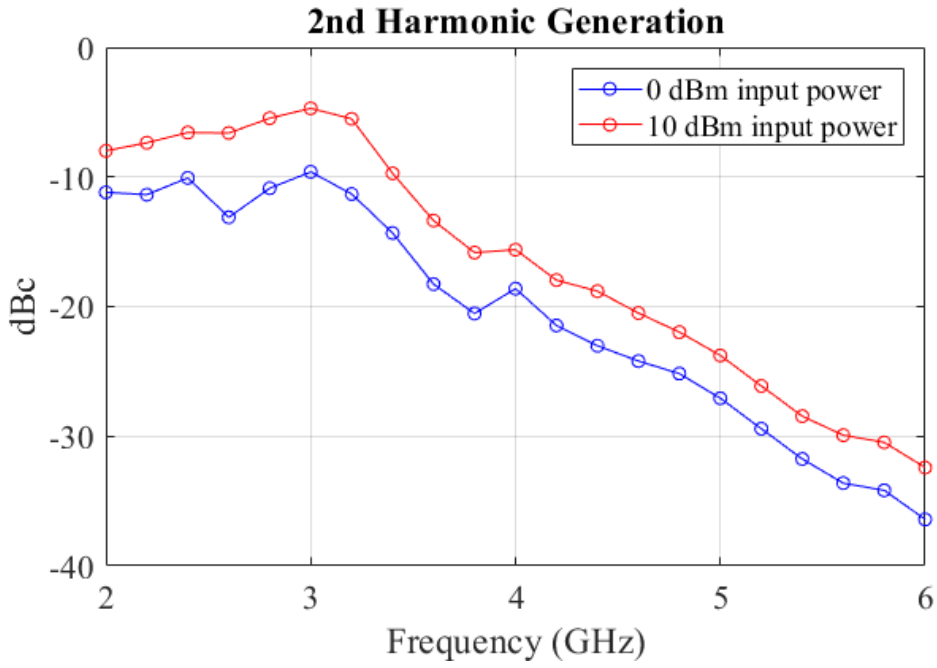

Figure A.11. 2nd harmonic generation at two different power levels.

response across the entire operating frequency range. Another important parameter to consider with harmonic generation is input power. In general, amplifiers becomes more non-linear with increasing input power. Figure A.11 shows the 2nd harmonic generation at input powers of 0 dBm and 10 dBm. The 10 dB increase in input power results in a couple dB increase of the 2nd harmonic generation. As a result, at higher power levels the harmonics become more important to consider. These measurements agree with the data in the TGA2597-SM datasheet [51].

To capture the higher order harmonics at V_D, a spectrum analyzer measurement was performed. The test set-up is the same as the network analyzer measurement except a function generator supplies the CW RF signal to the RFIN of the amplifier and the spectrum analyzer measures the resulting output. A Keysight EXA Signal Analyzer N9010A (10 Hz - 26.5 GHz) and a Keysight E4438C function generator (250 kHz - 6 GHz) were used for the measurement. A power level of 0 dBm was used for the input power to the amplifier. The power of the 1st, 2nd, and 3rd harmonics present at V_D were recorded. For

an efficient measurement that could resolve small power levels, a RBW of 1 kHz was used with a narrow span while the center frequency was set to the harmonic of interest. Very long sweep times would be required to measure all three harmonics simultaneously with a small RBW. The function generator itself produces higher order harmonics in addition to the desired fundamental (1st) harmonic. To check if the function generator harmonic generation was affecting the measurement, bandpass filters were placed at the function generator output at various frequencies. After accounting for the filter's passband insertion loss, the function generator's harmonic generation was found to not impact the measurement. As a result, the measurements were performed without using a filter for the function generator output as it would make the measurements more tedious. To account for loss in the test set-up, thru measurements were made to normalize the values recorded by the spectrum analyzer. For the GSG probe measurement, a thru structure on the Picoprobe CS-9 calibration substrate was used to connect the two GSG probes. For the SMA edge launch measurement, the 2x-Thru structure on the test board was used to connect the two cables. As mentioned previously, the Mini-Circuits ZFBT-6G-FT+ bias-tee's insertion loss is only smooth until about 9 GHz. The insertion loss of the bias tee will have a large impact on the measured values for the 2nd and 3rd harmonics. However, accounting for the loss with the thru measurement that includes the bias tee should be adequate for correcting these values. Although, the large dip in the insertion loss at 13.5 GHz may be an issue.

Figure A.12 shows the power level of the harmonics at V_D for an input power of 0 dBm. The power level of the 1st and 2nd harmonics is highest in the lower frequency range of operation. The third harmonic has an increase in power level in the fundamental frequency range of 4.7-6 GHz, corresponding to a third harmonic frequency range of 14.1-18 GHz. Although, the power level of the 1st harmonic is much higher than the other harmonics it is still important to consider them as the coupling mechanisms in a PCB tend to become more

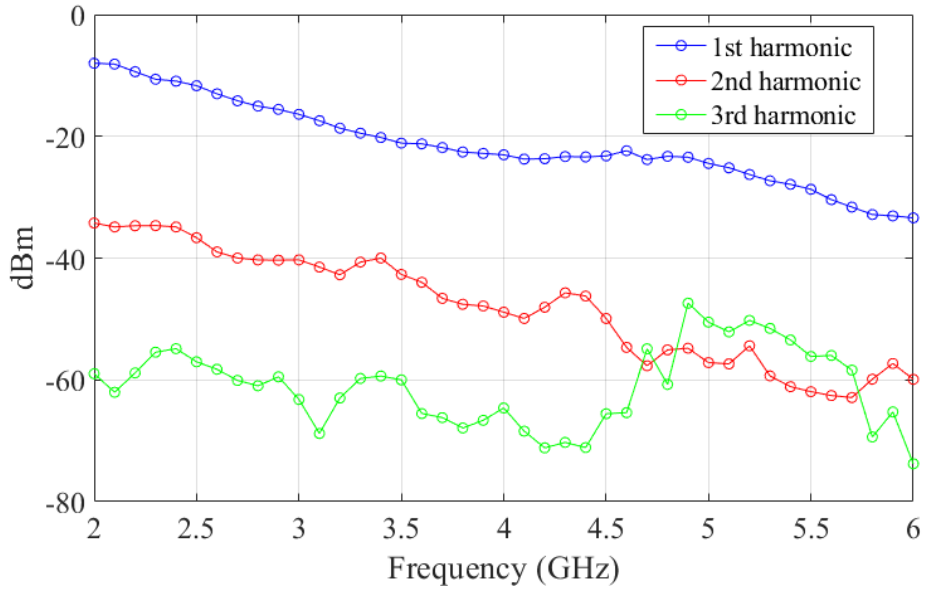

Figure A.12. RFIN to VD isolation for the first three harmonics.

efficient with increasing frequency. The power level of all the harmonics will increase with increasing input power while the separation (dBc) between the fundamental harmonic and higher-order harmonic will decrease as well.

The higher-order harmonic data at the amplifier output can be subtracted from the harmonic data at V_D to assess the performance of the internal bias tee outside of the amplifier's frequency range. Figure A.13 shows the isolation of the bias tee obtained from all the data from the three harmonics. As shown from the network analyzer measurements, the bias tee isolation is lowest in the lower frequency range of the amplifier. From 6 to 13 GHz, the isolation is relatively stable fluctuating between -45 dB to -55 dB. After 14 GHz, the internal bias tee isolation decreases and becomes very small. This decrease in isolation is only relevant for the 3rd harmonics produced in the 4.7-6 GHz operating frequency range of the amplifier. However, in this frequency range the power level of the 3rd harmonic is still low. Overall, the higher order harmonics are suppressed more than the 1st harmonic for much of the frequency range. The 1st harmonic will then be the most significant for noise coupling considerations. Many power amplifiers do not have a bias tee integrated

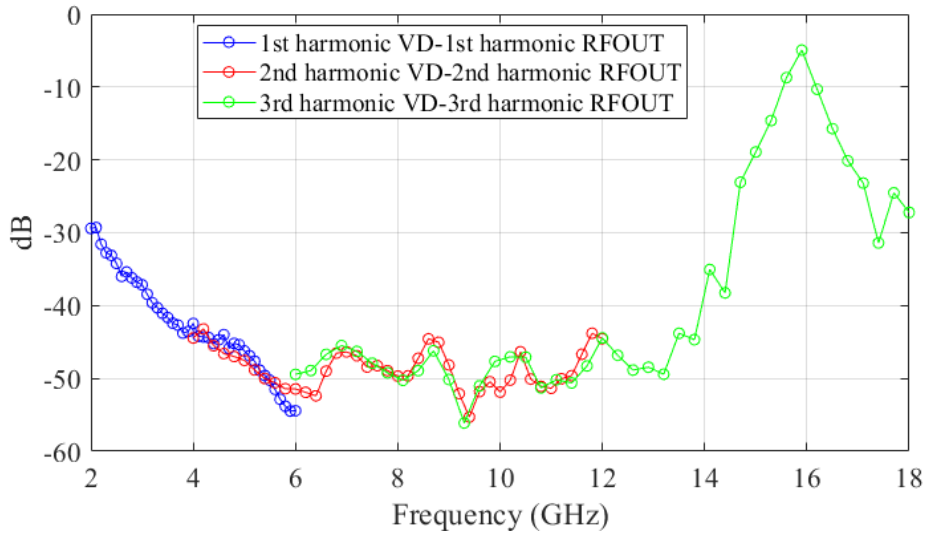

Figure A.13. Internal bias tee network isolation performance calculated from measured harmonic data at VD and the amplifier output.

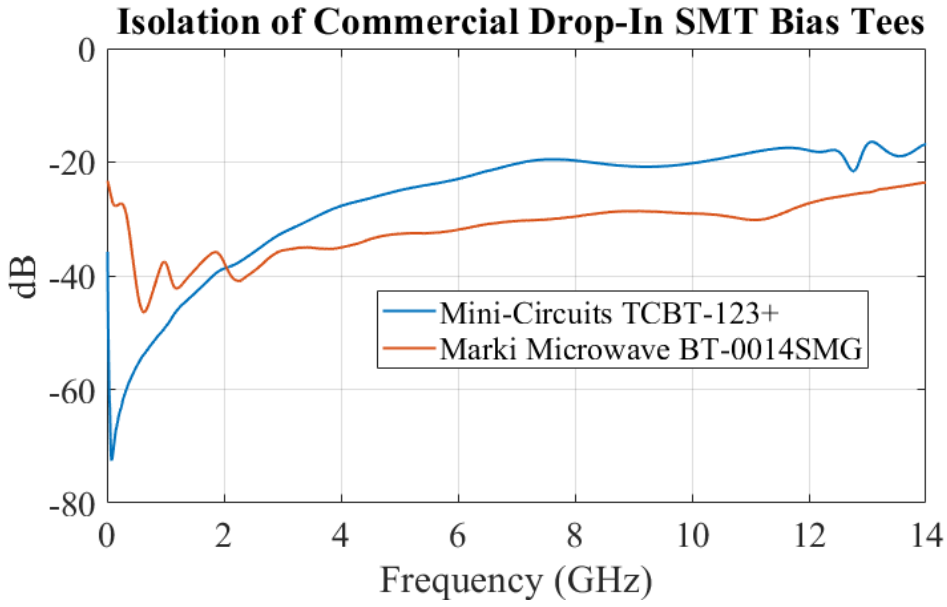

Figure A.14. Comparison of the isolation of two commercial drop-in SMT bias tees.

into the IC. There is a RF/V_{DD} pin for these amplifiers. For instance, wideband distributed amplifiers typically require an external bias tee [69]. Also, the majority of amplifiers from Mini-Circuits require an external bias tee. The use of an external bias tee allows for the isolation between V_D and RF to be easily characterized. Figure A.14, shows the isolation vs frequency for two commercial available SMT bias tees: Mini-Circuits TCBT-123+ [70] and Marki Microwave BT-0014SMG [71]. At low frequencies the isolation of the commercial bias tees is larger than the internal bias tee of the TGA2597. However, the isolation of the commercial bias tees decreases at higher frequencies while the internal bias tee had greater than 40 dB isolation from 6-13 GHz. A bias tee that uses discrete components may lose isolation at higher frequencies due to various parasitic coupling mechanisms. The parasitic coupling mechanisms are less efficient for smaller devices such as a bias tee implemented in a MMIC which explains why it maintains a higher isolation at higher frequencies. The isolation of the internal bias tee is limited at lower frequencies by the inductance values that can be obtained with MMIC spiral inductors. Overall, the use of an external bias tee is likely to result in an increase of RF leakage into the power distribution network especially for the higher order harmonics.

RF TO VG ISOLATION

The V_G net is also connected to the RF through a bias tee network. The output of the 1st gain stage and inter-stage matching network is connected to the gates of the transistors in the 2nd gain stage. In comparison, the drain which V_D is connected to through a bias tee network is at the output of the amplifier. As a result, there is expected to be some RF leakage to the external V_G net, but less than the RF leakage to V_D which is at the output of the amplifier. A network analyzer measurement was performed with the same test set-up as the RF to V_D isolation measurement except now V_G is supplied through a bias tee while V_D is supplied through a DC positioner. The output power is subtracted from the resulting measurement to reference it to the output power. Figure A.15 shows the measurement result

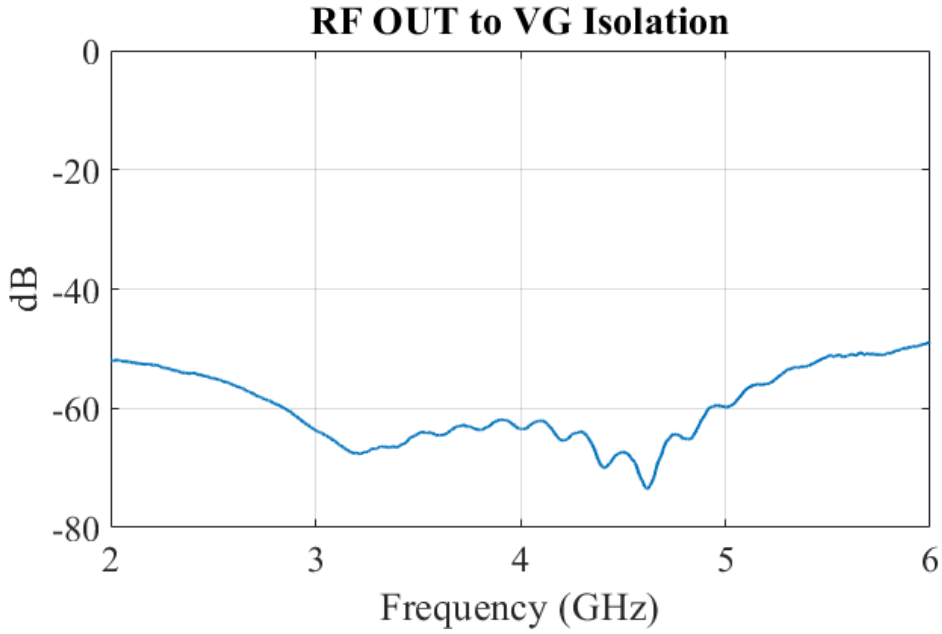

Figure A.15. Measured RF to VG isolation referenced to output power

and the RF to V_G RF leakage is much less than the RF leakage to V_D, as expected. In addition, the gate bias voltage typically only draws a few mA so it is less likely a power plane will be used. The absence of a power/GND cavity will result in less efficient coupling through the PCB. As a result, in most cases, the RF leakage on the V_D net will be of primary concern.

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VITA

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