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HIGH-VOLTAGE-GAIN DC-DC POWER ELECTRONIC CONVERTERS – NEW TOPOLOGIES AND CLASSIFICATION

by

BHANU PRASHANT REDDY BADDIPADIGA

A DISSERTATION

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

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Approved by

Mehdi Ferdowsi, Advisor Mariesa L. Crow Jonathan W. Kimball Pourya Shamsi Bruce M. McMillin

PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles:

Paper I - Pages 9 to 38, "A High-Voltage-Gain DC-DC Converter based on Modified Dickson Charge Pump Voltage Multiplier," accepted for publication in IEEE Transactions on Power Electronics.

Paper II - Pages 39 to 69, "High-Voltage-Gain DC-DC Converter using Diode-Capacitor Voltage Multiplier Cells," submitted to IEEE Transactions on Power Electronics.

Paper III - Pages 70 to 112, "A Family of High-Voltage-Gain DC-DC Converters based on a Generalized Structure," to be submitted to IEEE Transactions on Power Electronics.

ABSTRACT

This dissertation proposes two new high-voltage-gain dc-dc converters for integration of renewable energy sources in 380/400V dc distribution systems. The first high-voltage-gain converter is based on a modified Dickson charge pump voltage multiplier circuit. The second high-voltage-gain converter is based on a non-inverting diode-capacitor voltage multiplier cell. Both the proposed converters offer continuous input current and low voltage stress on switches which make them appealing for applications like integration of renewable energy sources. The proposed converters are capable for drawing power from a single source or two sources while having continuous input current in both cases. Theoretical analysis of the operation of the proposed converters and the component stresses are discussed with supporting simulation and hardware results. This dissertation also proposes a family of high-voltage-gain dc-dc converters that are based on a generalized structure. The two stage general structure consists of a two-phase interleaved (TPI) boost stage and a voltage multiplier (VM) stage. The TPI boost stage results in a classification of the family of converters into nonisolated and isolated converters. A few possible VM stages are discussed. The voltage gain derivations of the TPI boost stages and VM stages are presented in detail. An example converter is discussed with supporting hardware results to verify the general structure. The proposed family of converters can be powered using single source or two sources while having continuous input current in both cases. These high voltage gain dcdc converters are modular and scalable; making them ideal for harnessing energy from various renewable sources offering power at different levels.

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I dedicate my dissertation to my father Dr. Shiva Reddy Baddipadiga and mother Kamala Baddipadiga. They have taught me the importance of education and supported me in all my endeavors. I would also like to thank my brother Damodar Reddy Baddipadiga and my sister-in-law Swetha Baddipadiga for being part of my support system. I would also like to thank the long list of friends and well-wishers for their love and blessings.

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1.INTRODUCTION

1.1. HIGH-VOLTAGE-GAIN DC-DC CONVERTER APPLICATIONS

In the past, high-voltage-gain dc-dc power electronic converters were mainly used for powering HID lamps in automotive headlamps and integrating battery banks onto the high voltage dc bus of UPS's [1, 2]. However, over the last decade, they have been gaining popularity for integration of renewable energy sources [3-7]. Applications like dc distribution systems [8, 9], dc microgrids [10, 11], solid state transformer (SST) [12, 13], and grid-tied inverter systems [14] include a dc bus usually at a voltage of 400V. Renewable sources such as solar panels, fuel cells, etc., typically output power in the voltage range of 20V to 45V. High-voltage-gain dc-dc converters make it feasible for connecting such sources to the high voltage bus by boosting the low voltage from the sources to higher voltages.

One of the most recently growing applications is dc distribution systems at 400V [8, 9]. Such systems have been gaining more and more popularity for telecom, data centers, and commercial buildings due to its various benefits. It offers better efficiency, higher reliability at an improved power quality, and low cost compared to the ac distribution systems. The best of all, they offer simpler integration of renewable energy and energy storage. As of now, based on various different studies, 400V dc is being recognized as the optimal voltage level for dc distribution systems. One of the challenges with such systems would be the integration of different renewable sources and energy storage devices. A high-voltage-gain dc-dc converter would be the best solution for integrating low voltage renewable energy sources onto the 400V dc bus.

1.2. REVIEW OF EXISTING TOPOLOGIES

Conventional boost (see Figure. 1.1) and buck-boost converters (see Figure. 1.2) are the first choices of anyone who is trying to achieve higher output voltages compared to the input. The output voltages of the boost and buck-boost converters are given using (1.1) and (1.2) respectively.

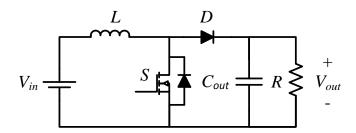


Figure. 1.1. Conventional boost converter

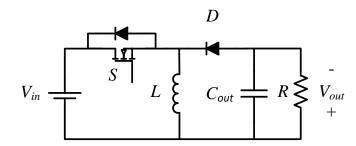


Figure. 1.2. Conventional buck-boost converter

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - d} \tag{1.1}$$

$$\frac{V_{out}}{V_{in}} = \frac{d}{1 - d} \tag{1.2}$$

From (1.1) and (1.2), it is observed that boost and buck-boost converters require higher duty cycles to achieve higher voltages. Higher duty cycles imply large input currents. They would increase the conduction losses in the switching MOSFET. Therefore, the converter efficiency is reduced. The peak blocking voltage of the MOSFET is equal to the output voltage. Also, due to high output voltage and large pulse currents, there is a serious reverse recovery problem in the diode of both converters. To summarize, the losses in the parasitics, high voltage stress on switch, and serious reverse recovery problem of the diode make the boost and buck-boost converters unsuitable for use as high voltage gain converters.

The next obvious choice would be conventional isolated converters such as forward, flyback, half-bridge, full-bridge, and push-pull converters. The voltage gain of these converters is dependent on the turns ratio of the transformer or coupled inductors. Therefore, these converters can achieve high voltage gains by using larger turns ratio on their transformers or coupled inductors. However, these converters draw discontinuous input current making them ill-suited for renewable energy applications such as solar. They would require large input filter capacitors to be able to operate with renewable sources like solar. Also, the leakage inductance in these converters leads to increased voltage spikes on its switches. Therefore, clamping circuits required to protect the switches make the system design complicated. With conventional non-isolated and isolated converters failing in one way or the other, new high-voltage-gain dc-dc converters have been sought for.

Many non-isolated and isolated high-voltage-gain dc-dc converters have been proposed in literature for the integration of renewable energy sources and energy storage

devices. The boost converters output voltage was extended using tapped inductors (see Figure. 1.3). Tapped inductor boost [15] uses an approach similar to flyback converter where the voltage gain of the converter can be increased by changing the duty ratio and the turn's ratio of the tapped inductor. The voltage gain of a tapped inductor boost converter is given as

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - d} + \frac{N_2}{N_1} \frac{d}{1 - d}$$
 (1.3)

The voltage gain was increased compared to a conventional boost. However, its drawback was the discontinuity in input current which made it unsuitable for applications using solar panels.

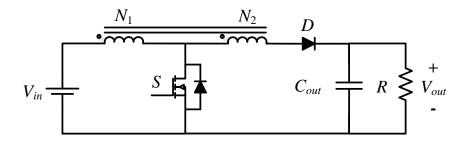


Figure. 1.3. Tapped inductor boost converter

Later, interleaved boost converters were modified using coupled inductors to achieve further higher gains. A two phase interleaved boost using coupled inductors [16] is shown in Figure. 1.4. The voltage gain of the converter is calculated using (1.4). The additional boost in the output voltage is achieved using the coupled inductors. In this case, the input current is continuous with smaller ripple owing to the interleaved operation of the two boost phases.

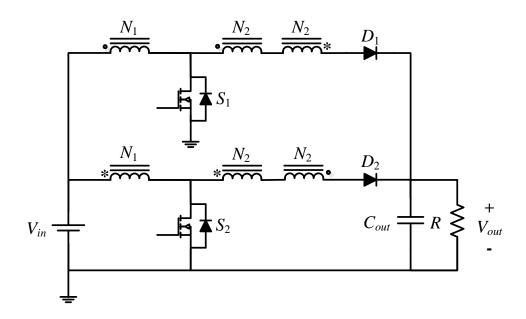


Figure. 1.4. Interleaved boost converter using coupled inductors

$$\frac{V_{out}}{V_{in}} = \left(\frac{N_2}{N_1} + 1\right) \frac{1}{1 - d} \tag{1.4}$$

In an attempt to further increase the output voltage, voltage multiplier cells were used in conjunction with the coupled inductor interleaved boost. This enabled to achieve further higher boost while maintaining continuity in input current. An interleaved boost with voltage multiplier cell [17] is shown in Figure. 1.5. The voltage gain of this converter is given as

$$\frac{V_{out}}{V_{in}} = \left(\frac{2N_2}{N_1} + 1\right) \frac{1}{1 - d} \tag{1.5}$$

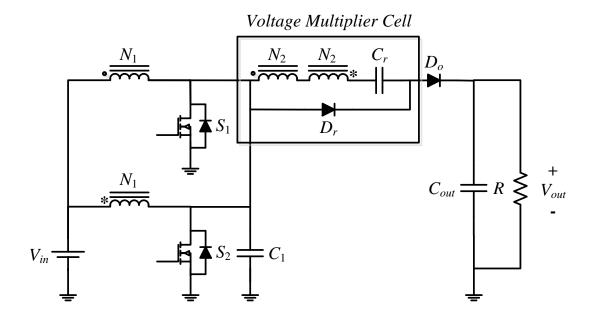


Figure. 1.5. Interleaved boost converter with voltage multiplier cell

Many more high-voltage-gain dc-dc converters have been explored over the last decade. Most of these high-voltage-gain converters use a boost stage in combination with voltage multiplier circuits. In some, a multi-phase interleaved boost stage is involved to achieve even higher voltage gains. The boost circuit or voltage multiplier circuit in some converters involves either a coupled inductor or a transformer or both to achieve further high voltage gains.

A classification of non-isolated boost-based dc-dc converters has been presented in [18]. The step-up topologies with wide conversion ratio have been mainly classified into five types. They are - (1). Cascaded boost converters, (2). Coupled-inductor based boost converters, (3). Switched-capacitor based boost converters, (4). Interleaved boost converters and (5). Three-state switching cell (3-SSC) based converters. This classification gives a better picture on how most of the high-voltage-gain dc-dc

converters are built. The main features that a high-voltage-gain dc-dc converter has to offer for use in renewable energy applications are high voltage gain, high efficiency, continuous input current, and low device stress. Most converters can only offer a few of these features making them less appealing for such applications.

1.3. RESEARCH CONTRIBUTION

In this dissertation, Papers I and II introduce two new non-isolated high-voltagegain dc-dc converters. The proposed converter in Paper I is based on a modified Dickson charge pump voltage multiplier circuit. This converter is capable of integrating a voltage source as low as 20V to a 400V dc bus. The major contribution of this converter is its lower voltage ratings on its voltage multiplier circuit capacitors which potentially reduces the size and cost of the converter. The converter proposed in Paper II is based on a noninverting diode-capacitor voltage multiplier circuit. It offers a high-voltage-gain while having a simple structure with low component count. Both these converters can be powered using two different sources or a single source in an interleaved manner. They offer continuous input current with smaller ripple making them ideal for different power sources like solar panels and batteries. They also offer low voltage stress on their semiconductor devices in comparison to their output voltage. Different modes of operation have been explained. The output voltage and component stress for the two converters have been derived. The theoretical analysis carried out is verified using supporting simulation and experimental results.

Finally, in Paper III, a family of high-voltage-gain dc-dc converters based on a generalized structure is proposed. The generalized structure has two stages – a two-phase

interleaved (TPI) boost stage on the input side and a voltage multiplier (VM) stage on the output side. The intermediate voltage between the two stages forms the key to the generalized structure. The proposed family of converters is classified into both nonisolated and isolated topologies based on the TPI boost stage used. The isolation in the converters is achieved using either coupled-inductors or a transformer. There are six different TPI boost stages that could be used as the first stage. This way one is able to build six different topologies using a single VM stage. Therefore, with 'N' different voltage multiplier cells, we can achieve a total of '6N' converter topologies under this family of converters. With the TPI boost stage on the input side, the proposed family of converters is capable of drawing power from two sources or a single source in interleaved manner. The continuity in input current is possible in all the converters operating with a single source; making them suitable for sources like solar panels and batteries. An example converter is built, analyzed using the proposed generalized structure. Experimental results are provided to support the analysis of the theoretical converter. The proposed family of converters paves the way to direct integration of renewable resources in low voltage (400V) dc systems. These converters are highly scalable, modular, and offer plug and play feature.

PAPER

I. A HIGH-VOLTAGE-GAIN DC-DC CONVERTER BASED ON MODIFIED DICKSON CHARGE PUMP VOLTAGE MULTIPLIER

Abstract – A high-voltage-gain dc-dc converter is introduced in this paper. The proposed converter resembles a two-phase interleaved boost converter on its input side while having a Dickson charge pump based voltage multiplier on its output side. This converter offers continuous input current which makes it more appealing for the integration of renewable sources like solar panels to a 400-V dc bus. Also, the proposed converter is capable of drawing power from either a single source or two independent sources. Furthermore, the voltage multiplier used offers low voltage ratings for capacitors which potentially leads to size reduction. The converter design and component selection has been discussed in detail with supporting simulation results. A hardware prototype of the proposed converter with V_{in} =20V and V_{out} =400V has been developed to validate the analytical results.

I. INTRODUCTION

Distribution systems at 400-V dc have been gaining popularity as they offer better efficiency, higher reliability at an improved power quality, and low cost compared to ac distribution systems [1-4]. They offer a simpler integration of renewable energy and energy storage systems. Currently, telecom centers, data centers, commercial buildings, residential buildings, and microgrids are among the emerging examples of dc distribution systems [5-7]. One of the challenges facing such systems is the power electronic

converters for integrating renewable sources into the 400-V dc bus. A typical voltage range for solar panels is between 20V dc to 40V dc. Stepping up these voltages to 400-V dc using classic boost and buck-boost converters requires high duty ratios which results in high component stress and lower efficiency. Therefore, a typical choice would be using two cascaded converters; which results in inefficient operation, reduced reliability, increased size, and stability issues. Isolated topologies like flyback, forward, half-bridge, full-bridge, and push-pull converters have discontinuous input currents and hence would require large input capacitors.

High-voltage-gain dc-dc converters using a boost stage followed by voltage multiplier (VM) cells have been proposed in [8-11]. The second order hybrid boosting converter proposed in [8] offers relatively low voltage gain in comparison to its voltage multiplier component count. It also has a very large input current ripple in proportion to its average. High step-up converters using single-inductor-energy-storage-cell-based switched capacitors proposed in [9] do not offer voltage gains high enough to boost a 20V input to 400V at an reasonable switching duty cycle. The multiple-inductor-energy-storage-cell-based switched capacitor based high voltage converters [9] offer a relatively low voltage gain in proportion to its component count. The switched-capacitor-based active-network converter proposed in [10] has a discontinuous input current ripple due to the series and parallel connection of the inductors in its two modes of operation. The transformer-less high-gain boost converter proposed in [11] offers continuous input current but the switches experience a high voltage stress – more than 2/3rd of its output voltage.

High-voltage-gain dc-dc converters using coupled inductors and high frequency transformers have been proposed for the integration of solar panels to 400V dc bus [12-18]. In such converters, the design of high frequency transformers and coupled inductors is complicated as the leakage inductance increases when higher voltage gains are intended. As a result, the converter switches experience large voltage spikes and therefore would require clamping circuitry to reduce the voltage stress on the switches. These clamping circuits have a negative effect on the converter voltage gains. A family of non-isolated high-voltage-gain dc-dc converters that makes use of VM cells derived from the Dickson charge pump (see Fig. 1) has been proposed in [19]. The voltage rating of each VM cell capacitor is twice that of its previous VM cell. Also, the inductors (L_1 , L_2) and switches (S_1 , S_2) experience different current stresses whenever even number of VM cells is used.

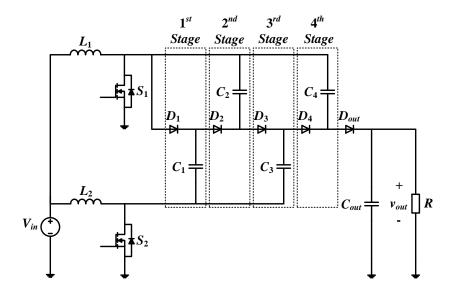


Fig. 1. High-voltage-gain dc-dc converter using Dickson charge pump

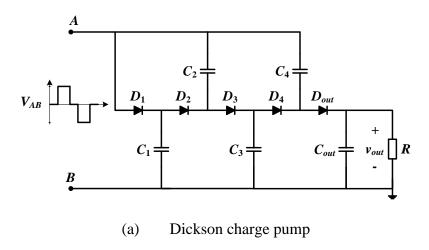
A high-voltage-gain dc-dc converter based on the modified Dickson charge pump voltage multiplier circuit is introduced in this paper. This converter is capable of stepping up voltages as low as 20V to 400V. The proposed converter offers continuous input current and low voltage stress (1/4th of its output voltage) on its switches. This converter can draw power from a single source or two independent sources while having continuous input currents, which makes it suitable for applications like solar panels. Compared to the topology presented in [19], the proposed converter requires lower voltage rating capacitors for its VM circuit and also one less diode. The inductors and switches experience identical current stresses making the component selection process for the converter simpler.

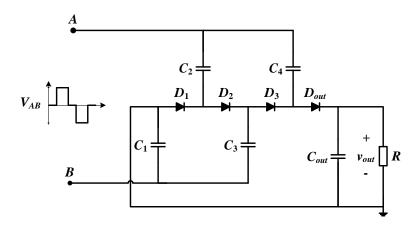
In section II, the modified Dickson charge pump voltage multiplier circuit has been discussed. Section III introduces the proposed high-voltage-gain topology and explains its modes of operations. The voltage gain of the proposed converter has been derived in section IV. Section V analyzes the component stress and provides supporting simulation results. Section VI discusses the experimental results obtained using the hardware prototype. A comparative analysis of the proposed converter and the high-voltage-gain converter shown in Fig. 1 has been discussed in section VII. Finally, section VIII concludes the paper.

II. MODIFIED DICKSON CHARGE PUMP VOLTAGE MULTIPLIER

The Dickson charge pump voltage multiplier circuit [20] shown in Fig. 2a offers a boosted dc output voltage by charging and discharging its capacitors. The input voltage (V_{AB}) is an modified square wave (MSW) voltage. The voltages of the capacitors in the

Dickson charge pump double at each stage as one traverses from the input side capacitor C_1 to the load side capacitor C_4 . For an output voltage of $V_{out} = 400$ V, the voltages of capacitors C_1 , C_2 , C_3 , and C_4 are 80V, 160V, 240V, and 320V respectively.





(b)

Fig. 2. Conventional and modified Dickson charge pump voltage multiplier circuits

Modified Dickson charge pump

The authors propose to make a slight modification to the Dickson charge pump circuit as shown in Fig. 2b. For a same output voltage, the voltages of all the capacitors in

the modified Dickson charge pump are smaller than the voltage of capacitor C_2 in the Dickson charge pump. For an output voltage of $V_{out} = 400$ V, the voltages of capacitors C_1 , C_2 , C_3 , and C_4 are only 150V, 50V, 50V, and 150V, respectively Therefore the volume of the capacitors used in the proposed modified Dickson charge pump voltage multiplier circuit is potentially less compared to the Dickson charge pump.

III. TOPOLOGY AND MODES OF OPERATION

The proposed converter provides a high voltage gain using the modified Dickson charge pump voltage multiplier circuit (see Fig. 3). On a closer look, it can be seen that the converter is made up of two stages. The first stage is a two-phase interleaved boost converter which outputs an MSW voltage between its output terminals A and B. The second stage is the modified Dickson chare pump voltage multiplier circuit that boosts the MSW voltage (V_{AB}) to provide a higher dc output voltage. The gating signals of the two interleaved boost stage switches S_1 and S_2 are shown in Fig. 4. For the proposed converter to operate normally, both switches S_1 and S_2 must have an overlap time where both are ON and also one of the switches must be ON at any point of time. This can be achieved by using duty ratios of greater than 50% for both the switches and having them operate at 180 degrees out of phase from each other. As can be seen from Fig. 4, such gate signals lead to three different modes of operation which are explained as follows.

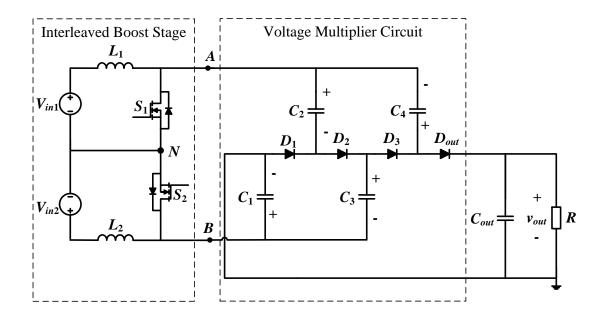


Fig. 3. Proposed high-voltage-gain dc-dc converter

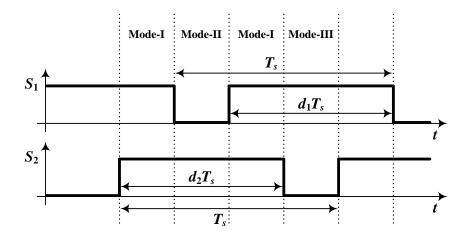


Fig. 4. Input boost converter switching signals for the proposed converter

A. Mode I

In this mode, both switches S_1 and S_2 of the two-phase interleaved boost converter are ON (see Fig. 5). Input sources V_{in1} and V_{in2} charge inductors L_1 and L_2 respectively.

Inductor currents i_{L1} and i_{L2} both increase linearly. All the diodes of the voltage multiplier circuit are reverse-biased and hence OFF. The voltages of the multiplier capacitors remain same and the output diode D_{out} is reverse biased. Therefore, the load is supplied by the output capacitor.

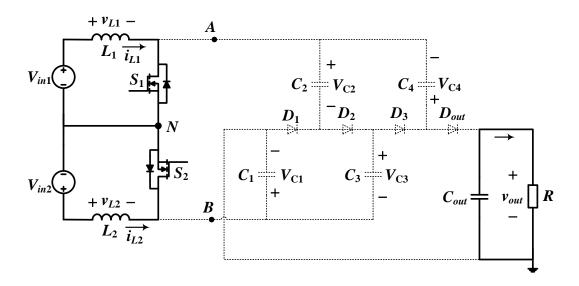


Fig. 5. Proposed converter operation in mode-I

B. Mode II

In this mode, switch S_1 is OFF and switch S_2 is ON. Diodes D_1 and D_3 are OFF as they are reverse biased while diodes D_2 and D_{out} are ON as they are forward biased (see Fig. 6). A part of inductor current i_{L1} flows through capacitors C_2 and C_3 and thereby charging them. The remaining current flows through the capacitors C_4 and C_1 discharging them to charge the output capacitor C_{out} and supply the load.

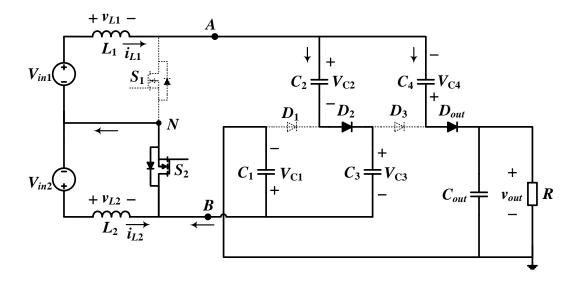


Fig. 6. Proposed converter operation in mode-II

C. Mode III

In this mode switch S_1 is ON and switch S_2 is OFF (see Fig. 7). Diodes D_1 and D_3 are ON as they are forward biased while diodes D_2 and D_{out} are OFF as they are reverse biased. Inductor current i_{L2} flows through diode-capacitor voltage multiplier cell capacitors C_1 , C_2 , C_3 , and C_4 . Capacitors C_1 and C_4 are charged while discharging capacitors C_2 and C_3 . In this mode, the output capacitor supplies the load.

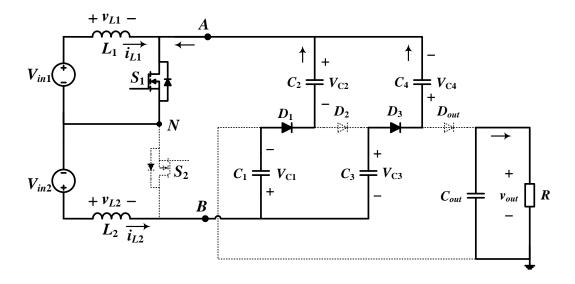


Fig. 7. Proposed converter operation in mode-III

IV. VOLTAGE GAIN OF THE CONVERTER

In the proposed converter, the input power is transferred to the output by charging and discharging the voltage multiplier circuit capacitors. For an ideal converter shown in Fig. 3, the voltage gain of the converter can be derived as described below. For inductors L_1 and L_2 , the average voltage across the inductors according to volt-second balance can be written as

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = 0 \tag{1}$$

From Fig. 6, based on the volt-second balance of inductor L_1 , one can write

$$V_{AN} = V_{C2} + V_{C3} = V_{out} - V_{C1} - V_{C4} = \frac{V_{in1}}{(1 - d_1)}$$
 (2)

where d_1 is the duty cycle of switch S_1 . From Fig. 7, based on the volt-second balance of the inductor L_2 , one can write

$$V_{BN} = V_{C1} - V_{C2} = V_{C4} - V_{C3} = \frac{V_{in2}}{(1 - d_2)}$$
(3)

Assuming capacitors C_2 and C_3 are identical, the voltage across them would be equal and can be written as

$$V_{C2} = V_{C3} = \frac{1}{2} \times \frac{V_{in1}}{(1 - d_1)} \tag{4}$$

By substituting (4) in (3), one can derive capacitor voltages V_{C1} and V_{C4} to be

$$V_{C1} = V_{C4} = \frac{1}{2} \times \frac{V_{in1}}{(1 - d_1)} + \frac{V_{in2}}{(1 - d_2)}$$
 (5)

Finally, the output voltage is derived by substituting (5) in (2) which yields

$$V_{out} = \frac{2 \times V_{in1}}{(1 - d_1)} + \frac{2 \times V_{in2}}{(1 - d_2)}$$
 (6)

The proposed converter can be supplied from two inputs (see Fig. 3) as well as using only one input source. When a single input is used for the proposed converter, switches S_1 and S_2 have the same switching duty cycle 'd' and are 180 degrees out of phase from each other. The proposed converter with single source is shown in Fig. 8. The multiplier circuit capacitor voltages and the output voltage are simplified as shown below.

$$V_{C2} = V_{C3} = \frac{1}{2} \times \frac{V_{in}}{(1-d)} \tag{7}$$

$$V_{C1} = V_{C4} = \frac{3}{2} \times \frac{V_{in}}{(1 - d)} \tag{8}$$

$$V_{out} = \frac{4 \times V_{in}}{(1 - d)} \tag{9}$$

A 20-V input source at 80% switching duty cycle will generate an output voltage of 400V using the proposed converter in Fig. 8. Capacitors C_1 and C_4 are charged to 150V and capacitors C_2 and C_3 are charged to 50V.

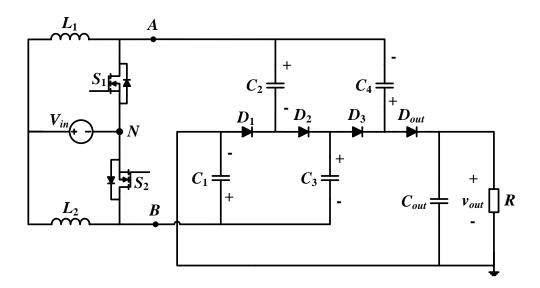


Fig. 8. Proposed converter with single input source

V. COMPONENT STRESS AND SIMULATION RESULTS

This section discusses the voltage and current stresses observed by different components and also provide simulation waveforms during steady-state operation of the proposed converter. The discussions in this section are based on the topology shown in Fig. 8, i.e., using a single voltage source to power the converter while operating both switches S_1 and S_2 of the two-phase interleaved boost stage at a fixed duty cycle d.

A simulation model of the proposed converter has been built in PLECS blockset of MATLAB. The parameters used in the simulation are given in Table I.

Table I. Simulation parameters

Parameter	Value
Input Voltage	20 V
Output Voltage	400 V
Load Resistance	800 Ω
Duty cycle of switches S_1 and S_2	80% or 0.8
Switching Frequency - f_{sw}	100 kHz
Boost Inductors L_1 and L_2	100 μΗ
VM capacitors	60 μF
Output Capacitor	22 μF

A. Inductor

The inductor currents in both phases of the interleaved boost stages are similar. The average inductor currents can be calculated using (10). The rms value of the inductor currents used in the calculation of inductor copper losses can be calculated as shown in (11).

$$I_{L1,avg} = I_{L2,avg} = \frac{2 \times I_{out}}{(1-d)}$$
 (10)

$$I_{L1,rms} = I_{L2,rms} = \sqrt{\left(\frac{2 \times I_{out}}{1 - d}\right)^2 + \left(\frac{V_{in} \times d}{2\sqrt{3} \times L \times f_{sw}}\right)^2}$$
(11)

The inductance required for a current ripple of ΔI_L is given by

$$L_{1} = L_{2} = L = \frac{V_{in} \times d(1 - d)}{4 \times \Delta I_{L} \times f_{sw}}$$
(12)

From (10), (11), and (12), it is observed that both the inductors carry same amount of current and require same inductance for an assumed current ripple. Therefore, a similar inductor can be used for both L_1 and L_2 . Moreover as the rms currents of inductors L_1 and L_2 are equal, minimal conduction losses can be achieved in the inductors compared to other similar converters (see Fig. 1) having different values of currents flowing through their boost stage inductors.

The inductor current and voltage waveforms obtained from PLECS simulation are shown in Fig. 9. At 200W of output power, both the inductors carry a current of 5A with a ripple of 1.6A in each.

B. Input Current

The input source is connected to an interleaved two-phase boost stage. Since it is a boost converter on the input side, the input current is continuous. As the two phases of the interleaved boost are 180 degrees out of phase from each other, the input current ripple is even smaller. This greatly reduces the size of the input filter capacitor required for the converter. The input current waveform of the proposed converter operating at 200W is shown in Fig. 9. It can be seen that the ripple of the input current is about 1.2A even though inductor currents i_{L1} and i_{L2} have a ripple of 1.6A each. The reason for this smaller input current ripple is both the boost switches being operated 180 degrees out of phase from each other.

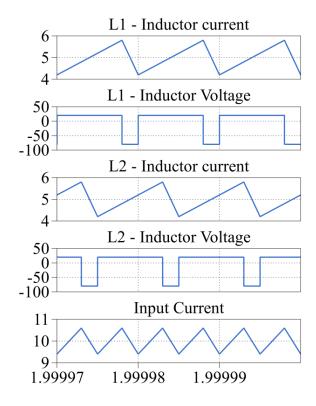


Fig. 9. Inductor L_1 and L_2 – current and voltage waveforms, Input current

C. Switches

The maximum voltage observed across the switches in the proposed converter is equal to the output of its boost stage. This is a small number compared to the high output voltage of the proposed converter. The switch blocking voltages can be calculated using (13). As current in both the inductors is the same, the current stress on both switches is same as well. The average current in the switches can be calculated using (14).

$$V_{S1} = V_{S2} = \frac{V_{in}}{(1-d)} \tag{13}$$

$$I_{S1,avg} = I_{S2,avg} = \frac{2 \times I_{out}}{(1-d)} \tag{14}$$

The waveforms of the switches in the proposed converter are shown in Figs. 10(a) and 10(b). Switches S_1 and S_2 have the same current and voltage stress as can be seen in the simulation waveforms. Since the converter in simulation is operating at 80% switching duty cycle with a 20V input, the maximum voltage stress seen on both switches is only 100V. Both switches S_1 and S_2 carry an average current of 5A.

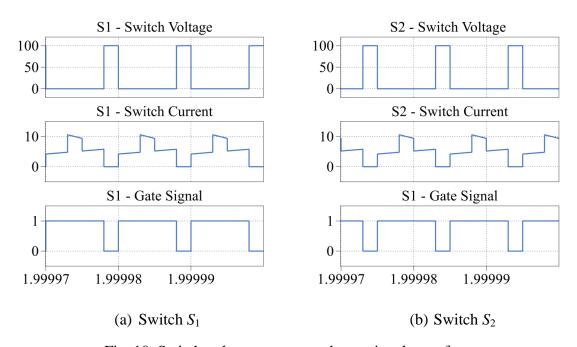


Fig. 10. Switch voltage, current and gate signal waveforms

D. Diodes

The diodes experience two times higher blocking voltages compared to the switches as it depends on the voltages of the voltage multiplier circuit capacitors. In this topology, all the diodes experience the same blocking voltage which can be calculated using (15). The average current in the diode can be calculated using (16). Since all the

diodes experience same maximum voltage stress, similar diodes can be used for all of them.

$$V_{d1} = V_{d2} = V_{d3} = V_{dout} = \frac{2 \times V_{in}}{(1 - d)}$$
 (15)

$$I_{d1,avg} = I_{d2,avg} = I_{d3,avg} = I_{dout,avg} = I_{out}$$
 (16)

The voltage and current waveforms of diodes D_1 , D_2 , D_3 , and D_{out} in the proposed converter are shown in Fig. 11. For the converter operating at 80% switching duty cycle and 20V input, the maximum blocking voltage seen by the diodes is 200V. The diodes conduct either only during mode II or mode III of the converter operation. All the diodes carry an average current of 0.5A which is equal to the output current. Diodes D_2 and D_{out} have different current waveforms. This is because of the voltage imbalance in the capacitors during the start of mode II. Only diode D_{out} initially conducts in order to charge the output capacitor and bring in a balance in the voltage. Once the voltage loops are balanced, then the current flowing through the diodes is dependent on the impedance of the capacitors.

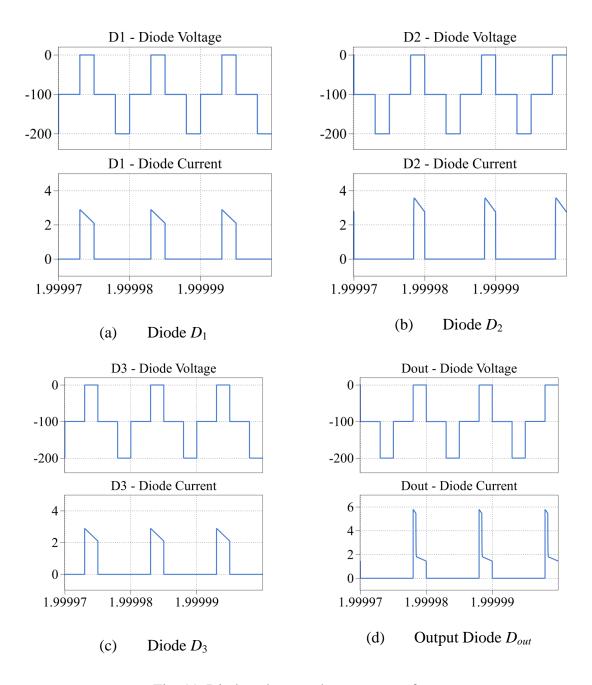


Fig. 11. Diode voltage and current waveforms

VI. EXPERIMENTAL RESULTS

A hardware prototype of the proposed converter was built to test and validate the proposed converter operation. The specifications of the components used for building the

hardware prototype are given in Table II. The power rating of the converter is 400W with an input voltage of 20V and an output voltage of 400V. The proposed converter is tested at a switching frequency of 100 kHz.

Table II. Component specifications of the Hardware Prototype

Component	Name	Rating	Part No
Inductor	L_1,L_2	100 μH, DCR=11 mΩ	CTX100-10-52LP
MOSFET	S_1,S_2	150 V, 43 A, Rds(on)=7.5 mΩ	IPA075N15N3G
Diode	D_1, D_2, D_3, D_{out}	250 V, 40 A, Vd=0.97 V	MBR40250T
VM capacitors	C_1, C_2, C_3, C_4	60 μF, 250 V, ESR=2.6 mΩ	C4ATDBW5600A3OJ
Output Capacitor	C_{out}	22 uF, 450 V, ESR=6.2 mΩ	B32774D4226

A theoretical loss analysis is performed using the ratings of the selected components of the hardware prototype. The converter is assumed to operate at 200W of output power. The calculated losses include conduction losses in inductors L_1 and L_2 , conduction and switching losses in switches S_1 and S_2 , conduction and reverse recovery losses in diodes, and conduction losses in the ESR of the capacitors. Fig. 12 shows the percentage distribution of losses in the system components. It is observed that the major percent of losses occurs in the diodes which are about 56%. Around 24% and 17% of the losses occur among the inductors and switches, respectively. The losses in the capacitors

are very small as the ESR of the film capacitors used is in the order of few milliohms and the rms currents are around 1A. The calculated efficiency was around 96.8% at 200W.

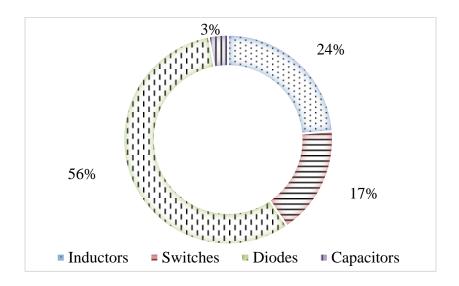


Fig. 12. Percentage distribution of losses in system components

A 400W prototype was built and tested to validate the analytical results. An efficiency of 93.76% was observed at 200W of output power. The difference in the calculated and experimental efficiency can be accounted for the core losses in the inductors that were not considered in the calculated efficiency and the approximate approach to calculating component losses. The efficiency of the prototype over a wide range of output power is shown in Fig. 13. A maximum efficiency of 94.16% was achieved at a power rating of 150W.

The experimental waveforms are shown in Figs. 14-17. The experimental waveforms conform to simulation waveforms. Fig. 14 shows the input current, inductor currents i_{L1} and i_{L2} , and the output voltage of the converter. It can be observed that the input current is continuous and has a smaller ripple compared to that in inductor currents.

The inductor currents are equal and are 180 degrees out of phase from each other as the two phases of the interleaved boost are operated in such way. The output voltage is 400V and the voltage ripple is almost negligible. Fig. 15 shows the inductor currents along with the gate signals of the switches.

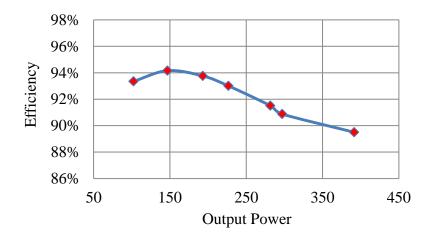


Fig. 13. Efficiency curve of the proposed converter

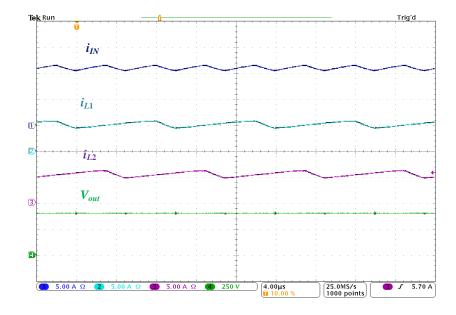


Fig. 14. Input current (i_{IN}) , Inductor currents (i_{L1}, i_{L2}) , and Output Voltage (V_{out})

The voltages of switches S_1 and S_2 are shown in Fig. 16. The turn off voltage of both switches is around 100V as can be calculated from (13). The inductor current waveforms are decreasing during the turn off of their respective switches. The 180 degree out of phase operation of switches S_1 and S_2 can be clearly seen in the switch voltages.

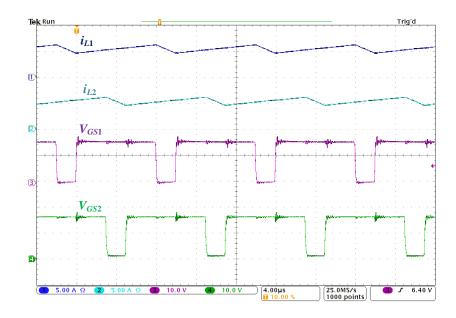


Fig. 15. Inductor currents (i_{L1}, i_{L2}) and Gate voltages (V_{GS1}, V_{GS2})

The reverse blocking voltages of diode D_2 and output diode D_{out} are shown in Fig. 17. The maximum blocking voltage of the diodes is observed to be 200V which is same as that calculated using (15). Also the wave shape of both diodes D_2 and D_{out} voltages are similar because they both are ON during mode I when the switch S_1 is turned OFF. Likewise, the wave shape of voltages of diodes D_1 and D_3 will be similar and have the maximum blocking voltage of 200V for the above test specifications.

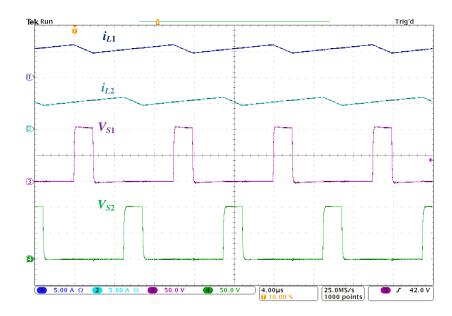


Fig. 16. Inductor currents (i_{L1}, i_{L2}) and Switch voltages (V_{S1}, V_{S2})

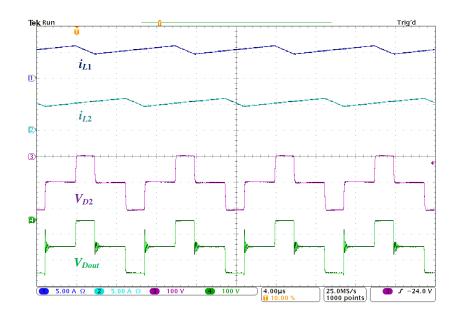


Fig. 17. Inductor currents (i_{L1} , i_{L2}) and Diode voltages (V_{D2} , V_{Dout})

The experimental waveforms provided validate the converter operation and analysis. The proposed converter is capable of providing voltage gains high enough to step up the output voltage of renewable sources to the distribution level 400V DC.

VII. PROPOSED CONVERTER VS. HIGH-VOLTAGE-GAIN TOPOLOGY USING DICKSON CHARGE PUMP VOLTAGE MULTIPLIER CELLS

A comparison between the proposed converter and a high-voltage-gain converter using Dickson charge pump voltage multiplier cells is shown in table III. The high-voltage-gain converter using the Dickson charge pump voltage multiplier cells [19] will be referred to as reference converter in the following sections of the paper (see Fig. 1). Both the converters are almost similar in operation but differ in terms of component stresses. The converters are being compared in terms of component stress and size while both offer a voltage gain of 20, i.e., a 20V input is stepped up to 400V on the output side. Here in this comparison, both converters are sourced from a single source despite the fact that they could be powered from two independent sources.

Both converters achieve a high voltage gain by charging and discharging of the voltage multiplier capacitors. They offer continuous input current which can be owed to the two-phase interleaved boost topology on the input side. The proposed converter is symmetric, i.e., both the interleaved boost phases on the input side experience same voltage and current stresses. Also, some of the capacitors in the voltage multiplier circuit have similar voltage stress. This simplifies the effort and time during component selection of the system design. The switches in the proposed converter have a higher duty ratio as the proposed converter offers slightly lower gain. This leads to a slightly higher voltage stress across the switches compared to the reference topology.

Table III. Comparison of the proposed converter to the reference converter

Component	Parameter	Reference Converter [19]	Proposed Converter
Input	Current	Continuous	Continuous
Inductor	Current	I_{L1} =6 A, I_{L2} =4 A	$I_{L1}=5 \text{ A}, I_{L2}=5 \text{ A}$
Switches	Voltage	$V_{S1}=80 \text{ V}, V_{S2}=80 \text{ V}$	V_{S1} =100 V, V_{S2} =100 V
	Duty Cycle	$D_1 = D_2 = 75\%$	$D_1 = D_2 = 80\%$
	Current	<i>I</i> _{S1} =6 A, <i>I</i> _{S2} =4 A	$I_{S1}=5 \text{ A}, I_{S2}=5 \text{ A}$
VM Capacitors	Capacitance for 1% voltage ripple	C_1 =12.5 μ F, C_2 =6.25 μ F, C_3 =4.17 μ F, C_4 =3.125 μ F	C_1 = C_4 =6.66 μF, C_2 = C_3 =20 μF
	Voltage	V _{C1} =80 V, V _{C2} =160 V, V _{C3} =240 V, V _{C4} =320 V	$V_{C1} = V_{C4} = 150 \text{ V},$ $V_{C2} = V_{C3} = 50 \text{ V}$
Diodes	Voltage	V_{D1} =160 V, V_{D2} =160 V, V_{D3} =160 V, V_{D4} =160 V, V_{Dout} =80 V	V _{D1} =200 V, V _{D2} =200 V, V _{D3} =200 V, V _{Dout} =200 V
Output Capacitor	Capacitance for 1V ripple	C _{out} =1.875 μF	C _{out} =1.875 μF
	Voltage	<i>V_{Cout}</i> =400 V	V _{Cout} =400 V

The major difference in the converters being compared is in their voltage multiplier circuits. Apart from the output capacitor, both the reference converter and proposed converter have four voltage multiplier capacitors. The capacitors in the reference converter have linearly increasing voltage stress as observed from C_1 to C_4 . The voltages of the capacitors C_1 , C_2 , C_3 , and C_4 are 80V, 160V, 240V, and 320V

respectively. For a 1% ripple voltage in the voltage multiplier capacitors, the required capacitance for C_1 , C_2 , C_3 , and C_4 are 12.5 μ F, 6.25 μ F, 4.17 μ F, and 3.125 μ F, respectively. The proposed converter has smaller voltage rating for the voltage multiplier capacitors. Capacitors C_1 , C_4 have a voltage stress of 150V and C_2 , C_3 have a voltage stress of 50V. For a 1% ripple voltage in the voltage multiplier capacitors, the required capacitance for C_1 , C_2 , C_3 , and C_4 are 6.66 μ F, 20 μ F, 20 μ F, and 6.66 μ F, respectively.

The proposed converter has a smaller size compared to the reference topology due to its voltage multiplier circuit capacitors. Ideally, this can be demonstrated by looking at the total energy of the voltage multiplier capacitors which can be calculated as follows.

$$E_{total} = \sum_{n=1}^{4} \frac{1}{2} \times C_n \times V_n^2 \tag{17}$$

The total energy of the voltage multiplier capacitors of the reference converter is 0.4J while that of the proposed converter is 0.2J. It can be seen that the capacitors of the proposed converter hold only 50% of the energy compared to the reference converter. A more practical way to compare the converter size is by looking at the volume of selected voltage multiplier capacitors available in the market. The voltage multiplier capacitors were selected from "KEMET R60-Series Film Capacitors" such that they had the closest capacitance and voltage ratings to what was required. It was observed that the proposed converter had 44% smaller volume of voltage multiplier capacitors compared to the reference converter. Therefore the size of the proposed converter is smaller compared to the reference converter.

The proposed converter has one less diode compared to the reference converter.

All the diodes experience the same reverse blocking voltage of 200V which is slightly

higher than that of the diodes in the reference converter. This is because of the slightly higher duty ratio of the proposed converter compared to the reference converter. As the output ratings are the same, the output capacitors of both the converters are the same.

VIII. CONCLUSION

In this paper, a high-voltage-gain dc-dc converter is introduced that can offer a voltage gain of 20, i.e., to step up a 20V input to 400V output. The proposed converter is based on a two-phase interleaved boost and the modified Dickson charge pump voltage multiplier circuit. It can draw power from a single source as well as from two independent sources while offering continuous input current in both cases. This makes the converter well suited for renewable applications like solar. The proposed converter is symmetric, i.e., the semiconductor components experience same voltage and current stresses which therefore reduces the effort and time spent in the component selection during the system design. The proposed converter has smaller voltage multiplier capacitors compared to a reference converter based on Dickson charge pump voltage multiplier cells; hence it is smaller in size. The converter finds it application in integration of individual solar panels onto the 400V distribution bus in datacenters, telecom centers, dc buildings and microgrids.

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II. A HIGH-VOLTAGE-GAIN DC-DC CONVERTER USING DIODE-CAPACITOR VOLTAGE MULTIPLIER CELLS

Abstract – In this paper, a high-voltage-gain dc-dc converter using diode-capacitor voltage multiplier cells is introduced. The proposed converter offers high voltage gain while benefitting from a simple structure and a low component count. Also, the semiconductor devices experience low voltage stresses. The proposed converter can draw power from a single source as well as from two independent sources. Moreover, it offers continuous input current with low ripple making it appealing in PV solar applications. The operating principle, converter design, and component selection have been discussed with supporting simulation results. A hardware prototype of the proposed converter with a voltage gain of 12 has been developed to validate the analytical results.

I. INTRODUCTION

Low voltage dc systems at 380V have been gaining popularity due to their various benefits including better efficiency, increased reliability, low cost, and simpler integration of renewable energy systems. Such systems have been finding applications in data and telecom centers [1], dc homes [2], dc microgrids [3-9], etc. Also, grid-tied inverter systems [10, 11] have an intermediate 380V dc bus between the energy source (PV panels, fuel cells, etc.) and the inverter. The integration of sustainable and cleaner renewable energy sources like solar and fuel cells into dc systems can be a challenge due to their widely varying voltage range (20V – 45V). The use of classical boost or buckboost converters is not desirable as their voltage gain is limited due to losses in parasitic components at larger duty cycles. Also, the semiconductor devices experience a larger

voltage stress which leads to increased losses. Isolated topologies like flyback, forward, push-pull, half-bridge and full-bridge topologies have discontinuous input currents which would require larger input filter capacitors. Therefore, high voltage dc-dc converters have been investigated for the integration of renewable energy sources.

High voltage gain converters using coupled inductors and transformers have been proposed in [12-17]. Switches in such converters experience high voltage spikes as a result of the energy stored in the leakage inductance of the coupled inductors and transformers. Therefore, they require clamping circuitry to reduce the voltage spikes and improve the converter efficiency by recovering the leakage energy. Also, the leakage inductance reduces the voltage gain of the converter. High voltage gain converters using diode-capacitor voltage multiplier (VM) circuits have been proposed in [18-21]. Dual switch high-voltage-gain dc-dc converters proposed in [18] and [19] have discontinuous input currents and hence would require large input capacitors when used for renewable energy applications. The converter proposed in [20] offers a low voltage gain with high component count. It also requires large inductors to maintain a small input current ripple. A hybrid boosting converter proposed in [21] has a discontinuous input current and a smaller voltage gain.

Non-inverting and inverting diode-capacitor voltage multiplier cells (shown in Fig. 1) have been proposed in [22]. These VM cells have two capacitors C_1 and C_2 that are charged using diodes D_1 and D_2 respectively and discharged through an output diode D_{out} . The load is connected across terminals A and B. These cells are not extendable, i.e., they cannot be connected in series to another to achieve higher voltage gains. A family of single-switch PWM converters based on these diode-capacitor VM cells are also

introduced in [22]. The proposed zeta derived and inverting zeta derived converters offer relatively low voltage gains and hence will not be able to boost a voltage as low as 20V to 380V at a reasonable duty cycle. Also, these converters have a discontinuous input current which is not appealing for renewable applications like solar.

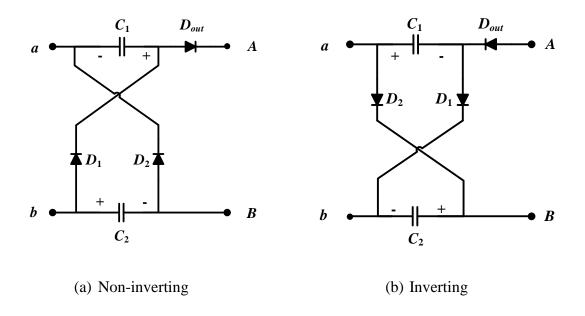


Fig. 1. Diode-capacitor VM cells

In this paper, a high voltage gain dc-dc converter based on non-inverting and inverting diode-capacitor VM cells is proposed. The proposed converter offers high voltage gain while having continuous input current when operating with either a single source or two independent sources. The semiconductor devices experience low voltage stress compared to the high output voltage of the converter. In section II, the proposed converter is introduced and its modes of operation in continuous conduction mode (CCM) are explained. The voltage gain of the proposed converter in CCM with two independent sources and a single source are derived in section III. Section IV analyzes

the component stress of the proposed converter and provides supporting simulation results. Section V discusses the proposed converter operating in discontinuous conduction mode (DCM). Experimental results obtained using developed prototype are presented in section VI. Finally, section VII concludes the paper.

II. PROPOSED CONVERTER AND MODES OF OPERATION

The diode-capacitor VM cell based high-voltage-gain dc-dc converter is introduced (see Figs. 2 and 3) in this section. The proposed converter comprises of two stages – a two-phase interleaved boost stage on the input side and a diode-capacitor VM cell on the output side. The diode-capacitor VM cell could either be a non-inverting diode-capacitor VM cell or an inverting diode-capacitor VM cell. Owing to the symmetry of the converters using non-inverting and inverting VM cells along the horizontal axis, one converter can be obtained by horizontally flipping the other. Therefore, both non-inverting and inverting diode-capacitor VM cells lead to basically one converter. In the next parts of this paper, only the non-inverting diode-capacitor VM cell based converter is analyzed. The proposed converter can operate both in CCM and DCM.

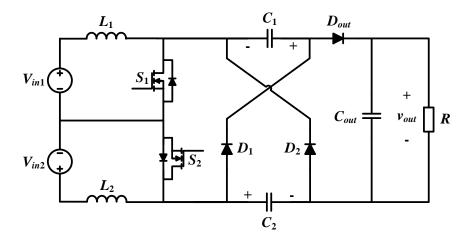


Fig. 2. High-voltage-gain converter using non-inverting diode-capacitor VM cell

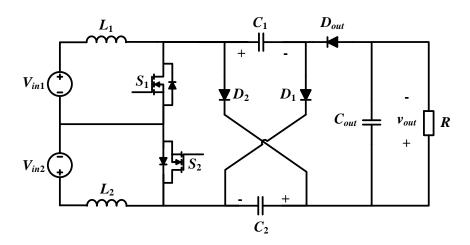


Fig. 3. High-voltage-gain converter using inverting diode-capacitor VM cell

The gating signals of the two-phase interleaved boost stage switches S_1 and S_2 for both CCM and DCM operation are shown in Fig 4. For the proposed converter to operate normally, both switches S_1 and S_2 must have an overlap time when both are ON and also one of the switches must be ON at any point of time. This can be achieved by using duty ratios higher than 50% for both switches and having them operate at 180 degrees out of

phase from each other. As can be seen from Fig. 4, such gate signals lead to three different modes of operation.

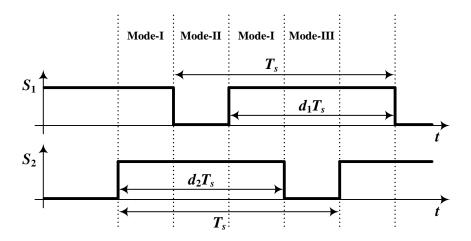


Fig. 4. Interleaved boost switching signals for the proposed converters

A. Mode I

In this mode, both switches S_1 and S_2 of the two-phase interleaved boost stage are ON (see Fig. 5). Input sources V_{in1} and V_{in2} charge inductors L_1 and L_2 . Inductor currents i_{L1} and i_{L2} both increase linearly. Both diodes D_1 and D_2 of the VM cell are reverse biased and are hence OFF. The voltages of the VM cell capacitors remain the same and output diode D_{out} is OFF as it is reverse biased. Therefore, the output capacitor supplies the load.

B. Mode II

In this mode, switch S_1 is OFF and switch S_2 is ON (see Fig. 6). Diodes D_1 and D_2 are OFF as they are reverse biased while output diode D_{out} is ON as it is forward biased. Therefore, VM cell capacitors C_1 and C_2 are in series connection. Inductor current i_{L1}

flows through capacitors C_1 and C_2 discharging them to charge the output capacitor and supply the load.

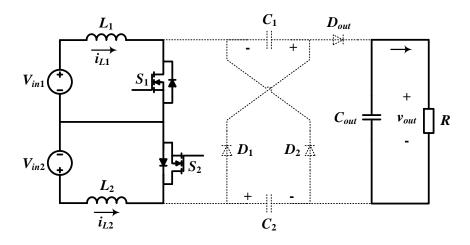


Fig. 5. Converter operation in mode-I

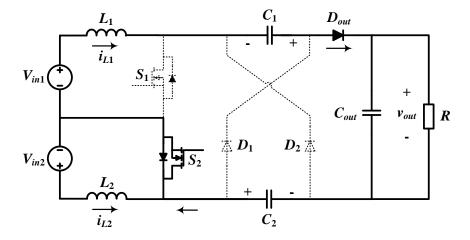


Fig. 6. Converter operation in mode-II

C. Mode III

In this mode, switch S_1 is ON and switch S_2 is OFF (see Fig. 7). Diodes D_1 and D_2 are ON as they are forward biased while output diode D_{out} is OFF as it is reverse biased. Therefore, VM cell capacitors C_1 and C_2 are connected in parallel to each other. Inductor current i_{L2} flows through diode-capacitor VM cell capacitors C_1 and C_2 charging them to a same voltage level while the output capacitor supplies the load.

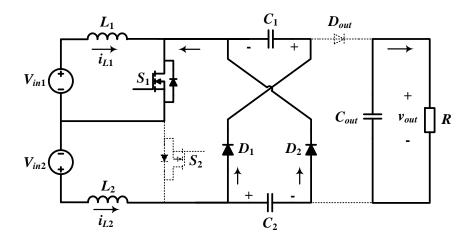


Fig. 7. Converter operation in mode-III

III. VOLTAGE GAIN OF THE PROPOSED CONVERTER

In the proposed converter, the input power is transferred to the output by charging and discharging the diode-capacitor VM cell capacitors. For a non-inverting diode-capacitor VM cell based converter (shown in Fig. 2) operating in CCM, the voltage gain can be derived as follows. Based on volt-second balance, the average voltage across inductors L_1 and L_2 can be written as

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = 0 \tag{1}$$

From Fig. 6, based on the volt-second balance of inductor L_1 , one can write

$$V_{out} - V_{C1} - V_{C2} = \frac{V_{in1}}{(1 - d_1)}$$
 (2)

From Fig. 7, based on the volt-sec balance of the inductor L_2 , one can write

$$V_{C1} = V_{C2} = \frac{V_{in2}}{(1 - d_2)} \tag{3}$$

In the above equation, the authors assume the capacitance of C_1 and C_2 to be identical. If different capacitors are used, the voltages are still the same but with a different ripple. Therefore, the capacitor voltage equations are the same irrespective of their capacitances. A major difference observed using different capacitors is a current spike in the smaller capacitor. This is because the voltage of the smaller capacitor is lesser than the other capacitor (during the start of mode III) as a result of its larger voltage ripple. Therefore, all the inductor current i_{L2} flows through the smaller capacitor until its voltage equals the other capacitor. Once both the voltages become equal, inductor current i_{L2} flows through the capacitors in the inverse ratio of their capacitances, i.e., $i_{C1}/i_{C2} = C_2/C_1$. By substituting (3) in (2), one can derive the output voltage as

$$V_{out} = \frac{V_{in1}}{(1 - d_1)} + \frac{2 \times V_{in2}}{(1 - d_2)} \tag{4}$$

The proposed converter can be supplied from two inputs (see Fig. 2) as well as using only one input source. When a single input is used for the proposed converters, the authors use a switching duty cycle d for both switches S_1 and S_2 and operate them at 180

degrees out of phase form each other. The proposed non-inverting diode-capacitor VM cell converter with single source is shown in Fig. 8. For a single source converter, the diode-capacitor VM cell capacitor voltages and output voltage are written as

$$V_{C1} = V_{C2} = \frac{V_{in}}{(1-d)} \tag{5}$$

$$V_{out} = \frac{3 \times V_{in}}{(1 - d)} \tag{6}$$

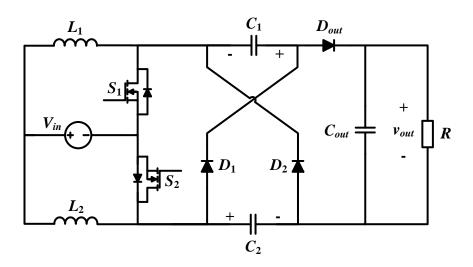


Fig. 8. Non-inverting diode-capacitor VM cell converter using single input source

IV. COMPONENT STRESS AND SIMULATION RESULTS

This section discusses the component stress observed on different components in the non-inverting diode-capacitor VM cell converter with single input source operating in CCM (see Fig. 8). It also provides supporting simulation waveforms of the converter operating in CCM at an output power of 200W (R=792 ohms and d=0.75). All the component stress equations and simulation waveforms presented in this section are under

the assumption of identical capacitances for C_1 and C_2 , unless otherwise specified. The simulation model of the proposed converter has been built in PLECS blockset based off MATLAB. The parameters used in the simulation are given in Table I.

Table I. Simulation parameters

Simulation Parameter	Value
Input Voltage	33 V
Output Voltage	396 V
Switching Frequency f_{sw}	100 kHz
Inductors L_1 and L_2	95 μΗ
VM capacitors	22 μF
Output Capacitor	15 μF

A. Inductor

Inductor current i_{L2} charges capacitors C_1 and C_2 as they are in parallel during mode III. In mode II, inductor current i_{L1} flows through capacitors C_1 and C_2 discharging them in series connection. Therefore, inductor L_2 carries twice the current in inductor L_1 . Average inductor currents i_{L1} and i_{L2} can be calculated as

$$I_{L1,avg} = \frac{I_{out}}{(1-d)} \tag{7}$$

$$I_{L2,avg} = \frac{2 \times I_{out}}{(1-d)} \tag{8}$$

The rms values of inductor currents used to determine copper losses in inductors L_1 and L_2 can be calculated as

$$I_{L1,rms} = \sqrt{\left(\frac{I_{out}}{(1-d)}\right)^2 + \left(\frac{V_{in} \times d}{2\sqrt{3} \times L \times f_{sw}}\right)^2}$$
 (9)

$$I_{L2,rms} = \sqrt{\left(\frac{2 \times I_{out}}{(1-d)}\right)^2 + \left(\frac{V_{in} \times d}{2\sqrt{3} \times L \times f_{sw}}\right)^2}$$
 (10)

The minimum inductances required for L_1 and L_2 to operate in CCM can be calculated as follows.

$$L_{1,\min} = \frac{d(1-d)^2 R}{6f_{sw}} \tag{11}$$

$$L_{2,\min} = \frac{d(1-d)^2 R}{12f_{sw}} \tag{12}$$

The inductance required for a current ripple of ΔI_L is given by

$$L = \frac{V_{in} \times d}{\Delta I_{I} \times f_{sur}} \tag{13}$$

The inductor waveforms obtained from PLECS simulation are shown in Fig. 9. At 200W of output power, inductors L_1 and L_2 carry an average current of 2A and 4A respectively.

B. Input Current

The input source is connected to a two-phase interleaved boost stage. The input current is continuous. The average input current is the sum of inductor currents i_{L1} and i_{L2} . As the two phases of the interleaved boost are 180 degrees out of phase from each other, the input current ripple is further reduced. This greatly reduces the size of the input filter capacitor required for the converter. The input current ripple can be calculated as

$$\Delta I_{L} = \left(\frac{V_{in} \times d}{L \times f_{sw}}\right) \left(\frac{2\left(d - \frac{m}{2}\right)\left(\frac{m+1}{2} - d\right)}{d(1-d)}\right)$$
(14)

where m = floor(2d). The first term in (14) represents the normal inductor current ripple while the second term represents the ripple cancelation due to interleaving operation. The input current waveform of the proposed converter operating at 200W is shown in Fig. 9.

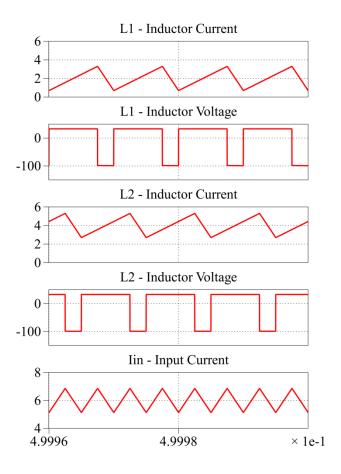


Fig. 9. Inductor current and voltages, input current

C. Switches

In the proposed converter, maximum voltage across switches S_1 and S_2 is observed during modes II and III, respectively. From Figs. 6 and 7, the voltage across switches S_1 and S_2 can be written as

$$V_{S1} = V_{out} - V_{C1} - V_{C2} \tag{15}$$

$$V_{S2} = V_{C1} = V_{C2} \tag{16}$$

Substituting (5) and (6) in (15) and (16), the switch blocking voltages can be calculated as.

$$V_{S1} = V_{S2} = \frac{V_{in}}{(1-d)} \tag{17}$$

The maximum voltage across the switches is only one-third of the output voltage. As the currents in the two inductors are not identical, the current stress seen by both switches are different as well. The average switch currents can be calculated using (18) and (19). The rms switch currents used in the calculation of the conduction losses are calculated using (20) and (21). In the switch average and rms current derivations, only the average values of switch currents during different modes of operation are considered and the ripple is neglected.

$$I_{S1,avg} = \left(\frac{3d-1}{1-d}\right)I_{out}$$
 (18)

$$I_{S2,avg} = \left(\frac{3d - 0.5}{1 - d}\right) I_{out} \tag{19}$$

$$I_{S1,rms} = \left(\sqrt{\frac{8-7d}{(1-d)^2}}\right) I_{out}$$
 (20)

$$I_{S2,rms} = \left(\sqrt{\frac{5-d}{(1-d)^2}}\right) I_{out}$$
 (21)

The switch waveforms of the proposed converter are shown in Figs. 10 (a) and (b). Switches S_1 and S_2 in the two-phase interleaved boost stage see different current stress but the same voltage stress as can also be seen in the simulation waveforms. Since the converter in simulation is operating at 75% switching duty cycle with a 33V input, the maximum voltage stress seen on both the switches is 132V. Switches S_1 and S_2 carry an average current of 2.5A and 3.5A, respectively.

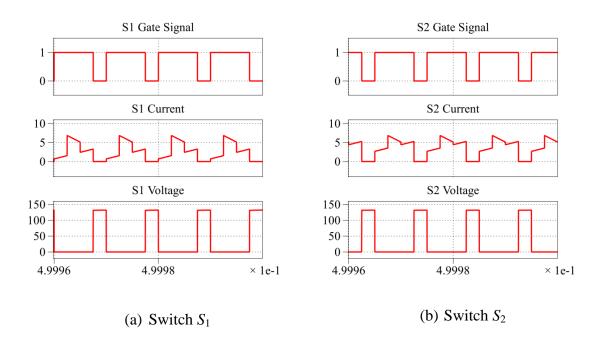


Fig. 10. Switch gate signal, current, and voltage waveforms

D. Diodes

The maximum blocking voltages of the diodes can be determined from the different modes of operation. Both diodes D_1 and D_2 experience a maximum voltage stress across them during mode II. They can be written as

$$V_{d1} = V_{C1} + \frac{V_{in}}{(1-d)} \tag{22}$$

$$V_{d2} = V_{C2} + \frac{V_{in}}{(1-d)} \tag{23}$$

The output diode experiences a maximum blocking voltage during mode III. It can be written as

$$V_{dout} = V_{out} - V_{C1} = V_{out} - V_{C2}$$
 (24)

Substituting (5) and (6) in (22), (23), and (24), we can calculate the diode blocking voltages as

$$V_{d1} = V_{d2} = V_{dout} = \frac{2 \times V_{in}}{(1 - d)}$$
 (25)

From (25), it can be seen that all the diodes of the converter experience the same blocking voltage. All the diodes experience a blocking voltage which is only two-thirds the output voltage. The diode average and rms currents used in the calculation of losses are given by

$$I_{d1,avg} = I_{d2,avg} = I_{dout,avg} = I_{out}$$
 (26)

$$I_{d1,rms} = I_{d2,rms} = \sqrt{\left(\frac{1-d}{4}\right) \left[\left(\frac{2 \times I_{out}}{(1-d)}\right)^{2} + \frac{1}{12}\left(\frac{V_{in} \times d}{L \times f_{sw}}\right)^{2}\right]}$$
 (27)

$$I_{dout,rms} = \sqrt{(1-d)\left[\left(\frac{I_{out}}{(1-d)}\right)^2 + \frac{1}{12}\left(\frac{V_{in} \times d}{L \times f_{sw}}\right)^2\right]}$$
 (28)

In the above diode current equations, the authors assume capacitors C_1 and C_2 to be equal. In cases where different capacitances are used for C_1 and C_2 , the average current equations of all diodes and the rms current equation of output diode will still remain the same. Only the rms current equations of diodes D_1 and D_2 will slightly vary due to the current spikes in them. Therefore, the above rms current equations of diodes D_1 and D_2 can still be used to approximate the losses. As the authors are assuming the capacitors to be identical, all the diodes experience same voltage and current stress. Therefore, a similar type of diode can be used for all of them. The voltage waveforms of diodes D_1 , D_2 , and D_{out} of the proposed converter are shown in Fig. 11. For the converter operating at 75% switching duty cycle and 33V input, the maximum blocking voltage seen by the diodes is 264V.

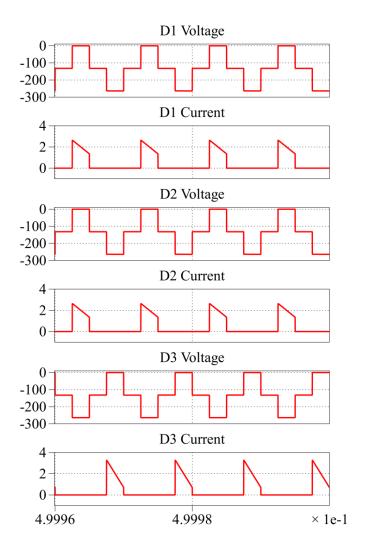


Fig. 11. Diode voltage and current waveforms

E. Capacitor Sizing

The proposed converter has three capacitors, two VM cell capacitors and one output capacitor. These capacitors are sized based on the amount of voltage ripple that can be allowed in them. To maintain a voltage ripple of ΔV_C in VM cell capacitors C_1 and C_2 , the capacitance required can be calculated as follows.

$$C_1 = C_2 = \frac{V_{out}}{R \times f_{sw} \times \Delta V_C} \tag{29}$$

The output capacitance required to have a voltage ripple of ΔV_O is calculated as

$$C_{out} = \frac{d \times V_{out}}{R \times f_{sw} \times \Delta V_O}$$
 (30)

In the simulation, capacitances of $22\mu\text{F}$, $22\mu\text{F}$, and $15\mu\text{F}$ have been used for C_1 , C_2 , and C_{out} , respectively to have a voltage ripple of less than or equal to 0.25V.

V. PROPOSED CONVERTER OPERATING IN DCM

Over a wide load range, the proposed converter may operate in both CCM and DCM. There is also an intermediate mode where only one of the inductor currents is discontinuous. This intermediate mode will be referred to as partial DCM or PDCM. A well designed converter with equal inductances for L_1 and L_2 will operate in CCM during full load conditions. As the load power starts to decrease (or load resistance increases), the converter will operate in partial DCM. In this mode, only the current of inductor L_1 will be discontinuous as it carries only half the current in L_2 . As the load power further decreases, the converter will operate in DCM where both inductor currents reach zero at some point during the switching cycle.

The boundary conditions for the proposed converter to operate in CCM are given using (11) and (12). For a selected value of L for inductances L_1 and L_2 , inductor current in L_1 will first turn discontinuous as the load power starts to decrease. The load resistance at which the proposed converter enters partial DCM can be calculated as

$$R_{Critical_PDCM} = \frac{6 \times L \times f_{sw}}{d(1-d)^2}$$
(31)

For the converter specifications given in Table-I, the proposed converter is at the boundary of CCM and partial DCM at a load resistance of 1,216 ohms. When the proposed converter is operating in partial DCM, the voltages of VM cell capacitors C_1 and C_2 are unchanged as the current of inductor L_2 is still continuous. They can be calculated using (5). The output voltage however is different and is derived as

$$V_{out_PDCM} = \frac{\left(V_{in} + V_{C1} + V_{C2}\right) + \sqrt{\left(V_{in} + V_{C1} + V_{C2}\right)^2 + \left(\frac{2 \times d^2 \times V_{in}^2 \times R}{L \times f_{sw}}\right)}}{2}$$
(32)

Substituting (5) in (32), the output voltage equation is written as

$$V_{out_PDCM} = \frac{\left(V_{in} + \frac{2V_{in}}{1 - d}\right) + \sqrt{\left(V_{in} + \frac{2V_{in}}{1 - d}\right)^{2} + \left(\frac{2 \times d^{2} \times V_{in}^{2} \times R}{L \times f_{sw}}\right)}}{2}$$
(33)

As the load power starts to further decrease, the converter will enter into DCM.

The critical resistance at which the converter enters DCM can be calculated as

$$R_{Critical_DCM} = \frac{4 \times L \times f_{sw} \times V_{out_PDCM}}{V_{in} \times d \times (1 - d)}$$
(34)

For the specifications given in Table-I, the proposed converter is at the boundary of partial DCM and DCM at a load resistance of 2,140 ohms. Therefore, the simulated converter stays in partial DCM between a load resistance of 1,216 and 2,140 ohms. For loads lesser than 1,216 ohms, it operates in CCM and for loads above 2,140 ohms, it

operates in DCM. When the proposed converter operates in DCM, the output voltage and the VM cell capacitor voltages can be calculated as

$$V_{out_DCM} = \frac{3V_{in} + \sqrt{(3V_{in})^2 + \left(\frac{4 \times d^2 \times V_{in}^2 \times R}{L \times f_{sw}}\right)}}{2}$$
(35)

$$V_{C1_DCM} = V_{C2_DCM} = \frac{d^2 \times V_{in}^2 + \left(\frac{4 \times L \times f_{sw} \times V_{out_DCM} \times V_{in}}{R}\right)}{\left(\frac{4 \times L \times f_{sw} \times V_{out_DCM}}{R}\right)}$$
(36)

For the proposed converter with two sources, partial DCM and DCM should be avoided as much as possible in order to avoid the input current being discontinuous. Even in the single source case, the input current can be discontinuous at low loads. Therefore, the proposed converter must be designed such that the converter operates in CCM for a wide range of load variations.

VI. EXPERIMENTAL RESULTS

A hardware prototype was built to test and validate the operation of the proposed non-inverting diode-capacitor VM cell converter. The specifications of the components used for building the hardware prototype are given in Table II. The power rating of the converter is 200W with an input voltage of 33V and an output voltage of 396V. The proposed converter is tested at a switching frequency of 100 kHz. A theoretical loss analysis is performed using the ratings of the selected components of the hardware prototype. The converter is assumed to operate at 200W of output power. The calculated

losses include conduction losses in inductors L_1 and L_2 , conduction and switching losses in switches S_1 and S_2 , conduction and reverse recovery losses in all diodes, and conduction losses in the ESR of all capacitors. Fig. 12 shows the percentage distribution of losses in the system components. It is observed that the major percentage of losses occur in the diodes which is about 80%. As all diodes are identical and they experience same voltage and current stresses, the losses can be equally distributed among them, i.e., 26.67% in each diode. Around 7% and 13% of the losses occur among the inductors and switches, respectively. The losses in the capacitors are very small as the ESR of film capacitors is in the order of few milliohms and the rms currents are around 1A.

Table II. Component specifications of the hardware prototype

Component	Name	Rating	Part No
Inductor	L_1,L_2	95 μH DCR≈11mΩ	ETD-49 A250 core 21 turns
MOSFET	S_1, S_2	150 V, 43 A Rds(on)=7.5 mΩ	IPA075N15N3G
Diode	D_1, D_2, D_{out}	600 V, 15 A Vf=0.73 V@0.5 A, Rd=0.0625 Ω Irr = 3 A, Trr=60 ns	MURF1560G
VM capacitors	C_1, C_2	22 uF, 250 V ESR= 5 mΩ	EPCOS B32796E2226K
Output Capacitor	C_{out}	15 uF, 450 V ESR=2.8 mΩ	C4ATGBW5150A3LJ

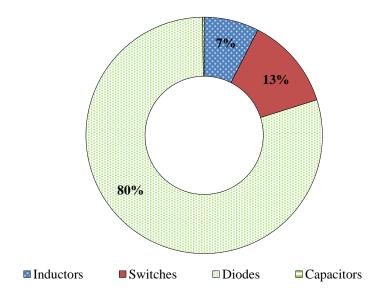


Fig. 12. Percentage distribution of losses in system components

The hardware prototype was tested at 200W of output power and an efficiency of 94.05% was observed. The efficiency plot of the hardware prototype is shown in Fig. 13. A maximum efficiency of 94.33% was observed at an output power of 175W. The experimental waveforms of the converter operating at 200W in CCM are shown in Fig. 14. The experimental waveforms conform to the simulation waveforms. Fig. 14 (a) shows the input current, inductor currents i_{L1} and i_{L2} , and also the output voltage. Inductor currents i_{L1} and i_{L2} are at 2A and 4A respectively. The input current is the sum of both the inductor currents. It can be observed that the input current is continuous and has a smaller ripple compared to that of inductor currents. The output voltage is observed to be 396V.

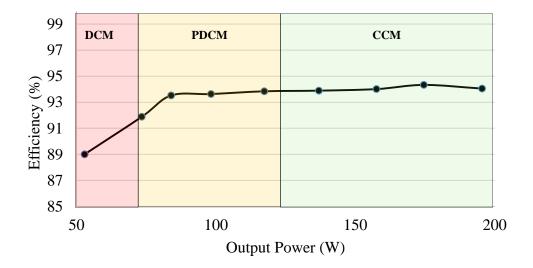
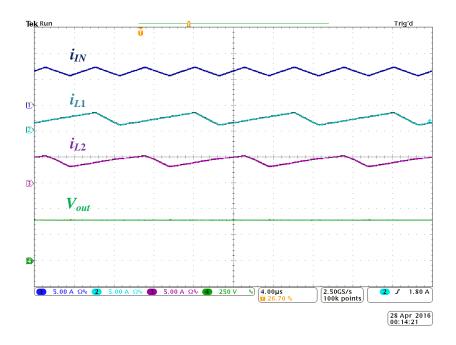
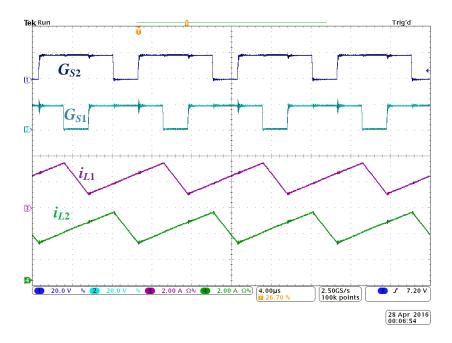


Fig. 13. Efficiency vs. output power

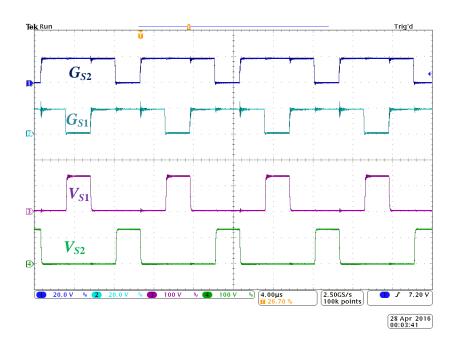


14 (a) Input current, Inductor currents, and Output Voltage

Fig. 14. Waveforms of the proposed converter operating in CCM at 200W

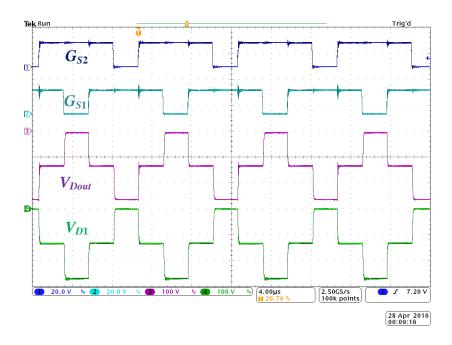


14 (b) Switching signals and Inductor currents



14 (c) Switching signals and switch voltages

Fig.14. Waveforms of the proposed converter operating in CCM at 200W (Contd..)



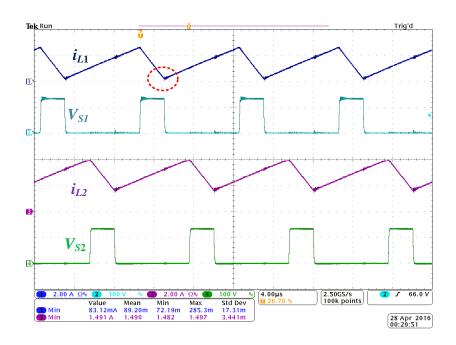
14 (d) Inductor currents and Diode D₁, D_{out} voltages

Fig.14. Waveforms of the proposed converter operating in CCM at 200W (Contd..)

Fig. 14 (b) shows the switching signals and inductor currents. The inductor currents are decreasing during the turn off of their respective switches. The voltage waveforms of switches S_1 and S_2 are shown in Fig. 14 (c). The turn off voltage of both switches is 132V. Also, the 180 degree out of phase operation of switches S_1 and S_2 can be seen in the switch voltages. The reverse blocking voltages of diodes D_2 and D_{out} are shown in Fig. 14 (d). The maximum blocking voltage of the diodes is observed to be 264V. Voltages of diodes D_1 and D_{out} are 180 degrees out of phase from each other because D_1 conducts when switch S_2 is OFF and D_{out} conducts when switch S_1 is OFF. The experimental waveforms validate the converter operation and analysis.

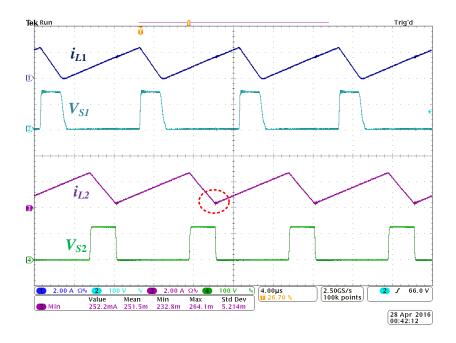
The converter waveforms at the boundaries of CCM, PDCM, and DCM are shown in Fig. 15. In Fig. 15 (a), it can be seen that the minimum of inductor current i_{L1} is

close to zero (83mA) while the minimum of inductor current i_{L2} is 1.491A. Therefore, at 1,261 ohms, the converter is operating close to the boundary of CCM and PDCM. Similarly in Fig. 15 (b), the minimum of inductor current i_{L1} is at zero while the minimum of inductor current i_{L2} is close to zero (252mA). Therefore, at 2,172 ohms, the converter is operating close to the boundary of PDCM and DCM. The load values at the boundary conditions are close to the values obtained from the analysis in section V.



15 (a) Boundary of CCM and PDCM at 1,261ohms

Fig. 15. Proposed converter at boundary conditions



15 (b) Boundary of PDCM and DCM at 2,172ohms

Fig.15. Proposed converter at boundary conditions (Contd..)

VII. CONCLUSION

In this paper, a high-voltage-gain dc-dc converter is introduced. The proposed converter offers high voltage gain while having a simple structure with low component count. The converter structure has two stages - a two-phase interleaved boost stage on the input and a non-inverting or inverting diode-capacitor VM cell on the output side. With the two-phase interleaved boost on its input side, the converter is capable of drawing power from a single source or two independent sources while offering continuous input current in both cases. Owing to the symmetric nature of the non-inverting and inverting diode-capacitor VM cells, the proposed converter can be obtained using either of the VM cells. The semiconductor devices experience low voltage stress compared to the output voltage. The switches and diodes experience only $1/3^{\rm rd}$ and $2/3^{\rm rd}$ of the output voltage,

respectively. The component stresses and voltage gain of the converter have been verified using both simulation and hardware results. The boundary conditions of the proposed converter to operate in CCM, PDCM, and DCM have also been verified. This converter can be utilized for the integration of solar panels and fuel cells onto a 400V dc bus.

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III.A FAMILY OF HIGH-VOLTAGE-GAIN DC-DC CONVERTERS BASED ON A GENERALIZED STRUCTURE

Abstract – A family of high-voltage-gain dc-dc converters is introduced in this paper. The proposed family of converters has been deduced from a generalized structure with two stages. On the input side, a two-phase interleaved boost stage boosts the input dc voltage to output a modified square wave voltage on the second stage. This output of the interleaved boost stage is further multiplied and rectified using a voltage multiplier stage. As a result, a high voltage gain is achieved using the proposed converters. The two-phase interleaved boost stage on the input side makes it possible for the converters to be operated using a single source or two independent sources. In a single source is used, the input current drawn is continuous with a small ripple. Owing to its generalized structure, the proposed family of converters comprises of both non-isolated and isolated converters with high voltage gain. The high voltage gain and continuous input current make these converters appealing in applications like the integration of renewable sources such as solar, fuel cells, etc., on to a 400V dc bus.

I. INTRODUCTION

High voltage gain dc-dc converters have been in use in many industry applications. In the past, they have been mainly used for powering high intensity discharge (HID) lamps in automotive headlamps and integrating the 48V dc battery plant onto the intermediate 380V dc bus of uninterruptible power supplies (UPS) in telecommunication centers [1, 2]. Over the last decade, these converters have been gaining popularity for the integration of renewable energy sources [3-7]. Renewable

sources such as solar modules and fuel cells provide low voltage dc at their outputs typically in the range of 20V to 45V. Applications like dc distribution systems [8, 9], dc microgrids [10, 11], and solid state transformer [12, 13] include a 380V dc bus. Also, a higher voltage dc input is preferred for a grid tied ac-dc inverter [14]. The integration of low voltage renewable sources onto the higher voltage dc bus is challenging. Use of classical boost and buck-boost converters to integrate such low voltage sources to a high voltage dc bus is not possible as the losses in their parasitics limit the voltage gain at larger duty cycles. Also, their semiconductor devices are subjected to higher voltage stress and reverse recovery problems. Isolated topologies such as flyback, forward, pushpull, half-bridge, and full-bridge converters have discontinuous input currents which make them unsuitable for renewable energy applications like solar. Therefore, they would require larger input filter capacitors which would lead to increased converter size and reduced reliability.

Many non-isolated and isolated high voltage gain dc-dc converters have been proposed in [3-7, 12-31] for the integration of renewable energy sources and energy storage devices. Few other high-voltage-gain converters have been proposed in [32-35]. All these high-voltage-gain converters use a boost stage in combination with voltage multiplier circuits. The boost circuit or voltage multiplier circuit in some involves either a coupled inductor or a transformer or both to achieve even higher voltage gains. A classification of non-isolated boost-based dc-dc converters has been presented in [36]. The step-up topologies with wide conversion ratio have been mainly classified into five types. They are - (1). Cascaded boost converters, (2). Coupled-inductor based boost converters, (3). Switched-capacitor based boost converters, (4). Interleaved boost

converters and (5). Three-state switching cell (3-SSC) based converters. This classification gives a better picture on how most of high voltage gain converters are built. The main features that the converter has to offer for use in renewable energy and energy storage applications are high voltage gain, high efficiency, continuous input current, and low device stress. Most converters can only offer a few of these features making them less appealing for such applications.

In this paper, a family of high-voltage-gain dc-dc converters is proposed. The proposed family of converters has a generic structure – a two-phase interleaved (TPI) boost stage on the input side and a voltage multiplier (VM) stage on the output side. Based on the construction of its TPI boost stage, the members of the proposed family of converters can be classified into non-isolated and isolated topologies. These converters offer high voltage gain with continuous input current and low semiconductor voltage stresses. The proposed family of converters is suitable for applications like integration of renewable energy sources. In section II, the generalized structure of proposed family of converters is discussed. Section III classifies the proposed family of converters based on the input side TPI boost stage. Few of the earlier cited high-voltage-gain dc-dc converters are members of the proposed family of converters. They will be referred to when different TPI boost stages are discussed in detail. The VM stage and few possible solutions have been described in section IV. Section V discusses the practical converter considerations for the proposed family of converters. An example converter derived using the generalized structure is discussed and analyzed with supporting hardware results in section V. Section VI concludes the paper.

II. GENERALIZED STRUCTURE OF THE PROPOSED FAMILY OF CONVERTERS

The uniqueness of the proposed family of converters is the generalized structure used in building them. Generalized structure of the proposed family of converter is shown in Fig. 1. As can be seen from the figure, the generic structure of the proposed family of converters has two stages. The first stage is a TPI boost stage on the input side. The second stage is a VM stage on the output side. The main link between the two stages is the intermediate voltage between them (V_{AB} in Fig. 2). This intermediate voltage is obtained by switching switches S_1 and S_2 of the two-phase interleaved boost stage at duty cycles d_1 and d_2 , respectively. The intermediate voltage is similar to the modified square wave (MSW) voltage output of a single phase inverter.

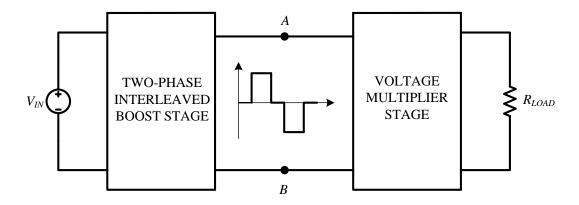


Fig. 1. Generalized structure of the proposed family of converters with single source

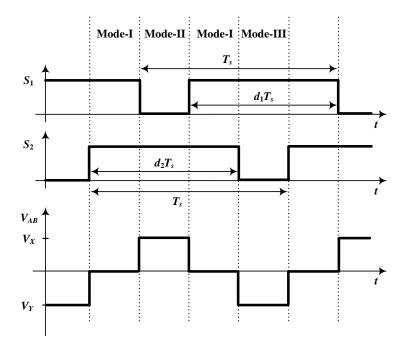


Fig. 2. Switching pulses (S_1 and S_2) and MSW voltage (V_{AB})

The TPI boost stage converts the dc voltage of the source to an MSW voltage. For the TPI boost stage to do so, one cannot keep both S_1 and S_2 off at the same time as the converter will violate Kirchhoff's law. Therefore, one of the two switches must be ON at all times. In case a symmetric operation is desired, S_1 and S_2 can be commanded with similar duty cycles with 180 degrees of phase shift (see Fig. 2). d_1 and d_2 are the corresponding duty cycles for S_1 and S_2 , and S_3 is the switching time period. As can be seen from Fig. 2, one of switches S_1 and S_2 is ON at any point of time. Such switching pulses result in three modes of operation. The MSW voltage output of the TPI boost stage is rectified and further boosted by the VM stage to provide a high voltage dc at its output. This is done through charging and discharging of its capacitors during modes II and III of operation.

The MSW voltage (V_{AB} in Fig. 2) has two voltage peaks – a positive peak V_X and a negative peak V_Y . The positive peak V_X is the voltage across terminals A and B during mode-II, i.e., switch S_1 is OFF and switch S_2 is ON. The negative peak V_Y is the voltage across terminals A and B during mode-III, i.e., switch S_1 is ON and switch S_2 is OFF. The voltage across terminals A and B during mode-I is preferred to be zero. Cases with a possibility of a non-zero voltage across terminals A and B during mode-I will be discussed in detail in section III.

III. TWO-PHASE INTERLEAVED (TPI) BOOST STAGE

The first stage of the proposed family of converters is a TPI boost stage. As there are two phases of boost on the input side, the converter can either be powered from a single source or two different sources. The TPI boost stage can be further enhanced to provide higher voltage gains by using coupled inductors and transformers. It also makes it possible to achieve galvanic isolation in the converter. Based on the construction of the TPI boost stage, the proposed family of converters has been classified as shown in Fig. 3. The family of converters is mainly classified into non-isolated and isolated converters. It can be observed from the classification that there are six ways to implement the TPI boost stage. Each of these implementations is discussed in this section of the paper.

The discussions that follow analyze the two-source TPI boost stage and then modify it for a single source TPI boost stage with both switches operating at same duty cycle 'd'. For the TPI boost stage to generate an MSW voltage output, the switches should follow the switching condition discussed in section II, i.e., both switches cannot be OFF at the same time. The following analysis of the ideal TPI boost stages is under the

assumption that the inductors and coupled inductors are selected such that they operate in continuous conduction mode (CCM). The voltage derivations presented are based on volt-sec balance of the inductors. The continuity of input currents when operating with two sources and a single source are also discussed.

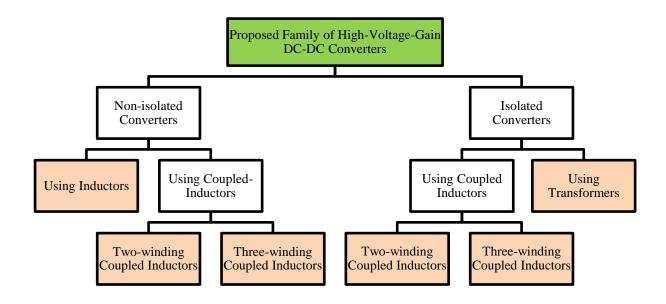


Fig. 3. Classification of proposed family of high-voltage-gain dc-dc converters

A. Non-isolated TPI Boost Stage

The non-isolated TPI boost stage in the proposed family of converters is classified into two types – one using inductors and the other using coupled inductors. The TPI boost stage using coupled inductors is further classified based on the number of windings in the coupled inductor. In this paper, only two-winding and three-winding coupled inductors have been considered as increasing the number of windings increases the size and makes the design more complicated.

1) Non-isolated TPI boost stage using inductors

This is the most basic implementation of the TPI boost stage (see Fig. 4). This stage outputs an MSW voltage at terminals A and B. For a two source TPI boost stage shown in Fig. 4(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltages V_A , V_B , and V_{AB} can be written as

$$V_A = 0, V_B = 0$$
 (1)

$$V_{AB} = V_A - V_B = 0 \tag{2}$$

From (2), it can be seen that the voltage across terminals A and B during mode I is zero. In mode II, voltages V_A , V_B , and V_X can be written as

$$V_A = \frac{V_{in1}}{1 - d_1}, \ V_B = 0 \tag{3}$$

$$V_X = V_A - V_B = \frac{V_{in1}}{1 - d_1} \tag{4}$$

In mode III, voltages V_A , V_B , and V_Y can be written as

$$V_A = 0, \ V_B = \frac{V_{in2}}{1 - d_2} \tag{5}$$

$$V_Y = V_B - V_A = \frac{V_{in2}}{1 - d_2} \tag{6}$$

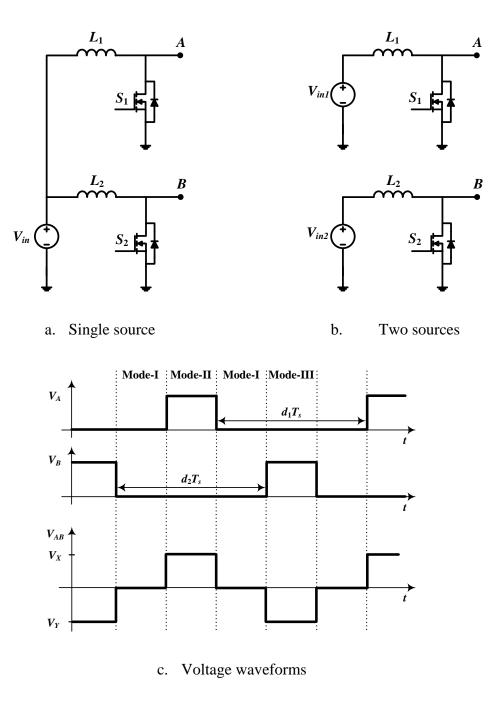


Fig. 4. Non-isolated TPI boost stage using inductors

For a single source TPI boost stage with both switches operating at switching duty cycle d, voltage equations V_X and V_Y can be written as

$$V_X = V_Y = \frac{V_{in}}{1 - d} \tag{7}$$

The input current for this TPI boost stage is continuous in both the two source and single source cases. As both switches are operating 180 degrees out of phase from each other, the input current ripple in the single source case is even smaller. One can couple the inductor based TPI boost stage to different VM stages to achieve higher voltage gains. In such converters, the output voltage gain is mainly dependent on the gain of the VM stage as the peak of the MSW voltage is limited by the duty cycle. Non-isolated TPI boost stage using inductors has been used in converters proposed in [18, 21, 23, 32, 37].

2) Non-isolated TPI boost stage using two-winding coupled inductors

The MSW output voltage of the TPI boost stage using inductors is limited by the duty cycle of the switches. One way to further enhance the voltage is by using coupled inductors. A two-winding coupled inductor based TPI boost stage is shown in Fig. 5. For a two source TPI boost stage shown in Fig. 5(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltages V_A , V_B , and V_{AB} can be written as

$$V_{A} = -\left(\frac{N_{21}}{N_{11}}\right)V_{in1}, V_{B} = -\left(\frac{N_{22}}{N_{12}}\right)V_{in2}$$
 (8)

$$V_{AB} = V_A - V_B = \left(\frac{N_{22}}{N_{12}}\right) V_{in2} - \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
 (9)

In mode II, voltages V_A , V_B , and V_X can be written as

$$V_{A} = \frac{V_{in1}}{1 - d_{1}} + \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_{1}} - V_{in1} \right), V_{B} = -\left(\frac{N_{22}}{N_{12}} \right) V_{in2}$$
 (10)

$$V_X = V_A - V_B = \frac{V_{in1}}{1 - d_1} + \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right) - \left(\frac{N_{21}}{N_{11}} \right) V_{in1} + \left(\frac{N_{22}}{N_{12}} \right) V_{in2}$$
(11)

In mode III, voltages V_A , V_B , and V_Y can be written as

$$V_{A} = -\left(\frac{N_{21}}{N_{11}}\right)V_{in1}, V_{B} = \frac{V_{in2}}{1 - d_{2}} + \frac{N_{22}}{N_{12}}\left(\frac{V_{in2}}{1 - d_{2}} - V_{in2}\right)$$
(12)

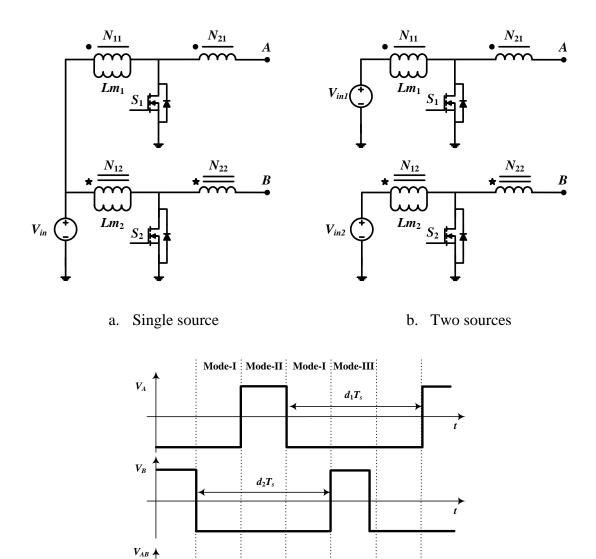
$$V_{Y} = V_{B} - V_{A} = \frac{V_{in2}}{1 - d_{2}} + \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right) - \left(\frac{N_{22}}{N_{12}}\right) V_{in2} + \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
(13)

In equations (8) to (13), N_{11} and N_{21} are the turns in the primary and secondary windings of coupled inductor L_{m1} , respectively. Also, N_{12} and N_{22} represent the turns in the primary and secondary windings of coupled inductor L_{m2} , respectively. On a closer observation, the sum of the last two terms in (11) and (13) is equal to voltage V_{AB} in mode-I shown in (9). If the coupled inductors turns ratio are selected such that voltage V_{AB} is zero in mode-I, (11) and (13) can be further simplified as

$$V_X = \frac{V_{in1}}{1 - d_1} + \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right) \tag{14}$$

$$V_{Y} = \frac{V_{in2}}{1 - d_{2}} + \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right)$$
 (15)

As the MSW voltage peaks are dependent on the coupled inductor turns-ratio, higher peaks can be achieved using higher turns-ratio.



c. Voltage waveforms

Fig. 5. Non-isolated TPI boost stage using two-winding coupled inductors

For a single source TPI boost stage (shown in Fig. 5(a)) with both its switches operating at duty cycle d, the MSW peak voltage equations can be simplified as

$$V_X = V_Y = (n+1)\frac{V_{in}}{1-d}$$
 (16)

where the turns ratio in the two-winding coupled inductors is assumed as follows.

$$n = \frac{N_{21}}{N_{11}} = \frac{N_{22}}{N_{12}} \tag{17}$$

From (7) and (16), it can be observed that the two-winding coupled inductor TPI boost stage provides an MSW voltage whose peak value is 'n' times more than the peak voltage obtained using inductor based TPI boost stage. The additional boost in the voltage is provided by the combination of secondary coils of both coupled inductors. Some high voltage gain converters based on the above mentioned TPI boost stage have been proposed in [38].

If two sources are used, the input currents drawn from the two sources are discontinuous. However with a single source, continuous input current is drawn from the source owing to the ripple cancellation due to the phase delay between the two switches. A non-zero voltage V_{AB} during mode-I appears as a dc bias on the MSW voltage. This dc bias causes discontinuity in the input current of the TPI boost stage with a single source making it unsuitable for renewable energy applications. Therefore, voltage V_{AB} during mode-I is desired to be zero. This can be achieved by selecting appropriate values of turns-ratio for the coupled inductors. The input current can also be discontinuous in the single source case if the output capacitor in the VM stage is connected to ground.

3) Non-isolated TPI boost stage using three-winding coupled inductors

In cases where the secondary coil of the coupled inductor is not sufficient to achieve the voltage boost, one can add more windings to the coupled inductor. The tertiary winding of the coupled inductor will be used just like the secondary winding and

is shown in Figs. 6(a) and (b). For a two source TPI boost stage shown in Fig. 6(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltages V_A , V_B , and V_{AB} can be written as

$$V_{A} = \left(\frac{N_{32}}{N_{12}}\right) V_{in2} - \left(\frac{N_{21}}{N_{11}}\right) V_{in1}, V_{B} = \left(\frac{N_{31}}{N_{11}}\right) V_{in1} - \left(\frac{N_{22}}{N_{12}}\right) V_{in2}$$
(18)

$$V_{AB} = V_A - V_B = \left(\frac{N_{32} + N_{22}}{N_{12}}\right) V_{in2} - \left(\frac{N_{31} + N_{21}}{N_{11}}\right) V_{in1}$$
(19)

In mode II, voltages V_A , V_B , and V_X can be written as

$$V_{A} = \frac{V_{in1}}{1 - d_{1}} + \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_{1}} - V_{in1} \right) + \left(\frac{N_{32}}{N_{12}} \right) V_{in2}$$
 (20)

$$V_{B} = -\frac{N_{31}}{N_{11}} \left(\frac{V_{in1}}{1 - d_{1}} - V_{in1} \right) - \left(\frac{N_{22}}{N_{12}} \right) V_{in2}$$
 (21)

$$V_X = V_A - V_B = \frac{V_{in1}}{1 - d_1} + \left(\frac{N_{31} + N_{21}}{N_{11}}\right) \frac{V_{in1}}{1 - d_1} - \left(\frac{N_{31} + N_{21}}{N_{11}}\right) V_{in1} + \left(\frac{N_{32} + N_{22}}{N_{12}}\right) V_{in2}$$
(22)

In mode III, voltages V_A , V_B , and V_Y can be written as

$$V_{A} = -\frac{N_{32}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}} - V_{in2} \right) - \left(\frac{N_{21}}{N_{11}} \right) V_{in1}$$
 (23)

$$V_{B} = \frac{V_{in2}}{1 - d_{2}} + \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}} - V_{in2} \right) + \left(\frac{N_{31}}{N_{11}} \right) V_{in1}$$
(24)

$$V_{Y} = V_{B} - V_{A} = \frac{V_{in2}}{1 - d_{2}} + \left(\frac{N_{32} + N_{22}}{N_{12}}\right) \frac{V_{in2}}{1 - d_{2}} - \left(\frac{N_{32} + N_{22}}{N_{12}}\right) V_{in2} + \left(\frac{N_{31} + N_{21}}{N_{11}}\right) V_{in1}$$
(25)

In equations (18) - (25), N_{11} , N_{21} , and N_{31} are the turns in the primary, secondary, and tertiary windings of coupled inductor L_{m1} , respectively. Also, N_{12} , N_{22} , and N_{32} are

the turns in the primary, secondary, and tertiary windings of coupled inductor L_{m2} , respectively. On closer observation, the sum of the last two terms in (22) and (25) is equal to V_{AB} in mode-I. If the coupled inductors turns ratio are selected such that voltage V_{AB} is zero in mode-I, (22) and (25) can be further simplified as

$$V_X = \frac{V_{in1}}{1 - d_1} + \left(\frac{N_{31} + N_{21}}{N_{11}}\right) \frac{V_{in1}}{1 - d_1}$$
 (26)

$$V_{Y} = \frac{V_{in2}}{1 - d_{2}} + \left(\frac{N_{32} + N_{22}}{N_{12}}\right) \frac{V_{in2}}{1 - d_{2}}$$
(27)

As the MSW voltage peaks are dependent on the coupled inductor turns-ratio, higher peaks can be achieved using higher turns-ratio.

For a single source TPI boost stage (shown in Fig. 4.6 (a)) with both its switches operating at duty cycle d, the MSW peak voltage equations can be simplified as

$$V_X = V_Y = (2n+1)\frac{V_{in}}{1-d}$$
 (28)

where the turns ratio in the three-winding coupled inductors is assumed as follows.

$$n = \frac{N_{21}}{N_{11}} = \frac{N_{31}}{N_{11}} = \frac{N_{22}}{N_{12}} = \frac{N_{32}}{N_{12}}$$
 (29)

From (28), it can be observed that the third-winding in the coupled inductor provides an additional boost of 'n' times the peak voltage obtained in the inductor-based TPI boost stage. High voltage gain converters based on the three-winding coupled inductor TPI boost stage have been proposed in [15-17].

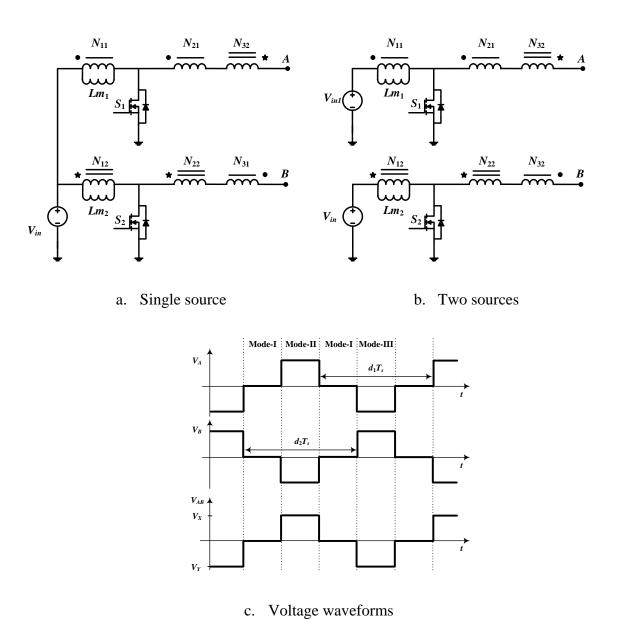


Fig. 6. Non-isolated TPI boost stage using three-winding coupled inductors

The input currents for this TPI boost stage operating with two sources are discontinuous. When a single source is used, the input current drawn is continuous. The input current in the single source case can be discontinuous if voltage V_{AB} during mode-I

is non-zero. Therefore, it is desirable to have voltage V_{AB} during mode-I to be zero. This can be achieved by selecting appropriate values of turns-ratio for the coupled inductors.

B. Isolated TPI Boost Stage

Galvanic isolation can be achieved using the TPI boost stage. Based on the components used to achieve isolation, the isolated TPI boost stage is further classified into two types – one using coupled inductors and the other using transformers. In the isolated TPI boost using coupled inductors, only two-winding and three-winding coupled inductors have been considered.

1) Isolated TPI boost stage using two-winding coupled inductors

An isolated TPI boost stage using two-winding coupled inductor is shown in Fig. 7. In this stage, the secondary windings of the coupled inductors are connected such that voltage V_{AB} is an MSW voltage. For a two source TPI boost stage shown in Fig. 7(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltage V_{AB} can be written as

$$V_{AB} = \left(\frac{N_{22}}{N_{12}}\right) V_{in2} - \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
(30)

Voltage V_{AB} during mode-I is desired to be zero for similar reasons mentioned for the non-isolated TPI boost stage with two winding and three winding coupled inductors. This can be achieved by selecting appropriate values of turns-ratio for the coupled inductors. In mode II, voltage V_X can be written as

$$V_X = \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right) - \left(\frac{N_{21}}{N_{11}} \right) V_{in1} + \left(\frac{N_{22}}{N_{12}} \right) V_{in2}$$
(31)

In mode III, voltage V_Y can be written as

$$V_{Y} = \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right) - \left(\frac{N_{22}}{N_{12}}\right) V_{in2} + \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
(32)

In (30) - (32), N_{11} and N_{21} are the number of turns in the primary and secondary windings of coupled inductor L_{m1} , respectively. N_{12} and N_{22} are the number of turns in the primary and secondary windings of coupled inductor L_{m2} , respectively. On a closer observation, the sum of the last two terms in (31) and (32) is equal to V_{AB} in mode-I. If the turns ratio in coupled inductors are selected to make voltage V_{AB} zero in mode-I, (31) and (32) can be further simplified as

$$V_X = \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right) \tag{33}$$

$$V_{Y} = \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}} \right) \tag{34}$$

As the MSW voltage peaks are dependent on the coupled inductor turns-ratio, higher peaks can be achieved using higher turns-ratios.

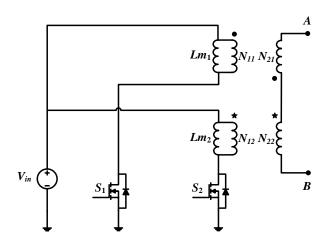
For a single source isolated TPI boost stage (shown in Fig. 7(a)) with both its switches operating at duty cycle d, the MSW peak voltage equations can be simplified as

$$V_X = V_Y = n \left(\frac{V_{in}}{1 - d} \right) \tag{35}$$

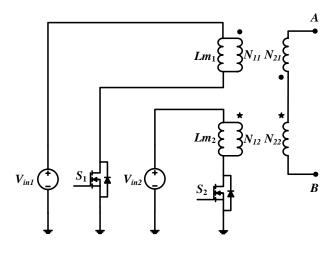
where the turns ratio in the two-winding coupled inductors is assumed as follows.

$$n = \frac{N_{21}}{N_{11}} = \frac{N_{22}}{N_{12}} \tag{36}$$

Converters using isolated TPI boost stage using two-winding coupled inductors have been proposed in [24-26, 31, 34, 38]. The input currents for this TPI boost stage with two sources are discontinuous. The input current is however continuous when a single source is used. The input current in the single source case can be discontinuous if the voltage V_{AB} is non zero in mode I. Therefore, it is desired to have voltage V_{AB} to be zero in mode-I.



a. Single source



b. Two sources

Fig. 7. Isolated TPI boost stage using two-winding coupled inductors

2) Isolated TPI boost stage using three-winding coupled inductors

An isolated TPI boost stage using three-winding coupled inductor is shown in Fig. 8. This stage is very similar to the isolated two-winding TPI boost stage. The main difference is that the tertiary windings of the coupled inductors are also connected in a manner similar to the secondary windings. Therefore, the output across terminals A' and B' is also an MSW voltage (similar to voltage across terminals A and B of secondary windings). The tertiary windings can be connected in series to the secondary windings (connecting B to A' or A to B') to achieve higher MSW voltage peaks or used separately in an interleaved manner.

For a two source isolated TPI boost stage shown in Fig. 8(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltages V_{AB} and $V_{A'B'}$ can be written as

$$V_{AB} = \left(\frac{N_{22}}{N_{12}}\right) V_{in2} - \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
(37)

$$V_{A'B'} = \left(\frac{N_{32}}{N_{12}}\right) V_{in2} - \left(\frac{N_{31}}{N_{11}}\right) V_{in1}$$
(38)

Voltages V_{AB} and $V_{A'B'}$ during mode-I are desired to be zero for same reasons specified in non-isolated coupled inductor based TPI boost stages. This can be achieved by selecting appropriate values of turns-ratio for the coupled inductors. In mode II, voltages V_X and $V_{X'}$ can be written as

$$V_X = \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right) - \left(\frac{N_{21}}{N_{11}} \right) V_{in1} + \left(\frac{N_{22}}{N_{12}} \right) V_{in2}$$
(39)

$$V_{X'} = \frac{N_{31}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1}\right) - \left(\frac{N_{31}}{N_{11}}\right) V_{in1} + \left(\frac{N_{32}}{N_{12}}\right) V_{in2}$$
(40)

In mode III, voltages V_Y and $V_{Y'}$ can be written as

$$V_{Y} = \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right) - \left(\frac{N_{22}}{N_{12}}\right) V_{in2} + \left(\frac{N_{21}}{N_{11}}\right) V_{in1}$$
(41)

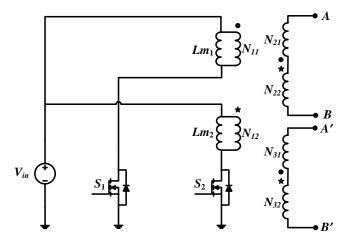
$$V_{Y'} = \frac{N_{32}}{N_{12}} \left(\frac{V_{in2}}{1 - d_2}\right) - \left(\frac{N_{32}}{N_{12}}\right) V_{in2} + \left(\frac{N_{31}}{N_{11}}\right) V_{in1}$$
(42)

In (37) - (42), N_{11} , N_{21} , and N_{31} are the number of turns in the primary, secondary, and tertiary windings of the coupled inductor L_{m1} , respectively. N_{12} , N_{22} , and N_{32} are the number turns in the primary, secondary, and tertiary windings of the coupled inductor L_{m2} , respectively. The sum of the last two terms in equations (39) and (40), (41) and (42) are equal to V_{AB} and $V_{A'B'}$ in mode-I, respectively. If the coupled inductors turns ratio are selected to make voltages V_{AB} and $V_{A'B'}$ zero in mode-I, (39) - (42) can be further simplified as

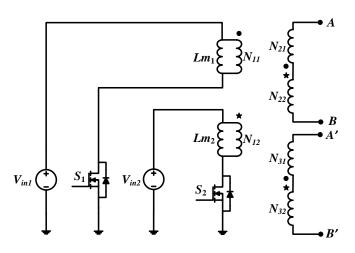
$$V_X = \frac{N_{21}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right), \ V_{X'} = \frac{N_{31}}{N_{11}} \left(\frac{V_{in1}}{1 - d_1} \right)$$
(43)

$$V_{Y} = \frac{N_{22}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right), \ V_{Y'} = \frac{N_{32}}{N_{12}} \left(\frac{V_{in2}}{1 - d_{2}}\right)$$
(44)

As the MSW voltage peaks are dependent on the coupled inductor turns-ratio, higher peaks can be achieved using higher turns-ratio.



a. Single source



b. Two sources

Fig. 8. Isolated TPI boost stage using three-winding coupled inductors

For a single source isolated TPI boost stage (shown in Fig. 8(a)) with both its switches operating at duty cycle d, the MSW peak voltage equations can be simplified as

$$V_X = V_{X'} = V_Y = V_{Y'} = n \left(\frac{V_{in}}{1 - d} \right)$$
 (45)

when the turns ratio in the three-winding coupled inductors is assumed as follows

$$n = \frac{N_{21}}{N_{11}} = \frac{N_{31}}{N_{11}} = \frac{N_{22}}{N_{12}} = \frac{N_{32}}{N_{12}}$$
(46)

Converters using isolated TPI boost stage using three-winding coupled inductors have been implemented in [24, 27]. When two sources are used, the input currents drawn are discontinuous with this TPI boost stage. However with a single source, it draws continuous input current from the source. The input current in the single source case can be discontinuous if the voltage V_{AB} is non zero in mode I. Therefore, it is desired to have voltage V_{AB} to be zero in mode-I.

3) Isolated TPI boost stage using transformer

Another way to achieve isolation in the TPI boost stage is by using transformer (see Fig. 9). It can be observed that a transformer is connected across terminals A and B of the non-isolated TPI boost stage using inductors. This isolated TPI boost stage outputs an MSW voltage at terminals A and B. For a two source TPI boost stage shown in Fig. 9(b), the peak values of the MSW voltage can be calculated as follows. In mode I, voltage V_{AB} can be written as

$$V_{AB} = 0 (47)$$

In mode II, positive peak V_X of the MSW voltage can be written as

$$V_X = \frac{N_2}{N_1} \left(\frac{V_{in1}}{1 - d_1} \right) \tag{48}$$

In mode III, negative peak V_Y of the MSW voltage can be written as

$$V_{Y} = \frac{N_{2}}{N_{1}} \left(\frac{V_{in2}}{1 - d_{2}} \right) \tag{49}$$

In (48) and (49), N_1 and N_2 are the primary and secondary turns in the transformer.

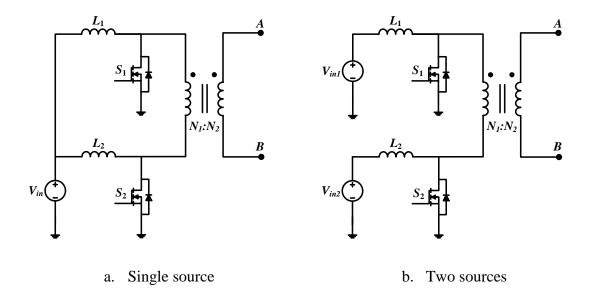


Fig. 9. Isolated TPI boost stage using transformer

For a single source isolated TPI boost stage (shown in Fig. 9(a)) with both switches operating at switching duty cycle d, voltage equations V_X and V_Y can be written as

$$V_X = V_Y = n \left(\frac{V_{in}}{1 - d} \right) \tag{50}$$

where n is the turns ratio of transformer written as

$$n = \frac{N_2}{N_1} \tag{51}$$

Converters using isolated TPI boost stage using transformer have been proposed in [29, 39]. The input current for this TPI boost stage is continuous in both two source and single source cases.

From the above analysis, it is seen that the six implementations of the TPI boost stage are capable of generating an MSW voltage at their output terminals. For all the above mentioned TPI boost stages, the voltage stress on switches S_1 and S_2 is calculated as follows

$$V_{S1} = \frac{V_{in1}}{1 - d_1}; V_{S2} = \frac{V_{in2}}{1 - d_2}$$
 (52)

IV. VOLTAGE MULTIPLIER (VM) STAGE

The VM stage in the proposed family of converters could be either diode-capacitor based or switched-capacitor based. Diode-capacitor based VM stage provides unidirectional power flow while switched-capacitor based VM stage is capable of bi-directional power flow. In this paper, we only use diode-capacitor based VM stage as the sources considered are unidirectional. The input to the VM stage is an MSW voltage (V_{AB}) shown in Fig. 2. The VM stage rectifies the MSW voltage and boosts it to a high voltage by charging and discharging its capacitors. Assuming that both positive and negative peaks of the MSW voltage are equal, i.e., $V_X = V_Y = V_{pk_MSW}$, and the VM stage gain of ' G_{VM} ', the output voltage can be written as

$$V_{out} = G_{vM} \times V_{pk_MSW} \tag{53}$$

If positive peak V_X and negative peak V_Y of the MSW voltage are different from each other, the voltage gain can only be calculated based on the operation of the VM stage.

A few possible VM stages that can be used in the proposed family of converters are discussed in this section. In some VM stages shown, an open 'Out-' terminal of the output capacitor can either be connected to the ground (GND) or to terminal 'B'. When 'Out-' is connected to 'B', the output capacitor voltage is represented as V_{Cout} . When 'Out-' terminal is connected to GND, the output capacitor voltage is represented as V_{Cout} - V_{Cout

$$V_{Cout-GND} = V_{Cout} + V_B \tag{54}$$

where V_B is terminal 'B' voltage in mode-II (either (3), (10), or (21)) of the TPI boost stage used. In the following parts of this section, only V_{Cout} is calculated for VM stages as $V_{Cout\text{-}GND}$ can be calculated using (54).

A simple diode-capacitor VM cell is shown in Fig. 10(a). It forms the basic building block for different diode-capacitor VM stages. Few simple VM stages are shown in Figs. 10(b), (c), and (d). Fig. 10(b) shows a voltage doubler circuit. The negative peak of the MSW voltage charges capacitor C_1 and the positive peak discharges it to charge output capacitor C_{out} . The voltages of the VM stage capacitors are calculated as

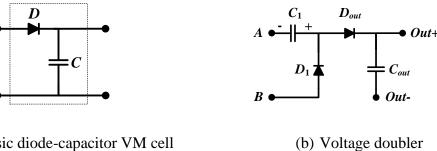
$$V_{C1} = V_Y; V_{Cout} = V_X + V_Y \tag{55}$$

Assuming that both the peaks of the MSW voltage are equal, voltage gain of the VM stage will be equal to two ($G_{VM} = 2$). Hence, it is called as a voltage doubler. Voltage doubler based converters are proposed in [25, 26, 37]. Fig. 10(c) and (d) show voltage tripler ($G_{VM} = 3$) and quadrupler ($G_{VM} = 4$) circuits, respectively. The voltage of the

capacitors in voltage tripler and quadrupler circuits are given using (56) and (57) respectively.

$$V_{C1} = V_X; V_{C2} = V_X + V_Y; V_{Cout} = 2V_X + V_Y$$
(56)

$$V_{C1} = V_Y; V_{C2} = V_X + V_Y; V_{C3} = 2V_X + V_Y; V_{Cout} = 2V_X + 2V_Y$$
(57)



(a) Basic diode-capacitor VM cell

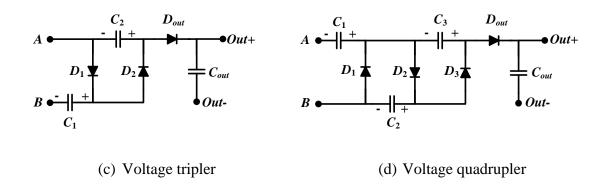


Fig. 10. Basic voltage multiplier stages

The Cockcroft-Walton (x8) voltage multiplier [40] is shown in Fig. 11. It is a network of 8 basic diode-capacitor VM cells shown in Fig. 10(a). Higher output voltages can be achieved by adding more diode-capacitor cells to the VM stage. The output voltage is the voltage across capacitors C_2 , C_4 , C_6 , and C_8 . The voltages of the VM stage capacitors and the output voltage are calculated as

$$V_{C1} = V_X; V_{C2} = V_{C3} = V_{C4} = V_{C5} = V_{C6} = V_{C7} = V_8 = V_X + V_Y$$
(58)

$$V_{Cout} = V_{C2} + V_{C4} + V_{C6} + V_{C8} = 4(V_X + V_Y)$$
(59)

A Cockcroft-Walton based converter has been proposed in [23]. Assuming that both the peaks of the MSW voltage are equal, voltage gain of Cockcroft-Walton (x8) VM stage will be equal to eight ($G_{VM} = 8$).

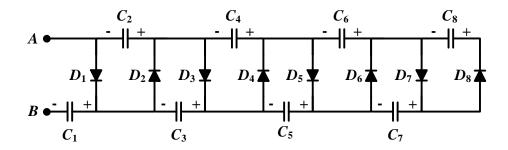


Fig. 11. Cockcroft-Walton (x8) VM stage

A Dickson charge pump [40] based VM stage is shown in Fig. 12. The VM stage shown has four diode-capacitor cells. The voltages of the VM stage capacitors and output voltage can be calculated as

$$V_{C1} = V_Y; V_{C2} = V_X + V_Y; V_{C3} = V_X + 2V_Y; V_{C4} = 2V_X + 2V_Y$$
(60)

$$V_{Cout} = 3V_X + 2V_Y \tag{61}$$

If $V_X = V_Y$, the voltage gain of the VM stage would be five times the MSW voltage peak, i.e., $G_{VM} = 5$. A Dickson charge pump based converter has been proposed in [21].

The voltage rating of the capacitors in Dickson charge pump VM stage are high as they double every time a new VM cell is added. Therefore, the size of the VM stages will increase as more VM cells are added downstream. A modified Dickon charge pump

(shown in Fig. 13) on the other hand provides a high voltage gain while having low voltage ratings for its capacitors. The capacitor voltages and the output voltages can be calculated as

$$V_{C1} = V_{C4} = \frac{V_X}{2} + V_Y; V_{C2} = V_{C3} = \frac{V_X}{2}$$
 (62)

$$V_{Cout} = 2V_X + 2V_Y \tag{63}$$

If $V_X = V_Y$, the voltage gain of the VM stage would be four times the MSW voltage peak, i.e., $G_{VM} = 4$.

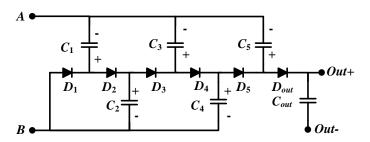


Fig. 12. Dickson charge pump based VM stage

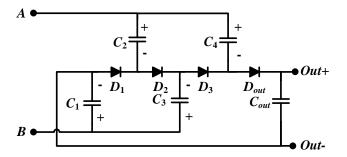


Fig. 13. Modified Dickson charge pump based VM stage

Non-inverting and inverting VM stages [41] are shown in Fig. 14. As the names suggest, the output voltages of the VM stages are non-inverting and inverting, respectively. The non-inverting and inverting VM stage capacitor voltages and the output voltage are calculated as

$$V_{C1-NI} = V_{C2-NI} = V_Y; V_{C1-I} = V_{C2-I} = V_X$$
(64)

$$V_{Cout-NI} = V_X + 2V_Y; V_{Cout-I} = 2V_X + V_Y$$
 (65)

Both non-inverting and inverting VM cells lead to a similar converter when used in the proposed family of converters. If $V_X=V_Y$, the voltage gain of the VM stage would be three times the MSW voltage peak, i.e., $G_{VM}=3$.

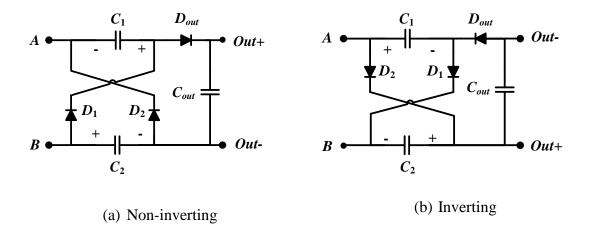


Fig. 14. Non-inverting and inverting VM stages

The VM stages mentioned above are just a few that could be used in the proposed family of converters. Few other VM stages that can be used in the proposed family of converters have been used in [18, 27, 42, 43]. With 'N' different VM stages available, the

proposed generalized structure will lead to '6N' different high-voltage-gain dc-dc converters.

V. PRACTICAL CONVERTER CONSIDERATIONS

The generic structure of the proposed family of converters will lead to many different converters capable of offering high voltage gains. All the analysis done in the previous sections is true when the converters are considered to be ideal. When practical converters are considered, there are a few effects that should be taken into account. The two main possible effects that could be observed are the effect of non-zero voltage across terminals *A* and *B* during mode-I and the effect of leakage inductance in the coupled inductors and transformers.

A. V_{AB} During Mode-I

In non-isolated and isolated TPI boost stages using coupled inductors, voltage V_{AB} during mode-I can be non-zero. This non-zero voltage V_{AB} during mode-I appears as a dc-bias (either positive or negative) on the MSW voltage. This dc bias leads to discontinuous input current in the single source case making the converters unsuitable for renewable energy applications. Therefore, it is desired to have a zero voltage across terminals A and B during mode-I. This can be achieved by proper selection of turn ratios on the coupled inductors. In practical cases with mismatch in turns ratio, the discontinuity seen in the input current is reasonably small.

B. Clamping Circuits for Reducing the Effect of Leakage Inductance

Ideally, coupled inductor based TPI boost stages operate as explained in section III. But in practice, the coupled inductors have leakage inductances which are approximately 1-2% of their magnetizing inductance. The leakage inductance has some advantages and disadvantages. The energy stored in the leakage inductance introduces high voltage spikes across the switches. This high voltage spike across switches can lead to switch failure. So a clamp circuit is required to channel the energy stored in the leakage inductor and prevent higher voltage stress across the switches. This clamp circuit adds to the component count of the converter.

Apart from requiring a clamp circuit, the leakage inductance also has a negative effect on the voltage gain of the converter. The voltage gain of the converter with leakage inductance is observed to be lower than the ideal converter. The drop in voltage gain is dependent on the clamping circuit used. However, the leakage inductance of the coupled inductor has some positive effects. The leakage inductance alleviates the reverse recovery of the diodes and thereby reduces the reverse recovery losses [15, 17, 28, 30]. Also, Zero Voltage Switching (ZVS) is possible due to the use of active clamping circuits [15, 17, 28, 30]. This helps in reducing the switching losses in the MOSFETs and thereby allowing the use of higher switching frequencies.

Practical non-isolated coupled inductor based TPI boost stages using simple diode-capacitor clamping circuit are shown in Figs. 15 and 16. Few active clamping solutions for non-isolated TPI boost stages have been used in [15, 17]. Similarly, in the isolated coupled inductor based TPI boost stages, the leakage of the coupled inductor leads to similar effects in the converter. There are many clamping circuits that can

resolve the leakage inductance issues [24-28, 39] in isolated topologies. In most cases, the input current drawn from the source using these clamping circuits was observed to have large ripple. A clamping circuit capable of resolving leakage inductance issues while providing a smaller input current ripple [30] has been shown in Fig. 17.

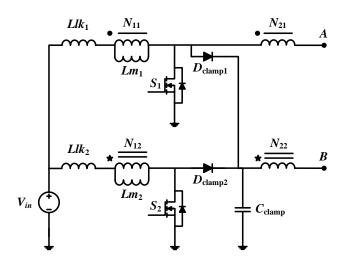


Fig. 15. Two winding coupled inductor based TPI boost with clamp circuit

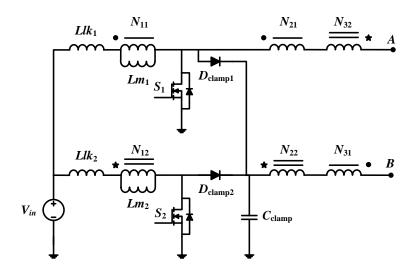


Fig. 16. Three winding coupled inductor based TPI boost with clamp circuit

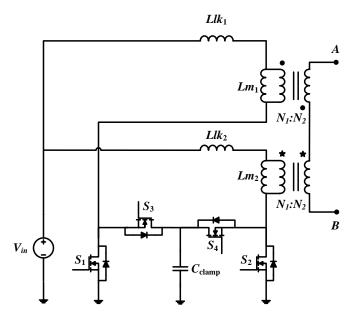


Fig. 17. Isolated coupled inductor based TPI boost stage with active clamp circuit

VI. EXAMPLE CONVERTER

This section uses the theory proposed in the earlier sections of the paper to build a high-voltage-gain dc-dc converter. For building an example converter, a TPI boost stage (Fig. 4(a)) and a VM stage (Fig. 14(a)) are selected from the possible solutions discussed in sections III and IV. This converter uses a single source non-isolated TPI boost stage with inductors with its switches S_1 and S_2 operating at same duty cycle 'd'. The MSW output voltage of the TPI boost stage would have equal peak voltages that can be calculated using (7). Using a non-inverting VM stage and the selected TPI boost stage, the example converter obtained is shown in Fig. 18.

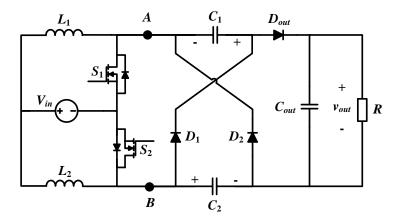


Fig. 18. Non-isolated high voltage gain converter using non-inverting VM stage

The output voltage of the converter can be derived as follows.

$$V_{pk,AMSW} = V_X = V_Y = \frac{V_{in}}{1 - d}$$
 (66)

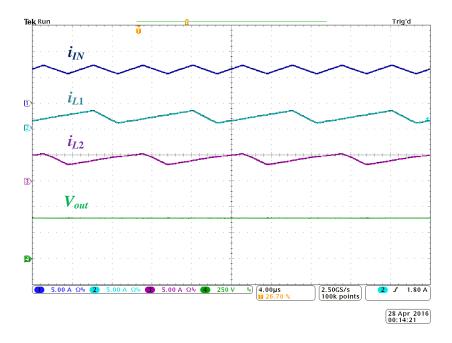
$$V_{Cout} = 2V_X + V_Y = 3V_{pk,AMSW} = 3\left(\frac{V_{in}}{1-d}\right)$$
 (67)

According to (67), the proposed converter offers an output voltage of 396V when operating with a 33V input source at a duty cycle of 75%. The peak of the MSW voltage is calculated as 132V. A hardware prototype of the example converter shown in Fig. 18 has been built for the specifications in Table-I. The switching frequency used was 100 kHz and the components used are listed in Table-I. The inductors are selected to operate in CCM.

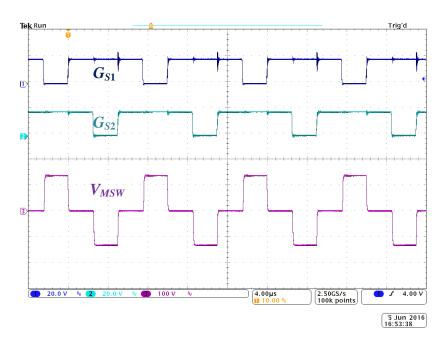
Table I. Experimental Parameters

Parameter	Value	Component	Value	Part No.
Input Voltage	33 V	Inductors L_1 and L_2	95 μΗ	ETD-49 A250 core 21 turns
Output Voltage	396 V	MOSFET	150 V, 43 A	IPA075N15N3G
Switching Frequency f_{sw}	100 kHz	Diode	600 V, 15 A	MURF1560G
Load Resistance	800 Ohms	VM capacitors	22 μF	EPCOS B32796E2226K
Output Power	200 W	Output Capacitor	15 μF	C4ATGBW5150A3LJ

The experimental waveforms obtained are shown in Figs. 19(a) and (b). The output voltage is observed to be 396V and it conforms to the output voltage calculated using (67). The MSW peak voltages are 132V. The experimental efficiency observed at 200W of output power is 94.05%. The inductor currents and the input current are all continuous. Switching signals of switches S_1 and S_2 are seen to be at 75% duty cycle and 180° apart from each other. This example converter verifies that the generalized structure is useful in building high voltage gain dc-dc converters. Single source converters built using the generalized structure offer continuous input current which is desirable in renewable energy applications.



(a) Input current, Inductor currents, and Output Voltage



(b) Switching signals and MSW voltage

Fig. 19. Waveforms of the example converter operating at 200W

VII. CONCLUSION

In this paper, a family of high-voltage-gain dc-dc converters based on a generic structure has been introduced. The generic structure is a two stage configuration – a TPI boost stage on the input side and a VM stage on the output side. Different possibilities for the TPI boost stage are analyzed and discussed in detail. All the analysis has been carried out for a two source case with switches operating at different duty cycles. Later, they have been analyzed for a single source with both switches operating at a same duty cycle. Owing to the ripple cancellation, all the TPI boost stages offer continuous input current with smaller ripple when operating using a single source. A few possible VM stages are discussed and their voltage gains have been derived. Two main practical converter considerations have been discussed. An example converter has been built using the generalized structure and analyzed. A hardware prototype of the example converter was developed to verify the analysis. The proposed family of converters built using the generalized structure offer high voltage gain and continuous input current when operating using a single source. These converters are most appealing in applications involving integration of renewable energy sources into 400V dc systems.

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SECTION

2. CONCLUSION

High-voltage-gain dc-dc power electronic converters have been gaining popularity for the integration of renewable energy sources into 400V dc systems. In this dissertation, two new dc-dc converter topologies that offer high-voltage-gain have been presented. The first topology is based on a two-phase interleaved boost stage and a modified Dickson charge pump voltage multiplier circuit. Higher output voltage is obtained by charging and discharging the VM stage capacitors. Having two phase boost on the input side, this converter can be powered using two sources or a single source in an interleaved manner. It is also capable of drawing continuous input current in both cases. The voltage stress on the semiconductor devices is relatively low compared to the higher output voltage. The major contribution of this topology is the low voltage rating of its VM stage capacitors which greatly helps in reducing both size and cost of the converter. The modes of operation for this converter have been explained and the output voltage has been derived. The current and voltage stress on its components have been derived and supported with simulation results. Also a hardware prototype was developed to verify the converter operation, voltage gain, and component stresses.

The second topology is constructed using a two phase interleaved boost stage and a non-inverting diode-capacitor voltage multiplier. This converter offers high voltage gain while having a simple structure with low component count. The voltage of gain of this converter is slightly lower compared to the first converter. But, similar to the first

converter, this converter can be powered using two sources or a single source in an interleaved manner. Also, continuous input current is drawn from the sources in both cases. The voltage stress on semiconductors is relatively low compared to the output voltage. The voltage gain and modes of operation of the converter have been discussed. Also, the different component stresses have been derived and supported with simulation results. Finally, a hardware prototype was developed to verify the converter operation and voltage gain. The boundary conditions between the CCM, PDCM, and DCM operation of the converter have been discussed and also verified using simulation results.

Both the topologies proposed offer high voltage gain, continuous input current, multi-input capability, and low voltage stress on the semiconductors making them appealing for applications involving integration of renewable energy sources. On a closer observation, it is seen that the two topologies introduced have a common structure in their construction. They both have an interleaved TPI boost stage on the input side and a VM stage on the output side. Based on this generalized structure, a family of highvoltage-gain dc-dc converters is introduced. Also, the switching scheme required for generating the intermediate voltage is discussed. The proposed family of converters is classified into non-isolated and isolated converters based on the TPI boost stage. The different possible TPI boost stages and their output voltages are derived. A few possible VM stages have been discussed and their voltage gains have been calculated. Two practical converter considerations have also been discussed. Finally, an example converter was built using the generalized structure. It output voltage was estimated using the derived equations and verified through hardware implementation. The proposed family of converters offers high voltage gain, continuous input current in the single

source case, and low voltage stress on switches making them suitable for integration of renewable energy sources on 400V dc bus systems.

Future work involves average and small signal studies for the proposed converters for designing closed loop converters. Also, control strategies implementing MPPT and power sharing are to be explored for two source converters. The bidirectional capability of the proposed converters can be studied for the integration of energy storage devices by using switched-capacitor voltage multiplier circuits and proper switching schemes. More work has to be done to improve the efficiency of the converters with better design and PCB layouts.

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VITA

Bhanu Prashant Reddy Baddipadiga was born in March, 1990. He graduated from Sreenidhi Institute of Science and Technology, Hyderabad (India) with Bachelors in Technology in Electrical and Electronics Engineering in 2007. He started his Ph.D. degree in August 2011. In December, 2016 he received his Ph.D. in Electrical Engineering from Missouri University of Science and Technology. His main research interests are design and control of high-voltage-gain dc-dc power electronic converters for applications like integration of renewable energy and energy storage devices.