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Characterization of an Integrated Circuit with Respect to Electrostatic Discharge-Induced Soft Failures

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CHARACTERIZATION OF AN INTEGRATED CIRCUIT WITH RESPECT TO ELECTROSTATIC DISCHARGE-INDUCED SOFT FAILURES

by

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This dissertation consists of the following articles, formatted in the style used by the Missouri University of Science and Technology.

Paper I on pages 19-44, as well as Paper II on pages 45-71, were published at the 2013 EOS/ESD Symposium in Las Vegas, NV.

Paper III on pages 72-97 was published at the 2015 EOS/ESD Symposium in Reno, NV and an extension to this work is intended for submission to the IEEE Transactions on Electromagnetic Compatibility.

Paper IV on pages 98-128 is intended for submission to the IEEE Transactions on Device and Materials Reliability.

ABSTRACT

This research proposal presents a methodology whereby an integrated circuit (IC) can be characterized with respect to soft-failures induced by Electrostatic Discharge (ESD)-like events. This methodology uses an exclusively "black-box" approach to determine the response of an IC in a system-level environment, thereby allowing it to be implemented without intimate knowledge of the DUT IC. Results from this methodology can be referenced during system design to raise awareness of specific vulnerabilities of the core system ICs.

During work on this methodology, several sub topics have been explored and developed in the field of system-level ESD. Sections 2 and 3 introduce two topics which were developed to facilitate the generation and expression of IC pin models. Papers 1 and 2 introduce injection methods for characterizing complete systems on an interface-by-interface basis and form the foundation for the following works. Papers 2 and 3 mirror Papers 1 and 2 but instead shift focus away from the system as a whole and outline methods for characterizing the integrated circuits directly. Finally, Section 4 outlines a model method which can be used to describe the failures found in Paper 4 in circuit simulation, rounding out the work. Additional measurements which were unable to be included in Paper 4 are included in Appendices A, B, and C.

ACKNOWLEDGMENTS

I would like to thank my advisor Dr. David Pommetenke, for supporting me from late in my undergraduate all the way through my graduate studies at the MS&T EMC Lab. Thank you also to the rest of my committe here at MS&T, Dr. Daryl Beetner, Dr. Jun Fan, and Dr. Victor Khilkevich, for their insights into this work. I would also like to extend special thanks Harald Gossner, the instigator of my research project. My time working with Harald in Munich was an enormous opportunity that I benefited from academically, professionally, and personally. Finally, I would like to thank my wife Patricia for her patience and support through my graduate work as well as my family for their role in where I am today.

TABLE OF CONTENTS

Page

PAPER

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION

1. INTRODUCTION

While a general understanding of integrated circuit (IC)-level electrostatic discharge (ESD) has been developed over the last decades, ESD in the scope of whole systems has only relatively recently received similar attention. In 2010 the Industry Council on ESD Target Levels published part one of a white paper [1] which detailed a systematic approach to dealing with system-level ESD, termed System Efficient ESD Design (SEED) which was followed up in 2012 by part two [2]. Since these publications, there have been a number of works which detail implementations of SEED principles on various systems such as [3; 4; 5]. These works have focused on mitigating failures which would lead to device destruction and permanent loss of system functionality, but ESD-induced soft-reliability issues such as data corruption and system upsets are also concerns.

In order to characterize the robustness of a system with respect to soft-failures, a "divide and conquer" approach was developed. This method begins by dividing a system into discrete subsystems such as communication interfaces, IO interfaces, and other peripherals. Once the subsystems have been identified (divide) then each is subjected to various stress pulses to determine their independent robustness levels (conquer). This was first implemented on the scope of a complete system in [6] before being applied directly to the application processor of a similar system in [7]. By splitting the DUT IC into logical pieces and characterizing each interface, models can be generated which are capable of describing the response of the system to a given stimulus on each pin. While similar techniques have been performed for hard failure analysis, this work closes the gap between

the hard- and soft-failure worlds by presenting a methodology whereby soft-failures can be similarly modelled. With these models in hand, system-level simulation can then identify problem areas where targeted fixes can be applied in either hardware or software to counter any potential weaknesses.

In this work the black-box characterization of a highly integrated circuit is presented, as well as both integral and closely related work. In Sections 2-3 and Papers 1-3, several ancillary measurement techniques are presented which describe various aspects of the system setup. Paper 4 contains the characterization methodology and supporting information about the IC under test. Finally, Section 4 integrates the results from Paper 4 into the modelling techniques from Sections 2-3 by proposing a circuit simulation model which is capable of reflecting various failures both hard and soft.

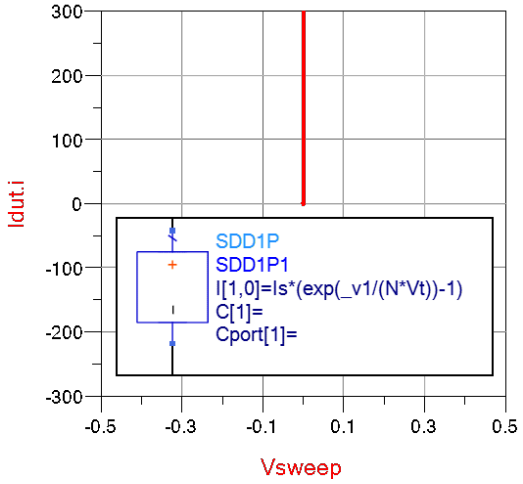
2. PIECEWISE LINEAR IV CURVES

2.1. INTRODUCTION

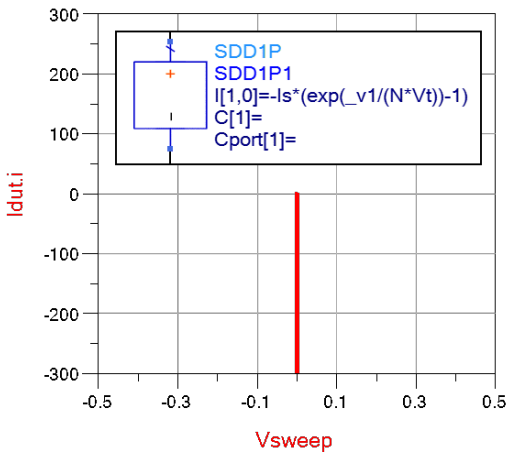
A key component of SEED is the ability to express measured IV behaviors inside simulation environments such as SPICE. These IV curves are, in general, nonlinear and can often contain apparent negative resistances associated with the phenomenon known as snapback. In reality, snapback is generally not a true negative resistance but traces an IV curve that sees a sudden increase in current and a decrease in voltage. In order to model these curves it is desirable to implement them as a piecewise function of current. Similar piecewise models constructed in VHDL-AMS [8] as well as Verilog-A [9] have been proposed by for both diode and snapback behaviors. Outside of the context of ESD, a purely SPICE-based approach to piecewise linear IV modeling was proposed in [10]. Originally the SPICE-technique was used to implement the real-world negative resistive behaviors of devices such as unijunction transistors and tunnel diodes in a simulation environment for educational purposes. Unfortunately the method relies on the now-deprecated ability of SPICE to accept negative values for the saturation current of a diode. While such a value is not physical, it should be mathematically acceptable by most solution engines. This section serves as an overview of an implementation of the piecewise linear SPICE model in Agilent/Keysight ADS.

2.1.1. Circuit Building Blocks. Implementation of the required circuit elements in ADS is similar to the original implementation. Although, like SPICE, ADS does not accept negative values for the saturation current of a diode, the environment does allow for both implicitly and explicitly defined IV relationships through the use of a 1-port symbolically defined device (SDD1P) [11]. By using these blocks to implement the fundamental diode

equation, sanity checks on the sign of Is are bypassed (Figure 2.1). The exponential relationship between the block current and voltage mimics that of the ideal diode equation as only a callback to the original implementation. Any sufficiently strong exponential relationship could also be used.



(a) Ideal diode implementation in Keysight ADS

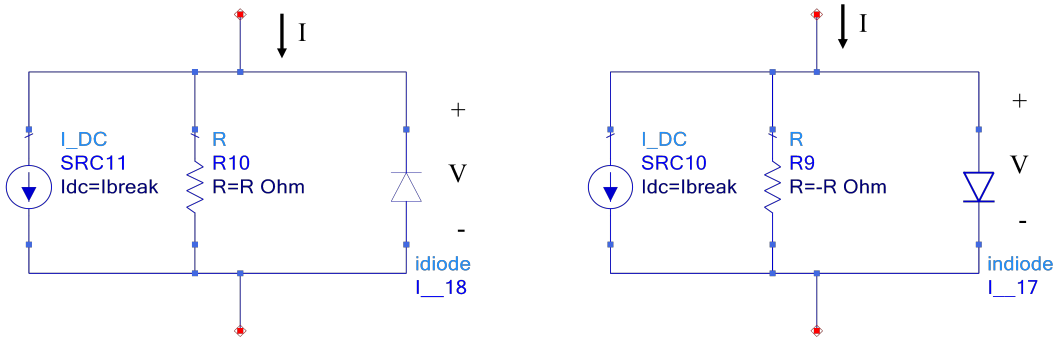


(b) Negative ideal diode implementation in Keysight ADS

Figure 2.1. Ideal and negative ideal diode implementations

Having implemented the positive and negative ideal diodes with equation blocks, the fundamental unit cells can also be created. These unit cells operate on the principle that while the total current is less than Ibreak the cell is shorted. However, once the current exceeds Ibreak, the cell resistance is switched in, and adds to the total resistance of the string of cells. This switching action is achieved by the very small turn-on voltage of the ideal diodes. When the current entering the cell is less than the break current, the remainder of the current (Ibreak âĂŞ I) must then flow through the cell resistance until the cell diode is forward biased. Once the cell diode is forward biased (which occurs at very low voltages due to the near-ideal turn-on behavior), a balance is struck between the current required to keep the ideal diode in conduction, and the current through the cell resistance. The result

is a vanishingly small positive or negative cell voltage. In essence, a short circuit. The implemented positive and negative cells are shown in Figure 2.2.



(a) Positive resistance unit cell implementation in Keysight ADS

(b) Negative resistance unit cell implementation in Keysight ADS

Figure 2.2. Positive and negative resistance unit cell implementations

Finally, by cascading these unit cells, arbitrary IV curves can be realized by the network. In Figure 2.3, a DC current source is swept to drive the attached model. The results of the DC simulation are shown in Figure 2.4 by plotting the resultant voltage against the swept current source value.

2.1.2. Simulation Using Piecewise Linear IV Models. Although it is trivial to achieve convergence for these circuits in a DC simulation, a transient solution is more difficult to achieve. After extensive study and experimentation, the primary issue seems to be that if the model, even momentarily, has an apparent resistance equal in magnitude but opposite in sign to the source resistance, then the internal current and voltage derivatives become too high. These rapidly changing values trigger a convergence failure as the internal timestep attempts to decrease below some absolute minimum limit in an attempt to track the current and voltage values. For this reason, the piecewise linear SPICE modeling method is limited to curves which do not exhibit negative resistances with a magnitude larger than the driving source resistance. At first one might believe that the model would only be

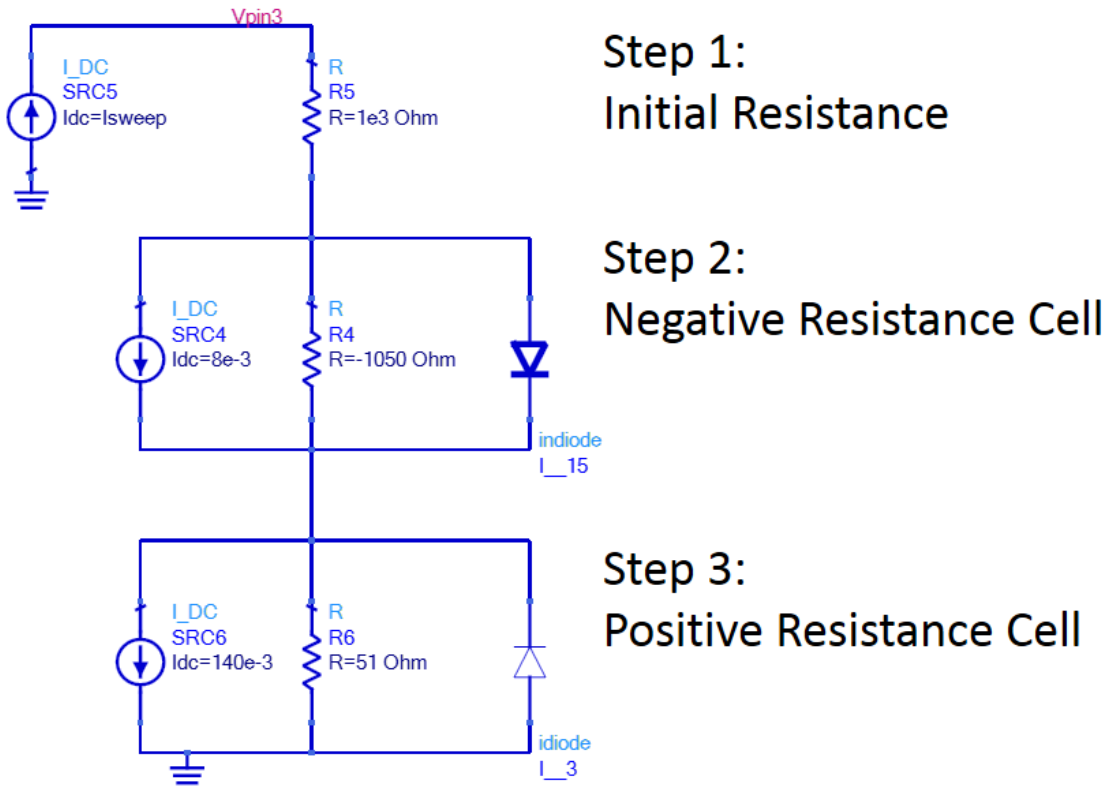


Figure 2.3. DC current swept model

incapable of expressing instantaneous resistances of exactly $Rsrc$. However, because the IV curve is not strictly piecewise and is instead a continuous function, even at the corners, in order to express a resistance which is less than $Rsrc$, the model must pass through $Rsrc$ at one or more corners resulting in instability. Finally, because the unit cells only function for positive currents, the model is invalid on the entire left hand side of the IV plane, as the only functioning portion of the model is the initial resistance. In order to construct a model which can represent both negative and positive behaviors of a device, two models must be used, each isolated by the previously developed ideal diodes such that one model corresponds to positive current flow and the other to negative. (Figure 2.5).

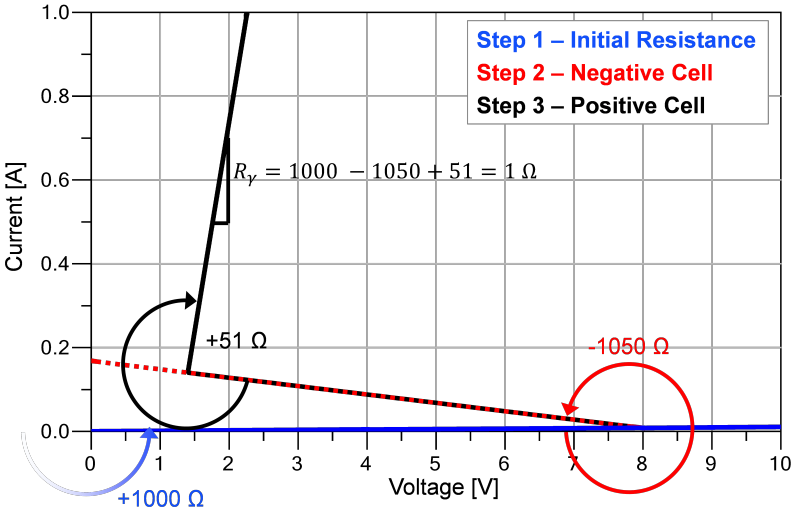


Figure 2.4. DC current swept IV curve

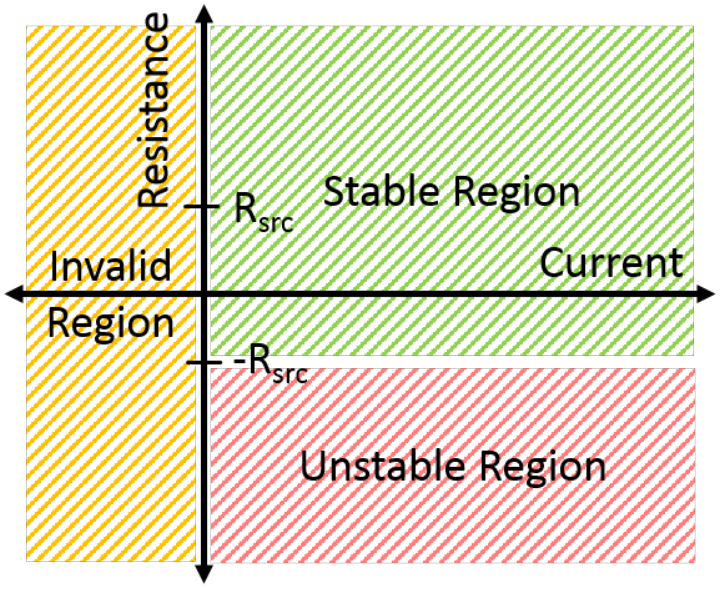


Figure 2.5. Regions of stability and validity for the piecewise linear IV SPICE model

After understanding the constraints on this technique, the device can then be modeled and run through a batched transient simulation to mimic the measurement performed by a TLP system. The positive half of a device IV curve is represented by a chain of an initial resistance, a negative resistance block, and a positive resistance block to create a snapback characteristic. The negative behavior is represented by a second chain of blocks with only an initial resistance and one negative resistance to create a diode-like behavior. An ideal diode is also included in the negative branch to isolate it from positive excitations. This ideal diode is not present in the positive characteristic branch to reduce the overall component count. The omission of this diode places the initial resistance of the positive branch in parallel with the overall negative behavioral branch which has only a negligible effect. The circuit shown in Figure 2.6 was excited by a batch of 77 individual transient simulations of 100 ns duration. Across these simulations, the source voltage $Vpulse$ was swept from -50 V to 50 V. The resultant transient voltage and current traces were then window-averaged by the simulator in the same way that a TLP system would in order to generate the resultant IV curve in Figure 2.7.

2.1.3. Conclusion. In this section, an easily-implementable method for implementing the piecewise linear IV behaviours commonly used to describe components in the ESD regime is presented. The method is implemented in a SPICE-like engine, the general limitations are outlined, and a bidirectional transient simulation of a device is demonstrated.

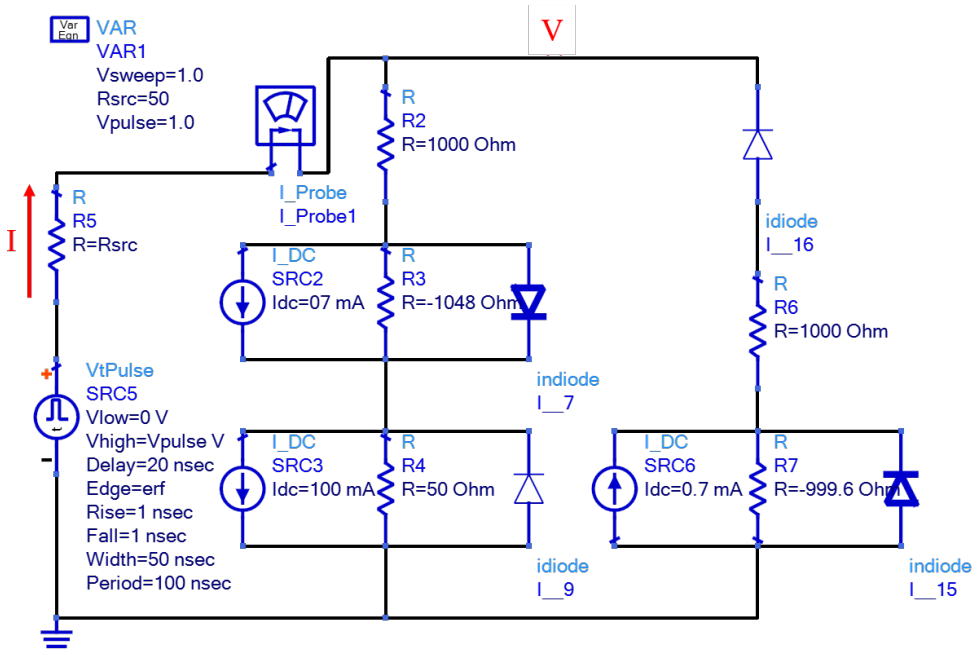


Figure 2.6. Transient simulation of a snapback-positive, diode-negative device

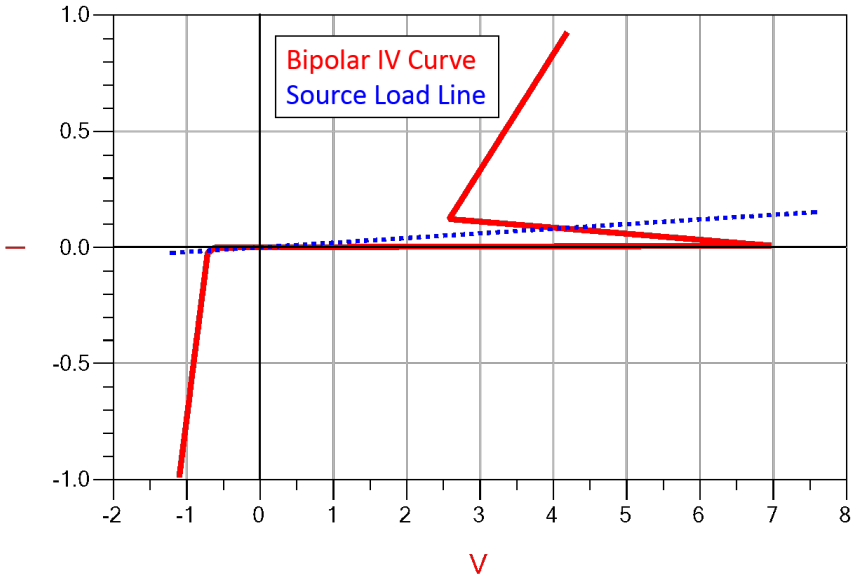


Figure 2.7. IV curve resulting from a batched transient simulation

3. THREE-TERMINAL PIN MODELING

3.1. INTRODUCTION

While the TLP is an excellent tool for measuring the IV relationship between two pins, it should be noted that the use of a two-pin characterization system to better understand system-level ESD events is a fundamentally flawed approach Figure 3.1. By its very nature, a system-level ESD event takes place in the context of a system which not only includes the victim IC, but also everything which it is connected to. Common on-chip protection schemes frequently connect the IO to both VSS and VDD [12] and [13]. Furthermore, the behavior of some protection schemes is a function of the voltage between VDD and VSS. Finally, the presence of the off-chip low impedance decoupling network between VDD and VSS such as typically found in systems has also been shown to have a strong effect on the performance of the on-chip ESD protection scheme [14]. For these reasons, the assertion is made that using a TLP alone to perform a two-pin characterization of IO pins should be seen as unrealistic.

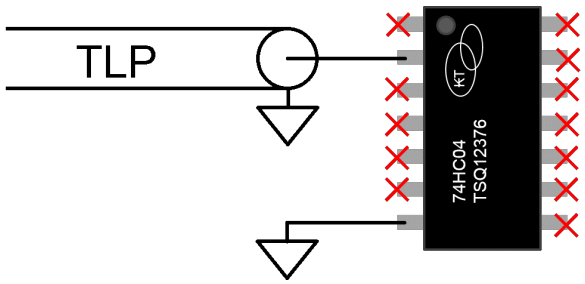


Figure 3.1. Using a TLP to measure an IV characteristic is a two-terminal technique which ignores the connections made to other IC pins

3.1.1. Measuring Pins in the Context of a System. In order to characterize the IO pin of an IC in a more realistic system-level case, the IC is instead placed into a simple circuit which is intended to more closely mimic a realistic system. Such a circuit should include a voltage source to provide a bias between the associated VDD and VSS of the IO under test, adequate decoupling capacitance on the same voltage source, and a second current transformer to measure the current leaving the IC VDD network during IO injection (Figure 3.2). In this way, the IO pin is treated as a three terminal model which includes connections to both VDD and VSS. This measurement technique has been implemented both on a waver probing station with needle probes (Figure 3.3) and by placing the IC in a "deadbug" configuration and forming the circuit by "manhattan construction" [15] (Figure 3.4). The primary application to this body of work is the ability of the technique to predict the amount of current which is shunted to the PCB power distribution network (PDN) during an ESD event. Such a prediction can potentially be used by system designers to ensure the stability of the PDN, or in soft-failure characterization to provide another parameter with which to correlate observed failures during strikes on IO pins.

The validity of this measurement technique is based on the assumption that the system VDD is held relatively stable during the event. This assumption is confirmed by measuring the disturbance on VDD in addition to the IV characteristic of the pin. For cases outside of this assumption, an even more complex nonlinear model must be measured and constructed to account for the effects of VDD perturbations on the IO clamp behavior. This case is considered to be overly complex and is left as potential future work.

3.1.2. Benefits of the Three-Terminal Model. The three terminal model provides two potential benefits. The first is accurately understanding the current distribution inside an IO cell under development. Application of the measurement methodology can determine whether the intended device triggers during an event or whether alternate, potentially

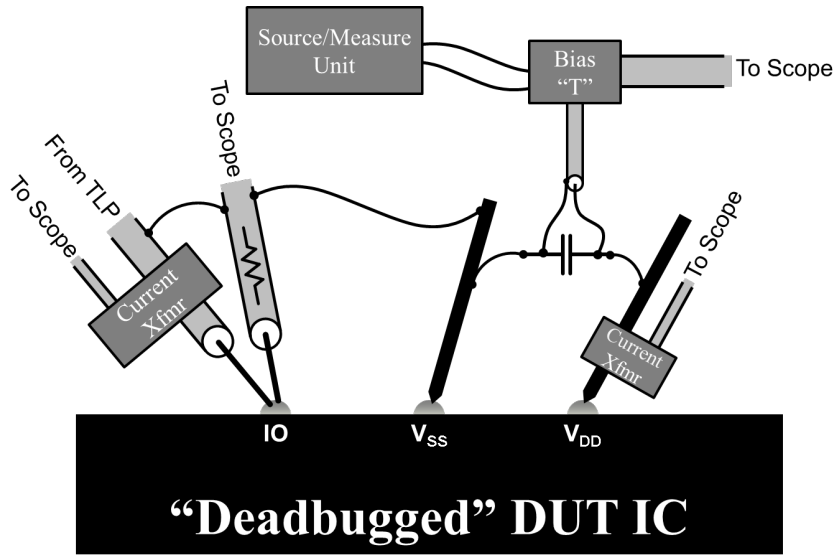


Figure 3.2. Diagram of the three-terminal IO measurement method

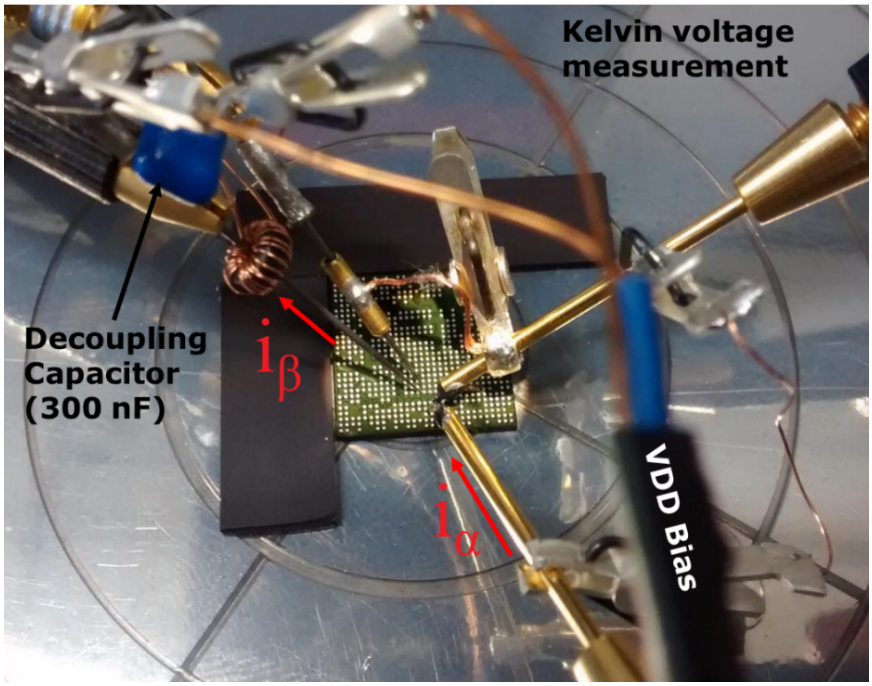


Figure 3.3. Three-terminal measurement of an IC IO pin on a wafer-probe station

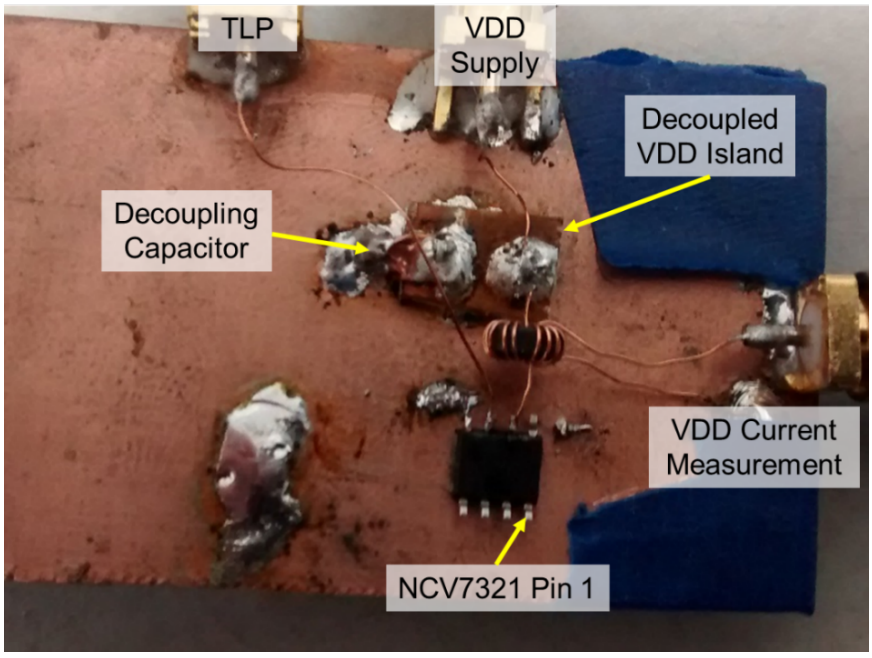


Figure 3.4. Three-terminal measurement of an IC IO pin in deadbug configuration

undersized paths become energized. The second potential benefit is the understanding of the amount of current shunted to the PCB-level PDN during a system-level ESD event. Work on the identification of soft-failures has shown that some errors are not caused directly by a current injected into an IO pin, but instead the resultant disturbance on the power distribution network. During SEED-style simulations, if the amount of current diverted to the voltage supply of the IC is known then such PDN-induced failures can be better addressed.

In the first example let us consider the IV curves (taken only to 0.5 A) shown in Figure 3.5. These curves were extracted using the deadbug measurement setup in Figure 3.4. In the positive regime, the device appears to be a simple diode to VDD. By measuring the voltage of the IO pin in both cases with respect to the VSS pins, a clear shift of approximately 3.3 V is visible in the diode characteristic. In contrast, the negative regime is ambiguous. Both curves seem to trigger at the same point, but the slope of the curve above -200 mA

shows a clear difference in behaviors. To investigate this phenomenon further, it is helpful to look at the transient waveforms of the IO pin current and the current leaving VDD.

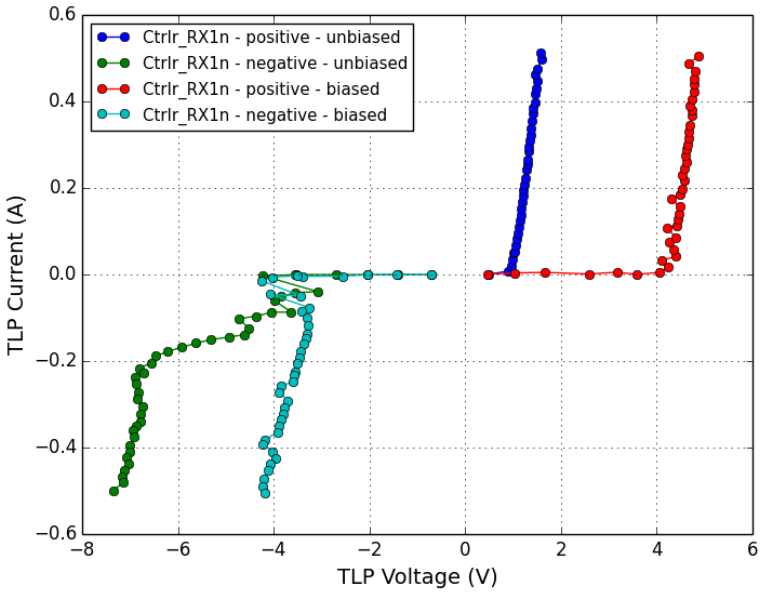
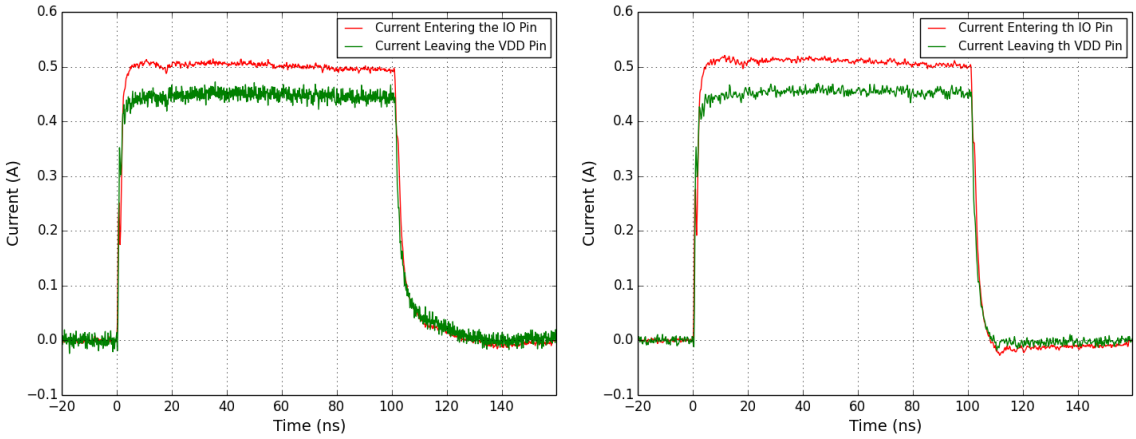


Figure 3.5. Measured IV curve of a high-speed USB 3.0 differential pin

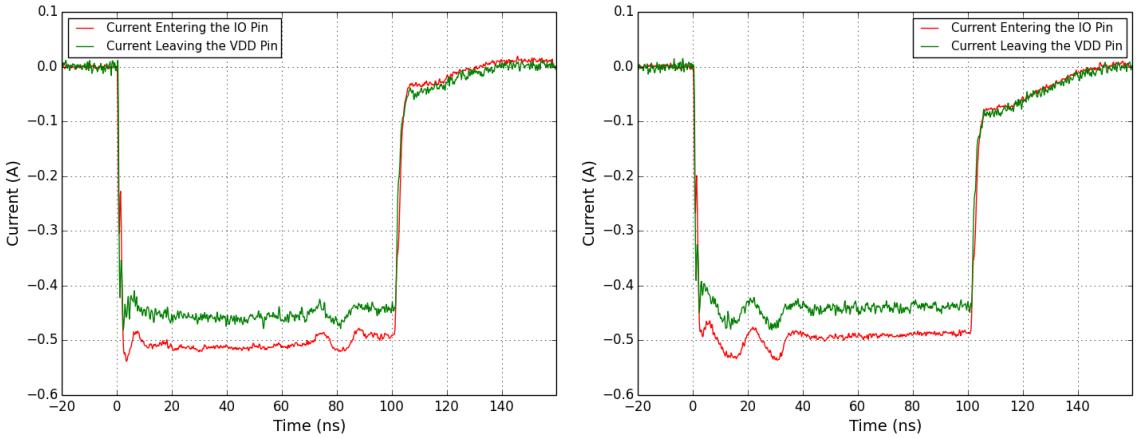
Figure 3.6 and Figure 3.7 show the transient curves measured at the 0.5 A points of the biased and unbiased positive and negative pin behaviors of an example device. In both cases, it is easy to see the similarity in magnitude as well as in the rising edges of the current waveforms between the IO and VDD currents, strongly indicating that both positive- and nevative-going current paths are from IO to VDD.

By observing these current waveforms we can see that (for the negative case) nearly all of the current which leaves the IO pin due to a negative injection, is sourced by the IC power distribution network. In reality there is a very small measured difference between the currents. By subtraction, the VSS current can then be calculated, and the IO IV curve can subsequently be visualized three different ways. At the top level, the IO current is plotted



(a) Positive unbiased behavior (b) Positive biased Behavior

Figure 3.6. A snapshot of a positive transient current waveform pair



(a) Negative unbiased behavior (b) Negative biased Behavior

Figure 3.7. A snapshot of a negative transient current waveform pair

against the IO voltage. The second two cases plot the IO pin voltage together with the VDD and VSS currents. In this way, the current split inside the IO cell is easily visualized. This is shown in Figure 3.8. By further examining the measurement, it is found that, for this device, the ratio of the current between VDD and VSS is approximately 8.5. This

radio indicates that in spite of the primary connection being to VDD, there is also a small connection to VSS. The generated model can now reflect this by shunting some fraction of the injected current to VSS. An example model is shown in Figure 3.9 and the comparison to the measured IV curve is shown in Figure 3.10.

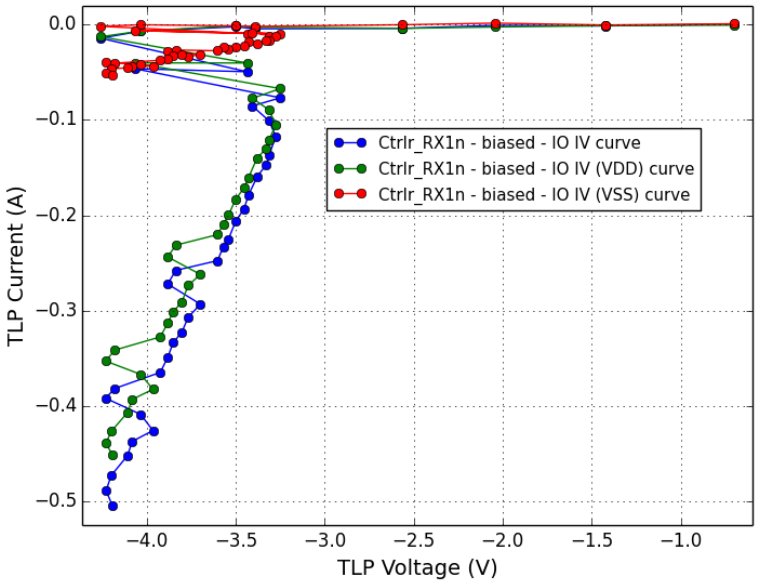


Figure 3.8. Split IO IV curves showing currents to VDD and VSS

3.1.3. Conclusion. Using the presented three-terminal measurements and modeling technique, behaviors of the IC IO pin can be extracted which include connections to VDD as well as VSS. Models designed from these measurements can now include this connection information without any input from the IC manufacturer. Such a model, when used in an accurate SEED simulation, is now capable of affecting the current disturbance of the system VDD network.

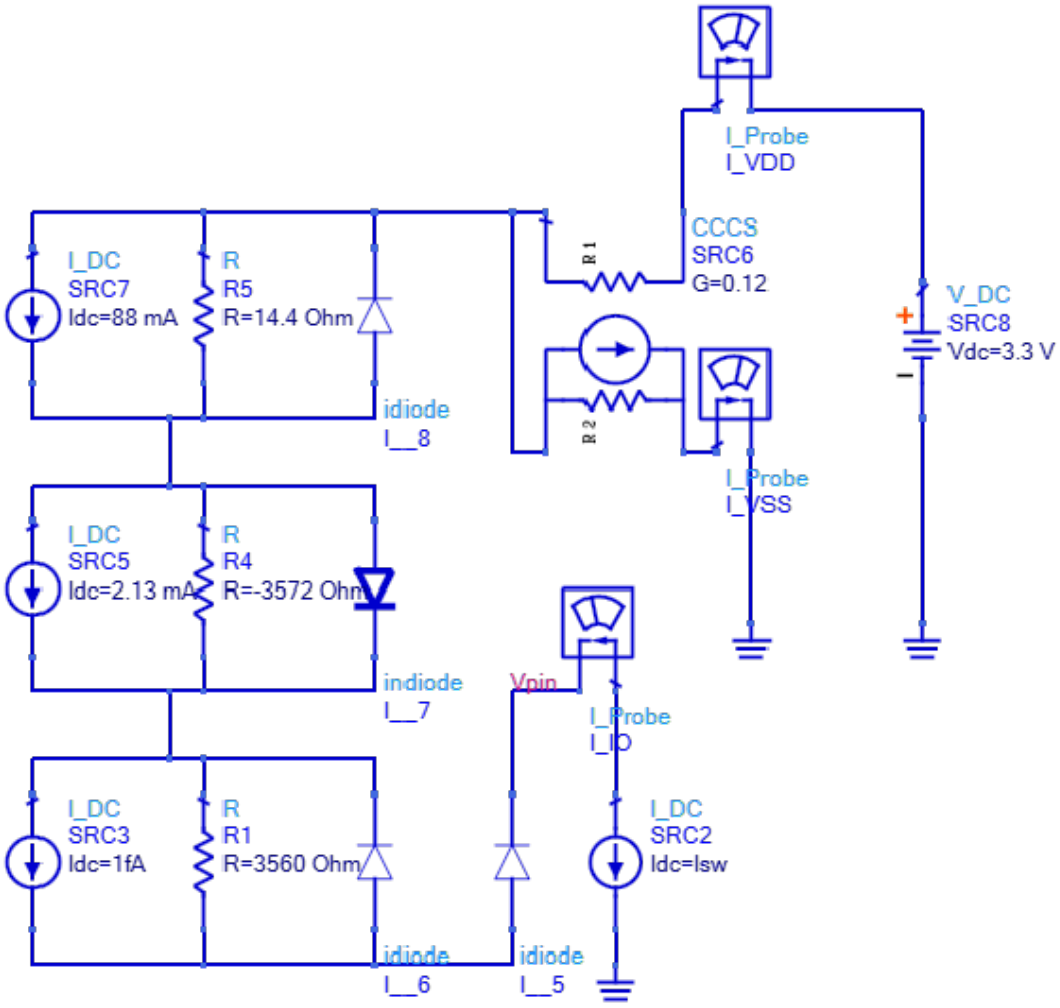


Figure 3.9. Piecewise linear three-terminal IO cell model

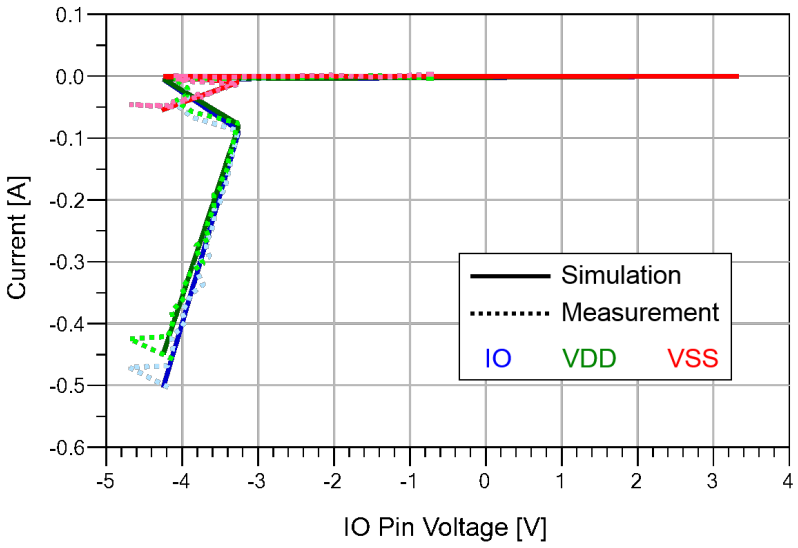


Figure 3.10. Measurement and model comparison

PAPER

I. POWERED SYSTEM-LEVEL CONDUCTIVE TLP PROBING METHOD FOR ESD/EMI HARD FAIL AND SOFT FAIL THRESHOLD EVALUATION

Thomas Schwingshackl, Benjamin Orr, Joost Willemen, Werner Simbürger, Harald Gossner, Wolfgang Bösch, and David Pommerenke

ABSTRACT

In this paper an advanced system-level TLP probing technique is presented to evaluate the ESD and EMI performance of a powered system applicable to high speed interfaces. It allows to detect hardware and software fail thresholds to assess the performance of an ESD/EMI protection solution. The method is demonstrated on a Intel mobile phone reference platform.

1. INTRODUCTION

In recent years, system level ESD has become a major focus in the area of ESD testing. At ESD pulse injection levels far below the hardware failure threshold soft-failures can occur. Those soft-failures can cause the shutdown, reboot or hang-up of application software or the whole system. Detecting soft-failure thresholds and investigating their root causes requires the ability to apply ESD pulses into the running system. Normally, system level ESD tests are carried out with a IEC 61000-4-2 ESD generator. In the last couple of years system level testing using Transmission Line Pulse (TLP) generators has become an alternative method for trouble shooting of system level ESD fails [1].

Conductive TLP pulse injection has the benefit that the amplitude of the injected disturbance can be accurately monitored and therefore provides quantitative information of the disturbance levels that can be tolerated or provoke soft and hard fails. When using conductive TLP injection loading of e.g. high-speed data lines by the injection probes and cabling parasitics have to be avoided. The challenge is to connect the DUT to the pulse source through some sort of barrier that isolates the pulse source from the DUT, but still allows the pulse to be delivered to the system. Previously, resistors and capacitors have been used in conductive injection systems to obtain the required isolation. These probes work by placing a relatively high impedance element into a transmission line in order to increase the impedance seen looking in to the TLP system. This impedance effectively isolates the net from the pulse source, but must remain small enough to inject the pulse from the TLP source. In this paper, the authors describe an injection system consisting of ultra-low capacitance bidirectional transient voltage suppressor (TVS) diodes embedded in coaxial injection probes as an alternative to the resistive and capacitive probes.

2. CONDUCTIVE TLP INJECTION CONFIGURATIONS

2.1. DEVICE LEVEL TESTING

A common method for measuring device level TLP characteristics uses the Kelvin configuration. Figure 2.1 shows a TLP setup using the Kelvin method to measure the TLP IV characteristics of a DUT [2]. Here the current pulse is applied to the DUT over the pulse force probe. The current transient is measured using a current sensor connected to a sampling oscilloscope. At the DUT the voltage transient is measured using e.g. a 5 kΩ probe connected to a sampling oscilloscope. The same method can be used for system level ESD tests of powered up systems when the pulse force probe, as shown in Figure 2.1, is exchanged with resistive (Figure 2.2a), capacitive (Figure 2.2b) or ultra low capacitance TVS diode probe tip (Figure 2.2c).

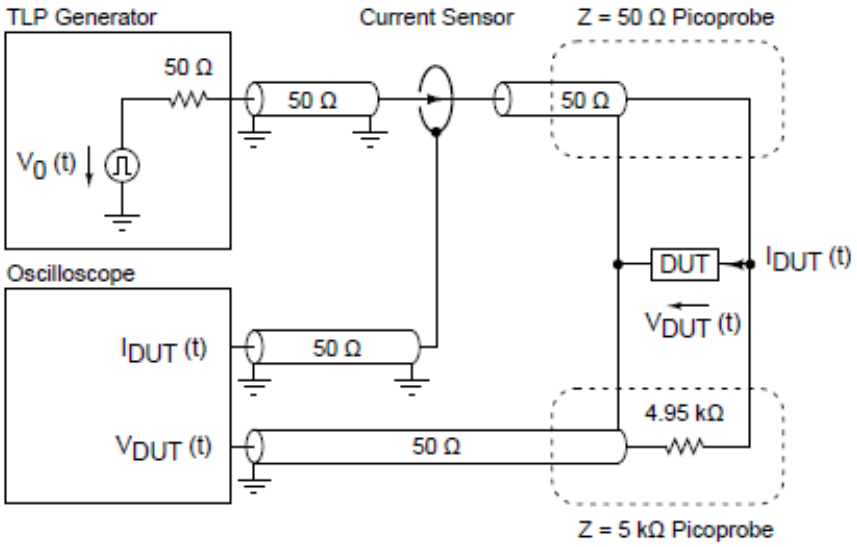
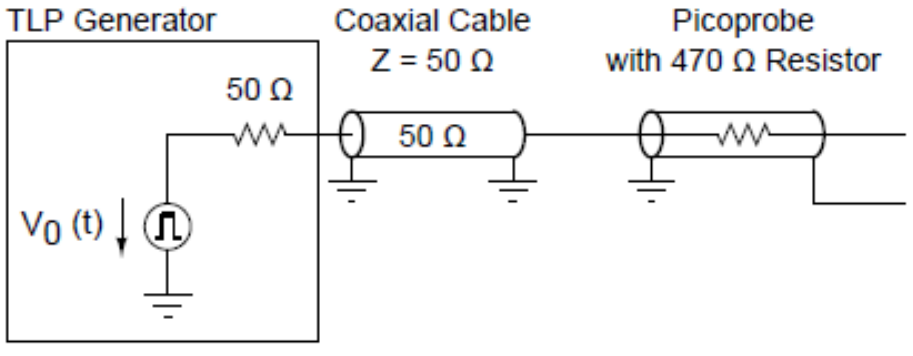
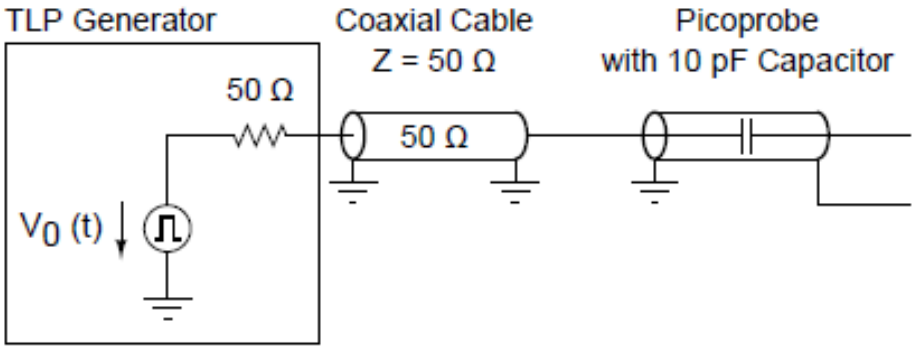


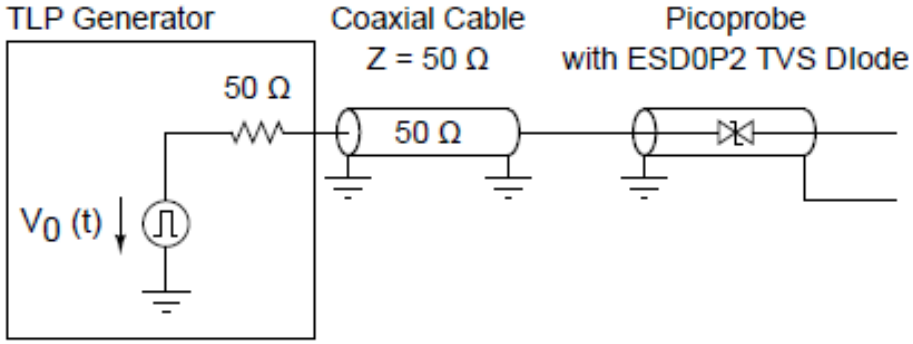
Figure 2.1. Conductive TLP measurement setup.



(a) Resistive probe tip.



(b) Capacitive probe tip.



(c) Ultra-low calacitance TVS probe tip.

Figure 2.2. TLP pulse force probe tip configurations.

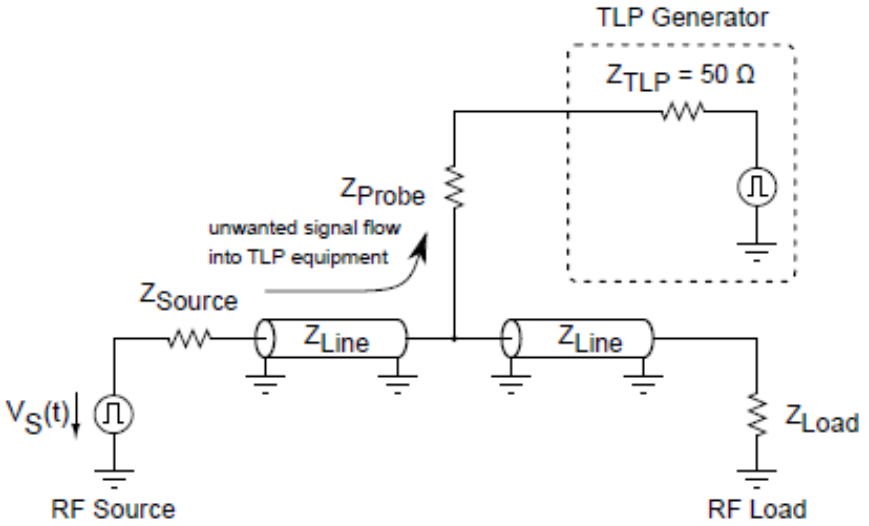
2.2. SYSTEM LEVEL TESTING USING HIGH IMPEDANCE PROBES

Detecting soft failures caused by ESD/EMI can only be done if the injection test equipment is isolated from the powered operating system. Figure 2.3a shows the configu-

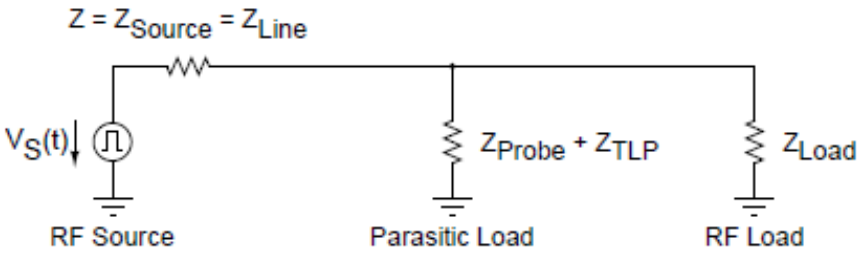
ration of a conductive TLP injection setup for powered system level tests. From the system equivalent circuit in Figure 2.3b it can be seen that the TLP injection setup adds a parasitic shunt impedance

$$Z_{\text{InjectionSetup}} = Z_{\text{Probe}} + Z_{\text{TLP}} \tag{2.1}$$

to the system connected between the data line and ground. $Z_{\text{InjectionSetup}}$ is responsible for signal distortion and reflections along the RF/data transmission line. Therefore the signal integrity of the powered system is violated. In order to avoid the unwanted parasitic load a highly isolating solution for Z_{Probe} has to be applied.



(a) Conductive TLP pulse force configuration.



(b) Equivalent circuit of conductive TLP injection setup.

Figure 2.3. TLP system connected to RF/high-speed data line.

2.3. RESISTIVE AND CAPACITIVE PROBES

Common approaches for conductive injection in to powered systems are probes with a high nominal value resistor, Figure 2.2a, and probes with a coupling capacitance, Figure 2.2b. Both resistive and capacitive probes have several drawbacks when pulsing in to powered systems, e.g. capacitive and resistive probes deform the applied current pulse, limit the signal bandwidth and limit the maximum TLP current injected to the system.

Figure 2.4 shows a 5 A TLP current pulse in to a 50 Ω load delivered through a 470 Ω resistive, a 10 pF capacitive and a 200 fF TVS diode probe as described in Figure 2.2. The capacitive probe is only conductive as long as the voltage across the capacitor changes with time. Therefore according to

$$I(t) = C \cdot \frac{dV}{dt} \tag{2.2}$$

where $I(t)$ is the time dependent current, C is the capacitance and dV/dt the time derivative of the voltage, the square wave TLP current pulse is deformed to a current spike. This leads to a drastically decreased testing and investigation flexibility as the wave form parameters rise time and pulse duration become non-effective. Resistive probes decrease the current capability of the test system due to the increased current source impedance, e.g. for a 470 Ω probe the current capability of a 50 Ω TLP pulse source is decreased by a factor of nearly 10.

A further drawback of both resistive and capacitive probe is the lower isolation capability of the test equipment from the net under test when there is no ESD pulse applied. Recalling 2.2 and Eqn. 2.1 the isolation of the test equipment is determined by the impedance added to the data lines.

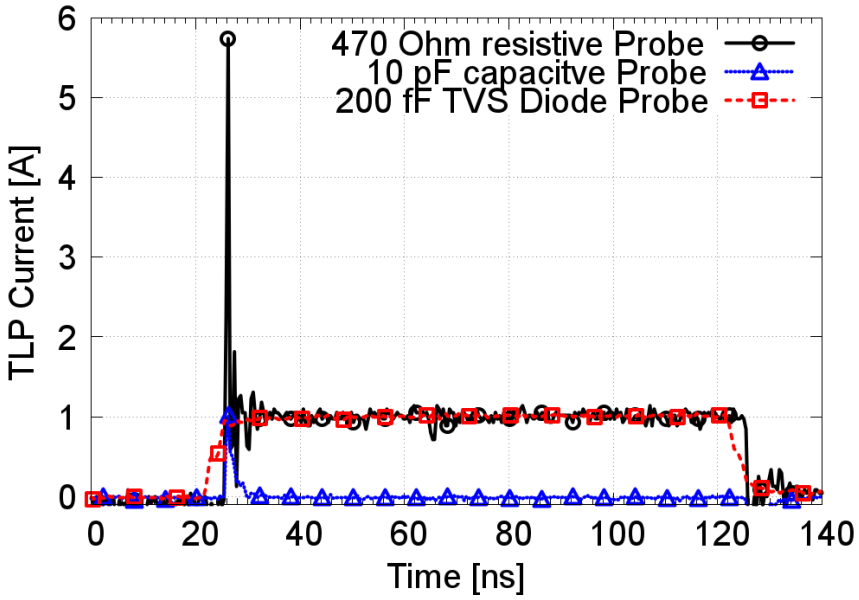


Figure 2.4. Comparison of 1A TLP current pulse delivered into a 50 Ω load using different injection probe concepts.

Table 2.1. Impedance of injection probe plus 50 Ω TLP source at f = 1GHz.

	Capacitive Probe (10 pF)	Resistive Probe (470 Ω)	TVS Diode Probe (200 fF)	TVS Diode Probe (100 fF)
Impedance in [Ω] at 1 GHz	65	520	795	1590

The calculated impedance can be directly related to the isolation performance and applicability to different data rates and frequencies. A higher impedance comes with a applicability to higher data rates and higher frequencies.

2.4. TRANSIENT VOLTAGE SUPPRESSOR DIODE PROBE CHARACTERIZATION

Using a TVS diode instead of a resistor or a capacitor in the probe has several benefits. To ensure the TVS diode used in the probe isolates the TLP system from the powered application the insertion loss of the TVS diode is determined by measuring its scattering parameters [3].

Figure 2.5 shows the insertion loss up to 20 GHz extracted from the scattering parameters of two different TVS diodes. The measurements were taken with a vector network analyzer (VNA) in a configuration according to Figure 2.3a. The diodes were placed instead of Z_{Probe}. The VNA was connected to the source and load ports. The junction capacitance, package bond wire and leakage current of the TVS diode mainly determine its frequency dependent impedance in the non conducting state. Due to the low junction capacitances, 100 fF and 200 fF, as well as the low bond wire inductance of 0.4 nH, the signal attenuation, respectively insertion loss, is less than 0.3 dB up to 7 GHz for the 200 fF diode and less than 0.2 dB up to 10 GHz for the 100 fF diode. The DC leakage current for both diodes is in the sub nA regime and is too low to have a significant contribution to the insertion loss. When a current pulse is applied to the system under test the TVS diode triggers, becomes conducting and the current pulse can flow into the system under test. Figure 2.6 shows the TLP I/V curve of the 200 fF TVS diode. The diode triggers at 10 V and then enters its low impedance regime with a dynamic resistance of 1.4 Ω. The TVS diode is turned on for the time of the applied current pulse and Z_{Probe} in Figure 2.3a equals the dynamic resistance of the TVS diode.

The time domain transition waveform from off-state to on-state is shown in Figure 2.7. The turn on time in Figure 2.7 and Figure 2.8 is defined as the time when the voltage at and current through the diode has reached steady state. The rapidly decaying

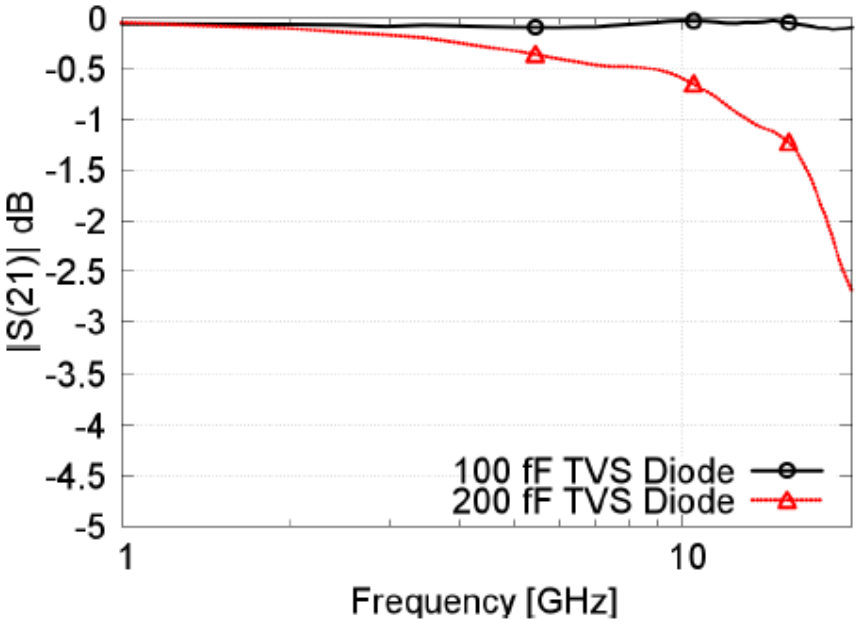


Figure 2.5. Insertion Loss of a 0.2 pF and a 0.1 pF TVS Diode

voltage overshoot in the first 3 ns causes a slight rounding of the current pulse delivered through the TVS diode and in to the system. Figure 2.8 shows comparison between a TLP current pulse delivered through a normal probe in to a 50 Ω load and through the TVS probe.

Figure 2.9 shows a 1 kV IEC 61000-4-2 pulse in to a 2 Ω target through two different probe configurations measured using the test setup in Figure 2.10. Both probe configurations, 100 fF and 200 fF TVS diode, hardly disturb the IEC 61000-4-2 current waveform. The higher current peak of the 200 fF TVS diode in Figure 2.10 is caused by the higher capacitance, according to Eqn. 2.2.

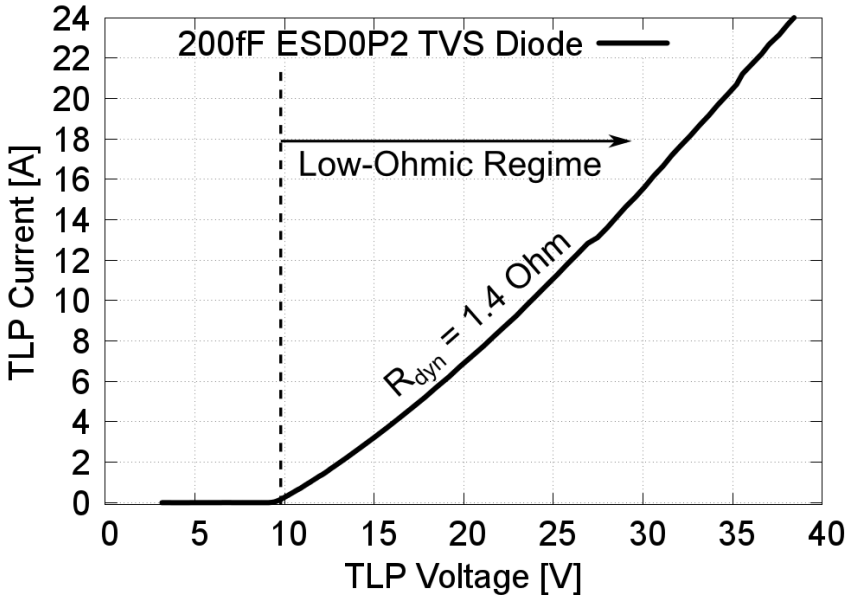


Figure 2.6. 200 fF ESD0P2 TVS Diode TLP I/V curve; trigger voltage Vtrig = 10 V, dynamic resistance Rdyn = 1.4 Ω

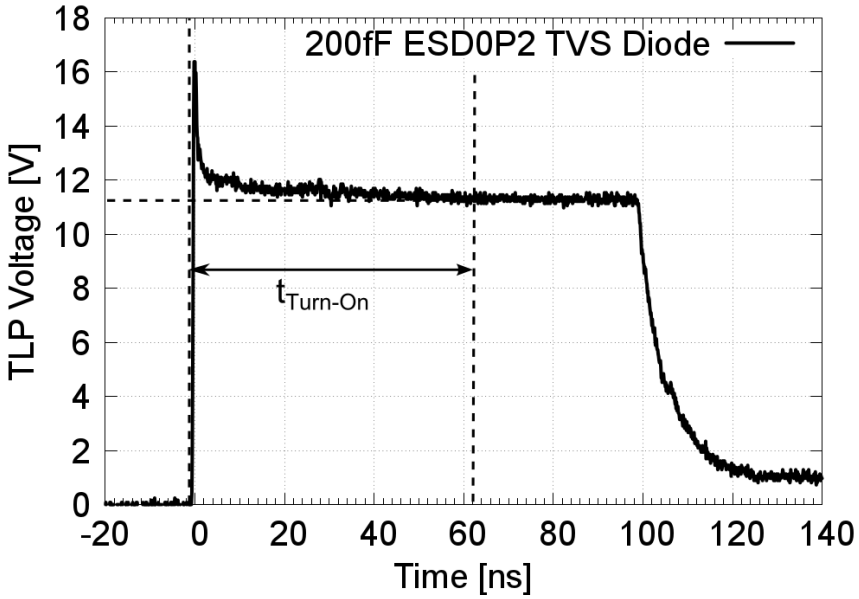


Figure 2.7. TLP Voltage waveform of the ESD0P2; Turn-on time tTurn-On = 60

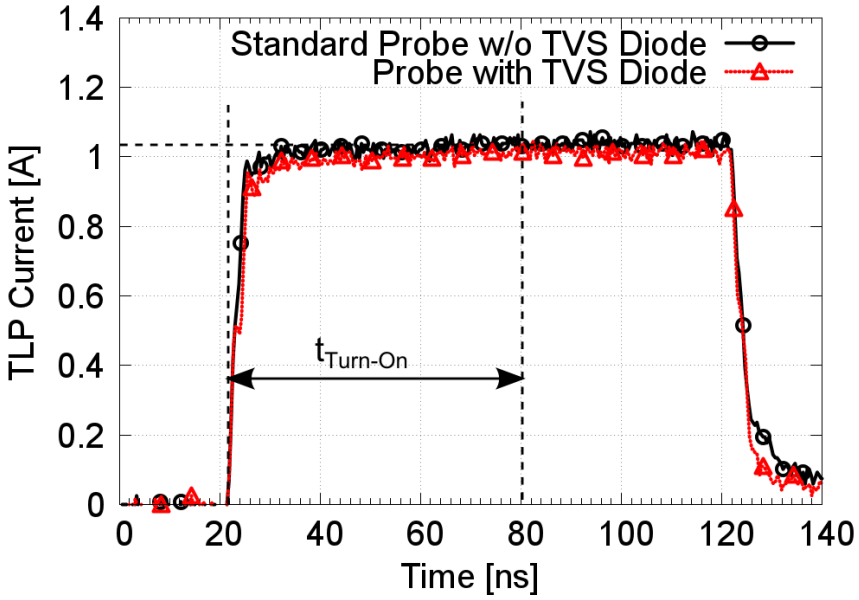


Figure 2.8. TLP current wave forms applied into 50 Ω load using TVS diode probe and standard probe.

2.5. PROBE PARASITICS

The injection probe consists of a TVS diode either implemented in a GGB PicoProbe Model 10 [4] or a TVS diode soldered on a PCB which is placed within the pulse force line. Figure 2.11 shows the TVS diode directly implemented in to the PicoProbe right after the probe tip. In Figure 2.12 the PCB version of the probe is shown.

Besides the 50 Ω source impedance of the pulse generator further parasitic elements are brought in to the system by the coax cables used to connect the injection point to the pulse source. Figure 2.13a shows the equivalent circuit of a coaxial cable or transmission line. For simplification in Figure 2.13 the resistive elements accounting for power losses in the cable were omitted.

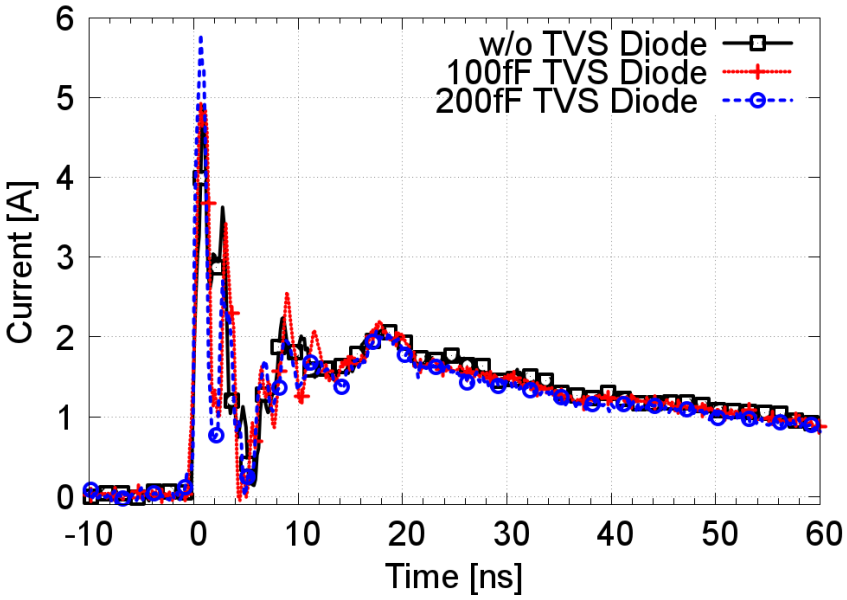


Figure 2.9. IEC61000-4-2 1 kV Pulse shape into 2 Ω target w/o TVS diode, with 100 fF TVS Diode and 200 fF TVS Diode.

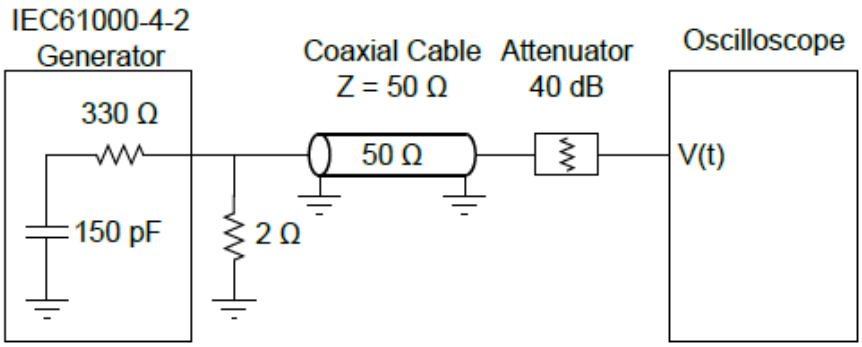


Figure 2.10. IEC61000-4-2 pulse source verification setup.

In Figure 2.13b the TVS diode is mounted directly after the probe tip and all following elements are isolated from the powered system. With increasing distance of the diode from the probe tip the parasitic elements added to the net under test increase. To evaluate the influence of the distance between probe tip and diode the scattering parameters

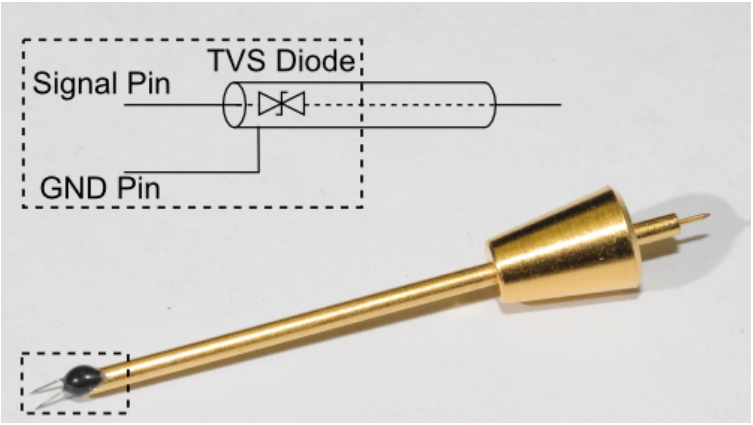


Figure 2.11. TVS Diode implemented on GGB PicoProbe Model 10.

of a 50 Ω trace with the probes in Figure 2.11 and Figure 2.12 attached were measured. Figure 2.14 shows the insertion loss of the two configurations.

Whereas the probe with TVS diode included in the PicoProbe (blue curve) shows a behavior as expected from the measurement in Figure 2.5, the pcb mounted TVS diode (red curve) indicates a resonance at 2.79 GHz and a 3 dB cut-off frequency of 2 GHz. The resonance at 2.79 GHz is caused by the parasitics of the coaxial cable between probe tip and TVS diode. Even in the undamped region below 1 GHz the probe can have an influence on the transferred signal, e.g. for differential data lines the attached probe can change the electrical length and increase the intra pair skew. A common measure for such effects and in general for characterizing a system's signal integrity is the eye diagram. The eye diagram is an oscilloscope measurement where consecutive bits of a data stream are superimposed over another. Figure 2.15 shows the eye diagram of a USB 3.0 transmission channel without a probe attached. The measurements were done according to the USB 3.0 standard and compliance specification [5]. The red rhombus in the middle is the so called eye mask and indicates the minimum opening of the eye.

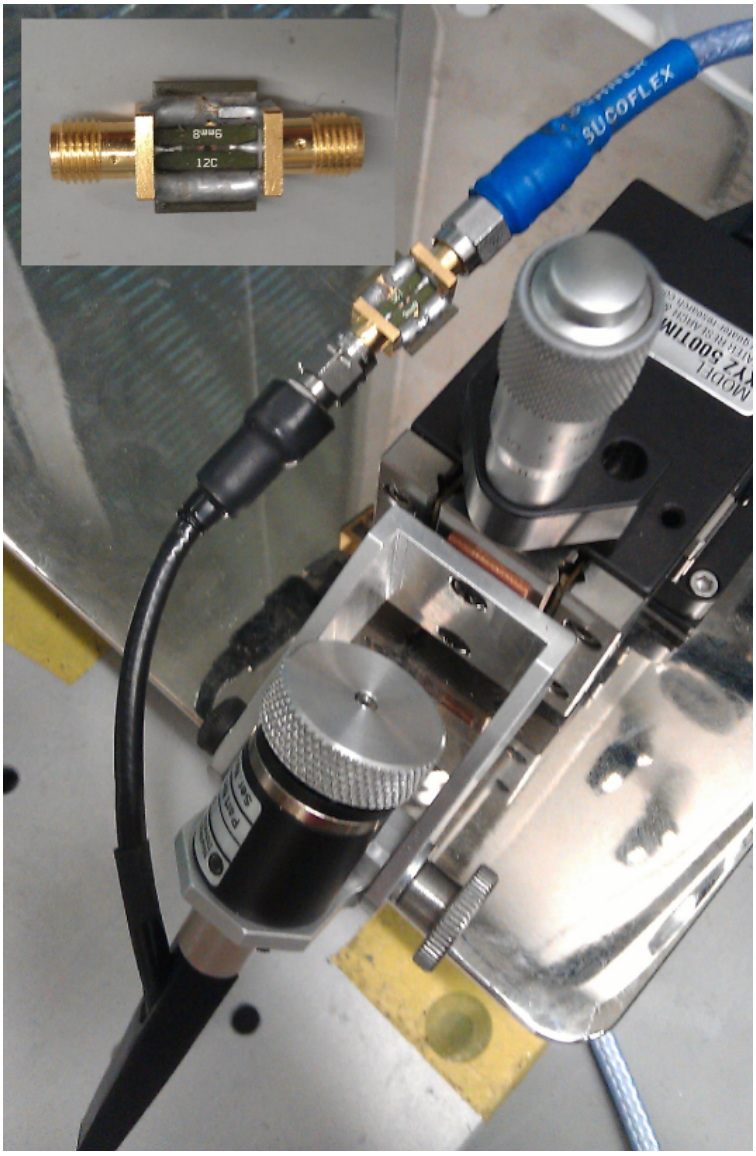
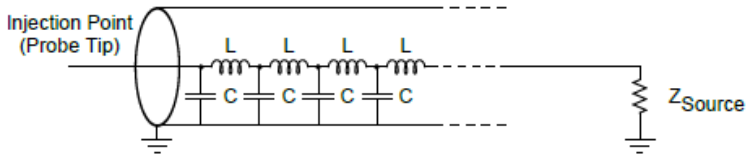
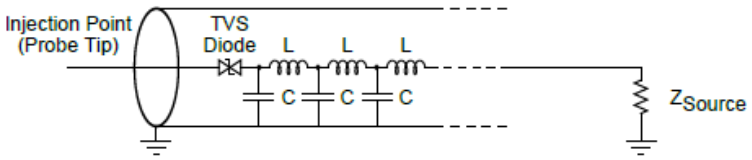


Figure 2.12. TVS Diode attached on PCB.

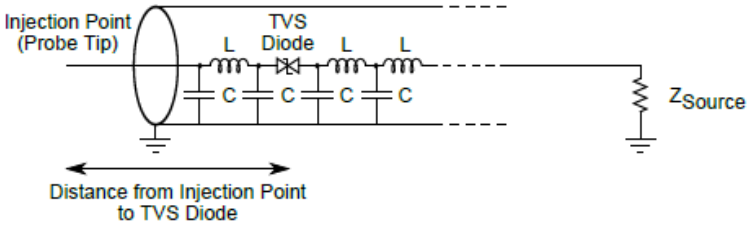
Comparing Figure 2.15 and Figure 2.16 the eye didn't change significantly due to the attached probe. In Figure 2.17 the probe as shown in Figure 2.12 is attached and the eye is almost closed because of the increased distance between injection point and TVS diode. Furthermore the bit error rate (BER) is increased, indicating the USB 3.0 channel is not



(a) Without TVS.



(b) TVS located directly at the injection point.



(c) TVS embedded in transmission line.

Figure 2.13. Coax cable equivalent circuit with TVS diode placed at different distance from injection point.

working within its specifications anymore. The BER is an extrapolated measure from the eye diagram typically plotted in a so called ”bathtub” plot, Figure 2.18 and Figure 2.19.

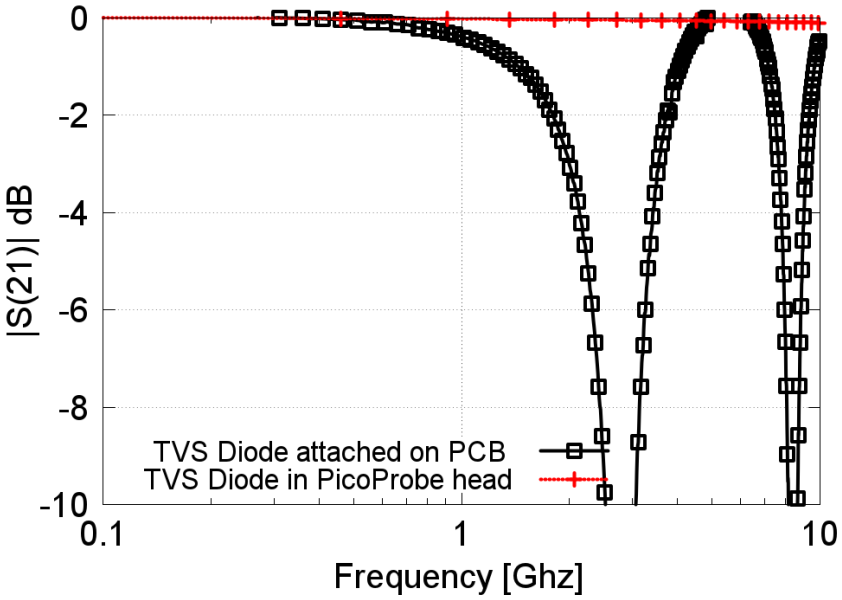


Figure 2.14. Insertion Loss of TVS Diode implemented in GGB PicoProbe Model 10 and TVS Diode attached on PCB.

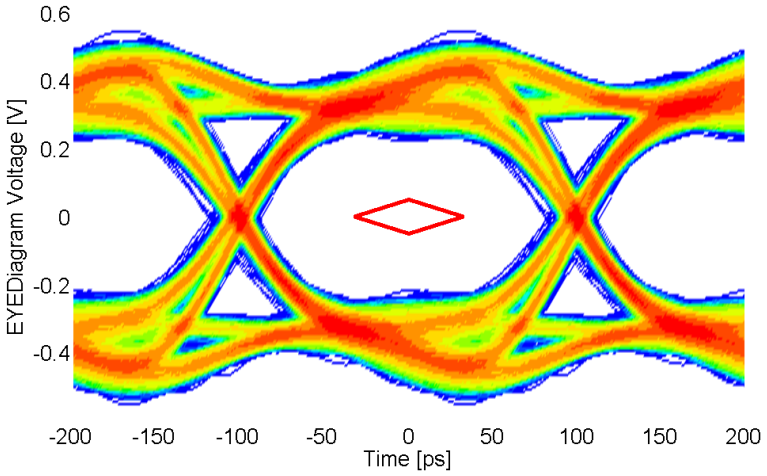


Figure 2.15. Eye Diagram of USB3.0 transmission channel w/o probe attached.

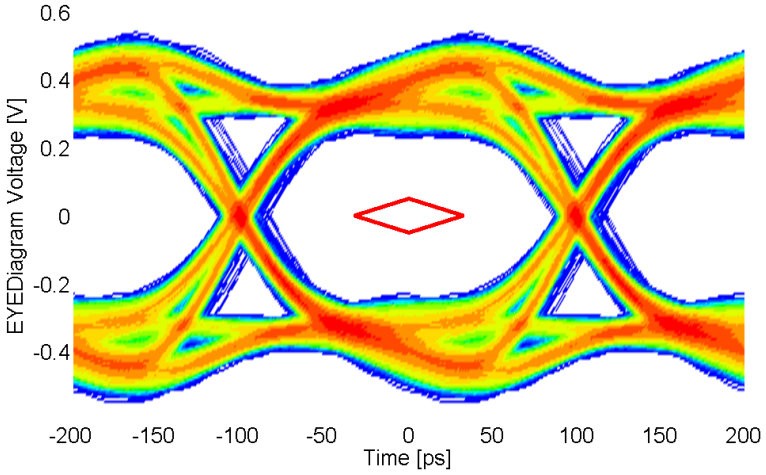


Figure 2.16. Eye Diagram of USB3.0 transmission channel with TVS diode in PicoProbe head attached.

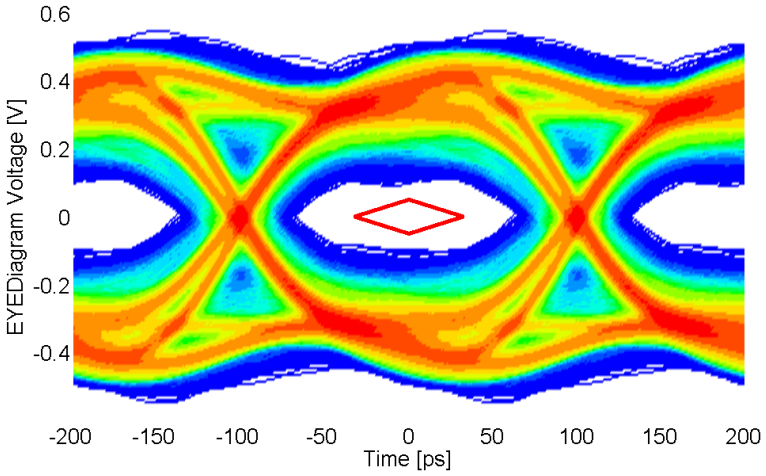


Figure 2.17. Eye Diagram of USB3.0 transmission channel with PCB mounted TVS diode probe attached.

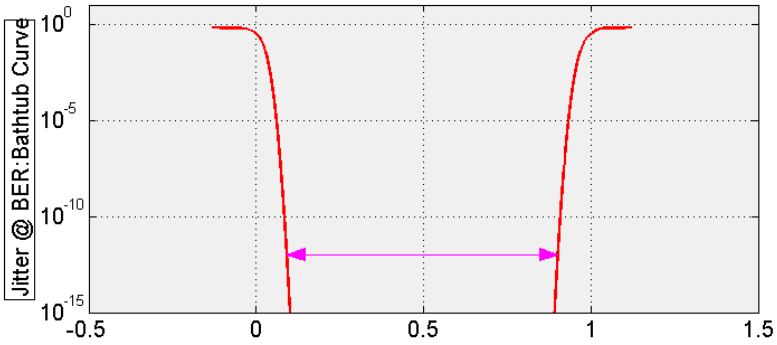


Figure 2.18. BER of USB3.0 Transmission Channel with TVS diode in PicoProbe head attached.

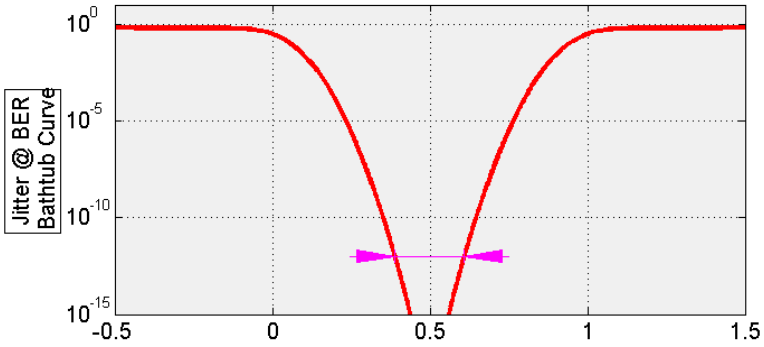


Figure 2.19. BER of USB3.0 Transmission Channel with PCB mounted TVS diode probe attached.

3. VERIFICATION OF THE DIODE INJECTION ON A FUNCTIONAL SYSTEM

In order to test this new probe, we analyzed a mobile phone's camera subsystem with a MIPI bus using a clock frequency of 250 MHz. The TVS diode probe was used to inject current in to one MIPI data line and to isolate the TLP from the signal path. The measurement setup is shown in Figure 3.1 and Figure 3.2. The waveforms at the lines were measured using a probe with a 4.95 kΩ attenuating resistor in the probe tip, which has a sufficiently high impedance to avoid signal disturbance.

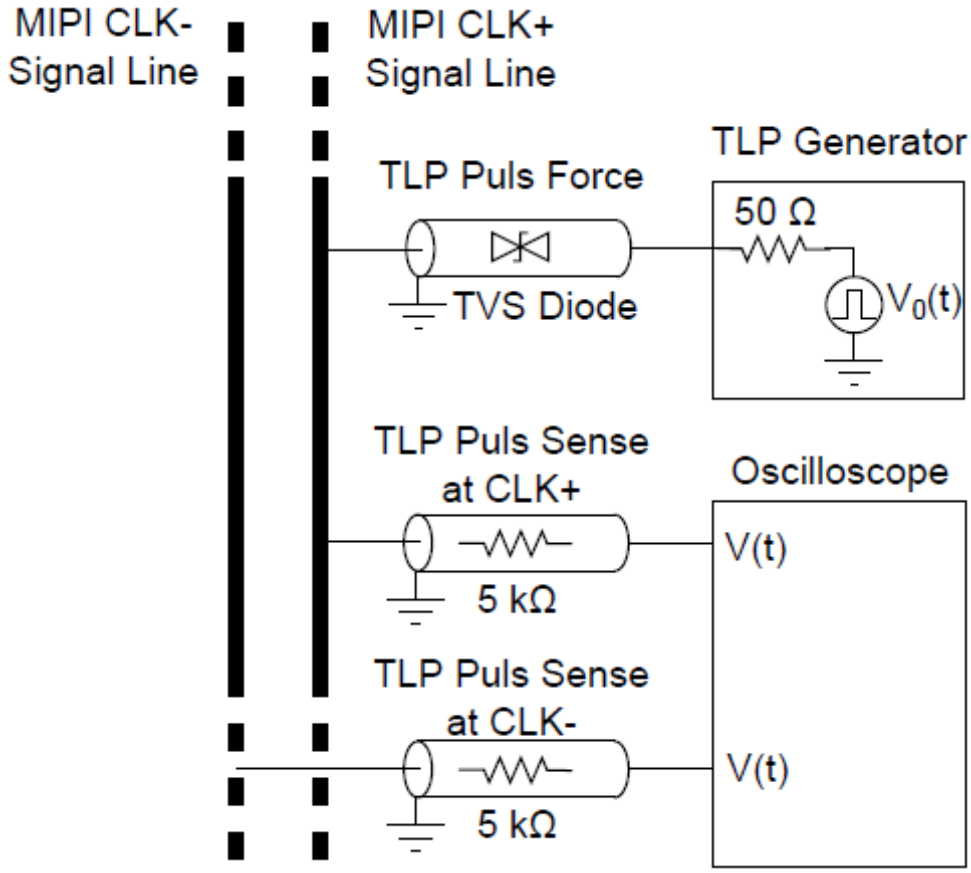


Figure 3.1. MIPI Bus TLP injection setup.

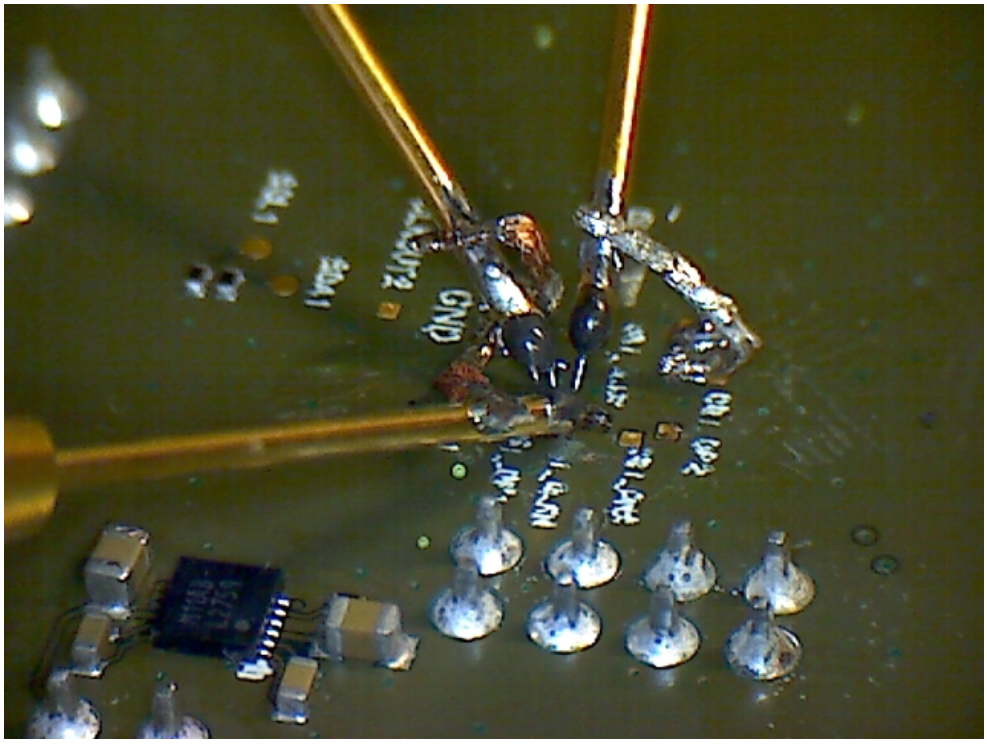


Figure 3.2. MIPI Bus TLP injection setup.

The lines were then evaluated for their susceptibility to pulses that would cause soft failures in the camera system, e.g. glitches on the screen, frozen screen, hang up of the camera software.

By setting the TLP step voltage to a small value (1 V), we created a situation where each pulse was not significantly greater in magnitude from the previous. This allowed us to a) create a very detailed IV curve and b) apply repeated pulses of essentially the same magnitude, reducing the chance that a failure due to a particular amplitude regime would be missed.

Figure 3.3 shows the extracted I/V curve from the captured voltage and current TLP waveforms. The captured waveforms clearly show the presence of a clock signal with

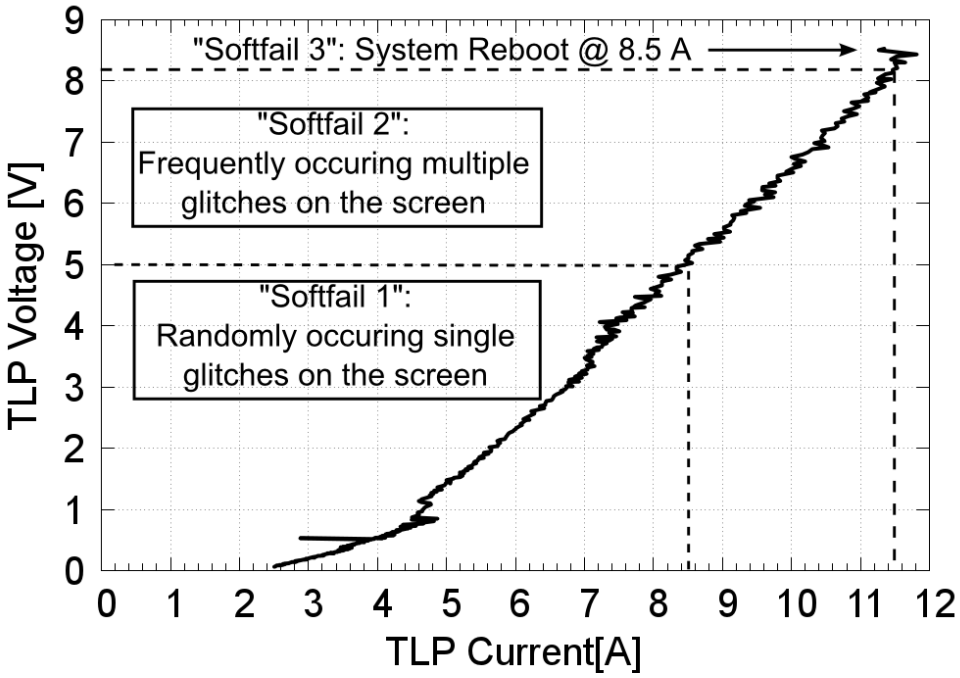


Figure 3.3. Measured TLP I/V curve on the MIPI bus with mapped soft failure levels.

250 MHz on the net when the pulse arrives, Figure 3.4. In comparison, the camera could not even be operated when a 50 Ω probe was used to pulse in to the MIPI bus.

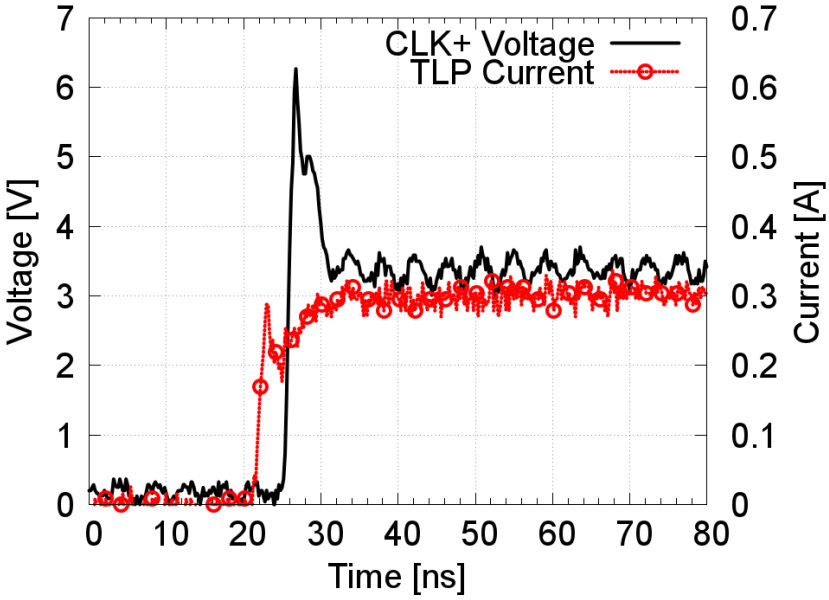


Figure 3.4. TLP pulse that arrives between data frames.

4. CONCLUSION

A TLP injection test has been presented which allows the assessment of stress pulse susceptibility at high speed data lines by high impedance test probes. In comparison to capacitive and resistive probes the applicability of TVS diode probes by means of data rates, frequency and stress levels is much more flexible. The TVS diode probe does not change the applied wave form independent of the used ESD pulse generator and its source impedance.

The selection criteria for the TVS diode used for the probe is determined by the application data rate and frequency. Scattering parameters and eye diagrams can be used to characterize the TVS diode probe's influence on the signal integrity of the system. As a rule of thumb it can be said that a TVS diode that can be used to protect a certain application can also be used within the TVS diode probe to test the system. Another selection criteria is the diode's trigger voltage as shown in Figure 2.6. The trigger voltage determines the lowest voltage level that can be applied to the system under test. In case lower stress levels are necessary a diode with a lower trigger, respectively breakdown voltage has to be chosen. Care has to be taken on the placement, respectively the distance between TVS diode and injection point. The parasitic capacitance of cabling between injection point and TVS diode can drastically reduce the applicable frequency range of the probe. With the 100 fF TVS diode soldered on a PCB an easy to build probe is realized that can be used for applications below 1 GHz. The GGB PicoProbe Model-10 TVS Diode probe can be used for ultra fast applications as it was shown for USB 3.0 (5 Gbit/s).

5. ACKNOWLEDGEMENTS

The authors want to thank GGB Industries for prototyping the customized PicoProbe Model 10 with included TVS diode.

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II. A SYSTEMATIC METHOD FOR DETERMINING SOFT-FAILURE ROBUSTNESS OF A SUBSYSTEM

Benjamin Orr, Pratik Maheshwari, Harald Gossner, David Pommerenke, and Wolfgang Stadler

ABSTRACT

A systematic method for evaluating soft fail robustness of a DUT subsystem is presented and demonstrated on a camera MIPI interface. Two different mobile phone platforms are studied under TLP injection while various methods for extracting failure thresholds and localization are applied. The root cause for the soft-failure threshold discrepancy is left for future work.

1. INTRODUCTION

The trend for consumer and industrial electronic devices has led to miniaturization and increased integration, resulting in very small devices with a large number of subsystems [1]. In order to improve the ESD robustness of these highly integrated devices, weak subsystems and points of failure must first be identified. Once they are known, targeted measures such as hardening the hardware and software against ESD events and similar surges can be used to reduce sensitivity of these weak points, thus improving the overall robustness of the system. We propose that System Efficient ESD Design (SEED) [2] can be applied to soft-failures, and is one method to approach this.

Much work has been done to mitigate hard-failures which would lead to device destruction and permanent loss of system functionality, but ESD-induced soft-reliability issues such as data corruption and system upsets are also concerns. In order to increase device robustness with respect to soft-failures, a "divide and conquer" approach is presented here. This method begins by dividing a device into discrete subsystems such as communication interfaces, IO interfaces, and other peripherals. Once the subsystems have been identified (divide) then each is subjected to TLP characterization in order to determine their independent robustness (conquer). By splitting the overall characterization into pieces and evaluating the susceptibility of these individual subsystems to direct 50 Ω TLP injection, targeted measures can then be employed to protect vulnerable systems that might exhibit failures during IEC 61000-4-2 testing in the final product. By using this method, an optimization strategy for soft-failures similar to hard failure analysis can be performed as long as the failure can be associated with a pin or pin combination in the susceptible subsystem.

This method is intended to be flexible enough to be applied to any subsystem on a DUT, thus completely characterizing the major IC(s) with respect to soft failure susceptibility. The method is first presented, and then validated on two functionally similar but architecturally different development boards for different mobile phone platforms such as in [3].

2. METHOD OVERVIEW

In order to evaluate a device with respect to its subsystems, failure criteria for each subsystem should be defined. In lieu of enumerating error symptoms and acceptable levels of functionality for all DUTs, the authors have attempted to provide a classification scheme for potential soft-errors which can be applied to many devices. Prior to testing, each subsystem should be identified and assigned an acceptable level of soft failure.

Once the subsystems that are to be tested are identified, specific failure criteria for those subsystems should be described, including their symptoms. This is also a subjective step which requires some consideration of the required device functionality. Note that the very definition of soft-failures precludes hardware symptoms such as DC leakage from being considered. During soft-failure characterization, only software-related symptoms such as a system reset or application crash are considered. Furthermore, the severity of each failure should be considered. For example, the loss of several frames being transmitted from a the video camera of a mobile phone to the main processor may not be considered significant interference, but the same millisecond disturbance on a high speed video camera would cause the loss of valuable information.

Table 2.1. Soft Failure Categorization

Level 1:	Undetected error, the system recovers without operator intervention
Level 2:	Brief but noticeable change in functionality, the system recovers without operator intervention
Level 3:	Change of functionality, the system requires operator intervention to correct
Level 4:	A latent error is introduced into the system that affects an operation not yet performed, the system requires operator intervention to correct

After the acceptable failures have been identified, we begin fault-testing the device. This testing is performed by direct electrical stresses to the subsystem nets during normal device operation in search of soft-failures which were previously defined. These stresses are introduced by direct TLP current injection rather than any of the various "real world" ESD models such as HBM or CDM. This controlled injection [4] allows us to build a quasi-static IV curve for the net/subsystem under consideration which can be used when applying mitigation strategies. Furthermore, this injection scheme helps to build a susceptibility model for each pin based on current/voltage, pulse width, and rise time, and polarity.

The final step in determining a subsystem's robustness is to identify the failing device. A subsystem often consists of a communication scheme which involves at least one transmitter and receiver. Even after a failure has been identified, the actual culprit is often still unknown. In order to completely identify the observed failure we need to determine which component of the subsystem is at fault. Again, because of the number of possible subsystems and their varied functions, a complete list of identification techniques cannot be listed here. However, in the following case studies, the methods that the authors used to identify the source of the failure are described in detail.

Once this method has been applied, the results can be easily compared in search of pins or subsystems (often pin groups) which are significantly weaker than the rest. These weak subsystems can then be improved by applying SEED which is a method of system and IC co-design based on high voltage ESD transient characterization of components as in [5], or by hardening the software or firmware against ESD-induced software glitches [6].

3. SYSTEM, TESTING AND FAILURE DESCRIPTION

In order to evaluate the effectiveness of the method, we used two development boards, both designed for software development and testing. Documentation was provided with each board pertaining to test points, debug ports, and system layout. Both of these development boards were equipped with cameras driven by the Mobile Industry Processor Interface (MIPI) D-PHY hardware interface and the Camera Serial Interface (CSI) software protocol.

To validate these tests, the camera subsystem was chosen because soft-failures that affected either the camera software or the displayed video were easily identifiable on the screen. Furthermore, camera modules of mobile devices tend to be attached to the system via flex-cables, leaving them very susceptible to IEC system-level testing. These factors make the camera an ideal subsystem to study our characterization methodology.

In order to detect soft failures, the camera software on the respective systems was started and placed in 'viewfinder' mode which generated a continuous stream of data from the camera to the processor. Next, we define the acceptable soft failure threshold as Level 3; an error that required user intervention to correct either by restarting the application, or power cycling the device. During testing on DUT 1, the most common failure was found to be screen 'tearing' where multiple frame fragments moved across the screen and obscured the view. For DUT 2, the most common soft failure was a software-reported crash where an error message was presented to the user and the application required a restart. Note that while the errors were symptomatically different, both required the user to restart the viewfinder application, but left the system otherwise unaffected.

Once errors were identified, several methods to determine the actual point of failure in the system were employed. Using these methods the points of failure were tracked to different endpoints on each DUT. Ultimately, these tests would culminate with an identification of the physical mechanism that caused the failure such as latch-up, ground bounce, PDN noise, or crosstalk. However, this is not a trivial task and is left for future work.

Because soft failures can be difficult to both define and identify, several subjective steps must be taken during device characterization. First, the subsystems which are to be considered must be identified and levels of functionality defined. Second, failure criterion should be described and symptoms and detection methods identified. Third, electrical stresses are applied to the system in search of previously defined soft failures. Fourth and finally, the culprit device must be identified in an attempt to localize the failure.

4. DUT 1: MEASUREMENTS AND OBSERVATIONS

In the case of DUT 1, several test points on the MIPI nets which are supplied for protocol analysis. These test points were easily adapted to TLP injection points. Because of the significant loading that the TLP and measurement systems can inflict on the DUT, high impedance voltage probes and diode-isolated injection probes [7] (shown in Figure 4.1 were used for injection and measurement. By using these probes, we ensured that the high speed bus functioned correctly while being probed. This is shown in Figure 4.2. For all TLP measurements, the current and voltage values are extracted by averaging over a window inside the pulse plateau as shown in Figure 4.3. A block diagram of the test setup is shown in Figure 4.4.

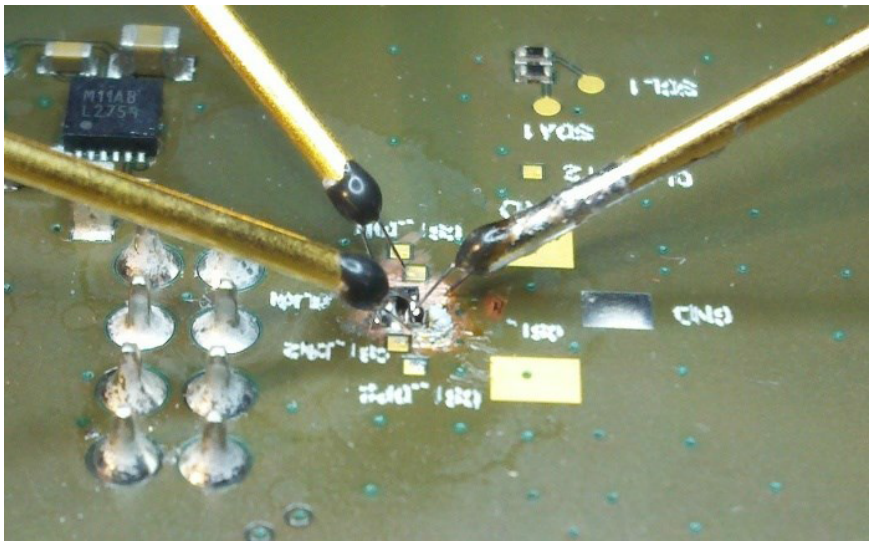

Figure 4.1. Measurement and Injection Probes

In order to measure the net susceptibility, the pulse polarity, width, and rise time were varied during each amplitude sweep. By setting the TLP step voltage to a small value

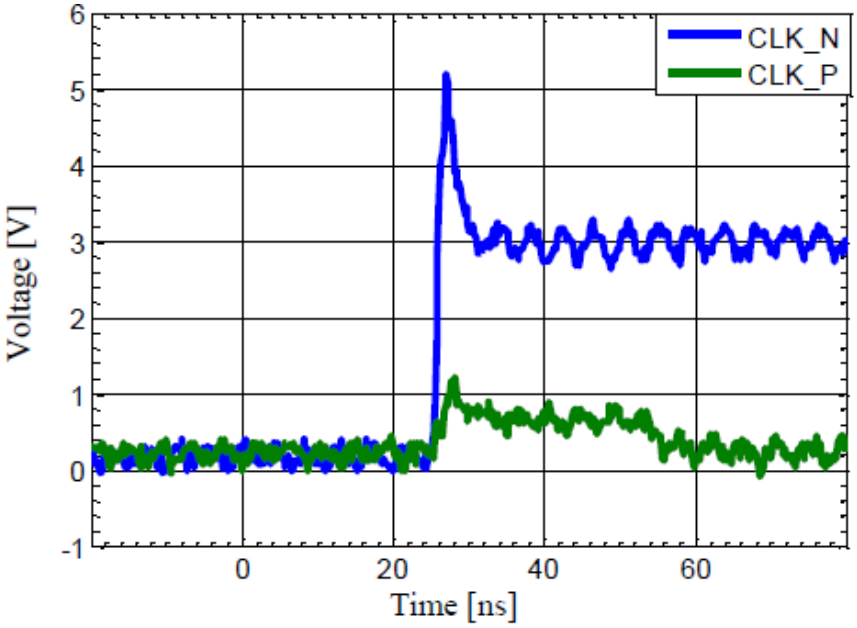

Figure 4.2. Injected Pulse Superimposed on Clock Line

(1 V), we created a situation where each applied pulse was not significantly different from the previous. This allowed us to: a) create a very detailed quasi-static IV curve and b) apply repeated pulses of essentially the same magnitude to the DUT. This pulse repetition reduced the chance that a failure caused by a pulse in a particular amplitude regime would be randomly missed.

When performing nondestructive testing, there is always the question of how large of a pulse the DUT should be subjected to without inflicting damage. Because DUT 1 was quite robust, we were sometimes able to continue the tests up to 10 A of injected current without error. As this is already quite high, all tests were terminated based on the quasi-static IV curve at a 10 A or 15 V limit. These current and voltage limits were related through the on-state resistance of the clamping diodes present on each of the data and clock nets.

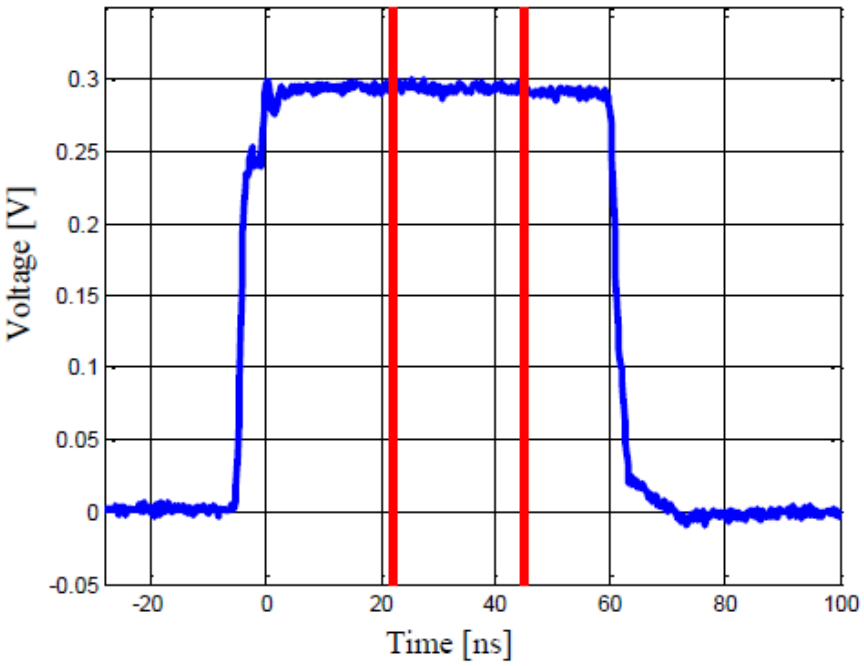

Figure 4.3. Measured TLP Pulse with Averaging Window

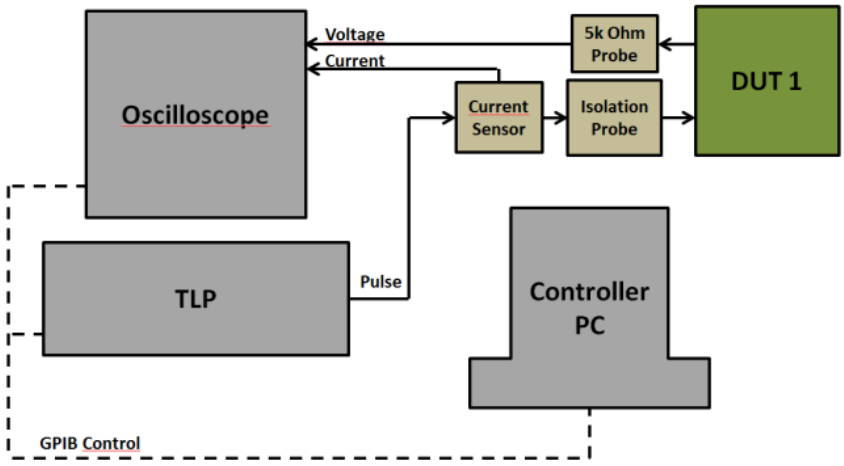

Figure 4.4. Measurement Setup for DUT 1

Often, we would encounter soft-failures prior to reaching the injection limits that we set for the experiment. These soft-failures would appear as screen "tearing", where multiple

frame fragments would be displayed on the screen at a time. These frame fragments would still contain the current image being captured by the camera, but the image was, in effect, distorted. This distortion was considered to be an unacceptable level of soft-failure for DUT 1.

4.1. PULSE POLARITY

As a standard component of each test, the polarity of the pulses was toggled, in order to build a characterization for each net with respect to bipolar signals. This was found to be a critical test, as the differential data pairs only exhibited repeatable soft failures during negative pulses. Figure 4.5 shows the positive test, and prematurely terminated negative test. Note the termination of the test at approximately −5 A was due to soft failures observed at several sequential pulses, not merely a single failure.

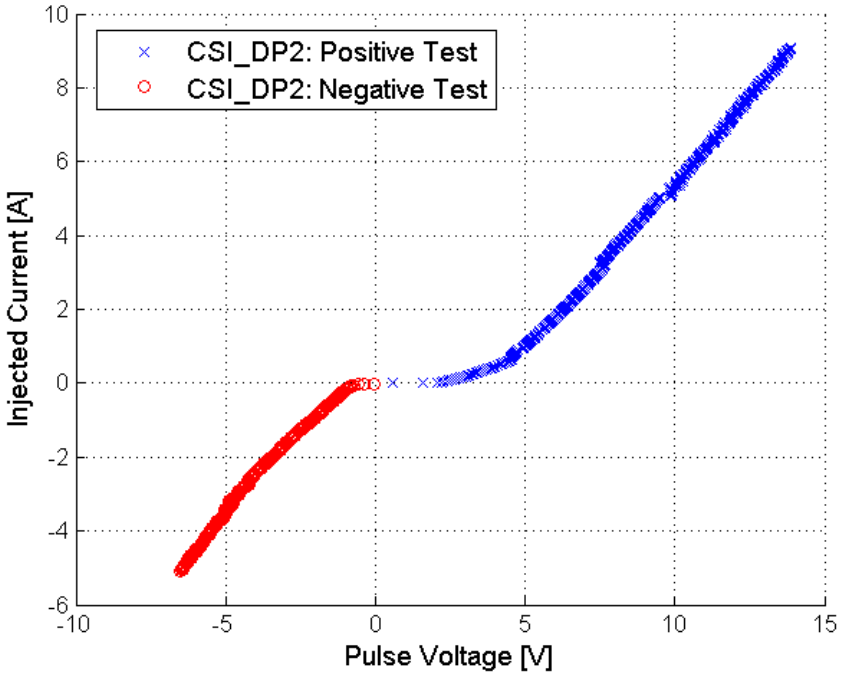

Figure 4.5. Negative Quasi-Static IV Curve Truncated due to Multiple Sequential Failures

4.2. PULSE RISE TIME

Using a TLP with a series of discrete rise time filters, we were able to test the DUT with respect to the rise time of the pulse. Continuing with the medium pulse width (65 ns), the rise time was approximately logarithmically swept from 0.1 ns to 10 ns. This test was performed on both sides of the differential nets and, as expected, no variation in failure threshold was observed with the rise time. Since this variable seemed to be inconsequential for this interface a rise time of 100 ps was used for all remaining tests.

4.3. PULSE WIDTH

After a repeatable failure was identified on the data nets during negative pulses 65 ns wide, the pulse width was swept through several non-equispaced values. This was done with the help of a TLP featuring a switched charge line system. Each test was terminated when the DUT exhibited several sequential soft failures, ensuring that spurious errors were not mistaken for true error thresholds.

Analysis of the quasi-static IV curves shown Figure 4.6 revealed that the tests were terminated at increasingly lower magnitudes of injected current for longer pulse widths. Although it is difficult to determine a precise value for the failure thresholds, using the first current value of the beginning of the failure sequence shows a clear dependence on pulse width. This dependence is shown in Figure 4.6.

4.4. FAILURE ANALYSIS

Once a failure was observed, the next step was to identify the source. In order to determine the point of failure we first need to consider the subsystem. In this experiment the subsystem is the very simple case of a camera which is transmitting a data stream to the

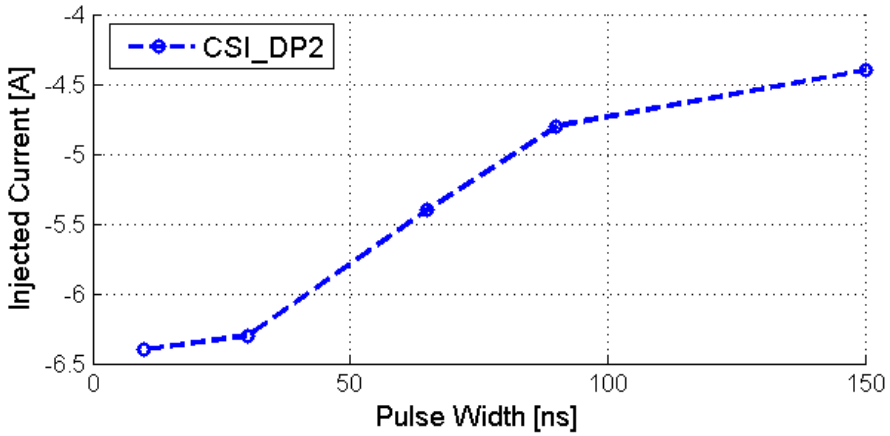

Figure 4.6. Approximate Failure Current with respect to Pulse Width

application processor (AP). Since this is a unidirectional transmission, the processor must either fail to receive the correct information, or the transmitter must fail to send the correct information.

In order to determine the point of failure, we looked into the data that was being transmitted over the channel. One method to do this would be protocol analysis. However, protocol analysis can require expensive instrumentation that can easily be affected by the pulse injection. To avoid these issues, we examined the spectrum of the magnetic fields surrounding the camera rather than the transmitted data itself.

In order to do this, we first established a predictable data pattern in the data stream. This pattern was established by covering half of the camera with an obstruction, which lead to the corresponding half of the displayed screen to be dark as shown in Figure 4.7. Conveniently, the data stream is broken into logical blocks, each about 45 ms long which corresponds to a frame rate of 22 fps. This can be observed by placing a magnetic field probe (Figure 4.8) over the camera module and connecting it to a spectrum analyzer set to zero-span mode. With this measurement setup, a consistent time-domain shape was

observed at many frequencies of the camera's data transmission. Measurements at any one of these frequencies were found to be repeatable over several measurements prior to the pulse injection.

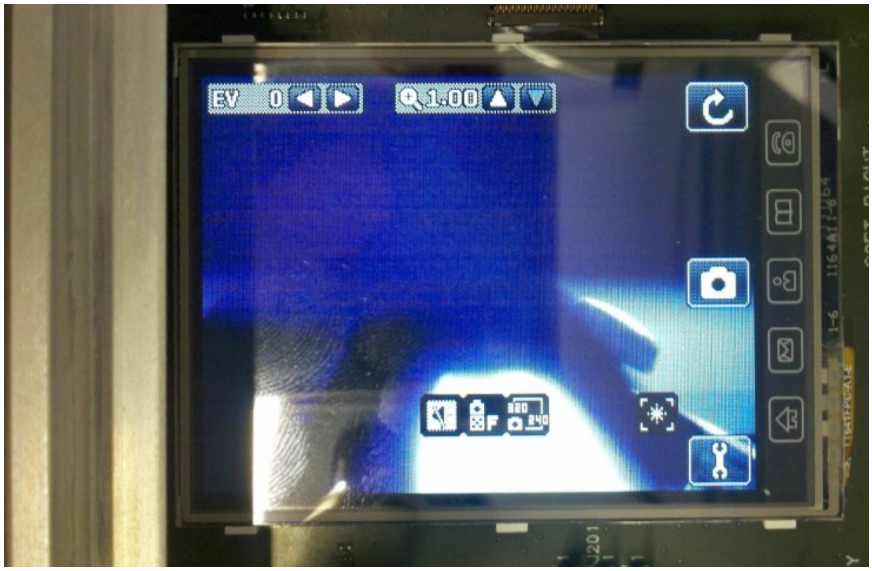

Figure 4.7. Camera Obstruction

Once this time-domain pattern was found, the spectral component was measured using the same magnetic loop probe. This probe is a small trace on a PCB which encloses a loop area of 5 mm^2 and has a unity relative permeability ($\mu_r \approx 1$). The probe was fixed above the camera module and measurements were taken both before and after the disturbance to observe the shape of the data spectral component.

In order to determine the failure origin, the time-domain shape of the frequency component was compared before and after the soft-failure event. In this case, the failure was a screen 'tearing' artifact shown in Figure 4.9, which required the user to restart the camera application. To investigate the root of the failure, the magnetic fields above the camera were observed both before and after the failure and found to consistently change as a result of the injection. The camera obstruction is visible in the frequency data (shown

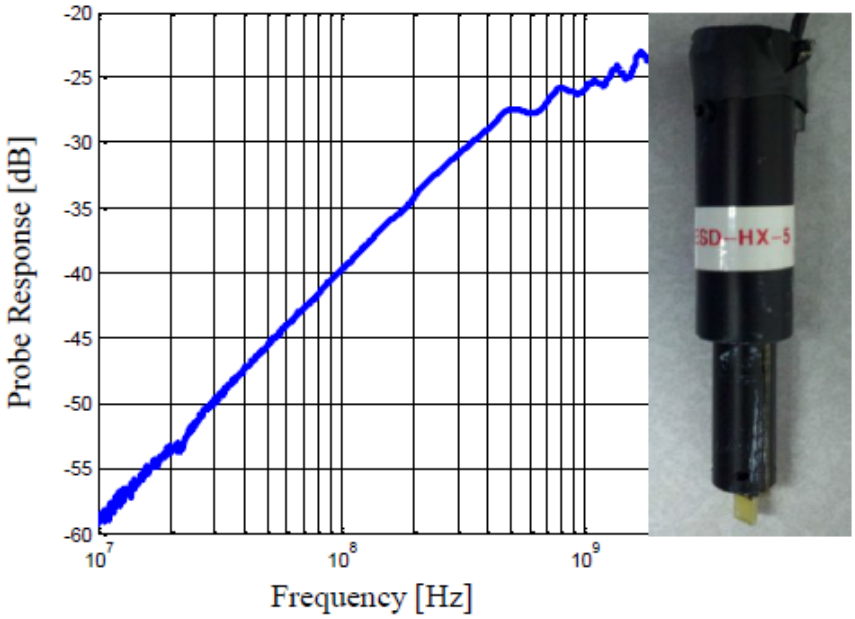

Figure 4.8. 5 mm Magnetic Field Probe

in Figure 4.9) as the lower amplitude portion of the frame. By observing a magnetic fields change above the camera, we conclude that the data transmitted by the camera has changed because of the pulse. Since this is a purely relative measurement technique, probe calibration is irrelevant and not considered here. It is important to note that because the data is broadband in nature, the zero-span center frequency was swept until we found a consistent time-domain shape. During this scanning technique, care was taken to not confuse clock harmonics with data signals.

Figure 4.9. Screen Tearing on DUT 1

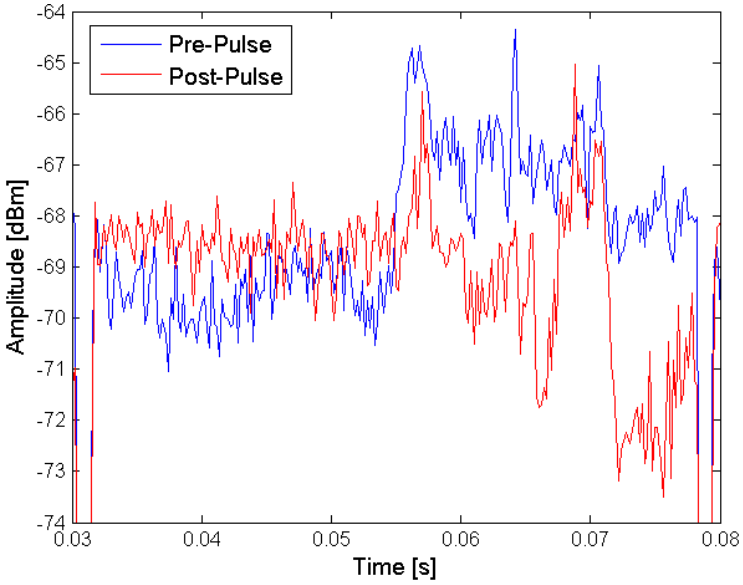

Figure 4.10. Magnetic Field Scan over the Camera on DUT 1

5. DUT 2: MEASUREMENTS AND OBSERVATIONS

In the case of DUT 2 which is an android-based mobile development platform, test points on the MIPI interface were available for voltage probing and TLP noise injection. Direct injection was performed on the DUT with the same isolation probes used on DUT 1. The setup used for evaluating the soft-error robustness to ESD is shown in Figure 5.1.

To begin tests, the TLP voltage was initialized to 6 V during both polarity tests and was varied in steps of 1V to obtain a fine-resolution quasi-static IV curve. Each test was repeated multiple times to ensure that the observed error thresholds consistently fell within the same range. The voltage and current values at each pulse were calculated by taking an average over the stabilized pulse waveform, in the same manner as the tests on DUT 1.

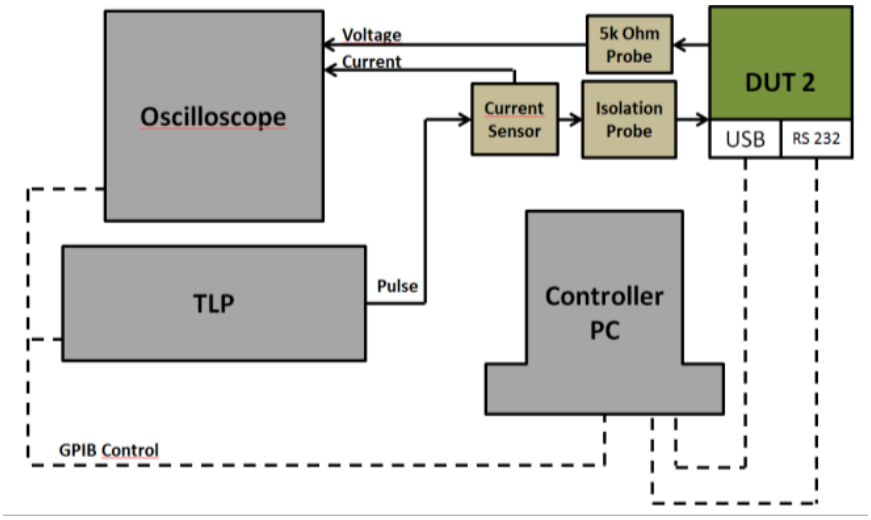

Figure 5.1. Measurement Setup for DUT 2

Unlike DUT 1, the soft-error exhibited by DUT 2 was in the form of an error message that was presented to the user following the crash of the camera software. An example of this failure is shown in Figure 5.2. Because this error was recognized by the system as

an error in software, we were able to take advantage of the availability of system log files. These logs are generated by the device operating system and document both normal device function, as well as errors. This is in contrast to DUT 1 which did not provide any software support. Using this error log, we were able to observe the failures in real time from the perspective of the system, rather than relying on a comparing of the system parameters before and after the soft failure.

Figure 5.2. DUT 2 Failure Symptom

5.1. PULSE POLARITY

The first tests were performed with pulse width of 70 ns, and 100 ps rise time, and were continued until repeated failures were observed. Figure 5.3 shows the quasi-static IV curve for CSI_DAT0_N. These values were chosen to be similar to the values used to test DUT 1. Eventually, many pulse widths and rise-times were examined.

This dual-polarity test indicates that DUT 2 behaves quite differently than DUT 1. It is clearly more susceptible to positive TLP injection than negative TLP injection. As shown, for negative pulse polarity the repeated failure occur around −250 mA while failures due to positive pulses can be observed for currents as low as 20 mA. It is important to note however, that both positive and negative failure levels observed for DUT 2 are approximately one order of magnitude lower than the levels observed for DUT 1. This is an especially interesting difference considering the relative similarity of the devices in terms of functionality.

5.2. PULSE WIDTH

After determining a difference in susceptibility to pulse polarity, the tests were continued using a varied pulse width until repeated failures were observed. Similar to DUT 1, increasing the pulse widths reduced the magnitude of the current required to induce repeated failures. Unlike DUT 1 where failures are only observed during negative pulses, the same pulse width dependence is observed for both positive and negative injection. The approximate failure thresholds with respect to pulse width are shown in Figure 5.4 and Figure 5.5.

5.3. FAILURE CULPRIT

The next step was to perform root-cause analysis in order to determine the source and type of error. To accomplish this, two methods were employed: near-field scan and reading software error logs. Due to an identical data transmission scheme between camera and device on DUT 2, the magnetic field scanning procedure introduced for DUT 1, was used on DUT 2.

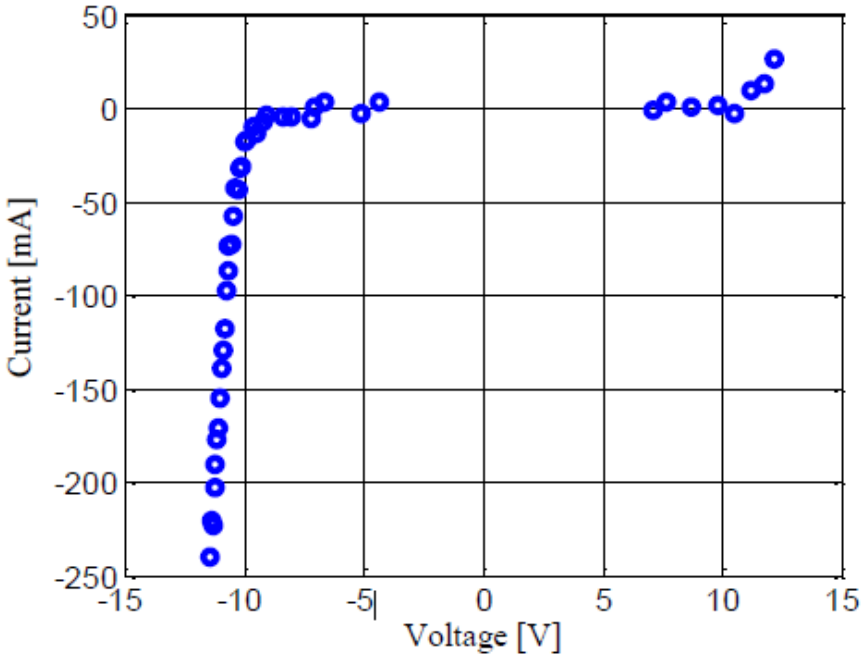

Figure 5.3. Quasi-static IV Curve for MIPI_DAT0_N on DUT 2 (70 ns Pulse Width)

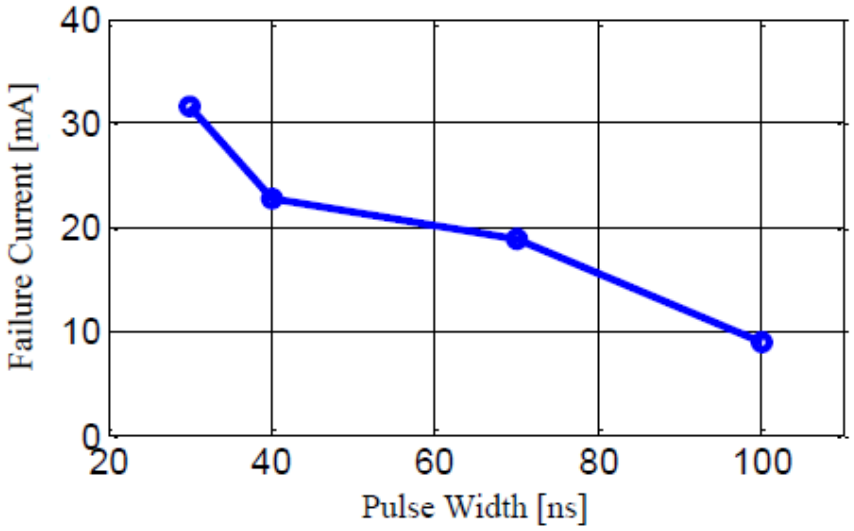

Figure 5.4. Approximate Failure Current Dependence for Positive Injection with Respect to Pulse Width

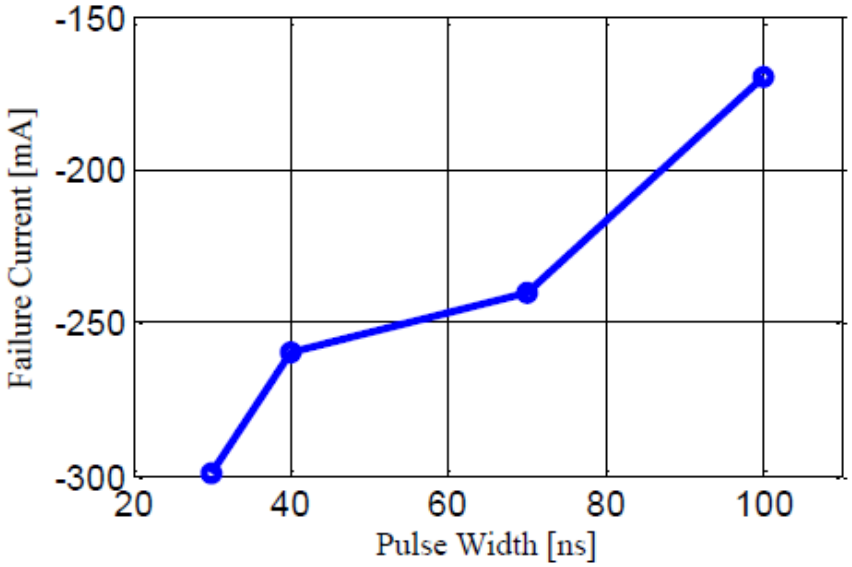

Figure 5.5. Approximate Failure Current for Negative Injection with Respect to Pulse Width

To repeat these tests, the camera on DUT 2 was partially obstructed which yielded a consistent frame shape in the spectral components of the data. The remainder of the scan procedure performed on DUT 1 was then repeated on DUT 2. To determine the origin of the failure, the data pattern was observed and captured while the field probe was placed directly over the camera during the pulse injection. Next, the camera data bus is pulsed until the soft-error is observed. Finally, the time-domain of spectral components are again captured and compared to those observed prior to the soft-failure. The results from camera scan are shown in Figure 5.6.

The portion of the frame which corresponds to the obstruction is visible as the lower amplitude half of the observed magnetic field at 207.8 MHz. After comparing the results, there appears to be only minimal change between the magnitude and shape of the data signals at 207.8 MHz before and after soft-failure. However, this alone is not sufficient proof that the data transmission was not changed, as it is possible that the soft-failure was

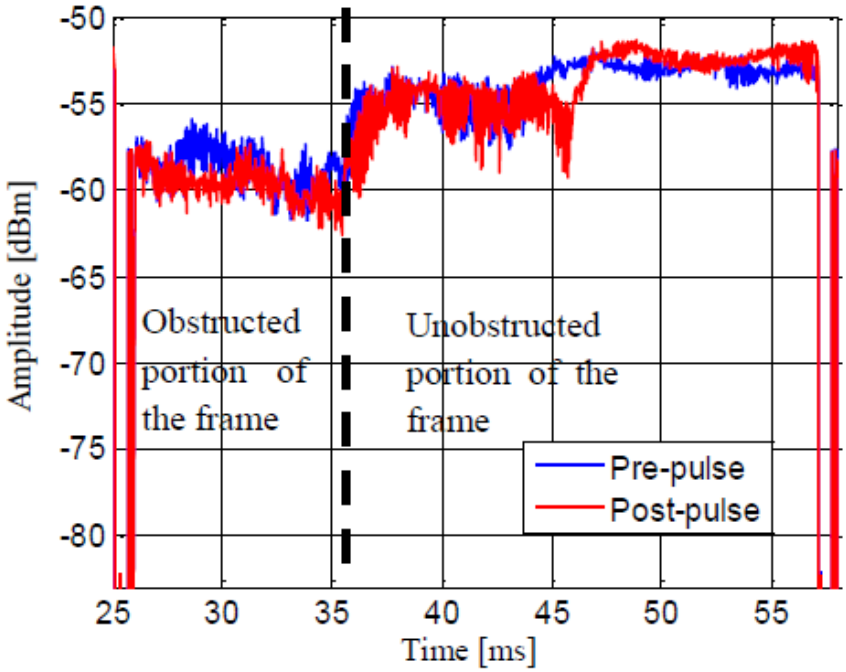

Figure 5.6. Magnetic Field Scan over Camera on DUT 2

caused by a phase change in the signal which leads to a synchronization loss. Such a phase change would not be visible by observing only the magnitude of the magnetic field.

5.4. SOFTWARE ERROR LOG

The second method used to determine the root cause of the soft failure was to analyze the device error logs. Because DUT 2 runs an android-based operating system, a software tool called Android Debug Bridge (ADB) was available which allowed us to easily read out the device error logs. During soft-failure testing, these logs revealed a timeout error was thrown by the camera software. This timeout error was observed to correspond with the injected pulse, and displayed error message. Upon review of the Android source code, it appeared that this error is normally thrown in response to a lost acknowledgement

signal that triggers a camera interrupt, further leading to an application crash. From this we concluded that the error is caused when the application processor fails to read the data being sent by the camera.

6. CONCLUSION

In this paper a method for determining soft-failure thresholds for DUT subsystems is presented and validated on two different DUTs. Although being architecturally different, these DUTs are functionally very similar, yet exhibit a large difference (an order of magnitude) in softfailure robustness as well as different error signatures on the camera subsystems. Using an EM scanning method and read-out of system logs, the failure location and culprit device were successfully determined for both DUTs. While DUT 1 shows a failure related to malfunction in data transmission at several Amps of ESD current, DUT2 throws a system upset in response to ESD injection even when no major signal change could be detected. DUT 1 is intrinsically robust against soft fails of the MIPI subsystem. Thus, no additional effort would be need when constructing a final end-user application, DUT 2 requires significant effort in shielding and on-board protection to realize an IEC safe mobile system. Based on the extracted failure current thresholds the dimensioning of the protection can be performed.

This investigation demonstrates an essential step towards assessing IC/PCB circuit architecture and firmware of subsystems regarding IEC ESD stress susceptibility as requested by SEED.

7. ACKNOWLEDGEMENTS

The authors would like to thank Thomas Schwingshackl for his contributions to several early measurements of DUT 1, without him, these measurements would have been far more tedious than they already were.

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III. A PASSIVE COUPLING CIRCUIT FOR INJECTING TLP-LIKE STRESS INTO ONLY ONE END OF A DRIVER/RECEIVER SYSTEM

Benjamin Orr, David Johnsson, Krzysztof Domanski, Harald Gossner, and David Pommerenke

ABSTRACT

In this paper, a simple passive circuit is presented which allows TLP stress and characterization pulses to be injected into only one side of a driver/receiver system. The circuit is simulated and tested, demonstrating the possibility for directional current injection on the order of 60:1. The circuit also provides a method for measuring both injected currents when paired with a typical TLP system.

1. INTRODUCTION

In order to gain a better understanding of the soft failure robustness of a system, there is interest in evaluating the robustness of the individual components of that system. These components may have a diverse set of ESD protection strategies as well as failure envelopes and signatures. Therefore, it is useful to understand the limitations and characteristics of each component so that protection strategies can be implemented which complement the strengths and shore up the weaknesses of each part of the system [1].

To evaluate the robustness of individual components (usually ICs) of a system to ESD phenomenon with respect to soft failures the components need to be placed in a functioning state to replicate the real-world use cases [2]. This often means that there must be an established connection on a driver/receiver channel, requiring a second component (hereafter: ADUT) to be directly connected to the DUT. This necessary connection between driver and receiver complicates the evaluation and characterization of the DUT by introducing a second ESD current path and point of failure which can be unintentionally excited by stress pulses intended for the DUT 1.1.

In this paper, we present a passive circuit which can be placed between a driver and receiver (or arbitrary DUT/ADUT) which is capable of coupling TLP [3] stress pulses into the DUT with minimal effect on the ADUT with minimal effect on the communication channel. This technique is referred to as Directionally Coupled Injection (DCI). In addition to DCI, this circuit also provides a noninvasive mechanism to measure the current injected into the DUT. If the total TLP current is also measured, the current into the ADUT can also be calculated, providing a complete picture of the current distribution during the injection.

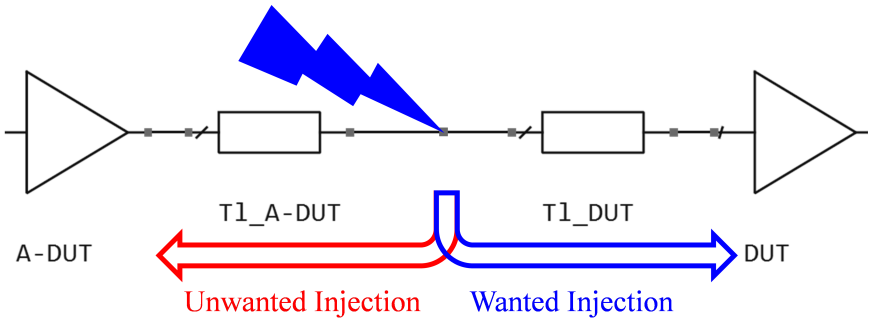


Figure 1.1. Current Injection Problem

In simulation, the directionality of the injection is demonstrated to be effectively infinite. In practice, similar directionalities can be obtained, but typically only in ranges of 1 to 2 amps before the circuit must be retuned.

2. CIRCUIT DEVELOPMENT

In order to couple a signal directionally into a net, a two-winding transformer, similar to that found inside of a passive current transducer is used in conjunction with a compensation circuit which forces one node of the transformer to a virtual ground (VGND) as shown in Figure 2.1. This virtual ground is only visible to the applied pulse, and does not interfere with the normal operation of the DUT/ADUT system.

In this paper, the injection-side winding of the transformer is referred to as the primary winding and the net-side winding of the transformer is referred to as the secondary winding. The transformer reflects the injection source onto the secondary side of the transformer, placing it in series with the net under test (NUT). The transformer turns ratio is chosen to balance the injection source impedance which is reflected into the NUT with the equivalent reflected voltage source. Because the reflected equivalent source appears to be in series with the NUT, it is only capable of driving the DUT with respect to the ADUT. To achieve a unidirectional injection, the VGND is established at the ADUT terminal of the secondary winding during the pulse injection. This VGND is created by injecting a current into the VGND node which is equal to the current flowing through the secondary winding. The result is that no current is drawn from the ADUT.

2.1. TRANSFORMER PARAMETERS

Because the secondary winding of the transformer is inside the signal path, care should be taken to minimize its effect on the signal. Two additional concerns are the magnitude of the equivalent pulse source reflected into the NUT and the PCB layout area of the injection circuit. The transformer parameters used in simulation and circuit

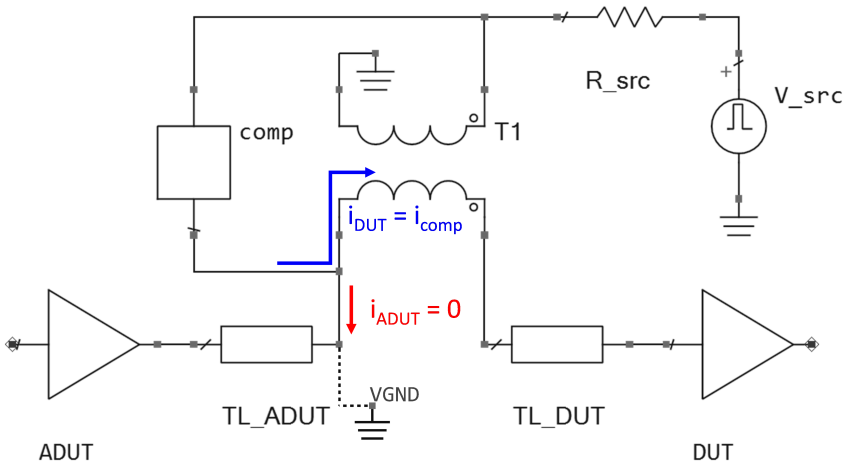


Figure 2.1. Compensated Transformer Injection Concept

Table 2.1. Coupled Inductor Properties

Parameter	**Value**	**Unit**
$\mu_{r,initial}$	10 000	none
Turns Ratio	7	none
$L_{primary}$	150	µH
$L_{secondary}$	3	µH

implementation are shown Table 2.1. A turns ratio of seven reflects a 50 Ω interference source into the NUT as a voltage source with one seventh the magnitude of the injected pulse with ≈ 1 Ω ($50/7^2$) of series resistance. This turns ratio can be adjusted to scale the pulse source magnitude and series impedance. A description of current transformer design and optimization can be found in [4].

2.2. ESTABLISHING THE VIRTUAL GROUND

In order to establish a virtual ground point, a portion of the pulse delivered by the TLP is used to feed the VGND. We will refer to this branch as the compensation path. To

understand the compensatory action, we simply sum the currents leaving the VGND, set the ADUT current to zero, and solve for the required IV characteristic of the compensation path. Performing this analysis shows that the relationship between the DUT characteristic and compensation coupling circuit is identically the turns ratio of the transformer. To demonstrate this, the DUT is approximated by a resistor and a diode voltage drop to simulate piecewise linear diode operation and the compensation path is similar but scaled by the turns ratio simulating a piecewise linear Zener diode. A simplified SPICE simulation demonstrates this compensation current equalization principle. The schematic is shown in Figure 2.2 and the compensation and DUT currents are shown in Figure 2.3.

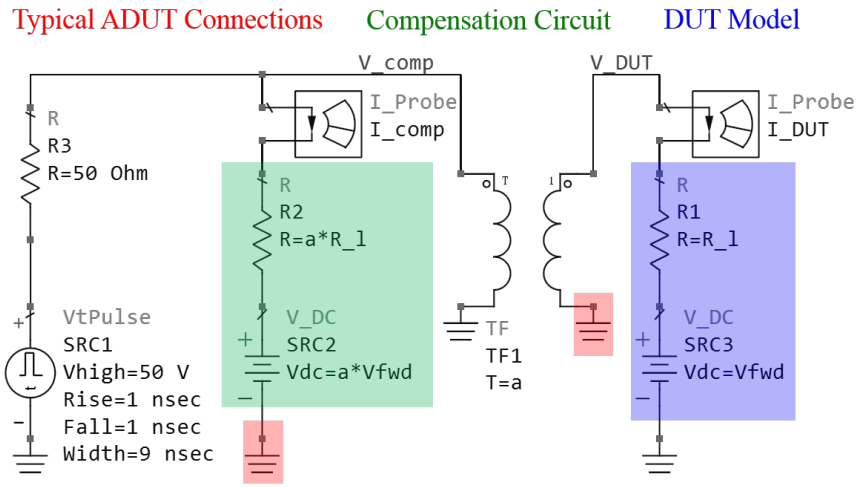


Figure 2.2. Matching the compensation circuit to the load

In this case, the voltage induced on the DUT node by the transformer $TF1$ is reduced by a factor of the turns ratio a from the source voltage. Writing the equations for the compensation current I_{comp} and DUT current I_{DUT} as functions of the voltages on the respective nodes we have the following:

$$i_{DUT} = \frac{V_{DUT} - V_{SRC3}}{R_1} \tag{2.1}$$

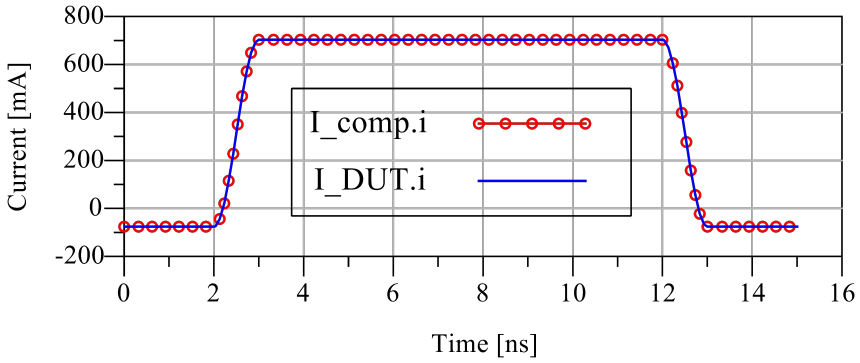


Figure 2.3. Comparing the compensation and DUT currents

$$i_{COMP} = \frac{V_{COMP} - V_{SRC2}}{R_2} \tag{2.2}$$

And by defining the relationships between the equivalent diode voltages and on-state resistances, and the inherent relationship between the compensation and DUT node voltages due to the transformer we see that:

$$V_{comp} = a * V_{DUT} \tag{2.3}$$

$$V_{SRC2} = a * V_{SRC3} \tag{2.4}$$

$$R_2 = a * R_1 \tag{2.5}$$

$$\frac{a * V_{DUT} - a * V_{SRC3}}{a * R_1} = i_{DUT} = i_{comp} \tag{2.6}$$

Therefore showing that if the relationship a is held, the compensation circuit delivers a current into the VGND which is identical to the current delivered to the DUT. Therefore, the initial assertion of zero ADUT current is realized. In practice, maintaining the relationship across a range of injection currents is difficult. However, maintaining a perfect VGND is not strictly necessary. In practice, the compensation path can be tuned to increase the stability of the VGND (and thus the injection directionality) around the desired injection current range.

2.3. IDEAL CIRCUIT SIMULATION

Beginning with the simulation, we first analyze an ideal case by using a perfect transformer model (Figure 2.4). In this circuit, a winding ratio of 7 is used and nonideal component properties and parasitics are neglected.

The coupling path comprises back-to-back diodes $D3$ and $D4$ along with $R14$. Given that the DUT load is a single diode in each polarity, the assumed 0.7 V drop dictates a 4.9 V drop across the compensation path which is achieved by a 4.2 V reverse breakdown and additional 0.7 V forward breakdown voltage of the series $D3$ and $D4$ combination. Given the on-state resistance of the DUT load diodes as 1 Ω, 7 Ω was selected as the series resistance of the compensation path. The on-state resistances of $D3$ and $D4$ was limited by the simulation environment to a minimum of 100 μΩ but is assumed to have a negligible contribution to the total resistive component of the compensation path. In addition to the transformer and compensation circuit, an additional resistor ($R15$) is placed in series with the primary winding of the transformer to provide a convenient current sense point for the primary winding current. This measurement can be scaled by a factor of the turns ratio to determine the secondary side current which is the same as the DUT current. Together with a measurement of the total injected current, the directionality can be evaluated. Alternatively,

a measurement of the VGND voltage plotted with the DUT current can also be used as a quality metric.

This additional resistor could be accounted for by reflecting the 1 Ω equivalent resistance across the transformer as a 20 mΩ resistance and lumped into an equivalent load resistance, but this is also considered negligible in this example.

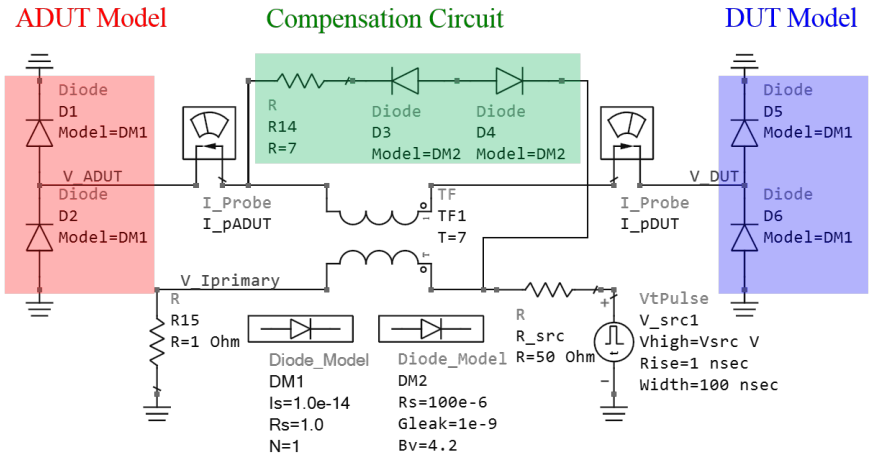


Figure 2.4. Ideal injection circuit simulation

The pulse source is a trapezoidal voltage source with a 50 Ω series resistance. The peak voltage of this source is swept across a batched set of transient simulations to simulate the linearity of the circuit with respect to the DUT current. The results of this simulation are shown in Figure 2.5. The neglected resistances of $D3$, $D4$, and $R15$ contribute to a slight imbalance causing a vanishingly small current to be drawn from the ADUT. The simulation also shows spikes in the ADUT current at the beginning and end of the pulse reach as high as -70 pA in magnitude. This edge distortion is caused by mismatched IV characteristics between the series turn-on behavior of $D3$ and $D4$ as compared to the load $D5$.

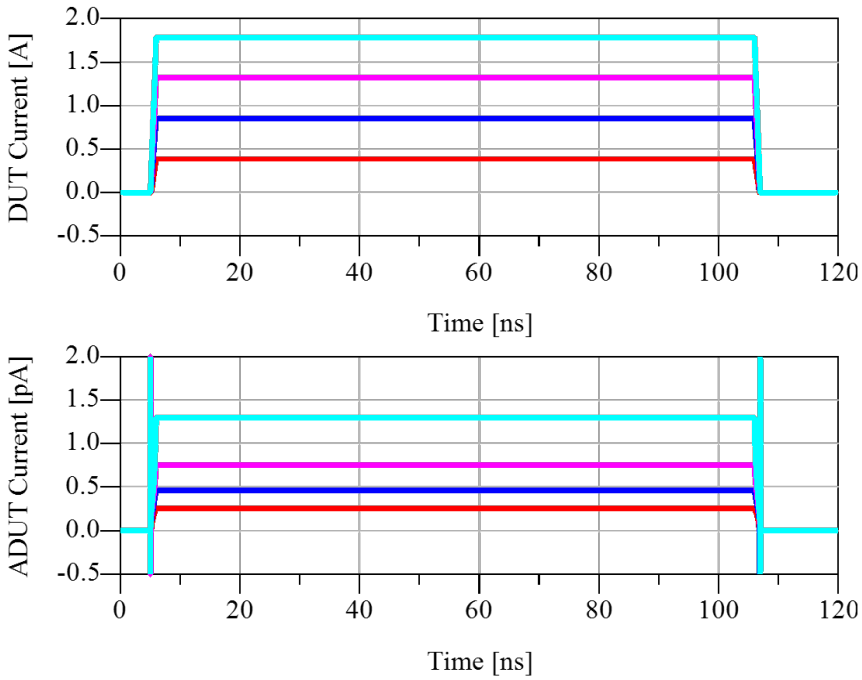


Figure 2.5. Ideally simulated DUT and ADUT currents for 5 levels of injection

3. CIRCUIT IMPLEMENTATION

The circuit was implemented on the microstrip test PCB, shown in Figure 3.1. This test board was used to evaluate independent DUT and ADUT loads. Once evaluated in a test environment, the circuit was implemented inside of a real test system and used to inject TLP-like stress pulses into an application processor (AP) on the receiving end of a functioning high speed MIPI camera interface.

3.1. TEST PCB

The test PCB consists of bottom-layer copper fill and top-layer microstrip with a characteristic impedance of approximately 50 Ω with SMA connectors on both sides. The microstrip was cut in the center of the PCB to allow the insertion of the toroidal transformer and the compensation circuit was formed by a TVS diode placed close to the VGND node, an optional series inductance, and a variable resistor for simple tuning. The schematic for this PCB is shown in Figure 3.2.

3.1.1. Test PCB Simulation. Instead of assuming that an ideal transformer model is representative of the hand-wound toroidal transformer used on the test PCB, it is implemented as two coupled inductors in simulation. This representation is still a first order model due to the roll-off of the core permeability with frequency but matches the measurement results well, revealing an important issue which impacts the circuit performance.

Based on the core geometry, the frequency independent inductance of the windings was calculated with Eqn. 3.1 and compared to low frequency measurements. The leakage inductance was measured by performing a shorted-secondary measurement and then this value was used to calculate the coupling coefficient K with Eqn. 3.2.

Table 3.1. Transformer Parameters for Test PCB

Property	**Value**	**Method**
L_1	131 µH	Calculated
L_1	2.6 µH	Calculated
L_{leak}	1.03 µH	Measured
K	0.96	Calculated

$$L_{coil} \approx \frac{\mu_0 \mu_r N^2 A}{2\pi r} \tag{3.1}$$

$$k = \sqrt{1 - \frac{L_{leak}}{L_1}} \tag{3.2}$$

Using the values in Table 3.1, the transformer was implemented in the simulation by $Mutual1$, $L6$ and $L7$ creating an equivalent leakage inductance. Although this leakage inductance is usually referred to the primary winding of the transformer, in this case it is helpful to reflect it across to the secondary winding. On the secondary side, it can be lumped into an approximation of the trace inductance ($L10$) which connects the injection circuit to the DUT. This procedure is not shown in Figure 3.2 because the coupled inductor model accounts for the leakage inductance. If the transformer were instead represented by three lumped inductor components as well as a coupling coefficient of unity, this would be visible. By placing an inductor ($L8$) into the compensation path, we can account for this equivalent load and leakage inductance. The required value is calculated using the same procedure which was used to calculate the compensation path resistance and diode breakdown voltage Eqn. 3.3.

$$L_{comp} = a * (L_{leak,secondary} + L_{trace}) \tag{3.3}$$

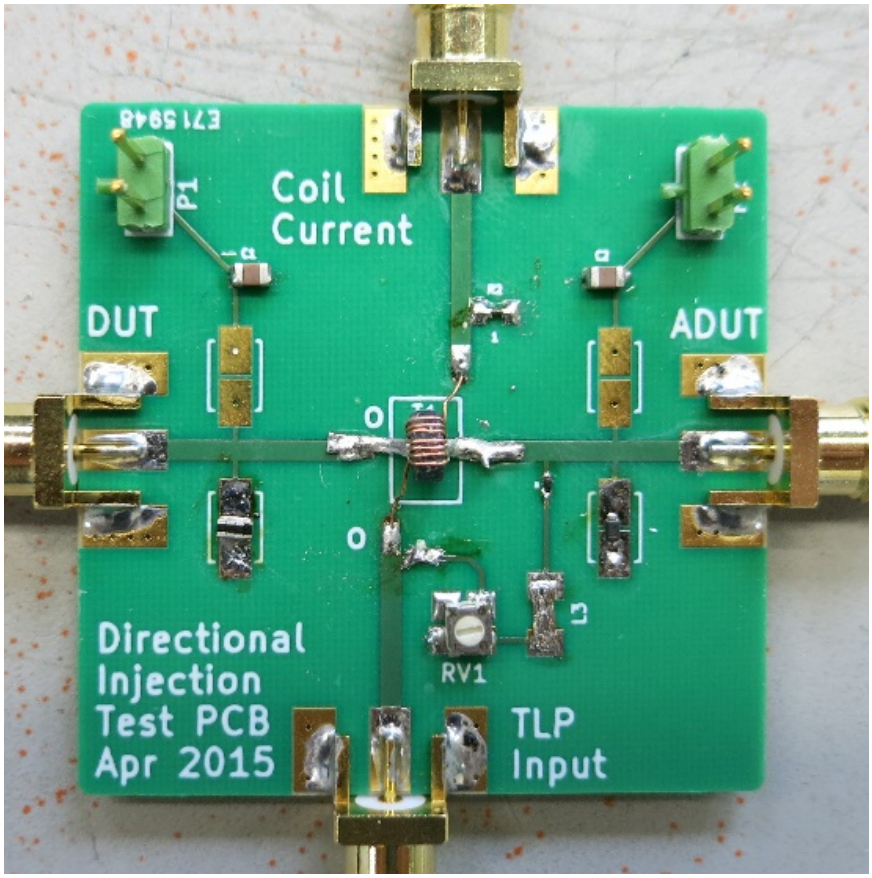


Figure 3.1. Populated Test PCB

Finally, the compensation path coupling diode is represented by $D3$, $D4$, and $C1$ based on both measured IV characteristic as well as the datasheet value of the off-state junction capacitance of the part.

Figure 3.3 shows the transient voltage and current waveforms over a range of pulse amplitudes as measured by the simulation environment. From these current and voltage waveforms it can easily be seen that the disturbance created at the ADUT node is minimal compared to the desired pulse injection. In these figures, trace colors represent pulse level and trace markers indicate either DUT or ADUT measurements.

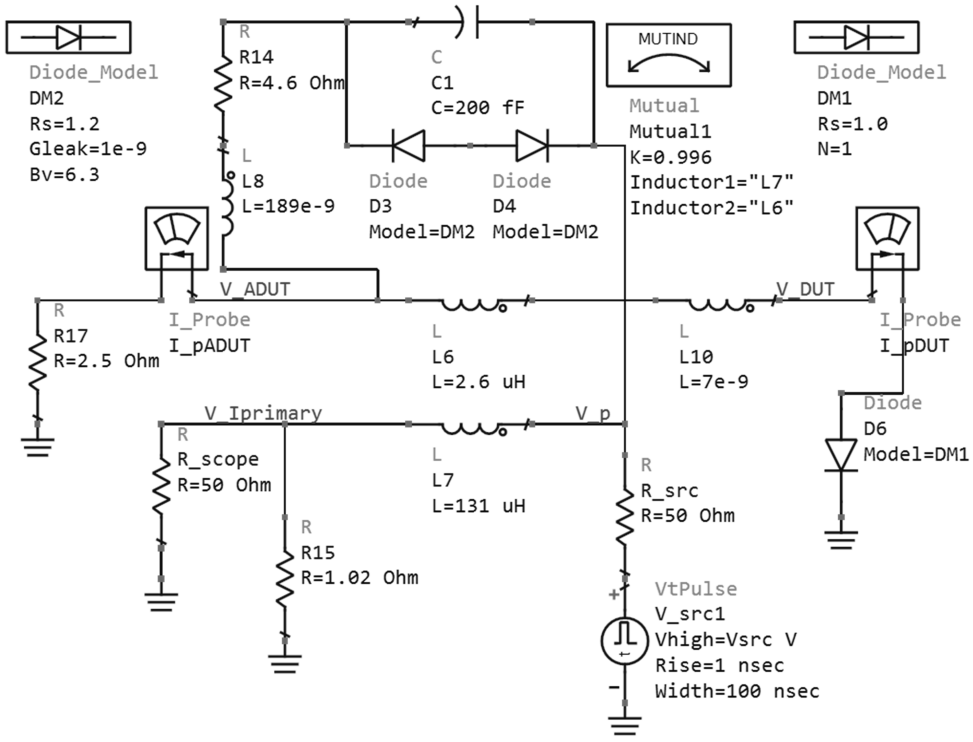
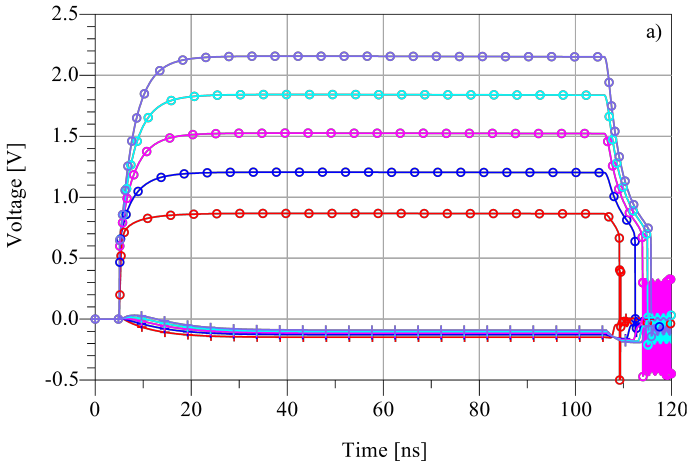
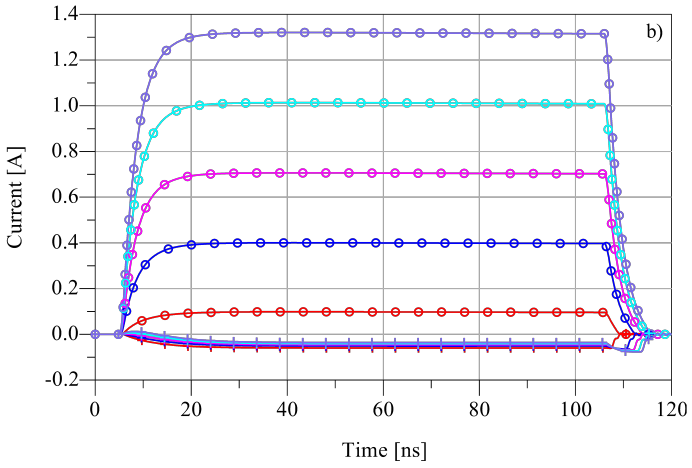


Figure 3.2. Test PCB equivalent circuit

By implementing the non-invasive current measurement point ($R15$) for the primary winding current in simulation, the performance of this measurement point can be evaluated against an ideal in-simulator current measurement. Figure 3.4 shows the error in the operation of this primary winding current measurement due to the non-ideal ($K < 1$) coupling between $L7$ and $L6$. Using the in-simulation current probe I_{pDUT}, the currents are compared to the measurement point $V_{Iprimary}$ and their absolute difference and percent error are plotted. It may be possible to improve this measurement by de-embedding an equivalent magnetizing inductance of the transformer but this is not explored here.



(a)



(b)

Figure 3.3. Test PCB simulated DUT ('o' marker) and ADUT ('+' marker) a) voltages and b) currents for five different injection levels

3.1.2. Test PCB Measurement. Actual measurements were performed using a diode and a 1 ohm resistor as loads. DCI was used to measure the diode as the DUT while the resistor played the role of ADUT. The results of the measurements are shown in Figure 3.5a along with the independently measured IV curves of the diode and resistor as well as the overall net behavior caused by the parallel loads.

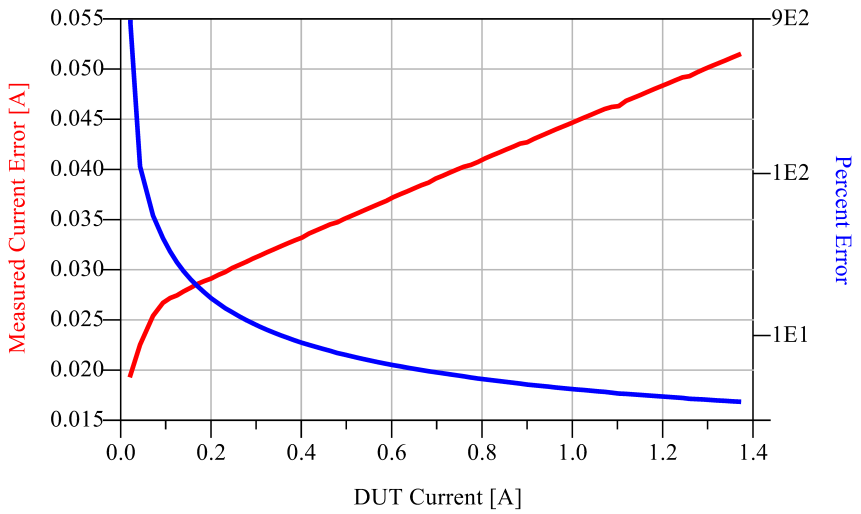
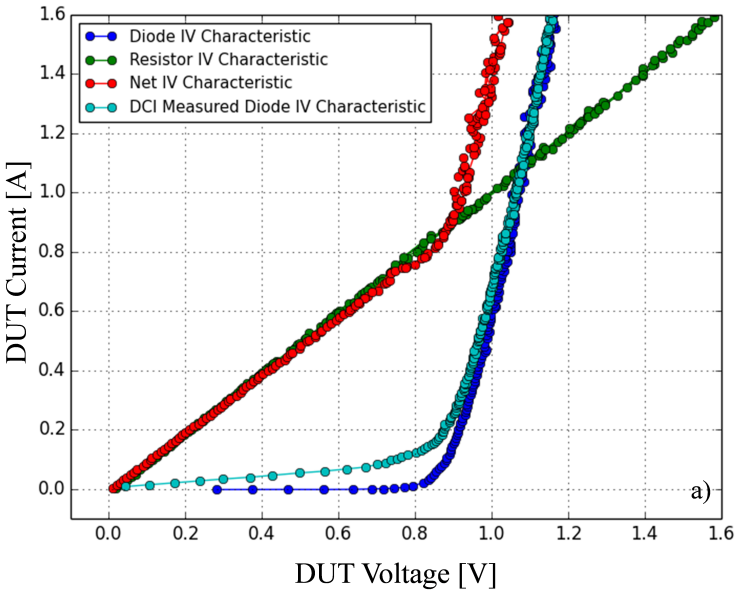


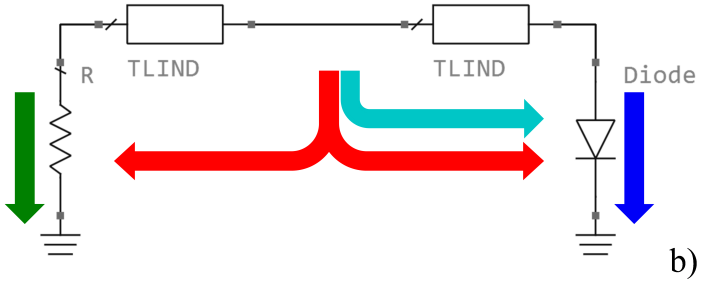
Figure 3.4. Test PCB simulated current measurement error through sense resistor

In the overall net measurement, the small resistor dominates, shunting current away from the diode until the voltage becomes large enough to switch the diode, creating a current divider. In the case when the directed injection is applied, the IV characteristics of the diode can be extracted without influence from the resistor. Here, the error in current measurement (Figure 3.4) is seen in the low-current offset in the DCI measurement.

The quality of the virtual ground is evaluated by plotting the VGND voltage with the DUT current. Figure 3.6 shows this VGND quality alongside the DCI measurement. In the ideal case of a perfectly tuned compensation circuit, the virtual ground would have zero resistance and no voltage offset. Here, the VGND has a resistance of approximately 250 mΩ with a small negative offset voltage due to a mismatch between the compensation path and DUT voltage relationship of Eqn. 2.4. Given that the ADUT is known to be a 1 Ω resistance, the current injected into the ADUT can be read directly from the voltage axis. In this case due to the very small ADUT resistance, the voltage offset in the VGND characteristic causes some large currents to be drawn from the ADUT for low DUT currents.



(a)



(b)

Figure 3.5. a) IV curve behavior with various measurement configurations; b) Color coded description of IV measurements

However, in the more realistic case where the ADUT is a diode to VSS such as commonly found in on-chip ESD protection, this VGND would be stable enough to prevent such a protection from triggering.

To test the feasibility of implementing the circuit in fast interfaces, the insertion loss of the circuit is shown in Figure 3.7. From this we see that the insertion loss of the

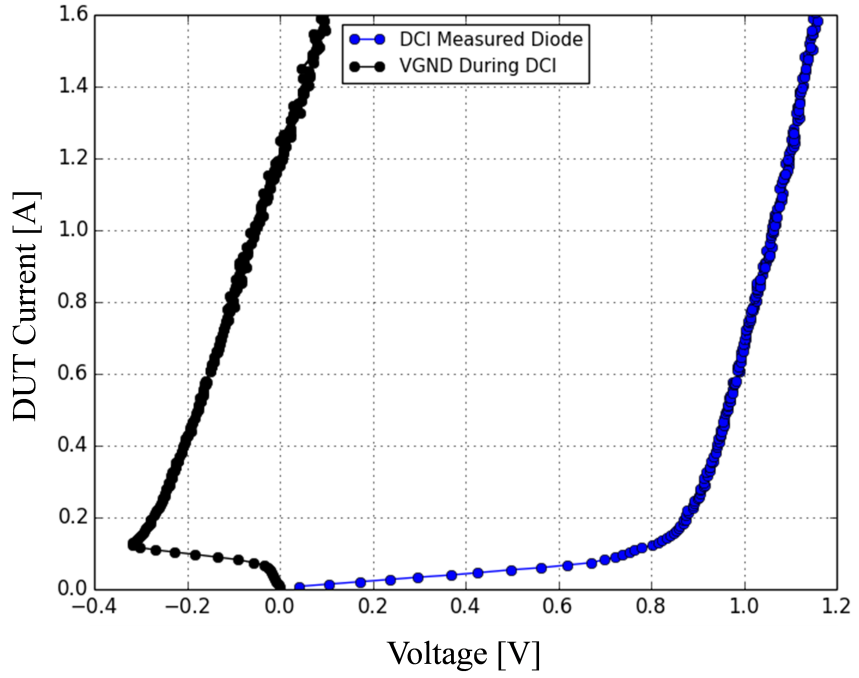


Figure 3.6. Virtual ground performance during directional measurements

DCI circuit is low enough to avoid interfering with the normal operation of medium to high speed interfaces such as USB 2.0, MIPI, and SDMMC.

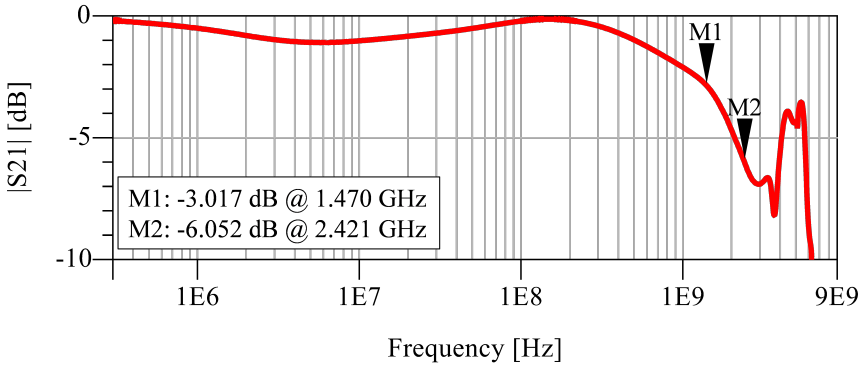


Figure 3.7. Directional injection circuit insertion loss

3.2. IMPLEMENTATION ON A REAL SYSTEM

The final test of the circuit was to implement it in a real system. This implementation took place on a set of fanout PCBs designed to break out several different interfaces on a system verification board (Figure 3.8). One such interface connects the secondary camera to the application processor (AP) through a high-speed MIPI bus clocked at approximately 333 MHz. In this implementation, a directional injection circuit was placed on each of the 4 MIPI nets such that stress pulses could be injected into the AP (receiver) and independent of the camera (driver).

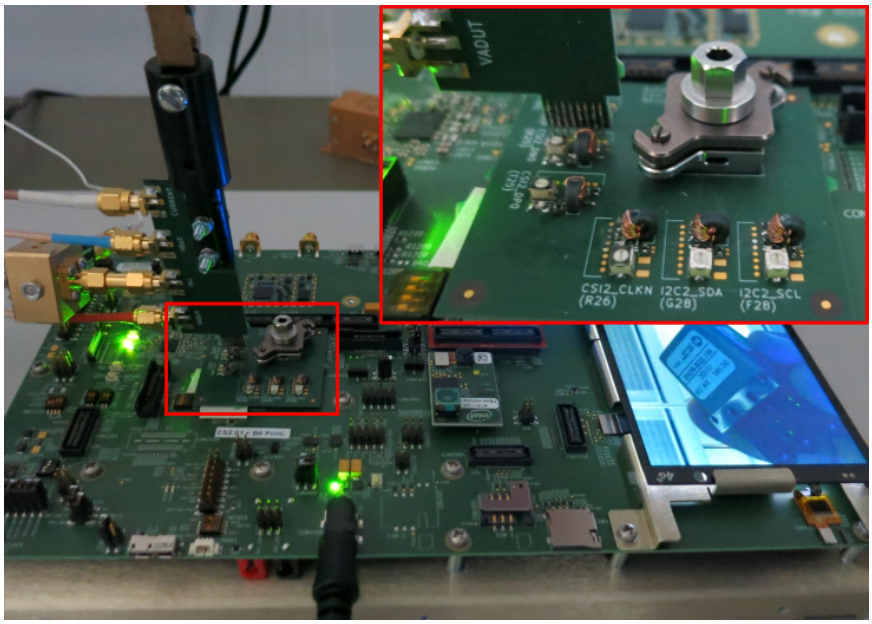


Figure 3.8. Fan out test board (camera) installed on functioning SVB

Continuing work from [5], the SVB was stressed and monitored for various failures during the operation. Two methods were used to detect failures. The first was a software event log which could be monitored during operation [6; 7] and the second was a human operator to keep track of user-observable errors such as image corruption or application

crashes that might go undetected by software alone. Inputs from the software log and operator were timestamped and combined with a pulse log from the TLP system to build a complete picture of the delivered pulse, software errors, and user experience during testing.

The occurrences of failures according to the software log and according to the operator were grouped into 50 mA intervals (bins), each with approximately 30 pulses due to a very small TLP charge voltage step. Taking the occurrence of a software-logged soft-failure and a user-observed soft failure both as binary variables, the sample mean is shown for each 50 mA bin along with an associated 90% confidence interval for the true failure probability. The estimated probabilities of logged and of observed failures for each bin is plotted alongside the AP pin IV curve as well as the VGND voltage to give a simple overview of the measurement. Two such overviews are shown in Figure 3.9 and Figure 3.10. In these tests, the applied pulses had a fast (1 - 5 ns) rise time and 75 and 50 ns pulse widths respectively. Subsequent tests for both shorter and longer pulses revealed that the observed soft failures have a strong dependence on the width of the applied pulse.

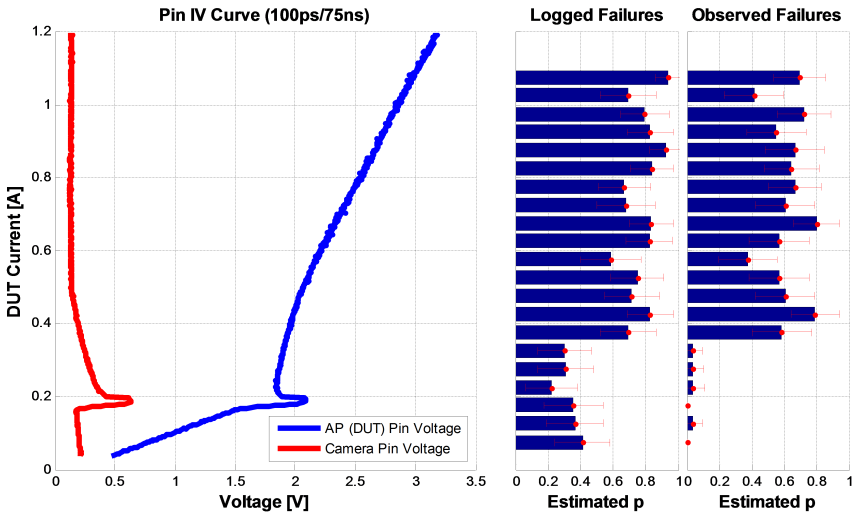


Figure 3.9. DUT (net:CSI2_CLKN) IV curve for fast 75 ns pulses with VGND performance and soft-failure analysis

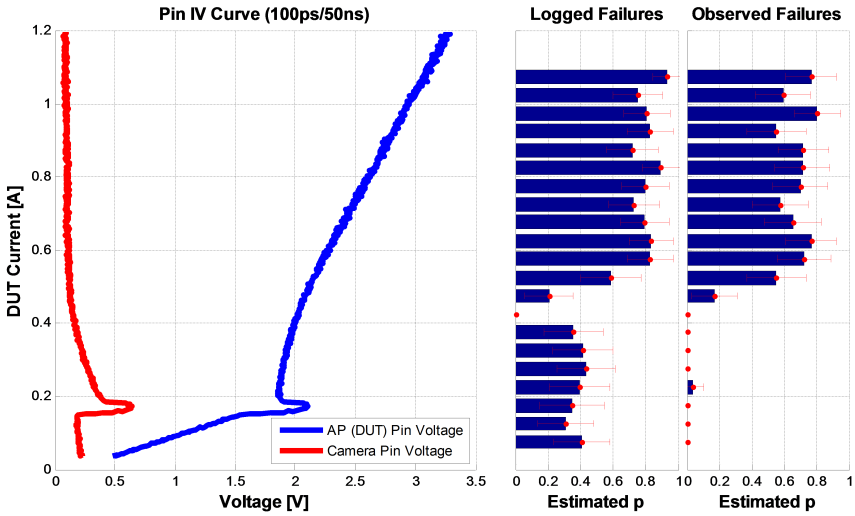


Figure 3.10. DUT (net:CSI2_CLKN) IV curve for fast 50 ns pulses with VGND performance and soft-failure analysis

It is important to note that because the clock signal contains a DC offset and a very small signaling level, the IV behavior of the signal itself will exhibit a similar offset. When analyzing the VGND performance in Figure 3.9 and Figure 3.10, the node is held steady by the compensation circuit and only the DC offset of the clock line can be seen on the camera pin side.

In addition to demonstrating the intended use-case of this circuit, these measurements also address the question about performance on snapback-based protection devices. Given that the compensation circuit was constructed with a TVS diode, there is some expected mismatch between the snapback behavior of the DUT and compensation behaviors which is clearly visible in the VGND quality curve. Even so, this mismatch causes at worst, a 0.63 V disturbance in the VGND behavior during the shallow snapback.

An example of the voltage transients during a 50 ns pulse as seen by the DUT and ADUT/VGND is shown in Figure 3.11. This transient waveform shows the system clock on both the ADUT and DUT side of the transformer superimposed on the applied

disturbance injected towards the DUT. The waveform also reveals a parasitic capacitive coupling between the pulse injection, DUT, and ADUT sides of the transformer indicated by the distortion on the ADUT voltage during the rising and falling edges of the interference pulse. This parasitic can contribute to diminished directivity during shorter pulse. It could possibly be reduced by circuit layout and transformer winding optimization.

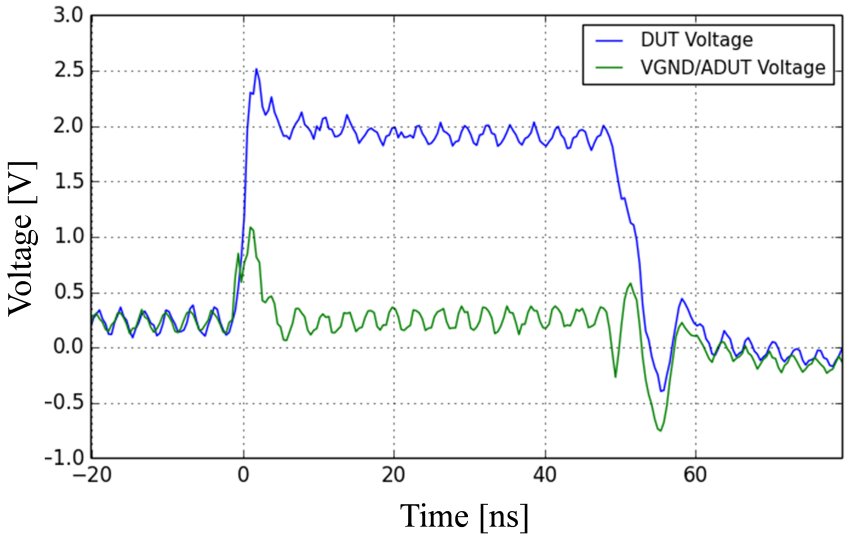


Figure 3.11. DUT and ADUT transient waveforms

4. CONCLUSION

A new TLP injection method has been developed which allows interference pulses injected into an operating signal line to be directed towards one end of the line. This allows for the in situ characterization of the soft fail robustness of a system under ESD as well as the ability to measure the IV characteristic of a functioning IO which could not otherwise be measured. The method shows good electrical transparency in the GHz range, indicating that it can be used in both low and high speed systems. This is demonstrated in the analysis of a camera interface of a system verification board.

Determining the pin-specific level of soft failure susceptibility on a system verification board in the early state of platform development provides a data set which can be used later during form factor board design, allowing designers to focus on weak pins. In a more advanced design methodology a full simulation-based design might be enabled which combines pin sensitivity models with simulation of induced ESD stress at the net under investigation.

5. ACKNOWLEDGEMENTS

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IV. CHARACTERIZATION OF AN APPLICATION PROCESSOR WITH RESPECT TO ESD-INDUCED SOFT FAILURES

Benjamin Orr, Sebastian Koch, Harald Gossner, and David Pommerenke

ABSTRACT

In this paper, we present a methodology to characterize a logic IC such as an application processor with respect to soft-failure susceptibility due to electrostatic discharge. By testing the IC while in a functional system, real-world use cases are realized while the IC itself is exposed to direct electrical interference. This test methodology enables the extraction of the IC behavior during stress on a pin-by-pin basis. It is possible to perform this characterization in the validation stages of component development, making it possible to provide system developers with valuable information about potential modes of failure. This early detection of potential soft errors and their sensitivities can therefore be used to design for soft-failure robustness from the very beginning of system hardware and software design.

1. INTRODUCTION

In recent years there has been interest in a more systematic approach to ESD-aware design. Rather than an iterative process in which failures due to ESD are addressed in the order that they are observed, a more advanced process known as System Efficient ESD Design (SEED) has been proposed [1]. While SEED has, for the most part, been applied to address hard failures, it has also been proposed that the method be employed to address soft failures. The core operational principle of SEED is that both the pin electrical behavior and failure limits be known. While the electrical behavior of a pin remains the same across hard- and soft-failure analysis, the extraction of soft-failure levels is a significantly more difficult task. In this paper we attempt to provide some insight into the pin-by-pin behavior of an IC with respect to soft-failures. In some cases, these behaviors can be precisely determined as thresholds to be addressed by SEED and in other cases, information about the types of error mechanisms can be used to bypass the SEED simulation flow entirely and correct the error in software.

By definition, a soft-failure is a system failure which is not due to physical damage and which can be corrected by, at most, power cycling the system to return it to a known-good state. Such failures can be due to incorrectly interpret signals which result in an error condition, or by an electrical stress which propagates through the system and alters the position of a state machine, flipping bits, or otherwise changing the system state. Arising from modern system complexity, soft-failures can be influenced by a myriad of overall system conditions. Examples of these conditions include but are not limited to, specific software or firmware [2], the shape of the applied pulse [3], and instantaneous power supply voltage [4]. Furthermore, because soft-failures can be dependent on rapidly changing

system variables such as specific register values or clock state (high, low, and transition), these failures can be likened to statistical events with only a probability of occurring during any given system and interference condition [5].

To address at least some of these issues, this work builds on the "divide and conquer" approach first presented in [3] with the addition of the directional injection technique from [6]. By exposing IO pins on the DUT IC to a variety of pulse shapes during various software conditions, certain failure signatures can be triggered, recorded, and associated for specific conditions. While not all relevant conditions are able to be set and measured, several pulse shapes and software conditions are tested repeatedly in an attempt to extract the probabilities of occurrence for different failure signatures during device operation.

Based on such a characterization, data on the pin-by-pin failure susceptibilities of an IC can be made available to system designers. Where applicable, such data can be integrated into pin SEED models to be used to detect potential soft failures at the simulation level. When such models are not realistic, the observed failures can potentially be addressed directly in software through defensive programming techniques [7].

2. TEST METHODOLOGY

2.1. PRELIMINARY

In order to characterize a DUT IC with respect to soft failures, the IC is first divided into subsystems. This partitioning scheme is leveraged to easily address groups of pins which may manifest similar failures rather than each pin individually. It also provides a convenient opportunity to narrow the selection of pins to test. By focusing characterization efforts on only pin groups which are likely to see interference (external pins) and ignoring those which likely do not (internal pins). In this way, the characterization of large scale devices with hundreds of pins becomes a tractable problem.

Once the interfaces have been selected, the minimum levels of functionality are listed for each case. Because soft-failures cover a wide variety of failure mechanisms it is important determine what constitutes a failure on an interface-by-interface basis. Furthermore, not all observed errors are of a critical nature and can thus be deemed acceptable levels of failure. These decisions about levels of failure should be made based on the intended use case and reliability requirements of the DUT. For example, a consumer device which may experience brief periods of lock-up as the system corrects itself may be acceptable while a similar failure in an aviation or medical device may be unacceptable. By identifying these acceptable levels of failure on a device-by-device basis, soft failures can be more easily categorized and addressed.

2.2. INJECTION AND CHARACTERIZATION SETTINGS

Because the DUT IC is required to be in a functional state, an early system prototype which is centered on the IC is used to approximate a real system (Figure 2.1). The exact system used to test a given DUT may vary based on its intended application.

Figure 2.1. An example system centered on the DUT which is suitable for testing.

Electrical interference is injected by a transmission line pulser system [8]. This method is used because of the well-defined source impedance, shape, and pulse repeatability. The pulse shape is generally trapezoidal with adjustable rise times, pulse widths, amplitudes, and polarities. Bipolar pulses are also generated which are based on the TLP source. A complete list of electrical test variables is found in Table 2.1.

Because soft-failures may depend on variables other than those that are accessible to testing environment, failures are treated as statistical events. For this reason it is advantageous to perform a large number of repeated tests at the same amplitude to establish a threshold. In this method, in lieu of performing repeated tests at the same amplitude,

the increment between each test is chosen to be very small. In this way, each pulse is not significantly different from its immediate predecessors, thereby generating a very large number of similar tests.

Table 2.1. Swept Electrical Parameters

Parameter	**Value Range**	**Units**
Amplitude	[1,0]	A
Polarity	Positive, Negative, Bipolar	None
Width	2.5, 5, 10, 50, 100	ns
Rise Time	0.1, 1, 25, 50	ns

Because the individual IC pins are in functional states during testing, it is necessary that they be connected to one or more other devices. When injecting interference pulses, it is desirable to direct the current pulse into the DUT IC without disturbing the connected device. In this way, the DUT can be characterized independently from other components in the system. To perform this directed current injection (DCI), the circuit developed in [6] is implemented multiple times, once immediately adjacent to each of the selected pins. This injection system allows observed failures to be attributed to the DUT IC interface and not the connected components.

Besides the injected interference, the second aspect of soft-failure characterization is the system state. In order to test for errors that may occur in an end user environment, this environment is emulated as closely as possible during characterization. Depending on the interfaces being tested, different end-user applications are run on the system such as file I/O, data acquisition, video streaming, or simple background calculations. Furthermore, the data transmitted across a bus can be varied, forcing things like dynamic encoding schemes of video transmissions to be stressed. This approach is not unlike software unit testing where various system calls and applications are carried out in simultaneously in search of potential incompatibilities. Table 2.2 shows several options for the software loads. Together with

Table 2.1, these parameters make up the "measurement space" of interference and settings which the system is exposed to during testing.

Table 2.2. Swept Software Parameters

Parameter	**Value Range**	**Units**
Priamry Interface Active	Yes, No	None
Average # of Threads/min	[2, 6]	none
Dynamic Data	Yes, No	None

2.3. FAILURE DETECTION

Based on the previously defined minimum levels of functionality, preliminary interface tests are performed to identify potential errors. These tests are taken in an uncontrolled manner to simply observe the different recorded failure symptoms. These preliminary observations are used to familiarize the operator with some typical failure modes of the device. Such observations may also be useful in the future to automate testing.

Considering the classification system in [3] (Table 2.3), it becomes evident that certain failures may be difficult to observe. In this method a two pronged approach is used to detect errors by directly monitoring the system user experience during testing as well as recording event logs from the DUT system software. By combining input from both of these sources, a more complete picture of the failures can be observed. Furthermore, by comparing both failure inputs, relationships between observed failure signatures and software-detectable failures can be constructed. Such relationships can then be used as an attack vector to better understand the failure mechanism or to correct the failure outright in software.

Treating the user experience and software logs as responses from the DUT, additional information is added in the form of stimulus type. Information from the TLP system which

Table 2.3. Soft Failure Categorization

Level 1:	Undetected error, the system recovers without operator intervention
Level 2:	Brief but noticeable change in functionality, the system recovers without operator intervention
Level 3:	Change of functionality, the system requires operator intervention to correct
Level 4:	A latent error is introduced into the system that affects an operation not yet performed, the system requires operator intervention to correct

is used to inject interference is combined with the DUT responses in a monolithic test log file to record both the stimulus and subsequent response. A diagram of the inputs is shown in Figure 2.2, and a color-coded excerpt of a log file is shown in Figure 2.3 where the first field is the test-specific timestamp, the second field is the event type: &P (pulse) &L (log line), or &F (failure). If a pulse is indicated, the next two fields identify the pulse number in the sequence and TLP charge voltage. If a log line is indicated, the system log follows. If a failure is indicated, the code follows indicating the failure level and unique identifier (Level 2, code 0001 in this example).

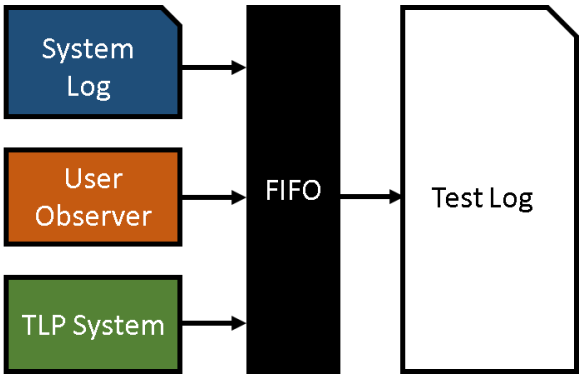

Figure 2.2. Test log creation

```
0217.044 &P #254 @29.5
0217.844 &P #255 @29.6
0217.924 &L [ 6404.950564] CIF ISP2.0 marvin_mipi_isr(5605)
   ERR: CIF_MIPI_ERR_CSI 100000
0217.934 &L [ 6404.964022] cif_isp20 eb000000.cif:
   CIF_ISP_PIC_SIZE_ERROR (0x00000001)
0218.514 &F L2.0001
0218.584 &P #256 @29.7
0218.614 &L [ 6405.682232] CIF ISP2.0 marvin_mipi_isr(5605)
   ERR: CIF_MIPI_ERR_CSI 100000
0218.664 &L [ 6405.689264] cif_isp20 eb000000.cif:
   CIF_ISP_PIC_SIZE_ERROR (0x00000001)
0218.674 &L [ 6405.698182] Measurement late
0219.474 &P #257 @29.8
```

Figure 2.3. A log file excerpt

2.4. DATA ANALYSIS

To visualize the failure profile of each pin, the log files are processed to estimate the probability of a given failure as a function of pin current. Leveraging the large number of pulses generated by the small TLP voltage step, the individual pulses are grouped into discrete current intervals or bins. By comparing the number of errors in each bin to the number of tests in the bin, the estimated failure probability on a type-by-type basis can be calculated along with an associated confidence interval for each bin. These values are plotted alongside the pin IV curve and directional injection virtual ground (VGND) stability curve. Because the current delivered during each pulse is a function of both the TLP source impedance as well as the apparent DUT impedance, the number of tests in each bin can vary. An example is shown in Figure 2.4.

It is important to note that the IV and VGND curves in the preceding figure are taken while the interface is active. Given that the pin under test (PUT) can swing between 0 and 1.8 V, the low current (< 0.2 A) behavior unsurprisingly shows evidence of the pin driver

fighting against the TLP. However, once the ESD protection turns on at about 200 mA, the curve becomes smooth. It is also worth noting that the current measurement system is subject to error in the low-current regime as noted in [6], which leads to an artificially low-resistance behavior prior to the turn-on of ESD protection elements.

Failure probability curves are shown vertically as functions of the DUT current. In this way, changes in failure probability can be easily compared to the IV curve behavior such as current level or shape (Do failures tend to correspond with corners in the IV curve? Do failures happen only at specific current levels? Etc.). Relationships between the pulse current and failure types can also be shown by examining measurements taken under different conditions.

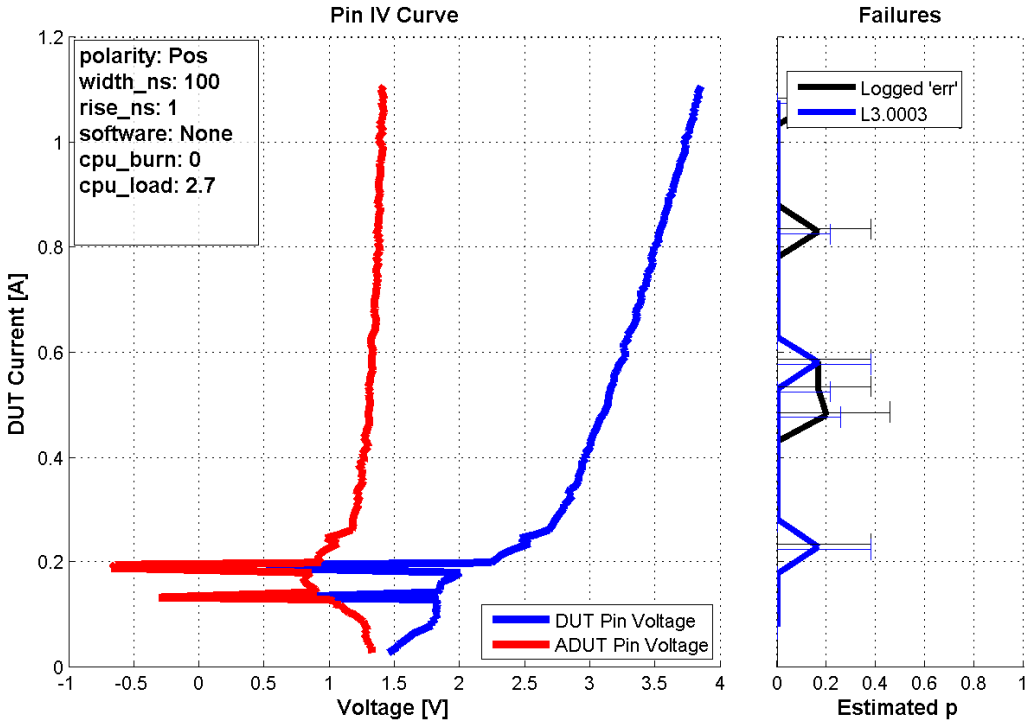

Figure 2.4. A set of both system-logged and user-observed failure probabilities and confidence intervals as a function of pin current plotted next to the pin IV and virtual ground stability curve.

3. CHARACTERIZATION EXAMPLES

Because soft-failures can be diverse and triggered by very specific sets of stimuli, the exact implementation of this characterization methodology can look quite different from one DUT to the next. To illustrate this variability, select results from three example interfaces of a mobile device application processor are presented below. These interfaces were chosen to cover several different use-cases spanning full- and half-duplex, low- and high-speed, inter- and intra-device communication, and single or daisy chained devices. Because of the sheer number of tests taken on each pin, not all results are able to be presented here.

3.1. CAMERA INTERFACE

The camera interface is a single lane Mobile Industry Processor Interface (MIPI) bus made up of a unidirectional differential clock and differential data pair. Tests were performed on one of each, the clock and data pins during different stress conditions. Preliminary tests revealed several failures on the clock pin while the camera software (and consequently the MIPI interface) was powered and transmitting data from the camera (Tx) to the application processor (Rx). These failures are listed in Table 3.1. By far the most common failures during testing are one of two distinct visual glitches (one grey, one purple) which are observed both on the screen and in captured video. In this section, only the results concerning the purple glitch (L2.0001) is shown. An overview of all observed failure sensitivities is shown in Table 3.2.

Focusing on the most significant failure signature, Figure 3.1 - Figure 3.3 show the results of three different measurements. Reading from the right hand side of the CSI2_CLKP measurements, it is seen that the estimated L2.0001 failure probability undergoes a step

Table 3.1. Commonly Observed Soft-Failures During Camera Testing

Failure Code	Description
L2.0001	Purple glitch across video (common)
L2.0002	Grey glitch across video (common)
L2.0004	Dark or bright glitch on bottom or whole screen (common)
L3.0001	"Can't connect to the camera" dialog box - Requires a restart of the camera application (extremely rare)

Table 3.2. Camera Interface Failure Sensitivities

Failure Code	Description
Polarity	Negative and positive behaviors are similar. No notable bipolar behavior.
Width	Both polarities exhibit both charge ($width * amplitude$) and width based failures.
Rise Time	No rise time dependencies observed from 100 ps to 50 ns.
Active Interface	When the camera is not in use, no failures are observed.
Average # of Threads/min	No dependency is observed for an average of 2-6 active threads/min.
Dynamic Data	Increasing activity on the interface by showing a dynamic image has no effect.

change from 0 to approximately 0.8 at increasing pulse amplitudes as the pulse width decreases. This inverse width/amplitude relationship indicates that the failure may be caused by the total charge injected into the pin.

The logged failures appear to also be affected by the charge threshold although in a different manner. Injecting even small currents into the pin appears to have a 40% probability of introducing a logged failure until such amplitudes as the previously mentioned charge threshold is reached. For reasons unknown, the estimated logged failure probabilities trend towards 0% before rising to track the L2.0001 failure curve. It is not clear why this null occurs, but examples of the failures both before and after the threshold are shown in Figure 3.4.

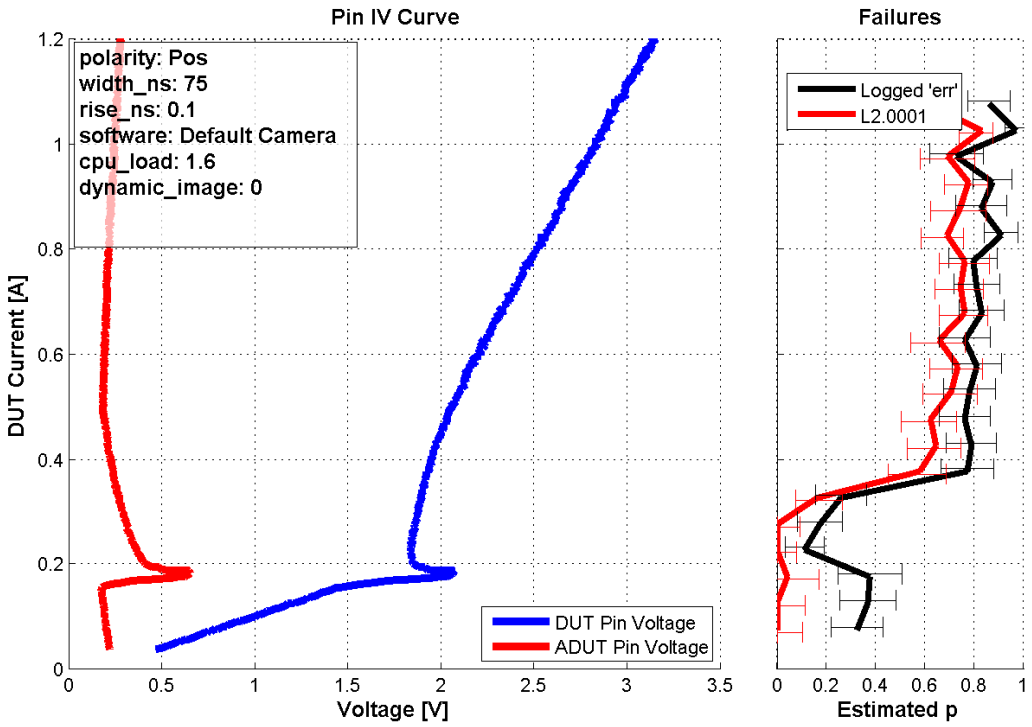

Figure 3.1. CSI2_DP0 - 75 ns pulse width

Figure 9 shows the results of a 25 ns pulse-width test on a data pin (CSI2_DP0). In the data pin case there are three logic levels: low, high, and idle (only low and high are present on the clock pin). Typical transmission (low and high) occurs between 0 and 50 mV while the idle state is 1 V. This idle state in the low-current (< 150 mA) behavior of the IV curve of the data pin as a region of voltage instability which is shown in Fig. 9. No attempt is made to correlate failure probabilities with the pin state (transmitting vs idle). Rather, any such dependence is reflected in the aggregate behavior of the interface and failure probabilities.

Comparing Figure 3.3 and Figure 3.5, the failure probability curve on the data pin does not indicate a similar width-dependence. Rather, the failure itself seems to stem from

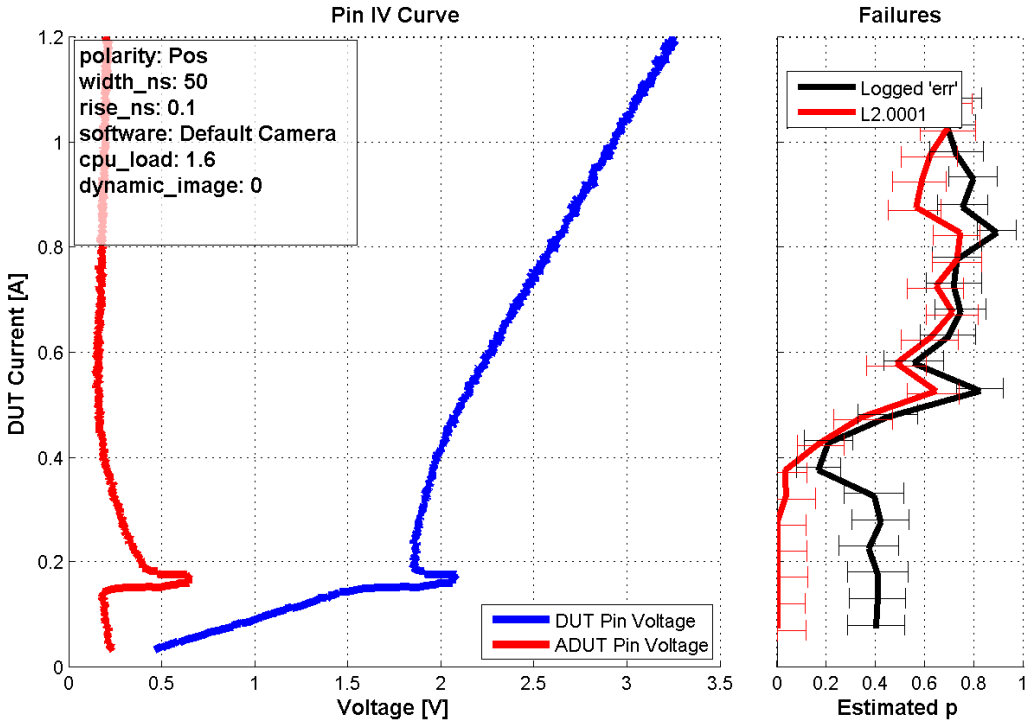

Figure 3.2. CSI2_DP0 - 50 ns pulse width

either the activation of the ESD protection circuits on chip or simply data corruption due to the interrupting pulse. Because this interface is designed for chip-to-chip communication it is likely that little is done to perform data verification during transmission.

The takeaway from these measurements is that although both pins exhibit very similar conditions, the low failure threshold of the data pins combined with the fact that the error itself is determined to be of low importance suggests that it may not be worth the effort to protect this interface. Additional visual errors such as L2.0002 and L2.0004 are also deemed noncritical and not worth addressing. Error, L3.0001, was observed only several times across the thousands of pulses delivered during characterization tests, and was therefore also deemed negligible due to infrequency of occurrence.

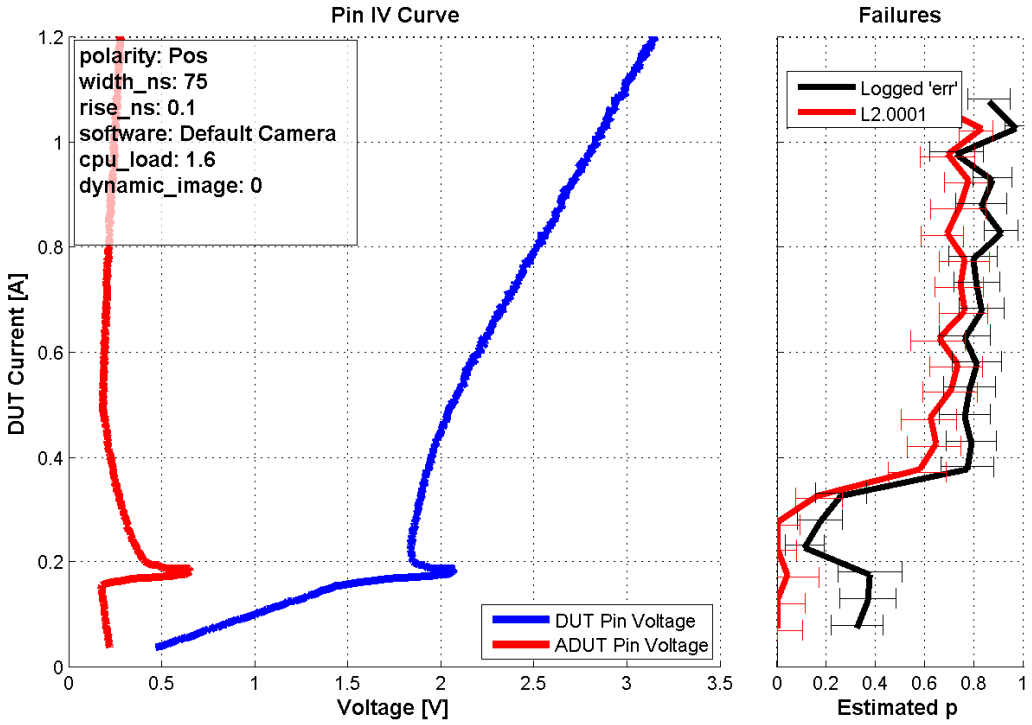

Figure 3.3. CSI2_DP0 - 25 ns pulse width

```
0011.298 &P #13 @3.3
0011.328 &L [ 7808.215946] CIF ISP2.0 marvin_mipi_isr(5605)
       ERR: CIF_MIPI_ERR_CSI 800000
                            •
                            •
                            •
0156.596 &P #272 @31.2
0156.636 &L [ 7952.260562] CIF ISP2.0 marvin_mipi_isr(5605)
       ERR: CIF_MIPI_ERR_CSI 100000
0156.689 &L [ 7952.270553] cif_isp20 eb000000.cif:
       CIF_ISP_PIC_SIZE_ERROR (0x00000001)
0157.137 &F L2.0001
```

Figure 3.4. Two log file entries from before and after the charge-dependent threshold on a CSI2_CLK pin

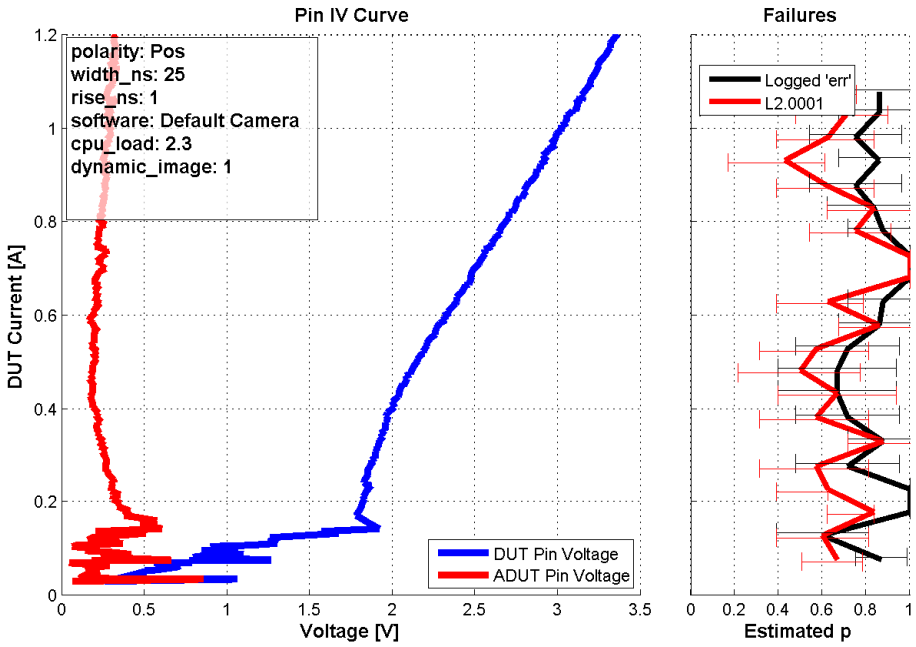

Figure 3.5. CSI2_DP0 - 25 ns pulse width

3.2. I^{2}C INTERFACE

A collection of sensors (Tx/Rx) are daisy chained to the application processor (Rx/Tx) through an Inter IC Communication (I^{2}C) interface. This sensor chain includes a magnetometer, gyroscope, and accelerometer. Tests were performed by directly observing the numeric sensor outputs through an end user application. The commonly observed failures are listed in Table 3.3 while an overview of the measurements are listed in Table 3.4. The primary modes of failure observed were a brief pause in the application, and an interface hang requiring a system restart (L3.0002 and L3.0003).

Unlike the camera interface, the sensor system showed minimal dependence on any of the swept parameters. Tests revealed that both pins (SCL and SDA) are relatively immune

Table 3.3. Commonly Observed Soft-Failures During Sensor Interface Testing

Failure Code	Description
L2.0003	I^2C pause / GPU reset
L2.0004	Dark or bright glitch on bottom or whole screen
L3.0002	System hang - Requires restart
L3.0003	I^2C bus hang - Requires restart

Table 3.4. Sensor Interface Failure Sensitivities

Failure Code	Description
Polarity	Negative and positive behaviors are similar. No notable bipolar behavior.
Width	No width dependency is observed from 2.5 ns to 100 ns.
Rise Time	No rise time dependencies observed from 100 ps to 50 ns.
Active Interface	When the sensors are not in use, no failures are observed.
Average # of Threads/min	No dependency is observed for an average of 2-6 active threads/min.

to narrow injections (< 10 ns) but began to fail for longer disturbances. No further test parameters were observed beyond this 10 ns minimum threshold. Unfortunately, although the failure signature is confined to a narrow class of injection, the most commonly observed errors require a system restart to correct. Several example tests which show this consistent low-probability behavior are shown in Figure 3.6 - Figure 3.6.

Even though the estimated failure probability is quite low for the L3.0002 and L3.0003 errors, the occurrence of such a severe issue on this interface should be considered critical. However, in lieu of recommending that corrective action be taken in hardware, a different approach is considered.

By examining the kernel log output at the time of the crash (Figure 3.9), a clear signature can be observed at the software level. This error indicates that the driver software which controls the I2C bus indicates that it is brought into multi-master arbitration mode.

However, since there are no other master-capable devices on the bus, the arbitration is never resolved and the bus is left in a nonoperational limbo leading to the L3.0003 error. In the case of the L3.0002 error, similar behavior is noticed in the log files. This error seems to stem from a stalled-process warning which goes unresolved. By examining both of these software-triggered error conditions it may be possible for software architects to address them directly with defensive programming techniques [7].

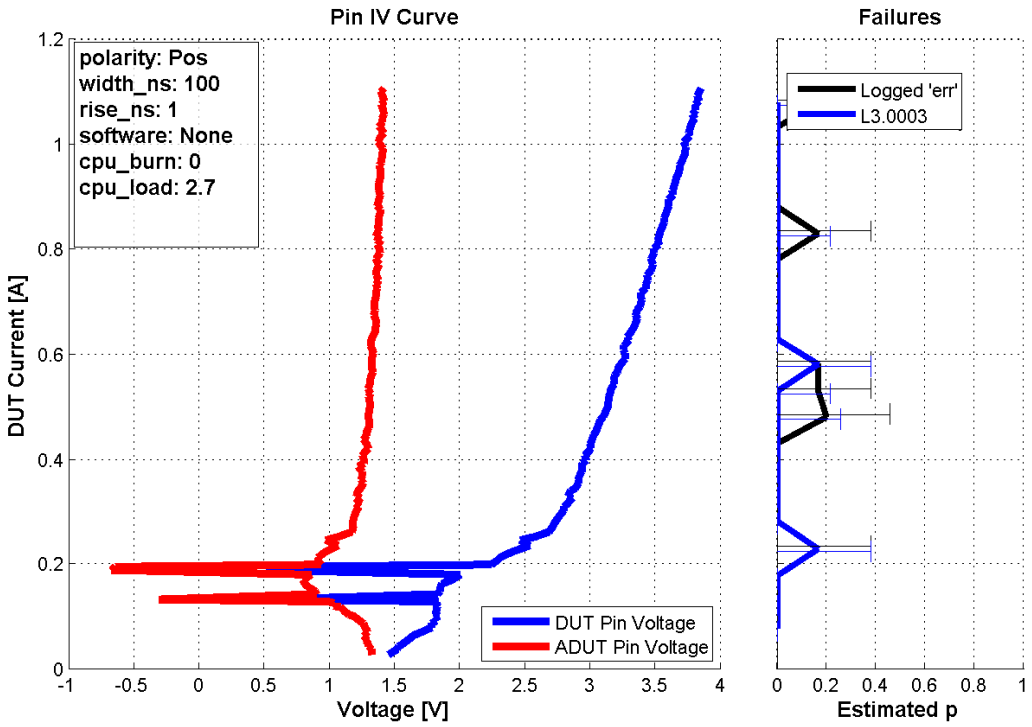

Figure 3.6. I2C5_SDA pin test

3.3. USB 3.0 INTERFACE

The USB 3.0 interface of the device provides intra-device high-speed connectivity between the DUT and a second device. Because this interface has no default connections,

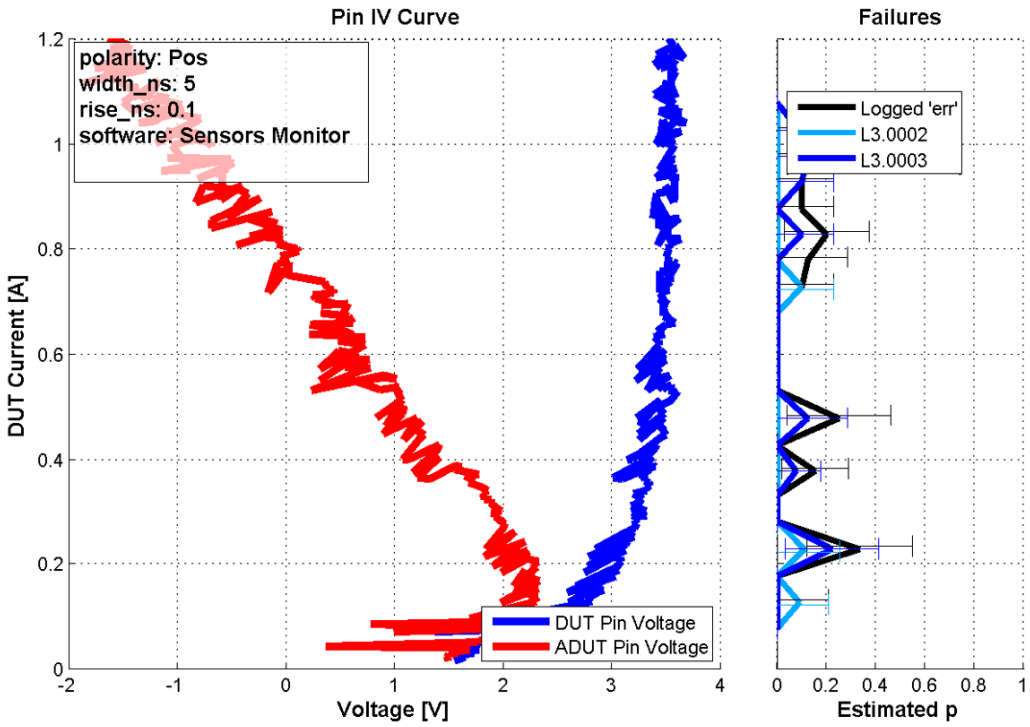

Figure 3.7. I2C5_SDA pin test

the DUT is attached to a host PC which initiates a file transfer over the Media Transfer Protocol (MTP) to activate the interface. The list of observed failures is shown in Table 3.5 and a summary of the test conditions in Table 3.6. Two critical failures were identified on this interface. The first is a bus disconnect, requiring re-enumeration and handshaking. The typical remedy for such interface disconnects is to re-mount the DUT via the host PC software or forcing re-enumeration by removing and reinserting the cable. The second critical error is a corrupted copy operation which is only revealed by a user-initiated checksum. Because this checksum is not normally performed during similar copy operations, this error is classified as a level 4 failure.

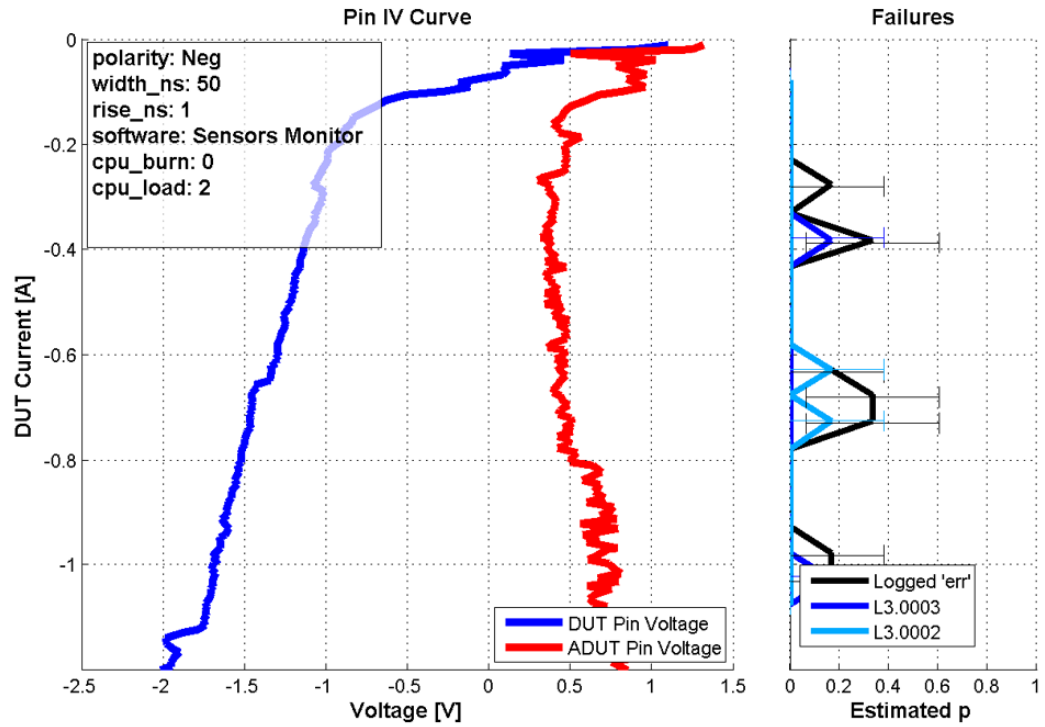

Figure 3.8. I2C5_SDA pin test

```
0255.263 &P #104 @60.1
0255.573 &L [  542.731357] I2C: M5: AL recvd.
0255.573 &L [  542.734344] msg l3gd20_gyr_i2c_read i2c read
   error: -13
0255.583 &L [  542.734541] I2C: M5: AL recvd.
0255.583 &L [  542.734601] msg lsm303dlhc_acc_i2c_read i2c read
   error: -13
0255.583 &L [  542.734611] I2C: BUSY
0255.593 &L [  542.734620] I2C: Driver state 0, Bus state 1.
0255.593 &L [  542.734628] msg lsm303dlhc_acc_i2c_read i2c read
   error: -16
0255.603 &L [  542.734636] I2C: BUSY
0255.653 &L [  542.734646] I2C: Driver state 0, Bus state 1.
```

Figure 3.9. Kernel-logged I^2C interface error indicating the multi-master arbitration mode

Table 3.5. Commonly Observed Soft-Failures During USB 3.0 Interface Testing

Failure Code	Description
L3.0004	Copy operation error - Requires re-enumeration
L4.0001	MD5 checksum failure - Requires that the file be recopied

Table 3.6. USB 3.0 Interface Failure Sensitivities

Failure Code	Description
Polarity	Errors occur almost exclusively during positive tests, bipolar tests occasionally trigger similar errors
Width	Positive interference may cause a charge ($width*amplitude$) based failures.
Rise Time	No rise time dependencies observed from 100 ps to 50 ns.
Average # of Threads/min	No dependency is observed for an average of 2-6 active threads/min.

In examining a pulse width sweep on an Rx pin (Figure 3.10 - Figure 3.12), there is some evidence that the width of the pulse is a factor in the occurrence of L3.0004. From the 100 and 50 ns cases, there is a clear decrease in the number of observed failures across the range of injected currents. Examining the 10 ns case, it is seen that the shape of the IV curve shifts drastically, and the first failures now occur at higher currents. No clear pattern is seen in L4.0001.

Comparing the widest of the positive pulse tests (Figure 3.10) to a similarly wide negative pulse test (Figure 3.13) which is found to be representative for the entire range of negative tests, the discrepancy between the positive and negative failure signatures is immediately apparent. No errors are observed in the negative direction.

The logged failures present an interesting case. Because the USB interface is "hot-pluggable", any disconnects observed by the DUT are not necessarily treated as errors. That is to say that the system software cannot distinguish between an intentional device disconnect and an ESD-induced disconnect error. The system software treats both as

typical disconnects and no corrective action is performed. This characteristic is evident in the plotted measurements where the reported errors are nearly exclusively of the observed type. Examining the infrequent logged failures which occurred in Figure 3.10 - Figure 3.13, the errors appears to be related to the device file system and were silently corrected.

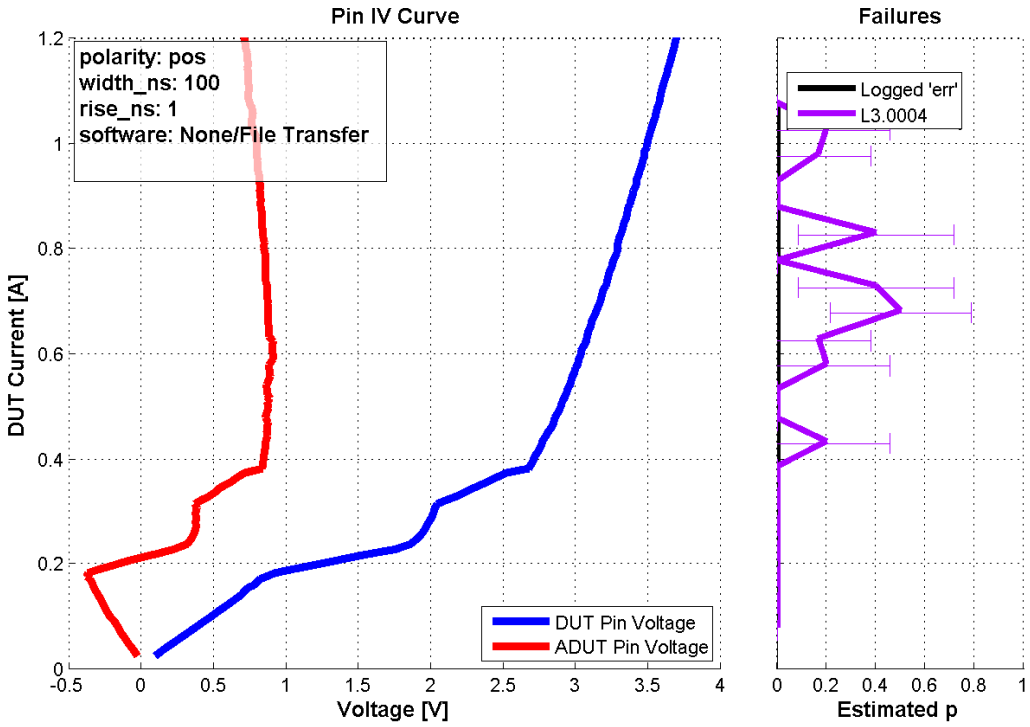

Figure 3.10. USB3_RxP - 100 ns pulse width

Based on the results measured here on the USB interface, it is concluded that any ESD protection strategies need only to focus on positive going stress.

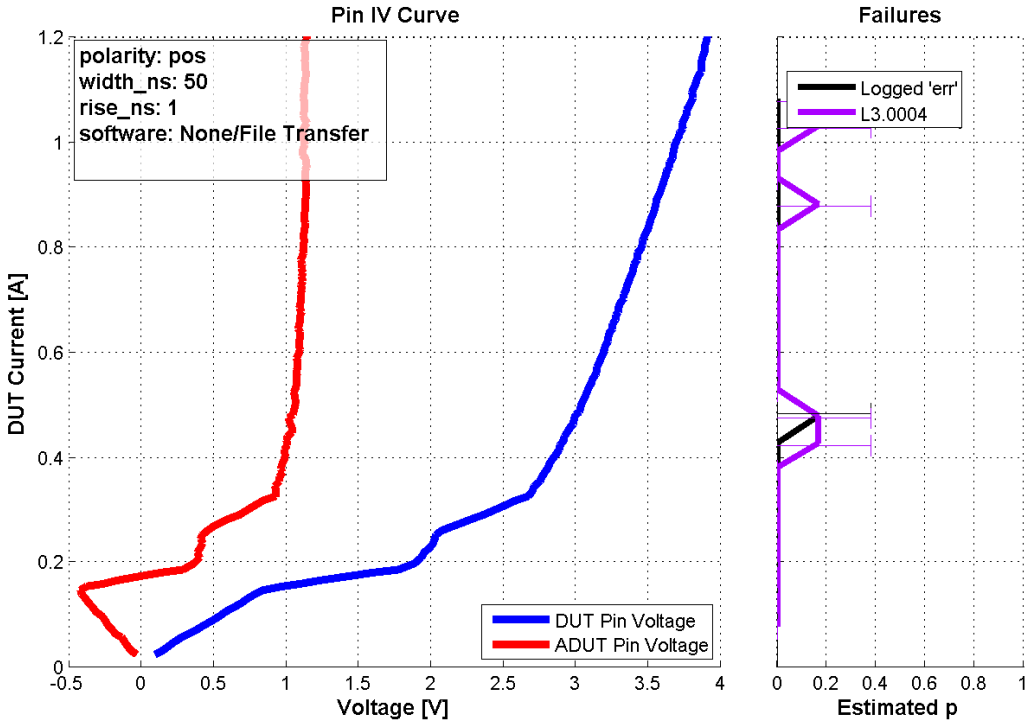

Figure 3.11. USB3_RxP - 50 ns pulse width

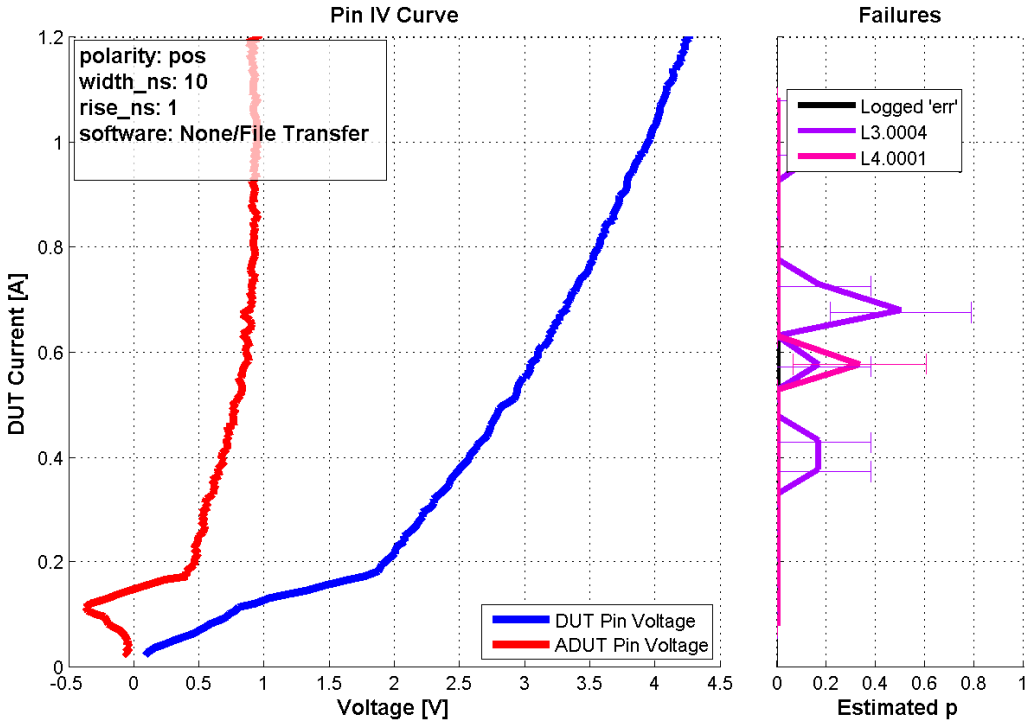

Figure 3.12. USB3_RxP - 10 ns pulse width

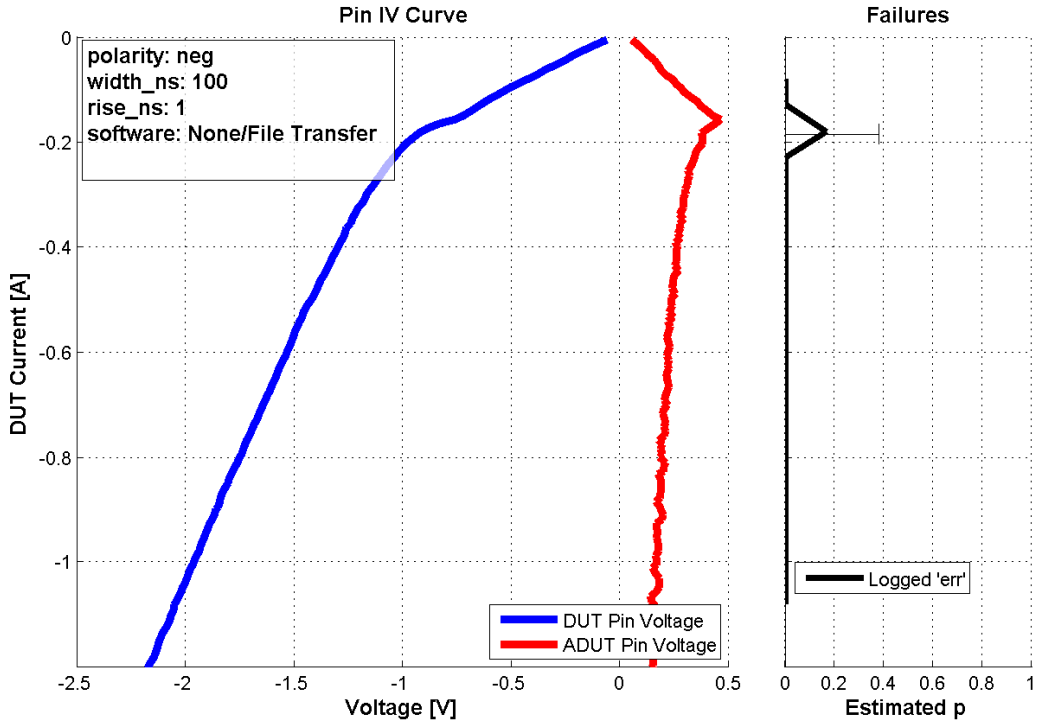

Figure 3.13. USB3_RxP - Negative USB injection example

4. SUMMARY AND ANALYSIS

To summarize, the characterization method is presented and applied to three different interfaces covering several use-cases. Nine separate failure signatures were observed across each of these characterizations (four L2, four L3, and one L4). The first interface demonstrates no significant failures. The second interface is found to have an entirely software-correctable failure which is used to provide feedback to system software teams. The third interface is found to only be sensitive to positive interference events.

Based on this pin-by-pin characterization of soft-failure sensitivities a design methodology can be implemented in a similar manner to the hard fail oriented IC/PCB codesign concept SEED. The understanding of the dependence of failure thresholds on interference pulse width and rise time allows the designer to investigate typical stress scenarios and choose appropriate PCB protections measurements e.g. RC filters, protection devices, or by changing trace layout. These protection-driven modifications can immediately be verified in simulation, thus, a comprehensive pre-hardware verification of the system design can be performed. The following steps are proposed to establish this design method soft fail SEED (SF-SEED) (Figure 4.1).

The first step is to perform the pinwise characterization described herein. In this methodology, selected pins are specified and targeted by a wide variety of pulses under a wide variety of conditions to determine their failure sensitivities. The second step is the generation of a model which is suitable for integrating into design flow software which can describe the failure sensitivities observed in step 1. Finally, these models can be used with the existing SEED methodology of IC and PCB codesign to design with soft-failures in mind, rounding out SF-SEED.

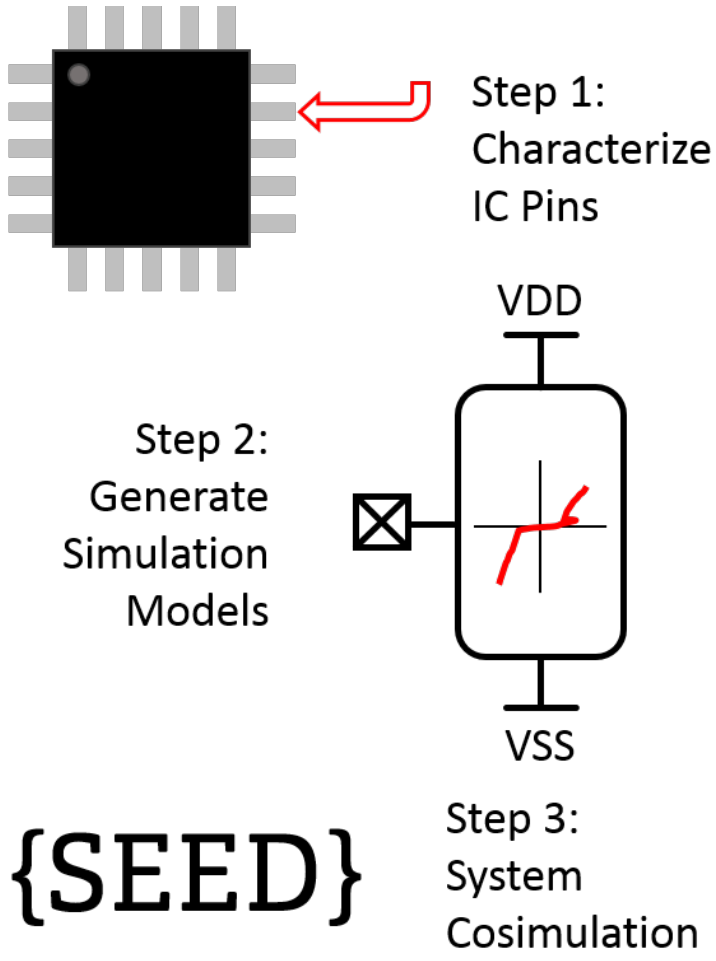

Figure 4.1. SF-SEED Simulation flow

Although the identification and characterization of these soft-errors is helpful, it is important to be aware of the inability of this, or any methodology to predict or even reproduce 100 % of the possible error conditions and scenarios which a system will experience in the field. Although the scope of tests performed during this methodology can be arbitrarily expanded on an implementation-by-implementation basis, it should be, at best, considered an 80 % solution.

5. CONCLUSION

In this paper, a method is outlined to perform ESD-induced soft-failure characterization of IC IO pins on an interface-by-interface basis. Using this characterization methodology several critical soft-failures are identified across three different interfaces. Specific electrical sensitivities such as polarity and pulse width are also identified which trigger error conditions. Using this information, targeted protection strategies are recommended to counter these observed failures. Such strategies can be implemented in systems built around the characterized device, streamlining development cycles and reducing the errors observed in the field.

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SECTION

4. SOFT-FAILURE CAPABLE SEED MODELS

Having established a method to represent arbitrary IV characteristics in SPICE, a method for measuring the behavior of a three-terminal device, and a method for characterizing an individual pin with respect to soft failures, these methods can now be combined. The proposed model is capable of representing the IV relationship of the pin in circuit simulation as well as any number of failure "modules" capable of describing various failure symptoms. These models, because of their flexibility are not discussed exhaustively here but several examples are given which directly relate to measurement results.

An overview of the proposed model is shown in Figure 4.1 and consists of two major parts. The first part is an electrical model to represent the pin IV characteristic which outputs control signals such as the pin current or voltage. The second part is any number of failure blocks which use the aforementioned control signals to generate outputs to indicate potential failures.

The electrical models are further subdivided into both long- and short-time models. The long-time model (LTM) is simply a representation of the familiar TLP IV behavior. This behavior, being measured when the applied TLP pulse has reached steady state, represents the nonlinear real portion of the apparent pin impedance $Z(i) = R(i)$. The short-time model (STM) is a representation of the nonlinear imaginary portion of the pin $Z(i) = jX(i)$ which dominates in the first 1-2 nanoseconds of the response. This short-time model may or may not be required depending on the desired level of model detail. The short-time behavior of an IC pin can be approximately determined with an appropriate Very Fast-TLP

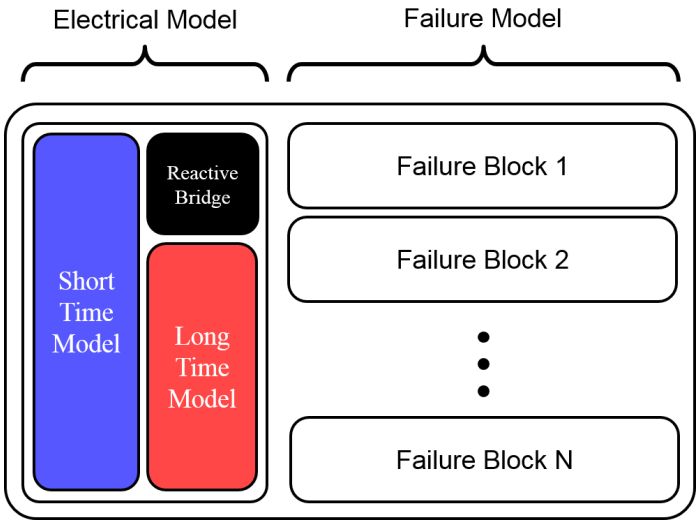
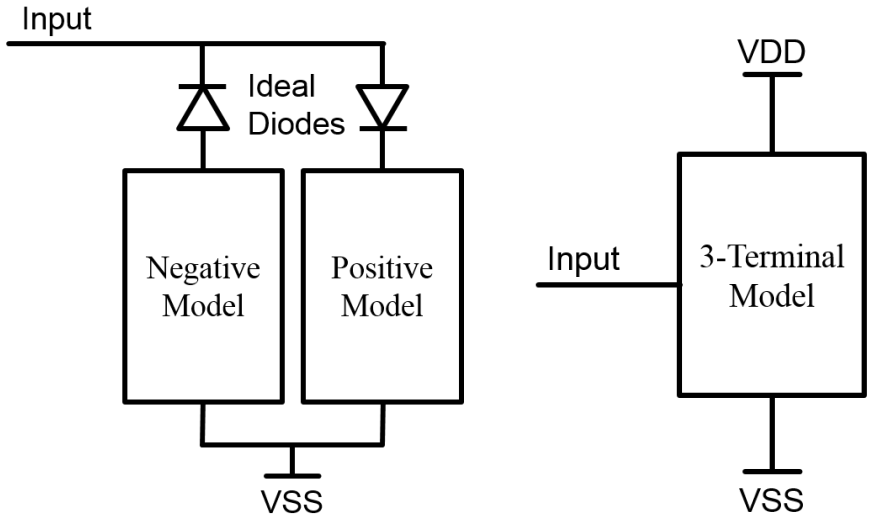


Figure 4.1. Pin model overview

measurement system which is capable of determining the rising-edge behavior of a pulse incident on the pin under test. By moving the TLP average window to measure the rising edge of the pulse, a rough model can then be built. To combine the LTM and STM, a small inductor 10 nH is used to isolate the LTM from the input. This arrangement momentarily isolates the pulse from the LTM, revealing only the STM.

The electrical model can be represented in either of the methods shown in Figure 4.2. In both cases, the IV behavior is measured while the pin is in the powered condition but in Figure 4.2a the VDD current measurement introduced in the three-terminal characterization method is unused. In this way, the behavior of the pin and power network are lumped together into a single representation. Alternatively, a full three-terminal model such as in Figure 4.2b can be implemented as described in Section 3. The decision to implement one or the other model can be arbitrary, or it can be dictated by observed device failure behaviors. If important observed failures depend on the current which is injected onto the VDD network then a three-terminal model may be better suited than the simplified model.



(a) Simplified two-terminal model (b) Full three-terminal model

Figure 4.2. Two and three-terminal electrical model formation

An example electrical model based on one of the pins measured in Paper 4 is shown in Figure 4.3. This electrical model uses a diode and capacitor to model the approximate short-time behavior of the pin, a piecewise-linear IV curve to describe the long-time behavior, and is arranged in the form of a simplified two terminal model such as in Figure 4.2a. Figure 4.4 shows a comparison between the short- and long-time behaviors of the measurement and model.

While there are two potential implementations of the electrical model, failure block implementations are far less constrained. Observed soft-failures may be correlated with injected charge, pulse voltage, pulse current, pulse width, pulse polarity, etc. necessitating the implementation of a wide variety of relationships between one or more control signal a digital or analog output voltage. These failure blocks are implemented as basic single input single output systems which transform the control parameter into a failure probability which is indicated by a voltage [0-1] V (Figure 4.5).

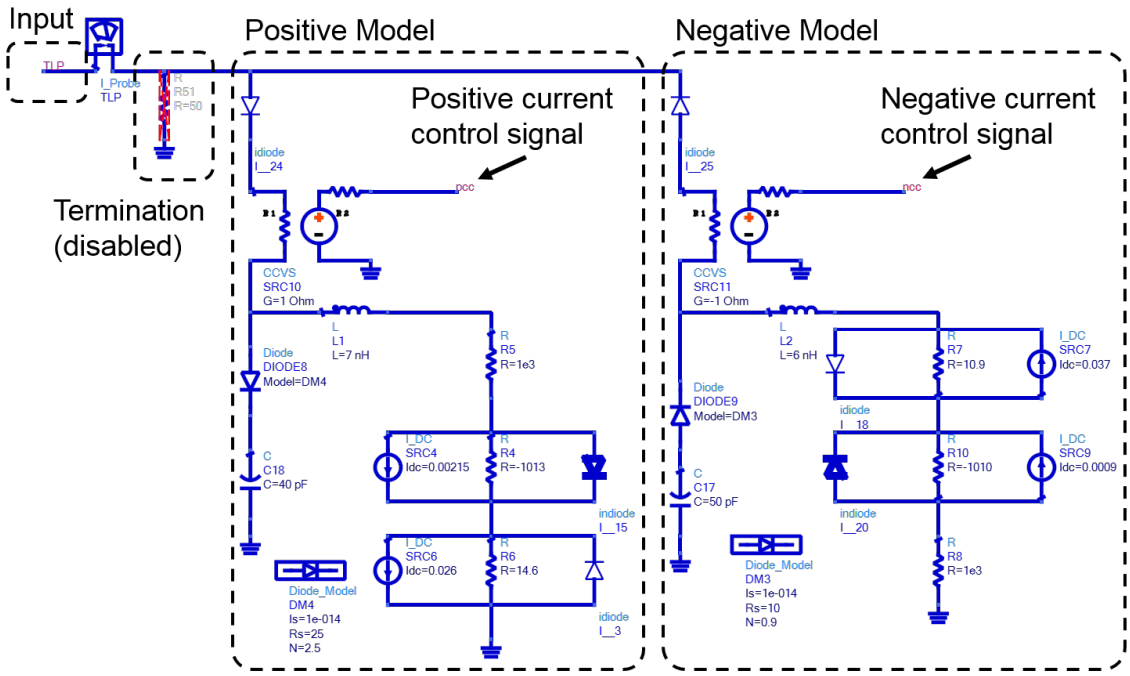


Figure 4.3. Example SPICE pin model

Examples of three single-input single-output failure blocks are shown in Figure 4.6. Figure 4.6a is a pulse charge detector which outputs a constant 0.8 V after the 20 nC threshold has been reached, Figure 4.6b acts as a nearly amplitude-independent pulse width detector which outputs a constant 0.8 V when pulses exceed 100 ns, Figure 4.6c is a pulse amplitude detector which outputs a ramp voltage proportional to the pin current after a minimum current threshold is reached. The outputs of each of these failure blocks are interpreted in simulation as the probability that the failure which they model will occur as a result of the given stimulus.

To demonstrate the functionality of this model format, the long and short time behaviors captured in Figure 4.3 are married with the failure blocks outlined in Figure 4.6. The resultant model (Figure 4.7) is excited by a series of batched transient simulations

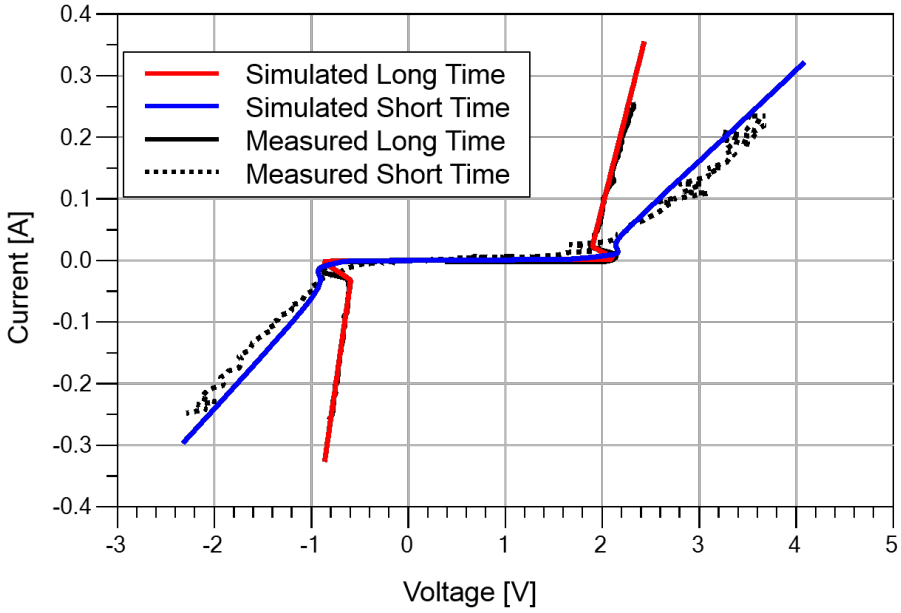
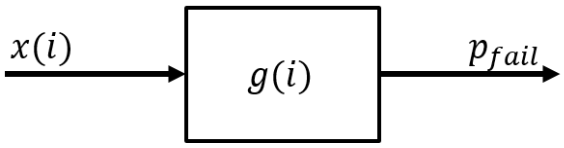
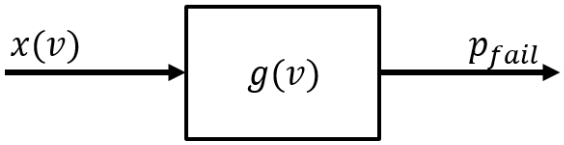


Figure 4.4. Comparison between three-terminal characterization measurements and simulation of long- and short-time models



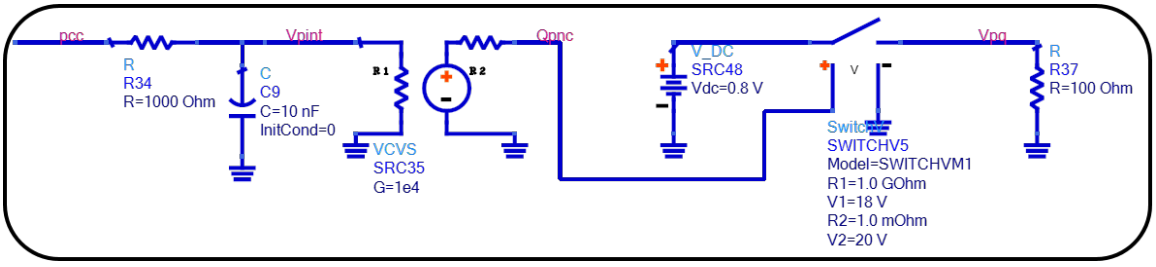
(a) Single-input, current dependent failure block



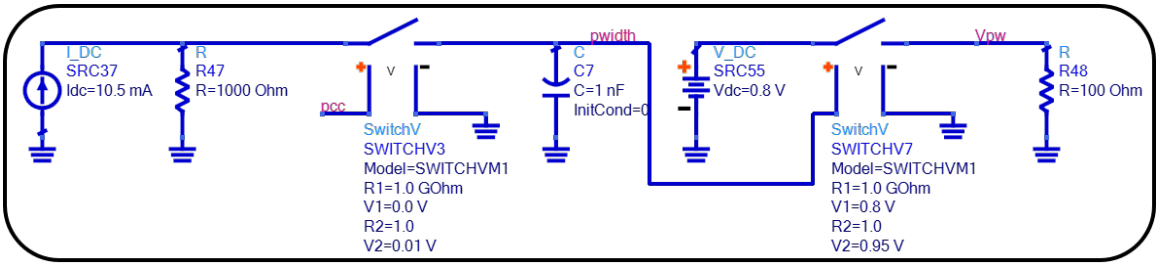
(b) Single-input, voltage dependent failure block

Figure 4.5. Failure block forms

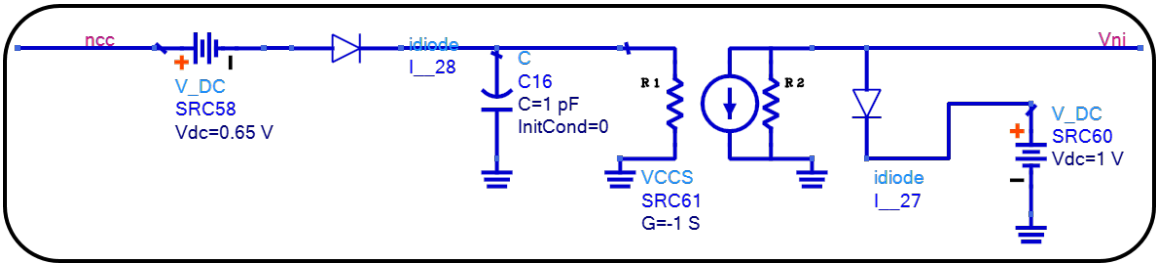
to emulate a TLP sweep. Keeping in mind that the current measured during DCI is overestimated due to the error phenomenon shown in Figure 3.4, a comparison of the measurement-generated model and the measurements themselves for several pulse widths



(a) Pulse charge detector (20 nC), input: ncc, output: Vpq



(b) Pulse width detector (100 ns), binary output, input: pcc, output: Vpw



(c) Pulse amplitude detector, ramp output, input: ncc, output: Vni

Figure 4.6. Example failure blocks

are shown in Figure 4.8 - Figure 4.13. In simulation, the blue and red curves both indicate the probability that the L2.0001 failure will occur and thus should be logically OR'ed together to find the failure probability. The pink curve in the negative measurements (Figure 4.12 and Figure 4.13) corresponds to the L2.0002 failure.

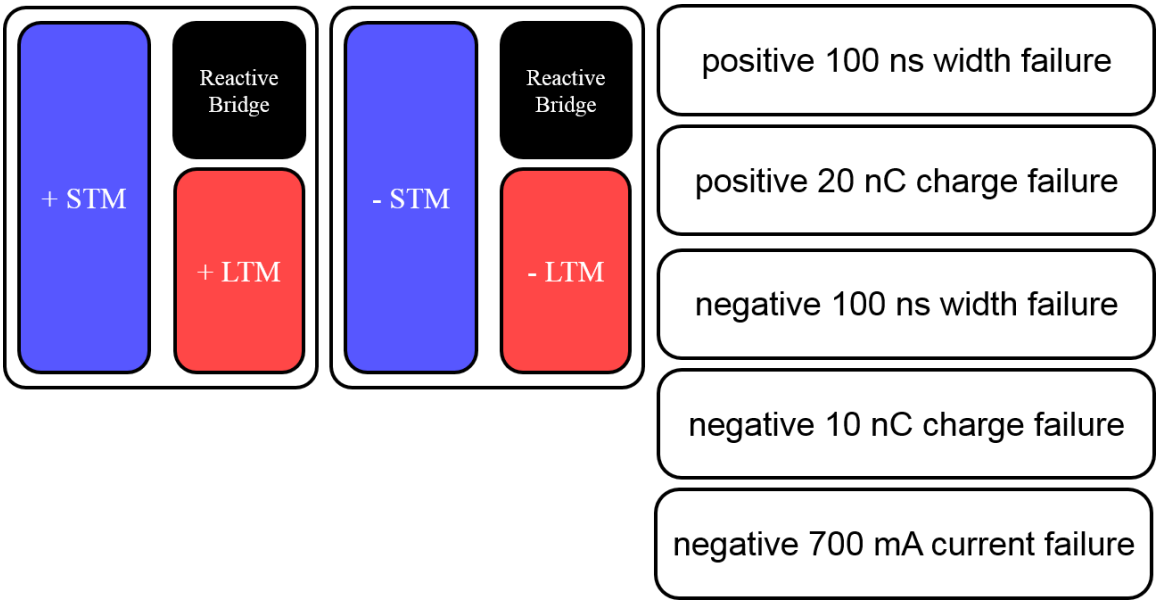


Figure 4.7. Complete pin model outline

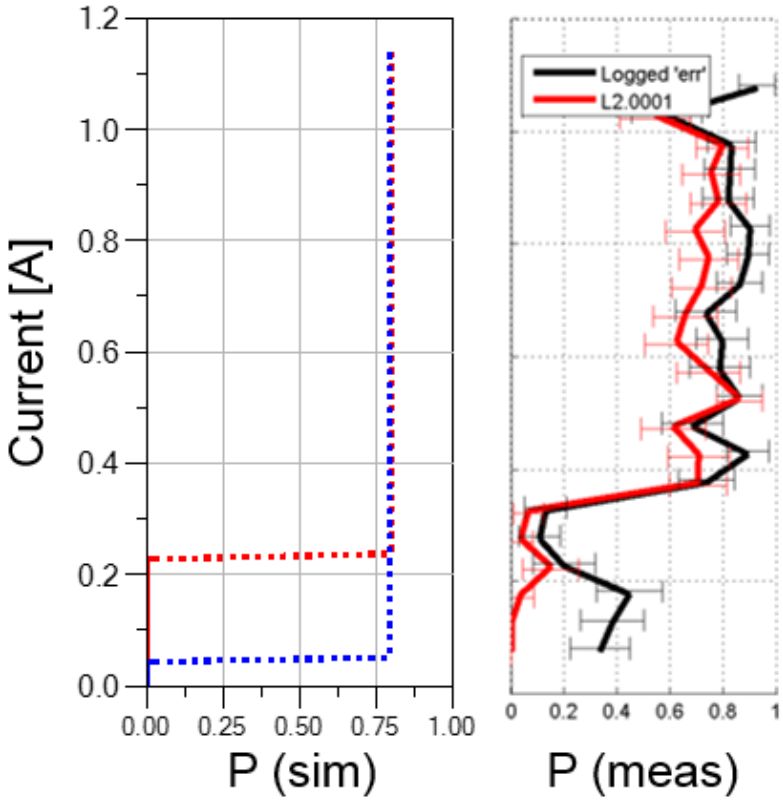


Figure 4.8. Measurement and model comparison (positive, 100 ns injection), the blue and red simulated traces indicate L2.0001

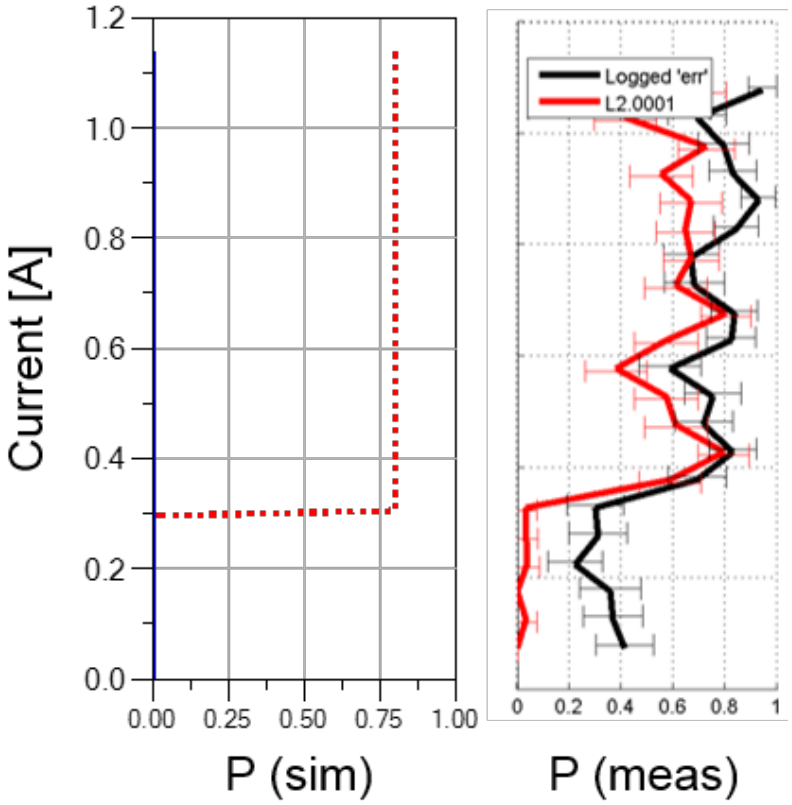


Figure 4.9. Measurement and model comparison (positive, 75 ns injection), the blue and red simulated traces indicate L2.0001

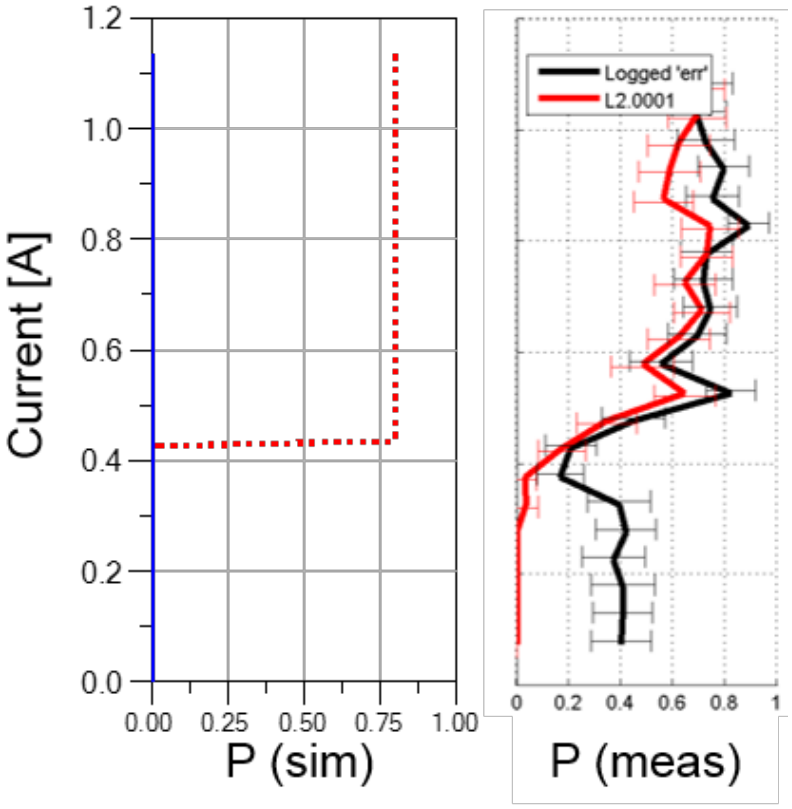


Figure 4.10. Measurement and model comparison (positive, 50 ns injection), the blue and red simulated traces indicate L2.0001

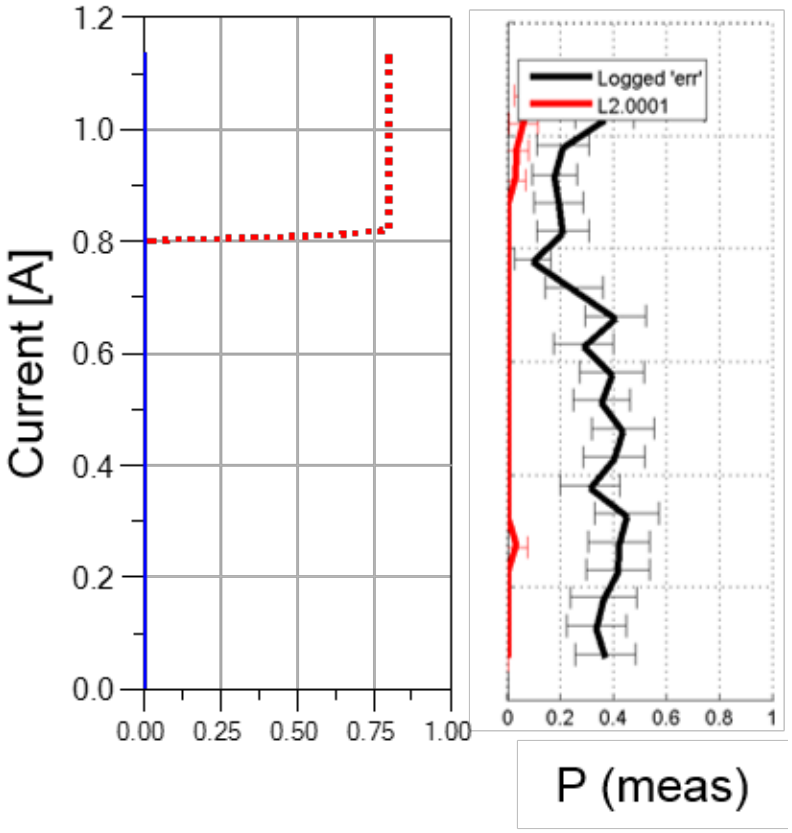


Figure 4.11. Measurement and model comparison (positive, 25 ns injection), the blue and red simulated traces indicate L2.0001

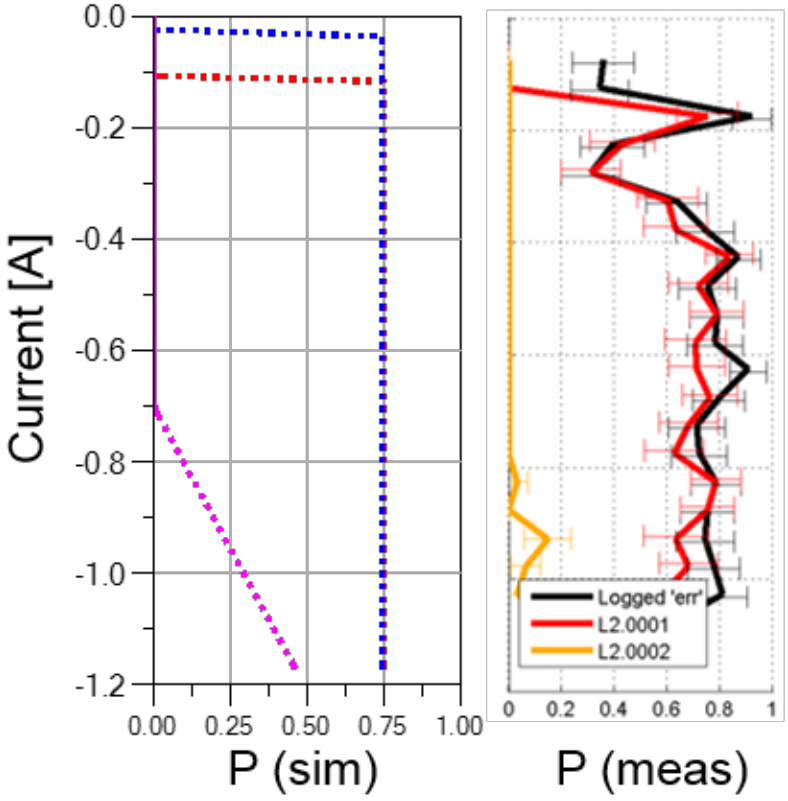


Figure 4.12. Measurement and model comparison (negative, 100 ns injection), the blue and red simulated traces indicate L2.0001, the pink trace indicates L2.0002

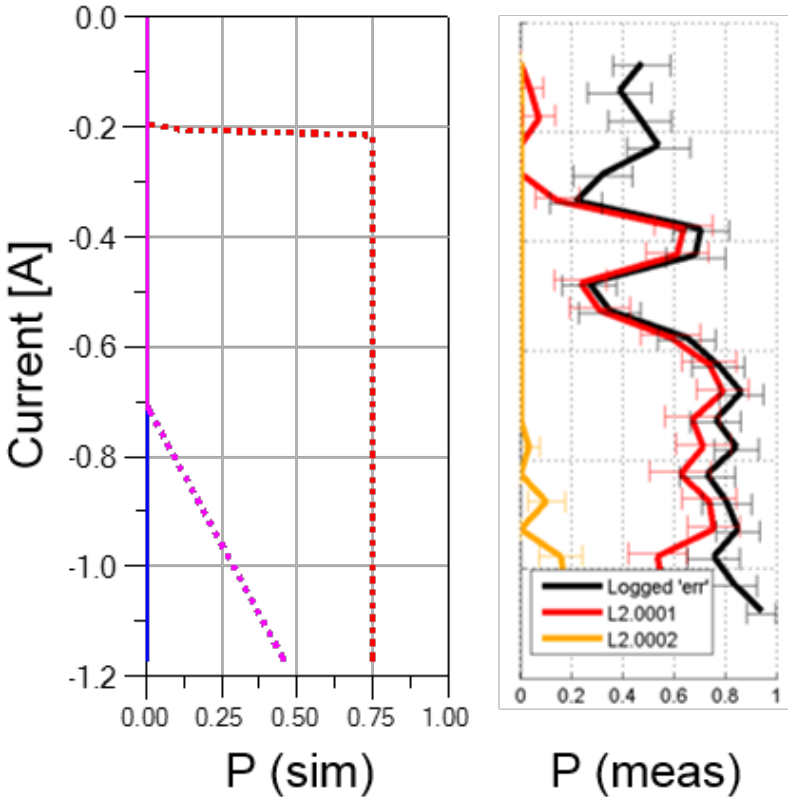


Figure 4.13. Measurement and model comparison (negative, 50 ns injection), the blue and red simulated traces indicate L2.0001, the pink trace indicates L2.0002

5. CONCLUSION

Over the course of this work, a methodology has been outlined which enables the characterization of an integrated circuit with respect to ESD-induced soft failures and the subsequent generation of models which are suitable for representing the aforementioned characterization in circuit simulation. During the development of this methodology, a number of challenges were encountered and addressed. The first challenge was the expression of arbitrary IV curves in SPICE. This was addressed by taking a previously developed method for expressing arbitrary IV relationships and reimplementing it in modern simulation software for use in the context of ESD. The second challenge was to determine an appropriate methodology for extracting the IV behavior of a DUT under relevant conditions. The third challenge was to determine a framework which can be used to simplify the problem of characterizing an integrated circuit with many hundreds of pins. By developing the diode injection system, the system characterization framework could be implemented and tested on the system scale rather than an individual IC itself. Once this framework was established, the challenge became to inject stress pulses into a system which only reached the DUT IC. To address this, the directed current injection system was developed, finally enabling the characterization of an IC inside of a running system. With this characterization in hand, a modeling methodology was proposed to describe the behavior of individual IC pins with respect to soft failures during circuit simulation. Such models can therefore be used to apply system-level ESD codesign methodologies to address soft-failures negating potential issues before they are discovered in the field.

APPENDIX A

CAMERA PIN (CSIX) CHARACTERIZATION MEASUREMENT RESULTS

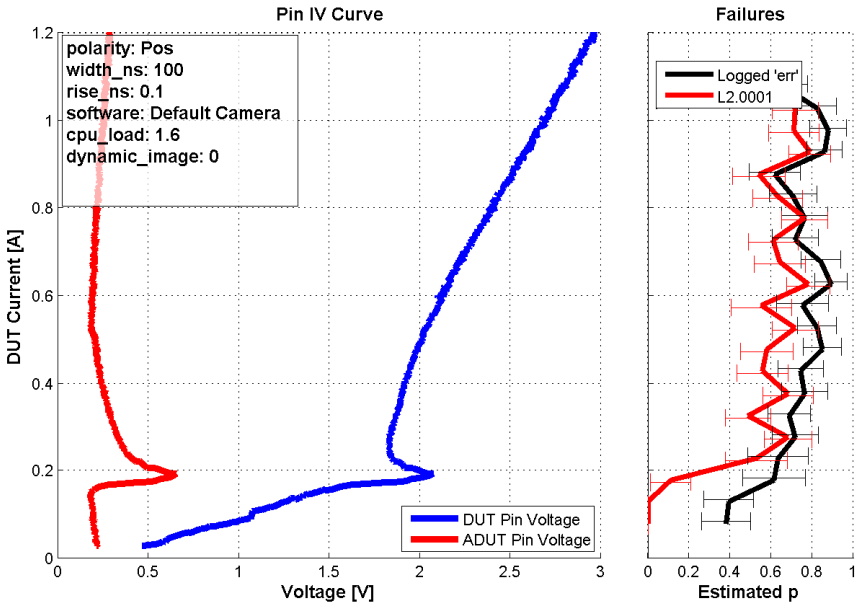


Figure A.1. CSIx_CLKx, positive pulse width test

NOTE: All test which fall under the category of pulse sweep did not record the L2.0002 failure. This error is therefore not plotted.

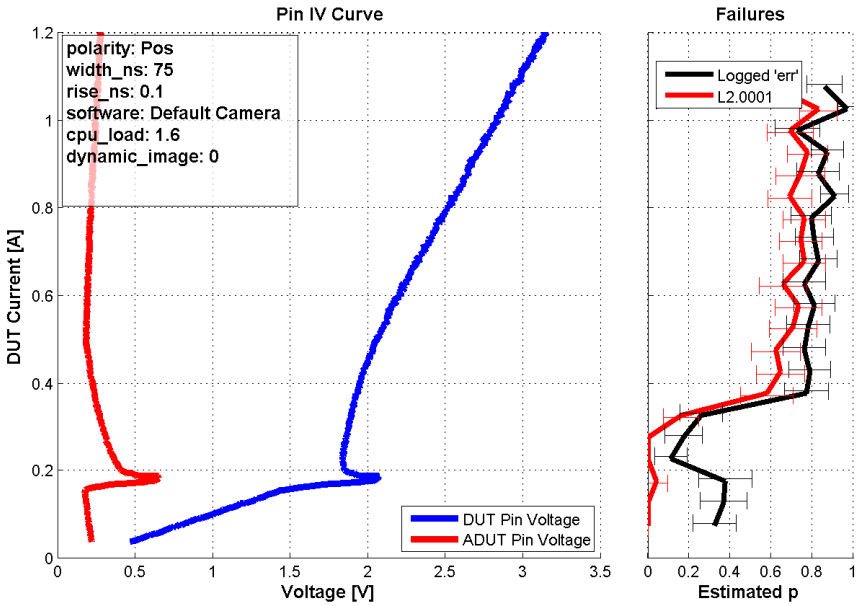


Figure A.2. CSIx_CLKx, positive pulse width test

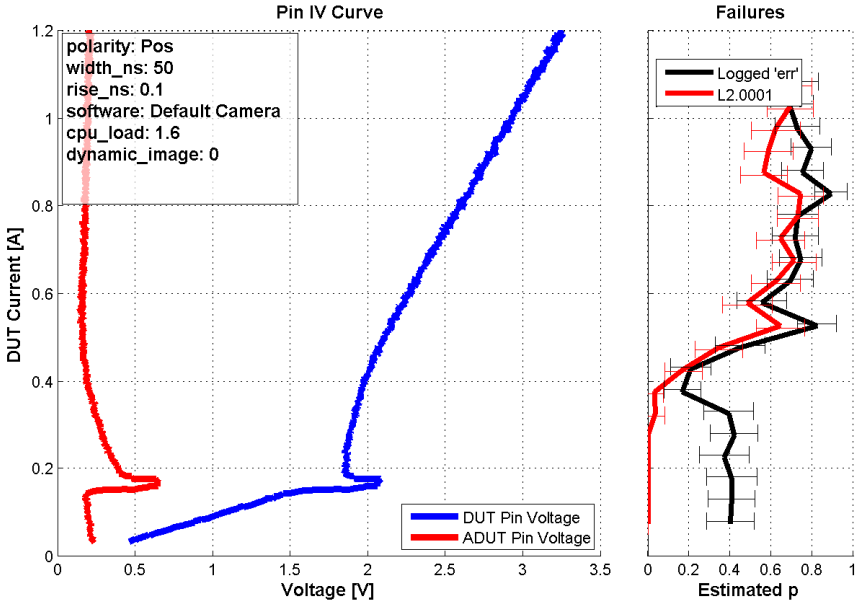


Figure A.3. CSIx_CLKx, positive pulse width test

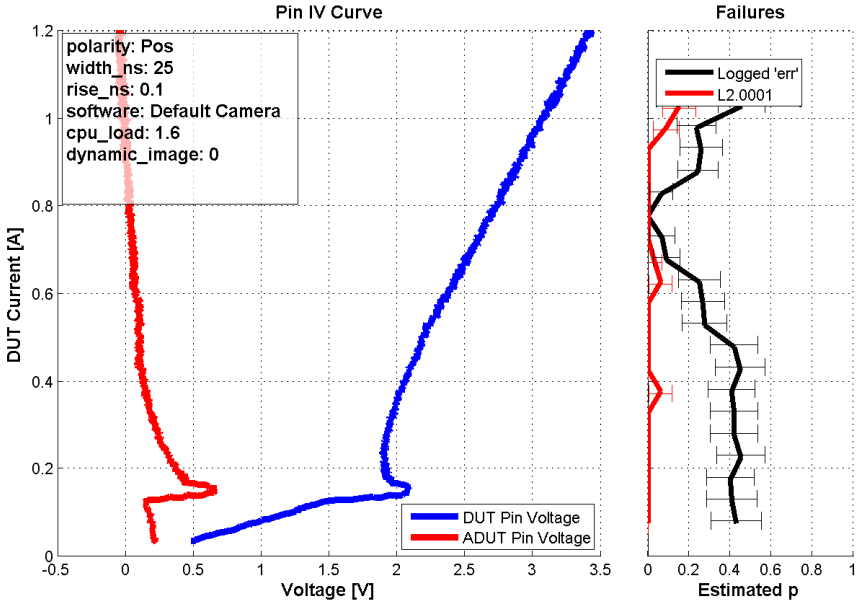


Figure A.4. CSIx_CLKx, positive pulse width test

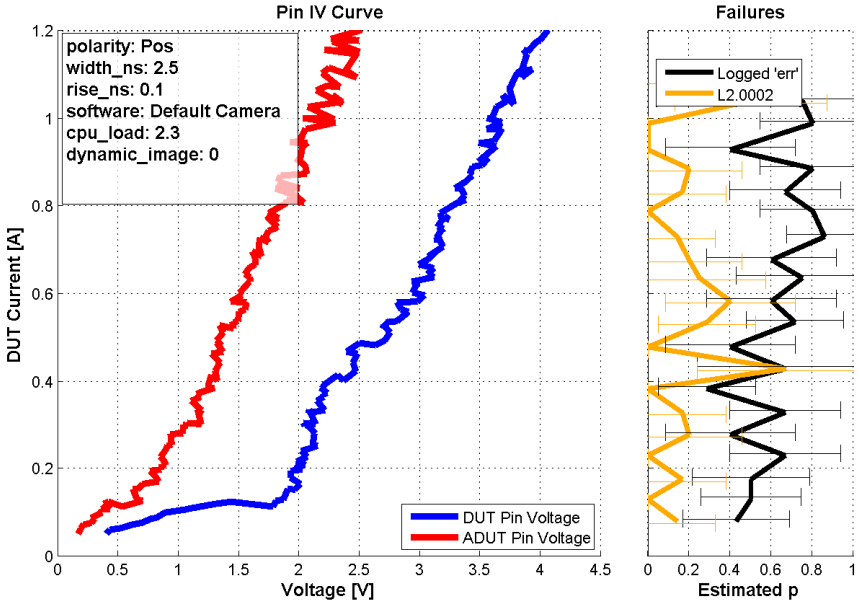


Figure A.5. CSIx_CLKx, positive pulse width test

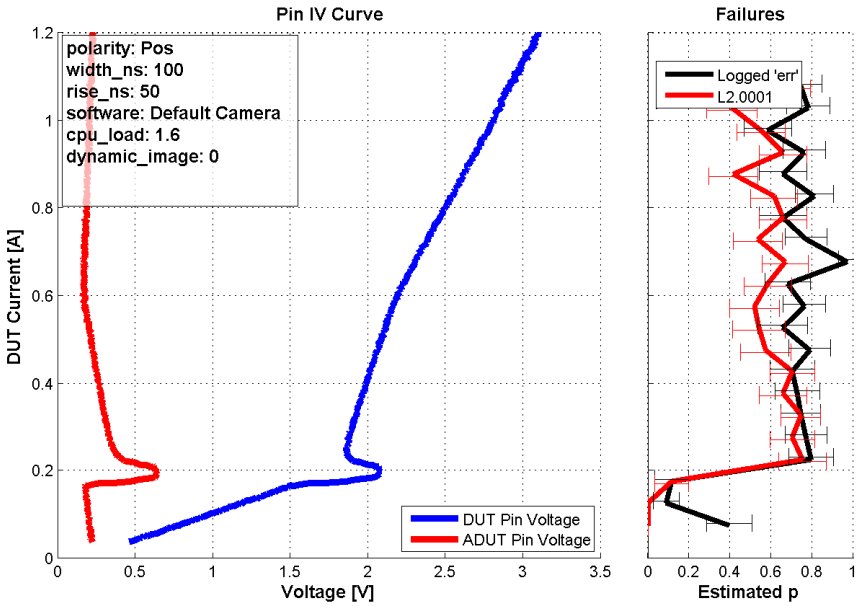


Figure A.6. CSIx_CLKx, positive pulse rise time test

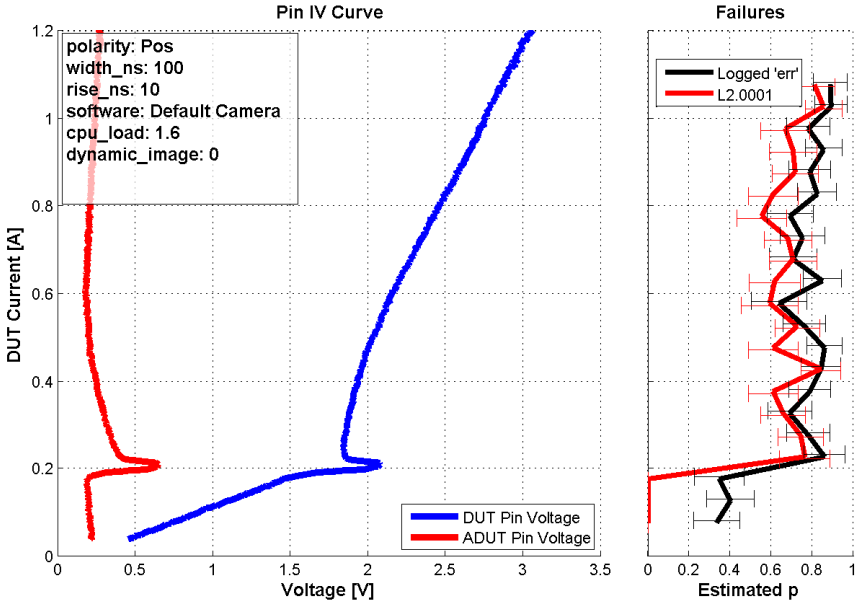


Figure A.7. CSIx_CLKx, positive pulse rise time test

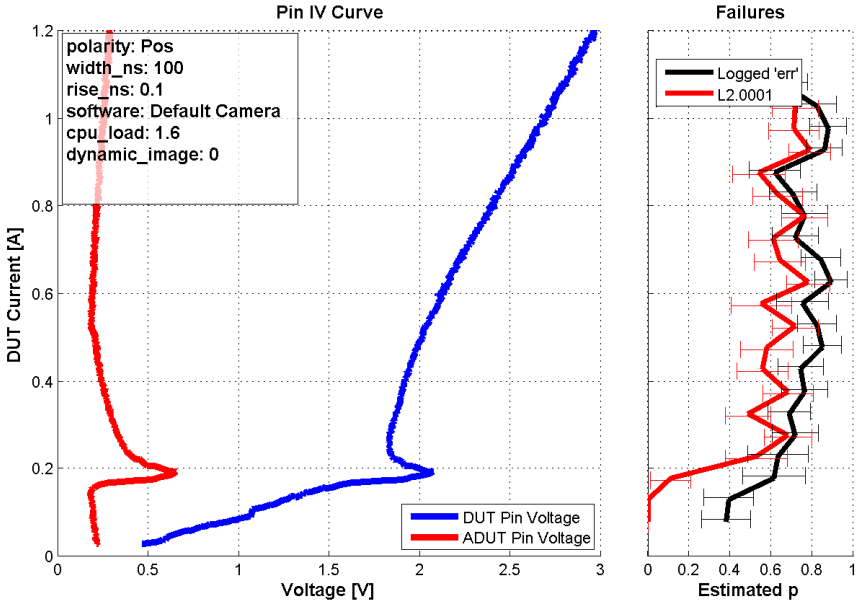


Figure A.8. CSIx_CLKx, positive pulse rise time test

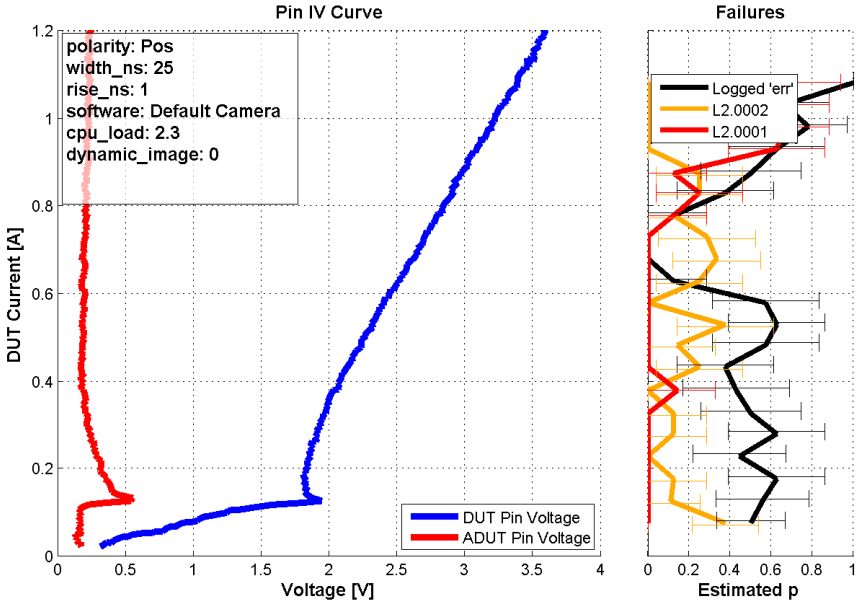


Figure A.9. CSIx_CLKx, positive average threadcount test

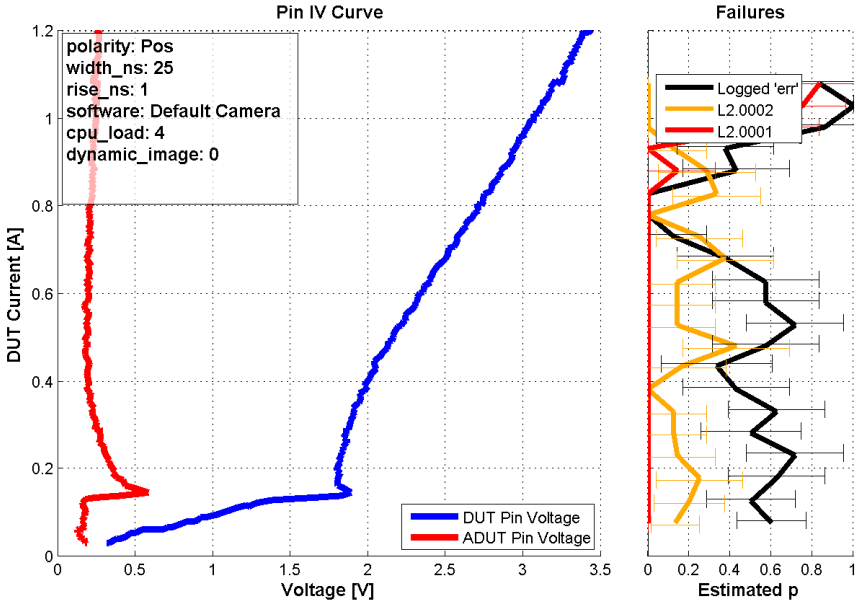


Figure A.10. CSIx_CLKx, positive average threadcount test

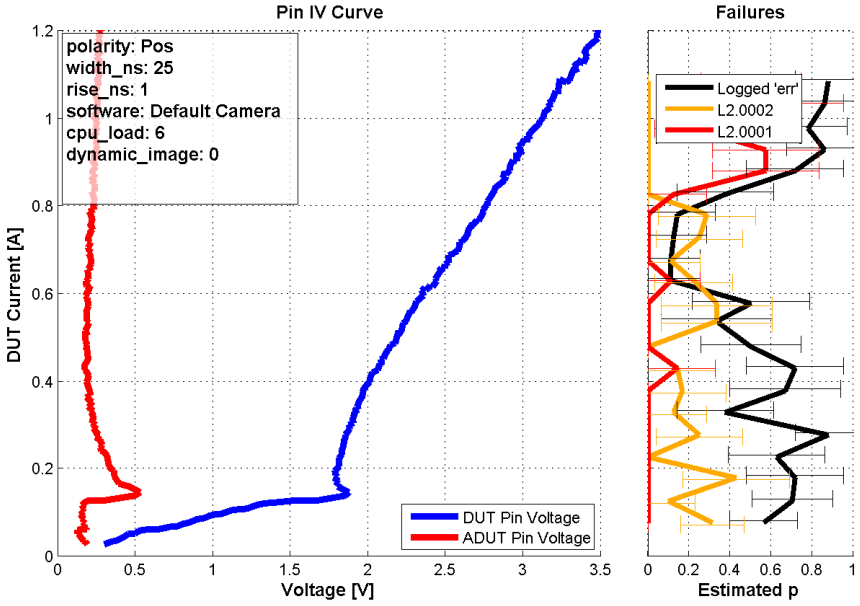


Figure A.11. CSIx_CLKx, positive average threadcount test

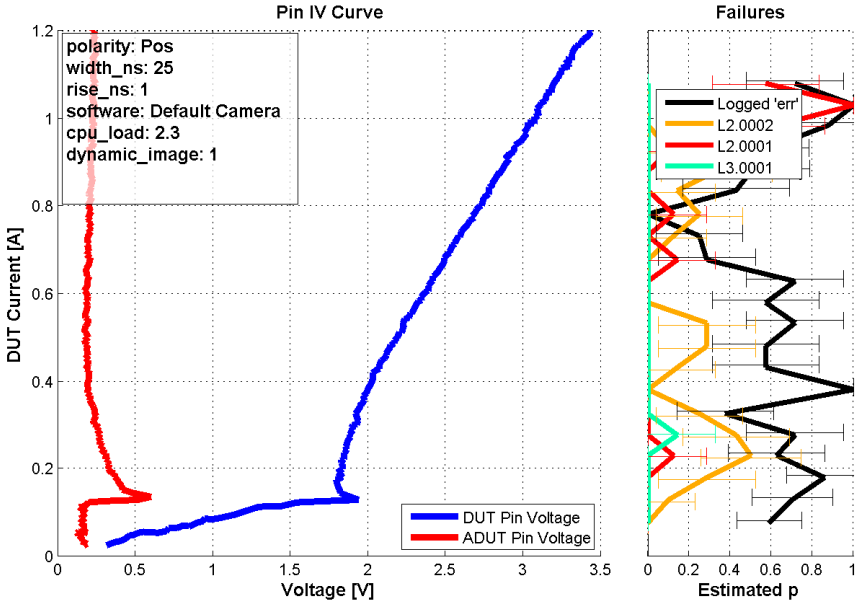


Figure A.12. CSIx_CLKx, positive average threadcount test

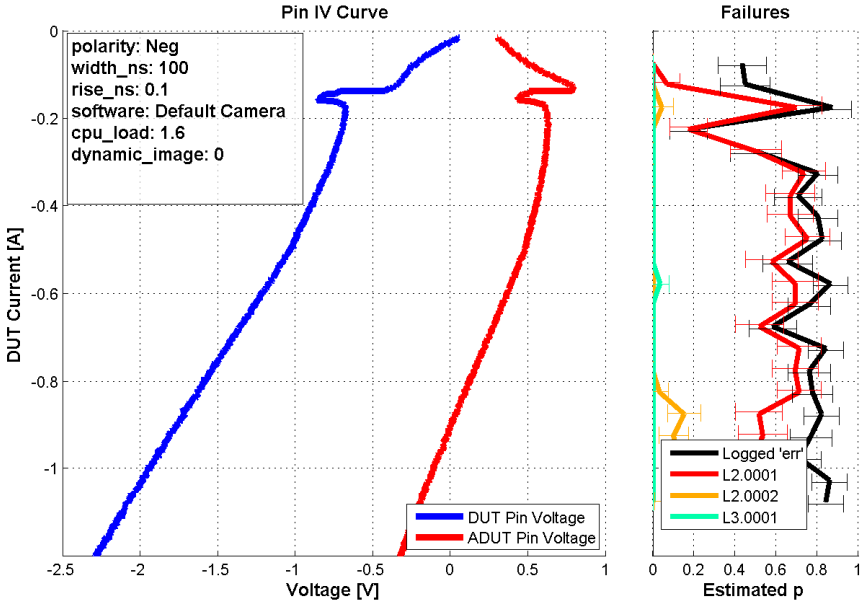


Figure A.13. CSIx_CLKx, negative pulse width test

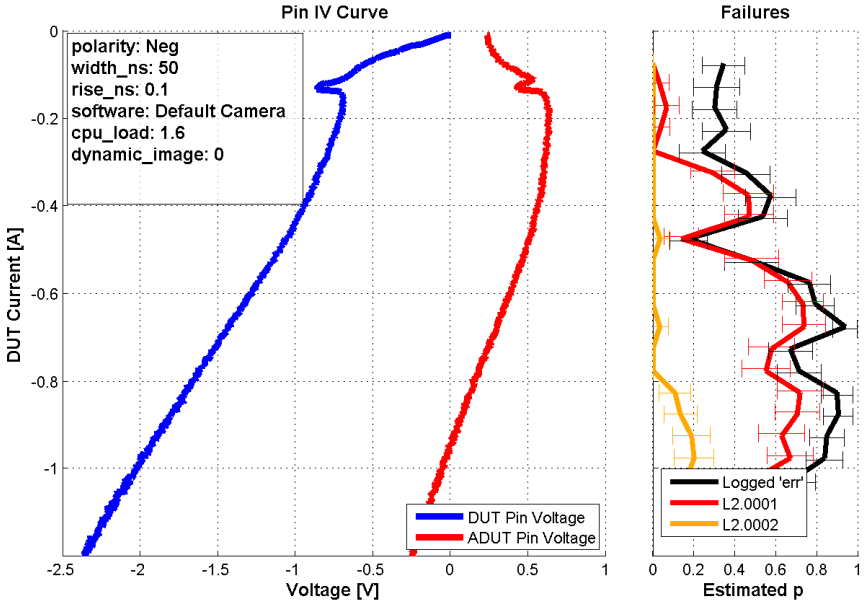


Figure A.14. CSIx_CLKx, negative pulse width test

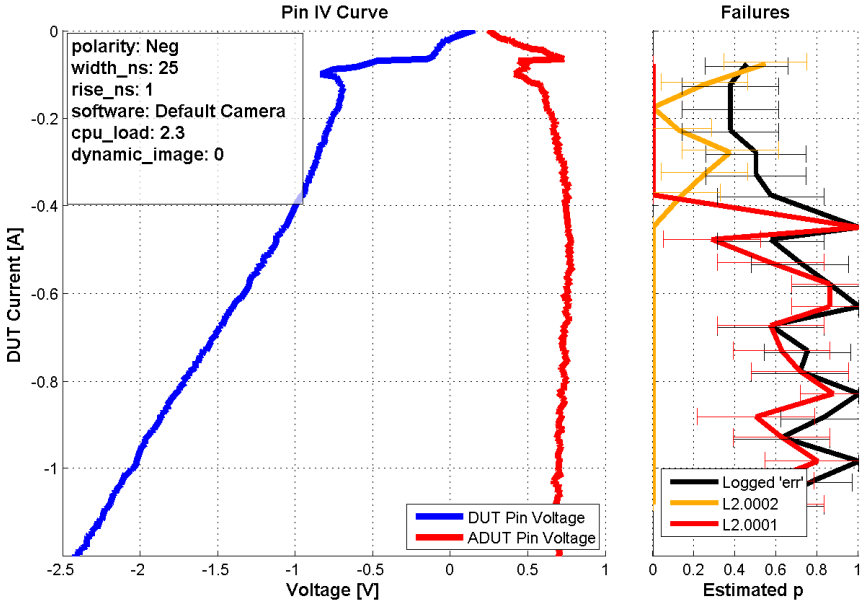


Figure A.15. CSIx_CLKx, negative pulse width test

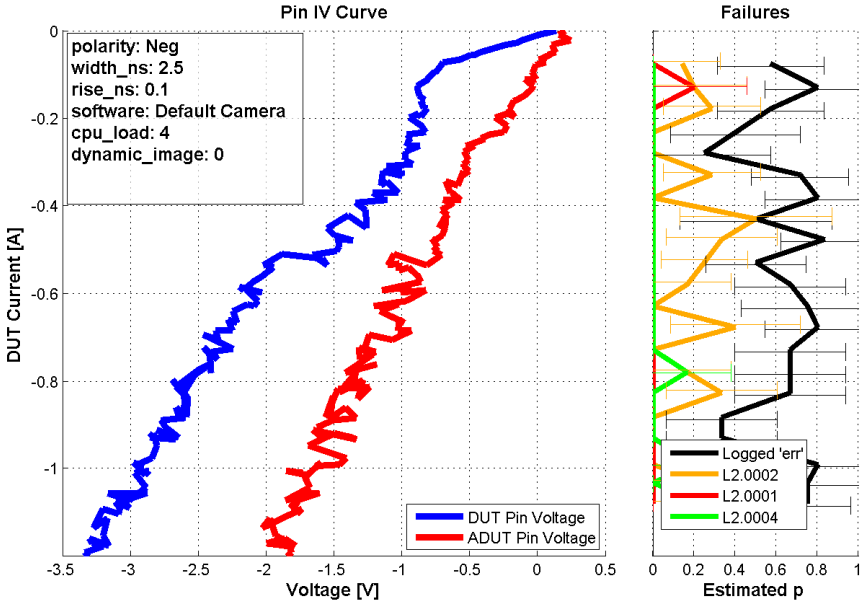


Figure A.16. CSIx_CLKx, negative pulse width test

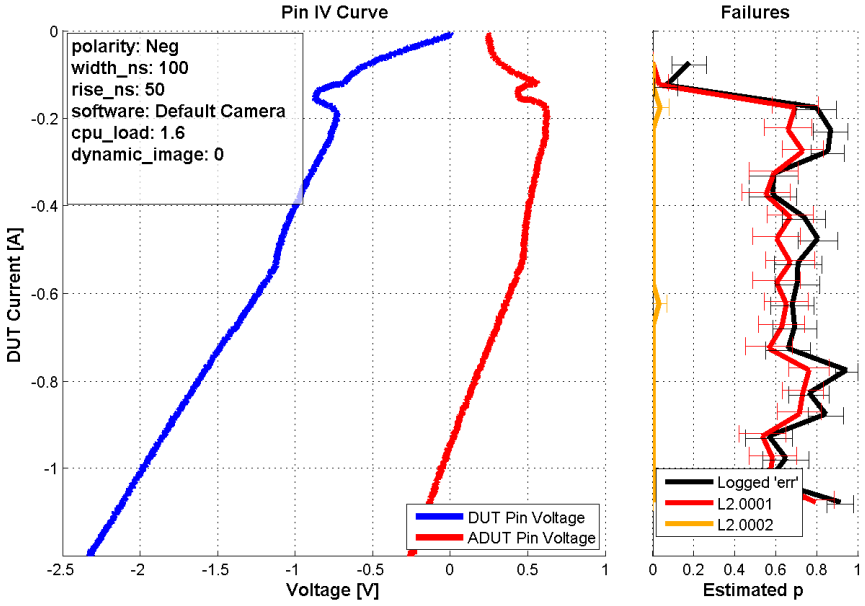


Figure A.17. CSIx_CLKx, negative pulse rise time test

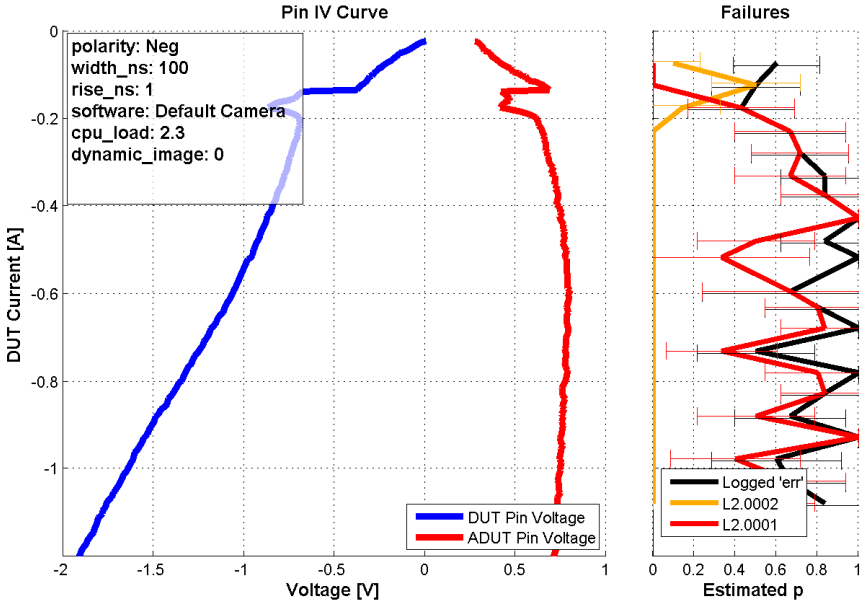


Figure A.18. CSIx_CLKx, negative pulse rise time test

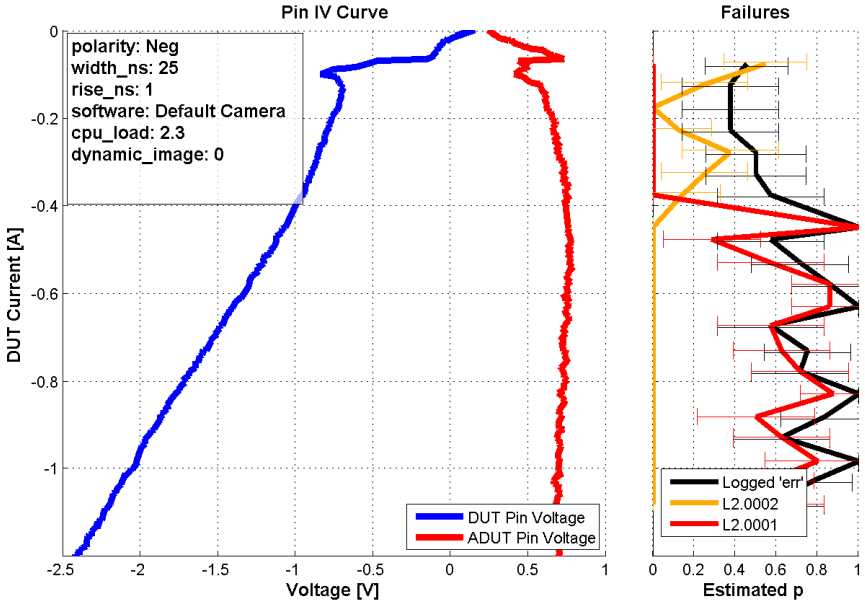


Figure A.19. CSIx_CLKx, negative average threadcount test

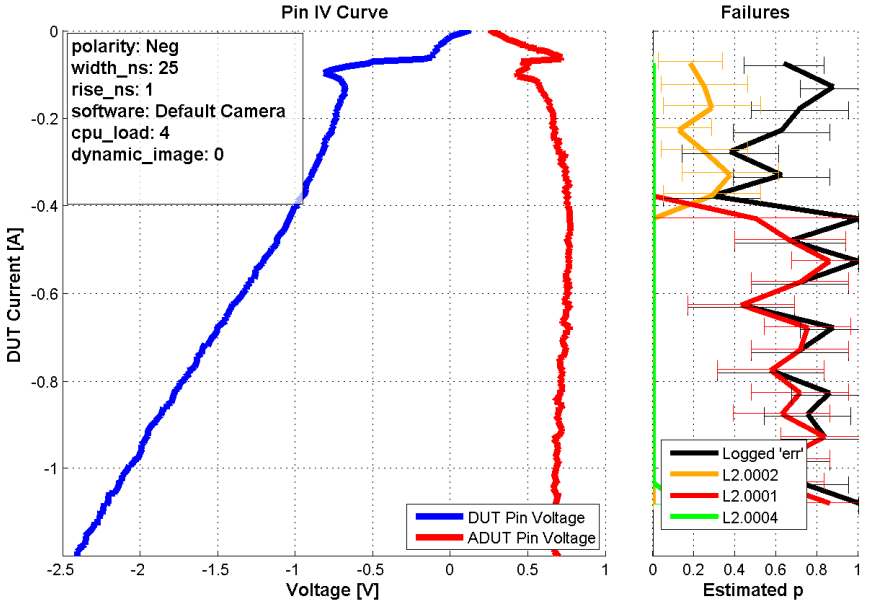


Figure A.20. CSIx_CLKx, negative average threadcount test

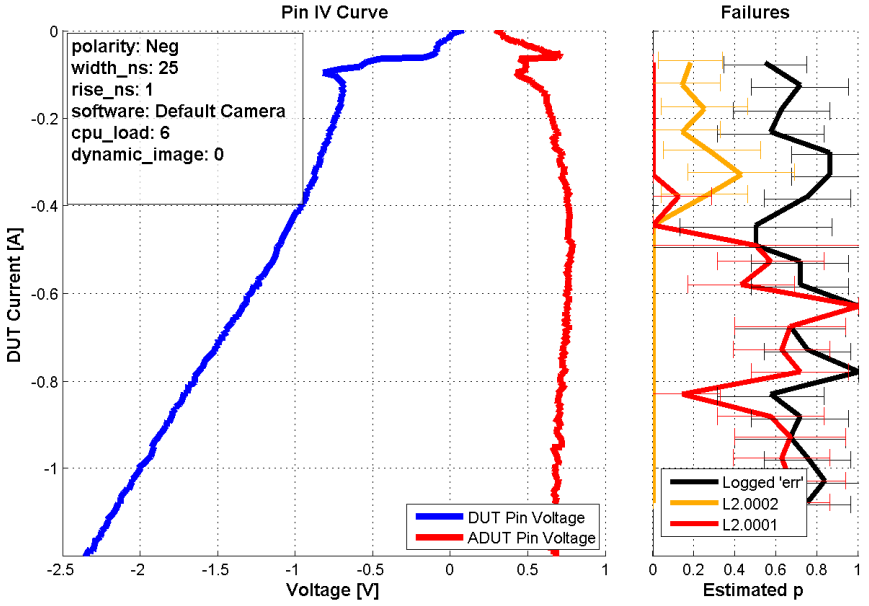


Figure A.21. CSIx_CLKx, negative average threadcount test

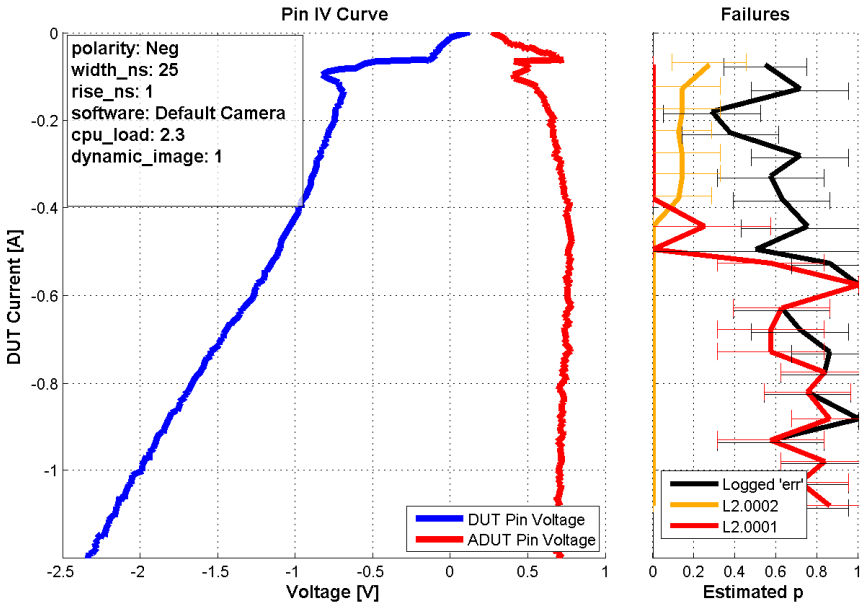


Figure A.22. CSIx_CLKx, negative average threadcount test

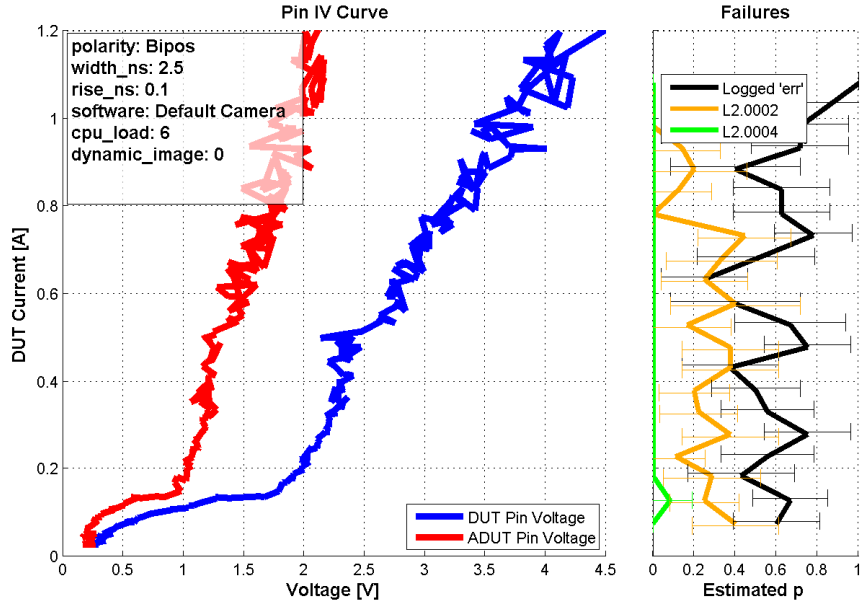


Figure A.23. CSIx_CLKx, bipolar test

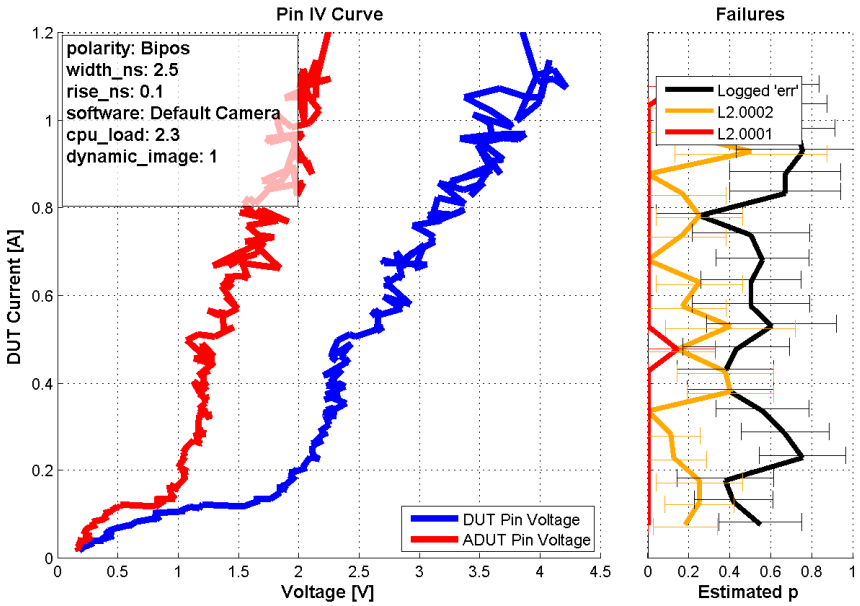


Figure A.24. CSIx_CLKx, bipolar test

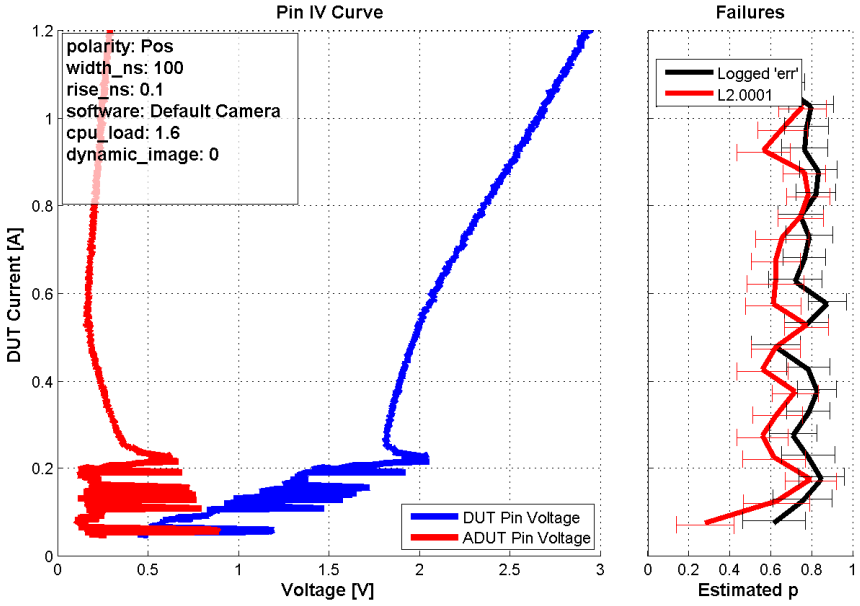


Figure A.25. CSIx_Cxx, positive pulse width test

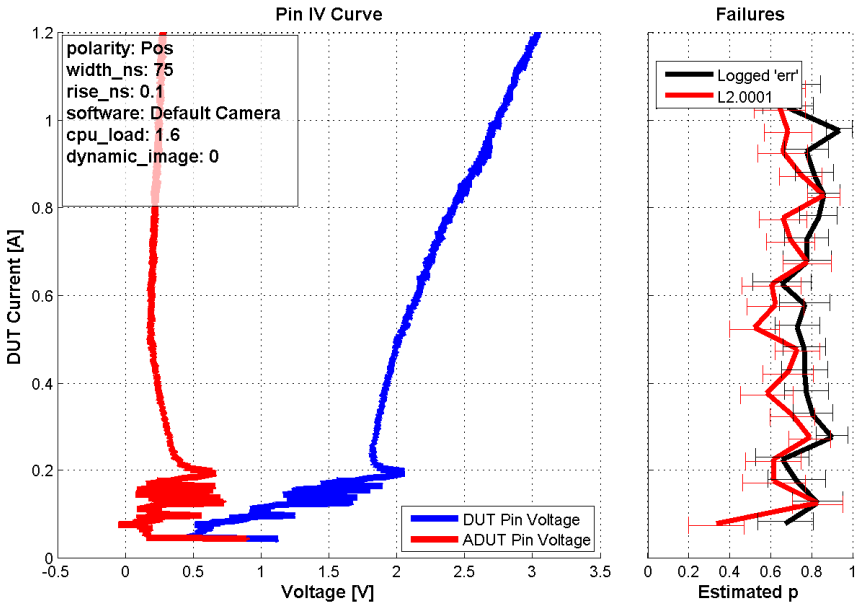


Figure A.26. CSIx_Cxx, positive pulse width test

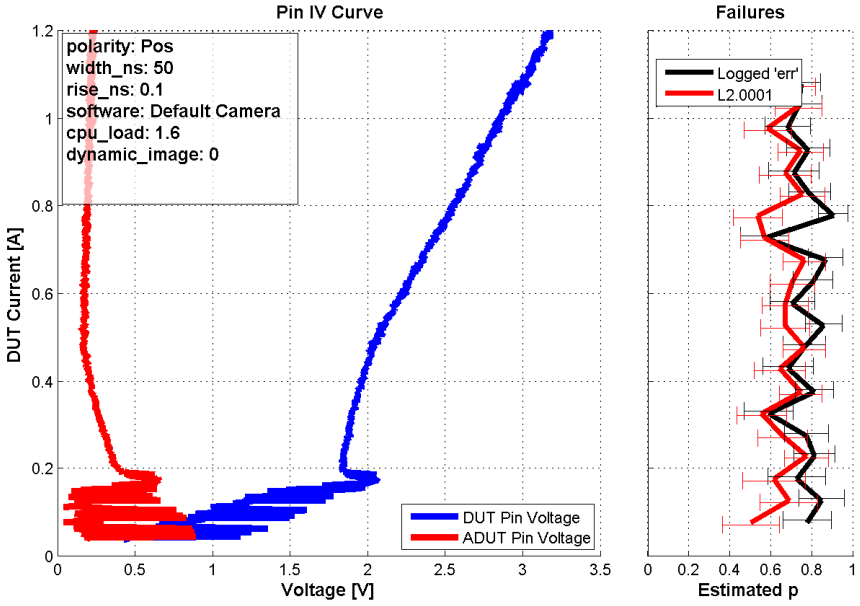


Figure A.27. CSIx_Cxx, positive pulse width test

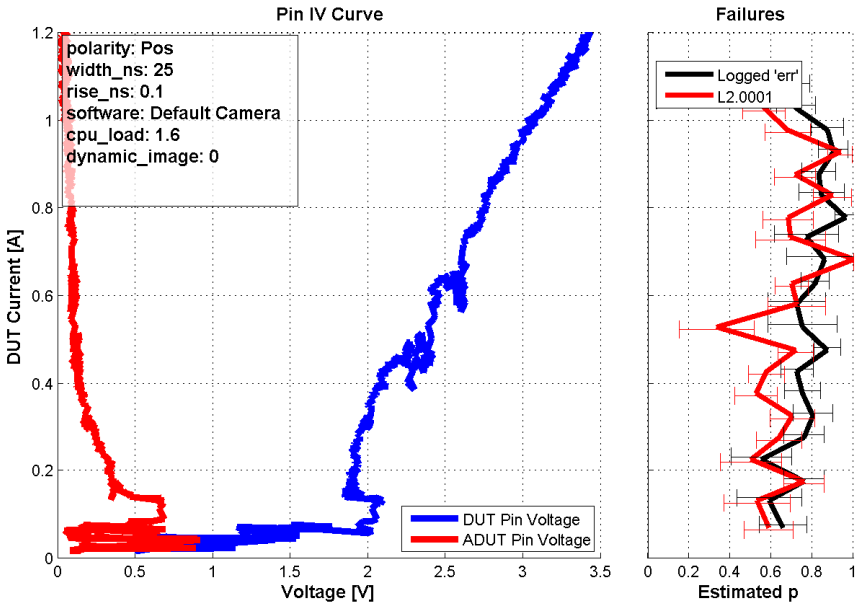


Figure A.28. CSIx_Cxx, positive pulse width test

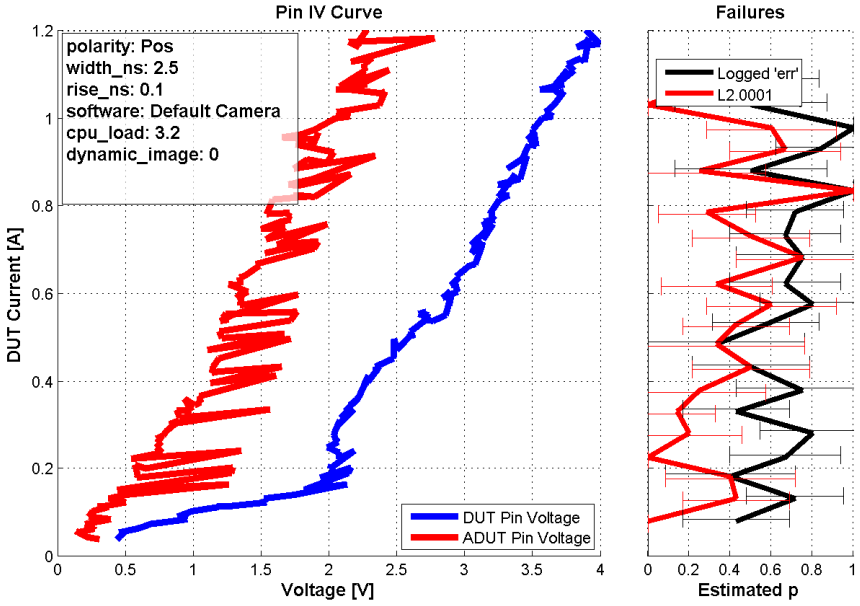


Figure A.29. CSIx_Cxx, positive pulse width test

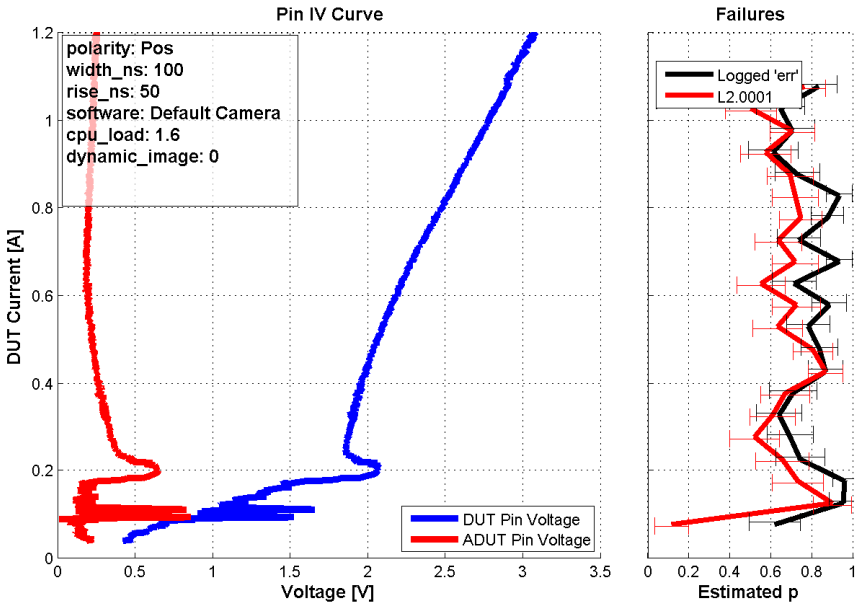


Figure A.30. CSIx_Cxx, positive pulse rise time test

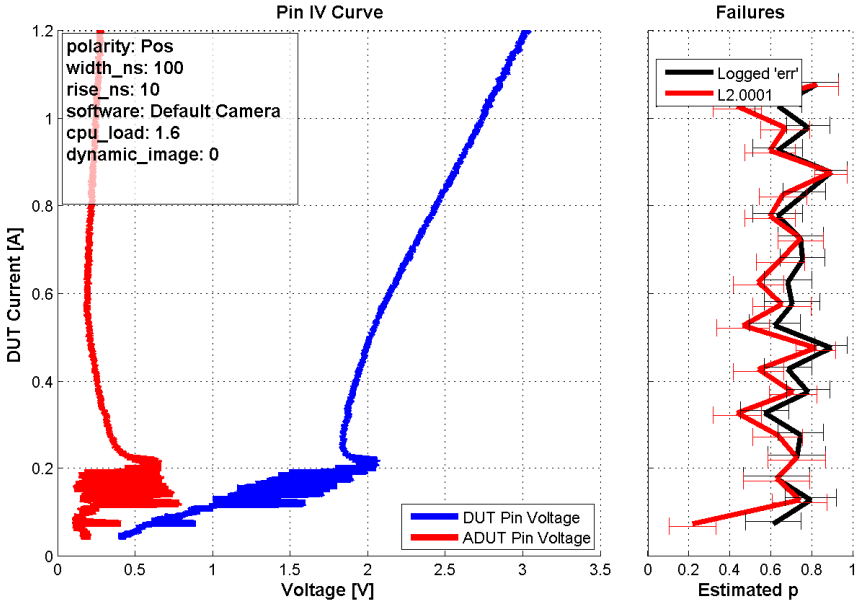


Figure A.31. CSIx_Cxx, positive pulse rise time test

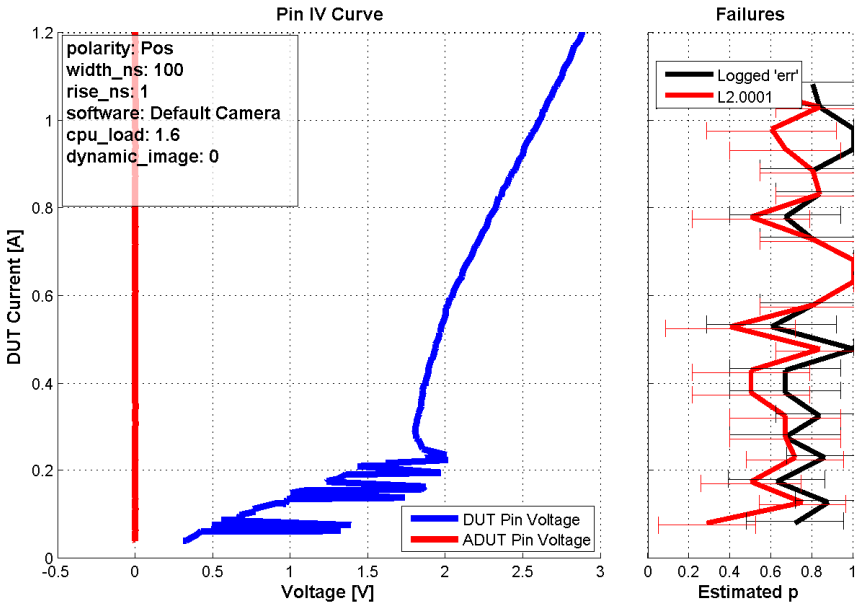


Figure A.32. CSIx_Cxx, positive pulse rise time test

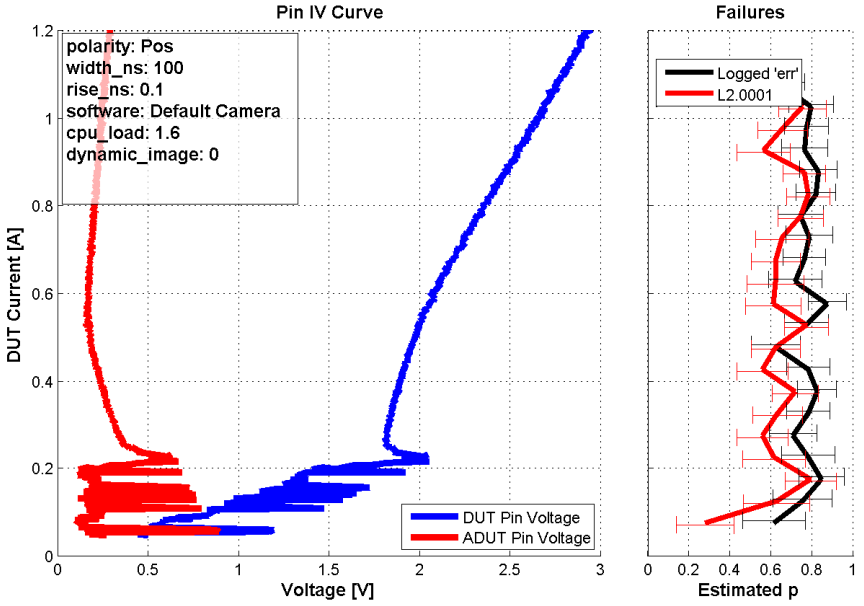


Figure A.33. CSIx_Cxx, positive pulse rise time test

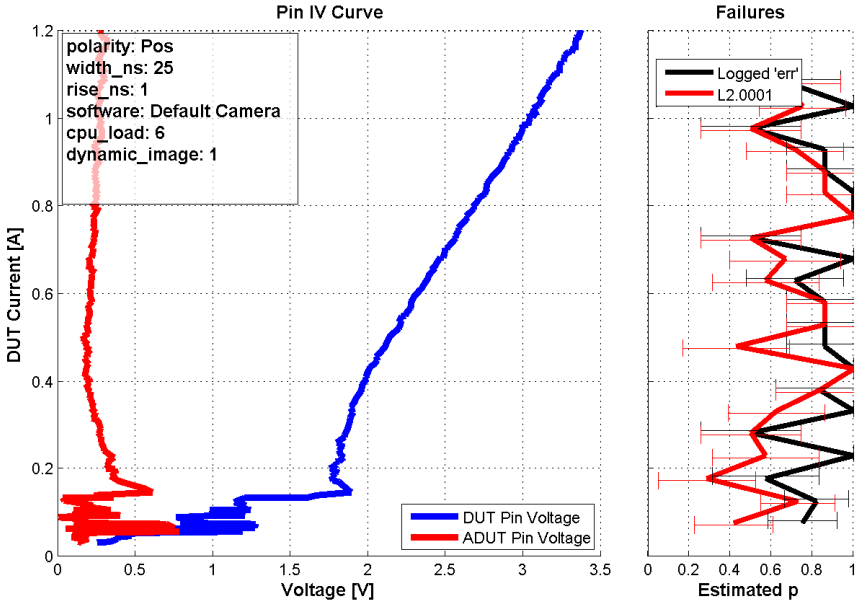


Figure A.34. CSIx_Cxx, positive average threadcount test

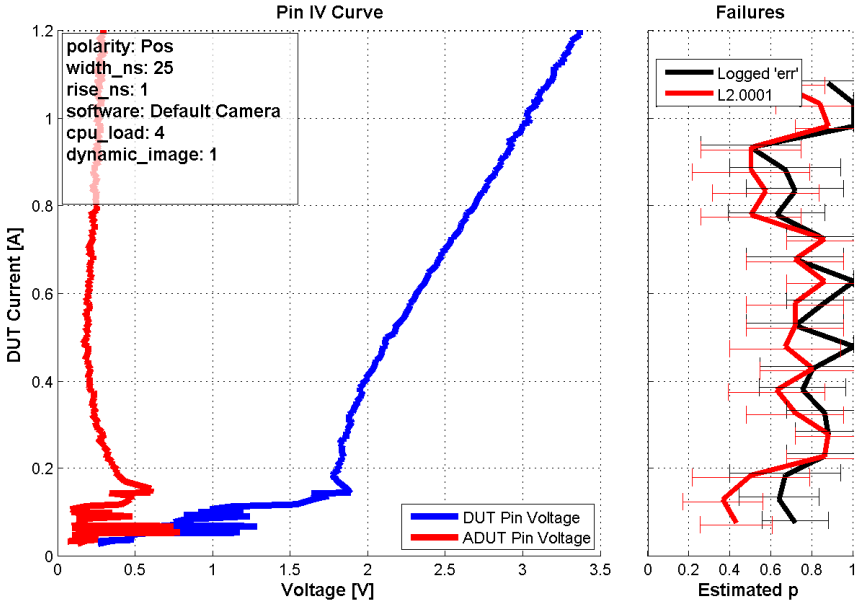


Figure A.35. CSIx_Cxx, positive average threadcount test

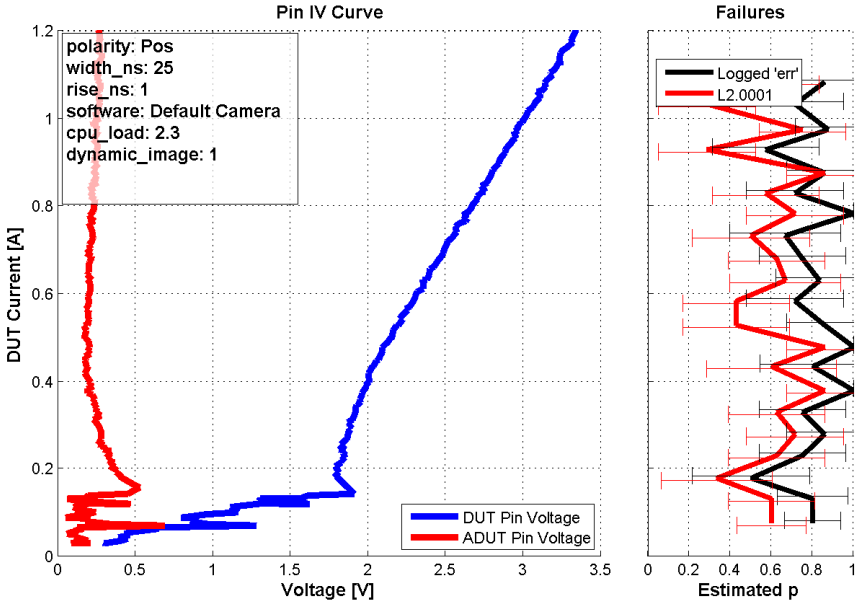


Figure A.36. CSIx_Cxx, positive average threadcount test

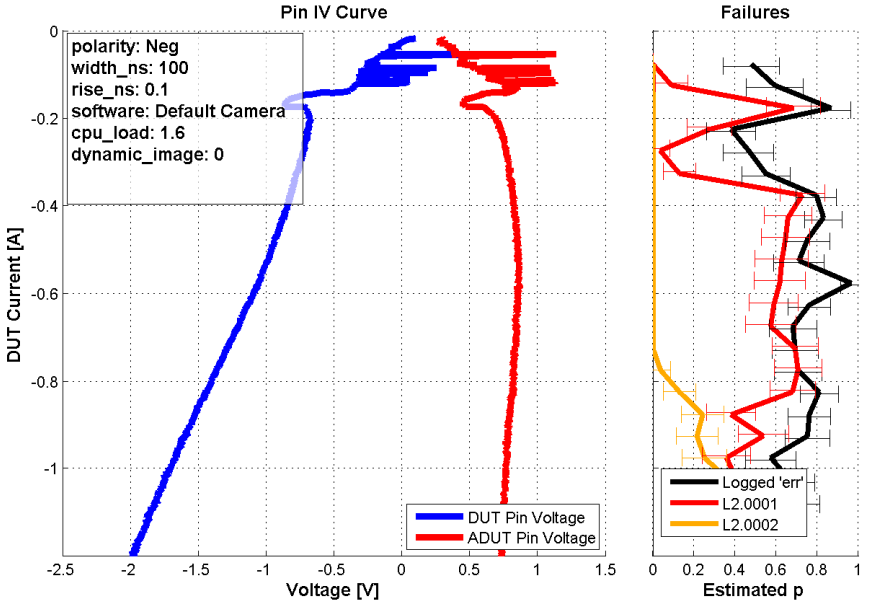


Figure A.37. CSIx_Cxx, negative pulse width test

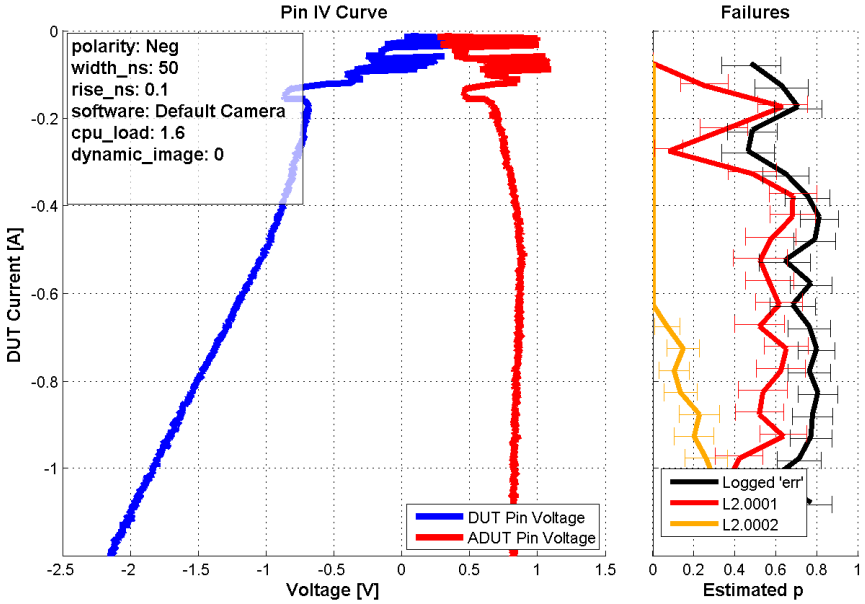


Figure A.38. CSIx_Cxx, negative pulse width test

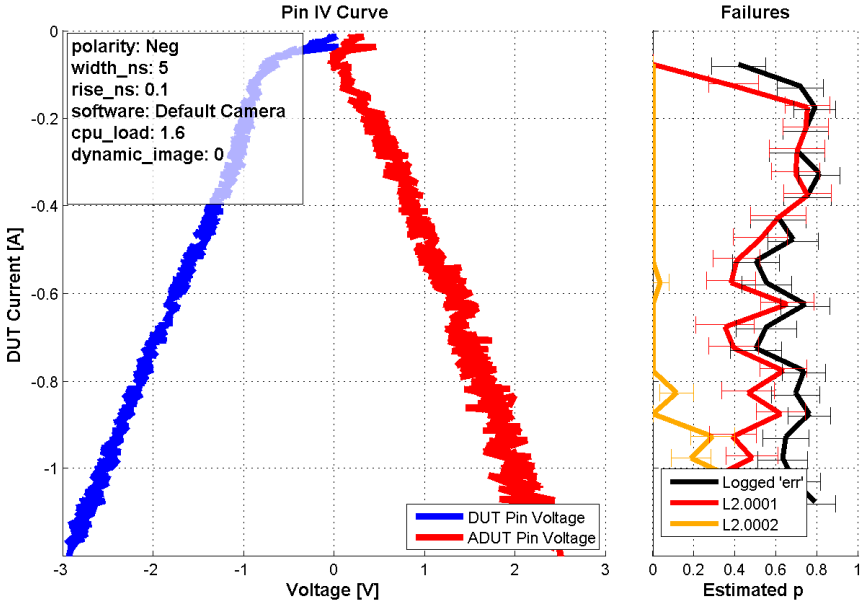


Figure A.39. CSIx_Cxx, negative pulse width test

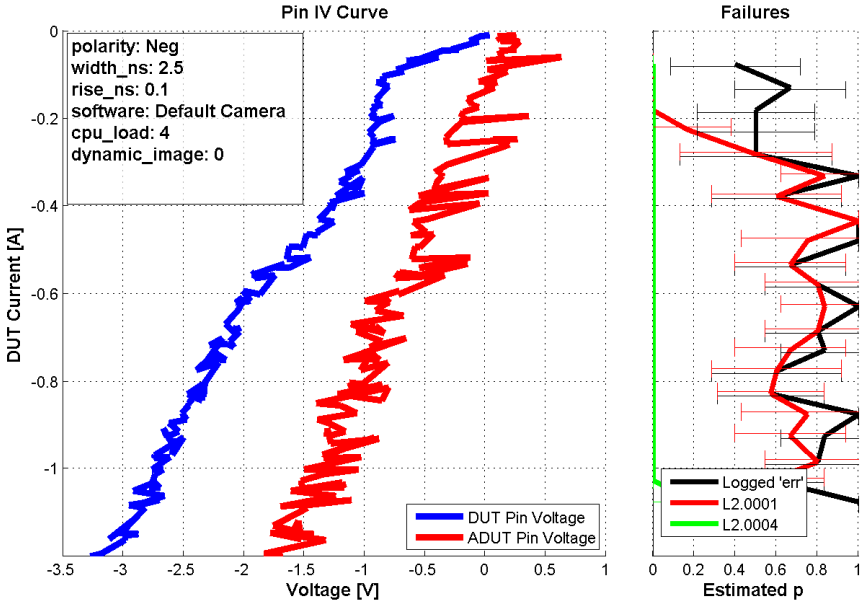


Figure A.40. CSIx_Cxx, negative pulse width test

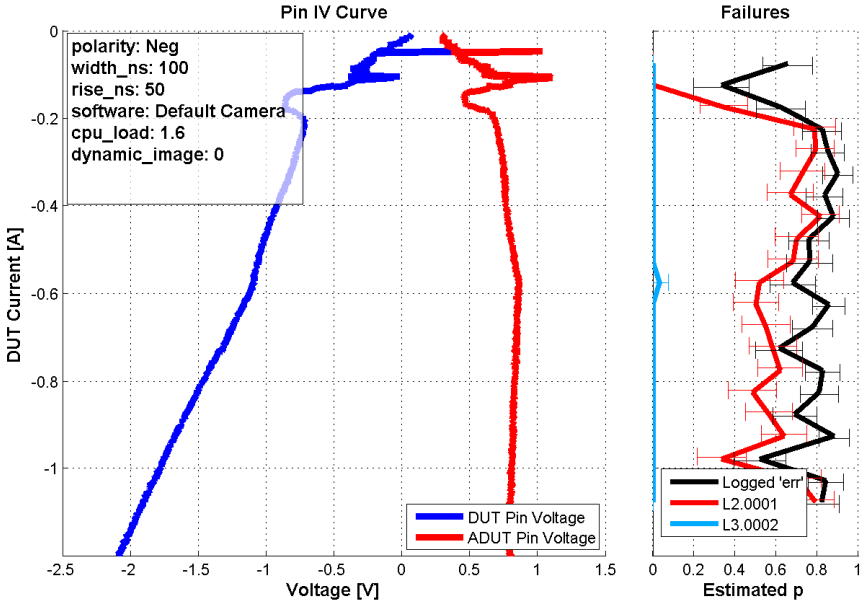


Figure A.41. CSIx_Cxx, negative pulse rise time test

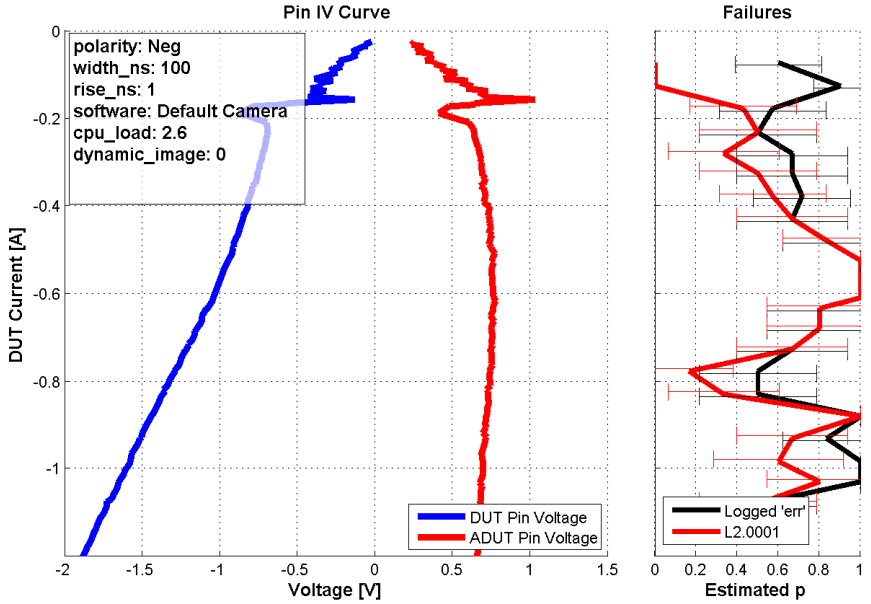


Figure A.42. CSIx_Cxx, negative pulse rise time test

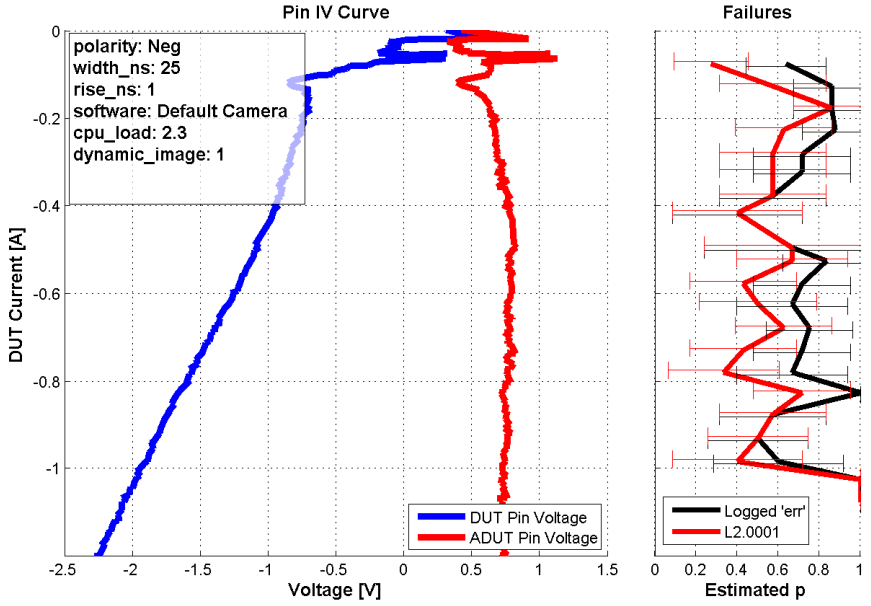


Figure A.43. CSIx_Cxx, negative pulse rise time test

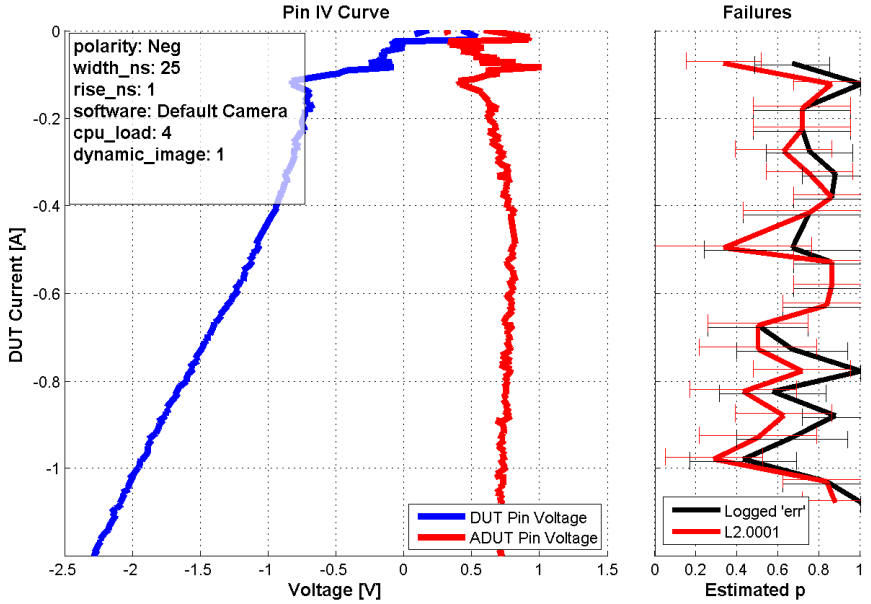


Figure A.44. CSIx_Cxx, negative pulse rise time test

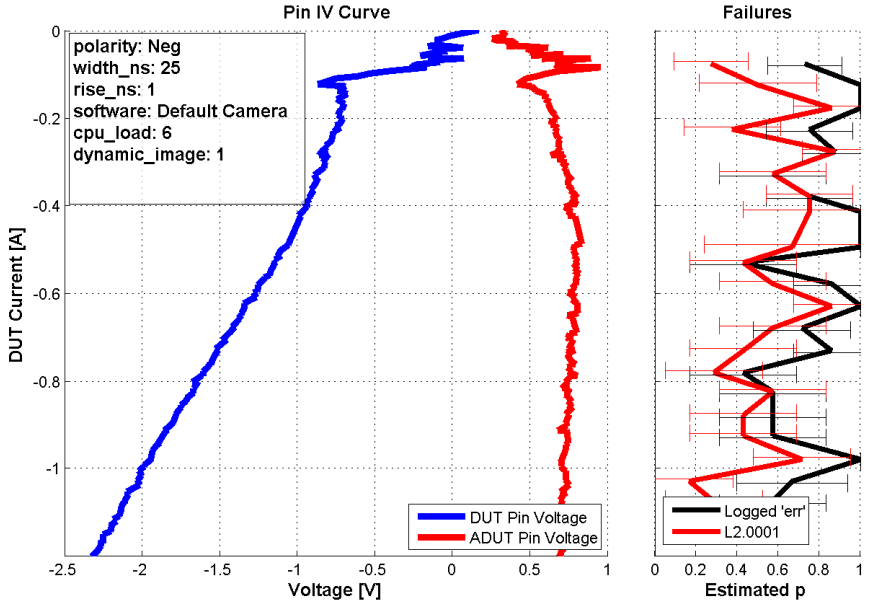


Figure A.45. CSIx_Cxx, negative pulse rise time test

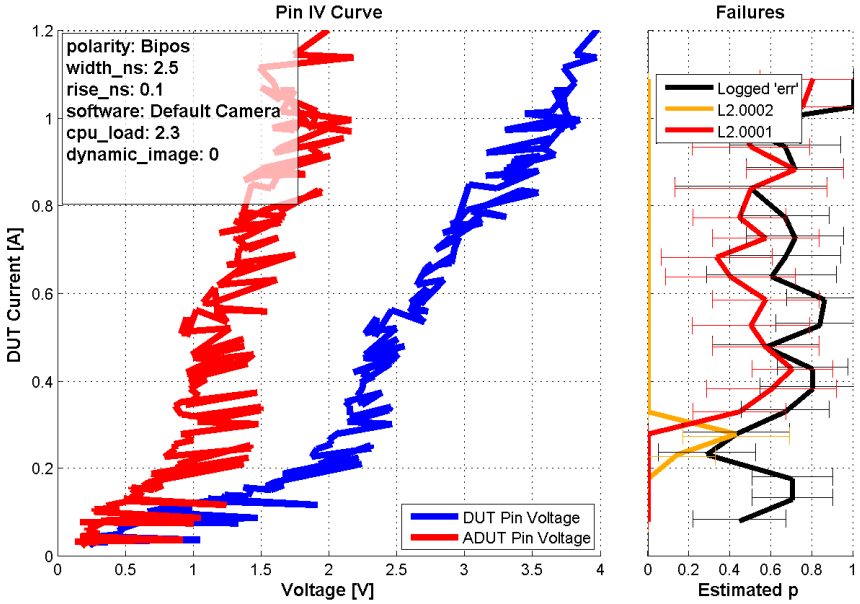


Figure A.46. CSIx_Cxx, bipolar test

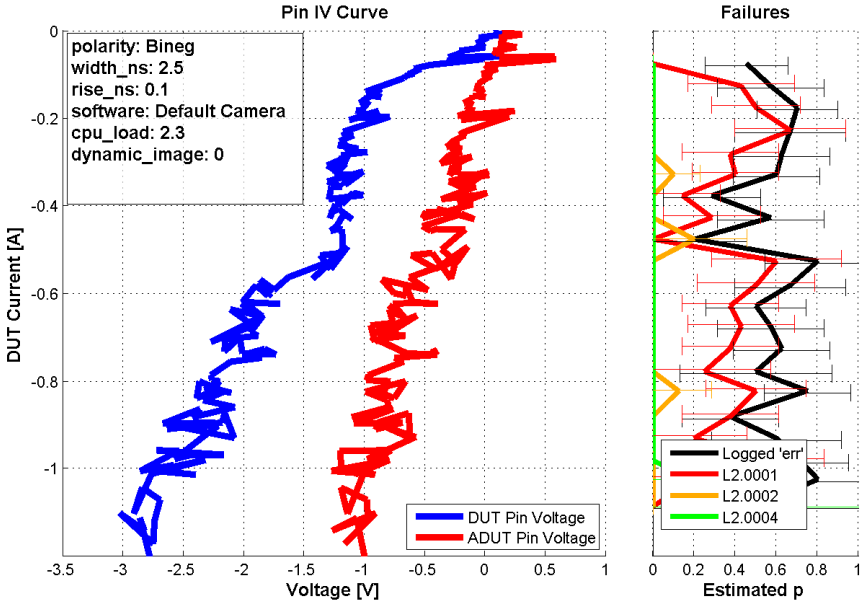


Figure A.47. CSIx_Cxx, bipolar test

APPENDIX B

SENSOR PIN (I2CX) CHARACTERIZATION MEASUREMENT RESULTS

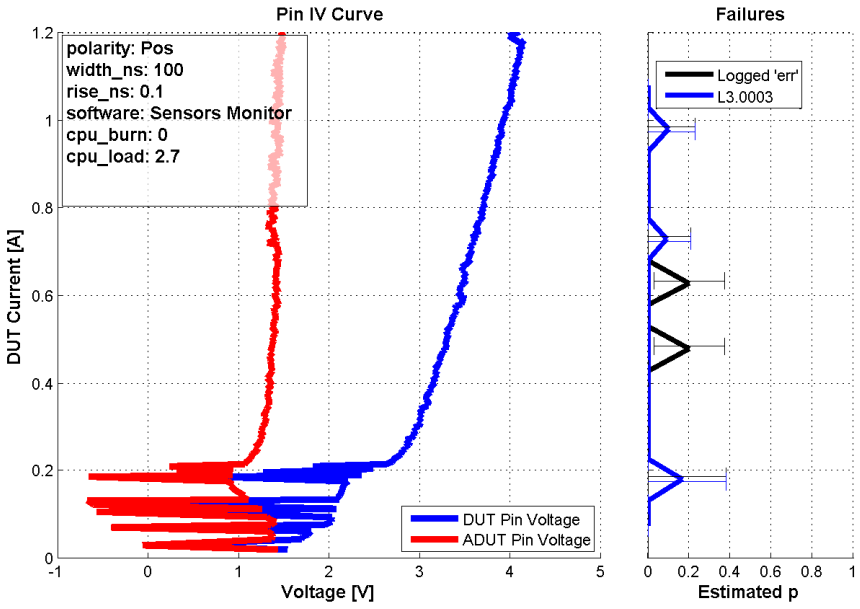


Figure B.1. I2Cx_SCL, positive pulse width test

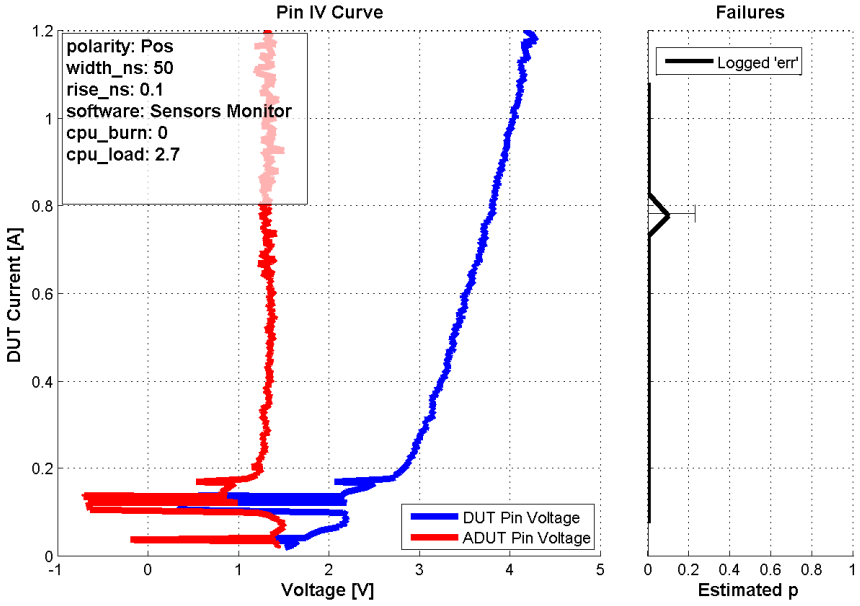


Figure B.2. I2Cx_SCL, positive pulse width test

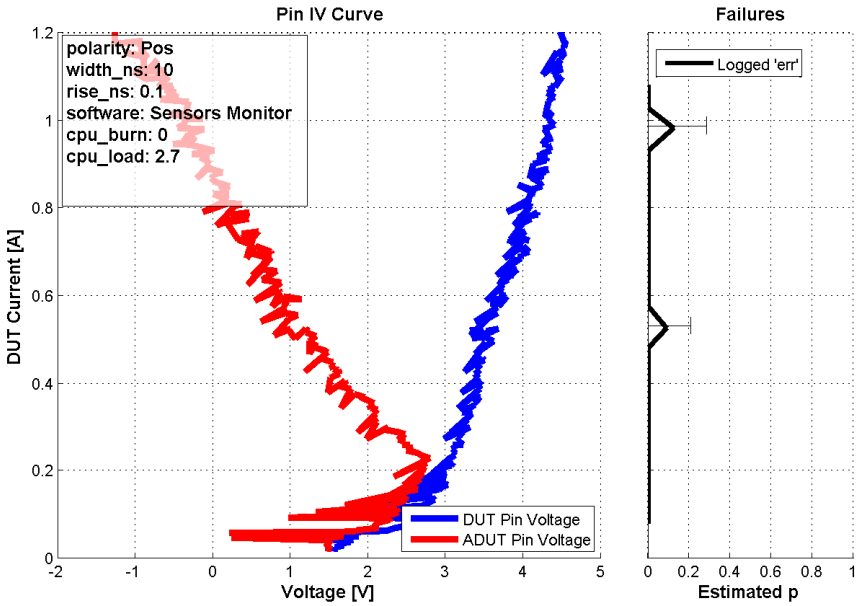


Figure B.3. I2Cx_SCL, positive pulse width test

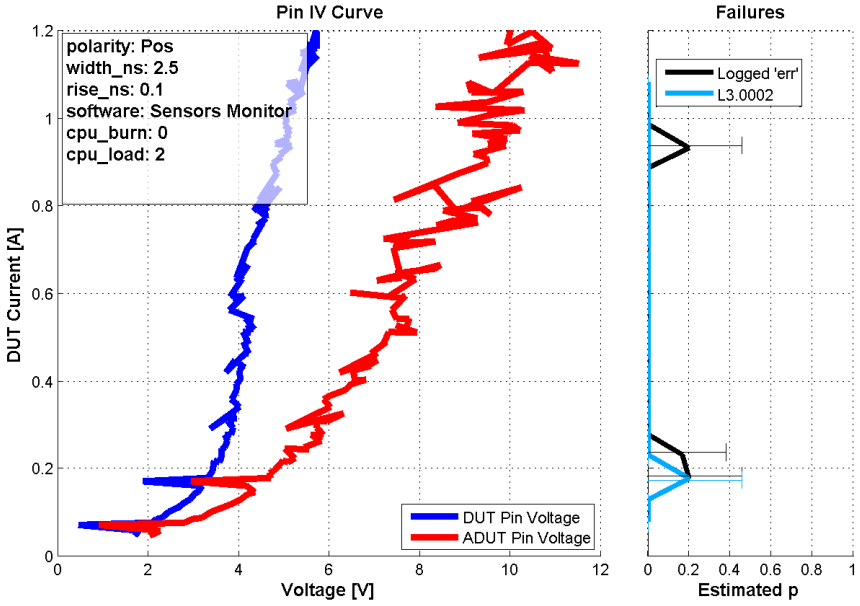


Figure B.4. I2Cx_SCL, positive pulse width test

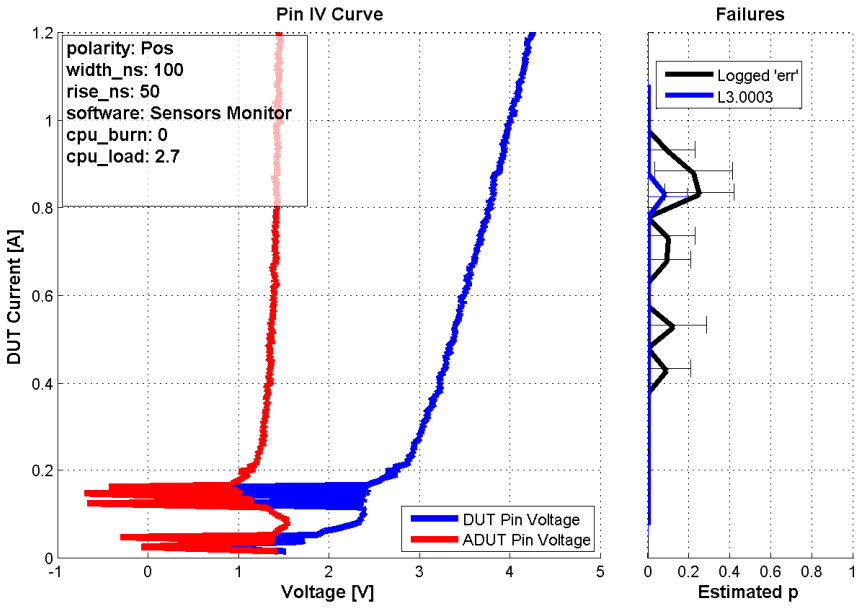


Figure B.5. I2Cx_SCL, positive pulse rise time test

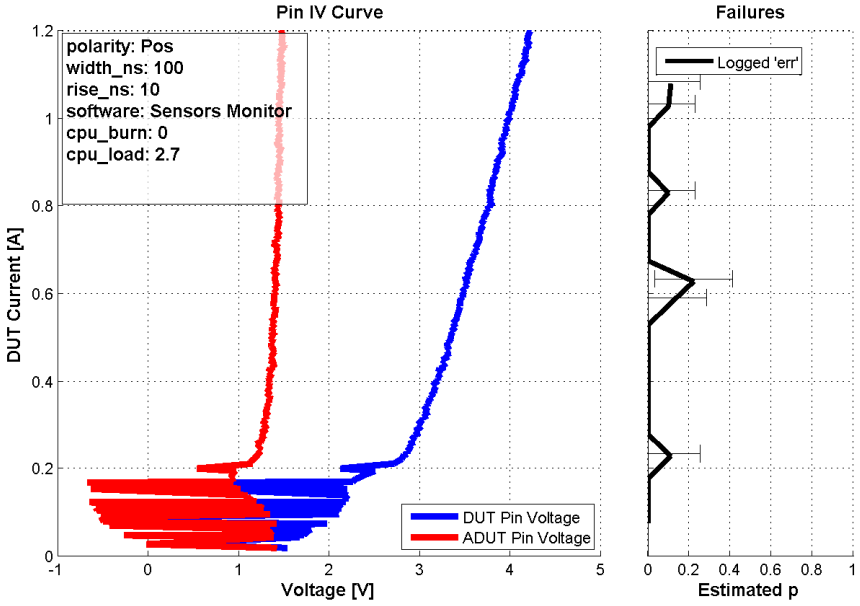


Figure B.6. I2Cx_SCL, positive pulse rise time test

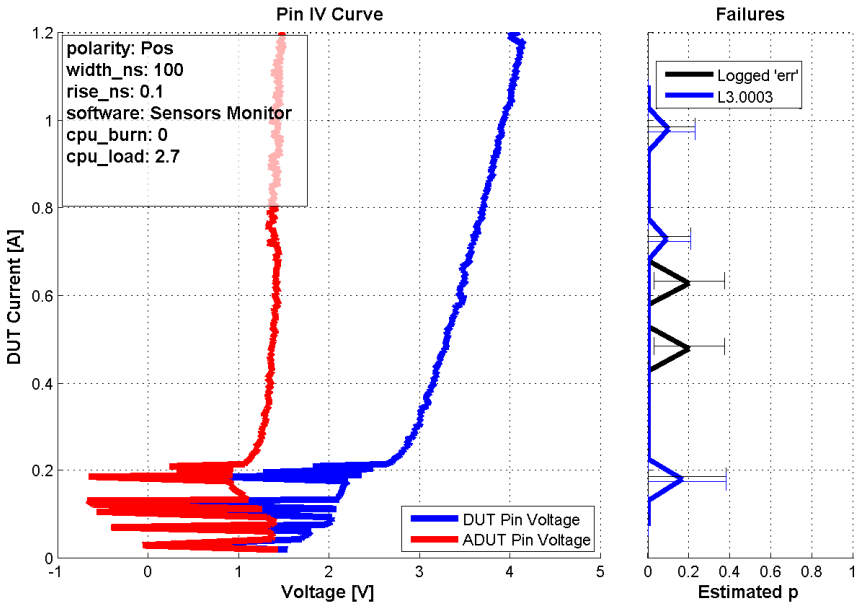


Figure B.7. I2Cx_SCL, positive pulse rise time test

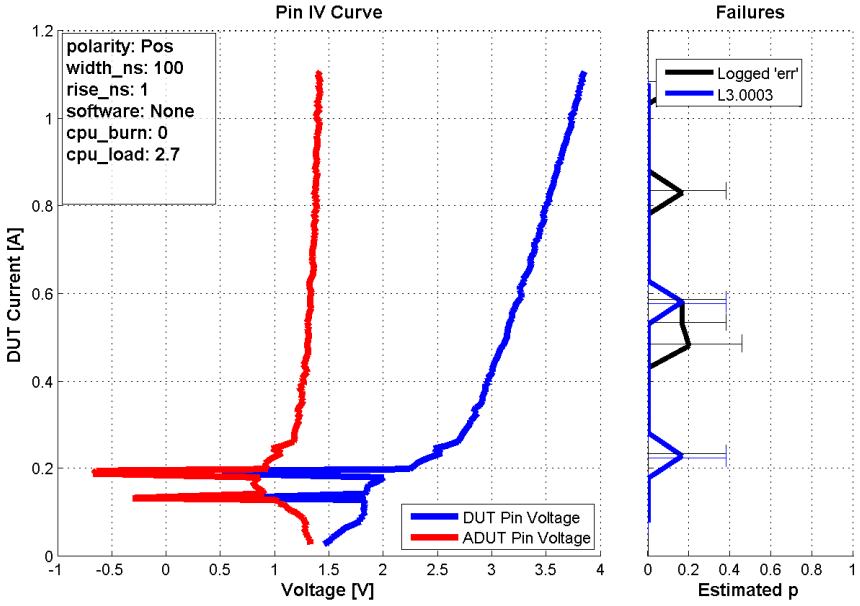


Figure B.8. I2Cx_SCL, positive average threadcount test

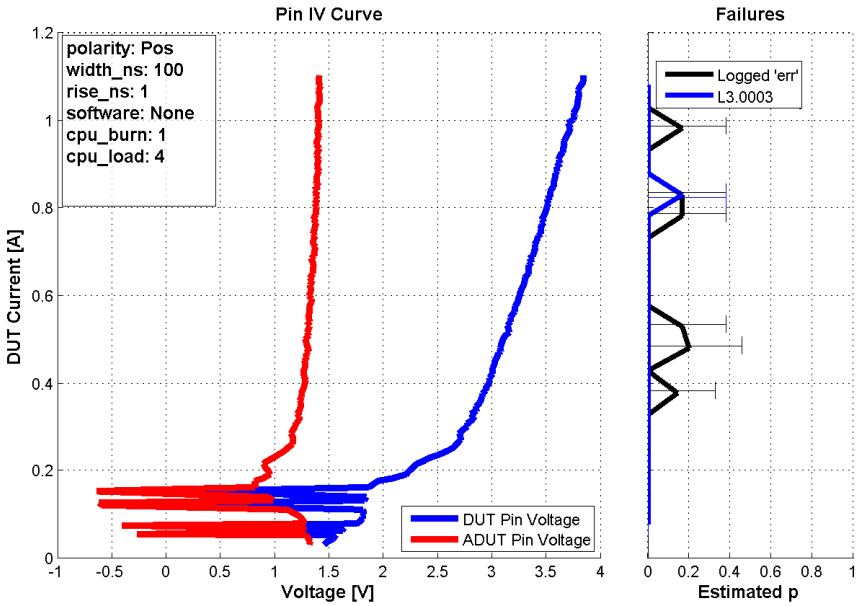


Figure B.9. I2Cx_SCL, positive average threadcount test

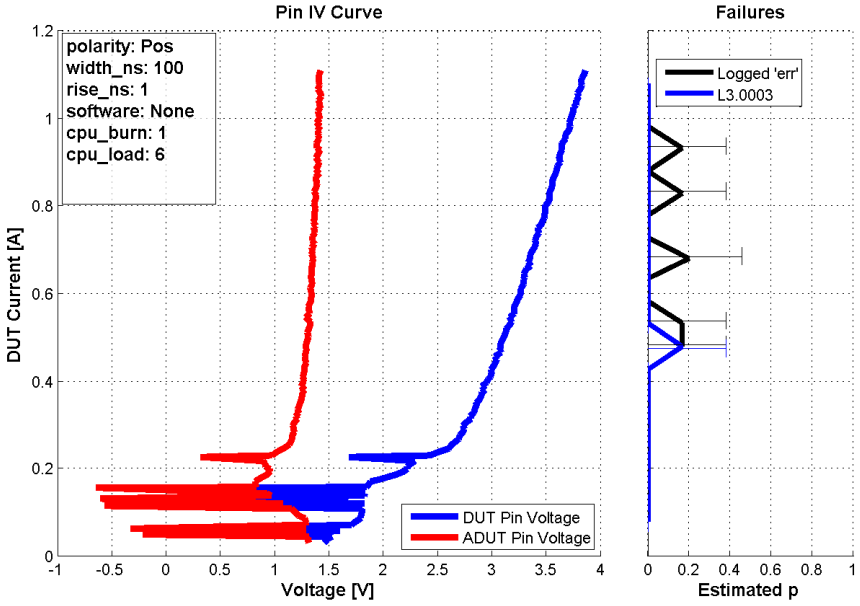


Figure B.10. I2Cx_SCL, positive average threadcount test

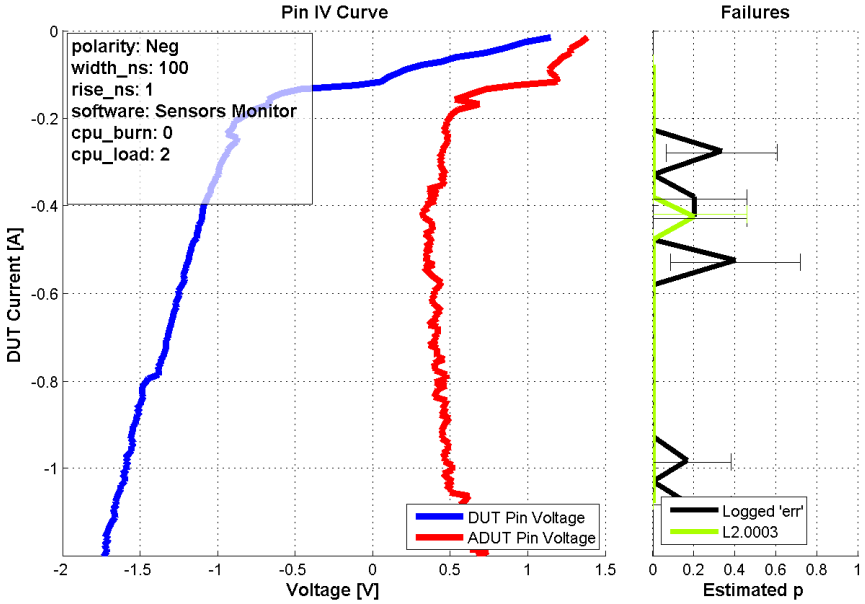


Figure B.11. I2Cx_SCL, negative pulse width test

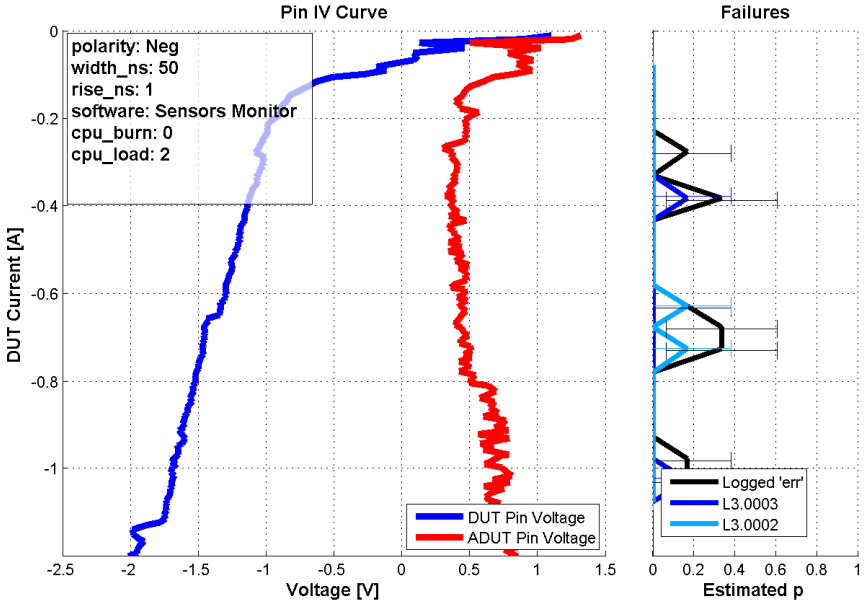


Figure B.12. I2Cx_SCL, negative pulse width test

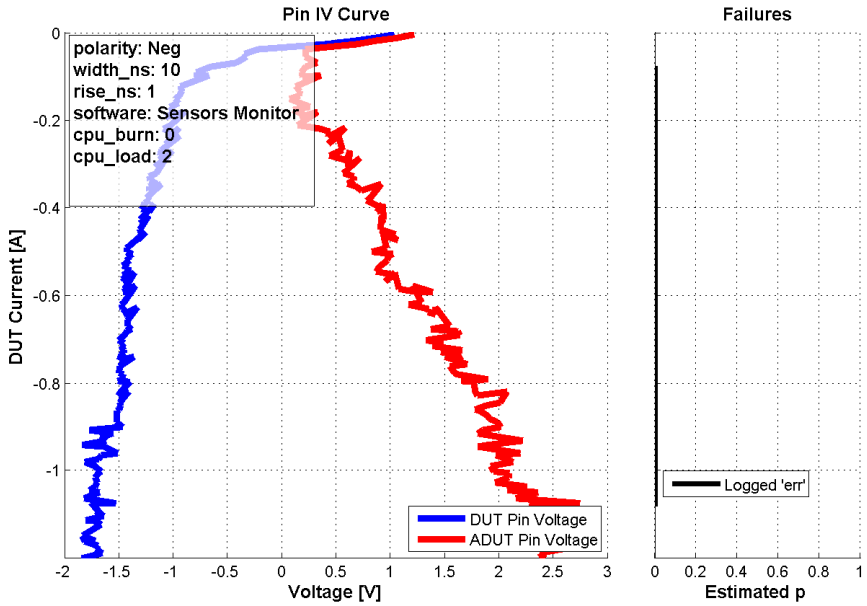


Figure B.13. I2Cx_SCL, negative pulse width test

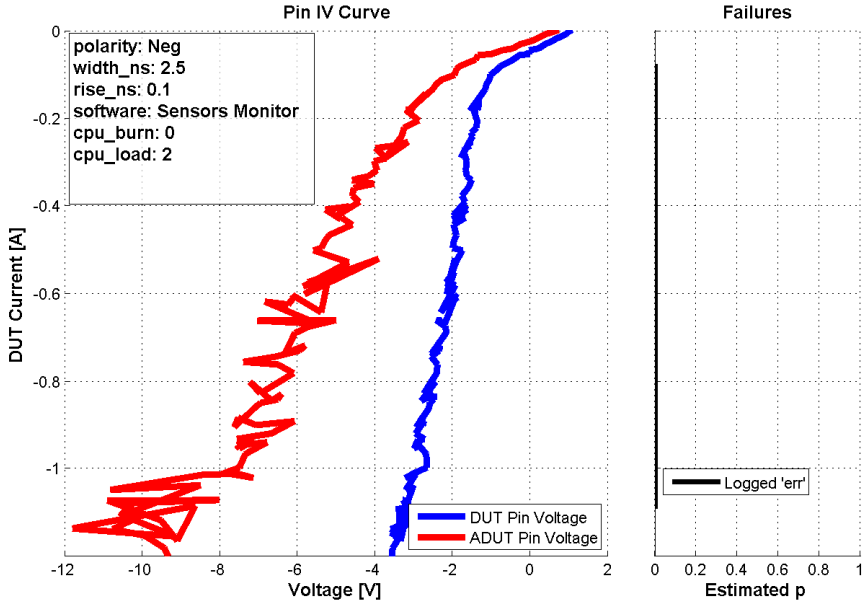


Figure B.14. I2Cx_SCL, negative pulse width test

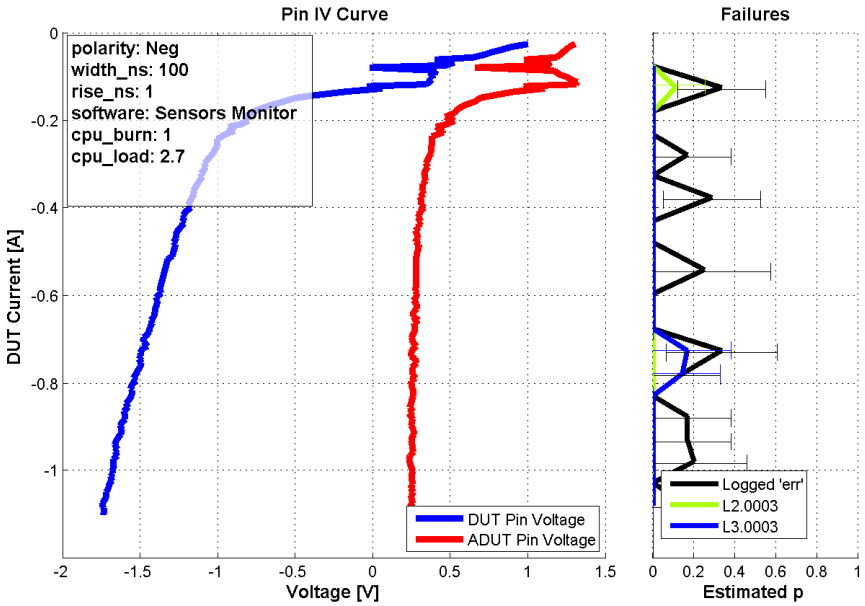


Figure B.15. I2Cx_SCL, negative average threadcount test

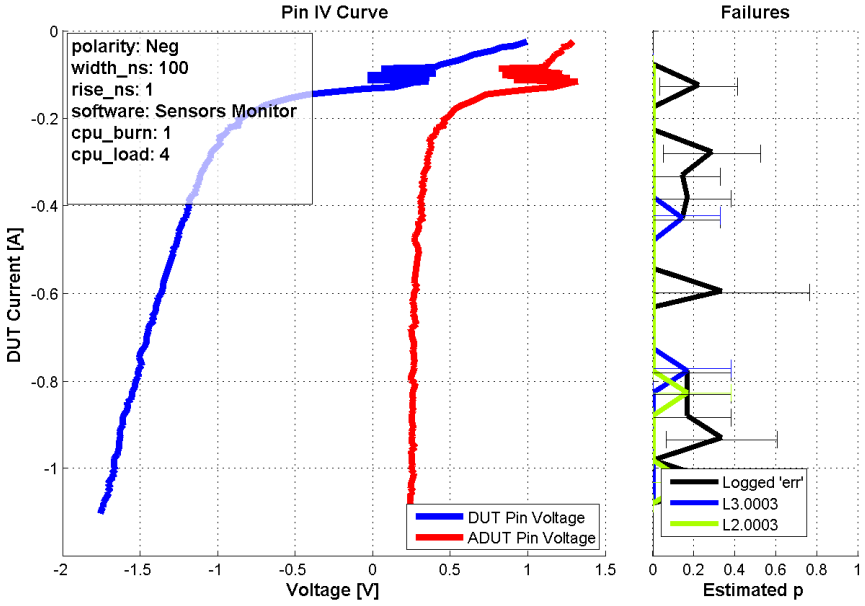


Figure B.16. I2Cx_SCL, negative average threadcount test

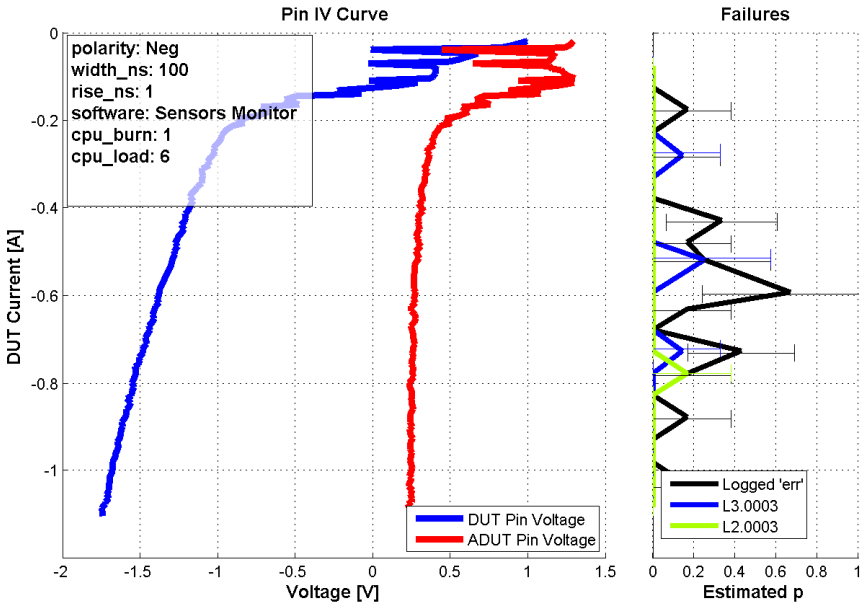


Figure B.17. I2Cx_SCL, negative average threadcount test

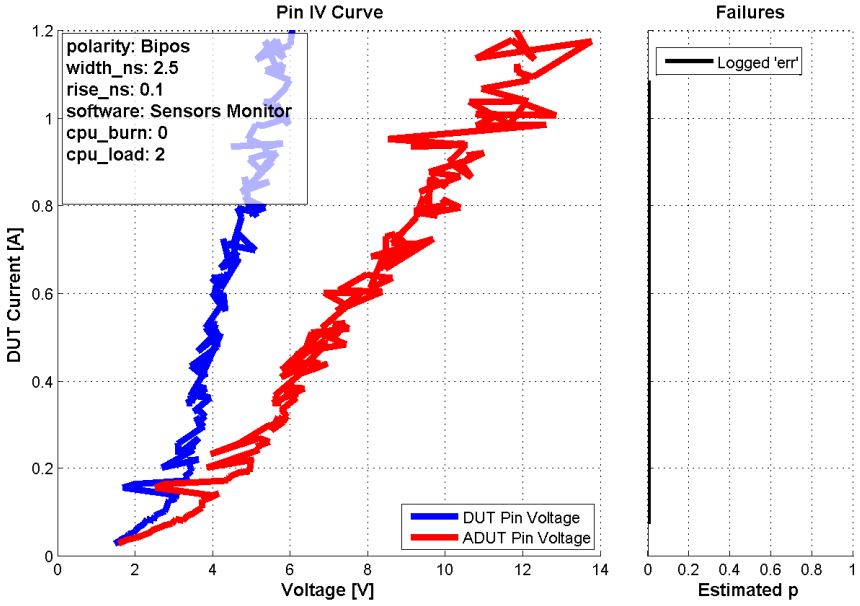


Figure B.18. I2Cx_SCL, bipolar test

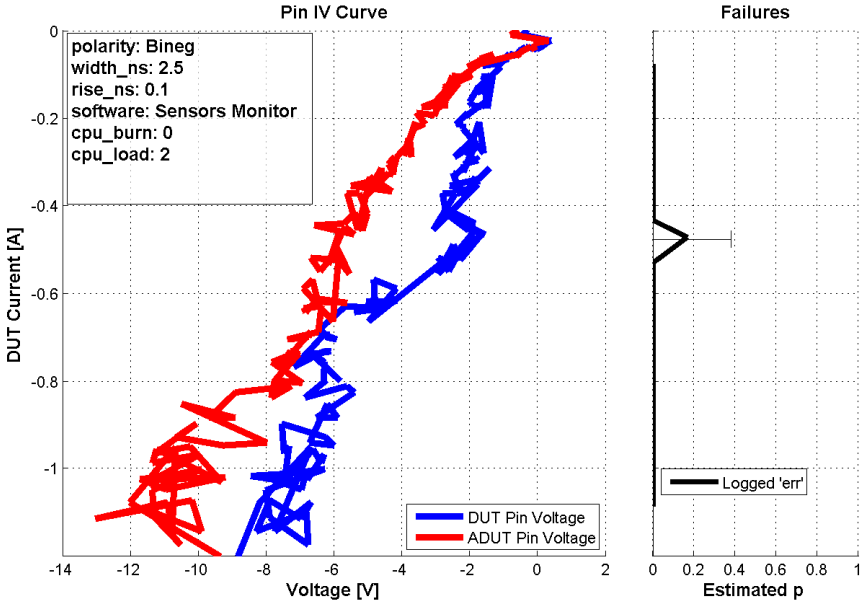


Figure B.19. I2Cx_SCL, bipolar test

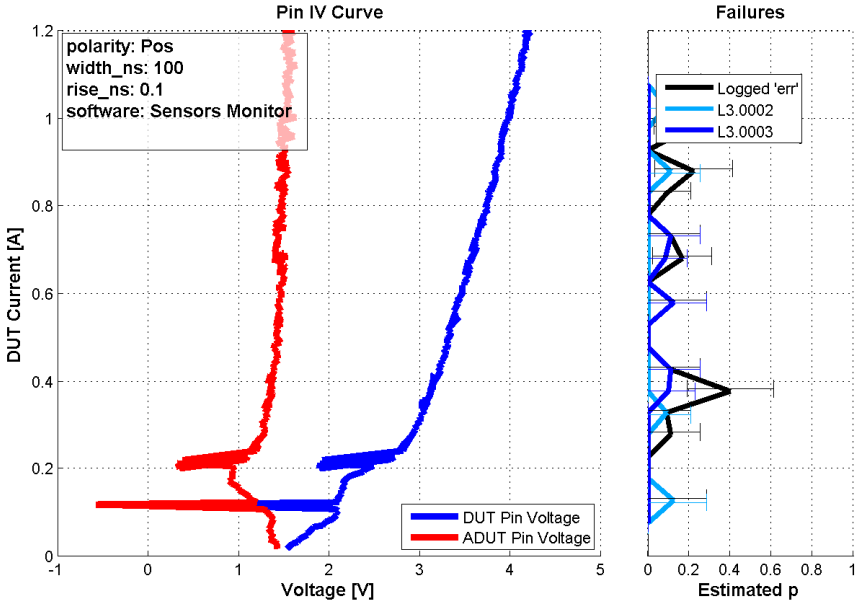


Figure B.20. I2Cx_SDA, positive pulse width test

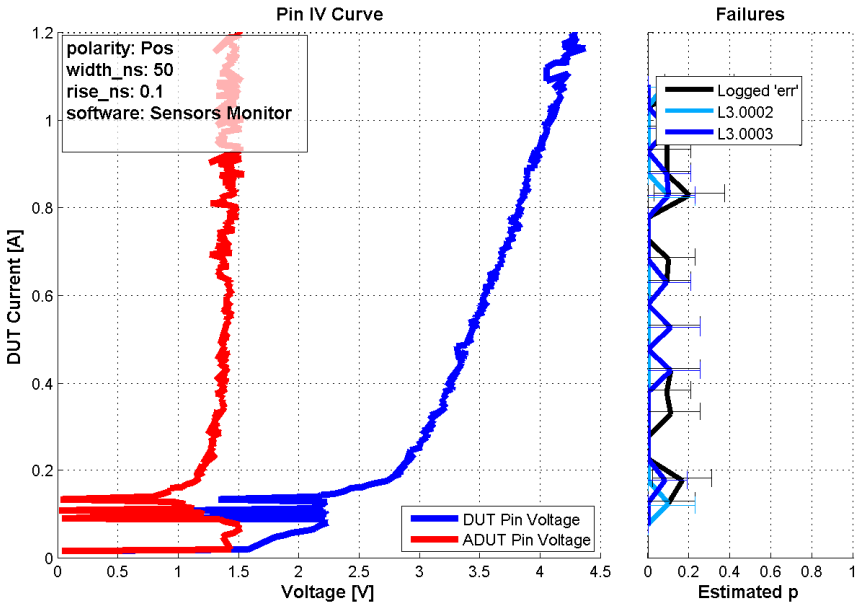


Figure B.21. I2Cx_SDA, positive pulse width test

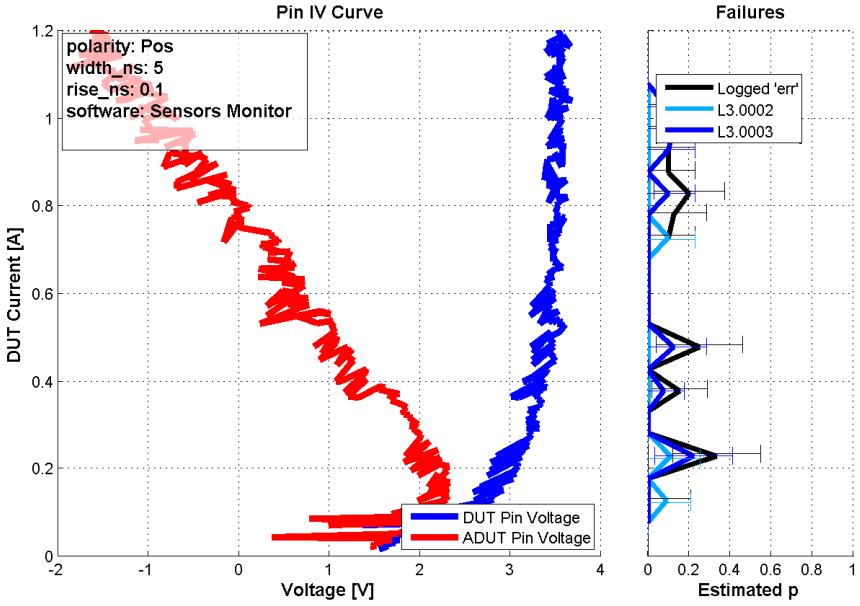


Figure B.22. I2Cx_SDA, positive pulse width test

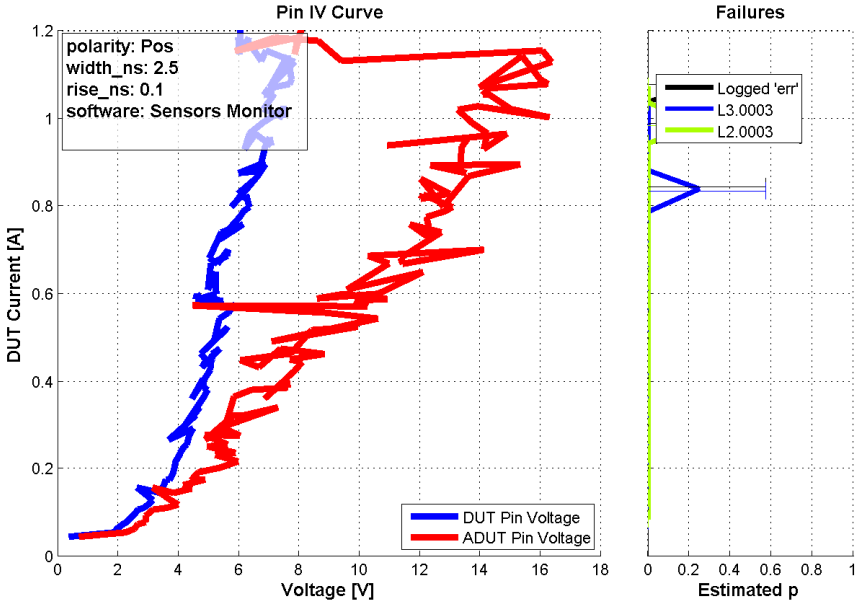


Figure B.23. I2Cx_SDA, positive pulse width test

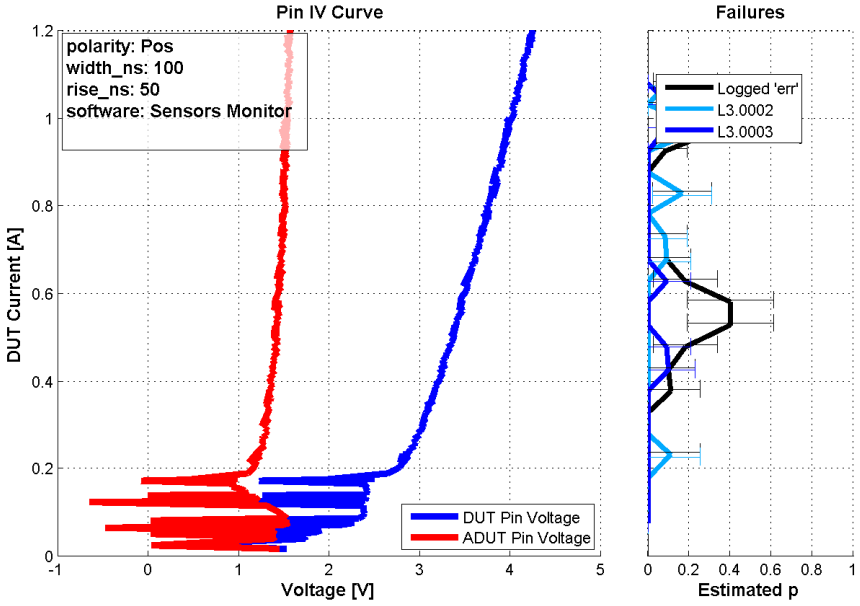


Figure B.24. I2Cx_SDA, positive pulse rise time test

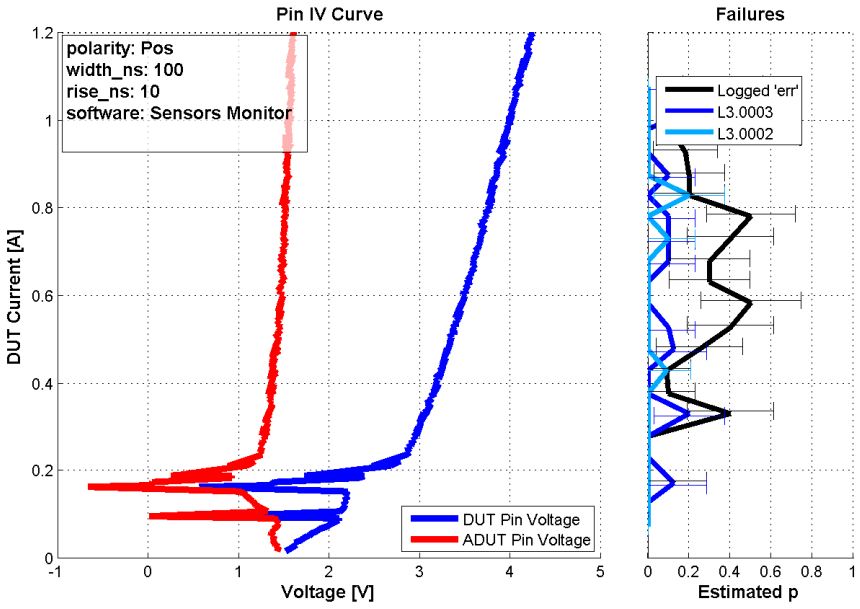


Figure B.25. I2Cx_SDA, positive pulse rise time test

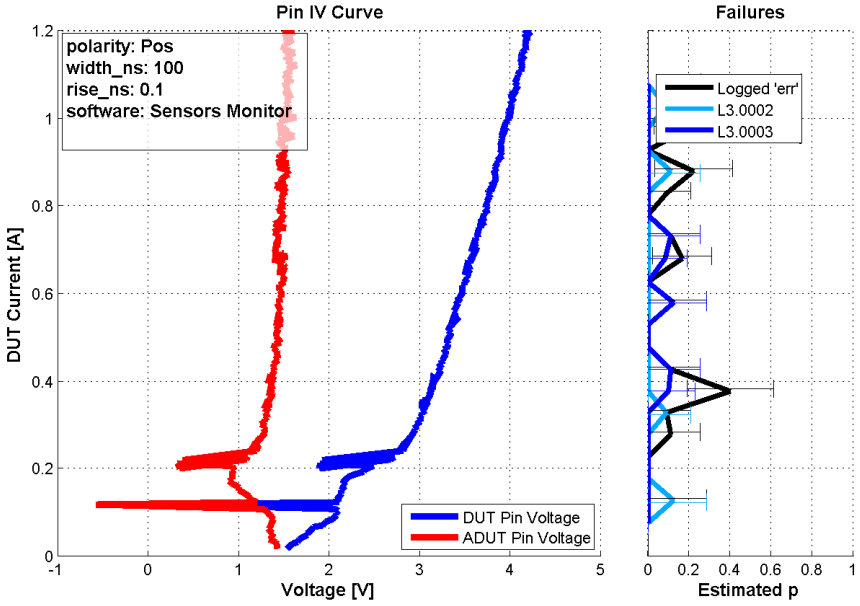


Figure B.26. I2Cx_SDA, positive pulse rise time test

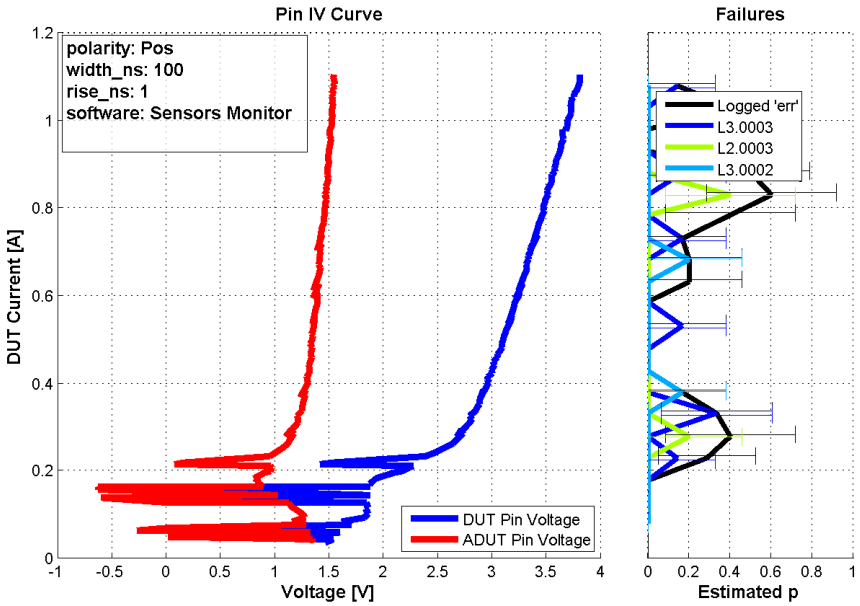


Figure B.27. I2Cx_SDA, positive average threadcount test

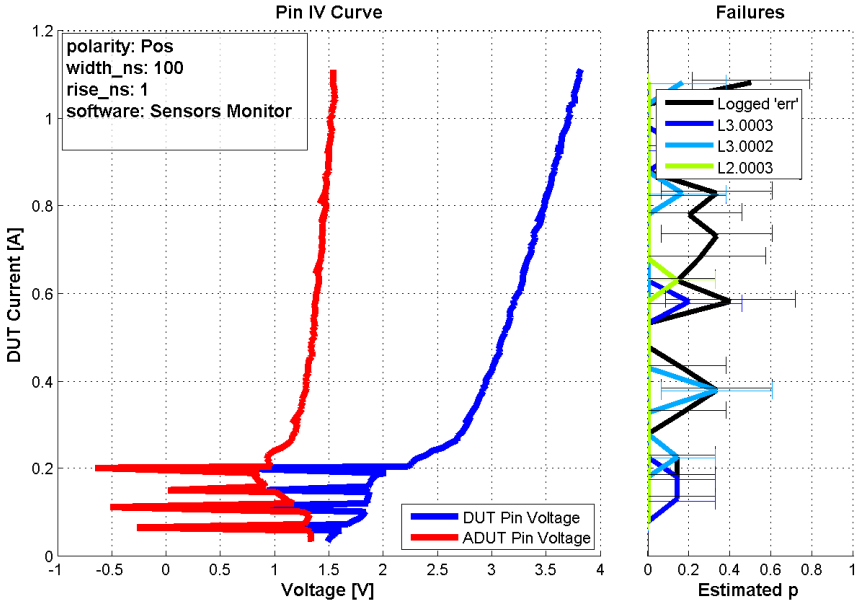


Figure B.28. I2Cx_SDA, positive average threadcount test

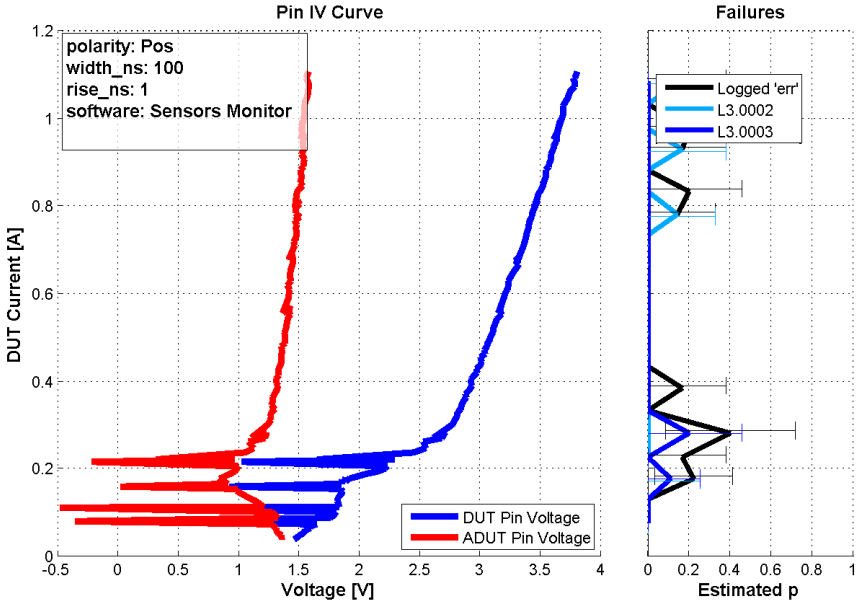


Figure B.29. I2Cx_SDA, positive average threadcount test

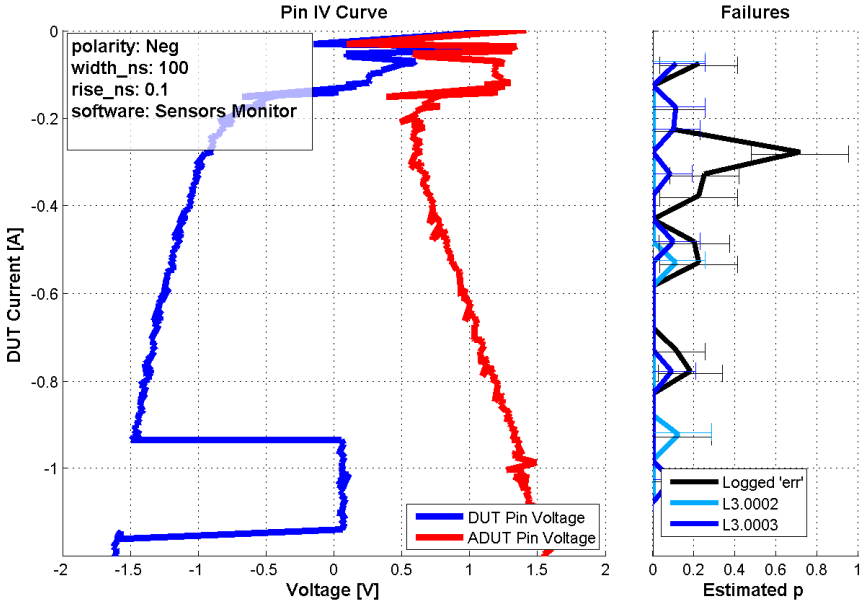


Figure B.30. I2Cx_SDA, negative pulse width test

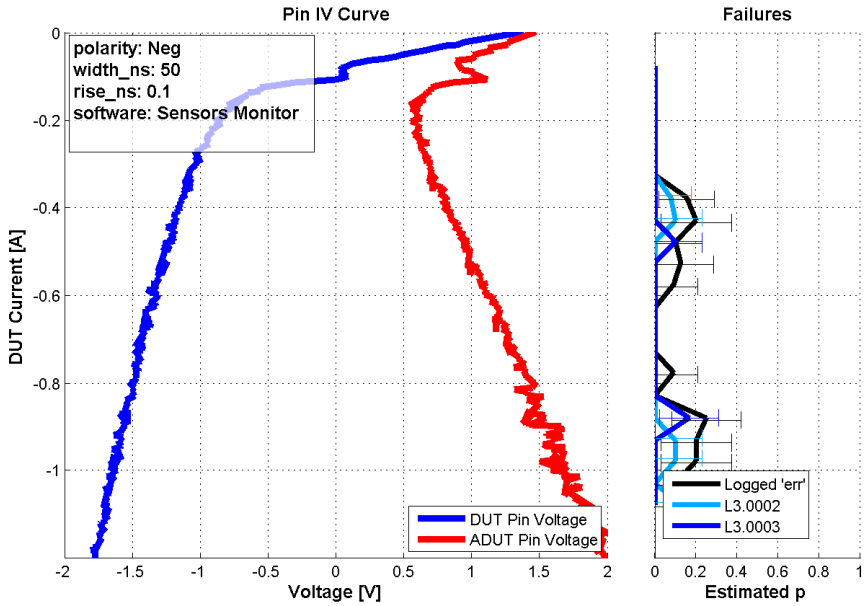


Figure B.31. I2Cx_SDA, negative pulse width test

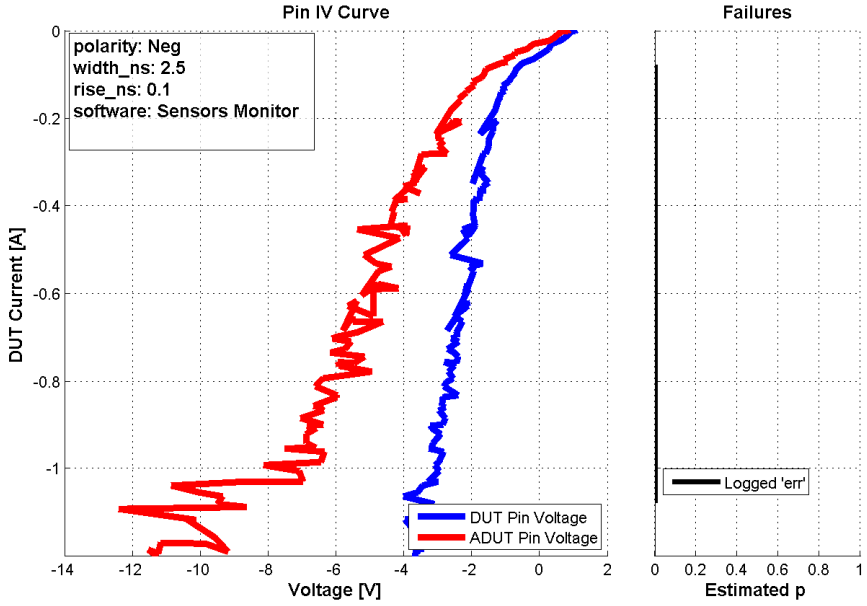


Figure B.32. I2Cx_SDA, negative pulse width test

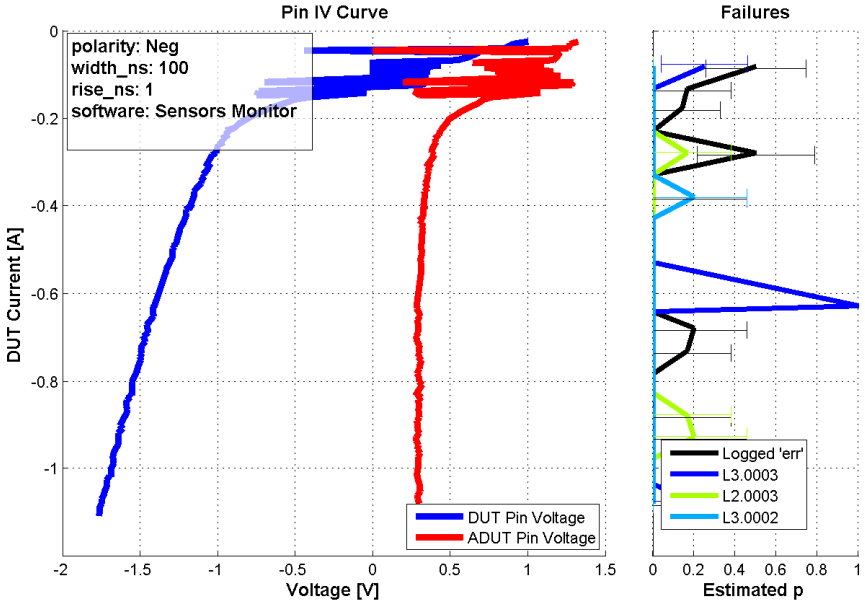


Figure B.33. I2Cx_SDA, negative average threadcount test

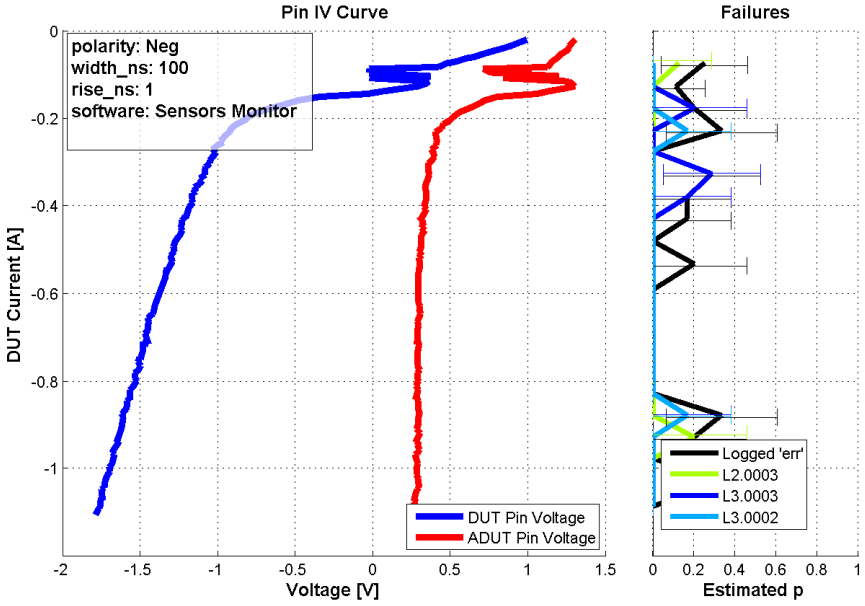


Figure B.34. I2Cx_SDA, negative average threadcount test

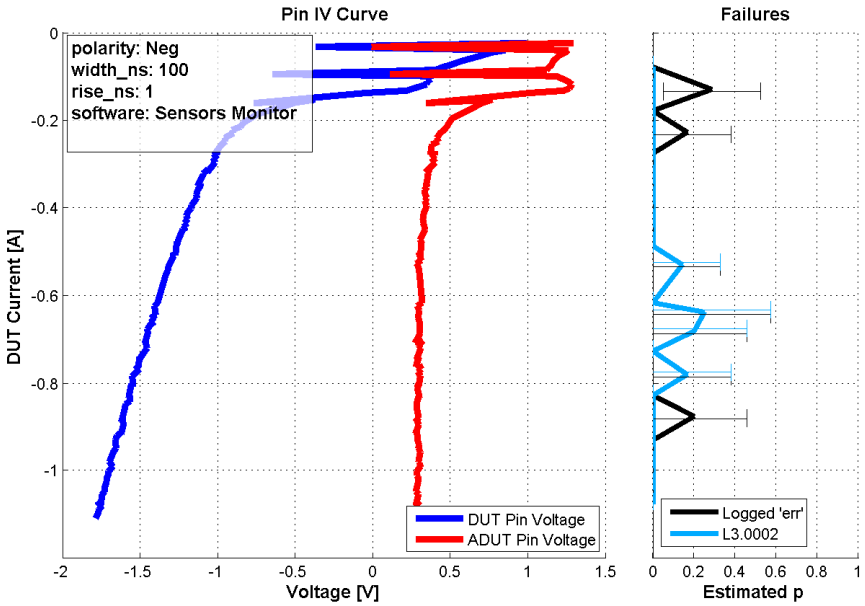


Figure B.35. I2Cx_SDA, negative average threadcount test

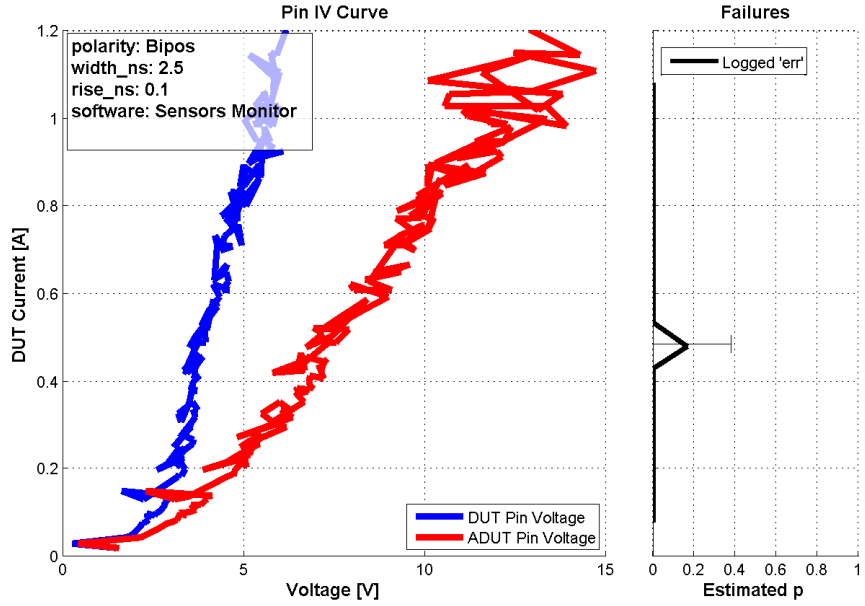


Figure B.36. I2Cx_SDA, bipolar test

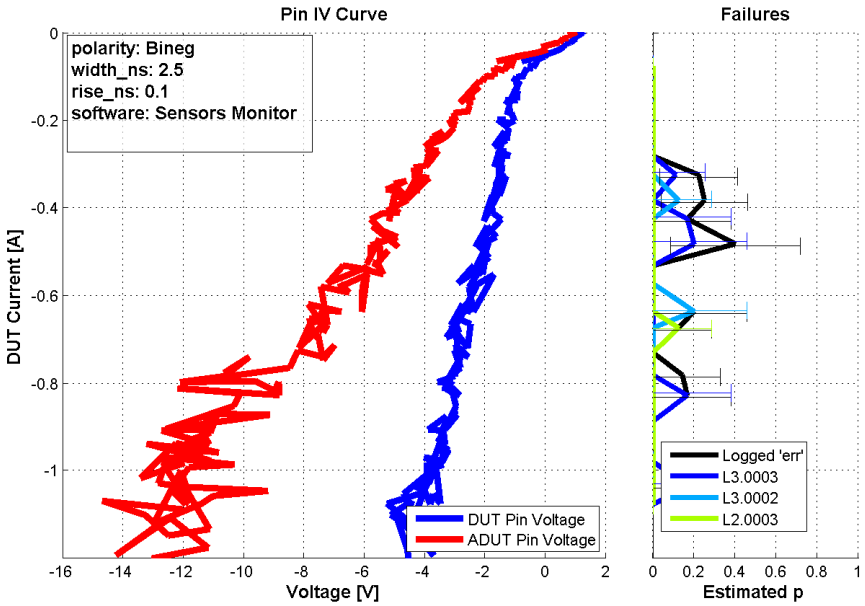


Figure B.37. I2Cx_SDA, bipolar test

APPENDIX C

USB 3.0 (USB3) CHARACTERIZATION MEASUREMENT RESULTS

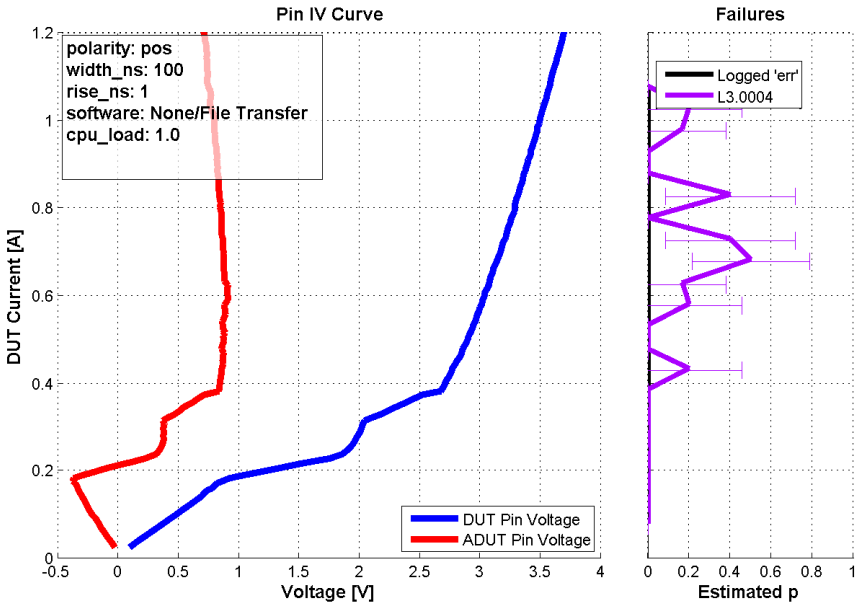


Figure C.1. USB3_Rxx, positive pulse width test

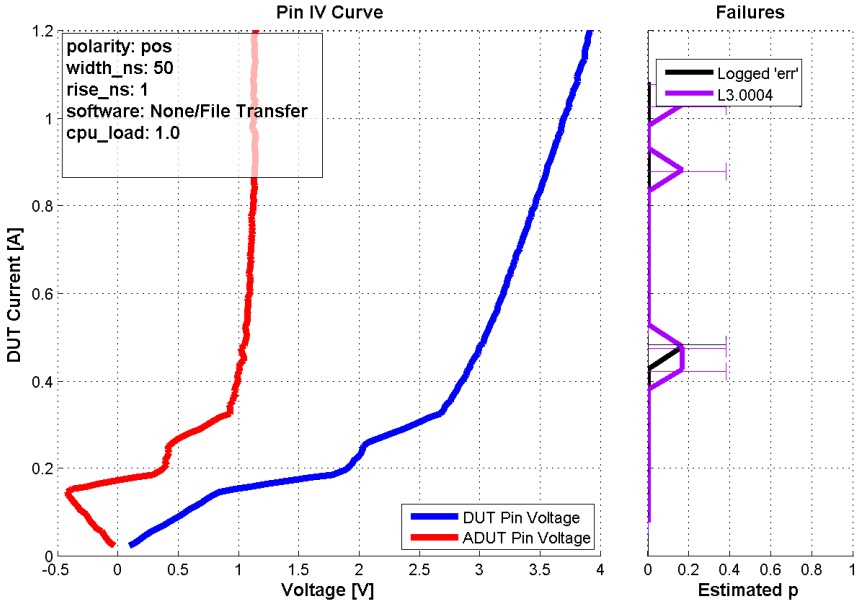


Figure C.2. USB3_Rxx, positive pulse width test

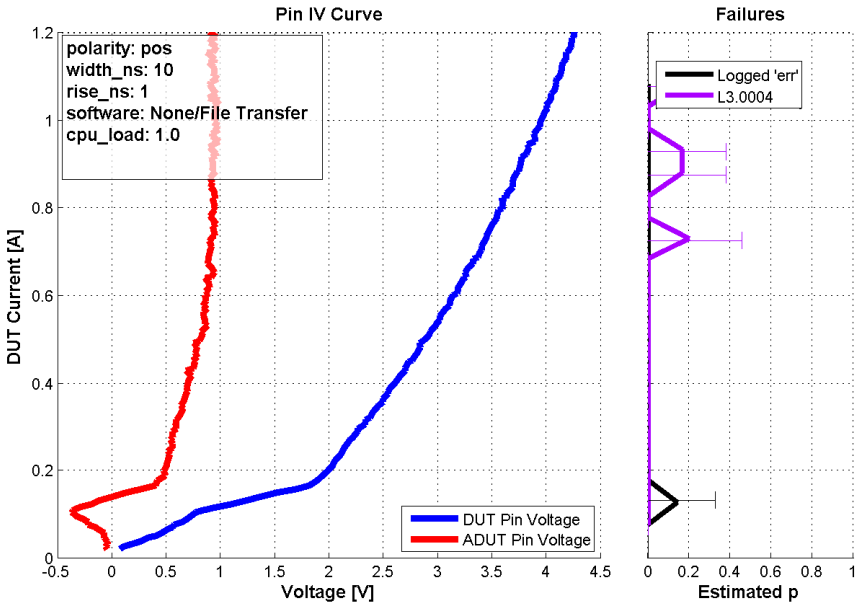


Figure C.3. USB3_Rxx, positive pulse width test

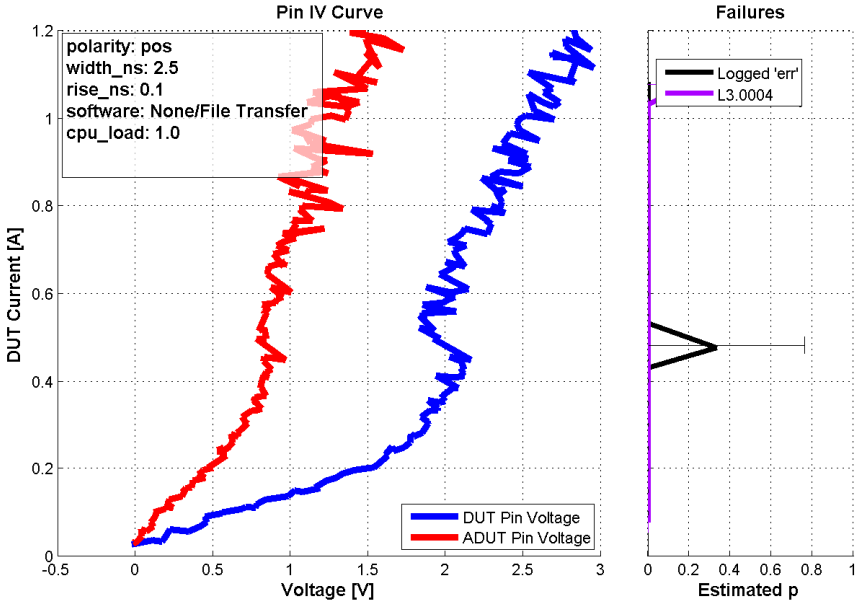


Figure C.4. USB3_Rxx, positive pulse width test

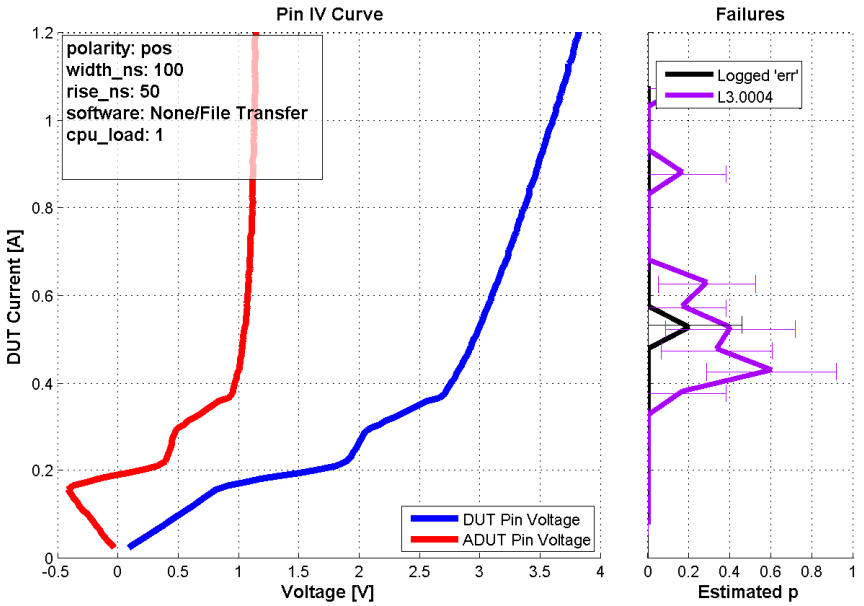


Figure C.5. USB3_Rxx, positive pulse rise time test

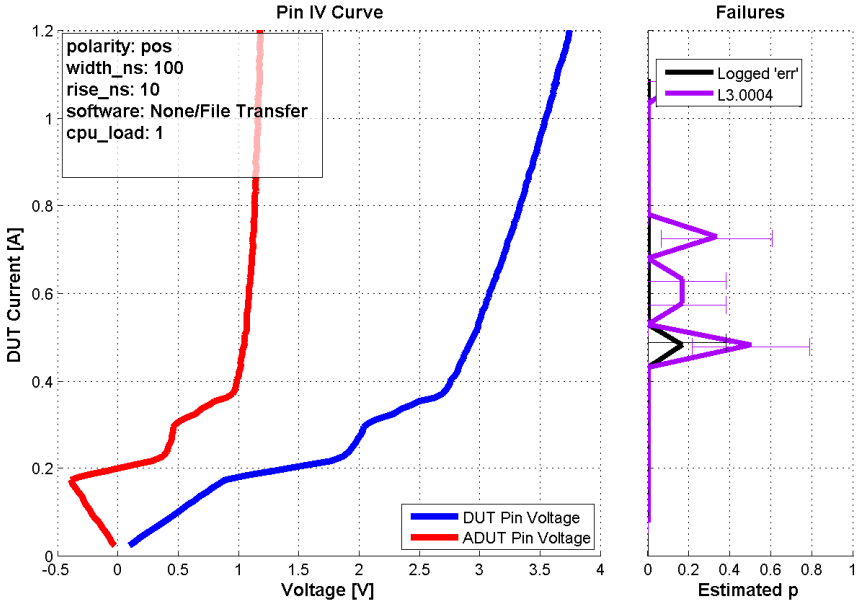


Figure C.6. USB3_Rxx, positive pulse rise time test

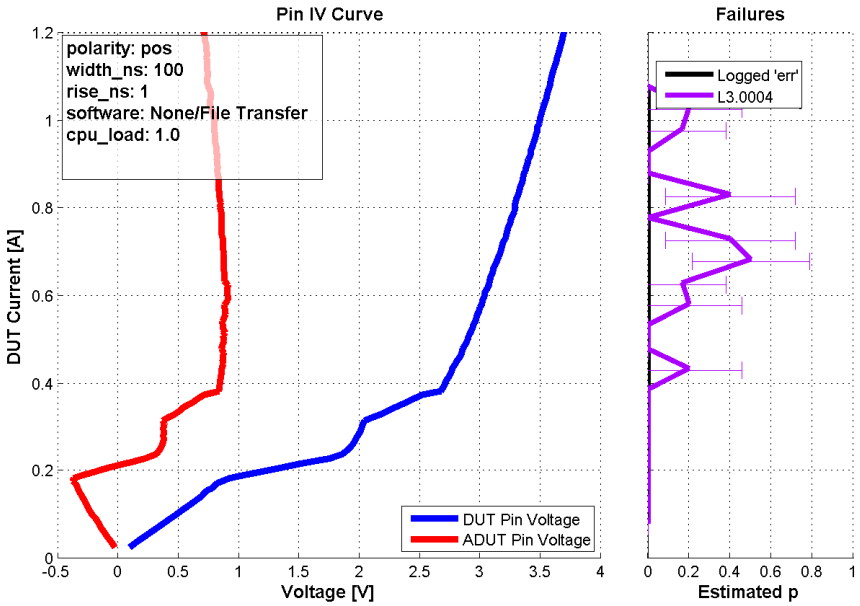


Figure C.7. USB3_Rxx, positive pulse rise time test

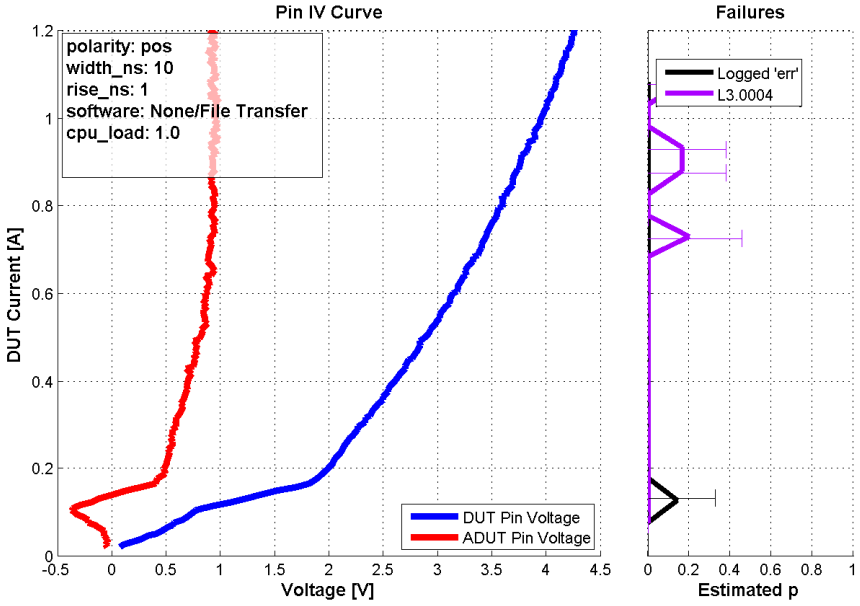


Figure C.8. USB3_Rxx, positive average threadcount test

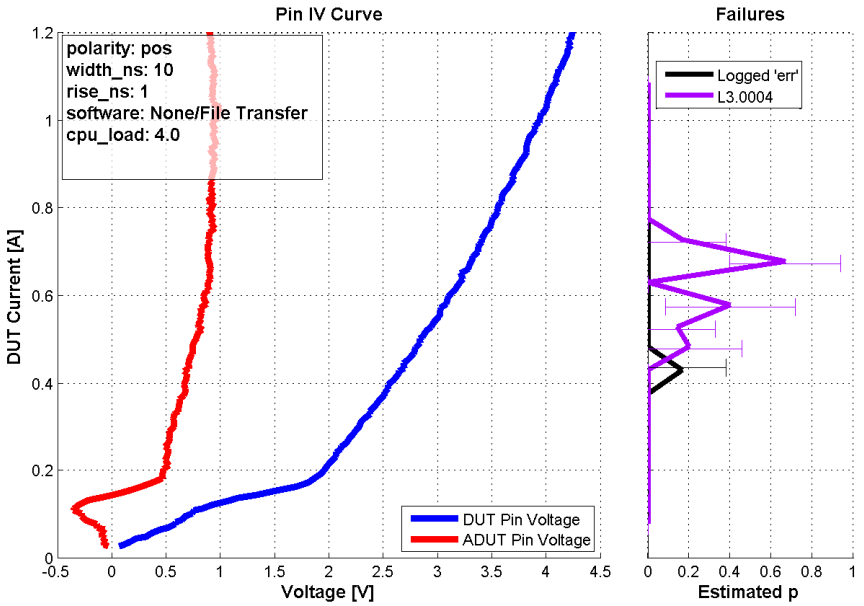


Figure C.9. USB3_Rxx, positive average threadcount test

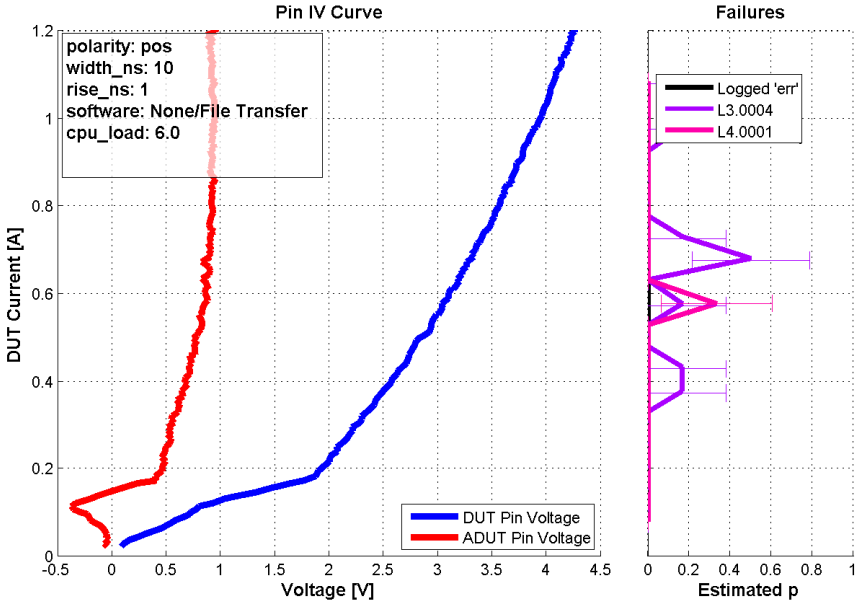


Figure C.10. USB3_Rxx, positive average threadcount test

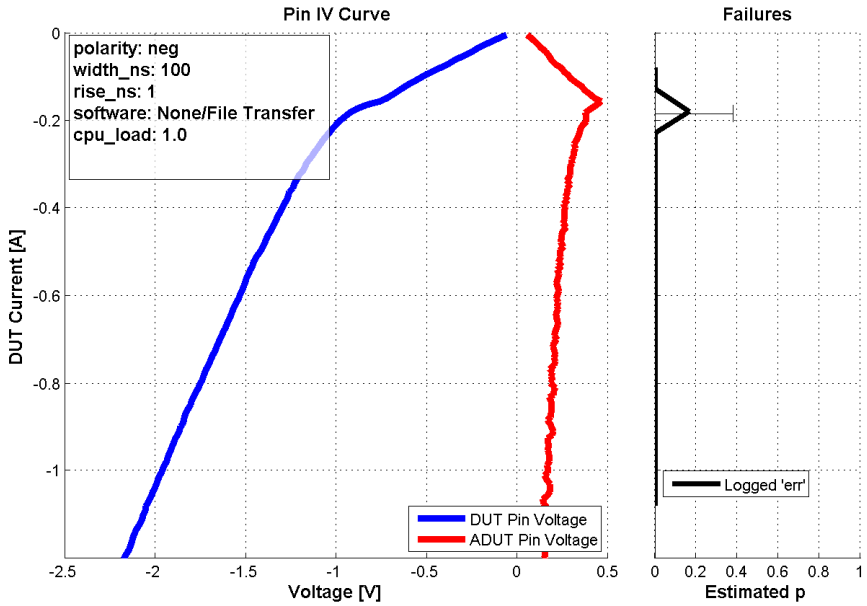


Figure C.11. USB3_Rxx, negative pulse width test

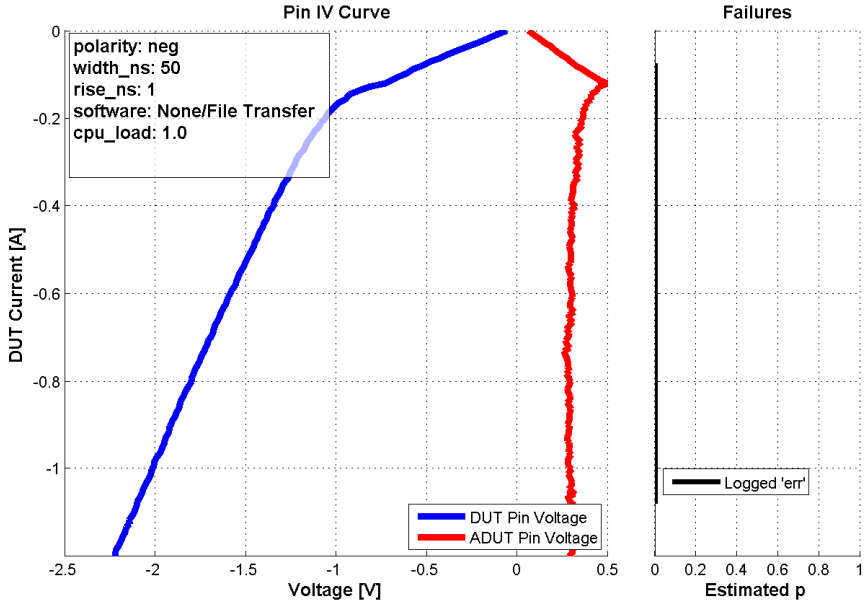


Figure C.12. USB3_Rxx, negative pulse width test

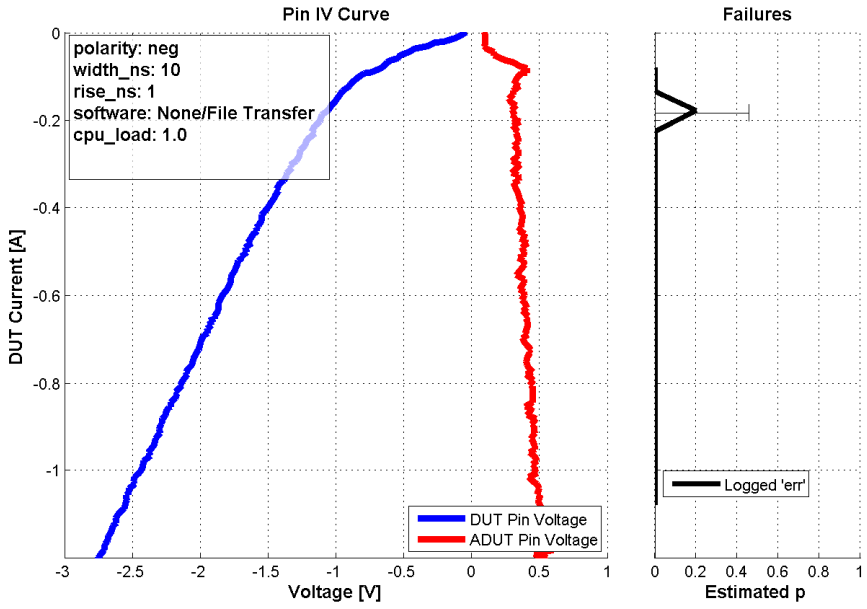


Figure C.13. USB3_Rxx, negative pulse width test

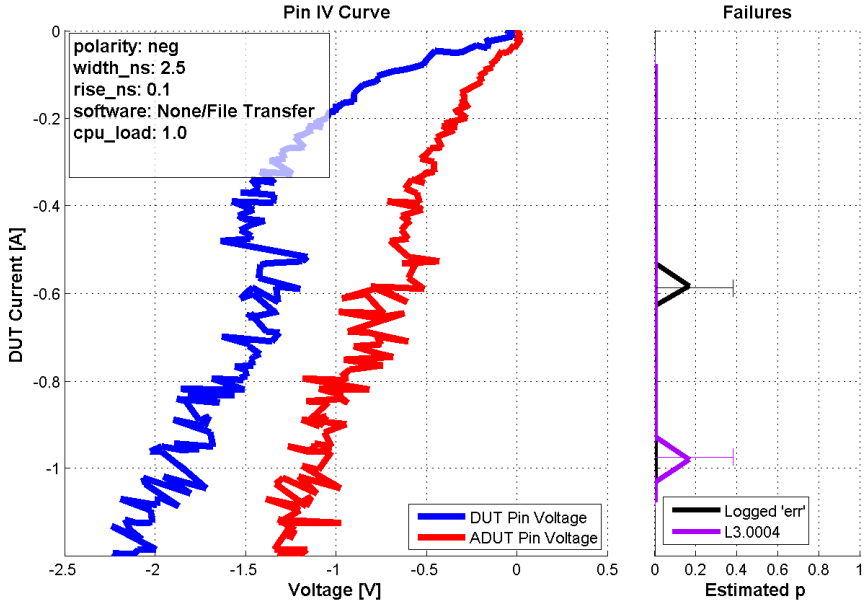


Figure C.14. USB3_Rxx, negative pulse width test

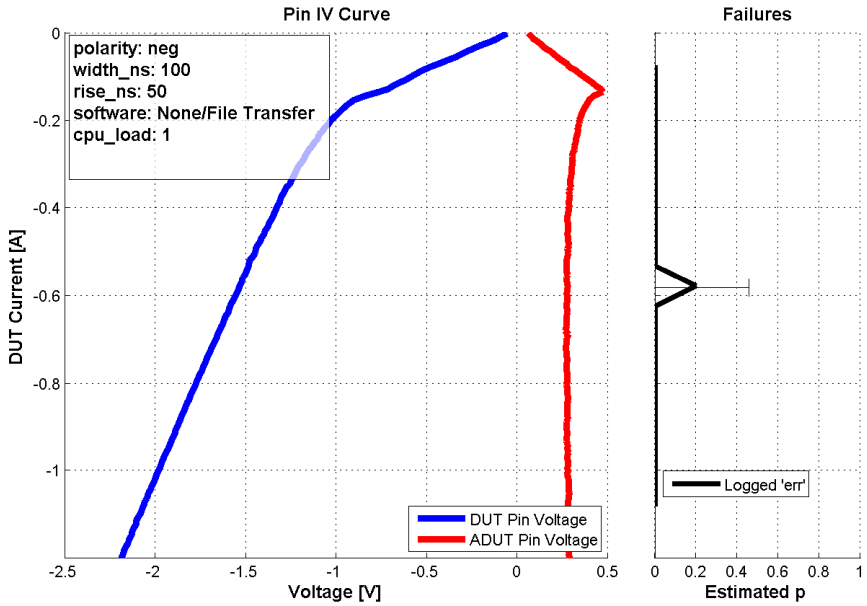


Figure C.15. USB3_Rxx, negative pulse rise time test

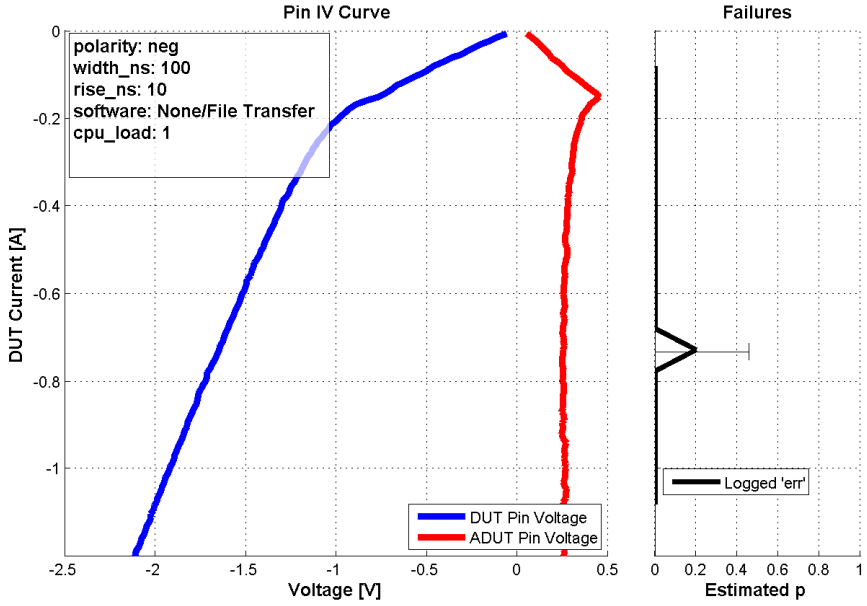


Figure C.16. USB3_Rxx, negative pulse rise time test

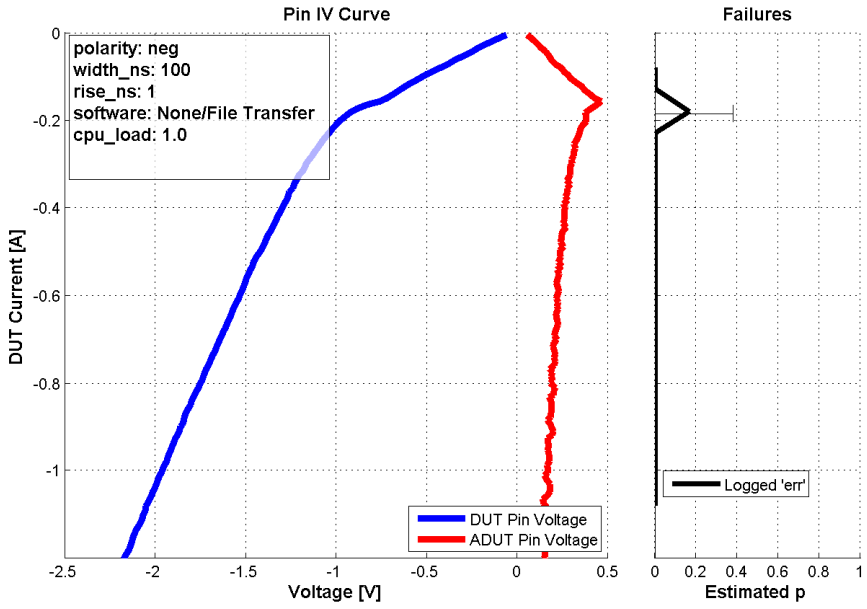


Figure C.17. USB3_Rxx, negative pulse rise time test

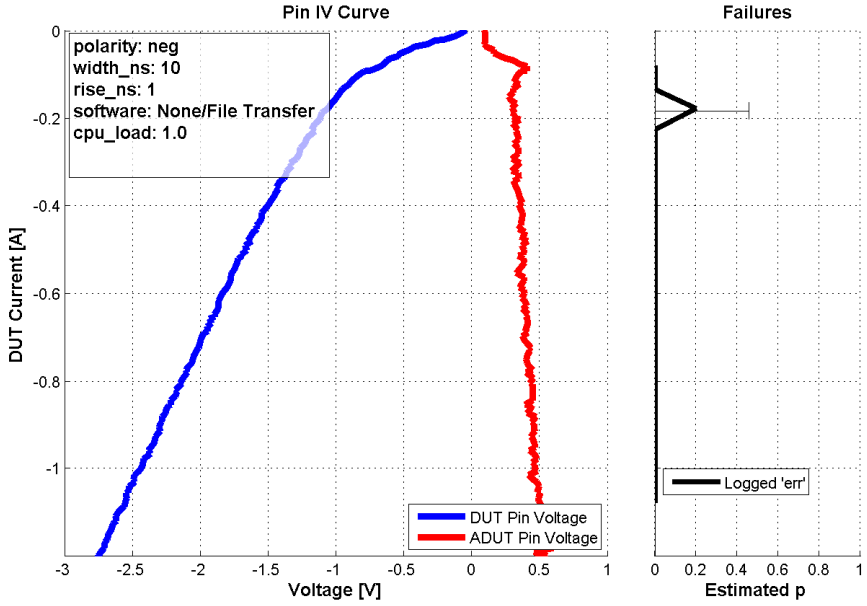


Figure C.18. USB3_Rxx, negative average threadcount test

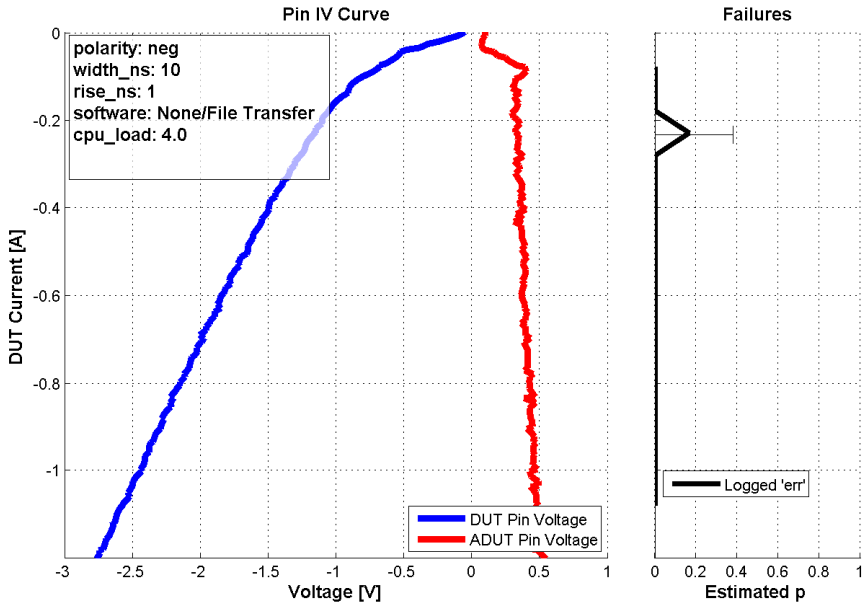


Figure C.19. USB3_Rxx, negative average threadcount test

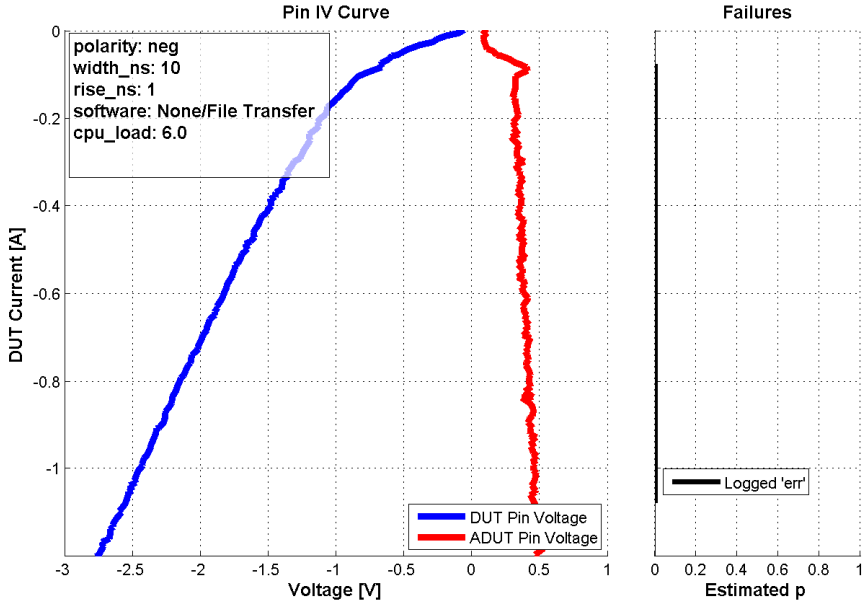


Figure C.20. USB3_Rxx, negative average threadcount test

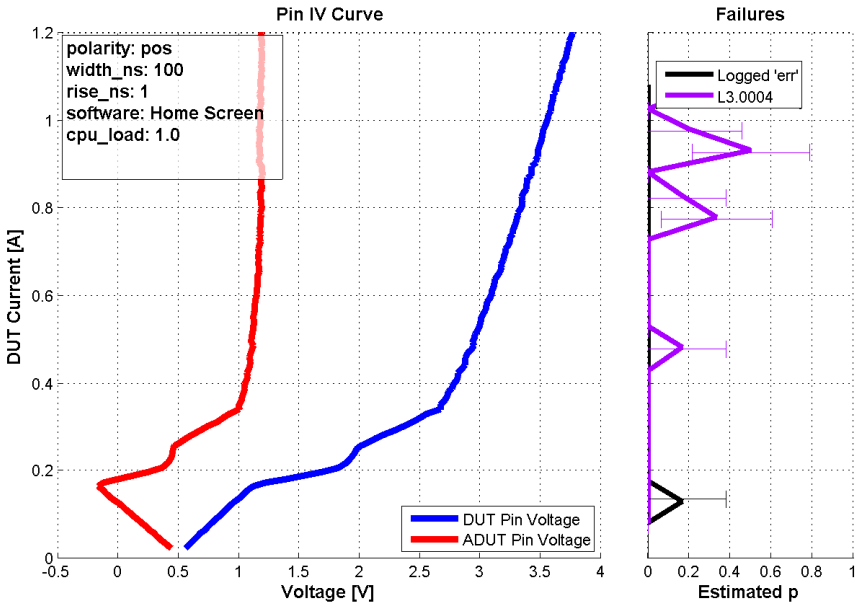


Figure C.21. USB3_Txx, positive pulse width test

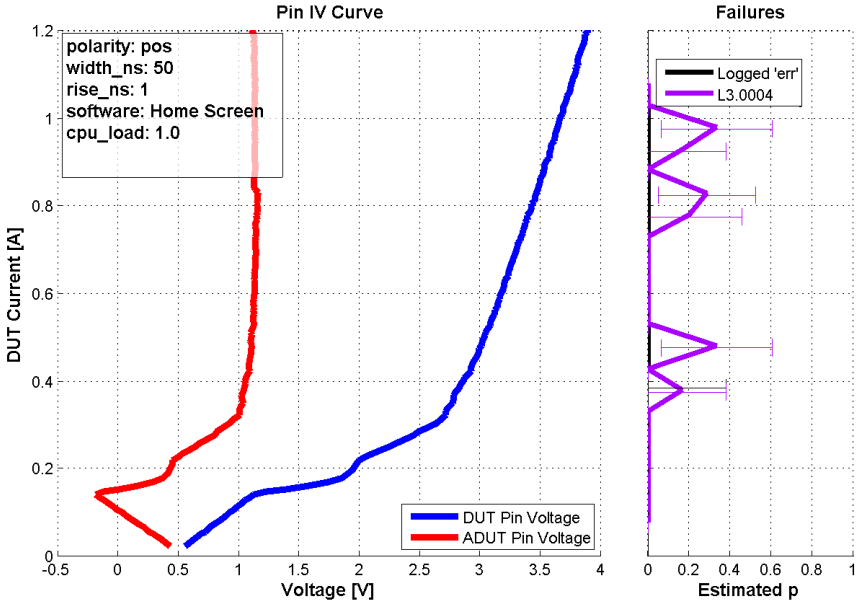


Figure C.22. USB3_Txx, positive pulse width test

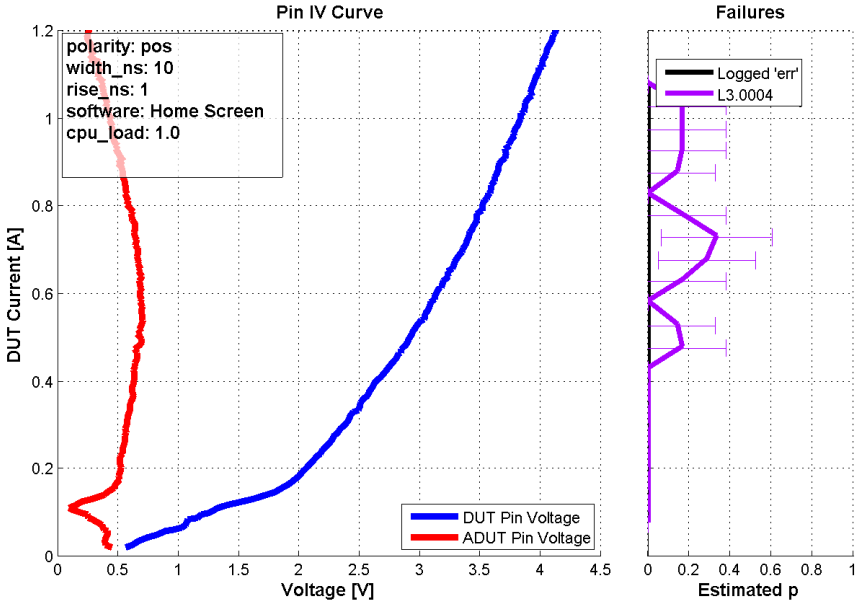


Figure C.23. USB3_Txx, positive pulse width test

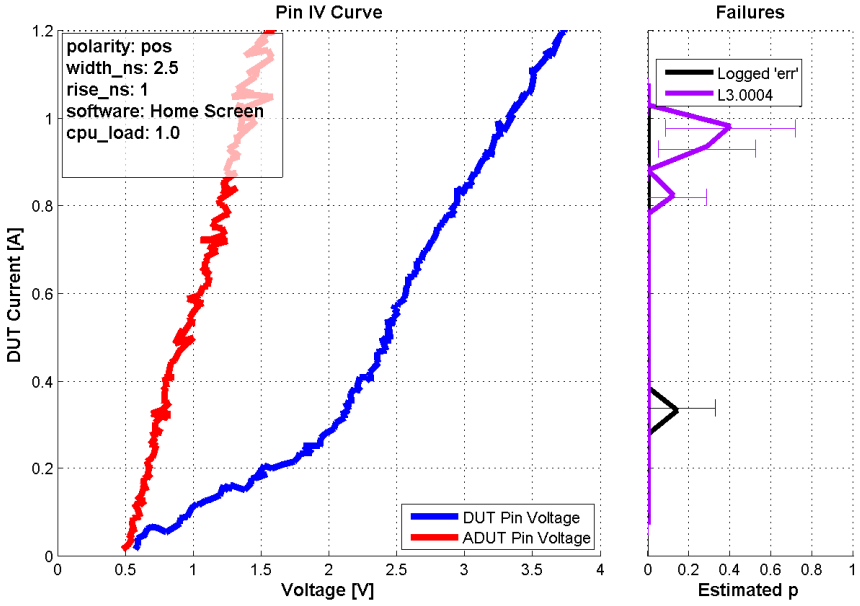


Figure C.24. USB3_Txx, positive pulse width test

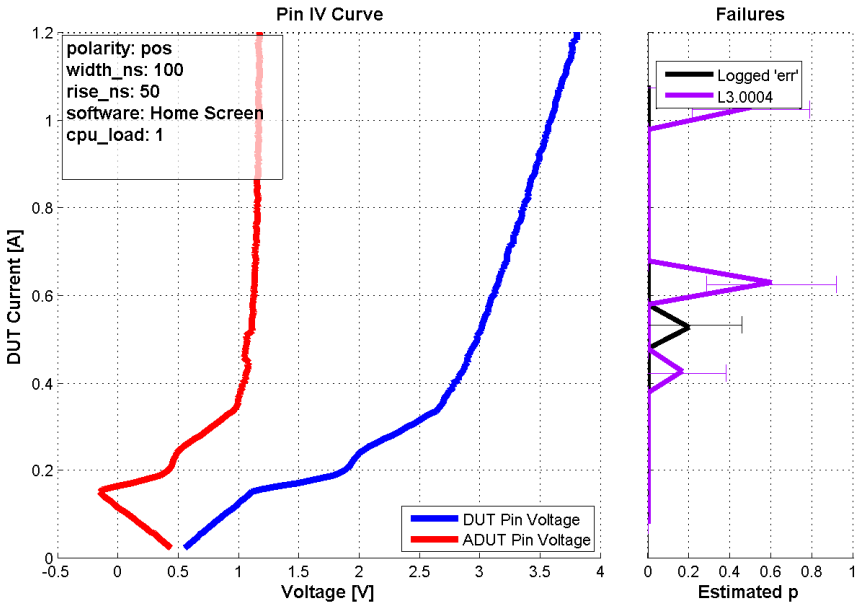


Figure C.25. USB3_Txx, positive pulse rise time test

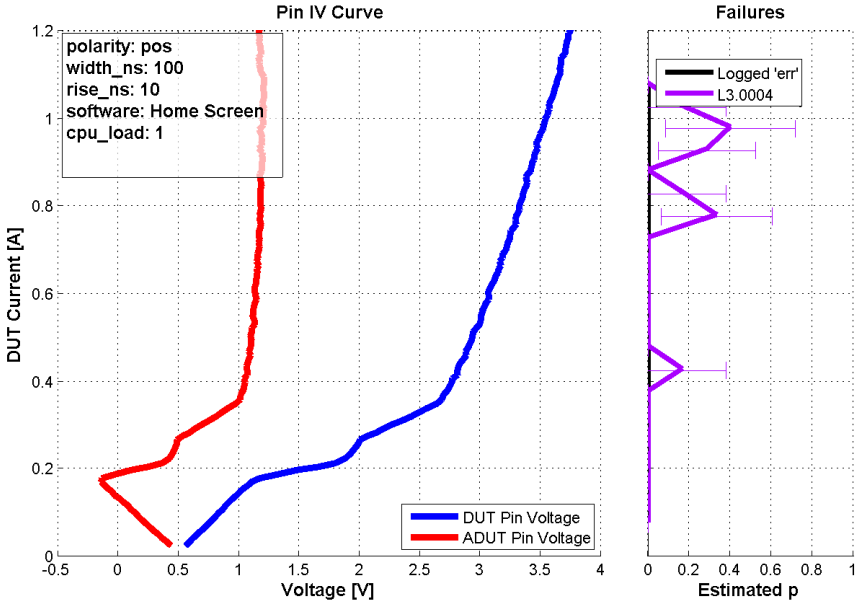


Figure C.26. USB3_Txx, positive pulse rise time test

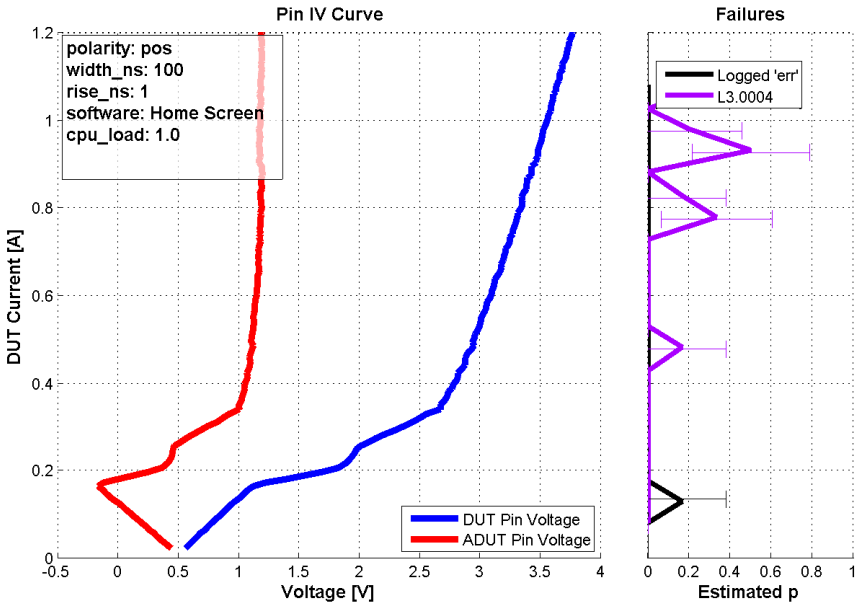


Figure C.27. USB3_Txx, positive pulse rise time test

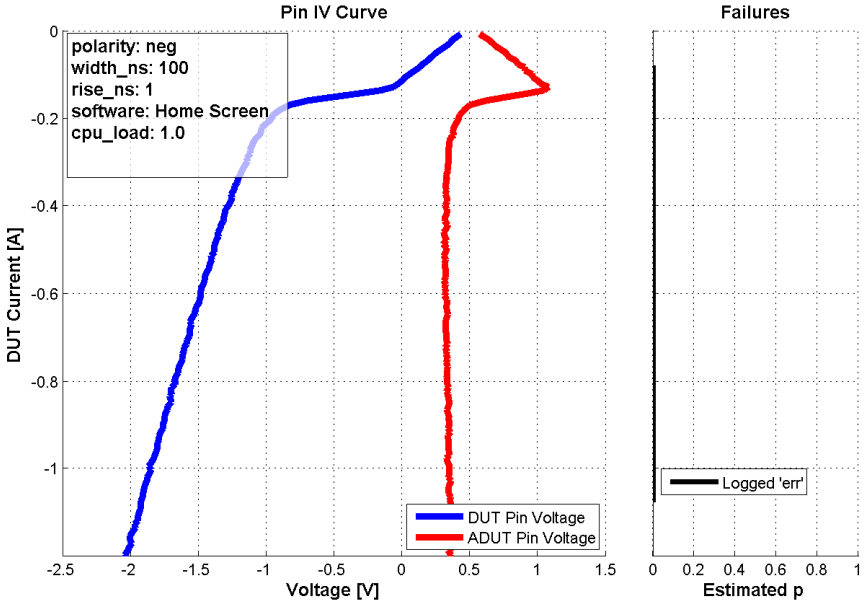


Figure C.28. USB3_Txx, negative pulse width test

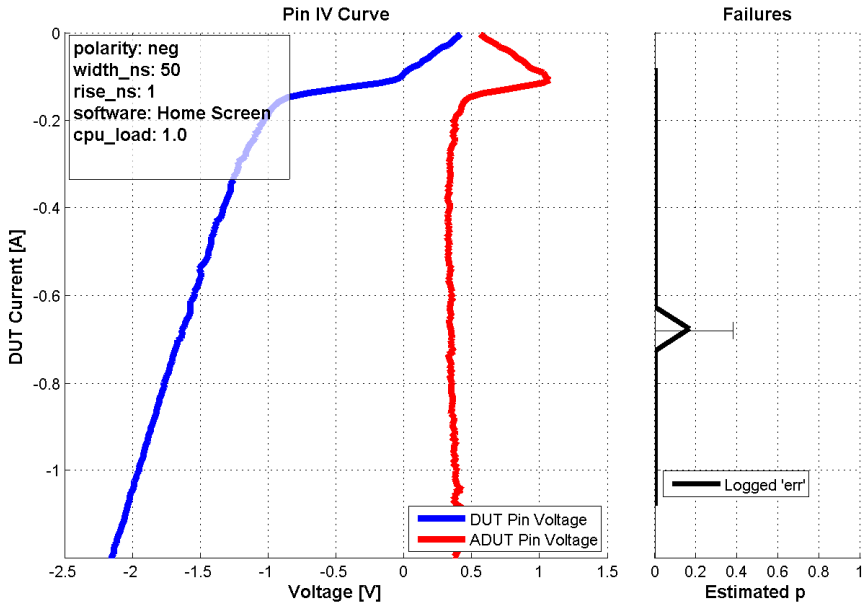


Figure C.29. USB3_Txx, negative pulse width test

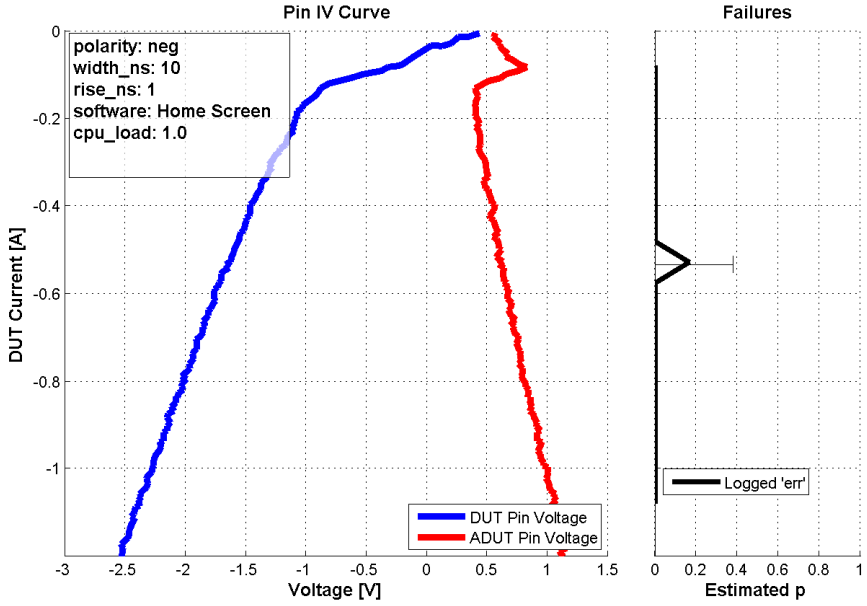


Figure C.30. USB3_Txx, negative pulse width test

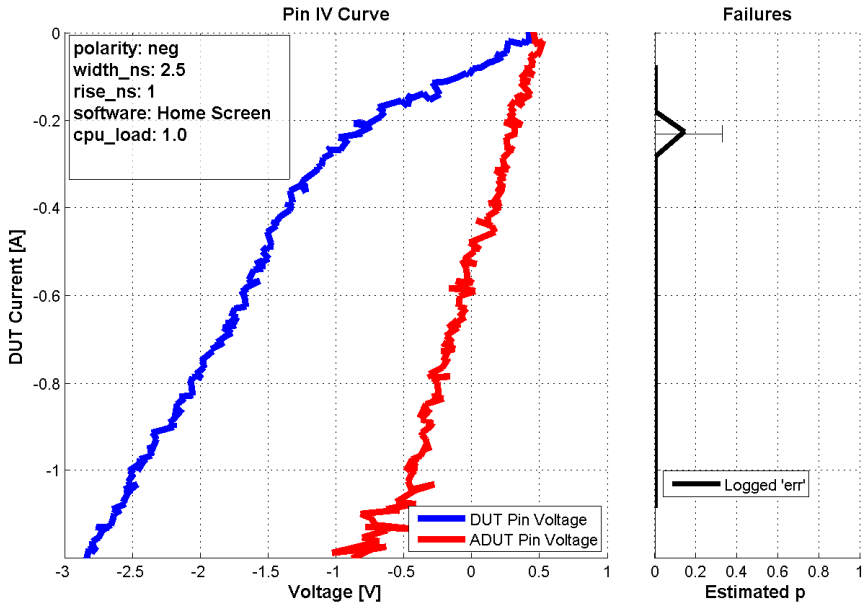


Figure C.31. USB3_Txx, negative pulse width test

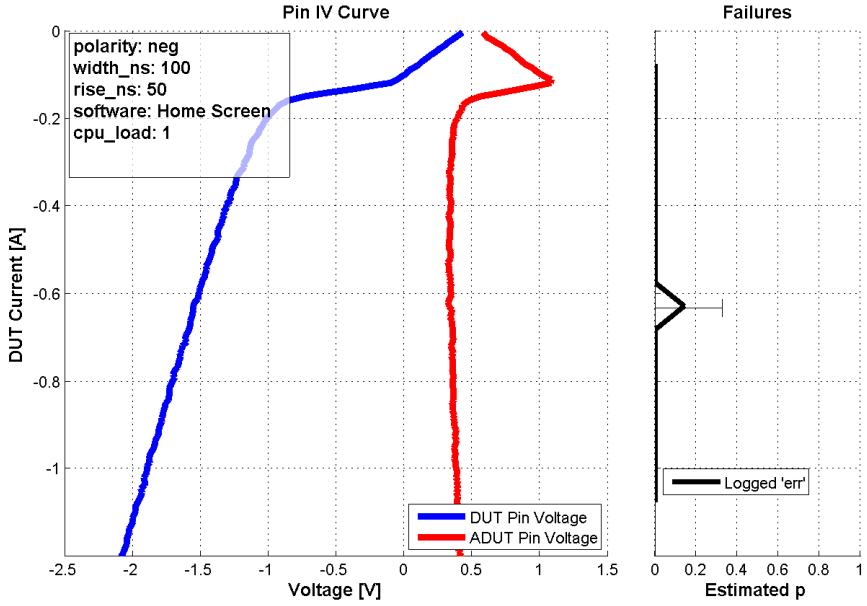


Figure C.32. USB3_Txx, negative pulse rise time test

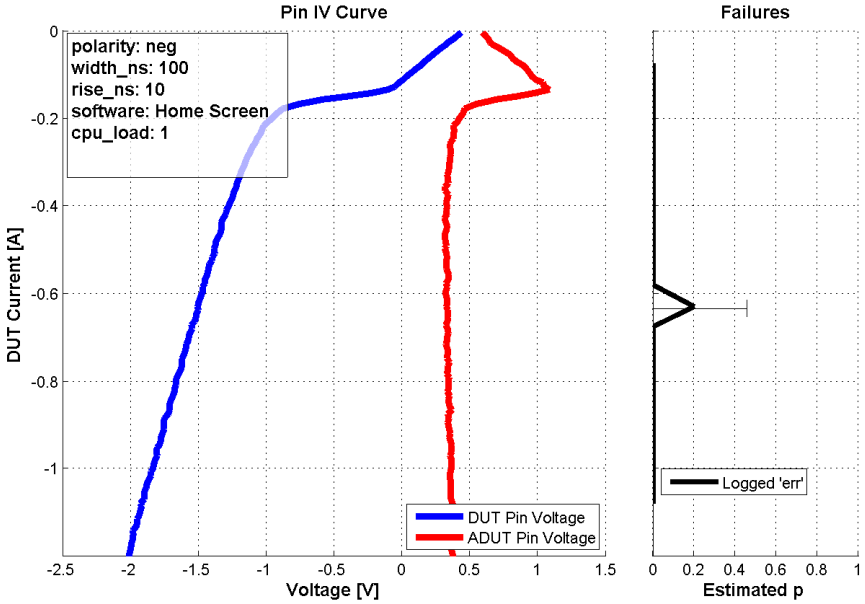


Figure C.33. USB3_Txx, negative pulse rise time test

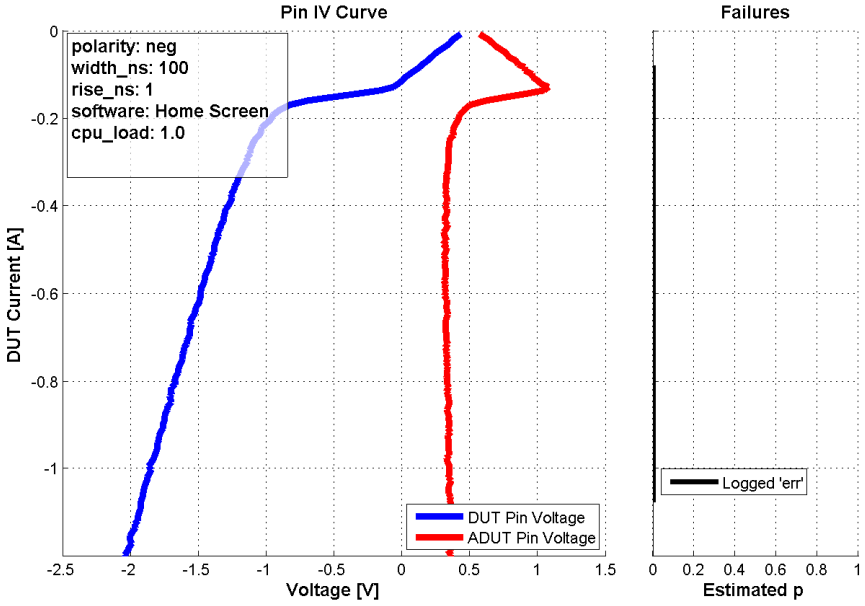


Figure C.34. USB3_Txx, negative pulse rise time test

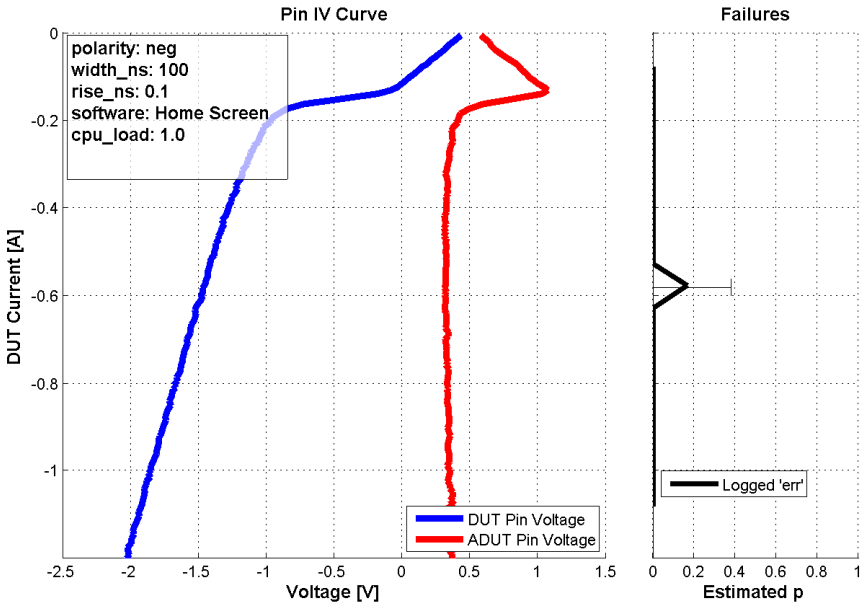


Figure C.35. USB3_Txx, negative pulse rise time

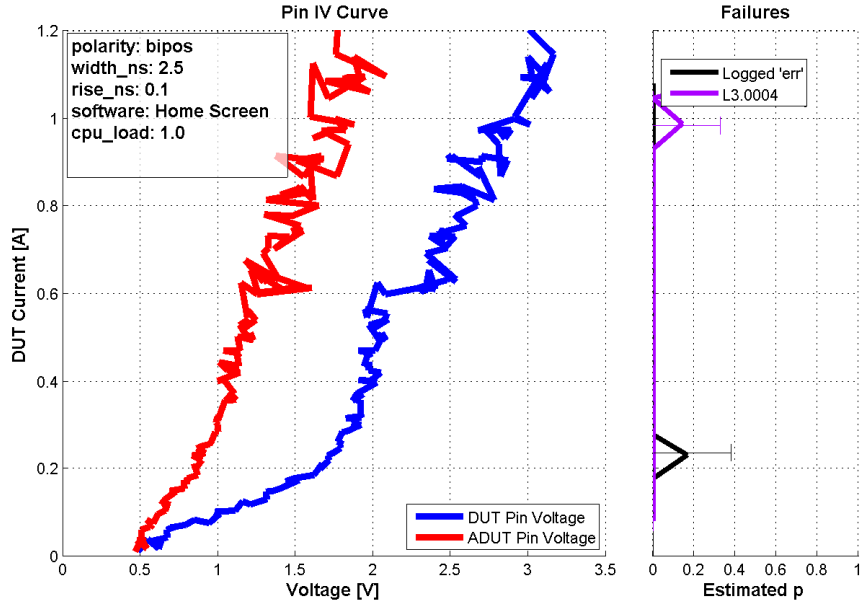


Figure C.36. USB3_Txx, bipolar test

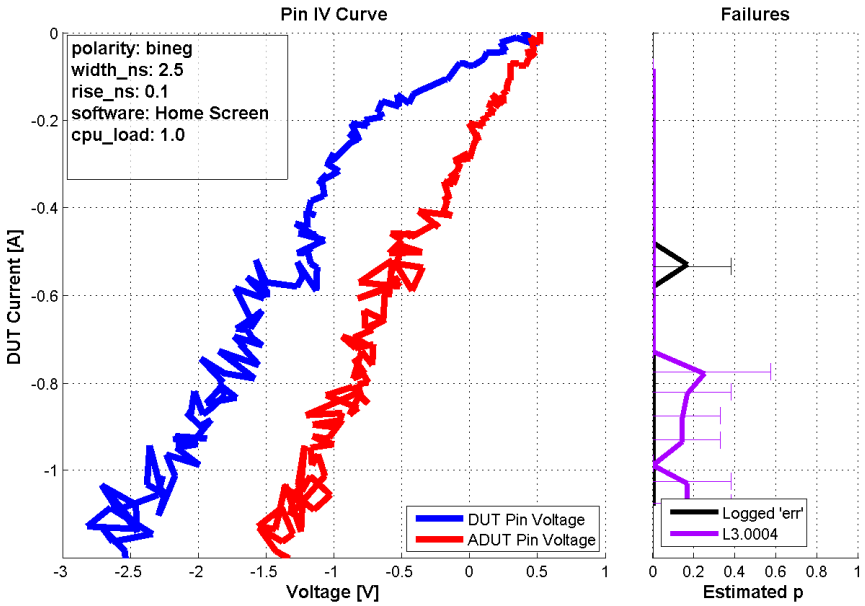


Figure C.37. USB3_Txx, bipolar test

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VITA

Benjamin John Orr began his undergraduate studies at the Missouri University of Science and Technology formerly known as the University Missouri-Rolla in September 2007. In 2011 he joined the Missouri University of Science and Technology EMC Lab as an undergraduate researcher. He graduated with his Bachelor of Science in Electrical Engineering as well as his Bachelor of Science in Computer Engineering in December of 2011. After graduation, he continued research with the EMC lab for his graduate studies in the Masters of Science program before transitioning to the Doctoral program to begin work on long-term research projects in cooperation with industry partners. In December of 2016 he received his Doctor of Philosophy in Electrical Engineering from Missouri University of Science and Technology.

During his time as an undergraduate at the Missouri University of Science and Technology, Ben was active in the university Newman Center and the local student branch of the IEEE. As a graduate research assistant he worked with a variety of companies including: Apple, Intel, Sony, LG, and vTitan to solve EMC, RFI, and ESD issues.