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Efficient and quantitative emc predictions (emission and immunity) for ECU modules

Guangyao Shen

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EFFICIENT AND QUANTITATIVE EMC PREDICTIONS (EMISSION AND
IMMUNITY) FOR ECU MODULES

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GUANGYAO SHEN

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Barbara Hale

PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three papers, formatted in the style used by the Missouri University of Science and Technology, listed as follows:

Paper I, Shen, G; Yang, S; Khilkevich, V.V.; Pommerenke, D.J.; Aichele, H.L.; Eichel, D.R.; Keller, C., "ESD Immunity Prediction of D Flip-Flop in the ISO 10605 Standard Using a Behavioral Modeling Methodology," in Electromagnetic Compatibility, IEEE Transactions on , vol.57, no.4, pp.651-659, Aug. 2015.

Paper II, Shen, G; Yang, S; Khilkevich, V.V.; Pommerenke, "Maximum Radiated Emissions Evaluation For The Heatsink/IC Structure Using The Measured Near Electrical Field Up To 40 GHz," submitted to Electromagnetic Compatibility, IEEE Transactions.

Paper III, Shen, G; Khilkevich, V.V.; Pommerenke, "Terminal Modeling Of DC-DC Converters With Stochastic Behavior," submitted to Electromagnetic Compatibility, IEEE Transactions.

ABSTRACT

This dissertation consists of three papers. In the first paper, a methodology of building an IC model capable of predicting failures for given disturbances at the clock input based on limited or no knowledge about IC internals was developed.

In the second paper, the maximized radiated emissions of the heat-sink/IC structure are predicted up to 40 GHz by creating an equivalent source using the measured electrical field in the gap between the heatsink and ICs. The electric field is detected by an E-field probe made of an open coaxial cable coated with absorbing material. A numerical model is built in CST microwave studio to obtain the maximized radiated field with the measured field used as a source to excite the heat-sink model. The evaluated maximized radiated field is in good agreement with the measured value; the error is within 6 dB.

In the third paper, a characterization method for converters with stochastic behavior is presented. The averaged and maximized spectrum of the measured voltages and currents are used to create the model. The phase information is obtained using a dedicated reference channel. After the equivalent source was determined, the actual induced noise voltage at the test load was compared to that predicted by the model with averaged and maximized spectrum to estimate its accuracy. The results indicate that the agreement with the direct measurement is within 5 dB up to 100 MHz when the load is within the characterization range.

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Finally, my heartfelt gratitude goes to my parents, my brother, my sisters and my girlfriend, Yilin Liang, for their support and encouragement towards achieving this goal.

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SECTION

1. INTRODUCTION

Clock and data signals in digital circuits rapidly switch between high and low levels. The switching voltage and current generate unwanted high-frequency electromagnetic fields, which interfere with nearby components causing conducted and radiated emissions.

In the first paper, a methodology of building an IC model capable of predicting failures for given disturbances at the clock input based on limited or no knowledge about IC internals was developed. In this paper, an 18 MHz D flip-flop IC is characterized and its behavioral model is presented. The resulting IC model is validated in the setup according to the ISO 10605 standard. A complete model of the setup combining the IC behavioral model and the passive parts of the setup, including parallel and twisted pair harnesses, is built to estimate the failure prediction accuracy in a totally simulated environment. The results show that the model can predict the failure level with the error of less than 20% in parallel harness case and around 30% in the twisted pair case.

In the second paper, the maximized radiated emissions of the heat-sink/IC structure are predicted up to 40 GHz by creating an equivalent source using the measured electrical field in the gap between the heatsink and ICs. The electric field is detected by an E-field probe made of an open coaxial cable coated with absorbing material. A numerical model is built in CST microwave studio to obtain the maximized radiated field with the measured field used as a source to excite the heat-sink model. The evaluated maximized radiated field is in good agreement with the measured value; the error is within 6 dB.

In the third paper, a characterization method for converters with stochastic behavior is presented. The averaged and maximized spectrum of the measured voltages and currents are used to create the model. The phase information is obtained using a dedicated reference channel. After the equivalent source was determined, the actual induced noise voltage at the test load was compared to that predicted by the model with averaged and maximized spectrum to estimate its accuracy. The results indicate that the agreement with the direct measurement is within 5 dB up to 100 MHz when the load is within the characterization range.

The primary contributions of this dissertation include:

An experimental methodology based on VNA measurements to build an equivalent circuit model of an IC was presented (Paper I).

A methodology to create a behavioral model of an IC was developed (Paper I).

A new E field probe was designed up to 40 GHz (Paper II).

A methodology to predict the radiation of heatsink/IC structure using measured near field as an equivalent source was developed (Paper II).

A characterization board was designed for terminal model characterization (Paper III).

A methodology was developed to deal with the terminal model characterization as the noise source has stochastic behavior (Paper III).

PAPER

I. ESD IMMUNITY PREDICTION OF D FLIP-FLOP IN THE ISO 10605 STANDARD USING BEHAVIORAL MODELING METHODOLOGY

Guangyao Shen, *Student Member, IEEE*, Victor Khilkevich, *Member, IEEE*, David Pommerenke, *Senior Member, IEEE*

ABSTRACT— As the ESD stress is becoming more and more important for integrated circuits (ICs), the ability to predict IC failures becomes critical. In this paper, an 18 MHz D flip-flop IC is characterized and its behavioral model is presented. The resulting IC model is validated in the setup according to the ISO 10605 standard. A complete model of the setup combining the IC behavioral model and the passive parts of the setup, including parallel and twisted pair harnesses, is built to estimate the failure prediction accuracy in a totally simulated environment. The results show that the model can predict the failure level with the error of less than 20% in parallel harness case and around 30% in the twisted pair case.

Index Terms—flip-flop; behavioral model; ISO 10605; parallel harness; twisted pair harness.

1. INTRODUCTION

These days, ESD stress is becoming more and more critical for electrical systems. More and more complex electronic modules have to work together without disturbing or being disturbed by electromagnetic interferences or fast transient events. Thus, several electromagnetic compatibility standards (including ESD) have been created to guarantee the safe operation of electronic systems in different environments such as vehicles [1].

The ISO 10605 [2] is a recent automotive standard detailing test methods for direct and indirect discharge. ISO 10605 specifies the electrostatic discharge (ESD) test methods necessary to evaluate electronic modules intended for vehicle use. It describes test procedures for evaluating both electronic modules on the bench and whole vehicles. It also describes a test procedure that classifies the ESD sensitivity of modules for packaging and handling.

It remains difficult to predict the reliability of the system in the ESD test if the ICs are considered as black box. It is possible to use IBIS models developed initially for SI applications [3] to predict the ESD-related behavior of ICs [4-6]. Besides modeling using IBIS standard, several other methods are currently under standardization process, under the supervision of the International Electro technical Commission (IEC), one of which is the direct power injection (DPI) [7]-[8].

In this paper an alternative modeling method is proposed, which emphasizes ease of IC characterization and model implementation. The focus is put on the system level ESD behavioral modelling of an 18 MHz D flip-flop IC. This is a relatively simple IC, but by using it is possible to simulate some aspects of failures of electronic modules.

At first, behavioral model for the simple D flip-flop has been developed by IC characterization based on the methodology in [9] and extended to utilize for the twisted pair case. An associated simulation methodology was proposed. The full wave model of the ESD gun and ISO 10605 standard setup was built. Then, the system-level model which combined the IC behavioral model and the full wave model was detailed and was used to predict the failure of the IC when the ESD gun discharged to the particular places (three islands and the platform). The predicted failure levels were validated by the measurement.

2. IC CHARACTERIZATION MEASUREMENT AND MODELING

A schematic diagram of the PCB used to test the IC immunity is shown in Figure 2.1. The input signal is fed to the clock pin of the IC, when the signal is large enough, the output state of the D flip-flop changes. When the IC is triggered, the LED turns on, which allows to monitor the event (a failure). In addition two passive probes are mounted on the PCB, which allows measuring input (clock) and output voltages during the test/characterization.

A decoupling capacitor was added parallel to the clock pin to create a more realistic situation, since the harness voltages in actual automotive electronic modules are almost always filtered.
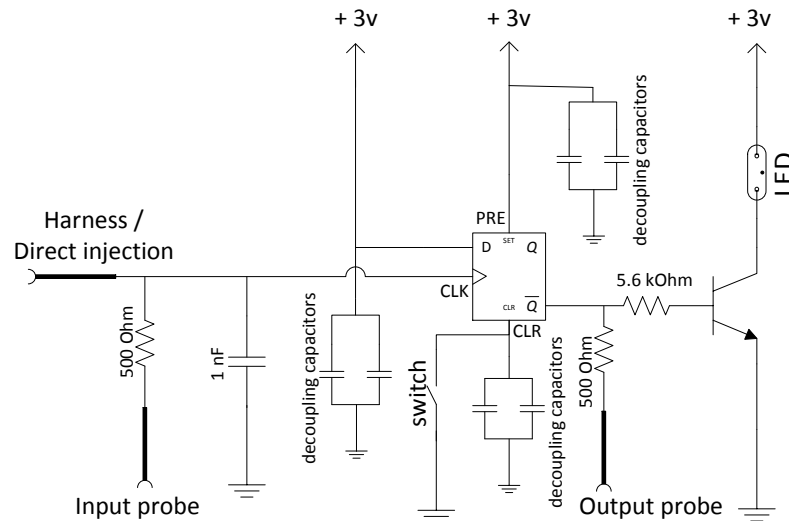
Figure 2. 1. Test PCB diagram

The photo of the PCB is displayed in Figure 2.2. The test IC was powered by a 3V battery. All the IC pins (PRE, Vcc, Vss and etc.) are decoupled by capacitors during the test.
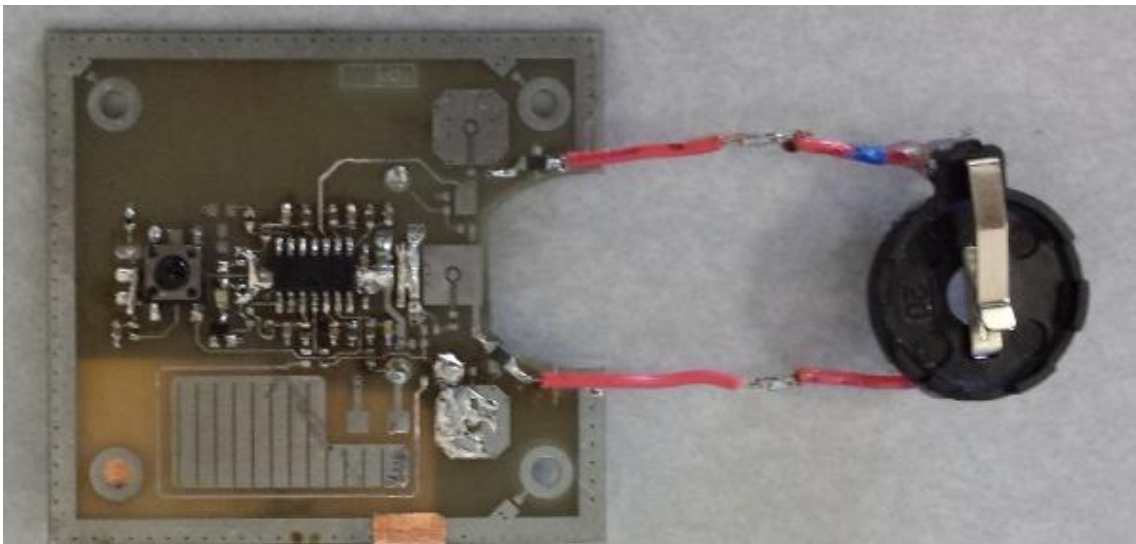
Figure 2. 2. Photo of the test PCB

The proposed model consists of the physical and behavioral parts. Physical and behavioral models were characterized separately as described below.

The input impedance of the IC was determined by measuring the reflection coefficient of the clock pin using a vector network analyzer. The reflection coefficient was converted to impedance as shown in Figure 2.3 and an equivalent model of the IC clock pin was created.

In the frequency range up to 3 GHz the input impedance of the IC can be modelled accurate enough by a 1.45 pF capacitor. Since ESD-induced signals have mostly high-frequency components, the resistive behaviour of the input pin below 20 MHz is not modelled.
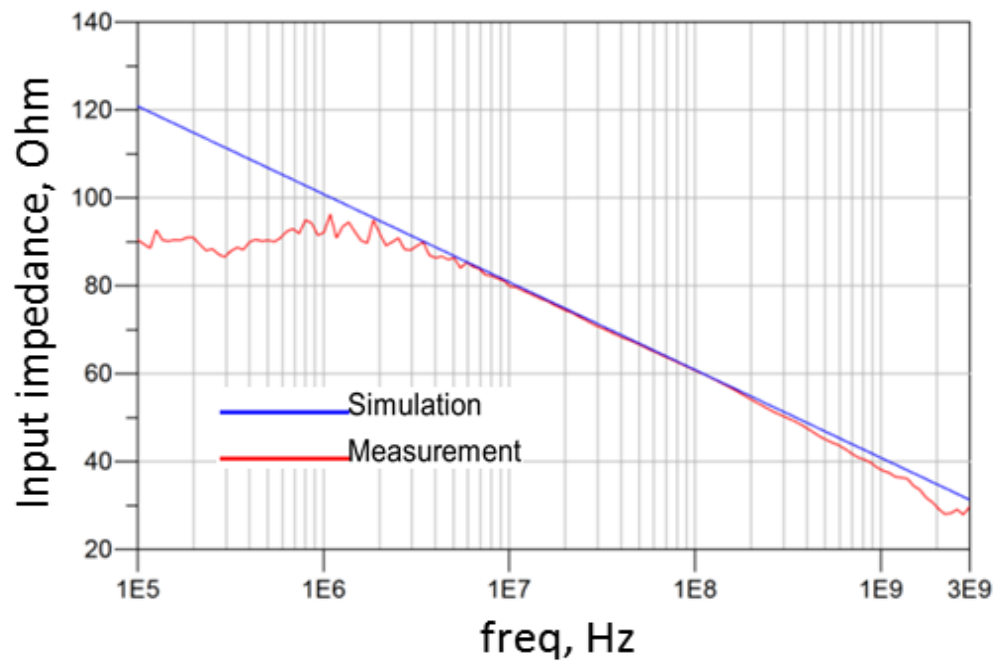
Figure 2. 3. Measured and simulated input impedance curve

In order to model the impedance of the decoupling capacitor, the whole input circuit was measured. By comparing impedances with and without the decoupling

capacitors, a complete equivalent circuit of the input impedance was created as shown in Figure 2.4 and 2.5.
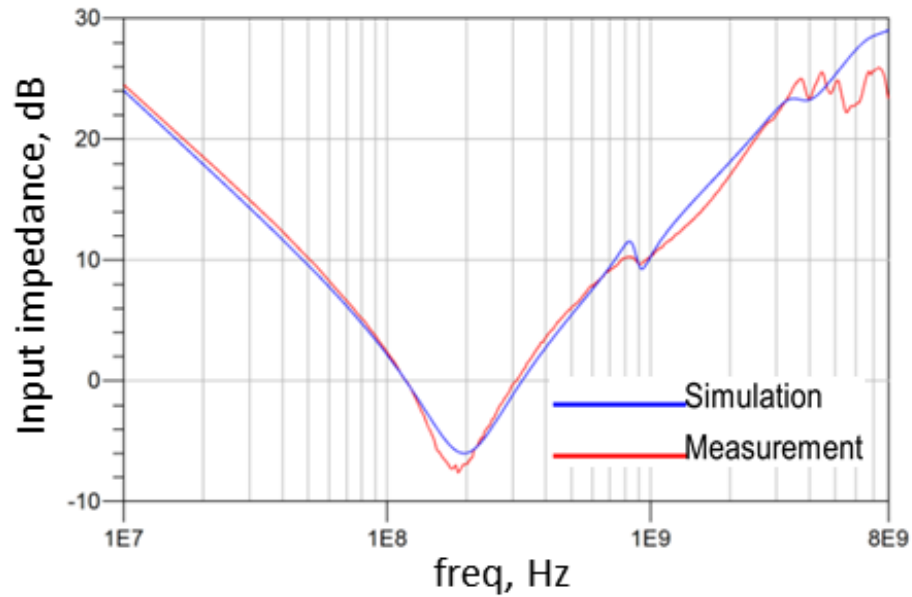
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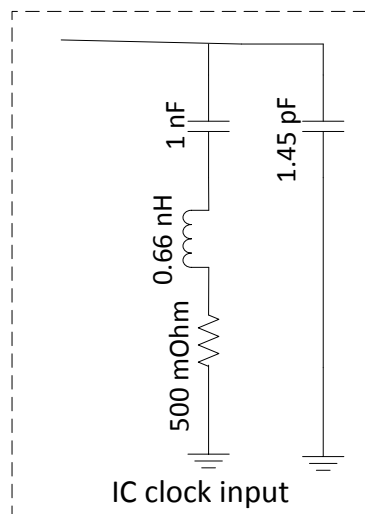
Figure 2. 5. The equivalent circuit when 1 nF capacitor was added at the clock pin

The IC switching behavior was characterized in the setup shown In Figure 2.6. Two kinds of waveforms were injected to the IC, one is a single trapezoidal pulse with different pulse width as shown in Figure 2.7, and another is a sine-wave packet of different frequency (from 100 MHz to 1GHz) and duration (number of period: Np) as shown in Figure 2.8. It was observed that the latter signal is especially important when the input signal is filtered by the decoupling capacitor. Both of these waveforms are generated by the computer controlled arbitrary waveform generator, amplified by the RF amplifier, and then injected into the pin of the IC under test (the clock pin).

The mechanisms responsible to the IC reaction to two types of signals are presumably different, therefore two sub-models were created, each responsible to a particular signal.
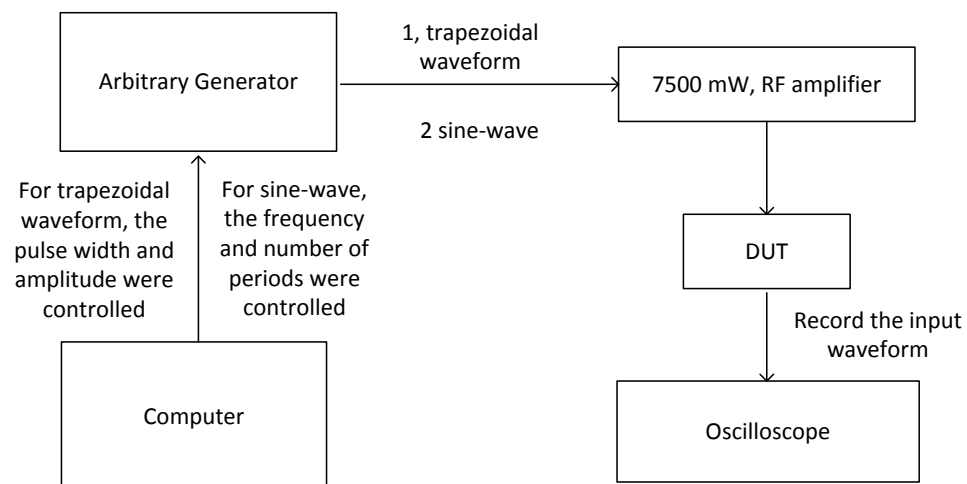
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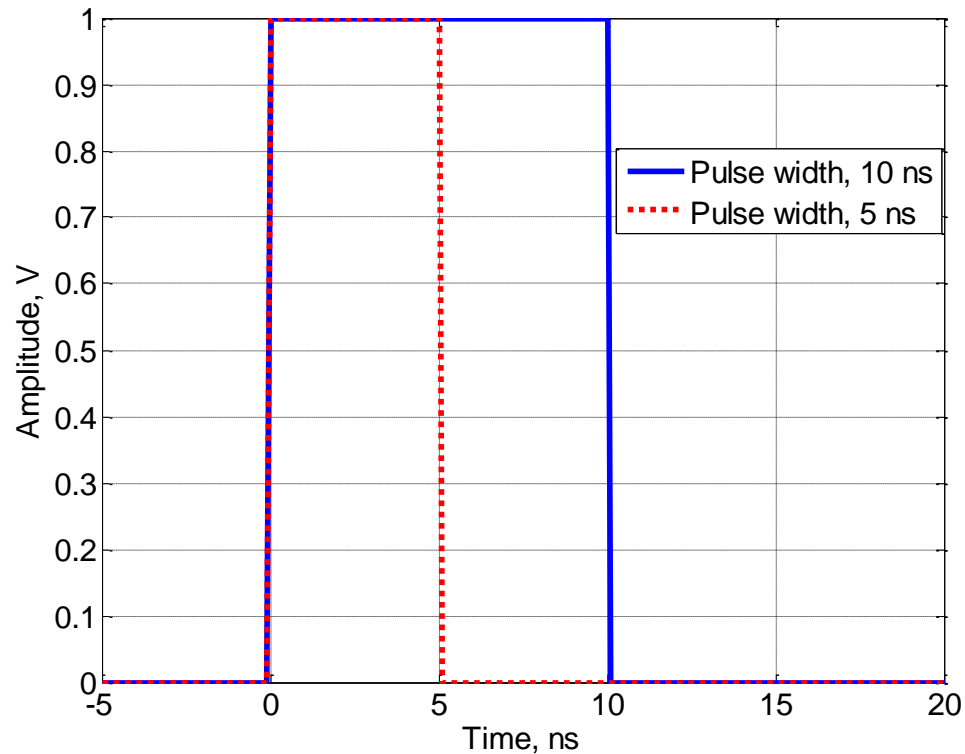
Figure 2. 7. Injected waveforms for trapezoidal pulse characterization

For each of the waveforms, injected into the IC pin, the generated signal was scaled up until the triggering of the flip-flop was observed. At the same time, the voltage induced at the IC clock pin was measured using a passive solder-in probe. This allowed to measure characterization curves that show the dependency of the maximum input voltage corresponding to triggering on the parameters of the signal.

The characterization curve for the trapezoidal pulse is shown in Figure 2.9. The only parameter for this curve is the pulse width. It can be observed that long pulses cause the IC to trigger at the static switching level (1.5 V). As the pulse becomes shorter, higher

voltages are required to switch the IC state. This behavior can be modelled well by the

low pass-filter followed by the threshold device as shown in Figure 2.12. The parameters

of the filter were tuned to match the measured curve resulting in the simulated curve

shown at Figure 2.9.
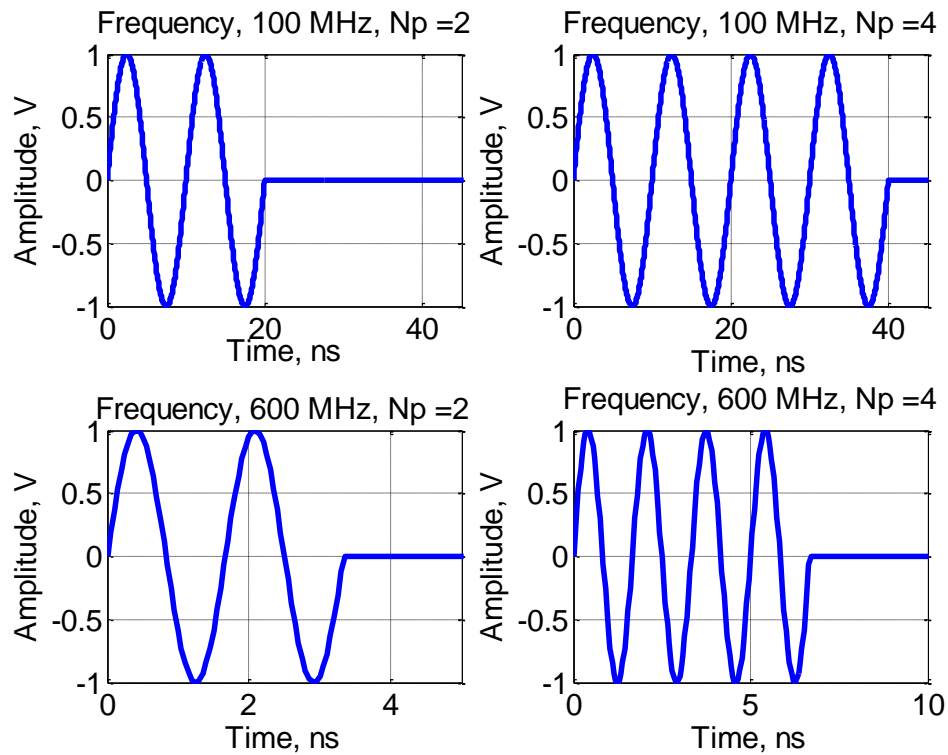
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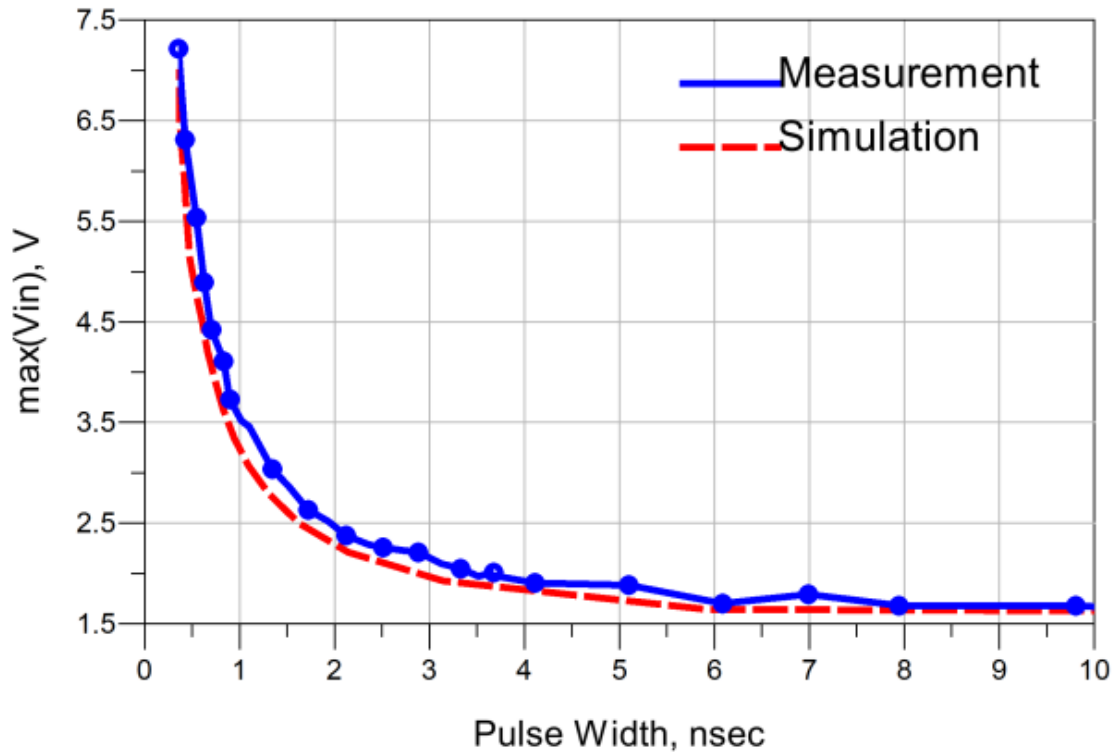
Figure 2. 9. Simulated curve compared with the measured data based on trapezoidal characterization

As can be noted, a model describing the IC reaction to the trapezoidal pulse is purely linear (up to the threshold device) and most likely corresponds to the low-pass filtering of the input pulse by the internal circuitry of the IC.

Besides this linear effect it was observed, that the IC reacts nonlinearly to the series of the bipolar pulses, i.e. the switching event depended on the number of pulses in the series, which cannot be accounted for by the linear model described above.

To characterize the IC behavior, sinusoidal signals given by

$$x(t) = \begin{cases} 0, & t < 0 \\ A\sin(2\pi ft), & 0 \le t \le N_p / f \\ 0, & t > N_p / f \end{cases}$$ (1)

were applied to the IC clock pin. The parameters of the signals were the frequency

f, and the number of periods Np. The recorded parameter again was the maximum

voltage of the input signal caused the IC triggering. The obtained characterization

curves are shown in Figure 2.11. It can be noted that as the number of period

increases, the IC can be disturbed by lower input voltages, which suggests some

kind of rectification effect. The measured input signals corresponding to the

triggering event in Figure 2.10 show that the signal is not clamped at -0.7 and 3.7

V as might be expected if the IC input protection circuit is engaged, so the

rectification must take place within the internal circuitry of the IC. And since this

circuitry is not available, a behavior model needs to be created.

To model this effect a circuit consisting of input impedance capacitor, nonlinear

element given by

$$y = \begin{cases} 0, & x < 0 \\ x, & x \ge 0 \end{cases}$$ (2)

where x and y are input and output signals respectively, and a low pass filter was

created as shown in Figure 2.13.
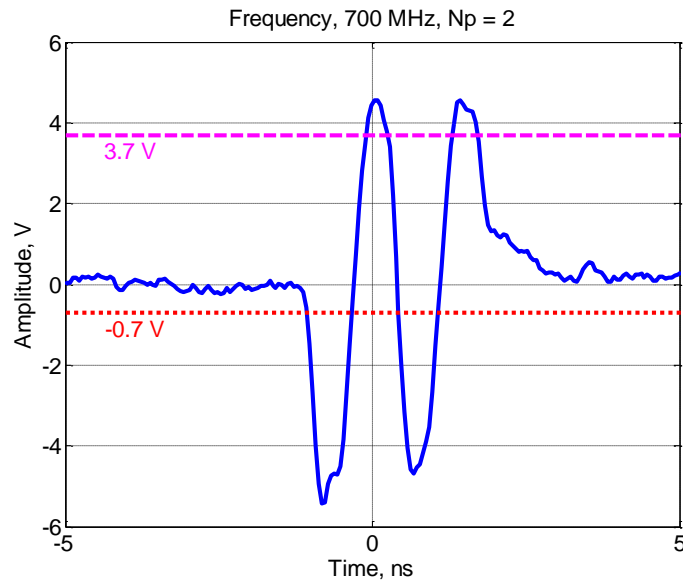
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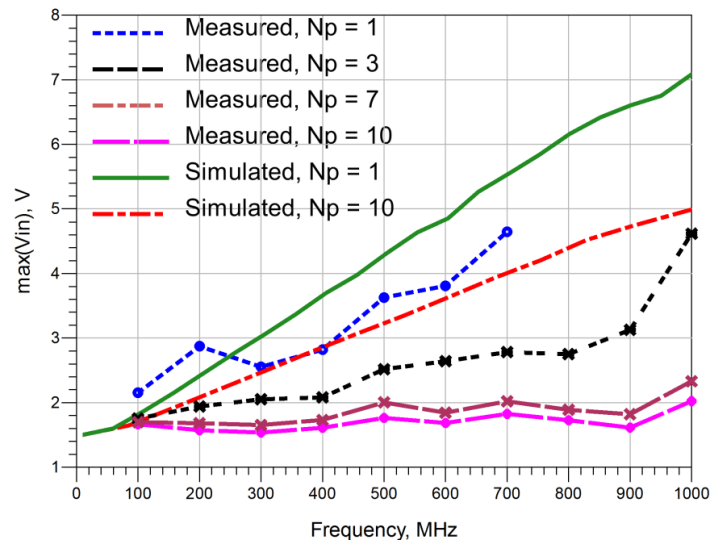
Figure 2. 11. Simulated curve compared with the measured data based on sine-wave
packet characterization

As two models introduced above are not completely independent in a sense that both trapezoidal and sinusoidal signals produce some outputs in both of them, the models were combined using a band-pass filter as shown in Figure 2.14, which allowed partially separate the incoming signals while retaining functionality of the model for the trapezoidal signal and at the same time model the rectification effect. The resulting simulated characterization curves for the sinusoidal signal obtained in the complete model in Figure 2.14 are shown in Figure 2.11 (red and green lines). The rectification effect definitely can be seen, but the agreement within the measured and modeled characterization curves is worse, compared to one that can be achieved in the isolated nonlinear model shown in Figure 2.13. However, this limited agreement was determined to be enough to predict the IC triggering in the actual test with reasonable accuracy, as can be seen later. The triggering of the model is determined by calculating the sum of output voltages of two sub-models (Vout1 and Vout2 shown in Figure 2.14) and comparing it to the static threshold level (1.5 V).
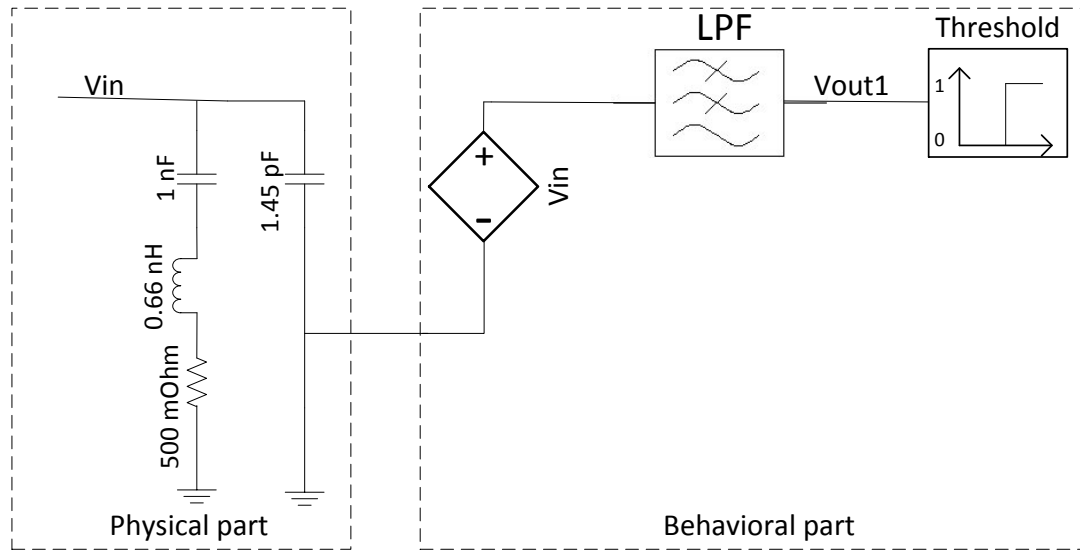
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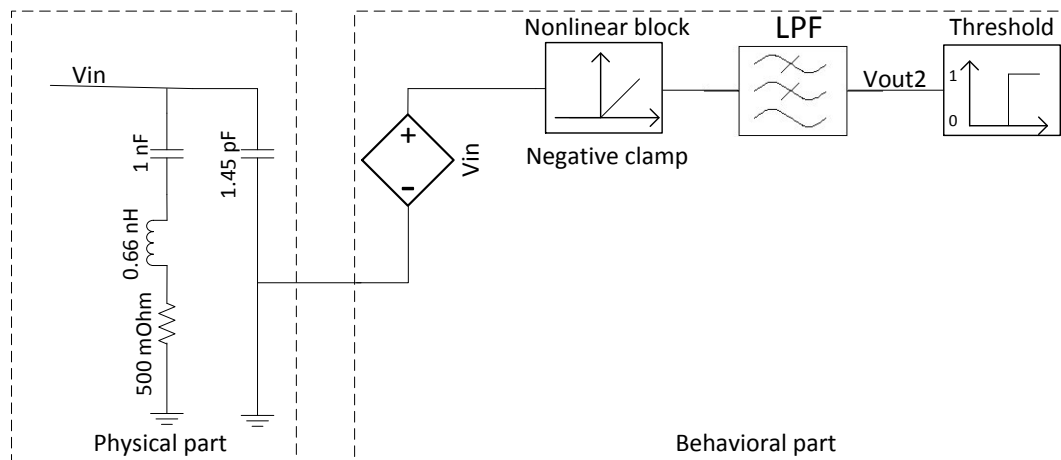
Figure 2. 13. IC behavioral model, Part II
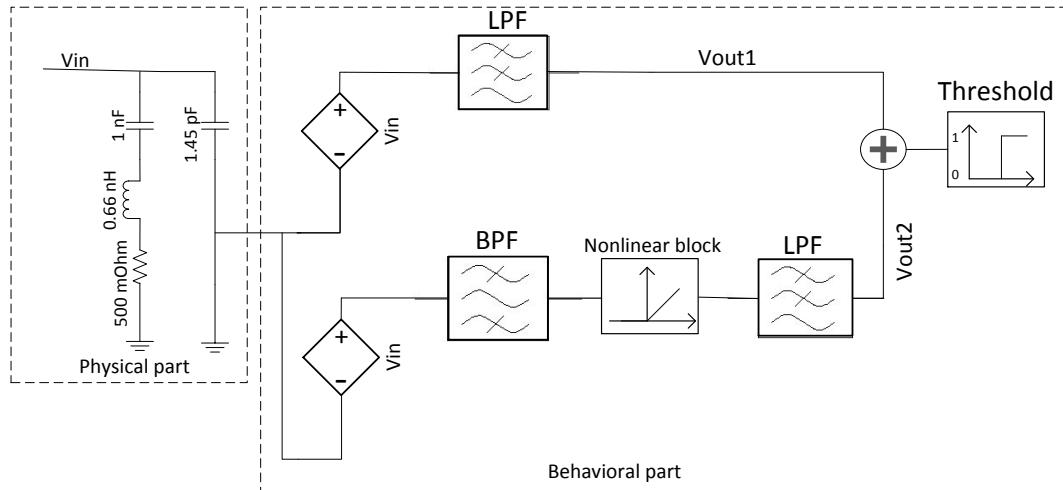
Figure 2. 14. IC behavioral model

3. ISO 10605 STANDARD SETUP

ISO 10605 is a standard test method for electrical disturbances from electrostatic discharge for road vehicles. The diagram of the test setup according to the standard is shown in Figure 3.1. The coupling strip and the coupling platform are located at 5 cm distance above the ground plane. There are direct discharge places, which are the three islands and the platform. The multi-wire harness (two parallel or twisted wires in our case) runs on top of the metal strip and is connected to the equipment under test (EUT – electronic module) placed on the platform. The PCB described in sec. II was used as the EUT. One wire of the harness was connected to the PCB ground, while another wire was connected to the IC clock pin. The ESD gun is discharged into indicated discharge points and the failures of the EUT (flip-flop triggering) are recorded.
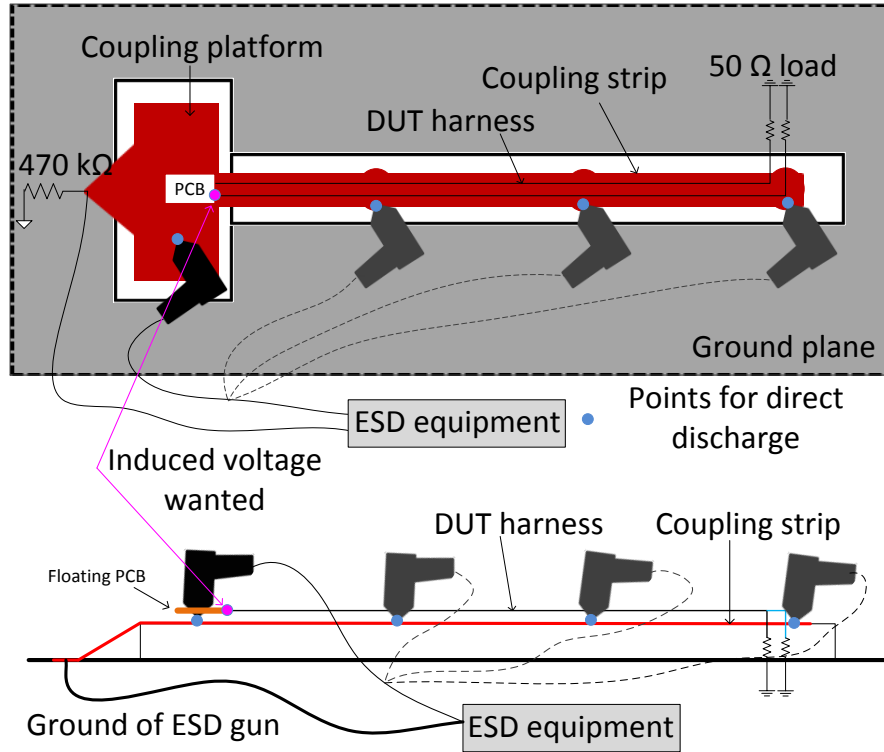
Figure 3.1. ISO 10605 Standard ESD Test Setup (top view and side view)

4. MEASUREMENT SETUP AND VALIDATION

In order to validate the IC model in the ISO 10605 standard setup, the
measurement setup was built as shown in Figure 4.1, 4.2, 4.3, 4.4, 4.5. It is possible to
perform measurements using an ESD gun or a cable loop that driven by a VNA or a TLP
generator (shown on the Figure 4.2). The later was done for the validation purposes.

Since the passive probe is added at the PCB side to measure the induced voltage,
the common mode impedance attached to the probe affects the grounding of the PCB
which is undesirable. In order to avoid this, semi-rigid coaxial cables, rather than wires
were used to construct the harness. The outer conductors of the cables model the harness
wired, while the inner conductors are used to monitor the voltages at the IC pins. At the
far end the outer conductors were terminated with 50 Ohm resistors. The schematic of the
harness connection description is shown in Figure 4.3.
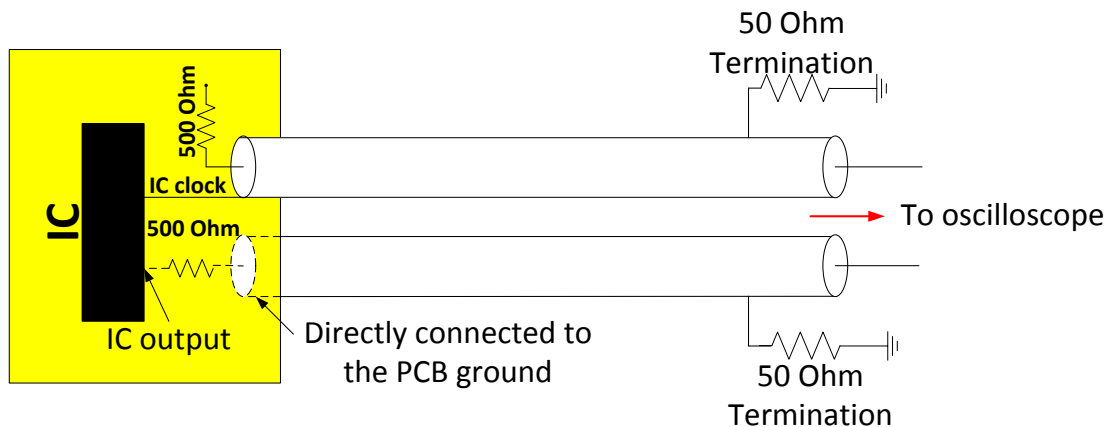
Figure 4.1. The schematic of the harness connection description
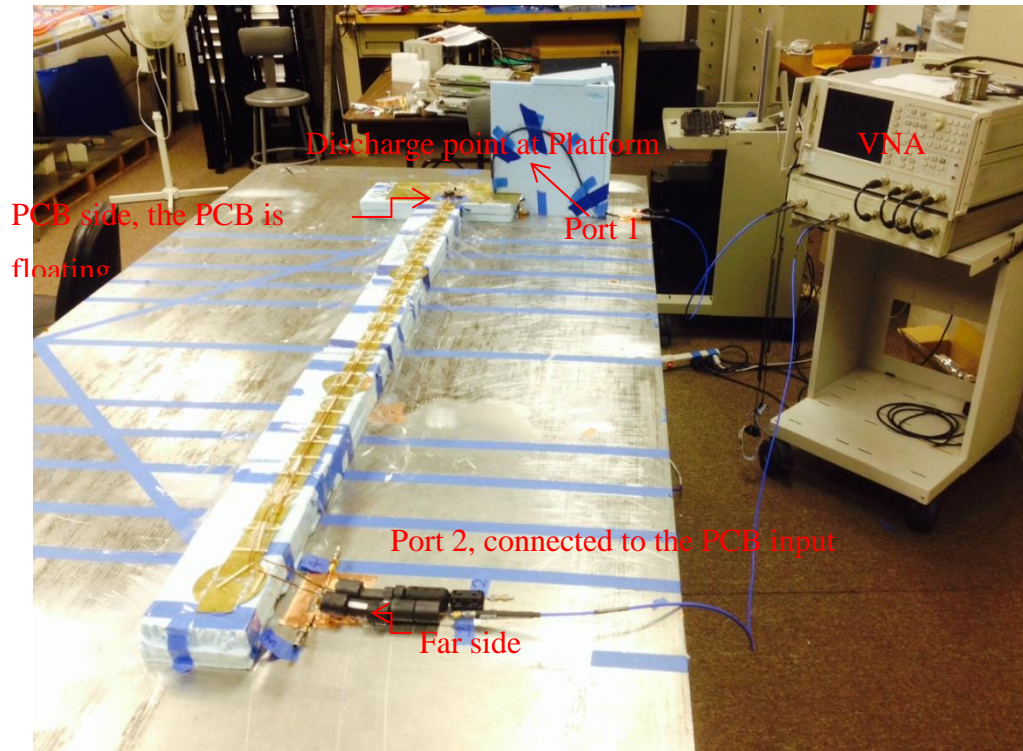
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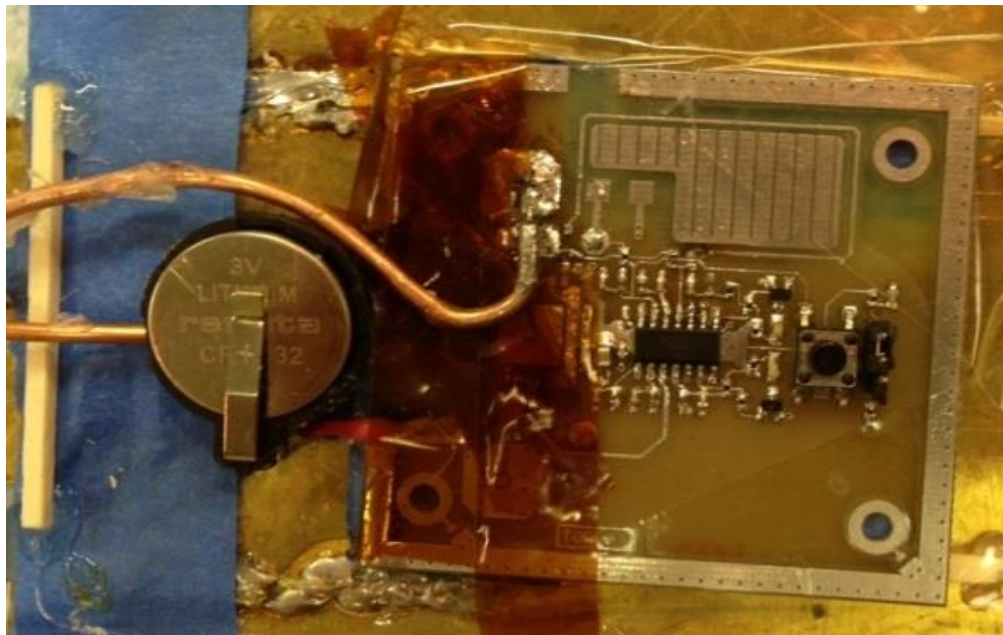
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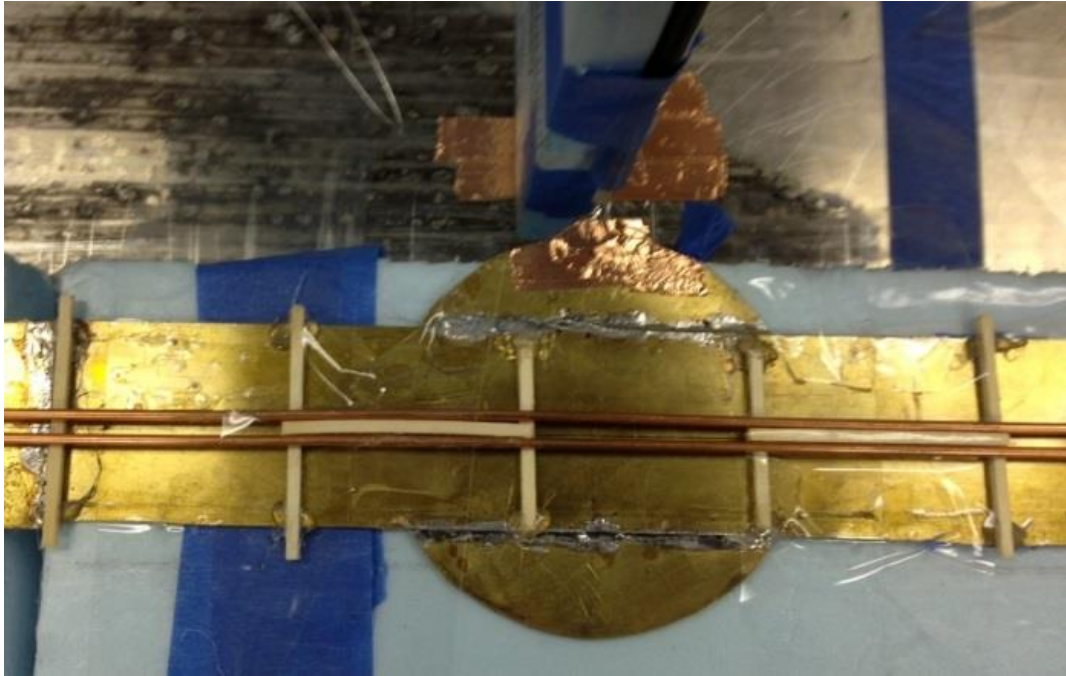
Figure 4.4. Discharge point (Island 2)
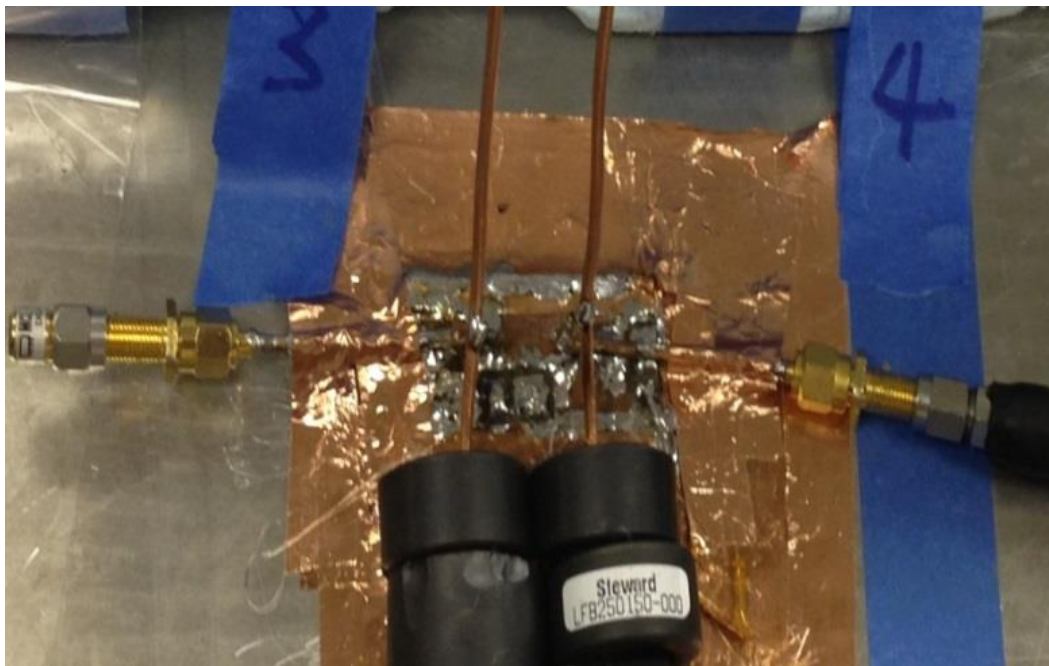
Figure 4.5. Far side

To validate the measurement setup, the full wave model with the discharge loop was created in CST microwave studio which was shown in Figure 4.6. One port was set at the input of the discharging loop and another port was set at the PCB input side.
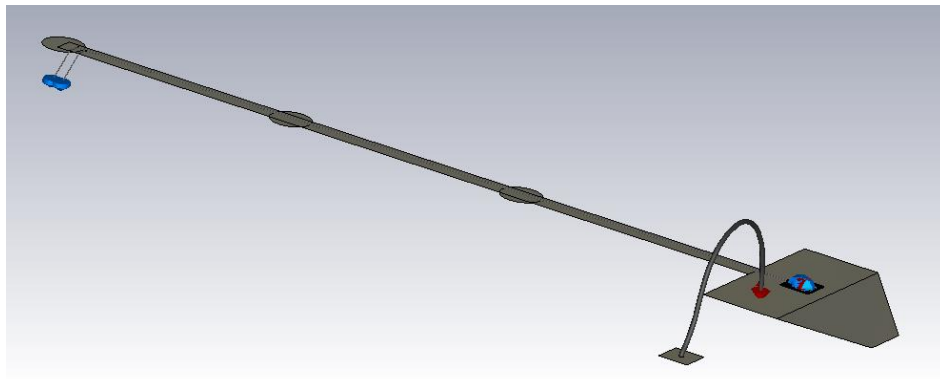
Figure 4.6. ISO 10605 Standard ESD Test Setup model when discharging at platform with a discharging loop

After the S-parameter of this block was simulated, the measured S-parameter was compared with the simulated results. The agreement between the simulation and measurement is good below 400 MHz which can be seen in Figure 4.7. At higher frequencies the difference increases, however, since the energy of the ESD signal is relatively low in this frequency range, it did not result in large differences in time domain waveforms (as shown below in Figure 4.10).
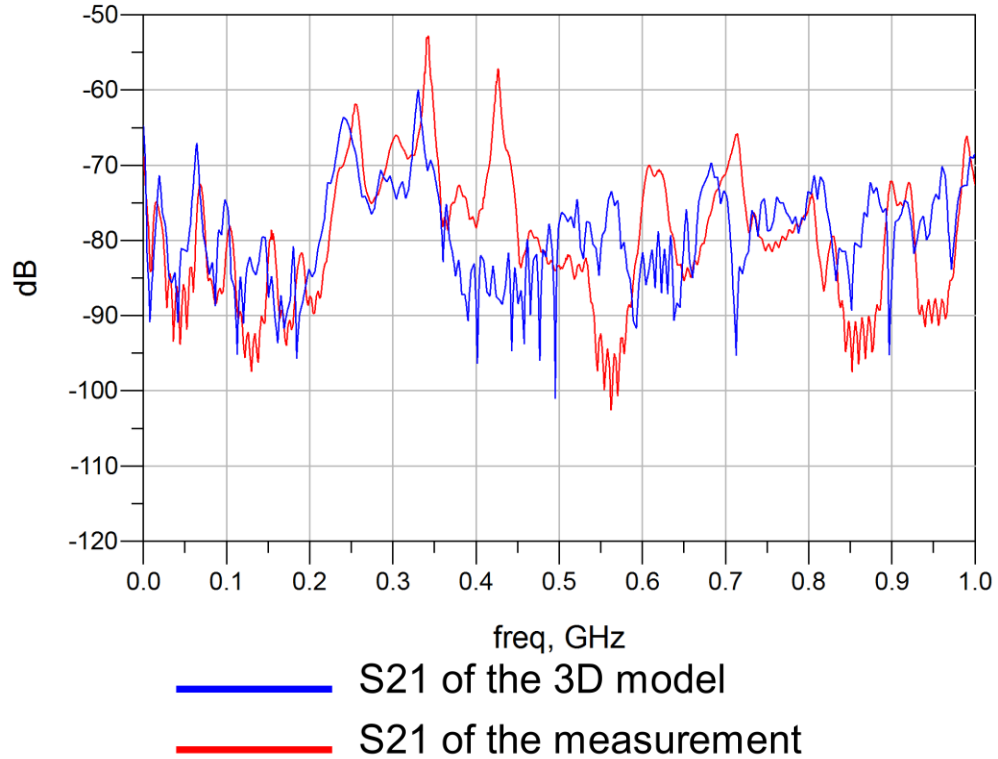
Figure 4.7. Simulated S21 compared with the measured data

After the setup was validated, the discharge loop was removed and the ESD gun was used which according to the ISO 10605 standard.

An illustration of the full model of this setup is shown in Figure 4.8. In this 3D full wave model, the three discharging islands and the platform were included, along with the ESD gun model developed earlier. In the full wave model, port 1 is the internal ESD gun source, and ports 2 and 3 are defined between the harness wires and the metal plate of the size of the EUT PCB (this allowed to exclude the PCB layout from the ISO setup model and solve it separately). S-parameter matrix of the setup was calculated using the time domain CST solver.
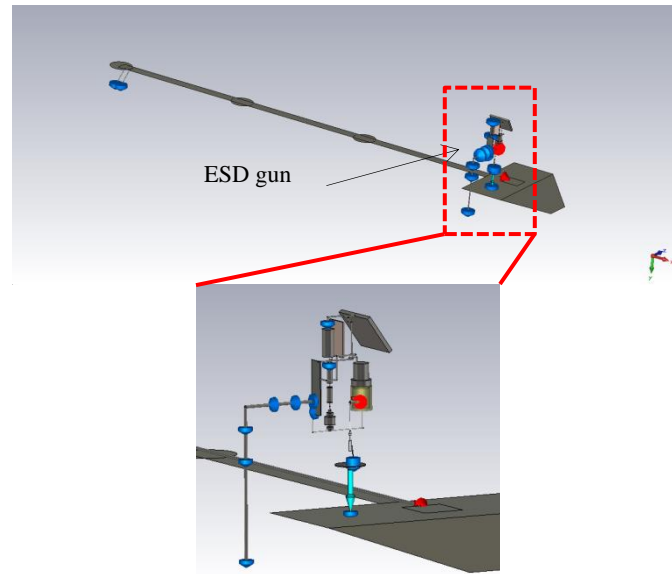
Figure 4.8. ISO 10605 Standard ESD Test Setup model when discharging at platform

Along with the ISO setup, a model of the PCB, including the layout geometry, was created and solved in terms of S-parameters using the CST time domain solver. In order to predict the IC triggering, all three models are combined as shown in Figure 4.9.

The quality of the model can be assessed by two criteria: 1) by comparing the calculated IC input voltage to the measured one (weaker criterion), and 2) by comparing the calculated ESD gun discharge level which caused the IC triggering (failure) to the measured one (stronger criterion).

The comparison between the simulated voltage at the input port and the measured one with the discharge at the Island 2 is shown in Figure 4.10. As can be seen, the simulated waveforms are in good agreement in with the measurement (17% difference at peak level). This result validates the linear part of the model (ISO setup + PCB + IC input

impedance). The accuracy is also comparable for the other discharging places (remaining two islands and the platform).
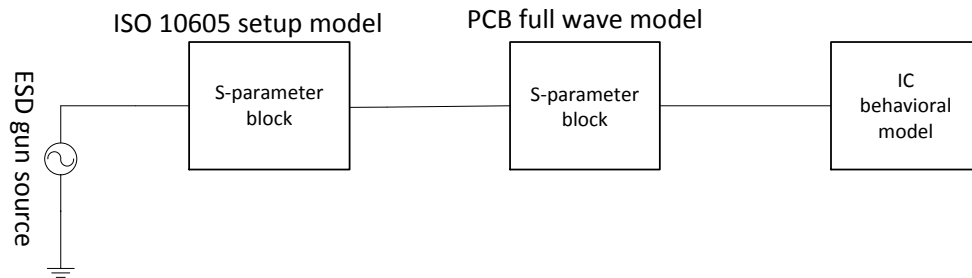
Figure 4.9. Full model to predict the triggering discharging level

The predicted and actual ESD gun discharge voltages corresponding to IC triggering (failure) are listed in the Table 4.1. As we can find the predicted triggering discharging levels have good agreement with the measurement.
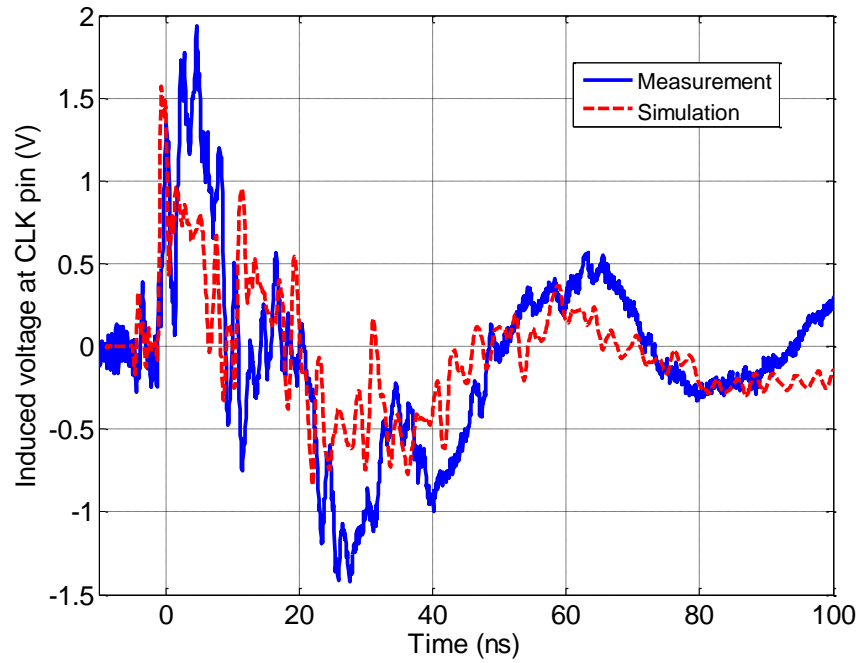
Figure 4.10. Comparison between measured and simulated input waveforms when discharging at island 2

Table 4.1. Measured and Simulated Results Comparison when Discharging at Different Places for 18 MHz IC

18 MHz IC Triggering Level Prediction (kV)				
Discharging Location	**Island 1**	**Island 2**	**Island 3**	**Platform**
Measured	-1.2 to -1.3	-1.6 to -1.7	-2.2 to -2.3	-5.5 to-5.6
Simulated	-1.51	-1.95	-2.2	-5.5

The largest error is about 17% which occurred when discharging at island 1. The errors at other places are much smaller.

5. TWISTED PAIR HARNESS CASE VALIDATION

In the actual vehicle applications, the harnesses are almost always are created using twisted pairs. In order to validate the IC modeling methodology in the twisted pair case, the harness in the measurement was replace with twisted pair as can be seen in Figure 5.1.
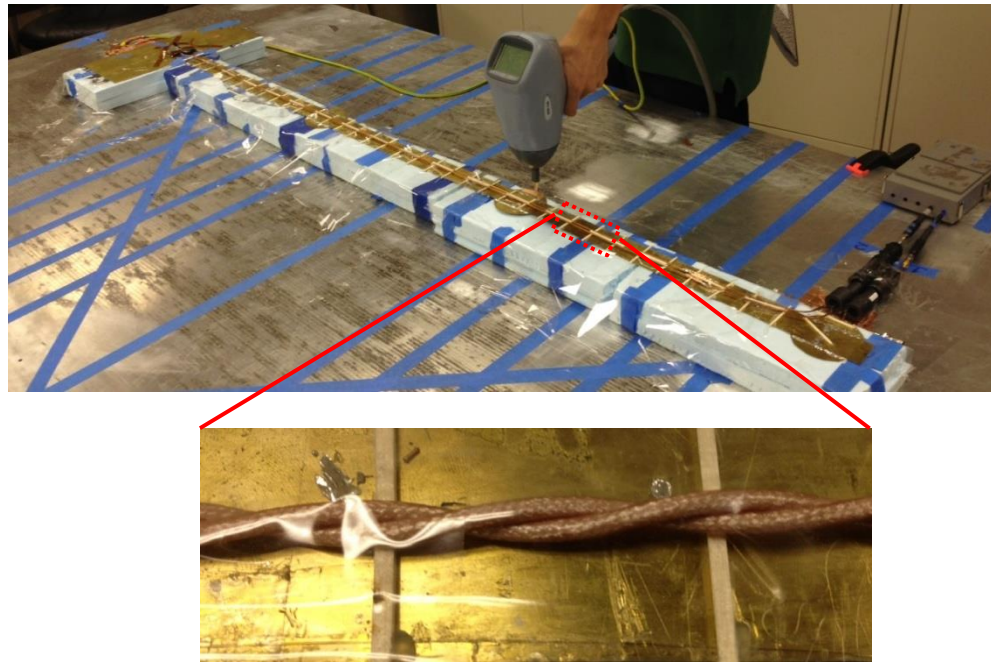
Figure 5. 1. ISO 10605 Standard ESD Test Setup with Twisted Pair

The full wave model was again created for twisted pair. Since the twisted pair geometry is intrinsically difficult to discretize with a rectangular grid used by the CST

time domain solver, the CST cable studio [11] was used for modeling, which eliminated

the need to create a 3D model for the harness as shown in Figure 5.2.
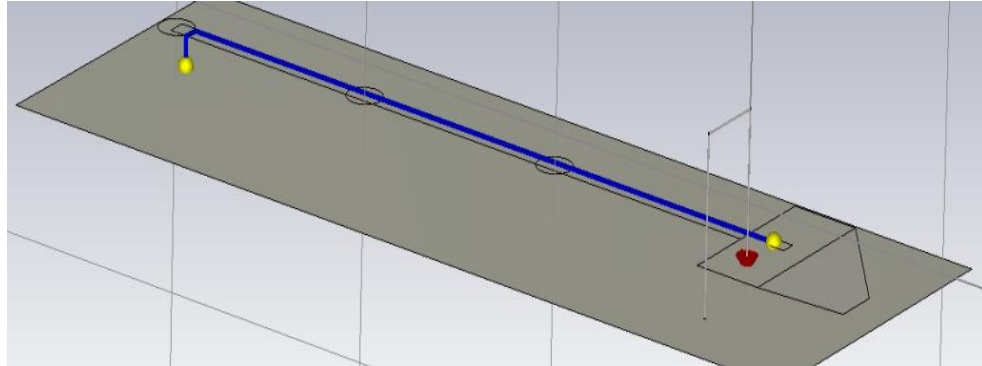
Figure 5. 2. ISO 10605 Standard ESD Test Setup model for Twisted Pair

A cable studio model did not allow to reach the mesh count needed to discretize

the full-wave model of the ESD gun (for technical reasons), so the gun in the model was

replaced by a simple loop driven by the source, representing a recorded ESD-gun

discharge current which is shown in Figure 5.3.

The predicted and actual ESD gun discharge voltages corresponding to IC

triggering (failure) in the twisted pair case are listed in the Table 5.1.
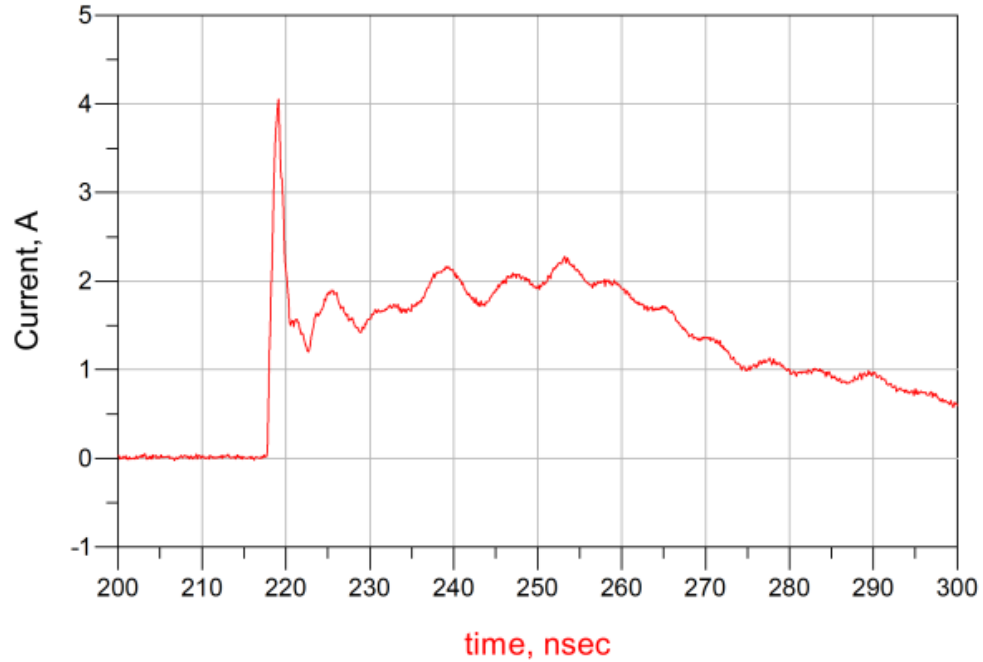
Figure 5. 3. Current Source of the ESD gun when discharge at 1 kV

Table 5.1. Triggering Discharging Level Comparison for Twisted Pair

18 MHz IC Triggering Level Prediction (kV)				
Discharging Location	Island 1	Island 2	Island 3	Platform
Measured	-1.4 to -1.5	-1.6 to -1.7	-3.2 to -3.3	-5.0 to-5.1
Simulated	-1.8	-2.2	-4.1	-6.4

The largest observed error is about 30% which occurred when discharging at island 2.

6. CONCLUSION

In this paper, the ESD immunity behavior of an 18 MHz D flip-flop used in ISO 10605 standard is investigated. The test IC was characterized by direct injection of particular waveforms, and a behavioral model was created. The whole model combining the full wave model of ISO 10605 setup and PCB with the behavioral model of the IC was used created to predict the induced voltage at the clock pin and the IC triggering. The simulated waveforms agreed well with the measurement and the failure discharging level of the ESD gun can also be predicted. The largest errors are about 20% when the harness is parallel wires. The largest error for the predicted triggering level when the harness is twisted pair is about 30%.

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II. MAXIMUM RADIATED EMISSIONS EVALUATION FOR THE HEATSINK/IC STRUCTURE USING THE MEASURED NEAR ELECTRICAL FIELD UP TO 40 GHZ

Guangyao Shen, *Student Member, IEEE*, Sen Yang, Jingdong Sun, David Pommerenke, *Senior Member, IEEE*, and Victor Khilkevich, *Member, IEEE*

ABSTRACT—Creating an equivalent field source is an efficient method to predict the radiated emissions. In this paper, the maximized radiated emissions of the heat-sink/IC structure are predicted up to 40 GHz by creating an equivalent source using the measured electrical field in the gap between the heatsink and ICs. The electric field is detected by an E-field probe made of an open coaxial cable coated with absorbing material. A numerical model is built in CST microwave studio to obtain the maximized radiated field with the measured field used as a source to excite the heat-sink model. The evaluated maximized radiated field is in good agreement with the measured value; the error is within 6 dB.

Index Terms—Field transformation; equivalent principle; probe calibration; maximized radiated field.

1. INTRODUCTION

The heat sinks are a common method to improve the heat dissipation of digital ICs. At the same time, the heat-sinks are known to be EMI sources [1].

Many articles have been published to model the radiated emissions of the heatsinks [1]-[6]. In [1] and [5], full wave modelling was used to model the radiated emissions of the heatsink. In [6] the heatsink was modelled as a superposition of a patch antenna and a fat monopole and then the worst case maximum radiated field was obtained. The full-wave methods are generally highly accurate, but they require information about the source which is usually not available. The worst case estimations often are too pessimistic.

Another approach is to create the equivalent source using the Huygens equivalent and perform a near field to far field transformation [7]-[9]. Application of the Huygens principle implies measuring tangential components of the EM field on a surface enclosing the source of EMI [10]. In [11] the near field was obtained on the surface completely enclosing the radiation structure. However in the case of the heatsink which is shown in Figure 1.1, the measurement needs to be performed over both horizontal and vertical planes, which is difficult to organize.

In this paper, an alternative method of measuring only the vertical component of the electric field in the gap between the heat sink and the ground plane (Figure 1.1 (b)) is proposed, which greatly simplifies the measurement process. The maximum radiated field is evaluated by the numerical model of the heatsink when it is driven by the measured near electric field source at the gap.

"Box"   "Gap"

(a)   (b)

Figure 1.1. Two methods to do field transformation

The presented work had two main objectives: 1) development of a simple E field probe that can work up to 40 GHz; and 2) using the detected near electric field to create an equivalent source and perform the field transformation.

The structure of the article is the following. In section II, the E field probe structure and calibration method are given. In section III, the near electric field measurement and transformation techniques are presented. The measurement setup for the maximized far field measurement and validation of the predicted values are introduced in Section IV. In Section V the entire procedure is applied to the active EMI sources (FPGA and clock ICs).

2. ELECTRICAL FIELD PROBE AND PROBE CALIBRATION

Probably the simplest way to detect the electromagnetic field is to used and open coaxial cable. The cable essentially forms a highly asymmetrical dipole antenna, with strong current on the outer surface of the cable shields. In the antenna design this current is usually suppressed by baluns or other similar devices [12]. Another way to eliminate the unwanted common mode current is to use a differential probe design [13]. Both methods are not very suitable for heat sink measurement. The balancing devices are difficult to build (especially the broadband ones), and the symmetrical differential E-field probes are not suitable to measure the fields close to the metallic ground planes. Instead of this in the proposed design, the common mode current is suppressed by applying a flexible electromagnetic absorber (WX-A020) [14] to the coaxial cable as illustrated in Figure 2.1.

Figure 2.1. E-field probe

The probe is calibrated using a combination of measurement and simulation. For the calibration a special structure containing a heat-sink driven by the coaxial cable was built (Figure 2.2).
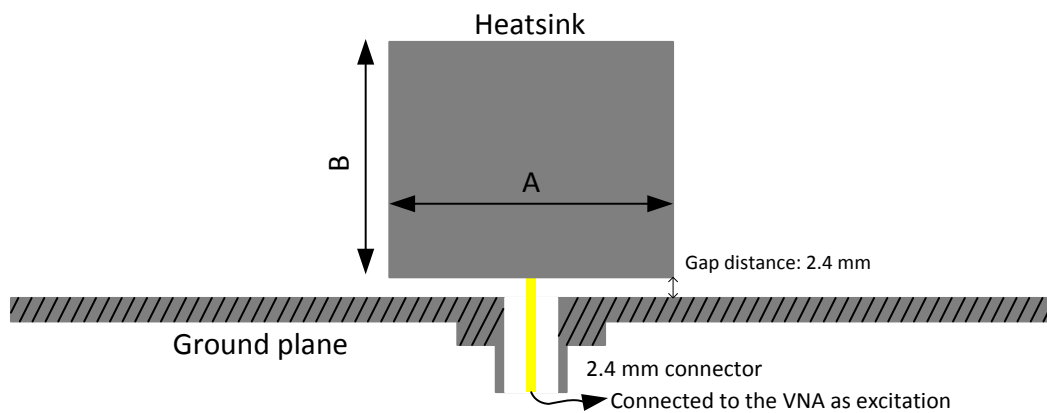
Figure 2.2. Diagram of the setup at the excitation of the heatsink

Two heat sinks were used for the calibration (heat sink 1 A=15 mm, B=25 mm; and heat sink 2 A=27 mm, B=25 mm).

The probe tip height over the ground plane and the distance between the probe and the heatsink were kept the same during the calibration and the DUT measurement (1 mm and 2 mm respectively). Figure 2.3 illustrates the process of the probe calibration.

The gap between the probe and
heat sink is around 2 mm.

Heat sink   Probe   VNA

Heat sink excitation
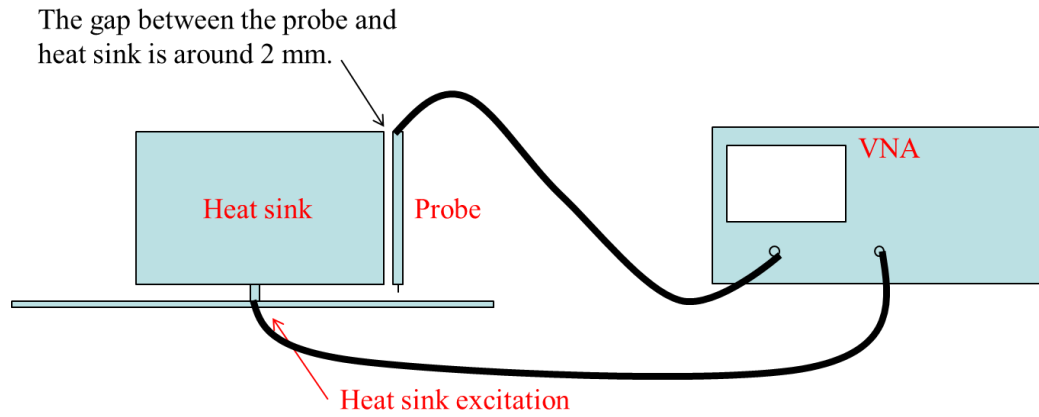
Figure 2.3. Calibration setup

Assuming the output voltage of the probe is proportional to the vertical component of the E-field in the gap between the heat sink and the ground plane, the probe factor can be defined as

$$A = E_z^c / V_{out} \tag{1}$$

The unknown E_z^c field at the gap across the position of the probe is obtained by the full-wave simulation of the heatsink (the model corresponds to the Figure 2.3).

Assuming, the probe load is non-reflective, the transmission coefficient from the heatsink

port to the probe output can be written as

$$S_{21}^{c} = \frac{V_{out}}{V_{inc}} \tag{2}$$

therefore the probe factor is calculated as

$$A = E_{z}^{c} / (S_{21}^{c} V_{inc}) \tag{3}$$

where V_{out} is the output voltage of the probe and V_{inc} is the incident voltage used in the

full-wave simulation.

The probe factor calculated according to (1) is in general dependent on the

position of the probe along the heat sink side. To simplify the data processing the

averaged probe factor was calculated by averaging A over many positions of the probe and smoothing the resulting curve as shown in Figure 2.4. The difference between the averaged probe factors obtained using the heat sinks 1 and 2 (see Figure 2.4) is not more than 3 dB, which is accurate enough for many applications and validates the proposed calibration procedure.
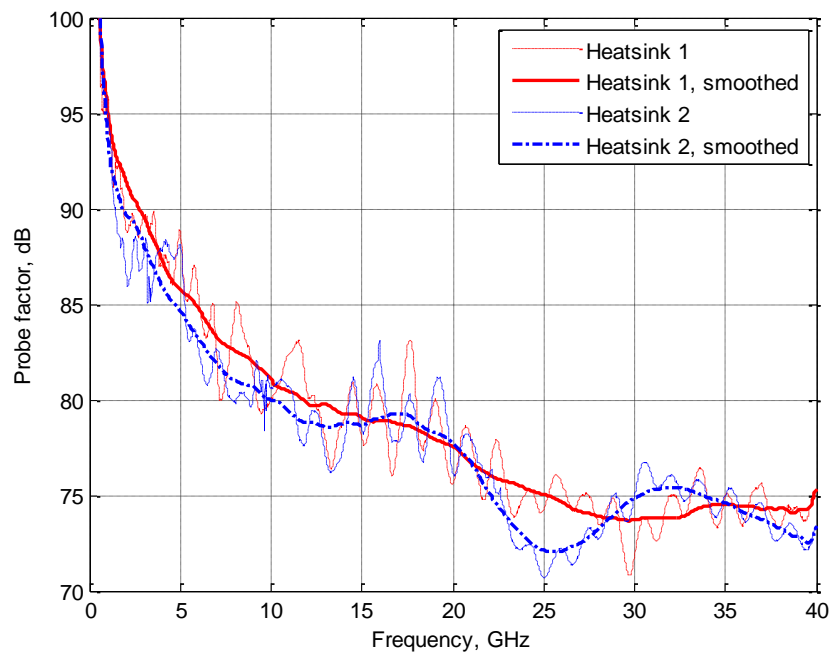
Figure 2.4. Probe factor comparison

3. NEAR FIELD TO FAR FIELD TRANSFORMATION

The near field generated by the heatsink was measured as shown in Figure 3.1. The probe was mounted on the manipulator with three degrees of freedom, allowing maintaining fixed elevation of the probe tip over the ground plane and the gap between the probe and the heatsink while allowing moving the probe parallel to the heat sink side.
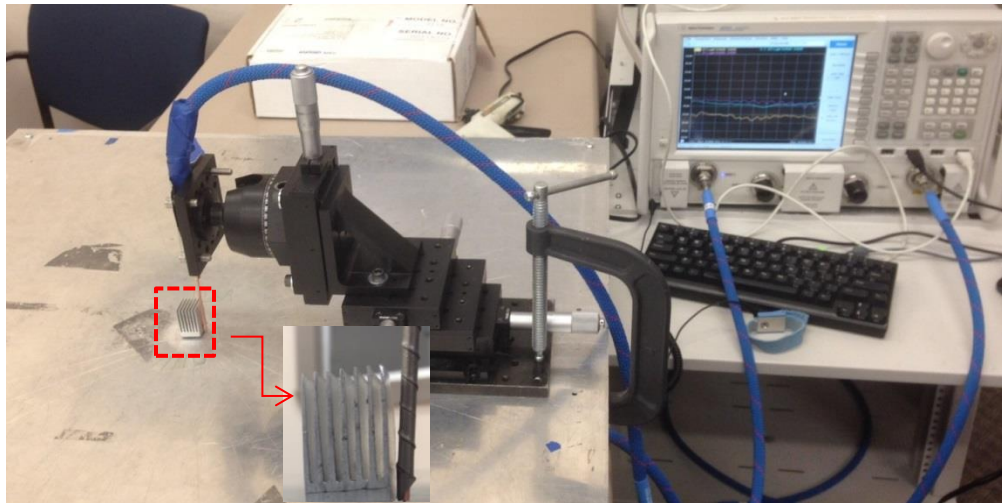
Figure 3.1.Near field scanning setup

The measured field is used to construct the near-field source in CST studio. Since only the tangential electric field components were measured, the inner volume of the source was filled by the PEC material to force the EM solver to calculate the missing

tangential magnetic field components. The model in CST microwave studio is shown in

Figure 3.2. The maximum far-field was obtained using the CST time domain solver.

The phase of the electric field at the gap between the heatsink and ground plane is

easily measured in the VNA driven case. However, in the actual IC/Heatsink

measurement performed using a spectrum analyzer, the phase is unavailable. To

investigate the impact of the NF source phase on the accuracy, two versions of the near

field sources were created – with and without the phase information.
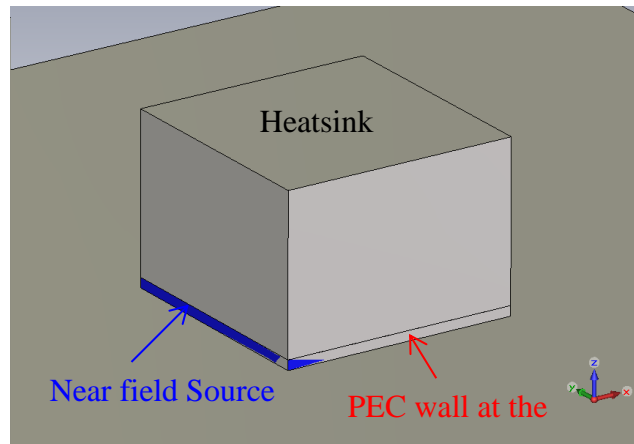
Figure 3.2. Field transformation model in CST

4. MAXIMUM FAR FIELD MEASUREMENT SETUP AND VALIDATION

The predicted EMI figure was validated against 1) the full-wave simulation model; 2) worst-case prediction according to [6] with conversion of the measured electric field to the voltage between the heat sink and the ground plane; and 3) measurement.

To measure the maximum far-field a special setup was built as shown in Figure 4.1. A horn antenna was attached to a plastic frame allowing scanning it with respect to the polar angle. The azimuthal scan was performed by rotating the heatsink on its axis.

Figure 4.1. Maximum far field measurement setup

To cover the frequency range from 1 to 40 GHz two broadband horn antennas were used: ETS Lindgren 3115 (1-18 GHz and ETS Lindgren 3117 (18-40 GHz).

The azimuth angle was varied by the step of 10 degrees, and for each value the polar scan was performed by slowly (relative to sweep time of the instrument) moving the frame around its axis, so that the maximum field value is recorded. The final result is obtained by selecting the maximum values over all azimuthal positions.

The maximized far field predicted by the near field source method was compared to the measurement along with the results of the 3D modeling ("CST port" curve) and the worst case estimation according to [6]. (Figure 4.2)
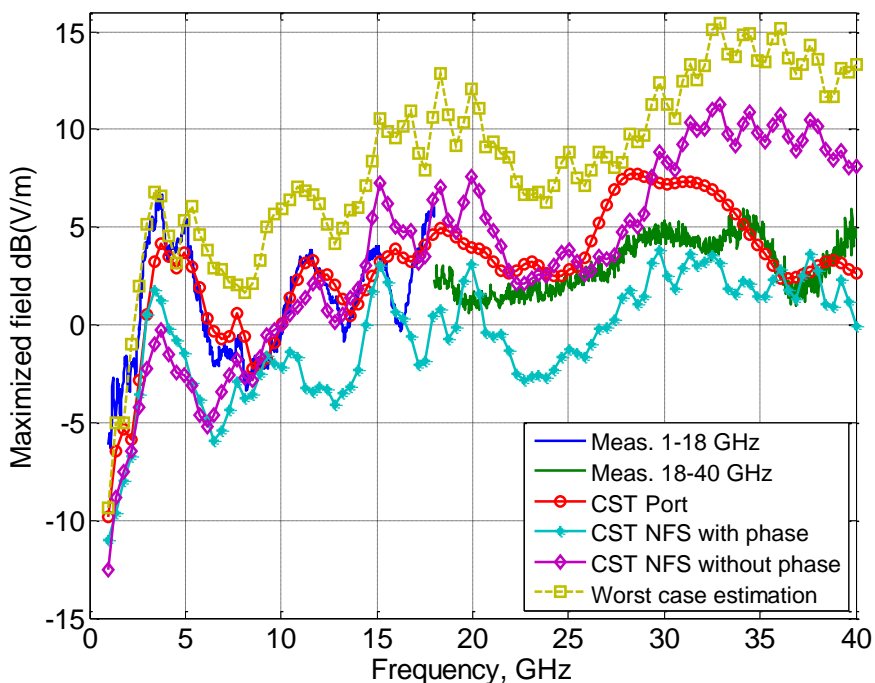
Figure 4.2.Transformation results comparison

The error curves are shown in Figure 4.3. For each of the predicted emission curves the absolute error was calculated taking the measured data as a reference. It can be seen that the best accuracy is achieved if the phase is included into the equivalent source. In this case the prediction accuracy is not worse than 7 dB in the entire frequency range. If the phase is not used, the accuracy is within 7 dB up to 18 GHz and is within 9 dB from 18 to 40 GHz.
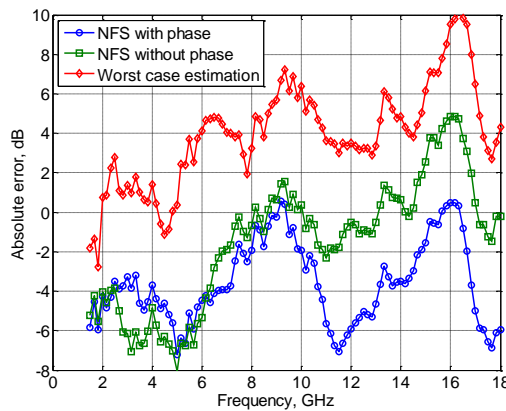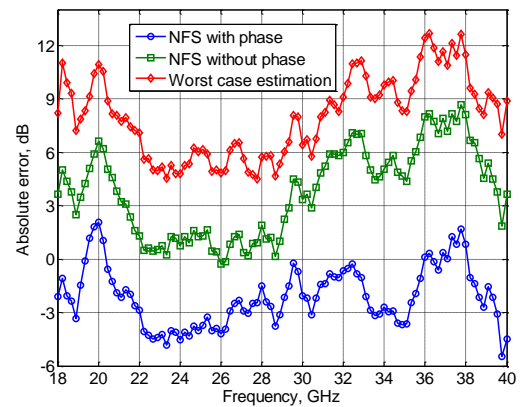
(a)   (b)

Figure 4.3. Absolute error for 1-18 GHz (a) and 18-40 GHz (b)

5. ACTIVE HARDWARE VALIDATION

In order to validate the prediction methodology in the actual hardware case, the method was tested on two devices. The first test vehicle is Cyclone III starter board (FPGA board). The FPGA running a dummy code implementing an array of adders was driven by the internal PLL clock with the frequency of 467.857 MHz. To simulate the heat sink, an aluminum block was placed above the IC (Figure 5.1).
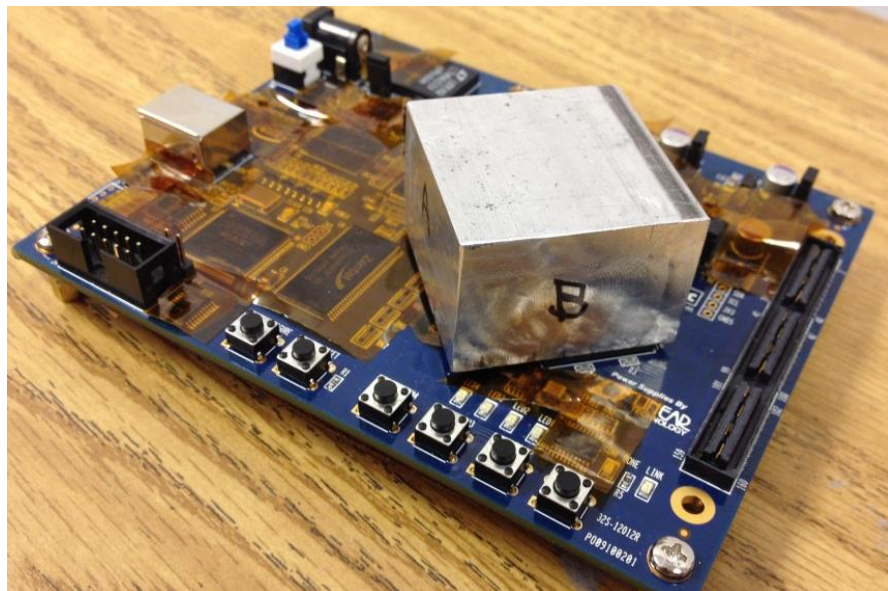
Figure 5.1. Cyclone III starter board for validation from low frequency part

The near field at the gap was measured by the Ez probe and a spectrum analyzer (i.e. only the magnitude is measured) and then transformed to the far-field as described

above. The far field for validation was measured in the setup shown in Figure 4.1. The

result of the transformation along with the worst case prediction results are shown in

Figure 5.2 (each marker represents the harmonic of the clock frequency). It can be seen

that the transformation result has a good agreement with the measurement as shown in

Figure 5.2. The error is within 5 dB for each harmonics. The frequency range (7.5 GHz)

was limited by the sensitivity of the far-field measurement.
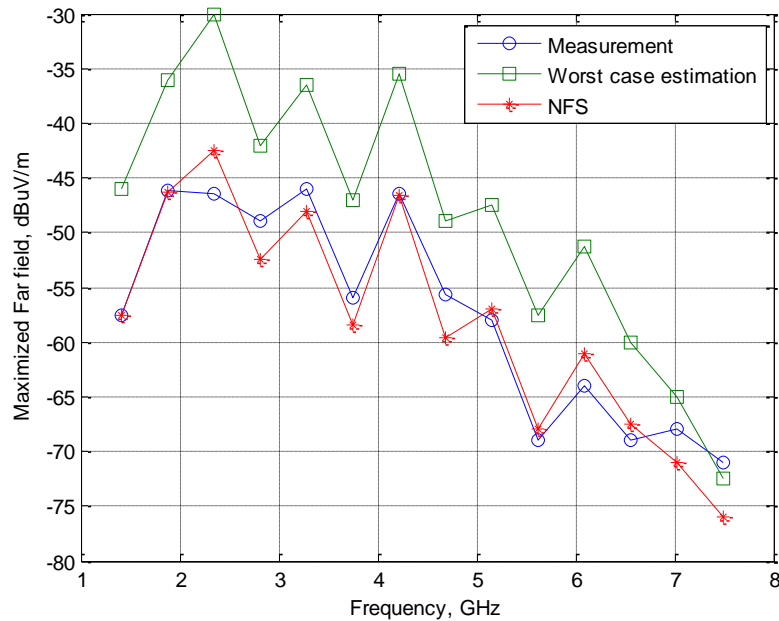
Figure 5.2. Transformation result comparison for Cyclone III starter board

In order to test the method at higher frequencies a clock 670 MHz clock IC (Figure 5.3) was also tested. This DUT allowed extending the frequency range up to 20 GHz.

Figure 5.3. Clock buffer IC board for validation

The near field at the gap was measured by the electrical field probe designed in Section I using a spectrum analyzer. The scanning results are illustrated by Figure 5.4 (only two frequencies are shown), with blue dots representing the probing locations. The field between the measured points was obtained by interpolation.
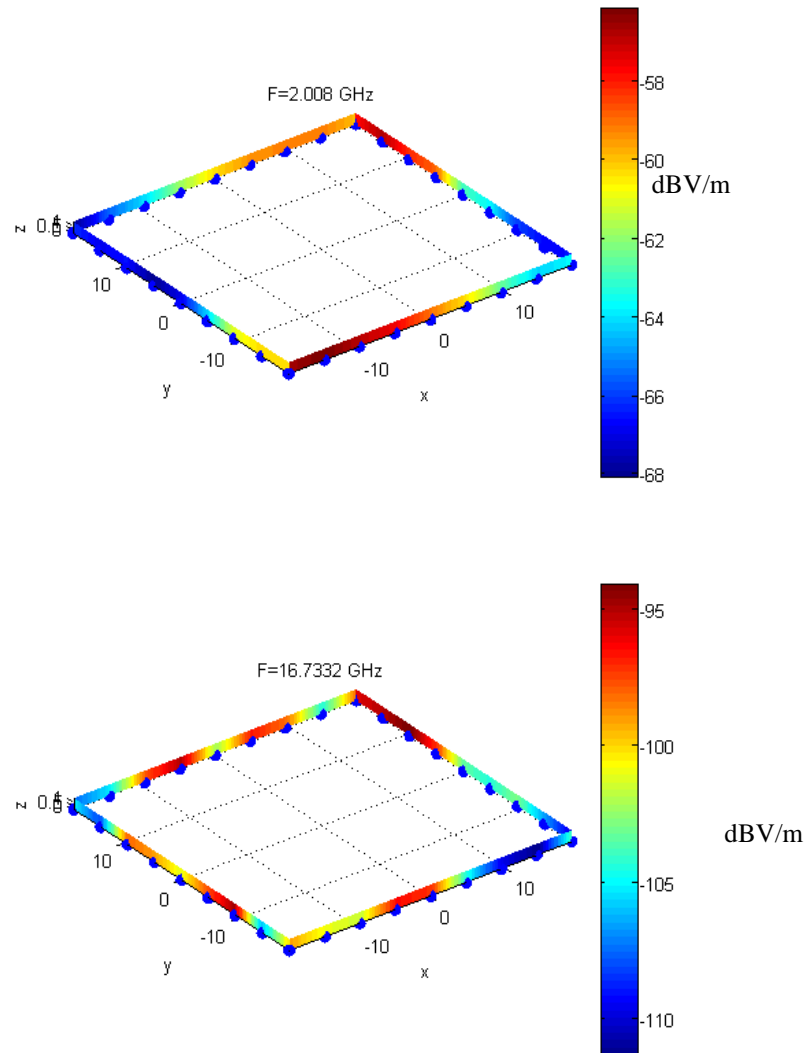
Figure 5.4.Near field 3D visualizations for two frequencies

The maximized far field was predicted by using the equivalent source created by the measured near field.

The errors of the maximized field transformation of heat sink/IC structure are within 6 dB except at four frequencies, where it reaches 8 and 10 dB. Overall the

transformation accuracy for the active DUTs agrees with the accuracy achieved in the

passive case with no phase information (Figure 5.5, 5.6).
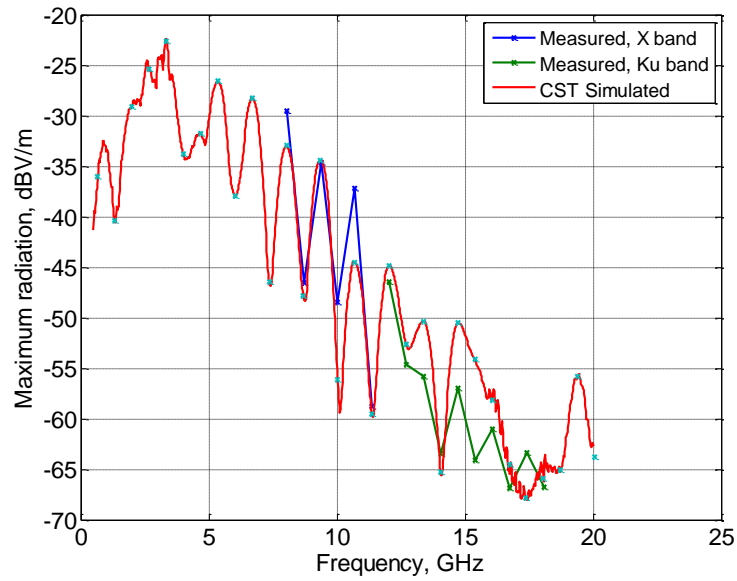
Figure 5.5.Transformation result comparison for the clock signal board
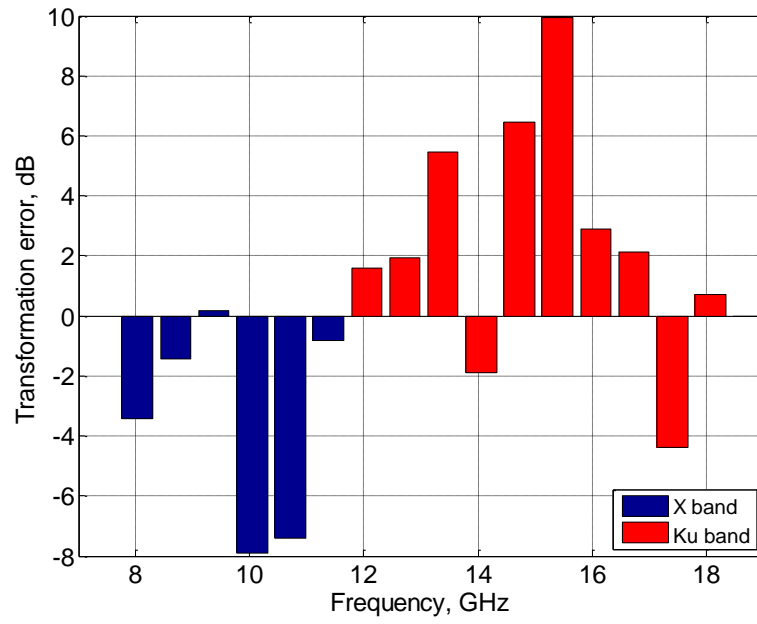
Figure 5.6. Absolute error for the Clock buffer IC board

6. CONCLUSION

In this paper, an E field probe was designed to detect the near field of the heatsink/IC structure in order to predict the maximized far field. The probe is operational up to 40 GHz. The proposed measurement/transformation technique is relatively simple to use and can provide accuracy of 6 dB up to 18 GHz and up to 9 dB from 18 to 40 GHz.

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III. TERMINAL MODELING OF DC-DC CONVERTERS WITH STOCHASTIC BEHAVIOR

Guangyao Shen, *Student Member, IEEE*, Satyajeet Shinde, Abhishek Patnaik, David Pommerenke, *Senior Member, IEEE*, and Victor Khilkevich, *Member, IEEE*

ABSTRACT—A terminal model is a common method to create equivalent models of DC-DC converters in order to predict conducted emissions. In this paper, a characterization method for converters with stochastic behavior is presented. The averaged and maximized spectrum of the measured voltages and currents are used to create the model. The phase information is obtained using a dedicated reference channel. After the equivalent source was determined, the actual induced noise voltage at the test load was compared to that predicted by the model with averaged and maximized spectrum to estimate its accuracy. The results indicate that the agreement with the direct measurement is within 5 dB up to 100 MHz when the load is within the characterization range.

Index Terms—Terminal model; DC-DC converter; stochastic behavior.

1. INTRODUCTION

DC-to-DC converters are widely used in vehicles as efficient power sources. Interference due to fast switching in the converters is one of the main conducted EMI problems associated with them [1]-[2]. Earlier work on the EMC performance of power electronic systems has tended to concentrate on switched mode power supplies [2]-[4].

A lot of work has been done to model the emissions of the converter system. In [4-9] time-domain EMI emission modeling has been used to characterize and model conducted EMI emissions sources, but this method needs to know the detailed structure of the converter system, which is not always possible. In [10], frequency-domain EMI emission modeling was used. The methods suffer from a lack of generality for practical design use in a converter system. The circuit-level models can be used [11]-[12]. However, in many cases the circuits of the converters are either not available, or too complex for simulation.

The terminal models based on the Thévenin or Norton equivalents were introduced as an equivalent to circuit models in [13]-[15]. The equivalent source models are created by attaching a number of loads to the terminals of interest to get the equivalent source EMF and its impedance by solving a system of linear equations [16]-[17]. However, all of these works assume that the signals are deterministic. This is not always the case in reality. For example, the switching cycle of the transistor may be not stable due to the generator instability, thermal effects, or the switching might be randomized intentionally. Because of this, there is a need to extend the terminal models to systems with stochastic behavior.

Various international standards [18]–[20] specify how conducted emission measurements should be performed. A configuration in Figure 1.1 based on [18] is used as the reference for the analysis presented here. But it is important to note that the work is not restricted to this particular arrangement or measurement method.

Typical Test Setup for Conducted Emissions Measurement
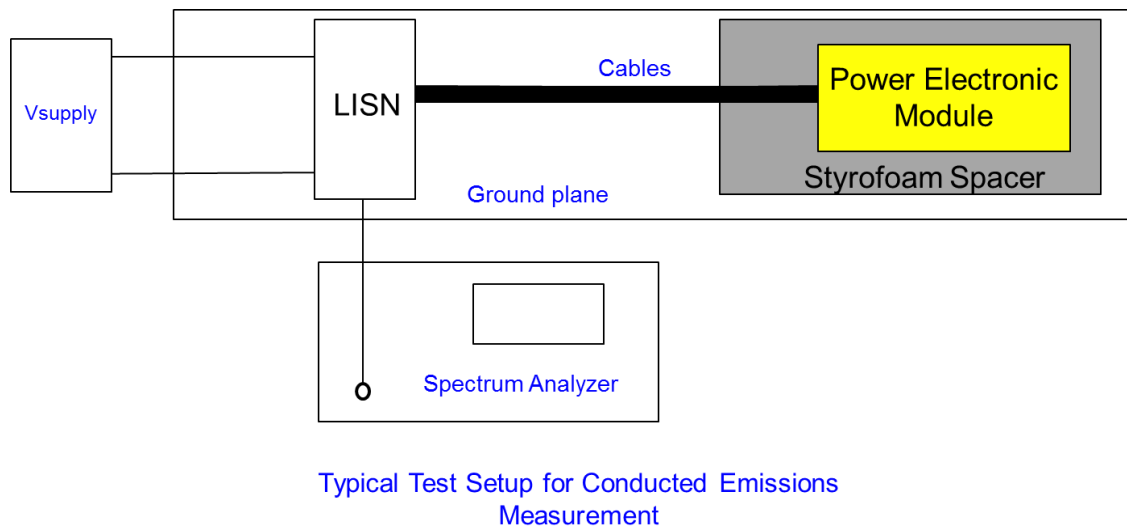
Figure 1.1.Typical measurement setup for conducted emission

In this paper a terminal model characterization method for converter system with stochastic behavior is proposed, which emphasizes ease of source characterization procedure and importance of the phase reference for converters with random signals. The focus is put on the terminal model characterization using time domain measurements.

The terminal model characterization method for the converter with stochastic behavior is based on the methodology presented in [16]-[17]. An associated method dealing with the random signal to obtain meaningful magnitude and phase is proposed. The full equivalent source model with EMF and source impedance is built. The predicted noise voltage and current levels are validated by the measurement.

2. TERMINAL MODEL CHARACTERIZATION METHODOLOGY

Figure 2.1 shows the diagram of the equivalent Thévenin model.

Figure 2.1. Equivalent terminal model of the EMI source

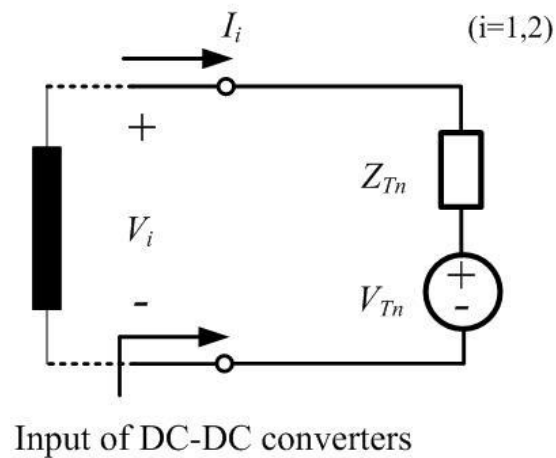The model in Figure 2.1 is characterized by two unknowns (internal impedance Ztn and source EMF Vtn) which can be found by measuring voltages and currents on two (unknown in general) loads attached to the source. This method can also be extended to a general case of n sources. The equations below [16] show how the equivalent source model is obtained in that case.

$$\begin{bmatrix} I_{11} & 1 & \cdots & 0 & 0 \\ I_{21} & 1 & & 0 & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & 0 & & I_{1n} & 1 \\ 0 & 0 & \cdots & I_{2n} & 1 \end{bmatrix} \begin{bmatrix} Z_{T1} \\ V_{T1} \\ \vdots \\ Z_{Tn} \\ V_{Tn} \end{bmatrix} = \begin{bmatrix} V_{11} \\ V_{21} \\ \vdots \\ V_{1n} \\ V_{2n} \end{bmatrix} \tag{1}$$

here the I_{ij} and V_{ij} are the characterization currents and voltages, where i is the index corresponding to a loading condition and j is index corresponding to a terminal. The V_{Tj} and Z_{Tj} are the equivalent source parameters for terminal j.

The measurements of voltages and currents are performed in time domain using a real-time scope, and are converted to frequency domain to formulate the equation (1) and solve it relative to Z_{Tj} and V_{Tj}.

3. CHARACTERIZATION BOARD DESIGN

In order to create the equivalent source model, a characterization board was designed [21].

3.1. PCB DESCRIPTION

The PCB was designed keeping in mind several requirements: 1) multiple load conditions for characterization; 2) on-board voltage probes; 3) on-board current probes; 4) electronic load switching.

A diagram of the characterization board with 2 input channels based on these requirements is shown Figure 3.1.
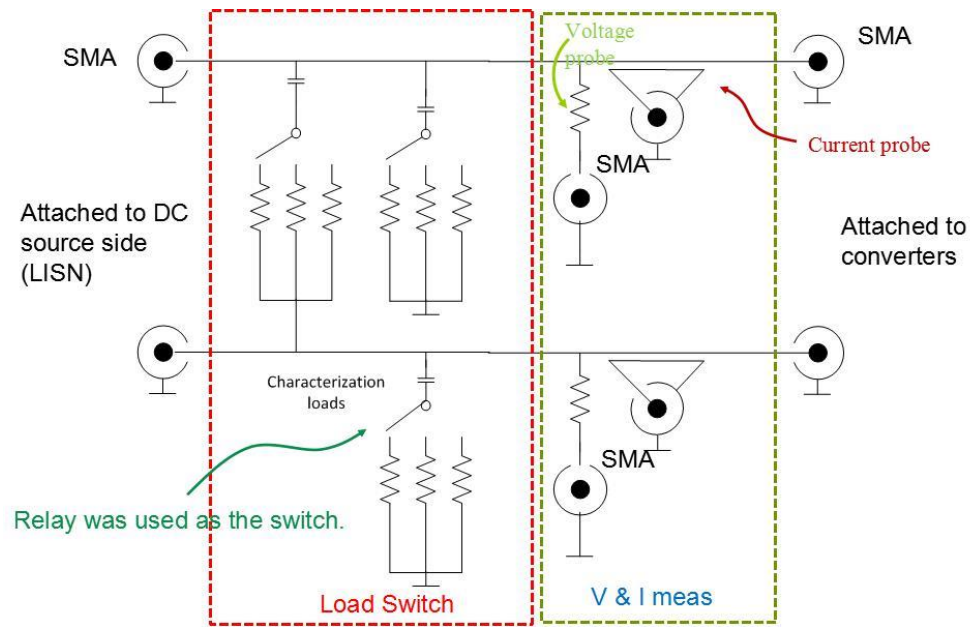

Figure 3.1. Schematic for the characterization board

The PCB has two parts: switched loads and measurement probes. Each channel has a set of switchable loads to the ground, but there is also a set of loads connected between the channels to allow characterizing mutually coupled converters. Each switchable load has a DC block capacitor preventing the influence of the loads on the DC current of the converts. The relays are used as switches for measurement automation.

For the voltage measurement, a 1 kOhm passive probe was used, i.e. the voltage at the output of the voltage divider formed by the on board 1 kOhm resistor and a 50 Ohm port of the instrument is measured and then scaled by the division factor to obtain the actual voltage at the measurement point. Since the resistor divider attenuates the signal by the factor of 21, a low noise amplifier is added to the voltage probe channel to compensate for the loss.

For the current measurement, a current probe was designed. The probe had to provide high sensitivity and accuracy in the frequency range from 100 kHz to 100 MHz with minimum parasitic capacitive coupling.

Taken these requirements into account, the current probe was designed as shown in Figure 3.2. The probe is essentially a transformer, consisting of a toroidal ferrite core with the primary winding formed by a wire soldered to the gap in the trace on the characterization PCB, and the secondary winding made of a semi-rigid cable as shown in Figure 3.2.

A resistor was added into the secondary winding as illustrated by Figure 3.2 to expand the bandwidth of the probe at the expense of its sensitivity. The transfer impedance of the probe (measured using a VNA and a 50 Ohm trace as demonstrated in Figure 3.3) is shown in Figure 3.4 for three values of the resistor.
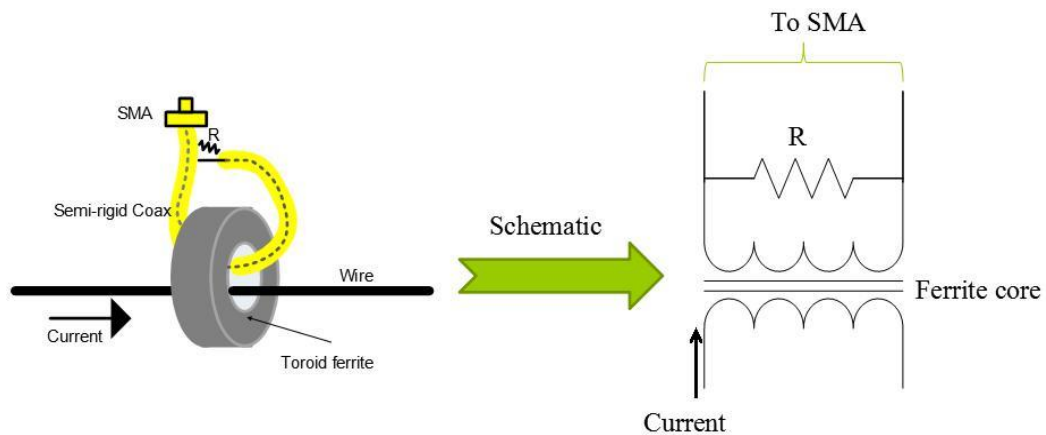
Figure 3.2. Current probe design
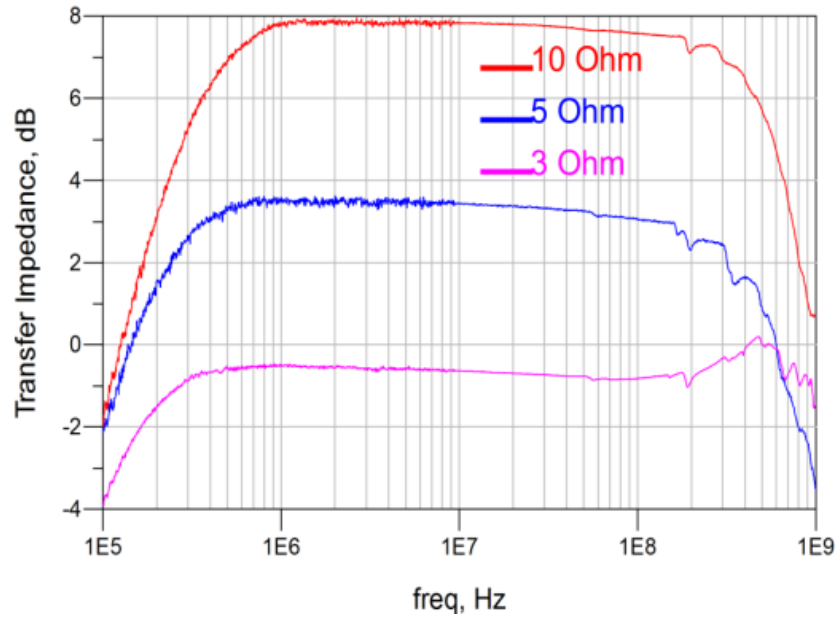

Figure 3.3. Current probe characterization

Figure 3.4. Transfer impedance of the current probe for three values of the resistor in the secondary winding

4. CHARACTERIZED SIGNAL CHARACTERISTICS

Conventional terminal models assume deterministic signals [16]-[17], however, many DC-DC converters demonstrate random behavior. Figure 4.1 shows a typical spectrum of the noise voltage produced by a DC-DC converter and measured by a spectrum analyzer.
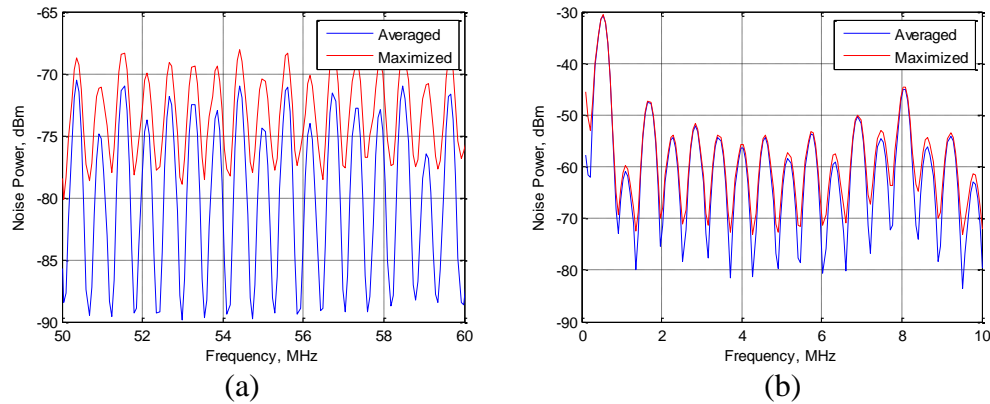
Figure 4.1. Averaged magnitude and Maximized magnitude for the output of voltage probe measured by Spectrum analyzer with IF bandwidth= 200 kHz, (a) 0 ~ 10 MHz, (b) 50 ~ 60 MHz

It can be seen that at low frequency range, the averaged and maximized magnitude are almost exactly the same, which means that the frequency components are stable. However, as the frequency goes higher, the averaged and maximized magnitudes start to diverge which indicates the signal randomness.

5. TERMINAL MODEL CHARACTERIZATION

In order to deal with the random signals, the three channel measurement was introduced, including two channels for the voltage and current measurement, and the third channel for the reference signal measurement. The measurement setup and procedure is shown in Figure 5.1.

For the characterization, two loads on the board were chosen (with nominal values of 13 and 250 Ohms). The characterization board is directly connected to the converter and the voltages and currents are measured using a real-time oscilloscope. A LISN is added between the characterization board and the DC source to eliminate the influence of the source and power wires on the impedance of the characterization loads.

The phase reference signal is measured either by direct probing of the transistor gate signal or by near-field field probe placed close to the transistor.
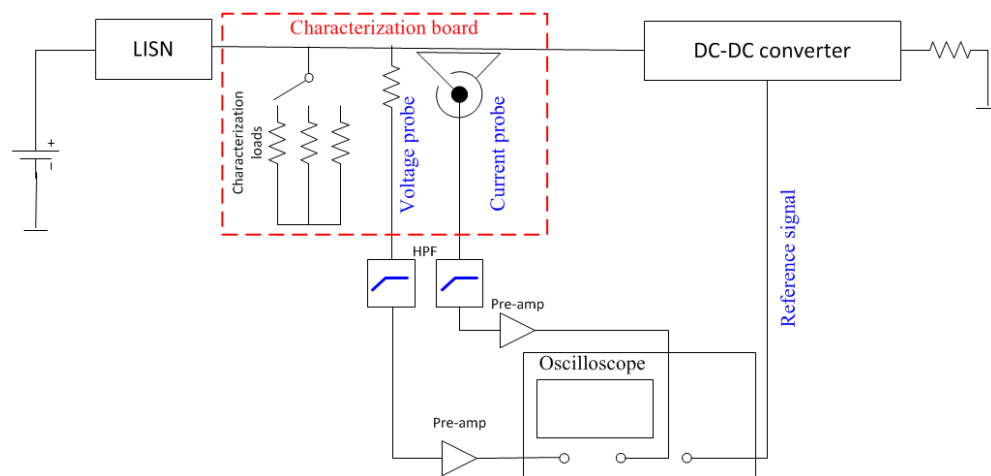
Figure 5.1. Measurement setup for the terminal model characterization

The voltages and currents are measured by oscilloscope and then converted into frequency domain:

$$|V_O|e^{j\varphi_O} = FFT(v(t) \cdot w(t)) \tag{2}$$
$$|I_O|e^{j\varphi_O} = FFT(i(t) \cdot w(t)) \tag{3}$$

where the w(t) is the flattop window function

The measurement is repeated multiple times to determine the averaged and maximized magnitude of the signals.

$$|V|_{avg} = \langle|V_O|\rangle, \quad |I|_{avg} = \langle|I_O|\rangle \tag{4}$$
$$|V|_{max} = max\{|V_O|\}, \quad |I|_{max} = max\{|I_O|\} \tag{5}$$

where $\langle\cdot\rangle$ represents averaging over realizations, and $max\{\cdot\}$ is the operator of taking a maximum value over realizations.

The averaged phase difference between voltage, current and the reference signal were calculated by taking the ratios as follows

$$|Refv|e^{j\varphi_{vavg}} = \left|\frac{FFT(v \cdot w(n))}{FFT(v_{ref} \cdot w(n))}\right| \tag{6}$$

$$|Refi|e^{j\varphi_{iavg}} = \left|\frac{FFT(i \cdot w(n))}{FFT(v_{ref} \cdot w(n))}\right| \tag{7}$$

where v_{ref} the voltage in the reference channel. The phase of the ratio in (6) is always deterministic even if the signals are random because both v and i are linearly dependent on vref. The averaging in the formulas (6) and (7) strictly speaking is unnecessary and is used only to suppress the additive measurement noise introduced by the amplifiers and the oscilloscope.

$$V_{\{1,2\}\{avg,max\}} = |V_{\{1,2\}\{avg,max\}}|e^{j\varphi_{Vavg\{1,2\}}} \tag{8}$$

$$I_{\{1,2\}\{avg,max\}} = |I_{\{1,2\}\{avg,max\}}|e^{j\varphi_{iavg\{1,2\}}} \tag{9}$$

where indices 1 and 2 refer to the characterization loads. Then, the average and maximized voltage and current spectra are constructed as

The spectra above are purely deterministic (since averaged and maximized magnitudes of random processes are deterministic quantities) and at the same time complex, which allows to use them as complex amplitudes of the signals and hence to calculate the parameters of the equivalent source model by solving (1).

6. TERMINAL MODEL VALIDATION

For the validation the model obtained with 10 and 250 Ohm resistors was used to predict the voltage and current produced by the converter at a 50 Ohm resistor. The results of the prediction were compared to the direct measurements.

The resistances given above represent only the DC impedance of the loads. The actual impedances measured by the VNA according to the setup in Figure 6.1 in the frequency range of interest are shown in Figure 6.2.

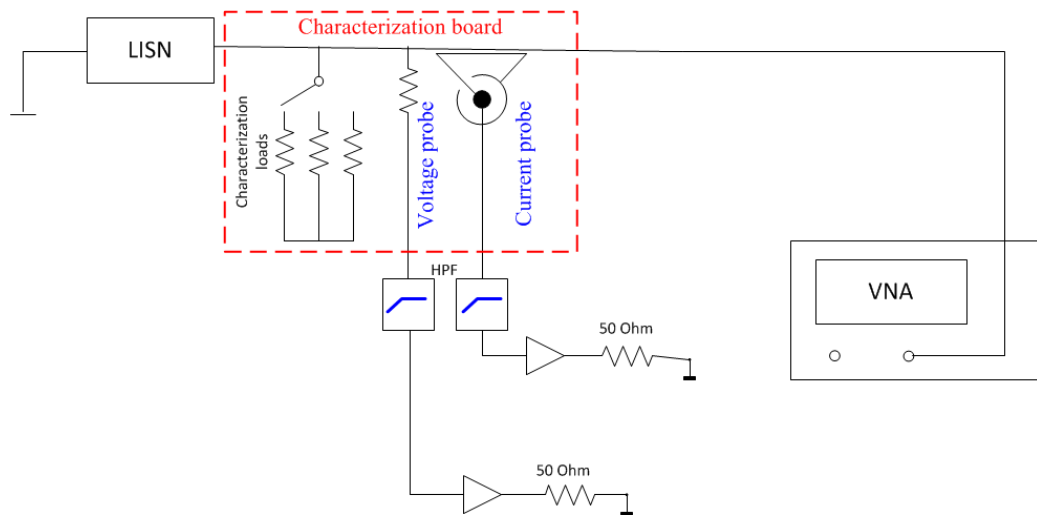Figure 6.1. Measurement setup for the impedance of the three loads (two characterization loads and one test load)

The characterization setup for the boost converter is shown in Figure 6.3. The measurement setup consists of LISN, characterization board and phase reference probe.
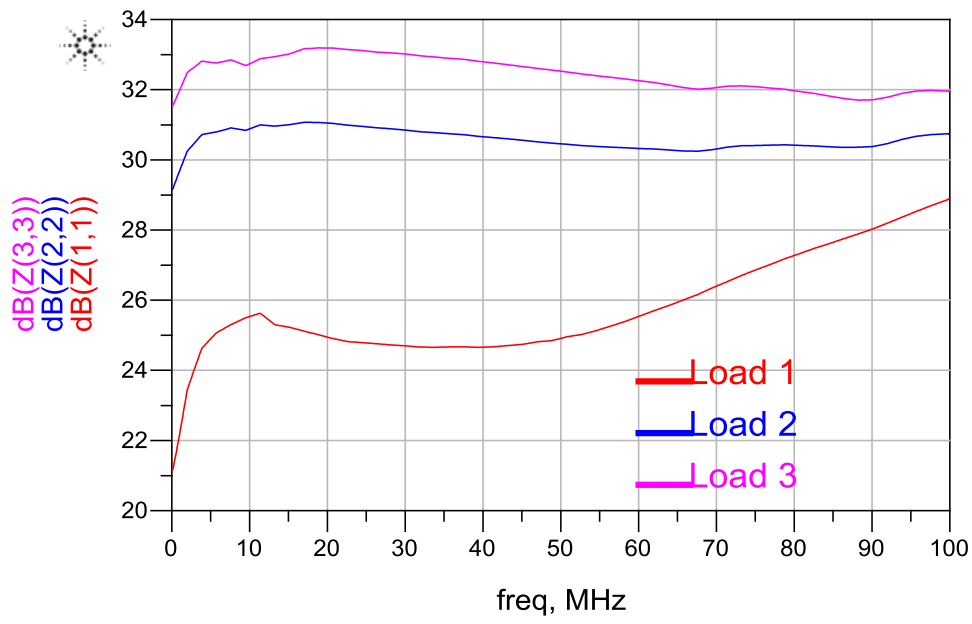
Figure 6.2. Measured impedances of three loads (13 Ohm, 50 Ohm, and 250 Ohm)
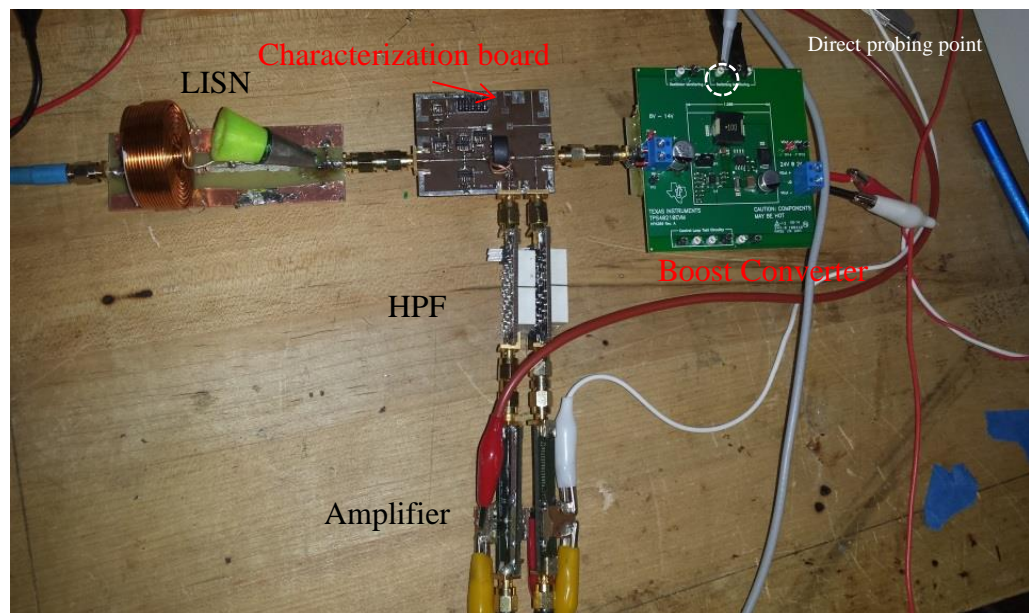
Figure 6.3. Characterization setup for boost converter

The converter was set to convert 12v DC to 24v DC. The converter was loaded by a dummy load (120 Ohm resistor).

In order to obtain the phase, the signal at the gate was probed by the high impedance probe. The phase reference waveform for several switching periods is shown in Figure 6.4. The switching frequency is about 580 kHz.
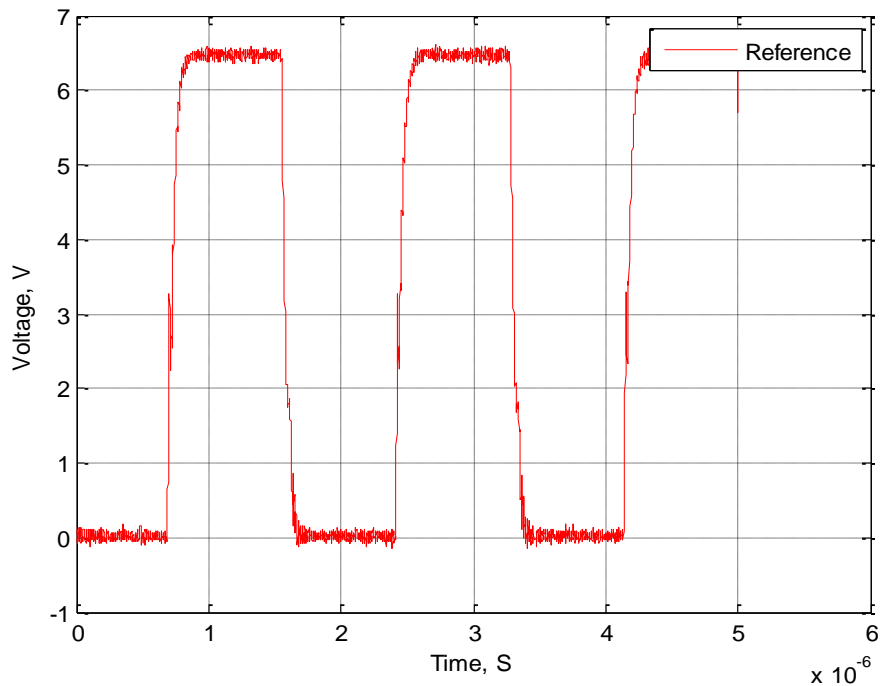
Figure 6.4. Time domain waveform of the phase reference signal

In order to obtain the averaged and maximized magnitude of the measured voltage and current, the measurement is repeated multiple times and the convergence of the

spectrum is shown in Figure 6.5. These curves can be used to determine the required

averaging factor.
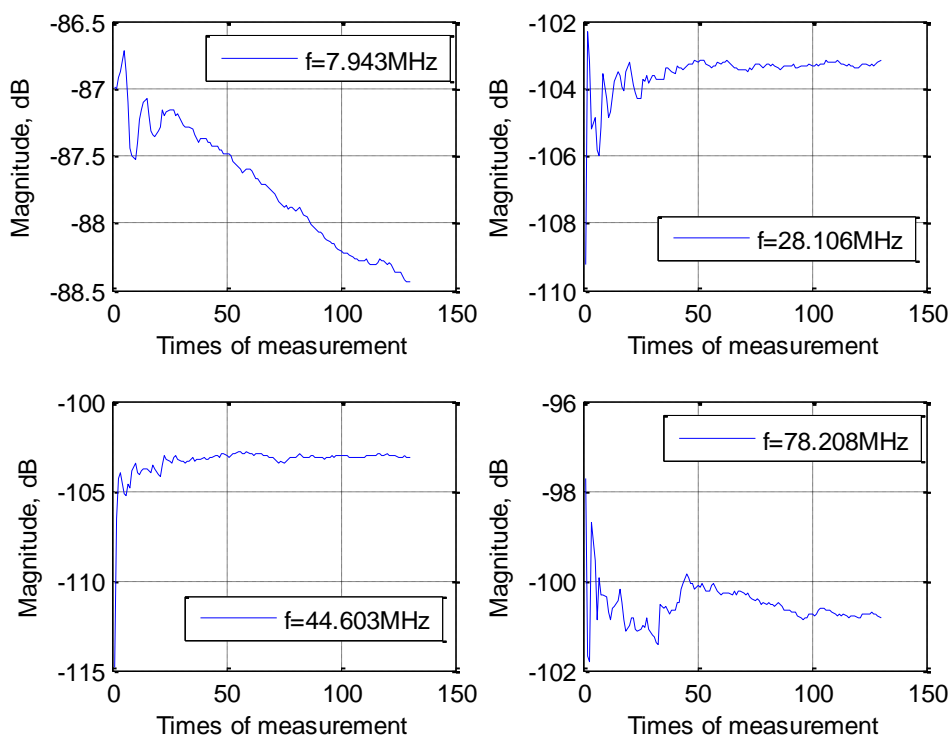
Figure 6.5. Averged magnitude convergence as a function of the number of averages

It can be seen that at 7 MHz, the magnitude stays almost constant (which

indicates an almost deterministic signal). At 78 MHz the averaged magnitude stabilizes

only after 100 averages. Based on results from Figure 6.5, the averaging factor was set to

135 both in characterization and validation measurements.

The measured averaged and maximized magnitude of the voltage for load 2 (50 Ohm) is shown in Figure 6.6. It can be seen that this converter produces random signals above approximately 10 MHz.
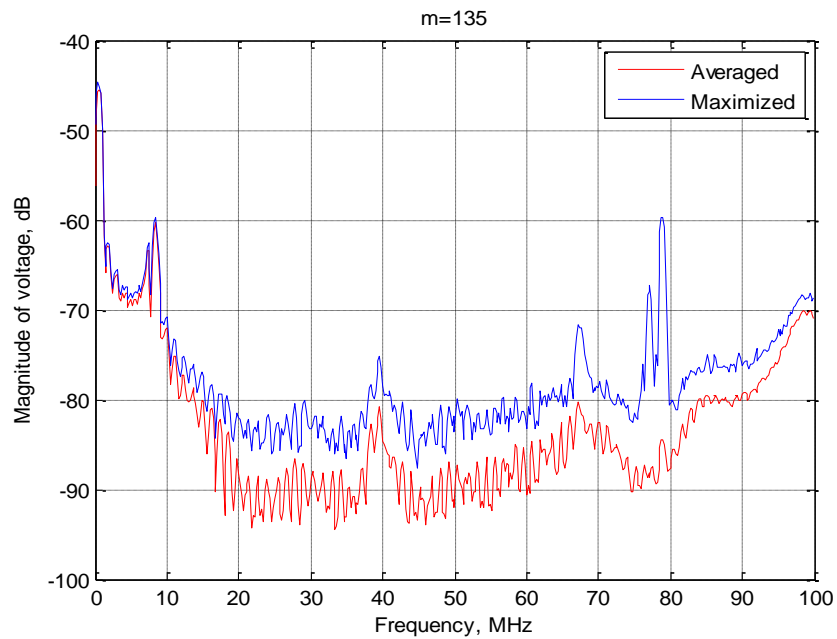
Figure 6.6. Spectrum comparison between the averaged and maximized magnitude

The schematic for the model validation is shown in Figure 6.7. The circuit contains the equivalent terminal source and an S-parameter block representing the measured impedance of the test load.
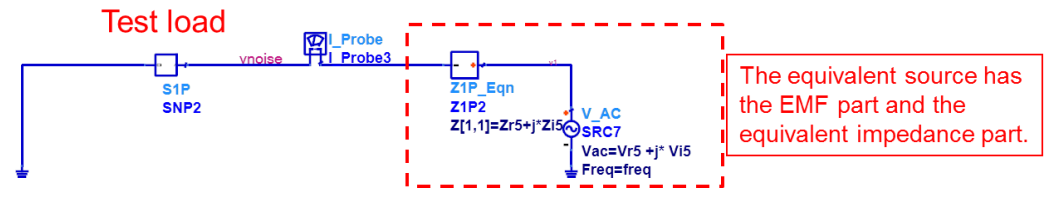
Figure 6.7. Terminal model validation to predict the noise voltage and current

The predicted noise voltage and current for averaged and maximized magnitude are shown in Figure 6.8 and 6.9 respectively.

Figure 6.8. Spectrum comparison for averaged voltage magnitude
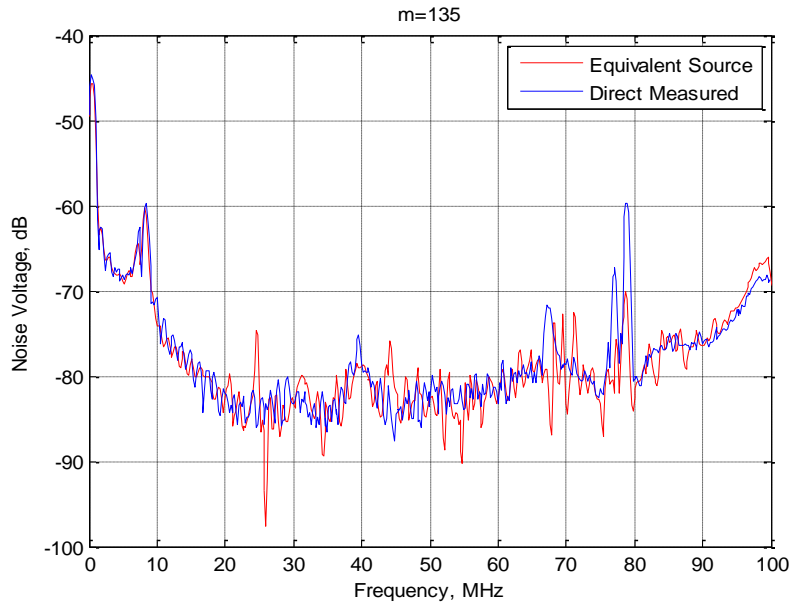
Figure 6.9. Spectrum comparison for maximized voltage magnitude

It can be seen that the agreement is within 2 dB up to 100 MHz for the averaged

magnitude case, for the maximized magnitude case, the error is mainly within 2 dB, but

at some frequencies, the error is much larger reaching 10 dB (this can be explained by a

much slower convergence of the maximized quantities compared to the averaged ones).

However, it was found that for all three loads conditions, the measured voltages are

almost the same, which indicates that the source impedance is quite small (probably due

to the EMI filter at the input of the converter).

In order to make the comparison more meaningful, the noise currents (which vary

a lot from one load to another) were also compared as shown in Figure 6.10 and Figure

6.11.
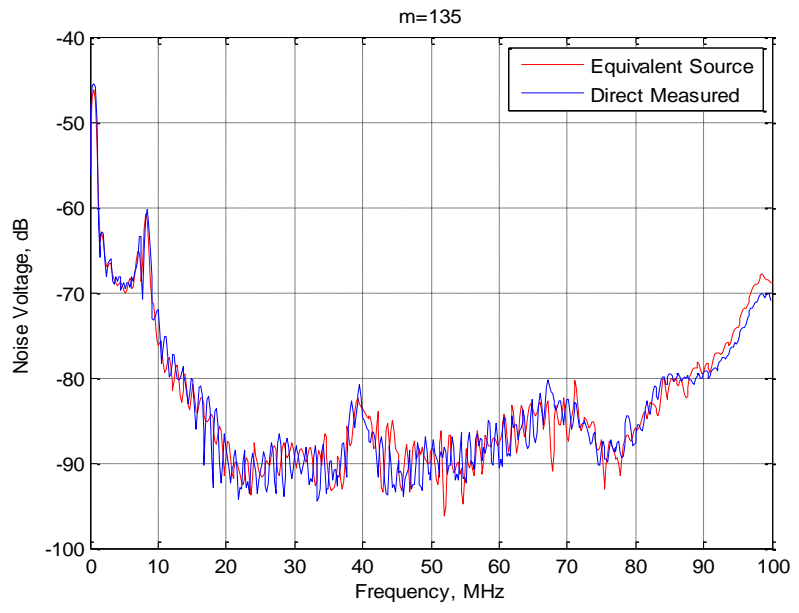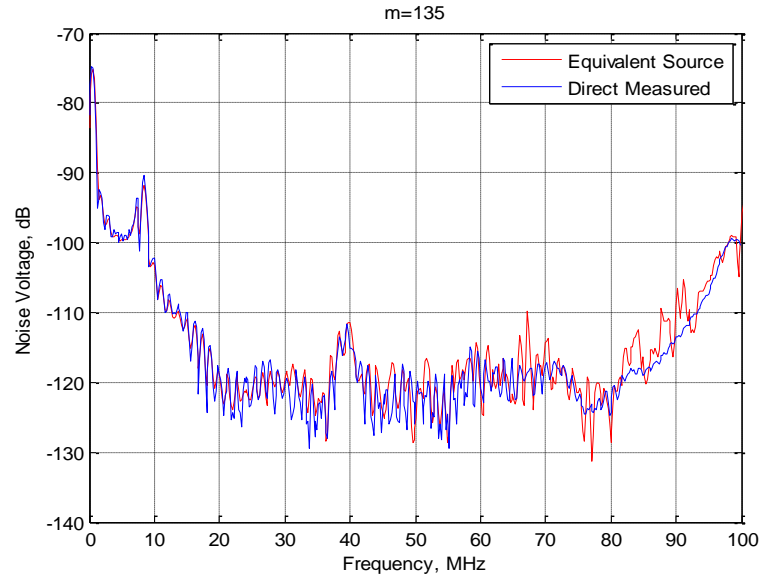
Figure 6.10. Spectrum comparison for averaged current magnitude
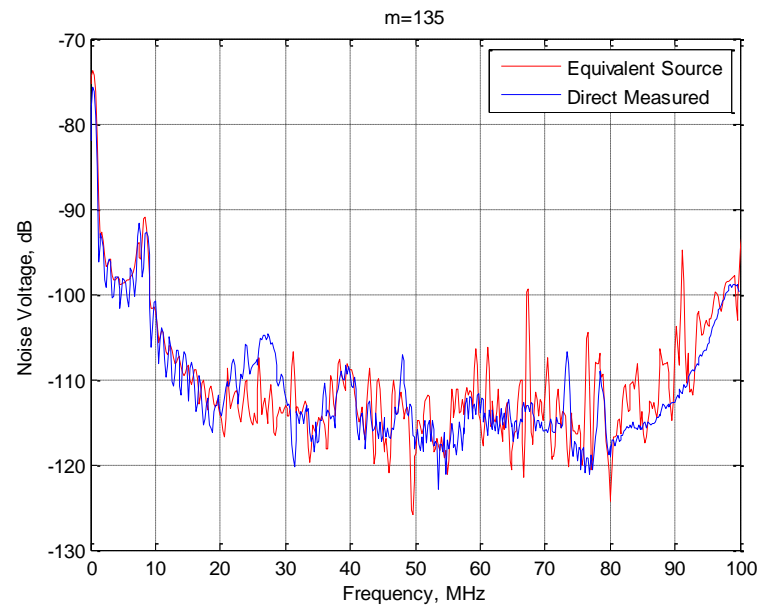
Figure 6.11. Spectrum comparison for maximized magnitude

It can be seen that the agreement is also good with the error within 10 dB for the maximized case. Higher error for the maximized quantities can be explained by slower convergence of the maximum of the random variable relative to its average.

7. CONCLUSION

In this paper, a terminal model characterization method for converter with stochastic behavior is proposed. The averaged and maximized spectrum of the measured voltages and currents are used to create the model. The phase information is obtained using a dedicated reference channel. The time record length can be determined by calculate the equivalent RBW.

The terminal model of a boost converter with random signal was created and validated. The predicted averaged and maximized noise voltages have a good accuracy up to 100 MHz when the test load is within the characterization range. The error is within 5 dB for averaged and 10 dB for maximized quantities.

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SECTION

2. CONCLUSIONS

In the first paper, a methodology of building an IC model capable of predicting failures for given disturbances at the clock input based on limited or no knowledge about IC internals was developed. In this paper, the ESD immunity behavior of an 18 MHz D flip-flop used in ISO 10605 standard is investigated. The test IC was characterized by direct injection of particular waveforms, and a behavioral model was created. The whole model combining the full wave model of ISO 10605 setup and PCB with the behavioral model of the IC was used created to predict the induced voltage at the clock pin and the IC triggering. The simulated waveforms agreed well with the measurement and the failure discharging level of the ESD gun can also be predicted. The largest errors are about 20% when the harness is parallel wires. The largest error for the predicted triggering level when the harness is twisted pair is about 30%.

In the second paper, the maximized radiated emissions of the heat-sink/IC structure are predicted up to 40 GHz by creating an equivalent source using the measured electrical field in the gap between the heatsink and ICs. The electric field is detected by an E-field probe made of an open coaxial cable coated with absorbing material. A numerical model is built in CST microwave studio to obtain the maximized radiated field with the measured field used as a source to excite the heat-sink model. The evaluated maximized radiated field is in good agreement with the measured value; the error is within 6 dB.

In the third paper, a characterization method for converters with stochastic behavior is presented. The averaged and maximized spectrum of the measured voltages

and currents are used to create the model. The phase information is obtained using a

dedicated reference channel. After the equivalent source was determined, the actual

induced noise voltage at the test load was compared to that predicted by the model with

averaged and maximized spectrum to estimate its accuracy. The results indicate that the

agreement with the direct measurement is within 5 dB up to 100 MHz when the load is

within the characterization range.

VITA

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