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Synchronization of pulse code modulation telemetry

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SYNCHRONIZATION OF PULSE CODE MODULATION TELEMEIRY

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A

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ABSTRACT

Pulse Code Modulation (PCM) is one of the most widely utilized radio telemetry techniques for the recovery of test data from aerospace vehicles. Synchronization of the receiver with the transmitted data is perhaps the prime requisite of a PCM telemetry system.

In this paper the frame synchronization process is analyzed by developing equations which define the three modes of synchronizer operation (SEARCH, VERIFY, and LOCK) in terms of the relative probabilities of operation. The criteria employed to optimize the synchronization process are the mean time to acquire true synchronization, the probability of true synchronization after verification of the synchronization decision, and the percentage of data lost due to synchronization dropout (the dropout resulting from noise in the received signal). The results of this analysis are used to derive optimum synchronization system parameter settings for a hypothetical telemetry system. The problem of deriving an optimum PCM synchronization code is also presented. It is based on the criteria of minimum probability of false occurrence of the pattern in the received signal.

Prior to discussing the frame synchronization problem, a general description of a typical airborne PCM telemetry system is made. Also, a brief description of bit synchronization and data regeneration techniques and their affect on the frame sync problem is included.

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I. INTRODUCTION

In PCM telemetry systems it is necessary to attain both bit and frame synchronization (hereafter the word synchronization will frequently be abbreviated as "sync") before received data may be identified. It is the primary purpose of this thesis to:

A. Develop expressions which define the three modes of operation (SEARCH, VERIFY, and LOCK) in acquiring frame sync.

B. Utilize these expressions to determine optimum frame synchronizer system parameters based upon operating criteria within each of the three operating modes.

C. Develop a set of equations required for determining frame sync patterns for PCM telemetry systems.

Additionally, in this thesis a typical PCM telemetry system and the problem of bit sync will be discussed.

The subjects of PCM sync and frame sync code evaluation have been presented in many technical papers. There has been lacking, however, a uniform approach for handling a variety of such problems. Also, a simple method of generating a good sync pattern has not been presented to date.

These problems will be attacked from a system design engineering standpoint. The results are intended to provide a guide which may

be used in telemetry ground station development or utilization.

Much of the basic groundwork concerning frame sync and frame sync patterns was presented at the 1961 and 1962 National Telemetry Conferences. E. R. Hill and J. L. Weblemoe[1] presented results and recommendations from a comprehensive study. The significant conclusions concerning frame sync are:

A. A single frame sync pattern in each frame is sufficient to obtain frame sync. Word sync patterns are unnecessary and tend to waste information capacity.

B. A dual-mode sync system containing a search and lock mode is recommended.

M. W. Williard[2] considered the problem of synchronization using both word and frame sync patterns and presented charts for calculating the probability of sync pattern detection. In subsequent papers Williard[3,4] developed equations for evaluating PCM sync in terms of the mean or average time required to acquire sync and the percentage data lost due to loss in pattern sync employing a dual-mode sync system. He also presented a paper outlining a method of evaluation of sync code patterns[4] based on the criteria of minimum probability of false occurrence of the pattern in the received signal.

G. E. Goode and J. L. Phillips[5] discussed the group sync problem with particular emphasis on the selection of optimum sync codes for correlation detection. In the 1962 NTC; Goode and Phillips[6] gave a

description and the performance characteristics of a frame sync pattern generator and recognizer which they had developed.

Dr. J. P. Magnin[7] considered a frame and sub-frame sync problem which employed a SEARCH, VERIFY, and LOCK mode system. Also in the 1962 National Symposium on Space Electronics and Telemetry, Dr. R. S. Codrington and Dr. J. P. Magnin[8] presented a paper discussing Legendre PCM sync codes which employed a criteria of minimum aperiodic correlation coefficients.

Synchronization codes were considered by R. G. Masching.[9] His aim was to present a simplified approach to determining optimum frame sync codes. Also J. J. Maury, Jr. and F. J. Styles[10] described an analysis of the criteria for frame sync code optimality and the application of their criteria to the derivation of formulae for sync code development.

The development contained here generally follows the works of Williard, Magnin, and Masching in the frame sync and sync code areas. The results of the development are subsequently used to develop a decommutation strategy for a hypothetical PCM system.

II. GENERAL DESCRIPTION OF A TYPICAL PCM AIRBORNE TELEMETRY SYSTEM

Telemetry is the process by which a quantitative measurement is transmitted to a remote location. Pulse Code Modulation (PCM) telemetry has emerged as one of the most popular telemetry forms during recent years for acquiring test information from aerospace vehicles, missile weapons systems, and aircraft. In PCM a group of binary digits is used to represent the signal voltage output of a physical sensor at a given instant of time.

A typical PCM airborne telemetry and data recovery system is shown in Figure 1. It is composed of: airborne elements.....sensors, conversion circuitry, commutation or multiplex circuitry, analog-to-digital converter, premodulation filter, transmitter and antenna; ground elements.....antenna, receiver, tape recorder, signal conditioner and bit synchronizer, frame synchronizer, format translator, display and/or recording devices.

A. Data Transmission - The elements of the data transmission or airborne telemetry system are briefly described in the following section.

1. Sensors - Sensors commonly used today are thermocouples, resistance-bridge temperature sensors, pressure sensors, strain gages, vibration sensors, accelerometers, gyros, bio-medical transducers, radiation sensors, and various other forms of instrumentation.

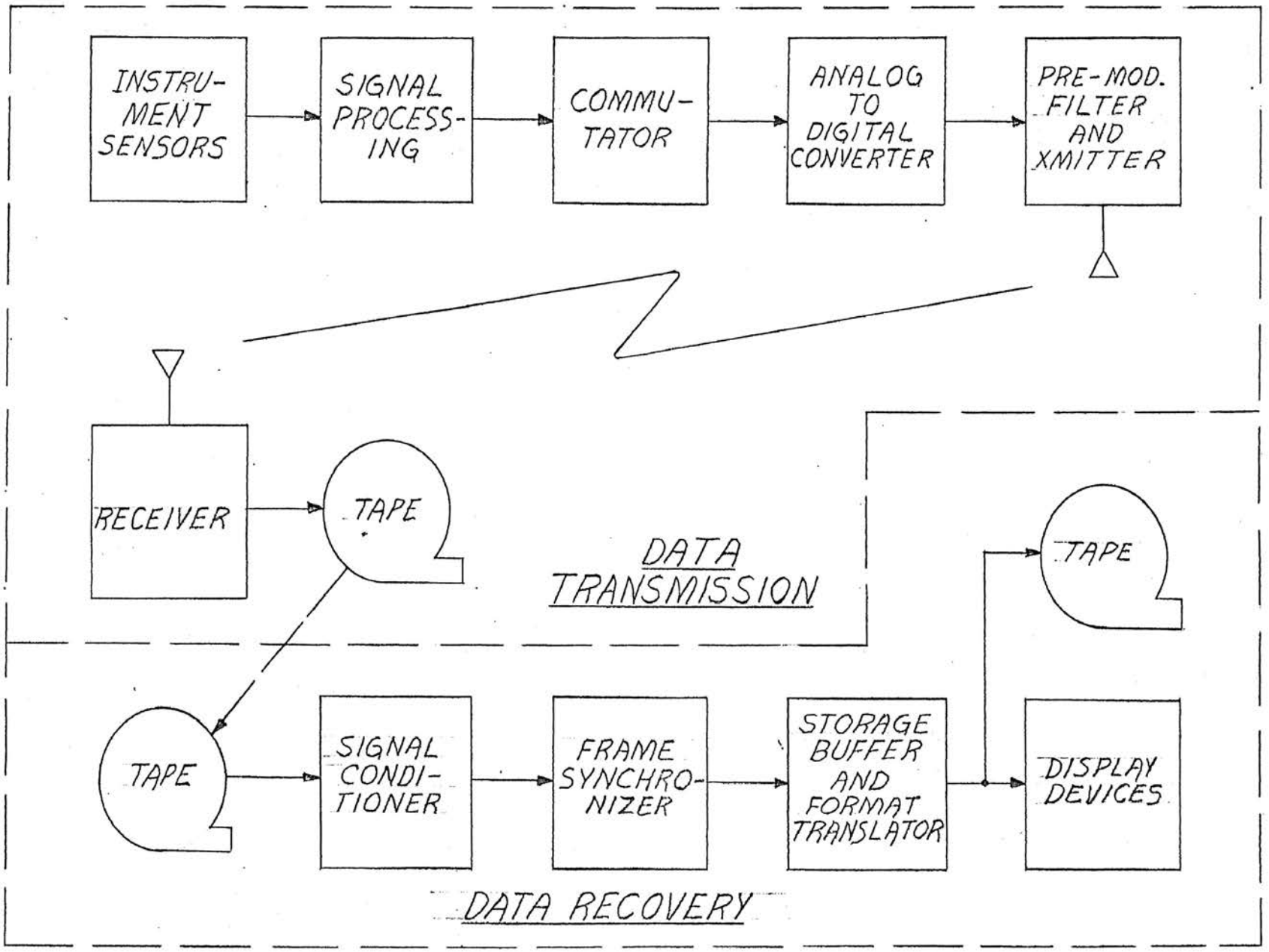


FIGURE 1 - Typical PCM Airborne Telemetry System

2. Signal Processing - Conversion circuitry is generally employed to condition the outputs of the instrument sensors to allow them to be compatible with the input range of the analog-to-digital converter.

3. Commutation - Basic to a PCM telemetry system is the multiplex and analog-to-digital conversion circuitry. An example of a commutation scheme for the PCM system to be considered here is depicted in Figures 2 and 3. Total word output of the system shown is 6000 words/second. For an eight bits/word representation, an overall bit rate of 48,000 bits/second results.

The commutation matrix shown in Figure 2 is clarified by examining the mechanical analog in Figure 3. The primary commutator consists of 60 segments, each segment sampled 100 times/second. Thirty of the primary segments are allocated for subcommutator use. Each subcommutator consists of 100 segments, each segment samples 10 times/sec. Other rates between 10 and 100 and higher than 100 samples/sec. may be attained by supercommutation, i.e. symmetrically cross-wiring a parameter to more than one segment on a given commutator. The final output of primary commutator A is a pulse, amplitude-modulated waveform (except during sync word times). It serves as an input to the analog-to-digital converter.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	. . .	55	56	57	58	59	60
FRAME	S1	S2	S3	B1	C1	D1	A7	A8	A9	B2	C2	D2	A13	A14	A15		A55	A56	A57	A58	A59	A60
				B11	C11	D11	A7	A8	A9	·	·	·	·	·	·		·	·	·	B20	C20	D20
				B21	C21	D21	·	·	·	·	·	·	·	·	·		·	·	·	B30	C30	D30
				·	·	·	·	·											·	·	·	·
				·	·	·	·	·											·	·	·	·
				B81	C81	D81	·	·											·	B90	C90	D90
				B91	C91	D91	·	·											·	B100	C100	D100
				B101	C101	D101	·	·											·	B110	C110	D110
	▼	▼	▼	B111	C111	D111	·	·											·	B120	C120	D120
	S1	S2	S3	B1	C1	D1	A7	A8	A9	B2	C2	D2	A13	A14	A15		A55	A56	A57	A58	A59	A60
				B11	C11	D11	A7	A8	A9	·	·	·	·	·	·		·	-	·	B20	C20	D20
				B21	C21	D21	·	·	·	·	·	·	·	·	·		·	·	·	B30	C30	D30
				·	·	·	·	·		·									·	·	·	·
				·	·	·	·	·											·	·	·	·
				B81	C81	D81	·	·											·	B90	C90	D90
				B91	C91	D91	·	·											·	B100	C100	D100
				B101	C101	D101	·	·											·	B110	C110	D110
	▼	▼	▼	B111	C111	D111	·	·											·	B120	C120	D120

S1, S2, S3 = PRIMARY SYNC WORDS.
NO. OF BITS BETWEEN PRIMARY SYNC WORDS = 480.
NO. OF WORDS PER FRAME = 720

FIGURE 2 - Typical PCM Commutation Matrix

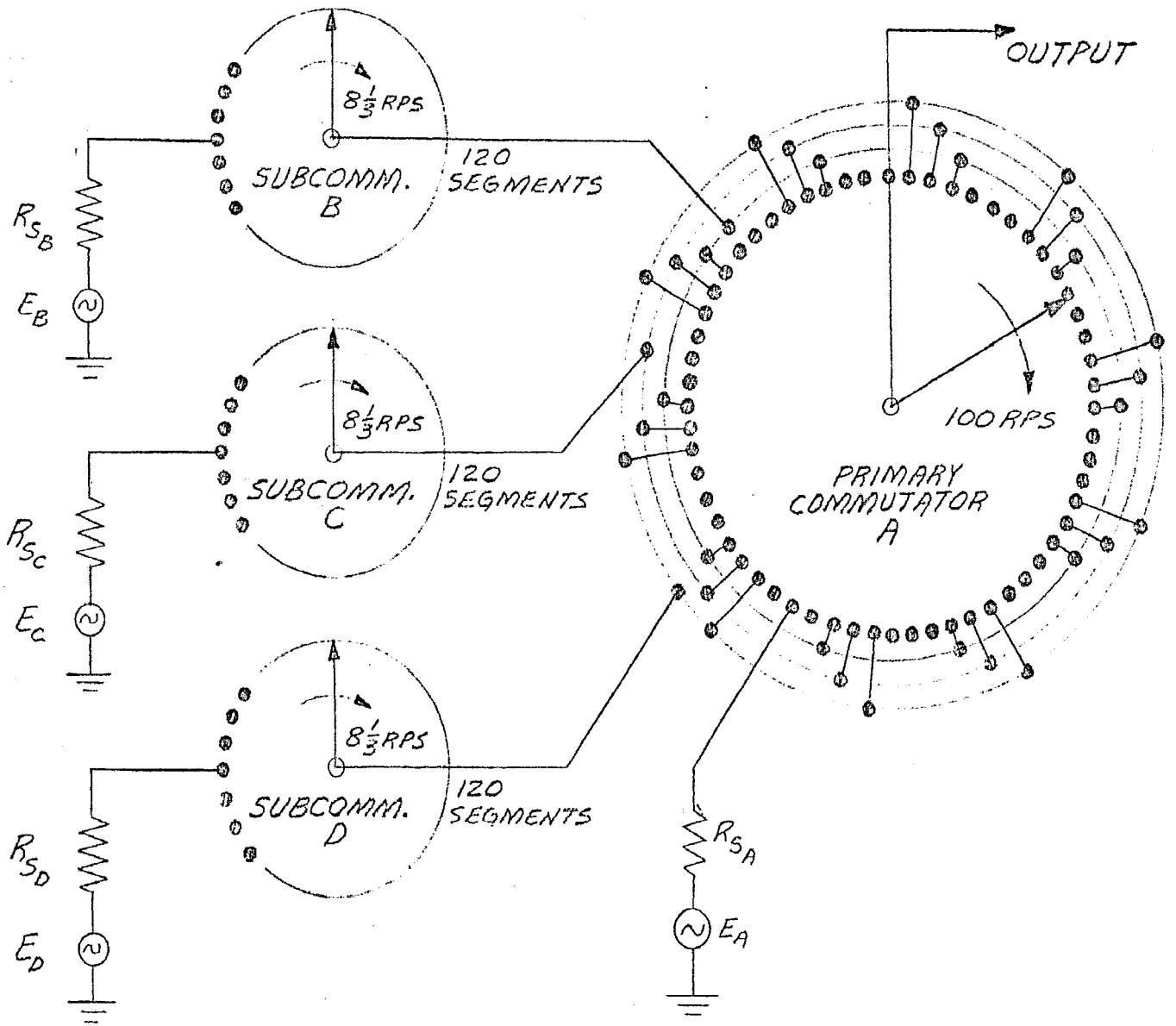


FIGURE 3 - Analogous Mechanical Switch Representation of the Matrix of Figure 2

3. (Continued)

The sample rate required to adequately reconstruct the behavior of a data parameter is dependent upon the maximum rate of change of the variable. A form of the sampling theorem is employed by every instrumentation engineer who determines the number of samples per second required to adequately represent the data. For narrow aperture sample-and-hold circuitry, sampled data as shown in Figure 4(c) can be approximated by multiplying the signal voltage of Figure 4(a) by a train of periodically spaced impulses of Figure 4(b).

The impulse train can be expressed mathematically as:

$$s(t) = T_o \sum_{n=-\infty}^{\infty} \delta(t - nT_o) \qquad \text{(II-1)}$$

Since s(t) is periodic and an even function, it can be represented by a Fourier cosine series.

$$s(t) = A_o + 2 \sum_{k=1}^{\infty} A_k \operatorname{Cos} k\omega_o t \qquad \text{(II-2)}$$

where

$\omega_o = 2\pi/T_o$ and the term A_k is given by

$$A_k = \frac{1}{T_o} \int_{-T_o/2}^{T_o/2} s(t) \operatorname{Cos} k\omega_o t \, dt$$

$$A_k = 1 \qquad k = 0, 1, 2 \ldots$$

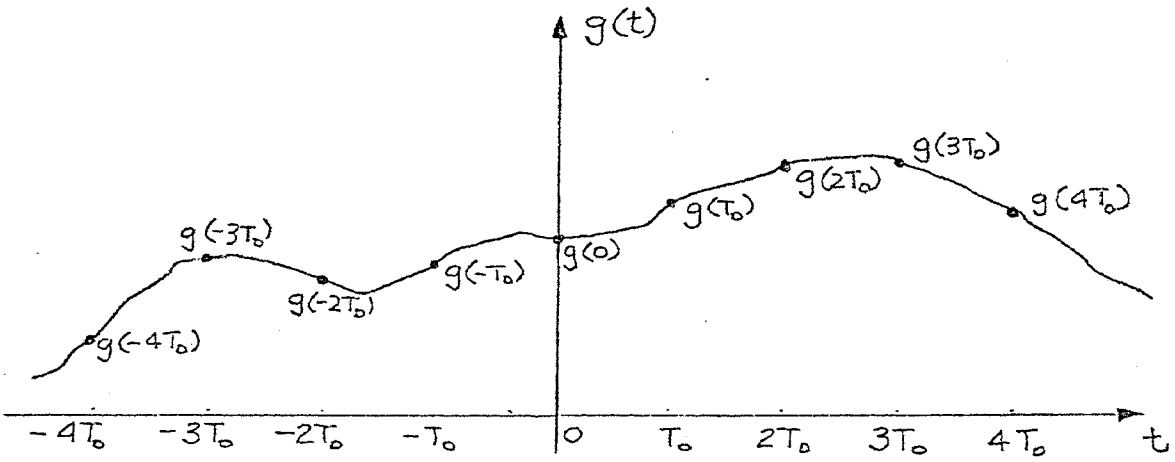


FIGURE 4(a) - Information Bearing Signal, g(t)

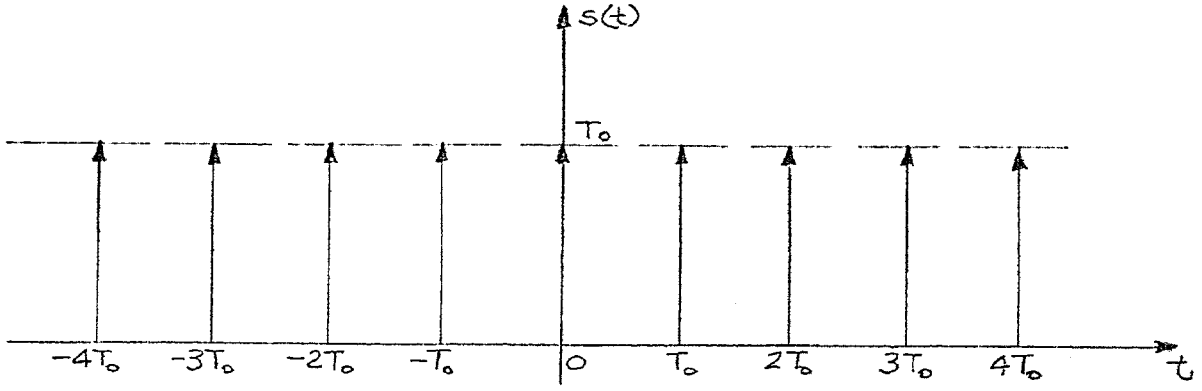


FIGURE 4(b) - The Sampling Train, s(t)

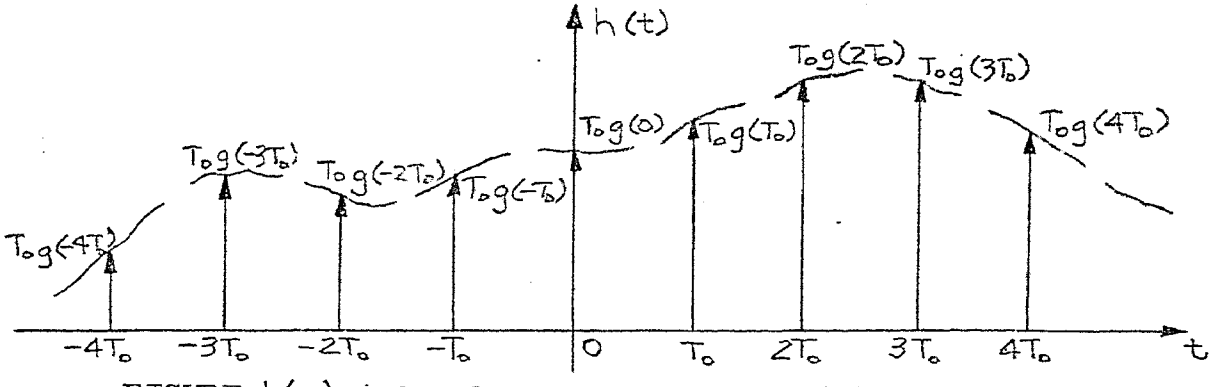


FIGURE 4(c) - Sampled Data Signal, h(t)

3. (Continued)

Thus the function s(t) can be written as

$$s(t) = 1 + 2 \sum_{k=1}^{\infty} \text{Cos } k\omega_o t \qquad \text{(II-3)}$$

For the purpose of this analysis let the information-bearing signal, g(t), of Figure 4(a) be defined on the double infinite interval $-\infty \leq t \leq \infty$. Also let its Fourier Transform $G(\omega)$ be such that $G(\omega) = 0$ for $|\omega| > W_1$.

By sampling g(t) at times $t = 0, \pm T_o, \pm 2T_o, \ldots$, the waveform h(t) of Figure 4(c) results, where

$$h(t) = g(t) \cdot s(t) \qquad \text{(II-4)}$$

Taking the Fourier Transform of h(t) gives

$$H(\omega) = \frac{1}{2\pi} \left[G(\omega) * S(\omega) \right] \qquad \text{(II-5)}$$

To find $H(\omega)$, the terms $G(\omega)$ and $S(\omega)/2\pi$ must be determined and the indicated convolution performed.

In obtaining the term $S(\omega)$, the transform of s(t) is performed as follows:

$$S(\omega) = \mathcal{F}\left[s(t)\right] = \mathcal{F}\left[1 + 2 \sum_{k=1}^{\infty} \text{Cos } k\omega_o t\right]$$

3. (Continued)

$$S(\omega) = 2\pi\delta(\omega) + 2\sum_{k=1}^{\infty} 2\pi\left[\frac{\delta(\omega+k\omega_o) + \delta(\omega-k\omega_o)}{2}\right]$$

$$= 2\pi\left[\sum_{k=1}^{\infty}\delta(\omega+k\omega_o) + \delta(\omega) + \sum_{k=1}^{\infty}\delta(\omega-k\omega_o)\right]$$

$$S(\omega) = 2\pi\left[\sum_{k=-1}^{-\infty}\delta(\omega-k\omega_o) + \delta(\omega) + \sum_{k=1}^{\infty}\delta(\omega-k\omega_o)\right]$$

$$= 2\pi \sum_{k=-\infty}^{\infty}\delta(\omega-k\omega_o)$$

$$\frac{S(\omega)}{2\pi} = \sum_{k=-\infty}^{\infty}\delta(\omega-k\omega_o) \qquad \text{(II-6)}$$

This is illustrated in Figure 5(b).

The shape of $G(\omega)$ is not important to this analysis; it is only necessary that $G(\omega) = 0$ for $|\omega| > W_1$. A typical $G(\omega)$ is therefore assumed for the remainder of the sampling analysis (Refer to Figure 5(a)).

Combining equations (II-5) and (II-6), we have:

$$H(\omega) = G(\omega) * \sum_{k=-\infty}^{\infty}\delta(\omega-k\omega_o)$$

$$= \sum_{k=-\infty}^{\infty} G(\omega-k\omega_o) \qquad \text{(II-7)}$$

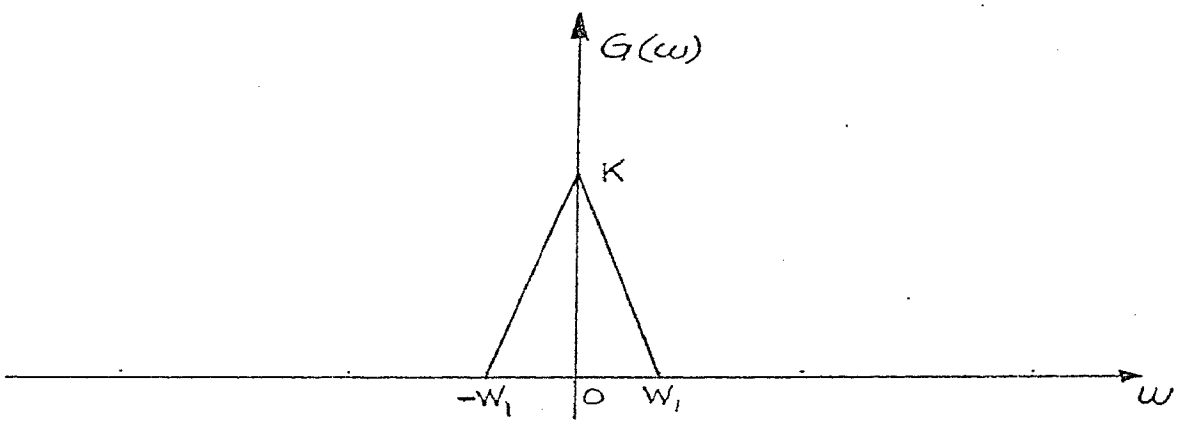


FIGURE 5(a) - Fourier Transform of g(t), G(ω)

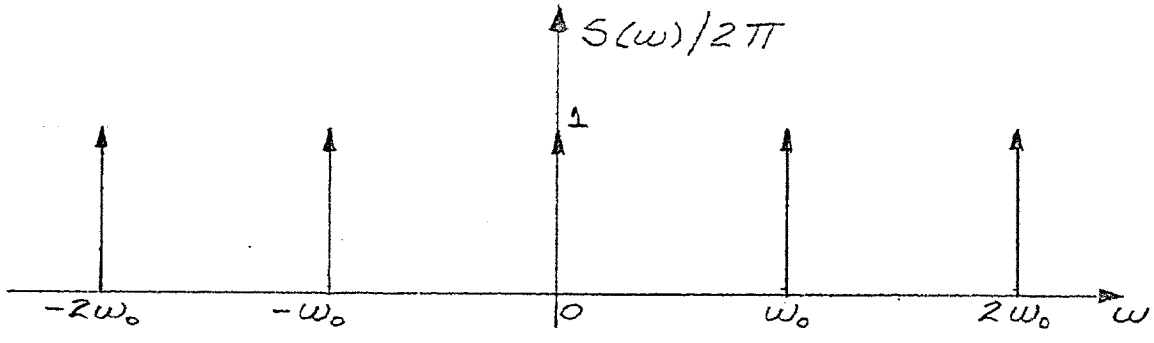


FIGURE 5(b) - Frequency Domain Representation of S(t)/2π

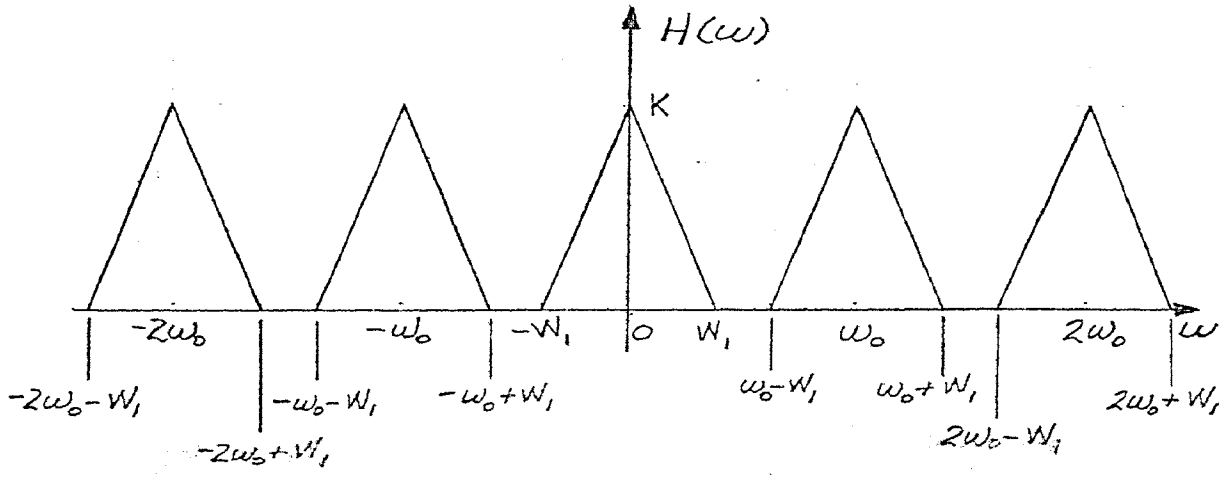


FIGURE 5(c) - H(ω) for $\omega_0 > 2W_1$

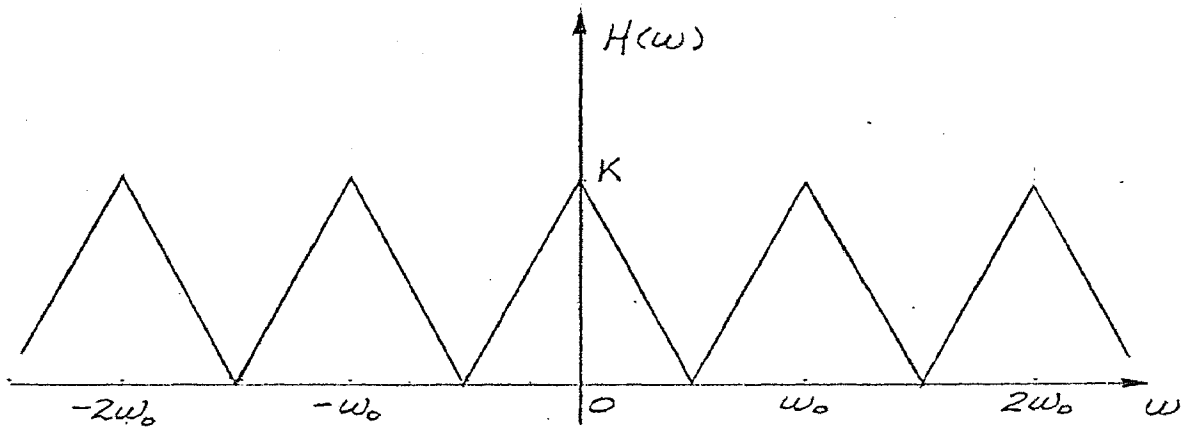


FIGURE 5(d) - $H(\omega)$ for $\omega_0 = 2W_1$

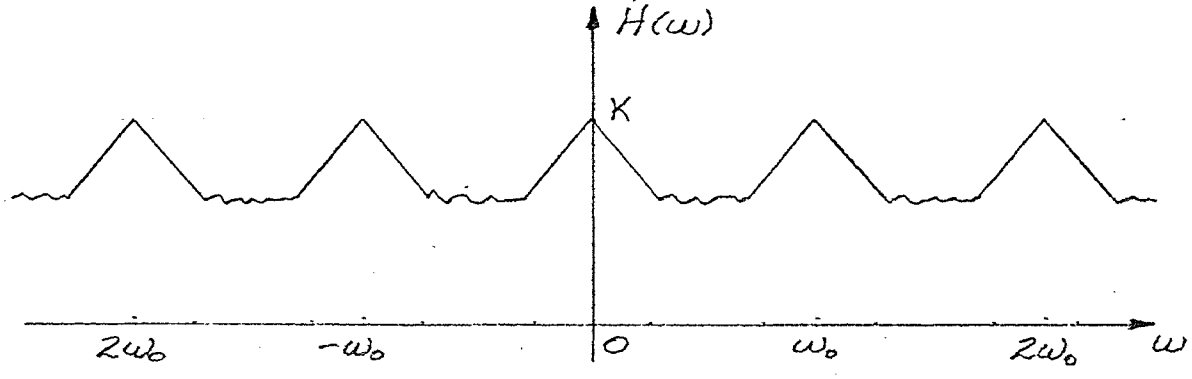


FIGURE 5(e) - $H(\omega)$ for $\omega_0 < 2W_1$

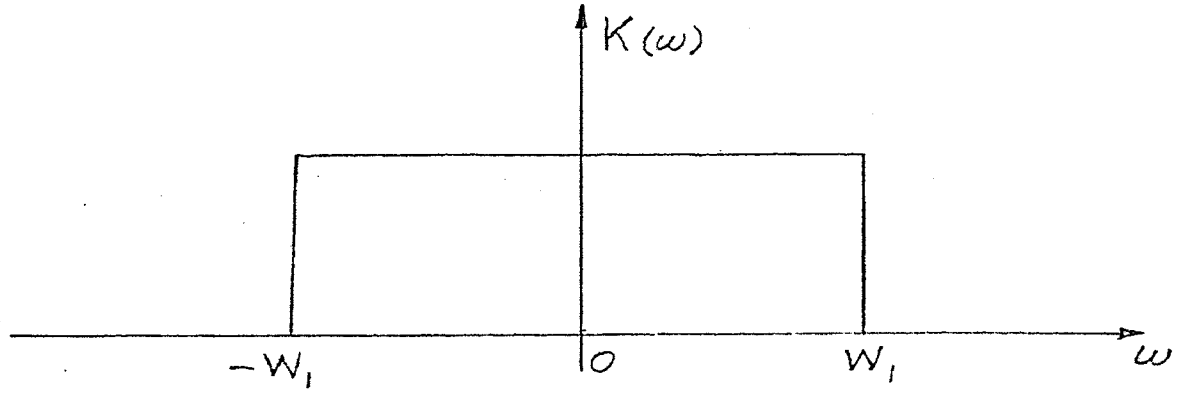


FIGURE 5(f) - Transfer Function of Ideal Low Pass Filter

3. (Continued)

In general, $G(\omega)$ is a complex function, thus the summation indicated for $H(\omega)$ must be performed by complex algebra. The difficulty of performing the summation depends upon the relationship of ω_o and W_1. For $\omega_o < 2W_1$ as shown in Figure 5(e), the adjacent translated $G(\omega)$ functions overlap. In the regions of overlap complex algebra must be employed to obtain the resulting $H(\omega)$.

With a sample rate sufficiently high to avoid overlap in the frequency domain, it is a simple matter to reconstruct the original data from the sampled data wavetrain. For $\omega_o \geq 2W_1$ the sampled data wavetrain, operated upon by a low pass filter having a simplified transfer function as shown in Figure 5(f) results in the output

$$\Theta(\omega) = K(\omega) \cdot H(\omega) = G(\omega) \qquad \text{(II-8)}$$

in the frequency domain, and

$$\theta(t) = k(t) * h(t) = g(t) \qquad \text{(II-9)}$$

in the time domain. Here $k(t)$ is equal to $\mathcal{F}^{-1} K(\omega)$, the impulsive response of the low pass filter. Thus, ideally, it can be stated that the sampled data can be perfectly reconstructed with a linear low pass filter, provided that the sampling frequency, ω_o, is at least twice as great as W_1, the highest frequency present in the sampled function.

3. (Continued)

Practically speaking, this theorem is almost useless since:

A. A function existing for a finite time cannot be said to contain only frequency components below W_1, and

B. Filters cannot be physically realized which are capable of perfect cut-off above a frequency W_1.

The theorem must therefore be tempered with engineering judgement. A sampling rate often used is five times the highest significant frequency.

4. Analog-to-Digital Conversion - Much can be said about analog-to-digital conversion processes. It is sufficient to note, however, that the sampled waveform previously examined must be converted to a digital form in a PCM telemetry system, and that the accuracy of the data as recovered is dependent upon the number of bits used to represent the analog data. For an "n" bit A/D conversion, there are 2^n discrete outputs. These outputs correspond to full scale input range between 0 and 100%. If each discrete output level is set to correspond to the mid-value of the equivalent input interval, then the maximum theoretical quantizing error is $\pm \frac{1}{2^{n+1}}$.

For an 8 bit/word PCM system, the quantization error would be $\pm \frac{1}{2^9}$ or $\pm$ 0.195%.

4. (Continued)

The commonly used digital codes as recommended by the Inter-Range Instrumentation Group (IRIG)[13] are as shown in Figure 6. Briefly these are:

A. RZ = Return-to-Zero Code

Advantage - High transition rate which aids bit sync.

Disadvantage - Fundamental bandwidth equal to bit rate.

B. NRZ = Non-Return-to-Zero Code

Advantage - Fundamental bandwidth only 1/2 bit rate.

Disadvantage - Low transition rate.

C. NRZ-M = Non-Return-to-Zero-Mark Code

Same as NRZ as regards bandwidth and transition density. Well suited to phase modulation transmission but has a high error rate due to noise.

D. Split-Phase

Advantage - High transition rate, ac coupled circuitry can be used, fundamental bandwidth only 1/2 bit rate.

Disadvantage - Difficult to distinguish bit levels.

5. Premodulation Filter, Transmitter, and Antenna - The premodulation or pre-transmission filter is employed for bandwidth limiting. This provides efficient spectrum utilization. The filters have little effect in systems with low bit rates. However they are quite significant in high bit rate systems.

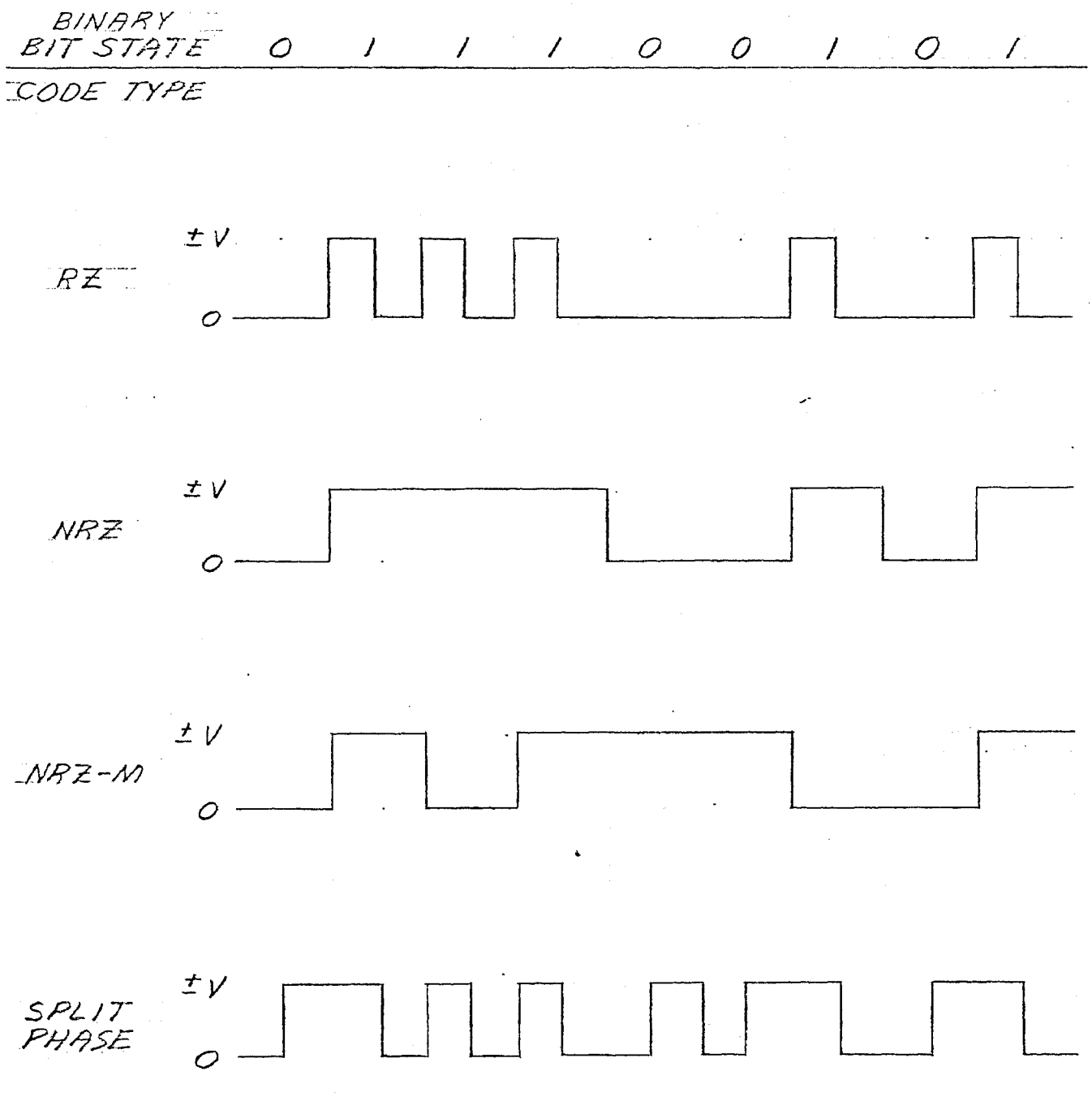


FIGURE 6 - PCM Bit Code Representations

5. (Continued)

The transmitter (usually FM or PM for PCM telemetry) and antenna are vital to any telemetry system but are mentioned here only for completeness. They have no effect on the analysis which follows.

B. Data Recovery - The basic elements which comprise a data recovery system are briefly described in the following sections.

1. Receiving Antenna and Receiver - The receiving antenna and receiver are portions of a telemetry system which, while also vital to the success of a data recovery system, are only mentioned in passing since they have little or no effect upon the analyses which follows.

2. Tape Recorder - A tape recorder is employed in virtually every telemetry system. They are used to provide a permanent record of the received data. After recording received data various filtering techniques, decommutation strategies, etc., may be employed to recover as much data as possible.

While this represents an advantage of tape recorders, there is also an inherent disadvantage; in the record and playback phases the signal-to-noise ratios are lowered.

2. (Continued)

Also effects of recorder "wow" and "flutter" can introduce large bit rate fluctuations which aggrevate the bit synchronization problem.

3. Signal Conditioner and Bit Synchronizer - Bit synchronization is the first step in the synchronization of a PCM signal. The process of signal conditioning and bit synchronization is employed in a PCM telemetry system to define the temporal position and "one" or "zero" value in the PCM serial wavetrain. This phase of PCM synchronization is further discussed in Section III of this thesis.

4. Frame Synchronizer - Frame synchronization of a PCM signal consists of identifying a specific bit position in a data frame. Having identified a bit position within a frame, it is a simple matter to identify any bit or word position within the data frame by counting bit times (pulses from the phase-locked oscillator in the bit synchronizer). The process of identifying a bit position within a frame is usually accomplished by inserting a fixed bit pattern in the data train in periodic intervals. A pattern recognizer may then be employed in the frame synchronizer to detect the known pattern. This establishes a reference bit position. The derivation of

4. (Continued)

optimum system parameters for the frame synchronization problem is the main topic of this paper and is discussed in Section IV.

5. Format Translation and Data Reduction - After obtaining frame sync, each word in the data frame is separated from the PCM bit train, identified, and placed in a buffer storage register in the decommutator. Upon storing a complete data frame in the register, the data time is read from the tape, then the data and corresponding time are rerecorded on another magnetic tape in a form suitable for use as input to a digital computer. This process is called format translation. The data tape, now in the proper format, serves as input to a data reduction program. This program accepts the raw data and in conjunction with instrument calibrations produces data parameters in engineering units. These units represent the input variations to the physical sensor in the airborne instrumentation system. The data reduction program thereby completes the telemetry process.

III. BIT SYNCHRONIZATION

Bit synchronization is the first step in the synchronization of a PCM signal. Bit sync is that process which defines the temporal position of a bit in the serial PCM wavetrain. Bit sync is attained when the PCM detector is locked in phase and frequency to the transmitted digital signal. In general the bit synchronizer must deduce the bit rate from a noisy, rate variable bit stream, possibly containing a dc offset. It must then decide upon the presence of a "one" or a "zero" during each bit interval.

The prime performance requirement of a PCM conditioner is the ability to maintain sync (in phase and frequency) with the bit period at low signal-to-noise ratios.[13] This requirement is necessary even though the data under these conditions may not be useable. The purpose is to eliminate the loss of data due to acquisition time after the signal-to-noise ratio improves. This suggests another performance measure of a PCM signal conditioner, namely the time required to acquire synchronization.

Early decommutation systems employed crude techniques of bit detection such as zero crossing detection. Most systems currently use phase-lock loop bit synchronizers and synchronous integrating bit detection.[14] These techniques yield nearly theoretical S/N performance. That is, the S/N performance index will be within a db of the ideal S/N versus error probability curve[13] (Figure 7), with effective

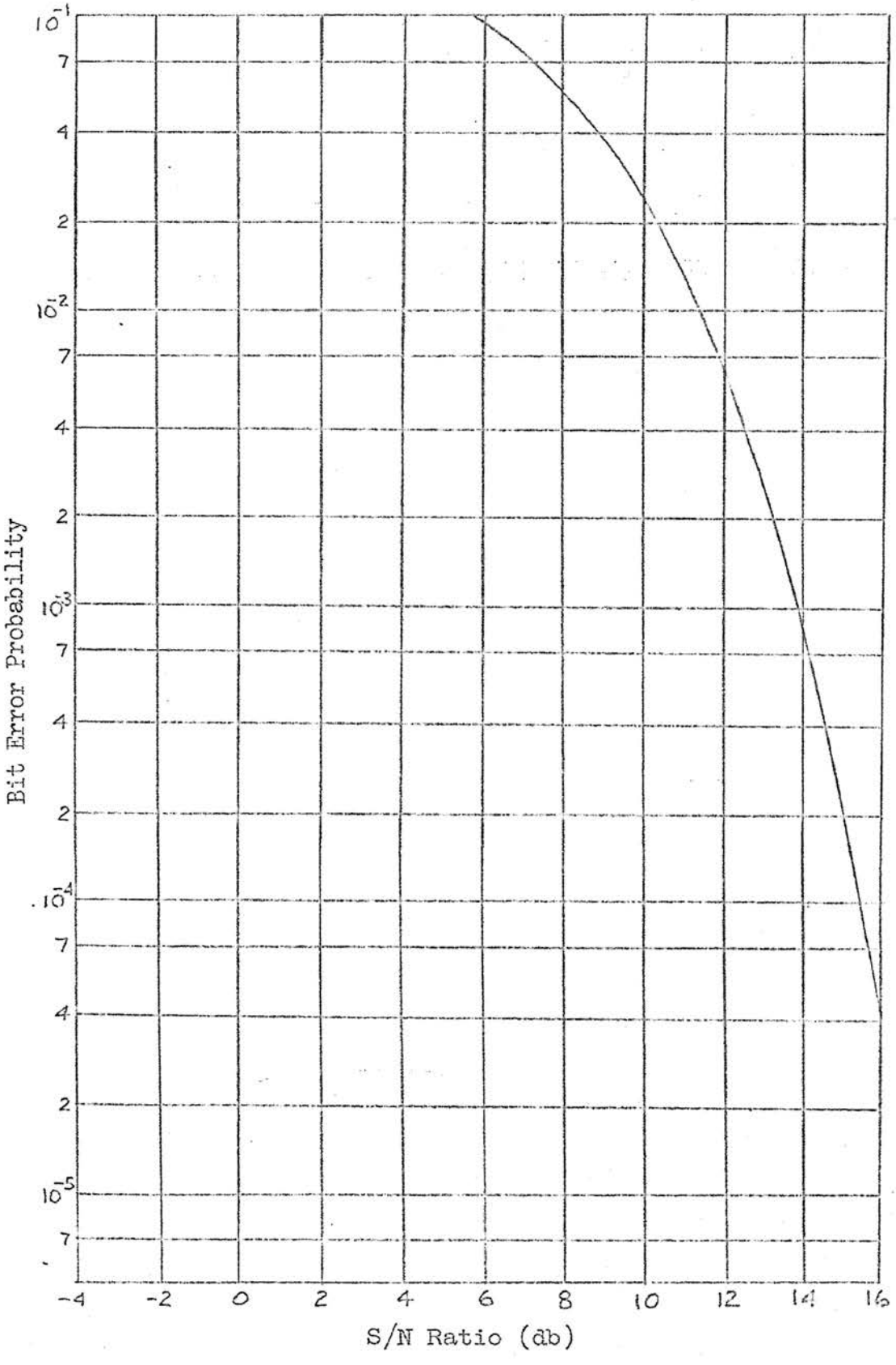


FIGURE 7 - Theoretical Bit Error Probability vs. S/N Ratio

synchronization extending as low as -3 db peak signal to RMS noise voltage. Acquisition time for this method of operation is often stated as being within 100 bit periods with 50% or more transitions under the S/N conditions previously stated. Block diagrams of a typical phase-locked loop PCM bit synchronizer are shown in Figures 8 and 9.

The input signal is passed through an Input Filter to remove noise which lies outside the PCM signal frequency band. The filtered signal is applied to the input of the Bit Detector. The Bit Detector extracts a signal from the combination of signal plus noise and squares it. The squared signal represents mid-amplitude signal transitions and is used to sync the phase-locked oscillator to the incoming signal. The Bit Detector employs a Positive Peak Detector, Negative Peak Detector, and a Floating Differential Comparator. The two peak detectors perform the function which their names imply. The instantaneous voltage difference between the two is the signal peak-to-peak amplitude. As dc offset, signal amplitude, and symmetry change, the signal baseline moves up and down. The peak detectors accurately track this varying signal. The outputs of the two peak detectors, equally weighted, are summed to establish a dc level midway between the peaks. This level is independent of offset, symmetry, data content, and amplitude variations. It is then used to establish a slicing voltage level. The sliced signal and summed reference voltage are then compared in the Floating Differential Comparator which detects whether the signal is more positive or more negative than the reference voltage. The

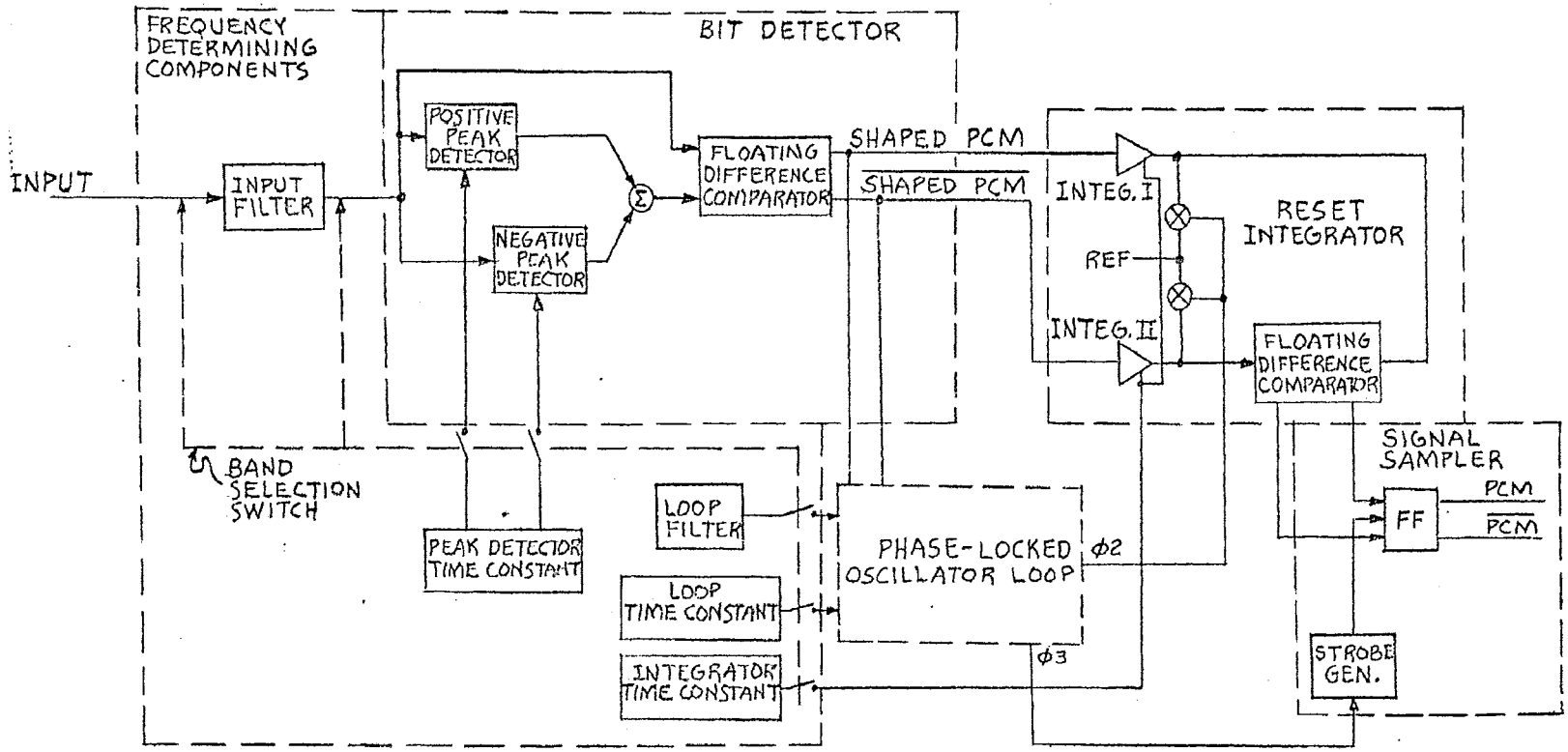


FIGURE 8 - PCM Bit Synchronizer

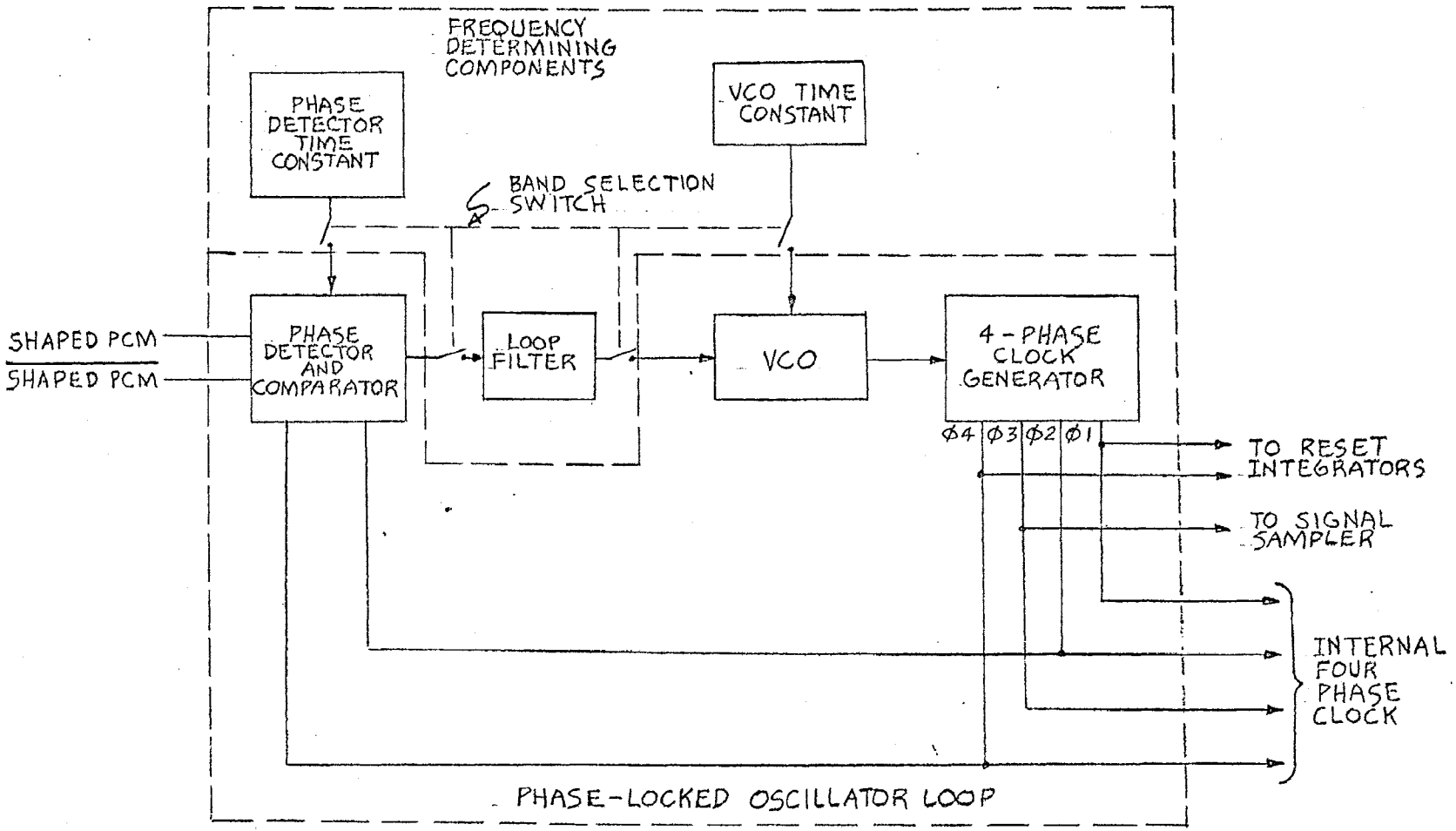


FIGURE 9 - Phase-Locked Oscillator Loop

output is then controlled accordingly. The squared signal output from this dynamic signal conditioning process is then fed to the input of the Phase-Locked Oscillator Loop to establish bit sync. It is also fed to the Reset Integrator to perform bit value decisions.

The Phase-Locked Oscillator Loop generates the output clock at a frequency which is in phase with the incoming PCM signal. The loop consists basically of a Phase Comparator, a Voltage-Controlled Oscillator, and a Four-Phase Clock Generator.

The Phase Comparator compares the phase pulses (generated by the signal transitions) with the local clock pulses. A voltage is then generated which is proportional to the frequency difference between the incoming signal and the local clock. It is positive if the incoming signal is higher than the clock in frequency, negative if lower. This voltage drives the Voltage-Controlled Oscillator which maintains the local oscillator at the same frequency and phase for the incoming signal. Thus bit sync is thereby achieved.

The Shaped PCM and $\overline{\text{Shaped PCM}}$ outputs of the Bit Detector are then fed to the Reset Integrator which makes a "one" or "zero" decision during each bit period. The bit period is determined by the Phase-Locked Loop. More specifically, the squared signal and its complement are fed into two integrators. The integrators are each set to a reference potential at the beginning of a bit period. Integrator I charges for a "one" while Integrator II remains constant. The converse operation results from a "zero". The presence of noise

on the input signal results (on the average) in both integrators charging equally. The Differential Comparator is utilized to determine which of the two is more positive. The bit decision is similarly based. A Signal Sampler makes the bit decision at the end of the bit period. The decision is based upon the value of the Differential Comparator. This operation concludes the bit synchronization and data regeneration process.

An alternate means of obtaining bit sync is called "carrier lock" rather than "phase lock". In this scheme the frequency information is obtained from the RF carrier and the phase information from the video signal. The method is described by E. R. Hill.[14]

IV. FRAME SYNCHRONIZATION

Frame synchronization of a PCM signal consists of identifying a specific bit position in a frame or cyclic block of PCM data. It is then an easy matter to identify any bit or word position in the frame by counting pulses generated by the phase-locked oscillator from the identified bit position. Having established frame sync, the decommutation process can be performed by use of simple sequential logic circuitry.

The method usually employed to obtain frame sync is to include in each frame of data a specific bit pattern. When this pattern is detected at the ground station by means of a "pattern recognizer," a reference bit position is established.

In this section and the remainder of this thesis, it will be assumed for the purpose of analysis that bit synchronization has been accomplished (ergo, a bit error rate is established) and that all bits in a frame other than those in the sync pattern are random in nature. Word synchronization will not be considered in the subsequent development. Thus in attempting to obtain frame sync, it will not be known which groups of bits comprise data words. This restriction further renders it impossible to select a frame sync pattern which would be unique within a frame. Even if the A/D converter in the system were inhibited from accidentally generating the frame sync pattern, it is conceivable, and even likely, that portions of two timewise adjacent data words (with no word sync) would form the frame sync pattern.

As previously mentioned, a "pattern recognizer" is a device which is used to identify a particular bit pattern. It is usually capable of being programmed to allow no more than a given number of errors in the pattern to be recognized. Several types of pattern recognizers are presently in use, the two most common are the analog recognizer (linear matched-filter) and the digital recognizer (shift register comparator). The analog variety have the advantage that the frame sync pattern can be detected directly from the video signal without previous bit detection. The digital variety requires bit detection and data reconstruction before the frame sync pattern can be identified. However, the probability of a false sync indication is so much smaller for the digital recognizer than the analog, that it is generally preferred. Also the linear matched-filter is not flexible with regard to the PCM bit rate. Conversely, the shift register recognizer can be designed to handle a wide range of bit rates. The succeeding development will be performed considering a shift register recognizer (E. R. Hill[12] has analyzed the frame sync problem using a linear-matched filter recognizer).

The frame sync problem will be analyzed here via the three sync operating modes: SEARCH, VERIFY, and LOCK. As previously mentioned it is assumed that bit sync has been accomplished. Thus the bit error rate has been established and will be considered here as an independent variable. The analysis of the three modes of operation of a synchronizer will be considered independent of the sync pattern. The sync pattern employed will have a "random" character with suitable

correlation properties. Further discussion of the properties of sync patterns is contained in Section V.

The sync mode analysis generally follows the one developed by Williard[2,10] and Magnin[9]. However, to the author's knowledge, no one has performed a complete three mode sync analysis as will be done here.

In considering the typical PCM telemetry system of Section II, the results of the analysis will be used to derive optimum parameter settings for the frame synchronizer.

A. SEARCH Mode Analysis

The function of the synchronizer is to maintain sync despite noise, whether it be noise due to equipment fluctuation, atmospheric conditions or tape recorder flutter. For the purpose of this development a 10% bit error rate is assumed. Williard[10] has attempted to justify the 10% random bit error rate as a reasonable threshold for useable data. The succeeding is largely predicated upon this assumed rate. However, it is not a difficult matter to revise the results if a different bit error rate is specified.

The two prime factors determining the sync capabilities of a PCM sync system are: (1) the probability of recognition of the true sync pattern when it is received, and (2) the probability of false recognition of a sync pattern somewhere in the data frame.

The probability of detecting a true sync pattern of length "n" bits, allowing " ϵ " bits to be in error, in a "p" bit error rate environment is[7]

$$P_c = (1-p)^n + \binom{n}{1}(1-p)^{n-1} \cdot p + \binom{n}{2}(1-p)^{n-2} \cdot p^2 + \ldots$$

$$\ldots + \binom{n}{\epsilon}(1-p)^{n-\epsilon} \cdot p^{\epsilon}$$

$$= \sum_{i=0}^{\epsilon} \binom{n}{i}(1-p)^{n-i} \cdot p^i \qquad \text{(IV-1)}$$

The probability of recognizing a set of "n" random bits as a probable sync pattern under the same examining conditions is[7]

$$P_f = (1-0.5)^n + \binom{n}{1}(1-0.5)^{n-1}(0.5) + \binom{n}{2}(1-0.5)^{n-2}(0.5)^2 +$$

$$\ldots + \binom{n}{\epsilon}(1-0.5)^{n-\epsilon} \cdot (0.5)^{\epsilon}$$

$$= (0.5)^n + \binom{n}{1}(0.5)^n + \binom{n}{2}(0.5)^n + \ldots \binom{n}{\epsilon}(0.5)^n$$

$$= (0.5)^n \sum_{i=0}^{\epsilon} \binom{n}{i} \qquad \text{(IV-2)}$$

For a group of "n" random bits, "P_f" is the probability of a false sync indication, and $(1-P_f)$ is the probability of not receiving a false sync indication. The probability of not receiving a false sync indication in "b" sets of "n" random bits ($b \gg n$) is $(1-P_f)^b$. Then the probability of a false sync indication in "b" sets of "n" random bits is

$$F = 1 - (1-P_f)^b \qquad \text{(IV-3)}$$

The probability of false synchronization for a random word of length "n" allowing "ϵ" errors is shown in Table I. A cross-plot of "P_f" versus "P_c" is shown in Figure 10 from Williard[2] for various error rates and word lengths. The same information with a change of variables is presented in Figure 11[14]. A plot of "F" versus "P_f" and "b", also from Williard[2], is given in Figure 12. The information contained in these curves will be used in the ensuing calculations.

When a scan is begun at the beginning of a frame, the probability of not obtaining a false decision before examining the next true sync pattern is (1-F). The probability of a true sync decision on the next sync pattern is then $P_c(1-F)$. The probability of no sync decision when examining the first frame and sync pattern is then

$$1 - \left[F + P_c(1-F)\right] = (1-P_c)(1-F) \qquad \text{(IV-4)}$$

The probability of a true sync decision on the second sync pattern is $P_c(1-F)\left[(1-P_c)(1-F)\right]$ and on the third is $P_c(1-F)\left[(1-P_c)(1-F)\right]^2$. The total probability, T, that the scanning decision is correct can be expressed as

$$T = P_c(1-F) + P_c(1-F)\left[(1-P_c)(1-F)\right] + P_c(1-F)\left[(1-P_c)(1-F)\right]^2 + P_c(1-F)\left[(1-P_c)(1-F)\right]^3 + \ldots.$$

Summing this expression for an infinite number of terms results in[3]

$$T = \frac{P_c(1-F)}{1 - (1-P_c)(1-F)} = \frac{P_c(1-F)}{F + P_c(1-F)} \qquad \text{(IV-5)}$$

TABLE I

P_f - Probability of False Sync in Any n Bit Random Data Word Allowing ϵ Errors

n	$P_f(0)$	$P_f(1)$	$P_f(2)$	$P_f(3)$	$P_f(4)$	$P_f(5)$	$P_f(6)$
1	5.000×10^{-1}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}
2	2.500×10^{-1}	7.500×10^{-1}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}
3	1.250×10^{-1}	5.000×10^{-1}	8.750×10^{-1}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}
4	6.250×10^{-2}	3.125×10^{-1}	6.875×10^{-1}	9.375×10^{-1}	1.000×10^{0}	1.000×10^{0}	1.000×10^{0}
5	3.125×10^{-2}	1.875×10^{-1}	5.000×10^{-1}	8.125×10^{-1}	9.688×10^{-1}	1.000×10^{0}	1.000×10^{0}
6	1.563×10^{-2}	1.094×10^{-1}	3.438×10^{-1}	6.562×10^{-1}	8.906×10^{-1}	9.844×10^{-1}	1.000×10^{0}
7	7.813×10^{-3}	6.250×10^{-2}	2.266×10^{-1}	5.000×10^{-1}	7.734×10^{-1}	9.375×10^{-1}	9.922×10^{-1}
8	3.906×10^{-3}	3.516×10^{-2}	1.445×10^{-1}	3.633×10^{-1}	6.367×10^{-1}	8.555×10^{-1}	9.648×10^{-1}
9	1.953×10^{-3}	1.953×10^{-2}	8.984×10^{-2}	2.539×10^{-1}	5.000×10^{-1}	7.461×10^{-1}	9.102×10^{-1}
10	9.766×10^{-4}	1.074×10^{-2}	5.469×10^{-2}	1.719×10^{-1}	3.770×10^{-1}	6.230×10^{-1}	8.281×10^{-1}
11	4.883×10^{-4}	5.859×10^{-3}	3.271×10^{-2}	1.133×10^{-1}	2.744×10^{-1}	5.000×10^{-1}	7.256×10^{-1}
12	2.441×10^{-4}	3.174×10^{-3}	1.929×10^{-2}	7.300×10^{-2}	1.938×10^{-1}	3.872×10^{-1}	6.128×10^{-1}
13	1.221×10^{-4}	1.709×10^{-3}	1.123×10^{-2}	4.614×10^{-2}	1.334×10^{-1}	2.905×10^{-1}	5.000×10^{-1}
14	6.104×10^{-5}	9.155×10^{-4}	6.470×10^{-3}	2.869×10^{-2}	8.978×10^{-2}	2.120×10^{-1}	3.953×10^{-1}
15	3.052×10^{-5}	4.883×10^{-4}	3.693×10^{-3}	1.758×10^{-2}	5.923×10^{-2}	1.509×10^{-1}	3.036×10^{-1}
16	1.526×10^{-5}	2.594×10^{-4}	2.090×10^{-3}	1.064×10^{-2}	3.841×10^{-2}	1.051×10^{-1}	2.274×10^{-1}
17	7.629×10^{-6}	1.373×10^{-4}	1.175×10^{-3}	6.363×10^{-3}	2.452×10^{-2}	7.173×10^{-2}	1.662×10^{-1}
18	3.815×10^{-6}	7.248×10^{-5}	6.561×10^{-4}	3.769×10^{-3}	1.544×10^{-2}	4.813×10^{-2}	1.189×10^{-1}
19	1.907×10^{-6}	3.815×10^{-5}	3.643×10^{-4}	2.213×10^{-3}	9.605×10^{-3}	3.178×10^{-2}	8.353×10^{-2}
20	9.537×10^{-7}	2.003×10^{-5}	2.012×10^{-4}	1.288×10^{-3}	5.909×10^{-3}	2.069×10^{-2}	5.766×10^{-2}
21	4.768×10^{-7}	1.049×10^{-5}	1.106×10^{-4}	7.448×10^{-4}	3.599×10^{-3}	1.330×10^{-2}	3.918×10^{-2}
22	2.384×10^{-7}	5.484×10^{-6}	6.056×10^{-5}	4.273×10^{-4}	2.172×10^{-3}	8.450×10^{-3}	2.624×10^{-2}
23	1.192×10^{-7}	2.861×10^{-6}	3.302×10^{-5}	2.441×10^{-4}	1.300×10^{-3}	5.311×10^{-3}	1.734×10^{-2}
24	5.960×10^{-8}	1.490×10^{-6}	1.794×10^{-5}	1.386×10^{-4}	7.719×10^{-4}	3.305×10^{-3}	1.133×10^{-2}
25	2.908×10^{-8}	7.749×10^{-7}	9.716×10^{-6}	7.826×10^{-5}	4.553×10^{-4}	2.039×10^{-3}	7.317×10^{-3}
26	1.490×10^{-8}	4.023×10^{-7}	5.245×10^{-6}	4.399×10^{-5}	2.668×10^{-4}	1.247×10^{-3}	4.678×10^{-3}
27	7.451×10^{-9}	2.086×10^{-7}	2.824×10^{-6}	2.462×10^{-5}	1.554×10^{-4}	7.569×10^{-4}	2.962×10^{-3}
28	3.725×10^{-9}	1.080×10^{-7}	1.516×10^{-6}	1.372×10^{-5}	9.000×10^{-5}	4.561×10^{-4}	1.860×10^{-3}
29	1.863×10^{-9}	5.588×10^{-8}	8.121×10^{-7}	7.618×10^{-6}	5.186×10^{-5}	2.731×10^{-4}	1.158×10^{-3}
30	9.313×10^{-10}	2.887×10^{-8}	4.340×10^{-7}	4.215×10^{-6}	2.974×10^{-5}	1.625×10^{-4}	7.155×10^{-4}
31	4.657×10^{-10}	1.490×10^{-8}	2.314×10^{-7}	2.325×10^{-6}	1.698×10^{-5}	9.610×10^{-5}	4.390×10^{-4}
32	2.328×10^{-10}	7.683×10^{-9}	1.232×10^{-7}	1.278×10^{-6}	9.651×10^{-6}	5.654×10^{-5}	2.675×10^{-4}

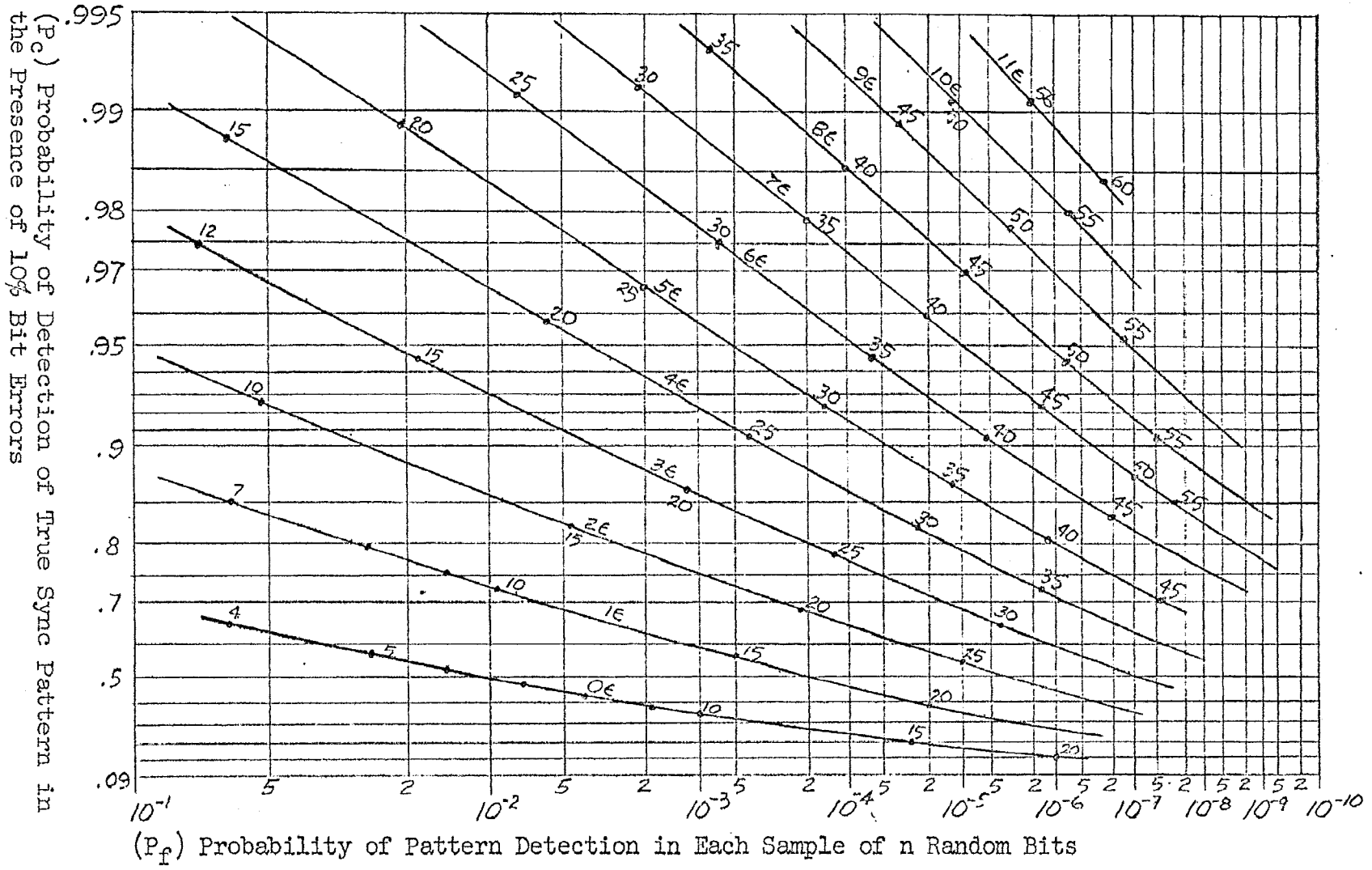


FIGURE 10 - Probability of True Sync Detection (P_c) and False Sync Detection in n Random Bits (P_f) vs. Number of Sync Pattern Bits (n) and Allowable Number of Errors (ϵ).

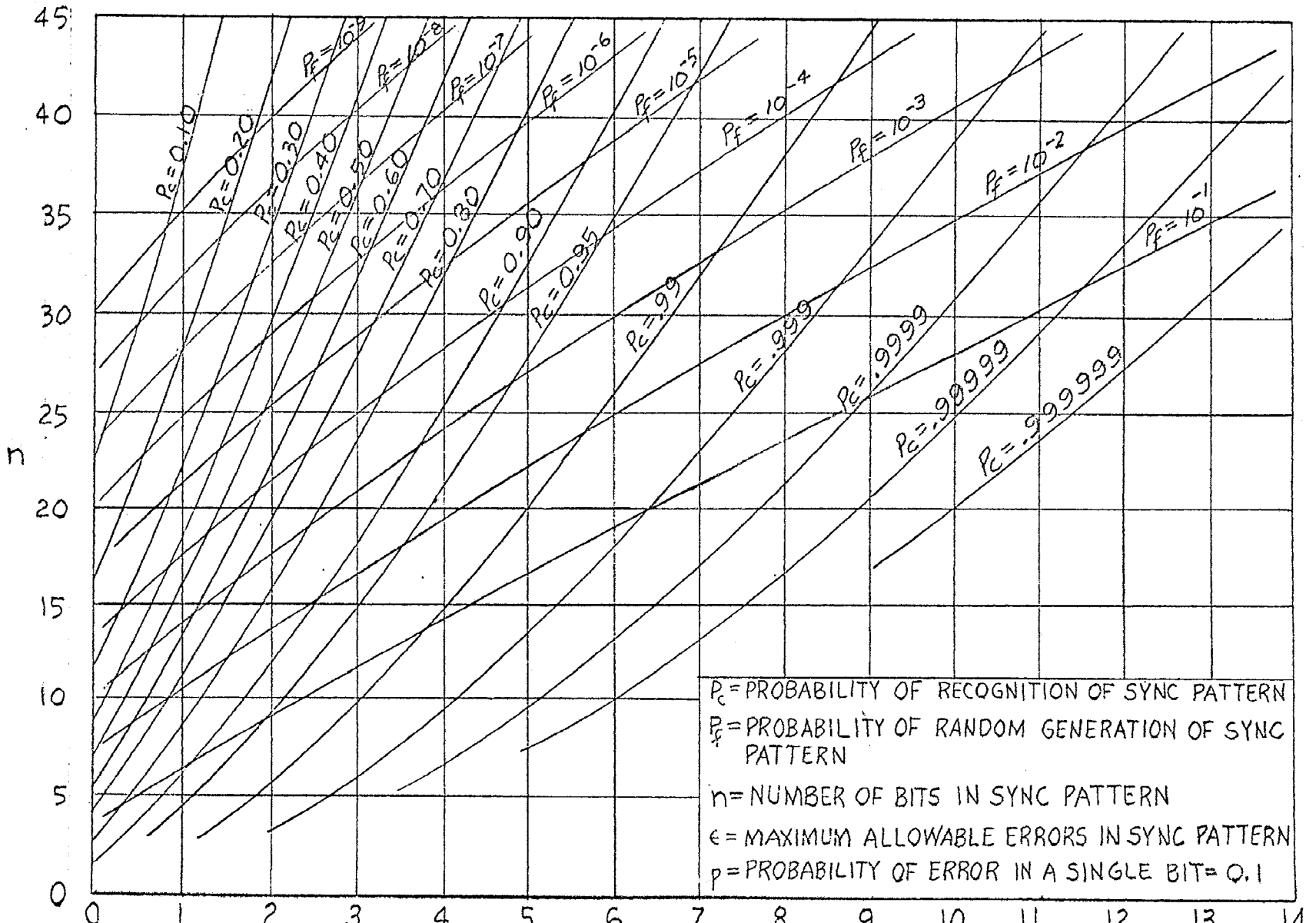
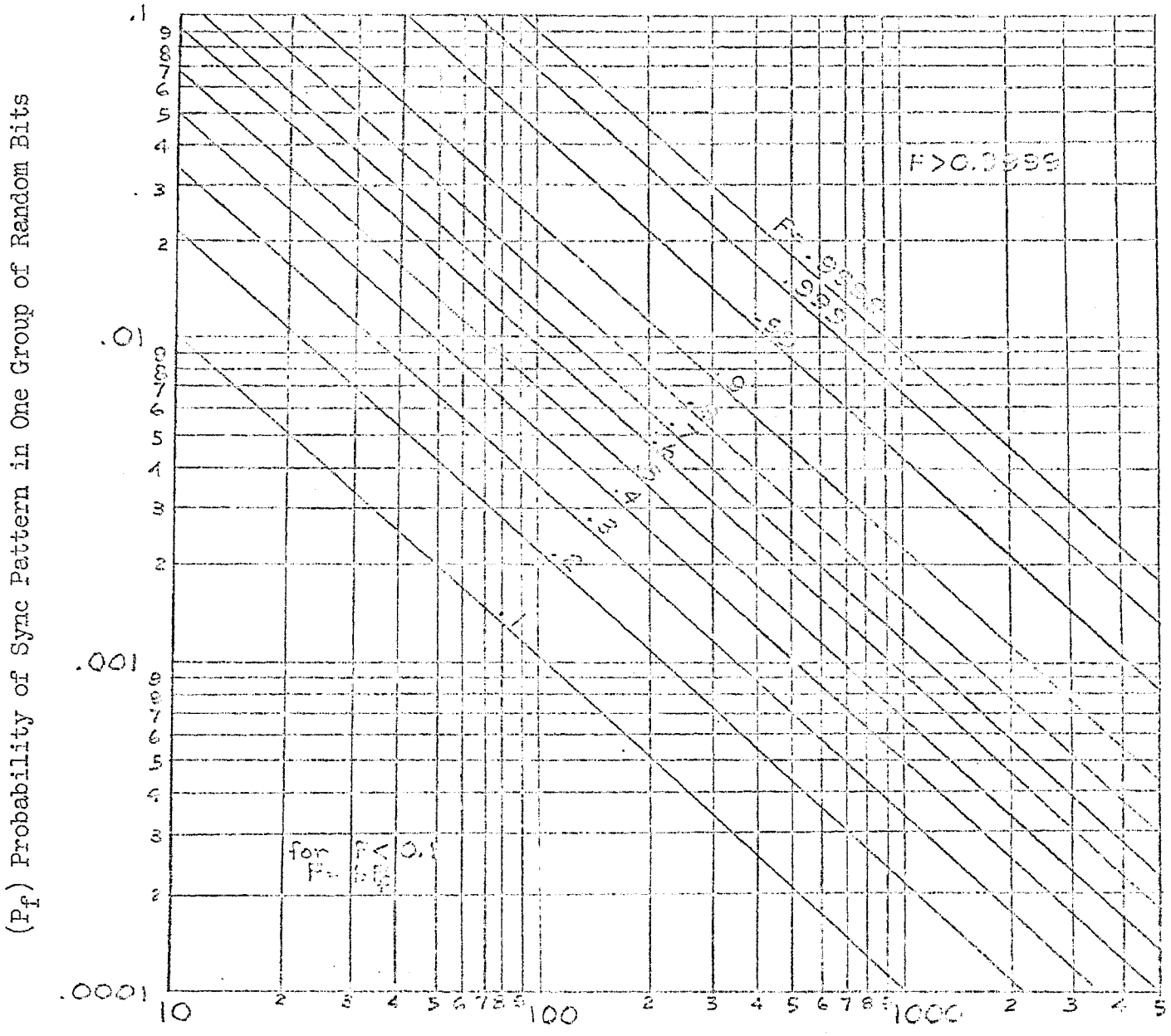


FIGURE 11 - Replot of Figure 10 With Variables Interchanged



(b) Number of Non Sync Patterns Between True Sync Patterns

FIGURE 12 - P_f vs. F and b

Similarly, the probability, W, that the scanning decision is false can be obtained by summing the probability of a false sync decision in each of "b" sets of "n" bits between true sync positions. This process yields the following result:

$$W = \frac{F}{F + P_c(1-F)} \qquad \text{(IV-6)}$$

Logically W + T = 1. This simply states that irrespective of the value of F and P_c, a scan decision (whether right or wrong) is always made.

The next part of this analysis deals with a development of an expression for the mean number of frames needed to reach a true decision in the SEARCH mode. The probability that a decision will be made in the k^{th} frame is

$$\left[F + P_c(1-F) \right]\left[(1-P_c)(1-F) \right]^{k-1} \qquad \text{(IV-7)}$$

Letting the term $\left[(1-P_c)(1-F)\right]$ be represented by "r", Equation (IV-7) can be expressed as

$$(1-r)r^{k-1} \qquad \text{(IV-8)}$$

The total probability of a sync decision being made by the end of the k^{th} frame is[3]

$$P_k = (1-r) + (1-r)r + (1-r)r^2 + \ldots . (1-r)r^{k-1}$$

$$P_k = \sum_{i=1}^{k} (1-r)r^{i-1}$$

$$= 1-r^k \qquad \text{(IV-9)}$$

Then the average number of frames needed to reach a decision is

$$M = \sum_{n=1}^{\infty} nP_n \qquad \text{(IV-10)}$$

where:

n = number of the frame under construction

P_n = probability of sync decision occurring in the n^{th} frame.

Therefore, the above term can be expressed as

$$M = (1-r) + 2r(1-r) + \ldots. n(1-r)r^{n-1}$$

$$= (1-r)(1 + 2r + 3r^2 + \ldots. nr^{n-1})$$

$$= (1 + r + r^2 + r^3 + \ldots.)$$

$$= \frac{1}{1-r} = \frac{1}{F + P_c(1-F)} \qquad \text{(IV-11)}$$

The average number of frames required to reach a true sync decision is then[3]

$$\frac{M}{T} = \frac{1}{P_c(1-F)} \qquad \text{(IV-12)}$$

This can be easily verified, intuitively, since $\frac{T}{M}$, the mean probability of a true decision per frame, is equal to $P_c(1-F)$, the

probability of a true decision in a given frame. To minimize the time spent in SEARCH, the ratio $\frac{M}{T}$ should be minimized.

Using the above expressions and the PCM Commutation scheme described in Section II (Figure 2), two sync parameters will now be derived. These are:

(1) The preferable synchronization word length (this will of necessity be an integral number of data word lengths).

(2) The optimum number of allowable errors in the pattern recognition process.

Table III presents SEARCH mode calculations assuming an error tolerance, ϵ, equal to 3.

TABLE II

SEARCH Mode Parameters

(b=479, ϵ =3, p=0.1, PCM word length = 8 bits)

n	Pc	Pf	F	M/T
8	0.995	0.363	$1 - 4.12\times10^{10}$	2.44×10^{9}
16	0.931	0.011	0.9939	1.76
24	0.780	1.385×10^{-4}	0.064	1.36
32	0.600	1.270×10^{-6}	0.608×10^{-3}	1.667
40	0.420	1.000×10^{-8}	0.479×10^{-5}	2.380

TABLE III

Error Tolerance in the SEARCH Mode

(n = 24, b = 479, p = 0.1)

ϵ	P_c	P_f	F	T
0	.0795	5.96×10^{-8}	2.85×10^{-5}	.999642
1	.2916	1.49×10^{-6}	7.14×10^{-4}	.997555
2	.5636	1.79×10^{-5}	8.59×10^{-3}	.98485
3	.7851	1.38×10^{-4}	6.43×10^{-2}	.91960
4	.9142	7.75×10^{-4}	3.09×10^{-1}	.6710
5	.9715	3.31×10^{-3}	7.95×10^{-1}	.20
6	.9926	1.13×10^{-2}	.996	4.3×10^{-3}
7	.9983	3.20×10^{-2}	.99998	2.43×10^{-5}
8	.9997	7.60×10^{-2}	$1-3.38 \times 10^{-17}$	3.38×10^{-17}

ϵ	W	M	M/T	W/T
0	3.580×10^{-4}	12.55	12.55	3.58×10^{-4}
1	2.445×10^{-3}	3.42	3.42	2.445×10^{-3}
2	1.515×10^{-2}	1.765	1.795	1.54×10^{-2}
3	8.040×10^{-2}	1.250	1.360	8.74×10^{-2}
4	.329	1.065	1.585	.49
5	.800	1.008	5.0	4.0
6	.9957	1.0^+	233.0	231.0
7	.999976	1.0^+	4.11×10^4	4.11×10^4
8	1.0^-	1.0^+	2.96×10^{16}	2.96×10^6

Using a 24 bit frame sync length, Table III is developed by letting the allowable error tolerance vary. This shows that as " ϵ " increases, it becomes less probable that a true sync decision (T) is found. At zero tolerance, $\epsilon = 0$, the probability of a correct decision, T, is high (0.999642). However, it requires a large number of frames to reach this decision (12.55). For a wide error tolerance, $\epsilon = 8$, the decision is made in only one frame, but the probability of finding the true sync word is exceedingly low ($T = 3.38 \times 10^{-17}$). For minimum time in the SEARCH mode, the value M/T = 1.36 at error tolerance $\epsilon = 3$ is selected. The same information is computed and shown in Table IV for bit error probabilities p = 0.1 and p = .001. From the table it can be seen that as the bit error rate decreases, the minimum M/T slowly decreases. However, the rate of change of M/T with ϵ around the minimum is much greater for p = 0.1 than for either p = 0.01 or p = 0.001. Thus an optimum setting for p = 0.1 is sufficient for $p < 0.1$. Values of $p > 0.1$ will not be considered since this value is being used as the threshold of "useable data."

B. VERIFY Mode Analysis

The SEARCH mode scans all incoming bits, one at a time, to find a sync position. Having decided upon the sync position the machine shifts to the VERIFY mode to check the validity of the scanner decision. In the VERIFY mode (as well as the LOCK mode) only the area about the sync position need be investigated. Once the sync word is determined to occur at proper intervals in the VERIFY mode, the machine "accepts" the decision and passes into the LOCK mode. The

TABLE IV

Error Tolerance for Varying Bit Error Probabilities

(n = 24, b = 479, p = 0.01)

ϵ	P_c	P_f	F	T	W	M	M/T	W/T
0	.7855	5.96×10^{-8}	2.85×10^{-5}	.999964	3.62×10^{-5}	1.27	1.27	3.62×10^{-5}
1	.9755	1.49×10^{-6}	7.14×10^{-4}	.99926	7.31×10^{-4}	1.026	1.026	7.31×10^{-4}
2	.9976	1.79×10^{-5}	8.59×10^{-3}	.99137	8.63×10^{-3}	1.002	1.012	8.71×10^{-3}
3	.99923	1.38×10^{-4}	6.43×10^{-2}	.9357	6.43×10^{-2}	1.0+	1.069	6.86×10^{-2}
4	.9999	7.72×10^{-4}	3.09×10^{-1}	.691	3.09×10^{-1}	1.0+	1.446	4.46×10^{-1}
5	1.0-	3.31×10^{-3}	7.95×10^{-1}	.205	7.95×10^{-1}	1.0+	4.850	3.83

(n = 24, b = 479, p = 0.001)

ϵ	P_c	P_f	F	T	W	M	M/T	W/T
0	.9764	5.96×10^{-8}	2.85×10^{-5}	.99971	2.92×10^{-5}	1.023	1.023	2.92×10^{-5}
1	.99990	1.49×10^{-6}	7.14×10^{-4}	.99929	7.14×10^{-4}	1.0+	1.0007	7.14×10^{-4}
2	.99993	1.79×10^{-5}	8.59×10^{-3}	.99141	8.59×10^{-3}	1.0+	1.0086	8.66×10^{-3}
3	1.0-	1.38×10^{-4}	6.43×10^{-2}	.9357	6.43×10^{-2}	1.0+	1.0686	6.81×10^{-2}
4	1.0-	7.72×10^{-4}	3.09×10^{-1}	.6910	3.09×10^{-1}	1.0+	1.446	4.46×10^{-1}
5	1.0-	3.31×10^{-3}	7.95×10^{-1}	.2050	7.95×10^{-1}	1.0+	4.85	3.83

"proper intervals" are determinable, a priori, from the nature of the commutation scheme employed.

A few new expressions, applicable to the SEARCH mode, which are useful in the verify mode analysis will now be developed.

The probability that the true sync word is recognized in the first frame of data is

$$P_{tc} = P_c(1-F) \qquad \text{(IV-13)}$$

and the probability that there will be no detection in one data frame is

$$r = (1-P_c)(1-F) \qquad \text{(IV-14)}$$

Then the probability of a false sync decision in one frame is F, in two frames is rF, in three frames is r^2F, etc. The accumulated probability of a false sync decision after "k" frames is then[7]

$$\begin{aligned} P_{fk} &= F + rF + r^2F + \ldots + r^{k-1}F \\ &= \frac{F}{1-r} \sum_{i=1}^{k} (1-r)r^{i-1} \\ &= \frac{F(1-r^k)}{(1-r)} \end{aligned} \qquad \text{(IV-15)}$$

In a similar manner the accumulated probability of a true sync decision after "k" frames is[7]

$$P_{tk} = \frac{P_{tc}\,(1-r^k)}{(1-r)} \qquad \text{(IV-16)}$$

and likewise the accumulated probability of no sync decision after "k" frames is[7]

$$P_{nk} = r^k \qquad \text{(IV-17)}$$

and

$$P_{fk} + P_{tk} + P_{nk} = 1$$

The above development is applicable to the SEARCH mode of operation. The remainder of this section will deal with the VERIFY operation.

The probability of leaving the SEARCH and VERIFY modes with a false sync decision after "j" check frames is[7]

$$P_{f_{sc}} = P_{fk}\left[P_f(\epsilon_v)\right]^j \qquad \text{(IV-18)}$$

where "ϵ_v" is the allowable number of errors in the VERIFY mode. This expression is also the probability of going into LOCK with a false sync. Similarly, the probability of leaving the SEARCH and VERIFY modes with a true sync decision after "j" check frames is[7]

$$P_{t_{sc}} = P_{tk}\left[P_c(\epsilon_v)\right]^j \qquad \text{(IV-19)}$$

The ratio of these two terms is of interest and may be used as a measure of the check mode effectiveness. This ratio may be expressed as

$$R = \frac{P_{f_{sc}}}{P_{t_{sc}}} = \frac{W}{T}\left[\frac{P_f(\epsilon_v)}{P_c(\epsilon_v)}\right]^j \qquad \text{(IV-20)}$$

Then, "R" may be made as small as required, thereby obtaining as much assurance as one wishes in the VERIFY mode. Table V illustrates the ratio, R, of false to true check mode probabilities allowing the error tolerance in the VERIFY mode to vary. Note that this ratio is independent of the number of frames spent in the SEARCH mode.

However, Table V does not show the effect that the decreased false to true probability ratio has on the probability of leaving the SEARCH and VERIFY mode with a true sync decision. Since the most probable

TABLE V

R, Ratio of False to True VERIFY Mode Probabilities

($n = 24$, $b = 479$, $\epsilon = 3$, $p = 0.1$)

ϵ_v	j = 1	j = 2	j = 3	j = 4	j = 5
0	6.57×10^{-8}	4.96×10^{-14}			
1	4.46×10^{-7}	2.29×10^{-12}	1.17×10^{-17}		
2	2.68×10^{-6}	8.83×10^{-11}	2.81×10^{-15}		
3	1.54×10^{-5}	2.70×10^{-9}	4.25×10^{-13}	8.35×10^{-17}	
4	7.38×10^{-5}	6.25×10^{-8}	5.27×10^{-11}	4.45×10^{-14}	
5	2.98×10^{-4}	1.01×10^{-6}	3.47×10^{-9}	1.17×10^{-11}	4.02×10^{-14}
6	9.94×10^{-4}	1.13×10^{-5}	1.29×10^{-7}	1.47×10^{-9}	1.68×10^{-11}
7	2.80×10^{-3}	8.95×10^{-5}	2.89×10^{-6}	9.18×10^{-8}	2.94×10^{-9}
8	6.65×10^{-3}	5.05×10^{-4}	3.84×10^{-5}	2.92×10^{-6}	2.22×10^{-7}

number of frames spent in SEARCH is M/T, the probability of leaving the SEARCH and VERIFY modes with a true sync decision is

$$\overline{P_{t_{sc}}} = P_{t_{sc}}(\epsilon)\left[\frac{1-r^{M/T}}{1-r}\right]\cdot\left[P_c(\epsilon_v)\right]^j \qquad \text{(IV-21)}$$

Similarly for a false sync decision

$$\overline{P_{f_{sc}}} = F(\epsilon)\left[\frac{1-r^{M/T}}{1-r}\right]\cdot\left[P_f(\epsilon_v)\right]^j \qquad \text{(IV-22)}$$

It can be shown that

$$\frac{\overline{P_{f_{sc}}}}{\overline{P_{t_{sc}}}} = \frac{P_{f_{sc}}}{P_{t_{sc}}}$$

or

$$\overline{R} = R \qquad \text{(IV-23)}$$

Therefore, Table V gives a description of the variation of $\overline{R}$ or R as a function of "ϵ_v" for different "j".

Table VI then shows the probability of leaving the SEARCH and VERIFY modes with the true sync decision for the same variables employed in Table V.

Finally Tables V and VI can be examined to determine the CHECK mode parameters. If the chance of false sync must be less than one in a million, it can be seen that there are five possible choices of ϵ_v and j as indicated by Table V. These are (1, 1), (5,2), (6,3),

(7,4) and (8,5) giving ϵ_v and j in that order. From Table VI these combinations yield the following values of $\overline{P}_{t_{sc}}$ respectively: 0.238, 0.775, 0.799, 0.816, 0.816. It appears that the best choices for the VERIFY mode parameters are $\epsilon_v = 5$, $j = 2$. This results in $R = \overline{R} = 1.0 \times 10^{-6}$ and $\overline{P}_{t_{sc}} = 0.775$.

TABLE VI

$\overline{P}_{t_{sc}}$, Probability of Leaving the SEARCH and VERIFY Modes With The True Sync Decision ($n = 24$, $b = 479$, $\epsilon = 3$, $p = 0.1$)

ϵ_v	j = 1	j = 2	j = 3	j = 4	j = 5
0	.065	.005	.0004	.00003	.000003
1	.238	.069	.002	.0006	.00018
2	.459	.258	.146	.0816	.046
3	.640	.503	.395	.310	.244
4	.754	.680	.621	.568	.519
5	.791	.770	.748	.736	.706
6	.811	.805	.799	.794	.787
7	.816	.816	.816	.816	.816
8	.816	.816	.816	.816	.816

C. LOCK Mode Analysis

The function of the LOCK mode is to check the sync position of each frame while the data is being processed. Bit counters which are used to establish data words are also used to count the bits per frame and determine the sync word position. Like the VERIFY mode,

only the sync word position need be checked for proper synchronization.

Typically after the SEARCH and VERIFY criteria are satisfied, the sync machinery switches to the LOCK mode. In this study, the pattern recognizer is used to check the sync position. The error tolerance can be increased at this point if desired, since the probability of finding the correct sync word (by the time the LOCK mode is entered) is high. If the new number of allowable errors is ϵ_L, then the sync pattern must appear during each frame in the proper position with a maximum of ϵ_L errors in order to maintain the LOCK mode operation.

In the LOCK mode the two significant operational characteristics which are significant are the mean number of frames required to reject a false sync and the mean number of frames required to reject a true sync. If a false sync decision was made in the SEARCH and VERIFY modes, and operation passed to the LOCK mode, the probability of rejecting the false sync pattern is:

Frame 1 . . . . . $(1-P_f')$

Frame 2 . . . . . $(1-P_f')P_f'$

Frame 3 . . . . . $(1-P_f')(P_f')^2$

.

.

.

Frame n . . . . . $(1-P_f')(P_f')^{n-1}$

and the mean number of frames before rejection will be[3]

$$J = (1-P_f')\left[1 + 2P_f' + 3P_f'^2 + \ldots\right]$$

$$= \frac{1}{(1-P_f')} \qquad \text{(IV-24)}$$

Similarly, the mean number of frames before rejection of a true sync pattern in the LOCK mode is

$$K = \frac{1}{(1-P_c')} \qquad \text{(IV-25)}$$

The terms P_f' and P_c' in the above are identical to the terms P_f and P_c developed in the SEARCH mode analysis, with the exception that the allowable number of errors in the LOCK mode is ϵ_L instead of ϵ.

Thus, using sync systems of the type discussed here, the mean number of frames required to define the true sync

$$L = \frac{(M + j)}{\overline{P}t_{sc}} + JR \qquad \text{(IV-26)}$$

The first term of this expression is the mean number of frames required to exit the VERIFY mode with a true decision. The second term is the product of the mean number of frames "J" required to realize that a scanner-verify decision is false, and the ratio "R" of the wrong to correct decisions of the SEARCH-VERIFY mode. The second term represents the time spent in the LOCK mode when the system is not in synchronization. Since the system is not in sync, on the average, until L frames pass, and since the system remains in sync for K frames, the

time the system is out of sync is directly related to the percentage of data lost; this is

$$\% \text{ Data Lost} = \frac{L}{L + K} \quad 100 \qquad \text{(IV-27)}$$

Table VII is data pertinent to the LOCK mode analysis of the system as previously considered in the SEARCH and VERIFY modes. From the table (note the $\epsilon = 3$ column) if the parameter ϵ_L is chosen to be 7, we see that less than 1% of the data will be lost. This table illustrates the need for the proper documentation strategy for a specific PCM system.

Table VIII is included to show the same analysis for lower bit error probabilities. As expected, decreasing bit error rates increase the percentage of time spent in sync; the analysis for $p = 0.1$ is valid for lower bit error rates.

TABLE VII

LOCK Mode Analysis

($n = 24$, $b = 479$, $p = 0.1$, $j = 2$, $\epsilon_v = 5$)

ϵ	Pt_{sc}	T	W/T	R	M
0	.61	.99964	3.580×10^{-4}	4.46×10^{-9}	12.55
1	.655	.99755	2.445×10^{-3}	2.84×10^{-8}	3.42
2	.720	.98485	1.540×10^{-2}	1.79×10^{-7}	1.765
3	.769	.9196	8.740×10^{-2}	1.01×10^{-6}	1.25
4	.623	.671	.49	5.69×10^{-6}	1.065
5	.189	.200	4:0	4.64×10^{-5}	1.008

TABLE VII (Continued)

			$\epsilon = 0$		$\epsilon = 1$		$\epsilon = 2$		$\epsilon = 3$		$\epsilon = 4$		$\epsilon = 5$	
ϵ_L	J	K	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL
0	1+	1.0865	23.85	95.5	8.3	88.5	5.24	82.7	4.22	79.6	5.075	82.5	15.95	93.5
1	1+	1.410		94.5		85.4		78.7		75.0		78.3		92.0
2	1+	2.290		91		78.2		69.6		64.8		69.0		87.5
3	1+	4.65		83.6		64.0		52.6		47.0		52.2		77.5
4	1+	11.65		67.2		41.6		31.0		26.6		30.3		57.8
5	1+	35		40.5		19.2		13.3		10.75		12.7		31.3
6	1.0114	135		15		5.8		3.76		3.04		3.63		10.5
7	1.033	589		3.9		1.39		.93		.72		.86		2.64
8	1.0825	2940		.81		.28		.178		.04		.17		.54

TABLE VIII

LOCK Mode Analysis with Varying Bit Error Rate

(n = 24, b = 479, p = 0.01, j = 0)

			$\epsilon = 0$		$\epsilon = 1$		$\epsilon = 2$		$\epsilon = 3$		$\epsilon = 4$		$\epsilon = 5$	
ϵ_L	J	K	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL
0	1+	4.66	1.27	21.4	1.0267	18.1	1.0207	18	1.1372	19.6	1.892	28.8	8.68	65
1	1+	40.8		3.02		2.52		2.51		2.76		4.42		17.5
2	1+	416		.304		.246		.246		.272		.452		2.04
3	1+	1300		.098		.079		.079		.087		.145		.667
4	1+	$\infty -$		0+		0+		0+		0+		0+		0+

(n = 24, b = 479, p = 0.001, j = 0)

			$\epsilon = 0$		$\epsilon = 1$		$\epsilon = 2$		$\epsilon = 3$		$\epsilon = 4$		$\epsilon = 5$	
ϵ_L	J	K	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL	L	%DL
0	1+	42.4	1.023	2.36	1.001	2.31	1.017	2.35	1.136	2.61	1.892	4.29	8.68	17
1	1+	10^4		.0102		.01001		.01017		.01136		.01892		.086
2	1+	$\infty -$		0+		0+		0+		0+		0+		0+
3	1+	$\infty -$		0+		0+		0+		0+		0+		0+

V. FRAME SYNC PATTERNS

Pulse Code Modulation telemetry systems require that sync information be transmitted along with the coded data for sync purposes. In this paper the frame sync problem has been considered, and in conjunction with this effort the development of optimum frame sync patterns will be included here. A frame sync pattern consists of a number of predetermined bits which are transmitted in a unique word position or positions during each frame. A pattern recognizer or digital autocorrelator is then employed in the receiving equipment. Its purpose is to determine the sync position as part of the decommutation process.

The foregoing frame sync analysis has assumed a random character for the bits between sync positions. This assumes the frame sync pattern has a random nature. The digital autocorrelation function of a random word has a single large spike at the correlation position and is therefore easy to detect.

A correlation function with several spikes or a broad, high-level value near the correlation position could lead to mistakes in positioning the word. This is especially true in the presence of noise.

The choice of a sync word is more involved than merely choosing a pattern with a good autocorrelation function. First, since the word is bracketed between data, the correlator (for certain search positions) "sees" some data bits and some pattern bits in the

correlator. This is known as an overlap condition. One degree of overlap means one pattern bit in the correlator, two degrees means two bits, etc. The maximum degree of overlap is n-1 bits for an "n" bit sync pattern. During the overlap conditions, then, the sync pattern must be such that correlation with partial data bits and a partial sync pattern is no worse than with only random data bits. Second, erroneous data bits due to noise must be considered. Some "good" autocorrelation words become quite "bad" when a few errors are tolerated. A possible number of errors must then be considered in selecting the proper word.

There are almost two distinct schools of thought concerning the specific choice of a primary sync word. The first could be called the Phillips and Goode[5,8] approach. The second might be called the Williard[4] approach, although his efforts were incomplete and were further improved by Masching[9]. It is the second approach that will be generally followed here.

The Phillips and Goode approach defines a sample variance which is proportional to the square of the difference between the number of bit agreements and conflicts in an overlap condition. A code having a minimum total sample variance (the sum of the sample variances from an overlap of 1 to n-1) is considered optimum since it most greatly resembles the autocorrelation of a random word. Techniques for generating pseudo-random Barker and Legendre codes generally generate minimum sample variance codes.

The Williard approach is based on minimizing the probability of false occurrence of the pattern in the received signal. For a code pattern of proper length there is a low probability of false sync in the random (data) region. The Williard approach is used to make the probability of false sync in each degree of pattern overlap less than the probability of false sync in the random region. The Phillips and Goode approach is to generate a minimum total autocorrelation function sequence. This does not necessarily give a pattern with a minimum probability of false sync in a noisy data stream for each degree of overlap.

The remainder of this section will be devoted to the development of an optimum code pattern utilizing the Williard-Masching approach.

A. Primary Sync Word Development

In Section IV the probability of a false sync indication in any n-bit random word, allowing "ϵ" errors, was shown to be

$$P_f = \frac{1}{2^n} \sum_{i=0}^{\epsilon} \binom{n}{i} \qquad \text{(IV-2)}$$

In Section IV the total number of bits between sync positions (recall that these were treated as random bits) was "b". There are actually, however, only B = b-2(n-1) data bits, which may be considered as random. The remaining bits are pattern bits and are therefore "fixed."

The probability of a false sync indication in pattern overlap areas will now be considered. The probability of a false sync

indication in an "m" overlap condition (i.e. when the pattern recognizer is examining "m" pattern bits and "n-m" random bits, allowing zero errors) is

$$H_k(0) = \left[\frac{1}{2}\right]^k p^c \cdot q^{\emptyset} \qquad \text{(V-1)}$$

where:

k = n-m = no. of random bits in the pattern recognizer.

c = no. of conflicts for error free transmission.

$\emptyset$ = no. of agreements for error free transmission

p = probability of bit error.

q = 1-p.

Then, allowing one error in the pattern recognition process, we have

$$\begin{aligned} H_k(1) = & \left[\frac{1}{2}\right]^k \left[c \cdot p^{c-1} \cdot q^{\emptyset+1}\right] \\ & + \left[\frac{1}{2}\right]^k \left[\emptyset \cdot p^{c+1} \cdot q^{\emptyset-1}\right] \\ & + \left[\frac{1}{2}\right]^k \left[k \cdot p^{c} \cdot q^{\emptyset}\right] + H_k(0) \end{aligned} \qquad \text{(V-2)}$$

and for two errors

$$\begin{aligned} H_k(2) = & \left[\frac{1}{2}\right]^k \left[\binom{c}{2} \cdot p^{c-2} \cdot q^{\emptyset+2}\right] \\ & + \left[\frac{1}{2}\right]^k \left[\binom{\emptyset}{2} \cdot p^{c+2} \cdot q^{\emptyset-2}\right] \\ & + \left[\frac{1}{2}\right]^k \left[\binom{k}{2} \cdot p^{c} \cdot q^{\emptyset}\right] + H_k(1) + H_k(0) \end{aligned} \qquad \text{(V-3)}$$

Then for ϵ errors

$$H_k(\epsilon) = \left[\frac{1}{2}\right]^k \left[\binom{c}{\epsilon} p^{c-\epsilon} \cdot q^{\phi+\epsilon}\right] + \left[\frac{1}{2}\right]^k \left[\binom{\phi}{\epsilon} p^{c+\epsilon} \cdot q^{\phi-\epsilon}\right] + \left[\frac{1}{2}\right]^k \left[\binom{k}{\epsilon} p^{c} \cdot q^{\phi}\right] + H_k(\epsilon-1) + \ldots H_k(1) + H_k(0) \qquad (V-4)$$

Williard[4] defines a term, R_m, which is the probability of false sync in an "m" overlap condition, allowing zero errors, normalized with respect to the probability of a false sync indication in "n" random bits, allowing zero errors. It can be expressed as

$$R_m = \frac{H_k(0)}{P_f(0)} = \frac{\left[\frac{1}{2}\right]^{n-m} \cdot p^c \cdot q^{\phi}}{\frac{1}{2}^n}$$

$$= 2^m p^c \cdot q^{\phi} \qquad (V-5)$$

To satisfy the criteria that the probability of false sync be less in every degree of overlap than in the random region, R_m must be less than 1.0 for every "m."

In Section IV the code length determined for the hypothetical PCM system was 24 bits. To continue the development of that system, Table IX presents R_m for degrees of overlap from 1 through 23 and for enough bit conflicts to find a value of $R_m < 1.0$. It can be seen that for 1 through 3 degrees of overlap, at least 1 conflict is required for $R_m < 1.0$; for 4 through 7 degrees, at least 2 conflicts,

TABLE IX

Normalized False Sync Probabilities (p = 0.1)

Overlap	Conflicts	R_m	Overlap	Conflicts	R_m
0	0	1	11	0	642.654
				1	71.406
1	0	1.8		2	7.934
	1	0.2		3	0.8815
2	0	3.24	12	0	1156.923
	1	0.36		1	128.547
				2	14.283
3	0	5.832		3	1.587
	1	0.648		4	0.1763
4	0	10.494	13	0	2082.024
	1	1.166		1	231.336
	2	0.1296		2	25.704
				3	2.856
5	0	18.891		4	0.3173
	1	2.099			
	2	0.2333	14	0	3747.789
				1	416.421
6	0	34.011		2	46.269
	1	3.779		3	5.141
	2	0.4199		4	0.5712
7	0	61.218	15	0	6744.708
	1	6.802		1	749.412
	2	0.7558		2	83.268
				3	9.252
8	0	110.241		4	1.028
	1	12.249		5	0.1142
	2	1.361			
	3	0.1512	16	0	12137.850
				1	1348.650
9	0	198.369		2	149.850
	1	22.041		3	16.650
	2	2.449		4	1.850
	3	0.2721		5	0.2056
10	0	356.967	17	0	21848.130
	1	39.663		1	2427.570
	2	4.407		2	269.730
	3	0.4897		3	29.970
				4	3.330
				5	0.370

TABLE IX (Continued)

Overlap	Conflicts	R_m
18	0	39320.073
	1	4368.897
	2	485.433
	3	53.937
	4	5.993
	5	0.666
19	0	70799.751
	1	7866.639
	2	874.071
	3	97.119
	4	10.791
	5	1.199
	6	0.1332
20	0	127368.633
	1	14152.077
	2	1572.453
	3	174.717
	4	19.413
	5	2.157
	6	0.2397
21	0	229346.286
	1	25482.924
	2	2831.436
	3	314.604
	4	34.956
	5	3.884
	6	0.4315
22	0	413270.829
	1	45918.981
	2	5102.109
	3	566.102
	4	62.901
	5	6.989
	6	0.7765
23	0	742954.518
	1	82550.502
	2	9172.278
	3	1019.142
	4	113.238
	5	12.582
	6	1.398
	7	0.1553

etc. Table X summarizes the number of conflicts required in each degree of overlap for $R_m < 1.0$.

Williard further defined the quantity $R_t = \sum_{m=1}^{n-1} R_m$ and stated that a good code will have $R_m < 1.0$ in every degree of overlap. He also stated that an optimum code will have a minimum R_t. However, he developed no method, other than one of trial and error which requires extensive computer evaluation, for generating "good" or "optimum" codes.

A method will now be developed to generate a good sync code by using the required number of conflicts in the various degrees of overlap to establish relationships among the pattern bits. From these relationships a pattern having correlation properties better than random data can be simply generated.

In Table XI the bit relationships for all possible conflicts in each degree of overlap is listed. The number of conflicts required in each degree of overlap for R_m 1.0 is also repeated there. To choose a code for which $R_m < 1.0$ for each "m," the number of bit relationships which must be satisfied in each degree of overlap must equal the required number of conflicts. The code which is selected for use in the sample system of Section IV is 66374524, expressed in octal notation. This code satisfies the bit relationships in Table XI which are denoted by asterisks. In passing, it is noted that the complement, reflection, and reflected complement of the above code all have the same correlation properties and satisfy the same

TABLE X

No. of Conflicts Required for $R_m < 1.0$ in Each Overlap Condition

Degree of Overlap	No. of Conflicts Required	Degree of Overlap	No. of Conflicts Required
0	0	14	4
1	1	15	5
2	1	16	5
3	1	17	5
4	2	18	5
5	2	19	6
6	2	20	6
7	2	21	6
8	3	22	6
9	3	23	7
10	3		
11	3		
12	4		
13	4		

TABLE XI

Sync Pattern Bit Relationships for

Conflicts in Each Degree of Overlap

Degree of Overlap	Conflicts Required for $R_m < 1.0$	Bit Relationships For All Possible Conflicts		
1	1	$*B_{24}=\overline{B}_1$		
2	1	$*B_{23}=\overline{B}_1$ $B_{24}=\overline{B}_2$		
3	1	$B_{22}=\overline{B}_1$ $*B_{23}=\overline{B}_2$ $B_{24}=\overline{B}_3$		
4	2	$*B_{21}=\overline{B}_1$ $B_{22}=\overline{B}_2$ $B_{23}=\overline{B}_3$ $*B_{24}=\overline{B}_4$		
5	2	$B_{20}=\overline{B}_1$ $*B_{21}=\overline{B}_2$ $*B_{22}=\overline{B}_3$	$B_{23}=\overline{B}_4$ $B_{24}=\overline{B}_5$	
6	2	$*B_{19}=\overline{B}_1$ $B_{20}=\overline{B}_2$ $B_{21}=\overline{B}_3$	$B_{22}=\overline{B}_4$ $*B_{23}=\overline{B}_5$ $B_{24}=\overline{B}_6$	
7	2	$B_{18}=\overline{B}_1$ $*B_{19}=\overline{B}_2$ $*B_{20}=\overline{B}_3$	$B_{21}=\overline{B}_4$ $B_{22}=\overline{B}_5$ $B_{23}=\overline{B}_6$	$B_{24}=\overline{B}_7$
8	3	$*B_{17}=\overline{B}_1$ $B_{18}=\overline{B}_2$ $*B_{19}=\overline{B}_3$	$B_{20}=\overline{B}_4$ $B_{21}=\overline{B}_5$ $B_{22}=\overline{B}_6$	$*B_{23}=\overline{B}_7$ $B_{24}=\overline{B}_8$

TABLE XI (Continued)

Degree of Overlap	Conflicts Required for $R_m < 1.0$	Bit Relationships For All Possible Conflicts		
9	3	$B_{16}=\overline{B}_1$	$*B_{19}=\overline{B}_4$	$B_{22}=\overline{B}_7$
		$*B_{17}=\overline{B}_2$	$B_{20}=\overline{B}_5$	$*B_{23}=\overline{B}_8$
		$B_{18}=\overline{B}_3$	$B_{21}=\overline{B}_6$	$B_{24}=\overline{B}_9$
10	3	$*B_{15}=\overline{B}_1$	$*B_{19}=\overline{B}_5$	$B_{23}=\overline{B}_9$
		$B_{16}=\overline{B}_2$	$*B_{20}=\overline{B}_6$	$B_{24}=\overline{B}_{10}$
		$B_{17}=\overline{B}_3$	$B_{21}=\overline{B}_7$	
		$B_{18}=\overline{B}_4$	$B_{22}=\overline{B}_8$	
11	3	$B_{14}=\overline{B}_1$	$B_{18}=\overline{B}_5$	$B_{22}=\overline{B}_9$
		$*B_{15}=\overline{B}_2$	$B_{19}=\overline{B}_6$	$B_{23}=\overline{B}_{10}$
		$B_{16}=\overline{B}_3$	$*B_{20}=\overline{B}_7$	$B_{24}=\overline{B}_{11}$
		$*B_{17}=\overline{B}_4$	$B_{21}=\overline{B}_8$	
12	4	$B_{13}=\overline{B}_1$	$*B_{17}=\overline{B}_5$	$*B_{21}=\overline{B}_9$
		$*B_{14}=\overline{B}_2$	$*B_{18}=\overline{B}_6$	$B_{22}=\overline{B}_{10}$
		$B_{15}=\overline{B}_3$	$B_{19}=\overline{B}_7$	$B_{23}=\overline{B}_{11}$
		$B_{16}=\overline{B}_4$	$B_{20}=\overline{B}_8$	$B_{24}=\overline{B}_{12}$
13	4	$*B_{12}=\overline{B}_1$	$B_{17}=\overline{B}_6$	$B_{22}=\overline{B}_{11}$
		$B_{13}=\overline{B}_2$	$*B_{18}=\overline{B}_7$	$B_{23}=\overline{B}_{12}$
		$B_{14}=\overline{B}_3$	$*B_{19}=\overline{B}_8$	$B_{24}=\overline{B}_{13}$
		$*B_{15}=\overline{B}_4$	$B_{20}=\overline{B}_9$	
		$B_{16}=\overline{B}_5$	$B_{21}=\overline{B}_{10}$	
14	4	$B_{11}=\overline{B}_1$	$B_{16}=\overline{B}_6$	$B_{21}=\overline{B}_{11}$
		$*B_{12}=\overline{B}_2$	$B_{17}=\overline{B}_7$	$B_{22}=\overline{B}_{12}$
		$*B_{13}=\overline{B}_3$	$B_{18}=\overline{B}_8$	$B_{23}=\overline{B}_{13}$
		$*B_{14}=\overline{B}_4$	$B_{19}=\overline{B}_9$	$B_{24}=\overline{B}_{14}$
		$*B_{15}=\overline{B}_5$	$B_{20}=\overline{B}_{10}$	

TABLE XI (Continued)

Degree of Overlap	Conflicts Required for $R_m < 1.0$	Bit Relationships For All Possible Conflicts			
15	5	*$B_{10}=\overline{B}_1$	$B_{15}=\overline{B}_6$	$B_{20}=\overline{B}_{11}$	
		*$B_{11}=\overline{B}_2$	*$B_{16}=\overline{B}_7$	$B_{21}=\overline{B}_{12}$	
		$B_{12}=\overline{B}_3$	*$B_{17}=\overline{B}_8$	$B_{22}=\overline{B}_{13}$	
		$B_{13}=\overline{B}_4$	$B_{18}=\overline{B}_9$	$B_{23}=\overline{B}_{14}$	
		*$B_{14}=\overline{B}_5$	$B_{19}=\overline{B}_{10}$	$B_{24}=\overline{B}_{15}$	
16	5	$B_9=\overline{B}_1$	$B_{15}=\overline{B}_7$	$B_{21}=\overline{B}_{13}$	
		*$B_{10}=\overline{B}_2$	$B_{16}=\overline{B}_8$	$B_{22}=\overline{B}_{14}$	
		$B_{11}=\overline{B}_3$	*$B_{17}=\overline{B}_9$	$B_{23}=\overline{B}_{15}$	
		*$B_{12}=\overline{B}_4$	*$B_{18}=\overline{B}_{10}$	$B_{24}=\overline{B}_{16}$	
		$B_{13}=\overline{B}_5$	$B_{19}=\overline{B}_{11}$		
		$B_{14}=\overline{B}_6$	*$B_{20}=\overline{B}_{12}$		
17	5	$B_8=\overline{B}_1$	*$B_{13}=\overline{B}_6$	*$B_{18}=\overline{B}_{11}$	$B_{23}=\overline{B}_{16}$
		$B_9=\overline{B}_2$	$B_{14}=\overline{B}_7$	$B_{19}=\overline{B}_{12}$	$B_{24}=\overline{B}_{17}$
		$B_{10}=\overline{B}_3$	*$B_{15}=\overline{B}_8$	$B_{20}=\overline{B}_{13}$	
		*$B_{11}=\overline{B}_4$	$B_{16}=\overline{B}_9$	$B_{21}=\overline{B}_{14}$	
		*$B_{12}=\overline{B}_5$	$B_{17}=\overline{B}_{10}$	$B_{22}=\overline{B}_{15}$	
18	5	*$B_7=\overline{B}_1$	$B_{12}=\overline{B}_6$	$B_{17}=\overline{B}_{11}$	$B_{22}=\overline{B}_{16}$
		$B_8=\overline{B}_2$	*$B_{13}=\overline{B}_7$	$B_{18}=\overline{B}_{12}$	$B_{23}=\overline{B}_{17}$
		*$B_9=\overline{B}_3$	$B_{14}=\overline{B}_8$	$B_{19}=\overline{B}_{13}$	$B_{24}=\overline{B}_{18}$
		*$B_{10}=\overline{B}_4$	$B_{15}=\overline{B}_9$	$B_{20}=\overline{B}_{14}$	
		*$B_{11}=\overline{B}_5$	$B_{16}=\overline{B}_{10}$	$B_{21}=\overline{B}_{15}$	
19	6	*$B_6=\overline{B}_1$	$B_{11}=\overline{B}_6$	*$B_{16}=\overline{B}_{11}$	$B_{21}=\overline{B}_{16}$
		*$B_7=\overline{B}_2$	$B_{12}=\overline{B}_7$	$B_{17}=\overline{B}_{12}$	$B_{22}=\overline{B}_{17}$
		*$B_8=\overline{B}_3$	$B_{13}=\overline{B}_8$	$B_{18}=\overline{B}_{13}$	$B_{23}=\overline{B}_{18}$
		$B_9=\overline{B}_4$	*$B_{14}=\overline{B}_9$	$B_{19}=\overline{B}_{14}$	$B_{24}=\overline{B}_{19}$
		*$B_{10}=\overline{B}_5$	$B_{15}=\overline{B}_{10}$	$B_{20}=\overline{B}_{15}$	

TABLE XI (Continued)

Degree of Overlap	Conflicts Required for $R_m < 1.0$	Bit Relationships For All Possible Conflicts			
20	6	$B_5 = \overline{B}_1$	$B_{10} = \overline{B}_6$	$B_{15} = \overline{B}_{11}$	$B_{20} = \overline{B}_{16}$
		$*B_6 = \overline{B}_2$	$B_{11} = \overline{B}_7$	$*B_{16} = \overline{B}_{12}$	$B_{21} = \overline{B}_{17}$
		$B_7 = \overline{B}_3$	$*B_{12} = \overline{B}_8$	$*B_{17} = \overline{B}_{13}$	$B_{22} = \overline{B}_{18}$
		$B_8 = \overline{B}_4$	$B_{13} = \overline{B}_9$	$*B_{18} = \overline{B}_{14}$	$B_{23} = \overline{B}_{19}$
		$B_9 = \overline{B}_5$	$B_{14} = \overline{B}_{10}$	$B_{19} = \overline{B}_{15}$	$*B_{24} = \overline{B}_{20}$
21	6	$B_4 = \overline{B}_1$	$B_{10} = \overline{B}_7$	$B_{16} = \overline{B}_{13}$	$B_{22} = \overline{B}_{19}$
		$B_5 = \overline{B}_2$	$*B_{11} = \overline{B}_8$	$B_{17} = \overline{B}_{14}$	$B_{23} = \overline{B}_{20}$
		$B_6 = \overline{B}_3$	$*B_{12} = \overline{B}_9$	$*B_{18} = \overline{B}_{15}$	$B_{24} = \overline{B}_{21}$
		$*B_7 = \overline{B}_4$	$*B_{13} = \overline{B}_{10}$	$B_{19} = \overline{B}_{16}$	
		$B_8 = \overline{B}_5$	$B_{14} = \overline{B}_{11}$	$B_{20} = \overline{B}_{17}$	
		$*B_9 = \overline{B}_6$	$B_{15} = \overline{B}_{12}$	$B_{21} = \overline{B}_{18}$	
22	6	$*B_3 = \overline{B}_1$	$*B_9 = \overline{B}_7$	$B_{15} = \overline{B}_{13}$	$B_{21} = \overline{B}_{19}$
		$B_4 = \overline{B}_2$	$B_{10} = \overline{B}_8$	$B_{16} = \overline{B}_{14}$	$B_{22} = \overline{B}_{20}$
		$*B_5 = \overline{B}_3$	$B_{11} = \overline{B}_9$	$B_{17} = \overline{B}_{15}$	$B_{23} = \overline{B}_{21}$
		$*B_6 = \overline{B}_4$	$B_{12} = \overline{B}_{10}$	$B_{18} = \overline{B}_{16}$	$B_{24} = \overline{B}_{22}$
		$*B_7 = \overline{B}_5$	$B_{13} = \overline{B}_{11}$	$B_{19} = \overline{B}_{17}$	
		$*B_8 = \overline{B}_6$	$B_{14} = \overline{B}_{12}$	$B_{20} = \overline{B}_{18}$	
23	7	$B_2 = \overline{B}_1$	$*B_8 = \overline{B}_7$	$*B_{14} = \overline{B}_{13}$	$B_{20} = \overline{B}_{19}$
		$*B_3 = \overline{B}_2$	$B_9 = \overline{B}_8$	$B_{15} = \overline{B}_{14}$	$B_{21} = \overline{B}_{20}$
		$*B_4 = \overline{B}_3$	$*B_{10} = \overline{B}_9$	$B_{16} = \overline{B}_{15}$	$B_{22} = \overline{B}_{21}$
		$B_5 = \overline{B}_4$	$B_{11} = \overline{B}_{10}$	$B_{17} = \overline{B}_{16}$	$B_{23} = \overline{B}_{22}$
		$*B_6 = \overline{B}_5$	$B_{12} = \overline{B}_{11}$	$B_{18} = \overline{B}_{17}$	$B_{24} = \overline{B}_{23}$
		$B_7 = \overline{B}_6$	$*B_{13} = \overline{B}_{12}$	$B_{19} = \overline{B}_{18}$	

bit relationships. It is through the process of satisfying the required number of bit relationships in each degree of overlap that a good sync code is generated. In generating the code above a bit error rate of 0.1 was used and no errors were allowed in the recognition process. A code which is better than another at $\epsilon=0$, however, does not necessarily remain better as the error tolerance is increased. To insure that the code chosen is satisfactory under allowable error conditions other than $\epsilon=0$, the probability of false sync in the pattern region has to be evaluated under those conditions. The term R_m used in the previous work should properly be termed $R_m(0)$. To determine the quality of a code allowing "ϵ" errors, it is necessary to evaluate the term $R_m(\epsilon)$ where

$$R_m(\epsilon) = \frac{h_k(\epsilon)}{p_f(\epsilon)} \qquad \text{(V-6)}$$

It is also necessary to determine that the probability of false sync in the overlap region is still less in each degree of overlap than the probability of false sync in an "n" bit random word allowing "ϵ" errors. Table XII gives the values of $R_m(\epsilon=3)$ for the sync code 663745248_8 and verifies the validity of this code under maximum allowable error conditions.

An "optimum" code may be found by a trial and error approach (as advocated by Masching[9]) by finding a minimum $R_t(\epsilon)$. This approach requires a great deal of computer time, however, since extensive calculations would have to be performed on each code, and

TABLE XII

R_m (ϵ =3) For The Sync Word 663745248

m	R_m (ϵ =3)	m	R_m (ϵ =3)
1	7.7922×10^{-1}	20	5.4906×10^{-2}
2	1.0101×10^{-3}	21	3.9250×10^{-4}
3	2.7922×10^{-3}	22	4.5094×10^{-3}
4	5.5700×10^{-3}	23	2.7056×10^{-5}
5	9.6681×10^{-2}		
6	2.1501×10^{-2}		
7	3.7085×10^{-2}		
8	2.4603×10^{-2}		
9	2.5036×10^{-3}		
10	2.1140×10^{-2}		
11	2.7706×10^{-4}		
12	1.4791×10^{-2}		
13	2.6623×10^{-2}		
14	1.4719×10^{-2}		
15	0.9524		
16	1.5526×10^{-1}		
17	5.0144×10^{-2}		
18	1.6948×10^{-2}		
19	1.8038×10^{-5}		

the number of possible 24 bit codes is 2^{24}. The effort required for obtaining an optimum code is hardly justified, since the probability of false sync with a good code (developed as previously shown) is less in each degree of overlap than in the random data region.

B. Subframe Sync Word Considerations

The preceeding portion of this section concentrated on the primary synchronization process. When subcommutation is employed as is done in the "example" PCM system introduced in Section II, a form of synchronization is required to position the subframe. The primary sync process scanned each bit position to determine the sync position. Given the primary sync word position and a prior information about the location of the subframe sync word within the frame, it remains only for the machine to detect the word by "looking" in the proper word position.

This secondary process, then, does not necessitate the use of a word with any particular autocorrelation properties as was necessary in the primary sync word case. However, during the primary sync process, while the machine is scanning for the primary sync word, the subframe sync word will pass through the pattern recognizer. When this occurs, because the subframe sync word is not random and is repetitive, it is necessary to select a subframe sync word that has a low probability of being mistaken for the primary sync word. That is, the subframe sync word should have a low cross-correlation value when correlated with the primary sync word.

A good subframe sync word is relatively easy to generate for a system as considered here, since the primary criteria is that the probability of false sync for any degree of overlap (of the primary and subframe sync words) be less than the probability in a random data region. It should be noted at this point that a subframe sync word need not be of the same length as the primary sync word since it is not employed in a scan operation.

For the PCM system of Section II, however, a subframe sync word of 24 bits will be used. Therefore it will be necessary for the subframe sync word to have an $R_m < 1.0$ for every "m" from 1 to 24. In this case "m" is the degree of overlap of the primary and the subframe sync words. Under the same condition, i.e. p = 0.1, Tables IX, X, and XI of this section are valid for the subframe sync process as well as the primary. However, they do not contain the 24th degree overlap condition.

Using the information contained in these tables, primarily Table XI, a subframe sync word was obtained by satisfying the required number of bit conflict relationships. The subframe sync word 57143224_8 thus has an $R_m < 1.0$ for every m from 1 to 24 when correlated with the primary sync word 66374524_8.

VI. CONCLUSIONS

In this paper the frame sync process has been analyzed by the development of the equations defining the SEARCH, VERIFY, and LOCK modes of operation.

The SEARCH mode equations presented are sufficient to determine the optimum synchronization word length and the optimum number of allowable errors in the SEARCH mode pattern recognition process for a PCM telemetry system.

In the VERIFY mode development the equation

$$R = \frac{W}{T}\left[\frac{P_f(\epsilon)}{P_c(\epsilon)}\right] \qquad \text{(IV-20)}$$

was ultimately derived and a means of determining the optimum number of allowable errors in the VERIFY mode was demonstrated. This was accomplished by examining the behavior of the terms "R" and "$\overline{P}_{t_{sc}}$" with the variations in "ϵ_v" in Tables V and VI.

Finally, in the LOCK mode analysis, the equation

$$L = \frac{(M+j)}{P_{t_{sc}}} + JR \qquad \text{(IV-26)}$$

was derived, which related the mean number of frames to define the true sync to the mean number of frames in the LOCK mode before rejection of a false sync pattern. The percentage of data lost in the sync process was then presented as

$$\% \text{ Data Lost} = \frac{L}{L+K} (100) \qquad \text{(IV-27)}$$

This equation was then shown to be instrumental in determining the allowable number of errors in the LOCK mode.

The equations presented and developed in the SEARCH, VERIFY, and LOCK modes were used in Section IV to demonstrate the selection of optimum frame sync parameters. This was accomplished using the hypothetical PCM system described in Section II.

Additionally, a primary and subframe sync word development was presented in Section V. Equations (V-1) through (V-5) from Williard[4] and Masching[9], which are useful in determining the probability of false sync in varying degrees of pattern overlap were included. Using these equations an "optimum" sync code can be generated via a digital computer routine. However, a simple method was presented in Section V for deriving "good" primary and subframe sync codes by satisfying the required number of relationships specified in Table XI.

Finally, the method presented for deriving primary and subframe sync codes was used in Section V to obtain a primary and subframe sync code for the hypothetical PCM system of Section II. Using the codes obtained, the probability of false sync in any pattern overlap condition was lower than in the random region.

The equations presented here for deriving the sync system parameters for the hypothetical system can easily be adapted to any PCM telemetry system.

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VITA

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