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DIGITAL SIMULATION OF A SIGNAL
CONDITIONER/BIT SYNCHRONIZER

BY

QUENTIN REED WEBB, 1940 -

A THESIS

Presented to the Faculty of the Graduate School of the

UNIVERSITY OF MISSOURI - ROLLA

In Partial Fulfillment of the Requirements for the Degree

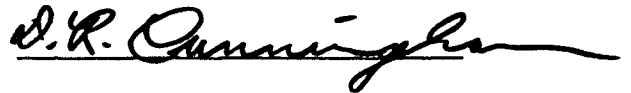
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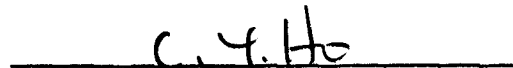
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Approved by



(Advisor)





ABSTRACT

A bit rate filter type signal conditioner/bit synchronizer used in a split-phase PCM system is modeled digitally in three stages to determine overall system performance. General computer algorithms are developed to approximate independent operation of each major segment within the device. Bit rate effects and signal time-base error are investigated yielding the characteristic G-curves for the phase detector. These characteristics facilitate subsequent analysis of a linear equivalent digital-data-transition tracking phase-locked loop under several typical time-base error input conditions. Using bit error probabilities as performance criteria, the conditioner/synchronizer is found to perform adequately at signal-to-noise ratios exceeding +10dB. For inputs below this value, the detection capability deteriorates rapidly with decreasing signal levels.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS

BIT	randomly generated binary data symbol
T	digital filter sampling interval, in seconds
TT	
WC	digital filter cutoff frequency, in radians
WN	
NRZ	non-return-to-zero signal
J	jitter condition imposed upon the input signal
KSHIFT	
IK	input bit sequence
TL	tracking loop
SIGI	split-phase representation of data word input to the signal conditioner
NOISEI	white Gaussian noise at conditioner input
SIGF	input data word processed by a digital filter
NOISEF	filtered noise
SIGC	comparator signal output
SIGPS	phase shifter signal output
SIGJ	the original data word jittered by the amount KSHIFT
VCO	split-phase clock in phase detector
PDOUT	phase detector output or error signal
SNR	input signal-to-noise ratio
PSNR	
R_s	
GCURV	loop nonlinearity value
SCURV	equivalent noise spectral density
BVAR	phase error variance
PVAR	

NOIND	noise output from integrate/reset device
VARR R	noise power normalized to the input SNR
CLK	clock used in split-phase/NRZ converter
SIGNJ SIGJR SIGJL	input data word with zero jitter, jitter right, and jitter left conditions, respectively
SNRZ SJRNRZ SJLNRZ	input signal under designated jitter converted to NRZ
SNJ SJR SJL	signal output of integrate/reset device or filter/sample value under specified condition of signal jitter
PENJ PEJR PEJL	error probabilities under designated jitter condition for each of the possible bit sequences IK
PEZJ PEFJR PEFJL	error probabilities for zero jitter or fixed jitter right or left averaged over the possible bit sequences
SNJF SJRF SJLF	output signal from the bit rate/2 filter in filter/sample mode for jitter as noted
PETOT	total probability of error for the system
B	mean square value of the noise
TIMERR	input error signal to the digital data- transition tracking phase-locked loop
PHASER	phase error in the tracking loop
RMSERR	rms value of the phase error in tracking loop

I. INTRODUCTION

In telemetry systems, symbol synchronization presents a serious problem at low signal-to-noise ratios. The detection of a split-phase pulse code modulated (S ϕ -PCM) signals in the presence of noise requires precise timing synchronization for use in associated bit detection circuitry. Recent advances in self-synchronizing digital-data transition tracking receivers provide high reliability systems for both low input signal-to-noise ratios (SNR) and widely varying data rates^{1,2}.

A signal conditioner/bit synchronizer is a device employed to reconstruct transmitter digital data from the recorded analog data recovered by the receiver. A general form of conditioner/synchronizer contains a timing estimation element, or synchronizer, and a bit detection portion to reproduce the digital data which was originally transmitted. Timing estimation is perhaps the most critical problem, since erroneous timing synchronization precludes correct bit detection. In many instances a decision directed phase-locked loop is implemented to supply the receiver with the knowledge of the time instants when the incoming modulation will change states. Self-synchronizing systems are useful in accomplishing this without loss of additional transmitter power solely for synchronization.

This thesis will model a specific bit rate filter variety of signal conditioner/bit synchronizer and investigate the associated performance characteristics. Developing an accurate representation of this device necessitates extensive digital simulation. The wide difference in frequency between the bit rate and tracking rate segments of the model prohibits direct simulation and simultaneous analysis on the digital computer. Therefore, bit rate behavior and tracking loop analysis must be approximated separately, with the combined results correlated to produce a meaningful description of the conditioner/synchronizer.

The basic structure of the model is shown in Figure 1. The synchronizer portion of the unit is essentially independent of the bit detection and decision elements of the conditioner. The synchronizer constructs an error signal from the transitions in the received input data, and a phase-locked tracking loop then provides a timing estimate for use in the bit detection elements. This tracking process defines the temporal position of a bit within the received serial $S\phi$ -PCM data. The synchronizer must estimate the input bit rate frequency and phase from this received variable-rate-data stream which is corrupted with additive white Gaussian noise. By specifying the statistics of the phase noise input to the tracking loop, a linear equivalent of the loop can be digitally simulated.

($s\phi$ -PCM)
SIGNAL PLUS ADDITIVE
WHITE GAUSSIAN NOISE

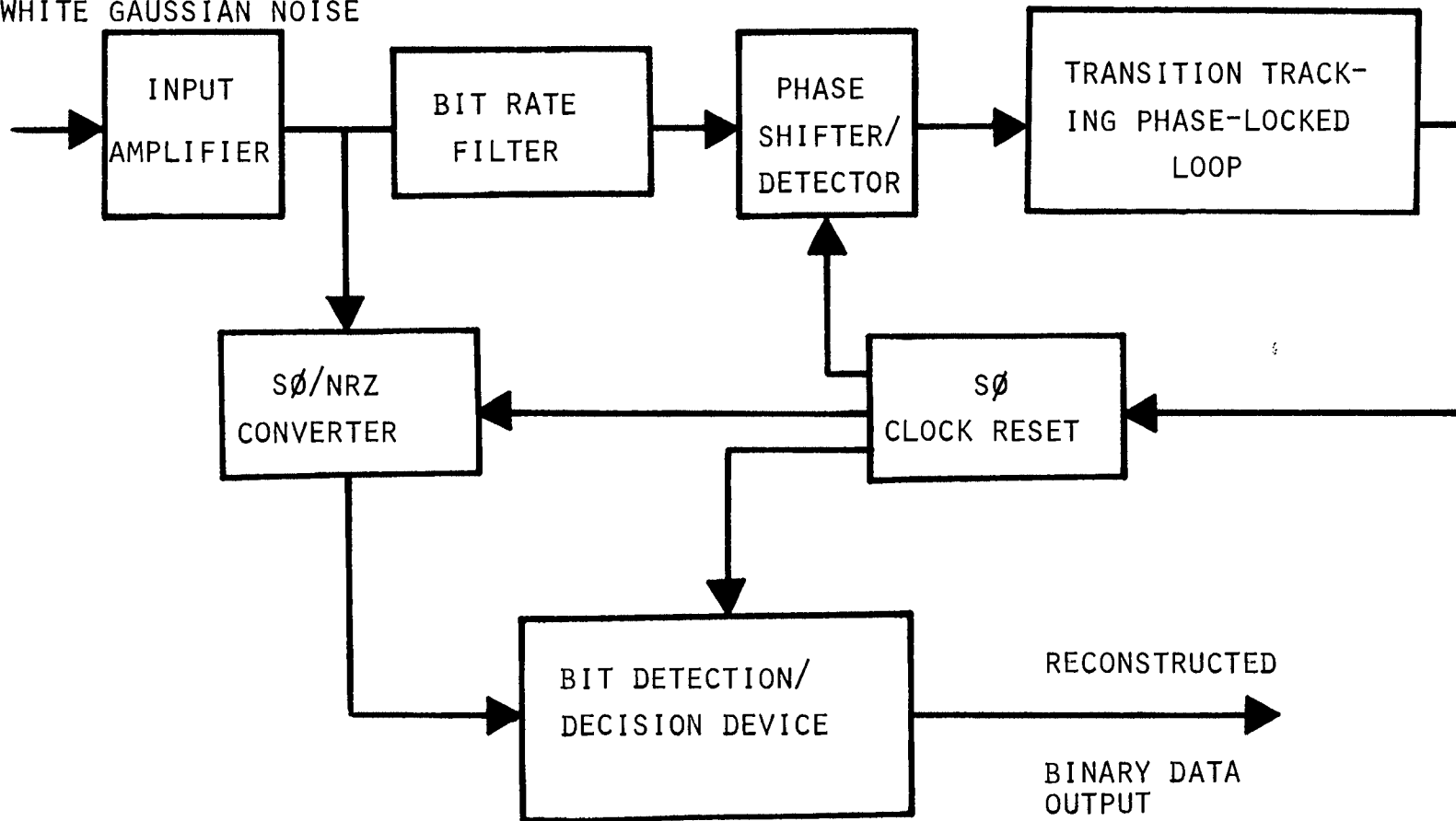


Figure 1. General Model of Signal Conditioner/Bit Synchronizer

The bit detection/decision portion of the signal conditioner extracts the timing information from the synchronizer and applies it to the specific detection/decision mode selected. The received $S\phi$ -PCM signal and additive noise are passed through a split-phase to non-return-to-zero ($S\phi$ -NRZ) converter, then the waveform is processed by either one of two methods which may be selected. These modes are termed "filter/sample" and "integrate/reset" methods in this thesis. Both signal and additive noise values are determined at a selected time increment and the resultant ratio is compared to a threshold level within the decision device. Finally, a "replica" of the originally transmitted data is constructed to conclude the conditioner/synchronizer processing.

Since limited computer time prevents a direct Monte Carlo simulation, the overall performance of the model is approximated by combining the results observed in both bit rate and tracking rate studies. The total probability of error for the system is determined by the input signal-to-noise ratio, the adjacent bit value, and the time-base jitter or error in the signal. The signal conditioner/bit synchronizer is thus characterized by the probability of bit error as a function of the input signal-to-noise ratio and the phase-error variance in the tracking loop.

II. REVIEW OF PREVIOUS LITERATURE

Extensive research has been conducted in the field of self-synchronizing digital-data communication systems. The analysis of both theoretical and practical realizations of the early-late gate and differentiating varieties of synchronizers has received special attention^{4,5}.

The more recent studies of self-synchronizing systems include the work of Wintz and Luecke⁷. An optimum synchronizer is developed and a subsequent sub-optimum, maximum likelihood model is simulated digitally using Monte Carlo techniques. Their synchronizer realization is formed by a cascade of a low-pass filter, a square-law nonlinearity, and a bandpass filter centered at the bit rate. A significant result of this study indicated that the square pulse which is commonly used in signaling does not perform as well as either the "half-sine" or "raised-cosine" pulses. Using these modified pulse shapes, near optimum performance can be achieved by the sub-optimum system.

Simon¹ analyzes the phase noise performance in a digital-data transition tracking loop, which resembles a Costas loop. An error signal, formed by the product of the in-phase and mid-phase channels, is used to drive the loop to synchronization. The loop nonlinearity curve and the spectral density of the equivalent noise (about the origin) are found as functions of the normalized phase

error within the tracking loop. These curves permit use of a linear equivalent data-transition tracking loop model. Simon determines these nonlinearities analytically, and then applies the Fokker-Planck equation to find the mean-square phase noise in the tracking loop as a function of the input signal-to-noise ratio.

Performance of the early-late gate and differentiating class of PCM bit synchronizers has been investigated by Stiffler⁵, with the signal shape and the type of feedback signal used within the loop varied to find subsequent effects upon performance. Both "raised-cosine" and the standard rectangular pulses are the signal shapes tested, and the loop feedback signals are either sampling pulses or sinusoids. Using phase error variance as the performance criterion, Stiffler concludes that the overall synchronizer performance is dependent upon both parameter variations and the specific combination of elements used.

Tracking loop performance is analyzed by Lindsey and Anderson³, where an early-late gate synchronizer is mechanized. When integration is performed only over a portion of the symbol time in the mid-phase channel, an improvement in loop SNR is noted. The tracking loop is developed to have an adaptive loop bandwidth dependent upon whether it is in acquisition or tracking modes. Again the loop nonlinearity curves and phase error variance (noise) versus signal-to-noise ratio characteristics are specified.

Hurd and Anderson² propose a digital model synchronizer for low signal-to-noise ratio coded systems. Phase detector design includes a variation of the mid-phase channel integration window for changes in the magnitude of timing error input. Monte Carlo techniques are used to digitally simulate the phase detector and the characteristic G or S-curves formulated. The variation in phase-lock loop parameters, loop bandwidth, damping factor, and loop signal-to-noise ratio are found for low input SNR's. Two cases are considered. For simplicity in design of the loop filter, the phase estimate is quantized to one bit. Phase-lock loop parameters are analyzed for both the quantized and non-quantized cases. The improved phase detector used by Hurd and Anderson provides a higher loop SNR, thus better synchronization, without a reduction in the tracking loop bandwidth.

McBride and Sage⁶ develop an optimum maximum-a-posteriori (MAP) estimation algorithm to provide timing estimation for self-synchronizing digital systems. Use of the Karhunen-Loeve expansion permits analytical investigation of the synchronization problem, finding the MAP estimate of phase error θ . Several sub-optimal synchronizers are proposed.

III. STATEMENT OF THE PROBLEM

In the analysis of baseband telemetry receiver operation, a simulation of the associated signal conditioner/bit synchronizer can be accomplished to specify performance criteria for the system. Direct simulation cannot be performed efficiently because of the wide difference in frequencies between bit rate effects and the tracking loop analysis. By formulating these models separately, and deriving system characteristics utilizing results from the combined models, the general problem of approximating the conditioner/synchronizer is developed in this thesis.

The mechanization of the model requires three basic algorithms. Initially, the phase detector of this particular conditioner must be specified to provide the phase error characteristics under varying input signal-to-noise levels and signal-noise or time-base jitter conditions. The loop nonlinearities, or G-curves, and the equivalent noise spectral density, or S-curves, can be constructed from digital Monte Carlo methods. These well known curves are required for the subsequent digital data transition-tracking loop analysis. Behavior of the linear equivalent transition tracking loop can be readily simulated through use of the IBM 360 Continuous System Modeling Program (CSMP) package. Loop performance can be described analytically, and the phase error statistics

generated in the CSMP digital implementation. Specific types of time-base jitter are impressed upon the tracking loop, and the phase noise characteristics are investigated under anticipated low signal-to-noise ratios. Tracking loop filter bandwidth may be altered to simulate the fundamental acquisition and tracking modes of operation.

To determine a meaningful qualitative analysis of the conditioner/synchronizer performance, the system's probability of bit error as a function of input signal-noise and signal-to-noise levels must be characterized. Final computer algorithms assert two methods of approximating detection, the filter-sample mode and the integrate-reset mode. Each of the four equally likely bit sequences, hence transition combinations, are generated with varying degrees of jitter, and the probability of bit error for a fixed value of jitter is obtained by averaging over the possible bit sequences encountered. Overall system performance may then be calculated by integrating out the signal jitter. Application of the Central Limit Theorem, with specific phase error jitter variance determined in the tracking loop analysis, permits this integration. Resolution of these algorithms provides a reasonable means of determining a signal conditioner/bit synchronizer realization for the split-phase PCM telemetry receiver.

IV. SYSTEM DESIGN DESCRIPTION

The signal conditioner/bit synchronizer considered here can be classified as a bit rate filter variety as opposed to the early-late gate type. Simulation methodology was conducted in the three stages depicted in Figure 2. The phase detector was mechanized on the IBM 360 digital computer and the Monte Carlo method used to generate a random eleven bit data word split-phase input signal to the synchronizer. The loop nonlinearity and equivalent noise spectra are derived from the error signal outputs of the phase detector. Tracking loop simulation was effected by modeling the linear equivalent phase-locked loop on the IBM 360 using the IBM CSMP. Three types of input time error signals were tracked, with variations in the input signal-to-noise ratio and loop filter bandwidth made to characterize the loop performance by the rms phase error value and phase error variance. The G and S curves developed in the initial bit rate effects portion of the study are incorporated into this phase of synchronizer simulation. Performance of the bit detection segment of the conditioner can be specified by the probability of bit error as a function of both input signal-to-noise ratio and the time base jitter in the signal. It is assumed that the jitter is essentially constant over a large number of symbol intervals, and that the response of the transition

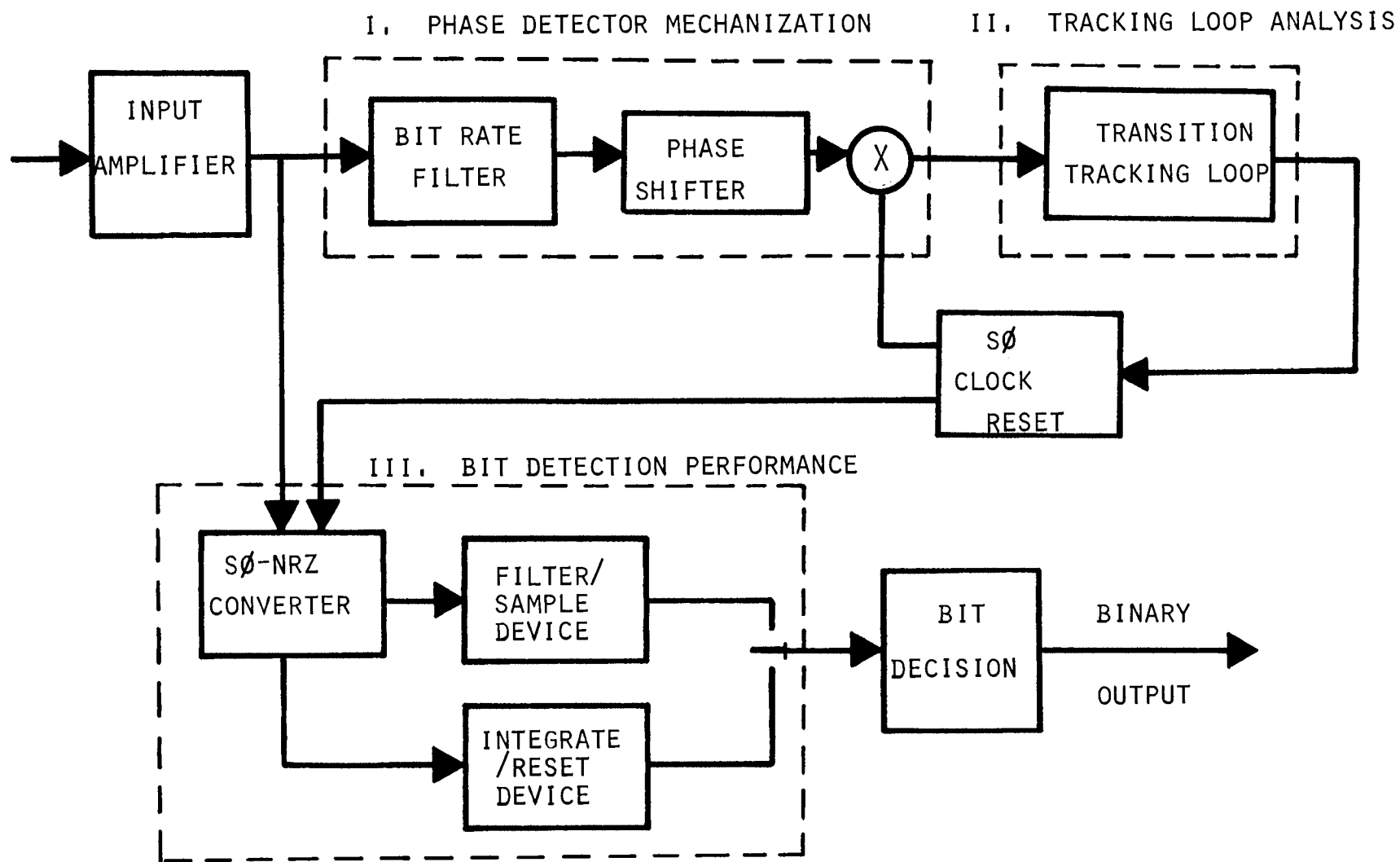


Figure 2. Stages of Digital Simulation

tracking loop is very slow with respect to a symbol interval. These assumptions permit us to construct the probability density function of the input signal jitter by using the Central Limit Theorem. Two basic techniques are then used to find the error probabilities conditioned upon signal-jitter and SNR. Overall system probability of error can then be approximated by merely integrating out the jitter. Combination of the results of the three stages of conditioner/synchronizer simulation yields a realistic estimate of the expected performance of the device.

A. Phase Detector Mechanization

The phase detector operates on the incoming signal and additive noise to construct an output waveform which indicates the occurrence or non-occurrence of a transition in the input serial data. This waveform is commonly denoted as the "error signal", which becomes the input to the transition-tracking phase-lock loop. Previous studies of the early-late gate variety of synchronizer emphasize formulation of the loop nonlinearity, $G(\lambda)$, and the equivalent noise spectral density, $S(0, \lambda)$. An adaptation of the Costas loop shown in Figure 3 forms an error signal, $e(t_n)$, by taking the product of the in-phase and mid-phase channel outputs. A filtered version of this waveform subsequently triggers a timing generator, which then provides a timing estimate to the in-phase and mid-phase

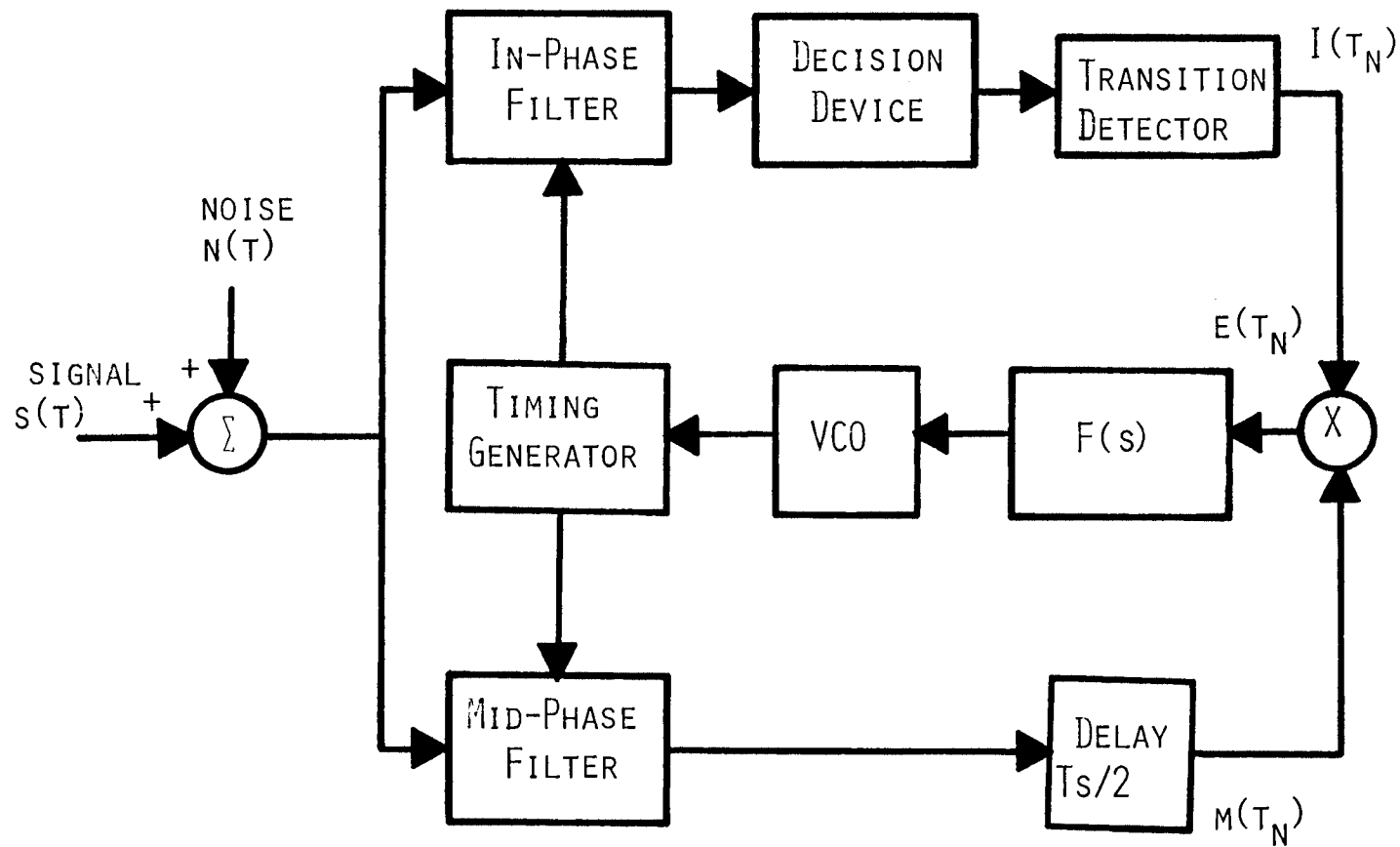


Figure 3. Early-Late Gate Bit Synchronizer

filters. By varying the length of the mid-phase integration window, the noise power in the loop can be substantially reduced¹, and a considerable improvement in the loop signal-to-noise ratio results. Hurd and Anderson² have designed an adaptive synchronizer which provides two mid-phase window widths, one wide for acquisition and a second narrower width for tracking operation.

The phase detector modeled in this thesis employs a different method of forming the error signal. Figure 4 illustrates this phase detector mechanization. The device is a cascade of a bit rate filter, a phase shifter, and a multiplier. The bit rate filter simulated is a second order Butterworth, and the bit rate (hence bit period) is chosen as 1.0 to simplify computer analysis. Monte Carlo techniques are used to generate a random data word of eleven bits, and this is converted to split-phase format for this study. The $S\phi$ -PCM signal and additive white Gaussian noise, with unity power spectral density at the input, are then processed by the linear filter. The signal output of the bit rate filter and the added filtered noise, normalized to the input signal-to-noise ratio, are then fed to the phase shifter. The phase shifter consists of comparator set at zero threshold, in-phase and 90° delay channels, and a modulo-2 summing device. The output of the phase shifter is a zero-one pulse train with the leading edge of each pulse indicating a sign transition in the input signal. Some typical waveforms for the

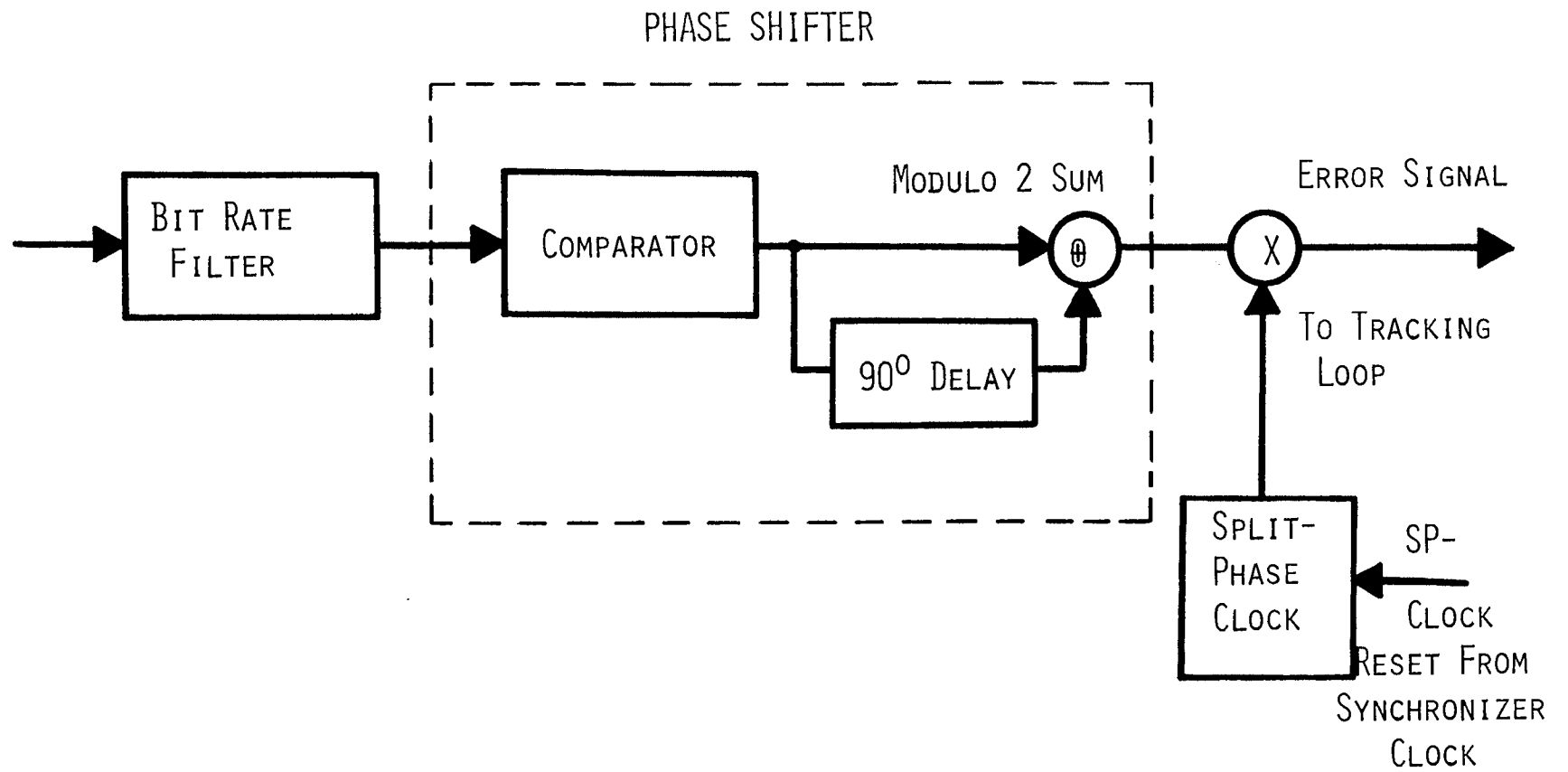


Figure 4. Phase Detector Mechanization

noiseless case are depicted in Figure 5(a-h). The phase shifter outputs for an unjittered signal and its jittered version are shown in 5(d) and 5(e), respectively. The phase shifter output is multiplied by a split-phase clock signal extracted from the synchronizer timing estimate. This product is the error signal analogous to the product of the in-phase and mid-phase channels in the early-late gate type synchronizer. The statistics of this error signal vary with the input signal-to-noise ratio and the time-base jitter in the signal. Again, the assumption is that the jitter is constant over a relatively long period with respect to the bit period holds.

The loop nonlinearity, or G curve, is found as

$$G(\lambda) \triangleq E\{e_K | \lambda, n, s\} \quad (1)$$

This is the expected value of the phase detector output signal conditioned upon the signal time-base error λ , the noise n , and the symbol sequence s . It is assumed that ones and zeros are equally likely. The average loop G-curve as a function of the normalized phase error has been evaluated analytically³ for the early-late gate synchronizer as

$$G(\lambda) = AT\lambda[1 - P_{E_t}(\lambda)] ; \quad |\lambda| \leq \frac{1}{2} \quad (2)$$

where P_{E_t} is the probability of incorrectly sensing a transition, represented by the complementary error function

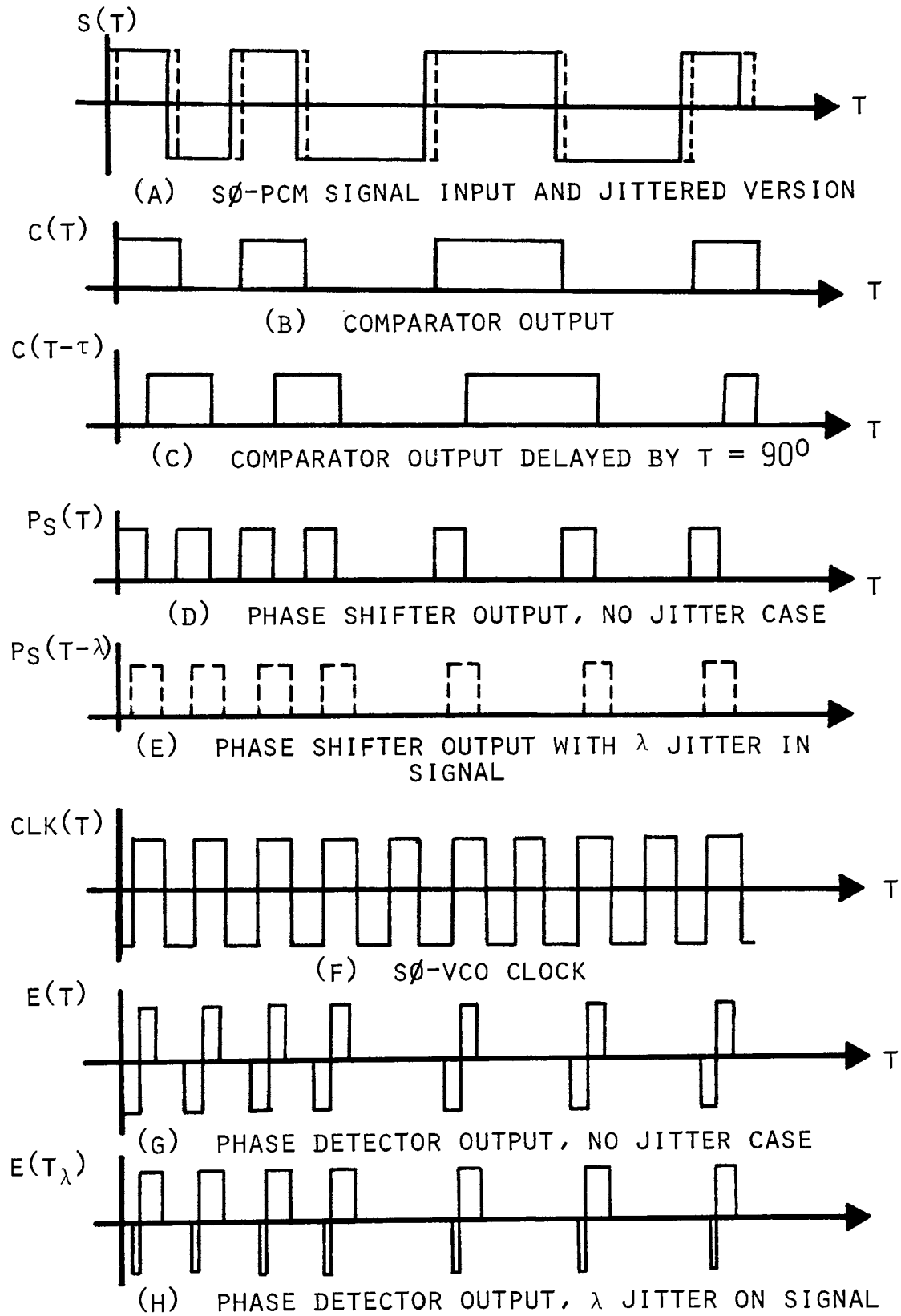


Figure 5. Typical Signal Waveforms in the Phase Detector

$$P_{E_Y}(\lambda) = \frac{1}{\sqrt{2\pi}} \int_A^{\infty} \exp[-x^2/2] dx \quad (3)$$

with $A = 2R_S(1 - 2|\lambda|)$, and $R_S = A^2T/N$, the input signal-to-noise ratio. Previous studies have investigated non-return-to-zero (NRZ) data inputs, and the resulting S-curves were found to be odd functions of λ and modulo 2π (or 1.0).

Digital simulation of the phase detector mechanism for this particular system resulted in the G-curves shown in Figure 6. The loop nonlinearities are again odd functions of λ ; however, the split-phase input waveform has resulted in the curve being modulo (π) . For large input signal-to-noise ratios, the characteristics are nearly linear for small values of signal time-base jitter. At low signal-to-noise ratios the expected value of the error signal is greatly dependent upon λ for all cases of jitter.

The problem of evaluating the equivalent noise spectrum for the additive noise, $n_\lambda(t)$, is treated as

$$S(\omega, \lambda) = [E_{n,s}(e_K e_{K+m}) - g^2(\lambda)] \quad (4)$$

The computation of $S(\omega, \lambda)$ has been accomplished by Simon¹, and since the error signal has only values of 0 and ± 1 , the spectrum consists of a constant and sinusoidal component with period $\omega_c = 2\pi/T$. If the loop bandwidth-time product is $\ll 1$, then $S(\omega, \lambda) = S(0, \lambda)$ which becomes

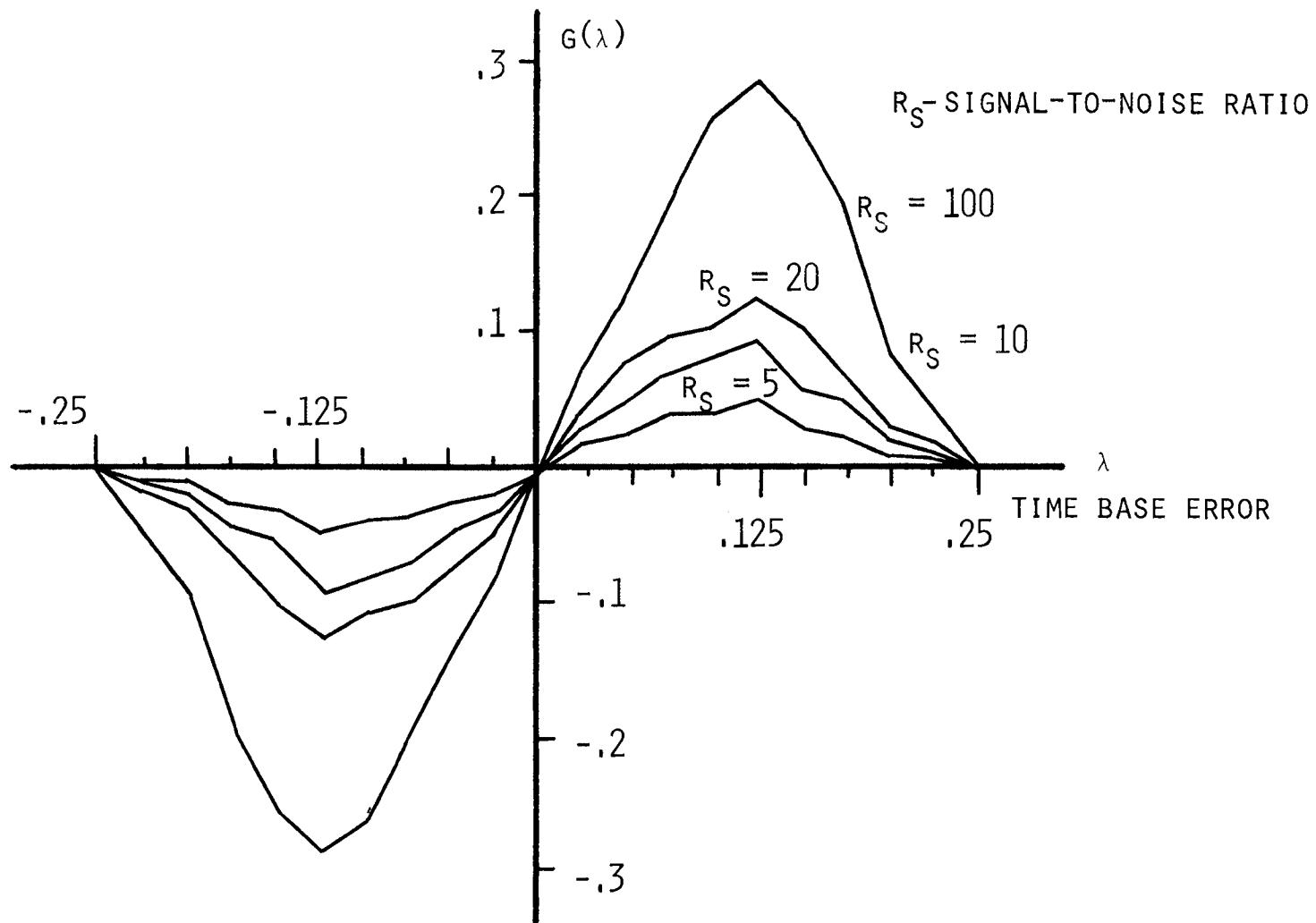


Figure 6. Loop Nonlinearity Curves

$$S(0, \lambda) = \int_{-\infty}^{\infty} [E_{n,s}(e_K e_{K+m}) - g^2(\lambda)] e^{-j\omega t} dt \Big|_{\omega=0}$$

$$S(0, \lambda) = \sigma_\lambda^2 \int_{-\infty}^{\infty} dt = \sigma_\lambda^2 \quad (5)$$

The digital simulation of the equivalent noise spectrum reveals that it is essentially constant over all λ , and is an even function of λ .

The computer algorithm used to compute the G-curves and noise equivalent spectrum, or S-curves, is shown in Appendix A.

B. Transition Tracking Loop Analysis

The synchronizer model uses a digital phase-locked loop to track the signal output of the phase detector mechanization. The relative high frequency of the error signal input compared to the slowly varying phase error within the tracking loop permits use of the Central Limit Theorem. The transition tracking loop model shown in Figure 7 incorporates the G-curve and S-curves derived in the previous section. The steady state performance of the tracking loop is of interest in this study. Application of the Fokker-Planck equation has been used to determine this performance analytically³. The actual simulation of the linear equivalent loop was easily

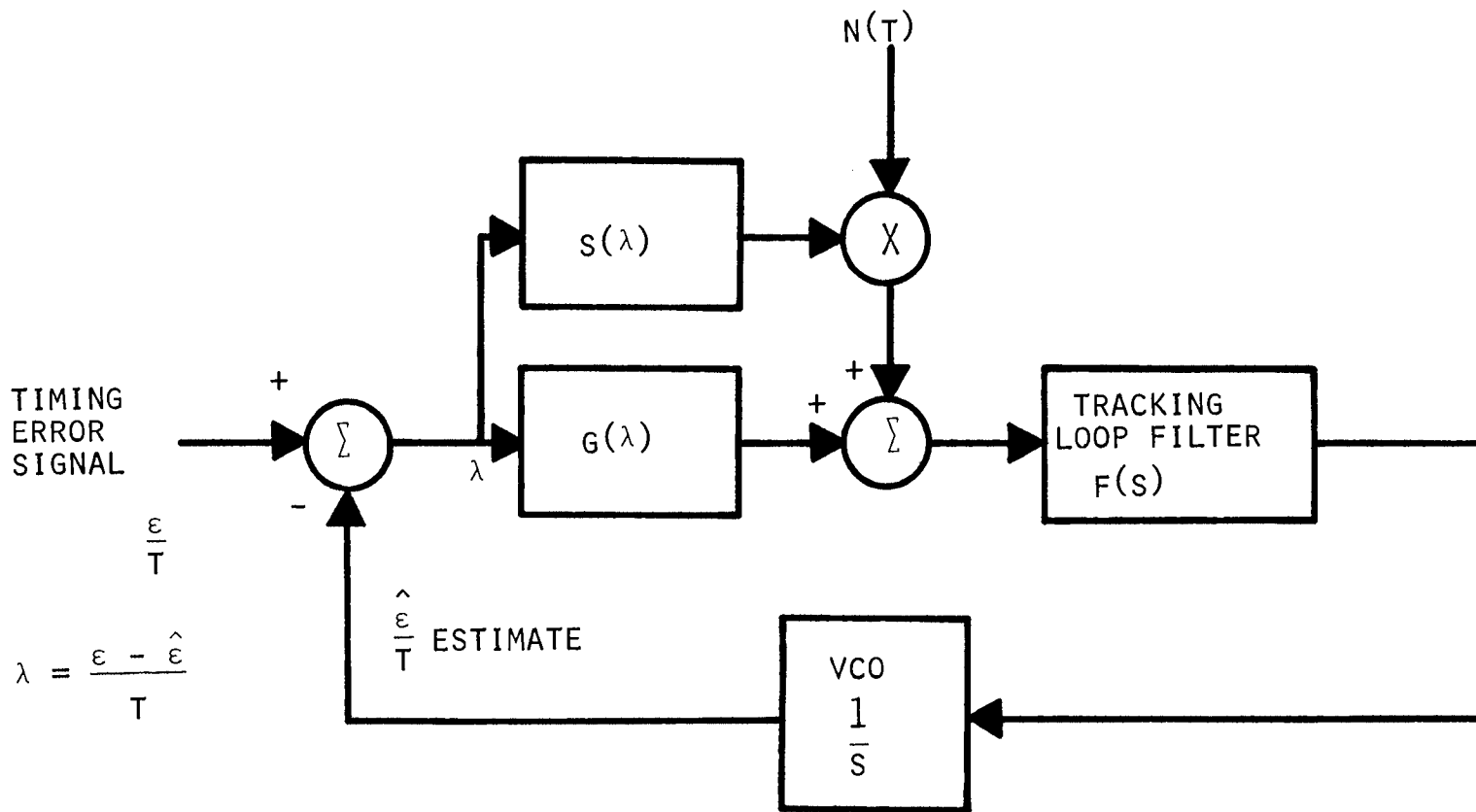


Figure 7. Linear Equivalent Tracking Loop

implemented using the Continuous System Modeling Program available on the IBM 360 digital computer. The signal time error signal input will be distributed zero mean Gaussian. This signal was tracked with the loop perturbed by additive Gaussian noise, and the steady-state phase error variance, σ_{λ}^2 , and the rms value of the phase error, λ_{rms} , evaluated for various combinations of loop bandwidth, input SNR, and the type of input time-base error signal applied. A sample computer algorithm used to determine these performance parameters is presented in Appendix B.

Three basic jitter models were analyzed. A random speed variation was generated by integrating a zero mean Gaussian random signal and using this as the error signal input to the loop. The computer simulation was initiated and the phase error signal, denoted λ , was evaluated after the loop had reached an obvious steady state. The rms value of the phase error and its variance were determined for four input SNR's between 10 and 20 dB inclusive, with the tracking loop filter cutoff frequency varied for each run. Tables 1 through 3 list the resulting phase error characteristics for specific combinations of the input parameters. It was noted that for the second type (Model B) of input jitter, that of a random speed variation plus a random delay input, there is no significant variation in either rms phase error or the phase

Jitter Model A - Random Speed Variation

Phase Error Variance

TL Bandwidth (Radians) - Input SNR	.2	.05	.005	.00125
-				
100.0	.0013	.0032	.0010	.0015
50.0	.0009	.0019	.0011	.0016
20.0	.0028	.0010	.0013	.0017
10.0	.0031	.0008	.0014	.0017

RMS Phase Error

TL Bandwidth (Radians) - Input SNR	.2	.05	.005	.00125
-				
100.0	.066	.059	.104	.150
50.0	.075	.054	.115	.153
20.0	.073	.039	.130	.157
10.0	.062	.028	.140	.160

Table 1. Tracking Loop Parameters, Random Speed Input

Jitter Model B - Random Speed Plus Random Delay

Phase Error Variance

TL Bandwidth (Radians) -	.2	.05	.005	.00125
Input SNR				
-				
100.0	2.0404	2.0406	2.0408	2.0408
50.0	2.0403	2.0405	2.0408	2.0408
20.0	2.0403	2.0405	2.0408	2.0408
10.0	2.0403	2.0405	20.408	2.0408

RMS Phase Error

TL Bandwidth (Radians) -	.2	.05	.005	.00125
Input SNR				
-				
100.0	1.43	1.429	1.428	1.428
50.0	1.431	1.429	1.428	1.428
20.0	1.432	1.429	1.428	1.428
10.0	1.432	1.429	1.428	1.428

Table 2. Tracking Loop Parameters, Random Speed Plus Delay Input

Jitter Model C - Random Speed Plus Sinusoid Input

Phase Error Variance

TL Bandwidth (Radians) - Input SNR	.2	.05	.005	.00125
-				
100.0	.0259	.0257	.0265	.0267
50.0	.0258	.0257	.0265	.0267
20.0	.0257	.0260	.0266	.0267
10.0	.0256	.0260	.0266	.0268

RMS Phase Error

TL Bandwidth (Radians) - Input SNR	.2	.05	.005	.00125
-				
100.0	.304	.345	.410	.417
50.0	.299	.350	.411	.417
20.0	.307	.363	.413	.418
10.0	.320	.373	.414	.419

Table 3. Tracking Loop Parameters, Random Speed Plus Sinusoid Input

error variance within the tracking loop at the ω_c and SNR values tested.

Values selected for the first-order Butterworth loop filter's cutoff frequency were chosen such that both relatively wide and narrow tracking ranges were considered². The values of rms phase error as a function of loop bandwidth are illustrated in Figure 8 for a random speed variation input and Figure 9 for a random speed variation and a worn part. The optimum loop bandwidth can be seen to differ for each of the contrasting types of input disturbances. Further studies of tracking loop behavior, specifically acquisition time and loss-of-lock characteristics, are beyond the scope of this investigation. Having obtained the phase error variance, we are able to investigate the bit detection performance of the conditioner/synchronizer using this time-base error statistic alone.

C. Bit Detection Performance

The relative effectiveness of a receiver or system is contingent upon its capability to detect and recover the original data with a high degree of reliability. For a given set of minimum performance standards or specifications, the system can be designed to meet these criteria by modifying the receiver structure, altering the signal pulse shape, or changing the signaling speed or data rate.

For the signal conditioner under investigation, the bit detection segment functions independently from the

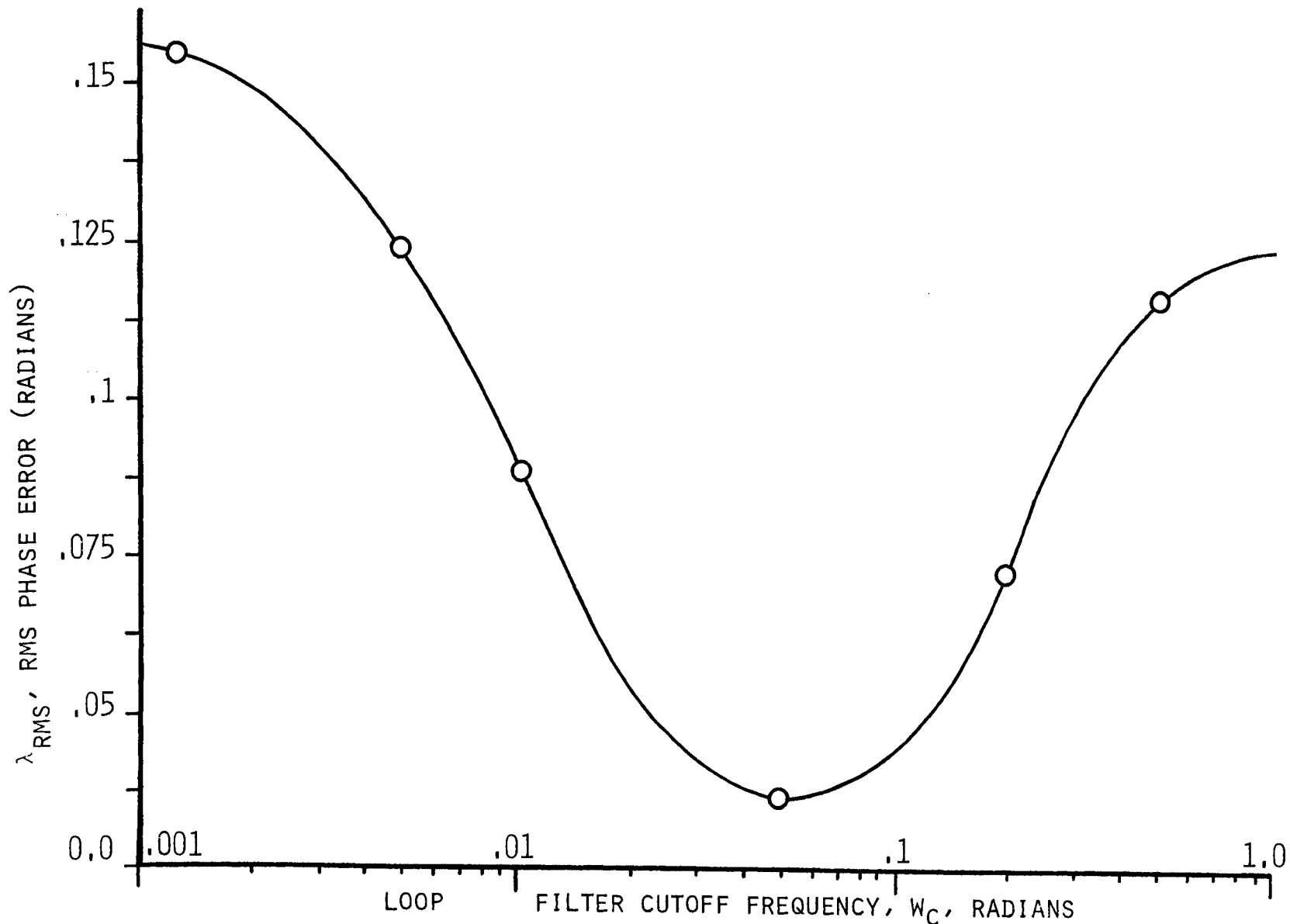


Figure 8. Rms Phase Error variations, Random Speed Input

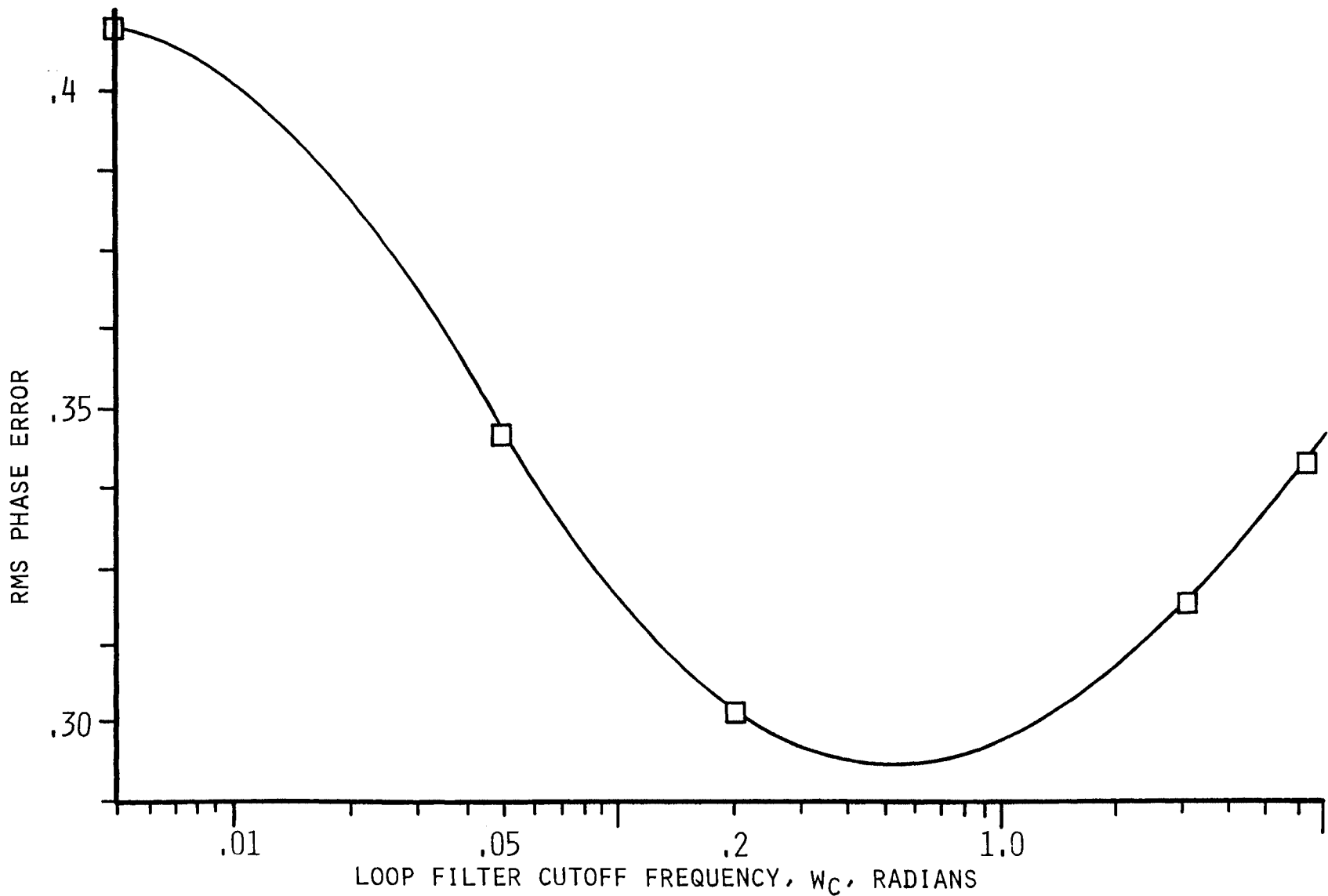


Figure 9. Rms Phase Error Variations, Random Speed and Additive Sinusoid Input

synchronizer structure. Only the timing estimate, needed for conversion and sampling, is drawn from the tracking loop split-phase clock. The bit detection configuration is shown in Figure 10. Two modes of signal processing were considered. The "Filter/Sample" and "Reset/Integrate" modes function as separate channels to obtain the parameters needed for a bit decision. Common to both methods of signal processing are input filtering and amplification, $S\phi$ -NRZ conversion, and sampling. The input data word 100010 contains each possible data bit sequence or the respective inverse, and the sequence was subsequently used as the input signal for the bit detection analysis. The split-phase version of the signal and bandlimited white Gaussian noise with unity power spectral density were filtered by a lowpass filter with cutoff frequency at 2.5 times the bit rate. This filter output is then converted from split-phase to non-return to zero format by a S-clock, which is positive for the first half cycle of a bit period. The NRZ signal and filtered noise then are processed using either the "Filter/Sample" or "Integrate/Reset" modes.

Noise statistics must be determined to evaluate the signal-to-noise ratio at the instant of sampling. The noise output of the 2.5 x bit rate filter is processed by the bit rate /2 baseband filter, and the noise power output is calculated. Assuming stationary, zero mean noise input to the system, the noise power preceding the sampler

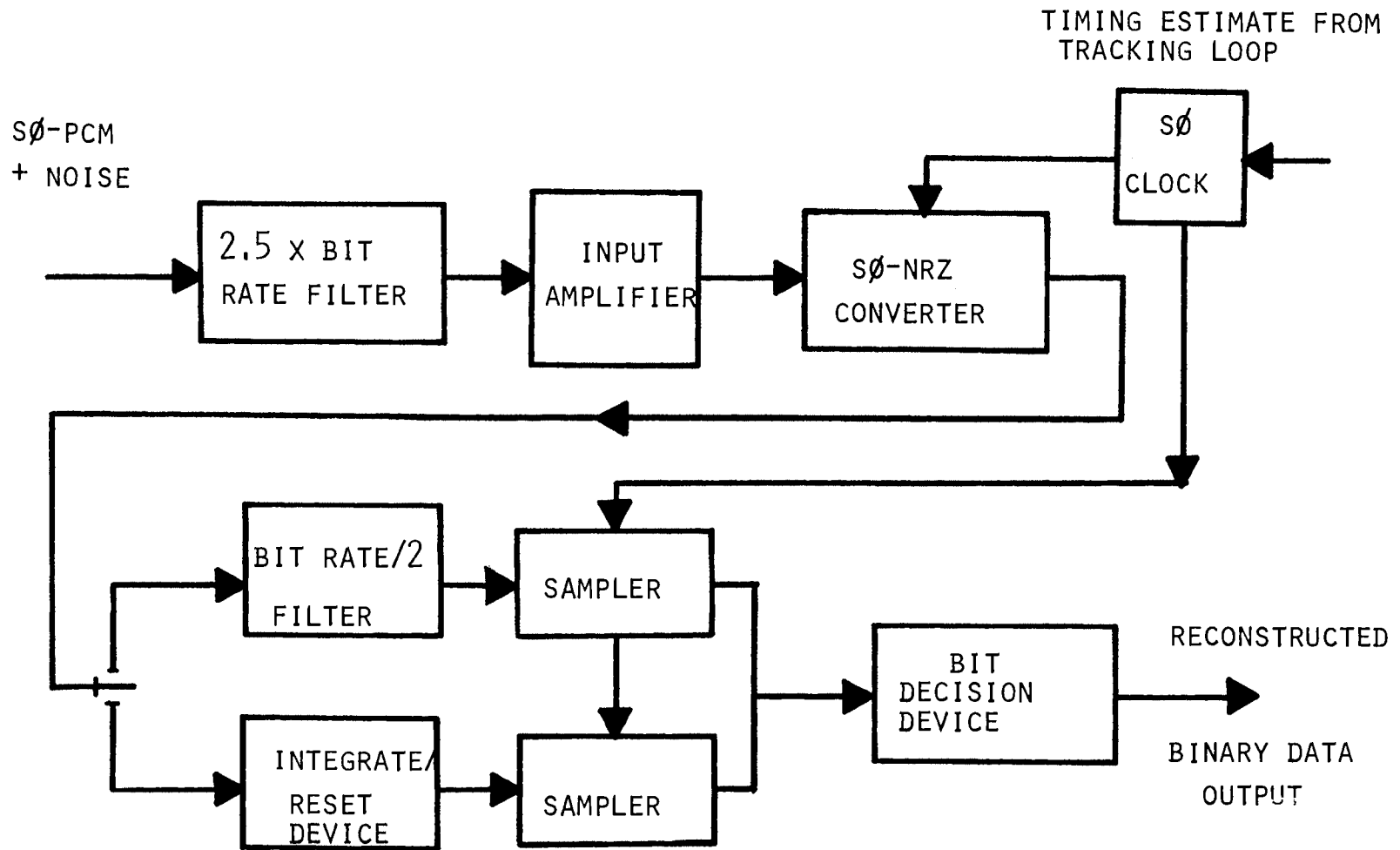


Figure 10. Bit Detection Configuration

is a constant value for both "Filter/Sample" and "Reset/Integrate" branches. Selection of the Filter/Sample mode passes the NRZ version of the filtered input symbol sequence through a second order Butterworth filter with cutoff frequency Π . The signal is sampled at the end of each center bit in the set of three symbols of the known sequence. The value of the signal at this sampling time can be compared to the noise power normalized to the input signal-to-noise ratio. This quantity becomes the argument of the error function used to determine the probability of bit error for the bit sequence and variations in values of input signal-jitter.

The noise is known to be zero mean Gaussian as a result of linear operations (filtering and conversion) upon the input white Gaussian noise. Therefore, the probability of error becomes

$$P(E) = \int_s^{\infty} [2\Pi\sigma^2]^{-\frac{1}{2}} \exp[-\frac{1}{2}(n/\sigma_n)^2] dn \quad (6)$$

by setting $u = n/\sigma_n\sqrt{2}$ and substituting we have

$$P(E) = \frac{1}{\sqrt{\Pi}} \int_{\frac{s}{\sigma_n\sqrt{2}}}^{\infty} e^{-u^2} du \quad (7)$$

using the definite integral

$$\int_0^{\infty} e^{-u^2} du = \frac{\sqrt{\pi}}{2}$$

the probability of bit error, in terms of the commonly used error function

$$P(E) = \frac{1}{2} \operatorname{erfc} \left(\frac{S}{\sigma_N \sqrt{2}} \right) \quad (8)$$

where

s = the value of the sampled signal

σ_N = the normalized noise variance at the input
to the sampling device

A digital computer program was implemented to determine the probability of bit error for several low input signal-to-noise ratios and signal-jitter conditions on the input. The results of this simulation are graphically displayed in Figures 11(a) and 11(b).

The Integrate/Reset channel integrates the converter output over the bit interval, samples the output at the end of each middle bit in the specific bit sequence tested, then resets for the next operation. The computed probabilities of error are averaged over the possible input bit sequences to establish the characteristics for varying SNR's and constant signal time base jitter. These averaged results, indicated graphically in Figures 12(a) and (b), display the bit detection characteristics for

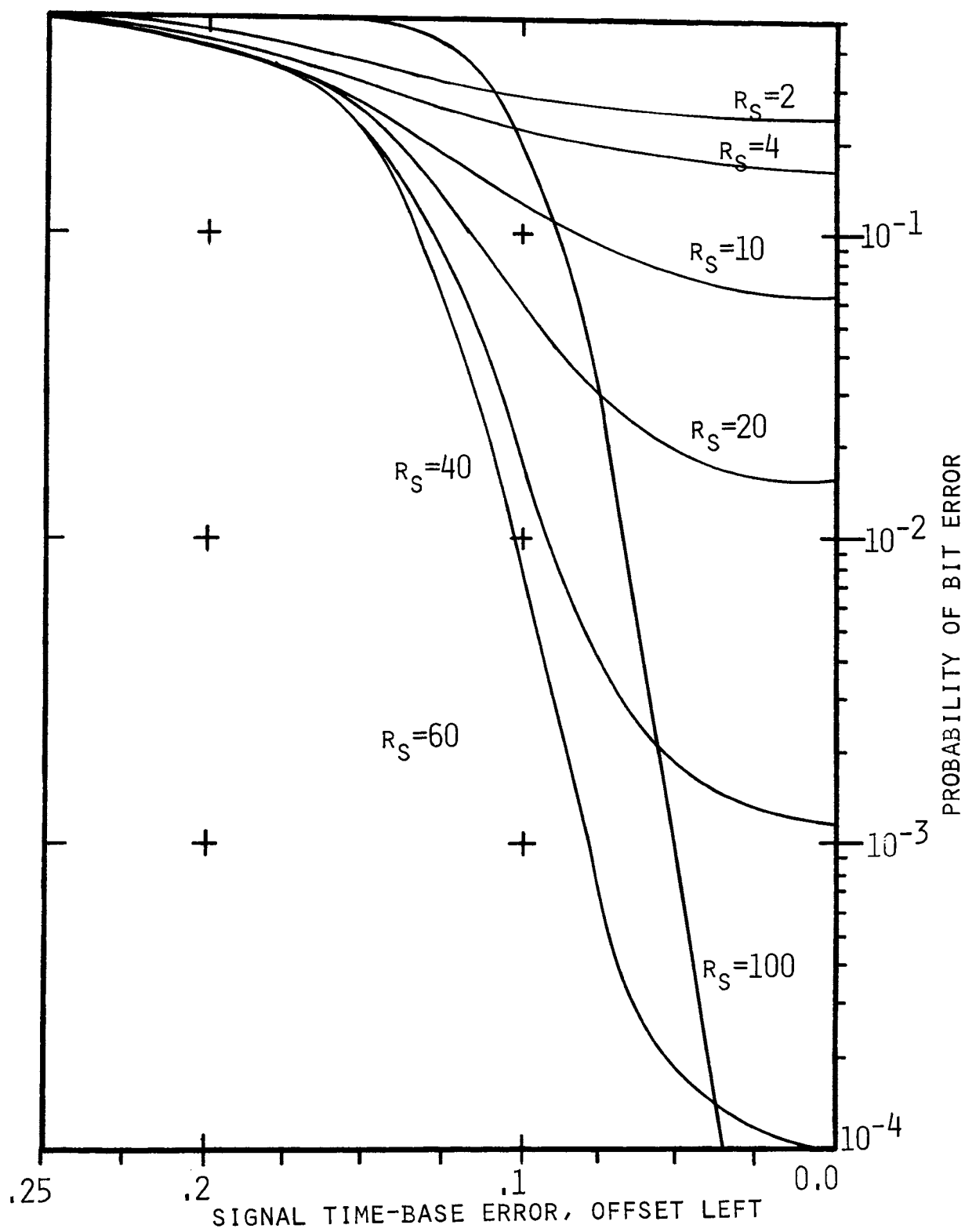


Figure 11(a). Error Probability Characteristics Using Filter/Sample Detection

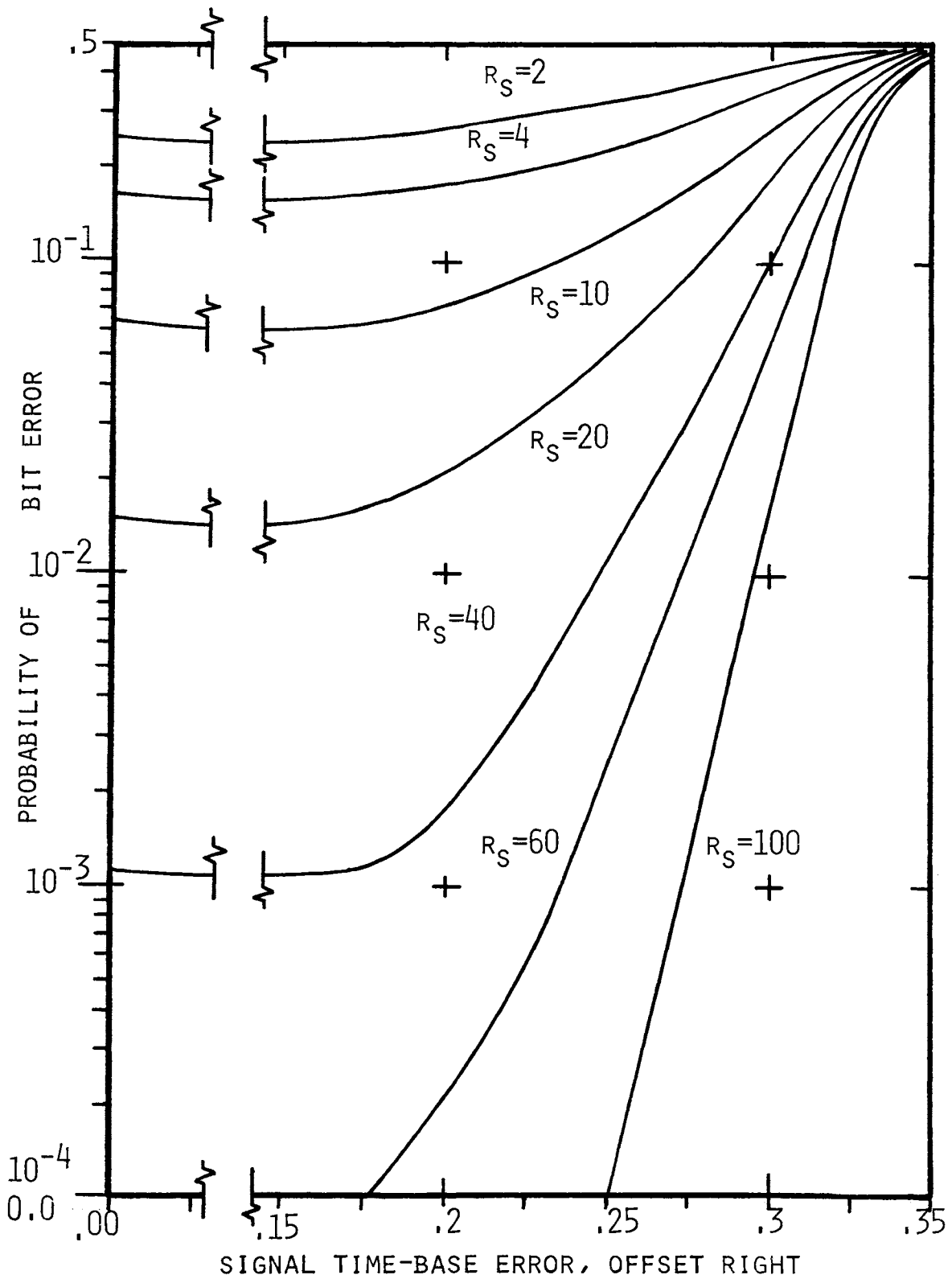


Figure 11(b). Error Probability Characteristics Using Filter/Sample Detection

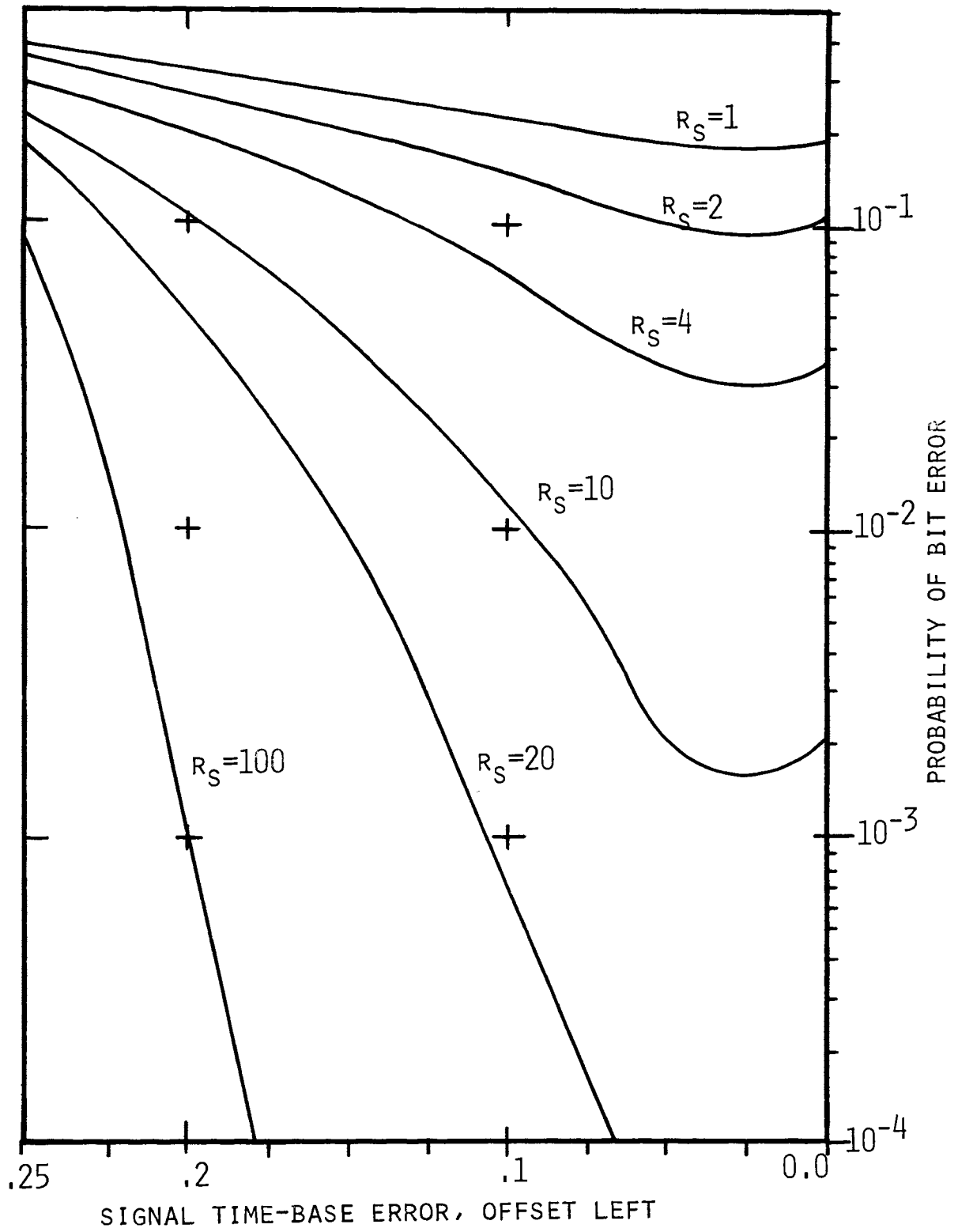


Figure 12(a). Error Probability Characteristics Using Integrate/Reset Detection

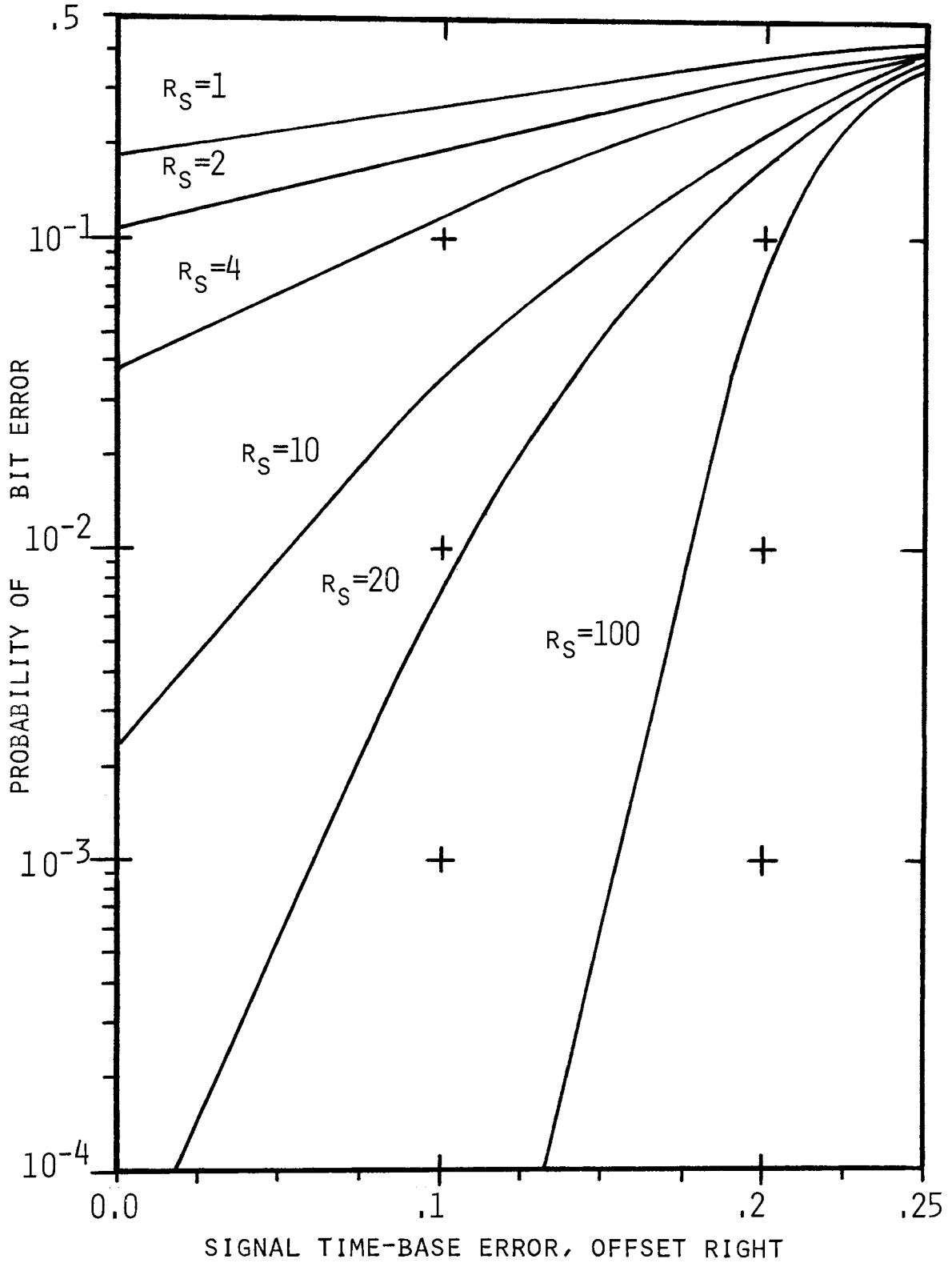


Figure 12(b). Error Probability Characteristics Using Integrate/Reset Detection

the signal conditioner in the integrator/reset mode. The digital computer algorithms used for simulation of the integrate/reset and filter/sample modes are contained in Appendices C and D, respectively.

V. SIMULATION RESULTS AND CONCLUSIONS

Overall signal conditioner performance has been approximated by combining results from the three computer algorithms. Nonlinearities derived in the phase detector analysis have been employed in the tracking loop portion to project the phase error statistics. In bit detection simulation, the filter-sample and integrate-reset methods yield dissimilar results for low input signal-to-noise ratio and signal time-base jitter condition combinations.

Operating in the filter-sample mode, conditioner performance deteriorated rapidly for input SNR's below 20 dB. The probability of bit error characteristics as a function of fixed signal jitter was not symmetric about the zero jitter condition. Error probability remained essentially constant for the case of jitter to the right up to 20 percent. This corresponds to a delay in data waveform input. Conversely, for very small values of signal jitter to the left, these same characteristics rose sharply indicating inferior performance for time-base error of this type. Figure 13 represents the total system performance in the filter-sample detection mode for typical values of phase error variance representing the different jitter models tracked. Error probabilities were determined by recognizing that the jitter was distributed normally with zero mean and variance equal to the

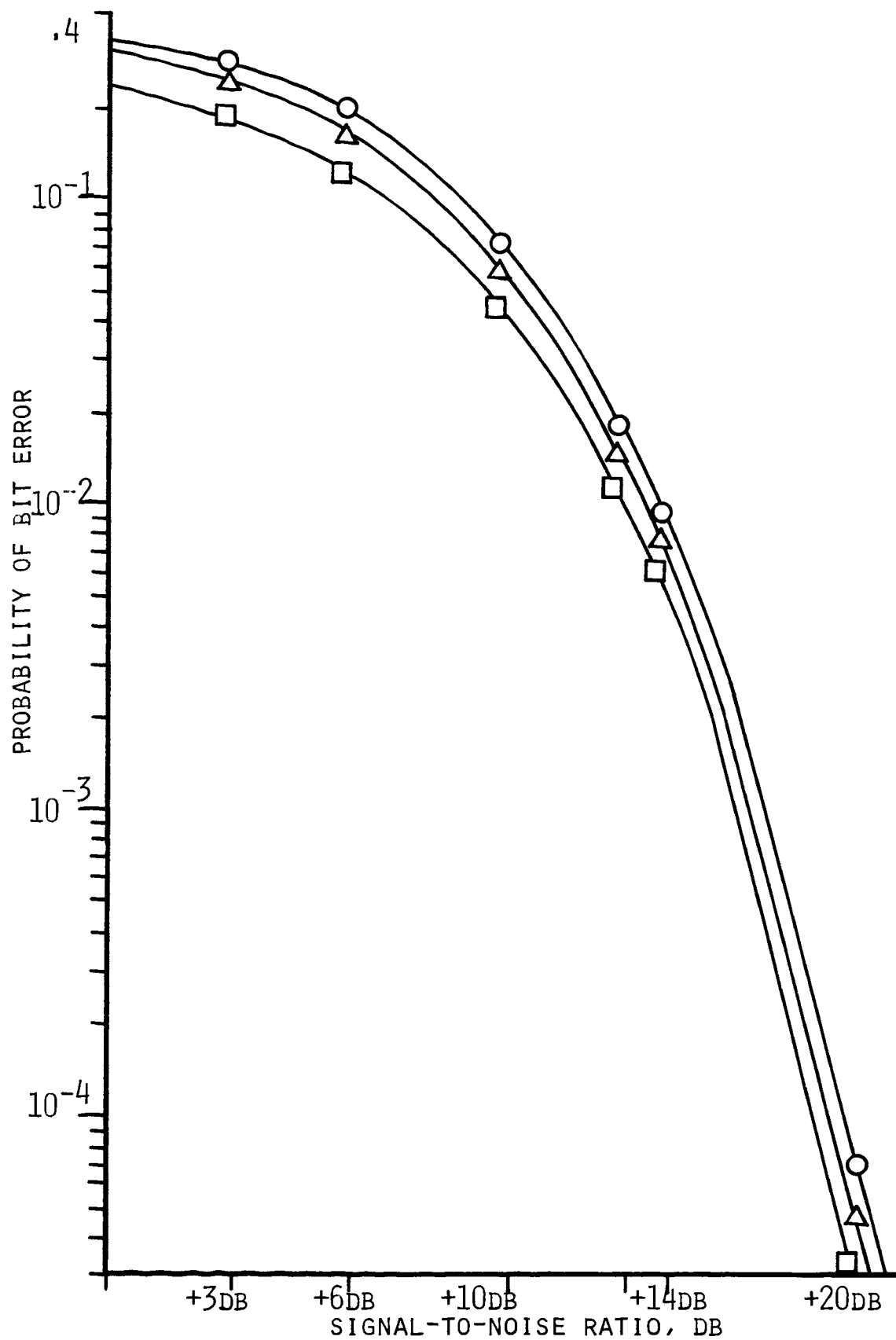


Figure 13. System Performance, Filter/Sample Mode

phase error variance found in the tracking loop study, the integrating the product of the error probability conditioned upon jitter and the probability density function of the jitter over the range of signal time-base error values. Differences in phase error values tested during this simulation did not appreciably alter overall system performance.

By comparison, the integrate-reset method of detection provided symmetrical error probability characteristics. These displayed a slight offset left of the zero jitter case, and provided a more gradual degradation in performance which had been originally anticipated. Overall system operation appears to be about 4 dB better when using the integrate-reset mode for bit detection. Composite system performance criteria for this method is illustrated in Figure 14.

The signal conditioner/bit synchronizer model simulated represented a practical device for implementation on split-phase pulse code modulated telemetry systems. At the low signal-to-noise ratios investigated, the performance of the conditioner deteriorates rapidly to unacceptable values. Initiation of coding schemes or emphasis filtering processes are alternatives available to improve performance characteristics for satisfactory operation at these low signal levels.

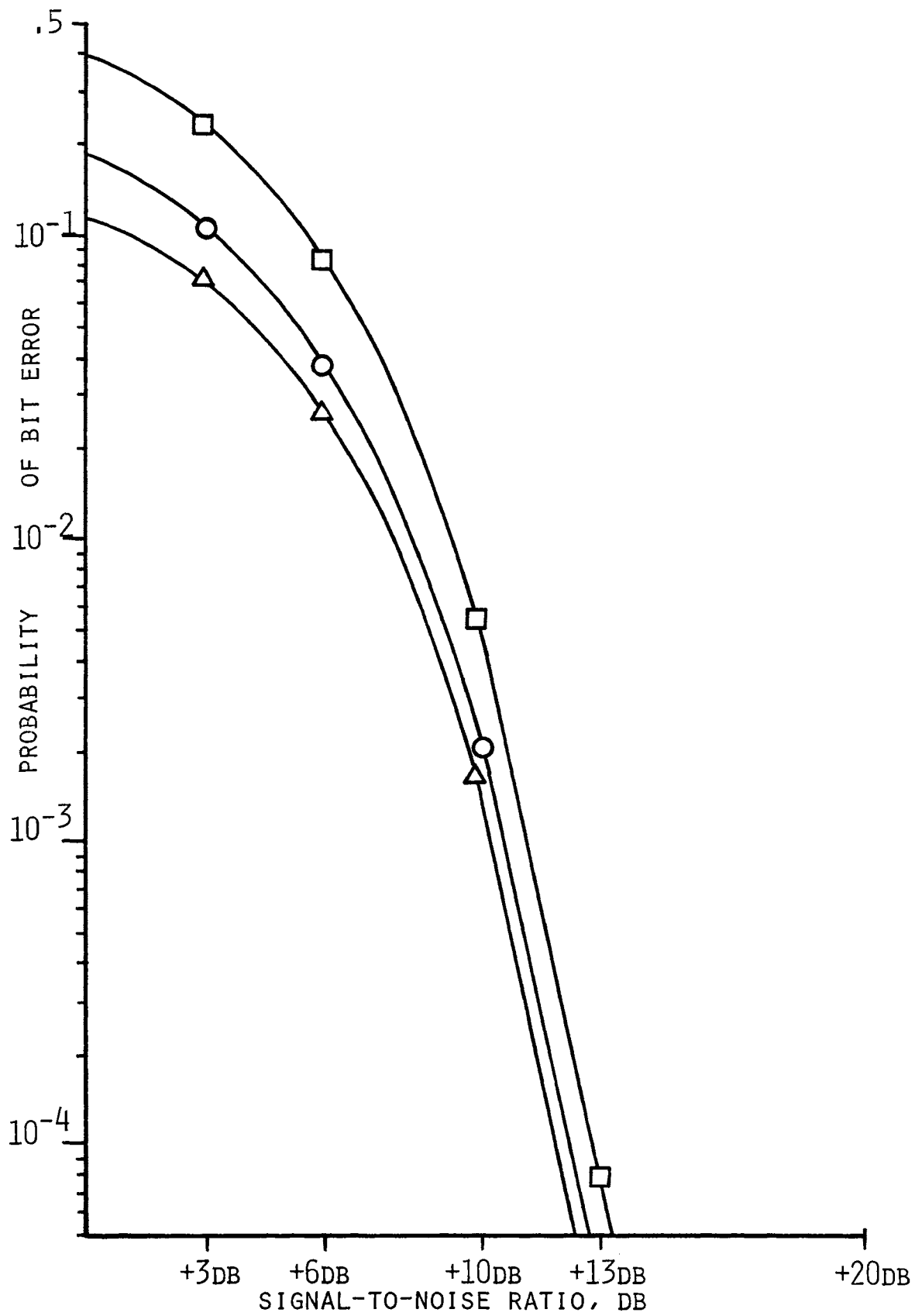


Figure 14. System Performance, Integrate/Reset Mode

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VITA

Quentin Reed Webb was born in Saint Louis, Missouri, on October 17, 1940. He received his primary and secondary education in Kirkwood, Missouri. He attended The Citadel, in Charleston, South Carolina, where he received his Bachelor of Science degree in Electrical Engineering in June, 1962.

Mr. Webb is currently serving in the United States Army. As a Major assigned to the Signal Corps, his duty positions have included assignment as a communications officer with the 101st Airborne Division and the 25th Infantry Division in the Republic of Vietnam. A graduate of the Army Signal and Infantry schools, he has served with the Air Defense Artillery element in the Republic of Korea, and with the United States Strike Command Headquarters at MacDill Air Force Base, Florida. While assigned to Strike Command, he participated in the communications element of the Project Gemini Spacecraft Recovery Forces in the eastern Atlantic.

He is married to the former Susan Cina of Glendale, Missouri, and they have three sons. He has been enrolled in the Graduate School of the University of Missouri - Rolla since January 1969.

APPENDIX A

DIGITAL COMPUTER ALGORITHM FOR ANALYSIS
OF BIT RATE EFFECTS

```

/WAT4 EE142136,TIME=03,PAGES=050 WEBB QUENTIN R 70.329 JOB 383
/
LIMITS=(T=3,P=50,C=1)
CLASS=W,PRIORITY=04,REGION=0132K,READER=R FADER1
/
*****
* THIS RUN IS MADE TO DETERMINE THE G CURVE AND S CURVE NON-
* LINEARITIES FOR THE TRACKING LOOP ANALYSIS.
*****
1 REAL SIGJ(500),GCURV(100),JITTER(100),SCURV(100)
2 REAL SIGI(441),NOISEI(841),SIGF(441),NOISEF(841),CASE(3)
3 INTEGER BIT(101),Y(501)
4 INTEGER SIGC(500),SIGPS(500),VCO(500),PDCOUT(500)
5 REAL X(3),Z(3)
6 T=.1
7 WC=6.28
8 IX=213711
/
GENERATE A RANDOM BIT STREAM TO BE USED AS THE PCM DATA INPUT
TO THE SIGNAL CONDITIONER/BIT SYNCHRONIZER.
/
9 DO 1 I=1,500
10 CALL RAND(IX,IY,YFL)
11 IF(YFL-.5) 2,2,3
12 2 Y(I)=0
13 GO TO 1
14 3 Y(I)=1
15 1 CONTINUE
16 DO 8 K=1,11
17 8 BIT(K)=Y(K+150)
18 WRITE(3,100) (BIT(I),I=1,11)
19 100 FORMAT(5X,'INPUT DATA WORD = ',11I1)
/
AN ELEVEN BIT DATA WORD IS READ INTO THE SIGNAL CONDITIONER.
/
20 N1=441
21 N2=841
22 DO 4 J=1,11
23 INT1=J*40-39
24 INT2=INT1+19
25 AMPL=BIT(J)*2-1
26 DO 4 K=INT1,INT2
27 SIGI(K)=AMPL
28 4 SIGI(K+20)=-AMPL
29 SIGI(441)=0.0
30 A=SQRT(40.0)
31 DO 5 L=1,841
32 5 NOISEF(L)=GAUSS(A)
33 WRITE(3,444) (SIGI(K),K=1,441)
34 444 FORMAT(//5X,'INPUT SIGNAL VALUES',//,(10X(10F10.7)))
/
THE INPUT SIGNAL-TO-NOISE POWER RATIO IS VARIED. SEVEN TRIAL SNR
VALUES ARE USED TO DETERMINE TO G-CURVE AND S-CURVE NONLINEARITIES.
/
35 DO 960 ISNR=1,7
36 READ 203, SNR
37 203 FORMAT(F12.7)
38 WRITE (3,205) SNR

```

```

39      205 FORMAT(/5X,'SNR = ',F12.7)
      C
      C THE INPUT SIGNAL SIGI AND THE INPUT NOISE NOISEI ARE ADDITIVE
      C VECTORS AND ARE PROCESSED BY A DIGITAL FILTER. IN THIS CASE THE
      C FILTER IS A SECOND ORDER BUTTERWORTH WITH BIT RATE BANDWIDTH =3140
      C RADIANS.
40      CALL FILTI(X,Z,WC,T)
      C
      C THE FOLLOWING SIMULATES THE INTRODUCTION OF TIME BASE JITTER INTO
      C THE SYSTEM TO DETERMINE THE G-CURVE AND S-CURVE NONLINEARITIES TO
      C BE USED IN THE TRACKING LOOP ANALYSIS.
41      DO 760 KSHIFT=1,10
42      JITTER(KSHIFT)=KSHIFT/40.0
43      DO 761 J=1,KSHIFT
44      761 SIGJ(J)=SIGI(J)
45      KM=KSHIFT + 1
46      DO 762 L=KM,441
47      762 SIGJ(L)=SIGI(L-KSHIFT)
48      DO 6 M=1,441
49      CALL FILT(X,Z,SIGJ(M),FS)
50      6 SIGF(M)=FS
      C
51      DO 7 N=1,841
52      CALL FILT(X,Z,NOISEI(N),FN)
53      7 NOISFF(N)=FN
      C
      C THE FOLLOWING PROGRAM PLACES THE FILTERED PCM DATA INTO THE
      C PHASE SHIFTER PORTION OF THE SIGNAL CONDITIONER.
54      R=1./SQRT(SNR)
      C
      C THE SIGNAL PLUS NOISE OUTPUT OF THE FILTER IS CLIPPED BY THE
      C PHASE SHIFTER, DESIGNATED HERE AS SIGC.
55      DO 99 I=1,441
56      A=SIGF(I)+R*NOISFF(I)
57      99 SIGC(I)=SIGN(.5,A)+.51
58      DO 446 K=442,455
59      446 SIGC(K)=SIGC(441)
      C
      C THE CLIPPED SIGNAL PLUS NOISE IS MOD2 SUMMED WITH ITS 90 DEGREE
      C DELAYED VERSION TO YIELD THE OUTPUT OF THE PHASE SHIFTER, CALLED
      C SIGPS.
60      DO 98 K=1,441
61      K10=K+10
62      JK=SIGC(K)+SIGC(K10)
63      98 SIGPS(K)=MOD(JK,2)
      C
      C THE FOLLOWING REPRESENTS THE VCO CLOCK OF THE TRACKING LOOP WITHIN
      C THE BIT SYNCHRONIZER.
64      K=5
65      DO 330 I=1,5
66      330 VCO(I)=+1
67      DO 331 J=5,89,4
68      JJ=(J-2)*K+1
69      JJJ=J*K

```



```

70      DO 331 L=JJ, JJJ
71      331 VCO(L)=+1
72          DO 332 M=1, 99, 4
73          MM=M*K+1
74          MMM=(M+2)*K
75          DO 332 N=MM, MMM
76          332 VCO(N)=-1
C.C.C.C.C
      THE FOLLOWING REPRESENTS THE PRODUCT OF THE OUTPUTS OF THE PHASE
      SHIFTER AND THE VCO CLOCK WITHIN THE TRACKING LOOP. THIS IS THE
      PHASE DETECTOR OUTPUT.
77      DO 340 I=1, 440
78      340 PDDOUT(I)=SIGPS(I)*VCO(I)
C.C.C.C.C
      THE FOLLOWING COMPUTES THE MEAN AND THE VARIANCE OF THE PHASE
      DETECTOR OUTPUT SIGNAL. THE G-CURVE AND S-CURVE DATA ARE FOUND.
79      PDSUM=0.0
80      SQSUM=0.0
81      DO 763 MSUM=1, 440
82      PDSUM=PDSUM+PDDOUT(MSUM)
83      SOSUM=SQSUM+PDDOUT(MSUM)*PDDOUT(MSUM)
84      763 CONTINUE
85      SMEAN=PDSUM/440.0
86      SMSQ=SQSUM/440.0
87      GCURV(KSHIFT)=SMEAN
88      SCURV(KSHIFT)=(SMSQ-(SMEAN*SMEAN))/(11.0)
89      762 WRITE(3,764) KSHIFT, JITTER(KSHIFT), GCURV(KSHIFT), SCURV(KSHIFT)
90      764 FORMAT(//5X, 'K = ', I2, 5X, 'JITTER = ', F10.7, 5X, 'G CURVE VALUE = ',
      1 F10.7, 5X, 'S CURVE VALUE = ', F10.7, /)
91      960 CONTINUE
92      STOP
93      END
94      SUBROUTINE FILTI(X, Z, WC, T)
95      REAL X(3), Z(3)
96      DO 50 I=1, 3
97      50 X(I)=0.0
98          FACT=2.0/(WC*T)
99          Z(1)=1.+(FACT*SQRT(2.0))+(FACT*FACT)
100         Z(2)=2.0-(2.0*FACT*FACT)
101         Z(3)=1.0-(FACT*SQRT(2.0))+(FACT*FACT)
102         RETURN
103         END
104      SUBROUTINE FILT(X, Z, U, Y)
105      REAL X(3), Z(3)
106      X(1)=(U-Z(2)*X(2)-Z(3)*X(3))/Z(1)
107      Y=X(1)+2.*X(2)+X(3)
108      X(3)=X(2)
109      X(2)=X(1)
110      RETURN
111      END
112      FUNCTION GAUSS(S)
113      INTEGER IX/213711/
114      A=-6.
115      DO 1 I=1, 12
116      A=A+RANDU(IX, IY)

```

```
117      1 IX=IY
118      GAUSS=A*S
119      RETURN
120      END

121      FUNCTION RANDU(IX,IY)
122      IY=IX*65539
123      IF(IY) 5,5,6
124      5 IY=IY+2147483647+1
125      6 X=IY
126      RANDU=X*.4656613E-9
127      RETURN
128      END

129      SUBROUTINE RAND(IX,IY,YFL)
130      IY = IX * 65539
131      IF (IY) 1,2,2
132      1 IY = IY + 2147483647+1
133      2 YFL = IY
134      YFL = YFL *.4656613E-9
135      IX = IY
136      RETURN
137      END
```

APPENDIX B

DIGITAL COMPUTER ALGORITHM FOR DATA-
TRANSITION TRACKING LOOP ANALYSIS

```

/** LIMITS=(R=130,T=5,P=50)
//S1 EXEC CSMP
//G.DATA DD *
*
* TITLE RANDOM SPEED VARIATION MODEL A
*
* INITIAL
R=SQRT(40.0)
*
* DYNAMIC
METHOD RKSPX
*
* PARAMETER WC=(.2,.05,.005,.00125)
N1=GAUSS(173,0.0,1.0)
TIMERR=INTGRL(0.0,N1)
*
* THE FOLLOWING ARE THE G AND S CURVES FOR A SIGNAL TO NOISE RATIO
* OF 100.0 AT THE INPUT TO THE SIGNAL CONDITIONER/BIT SYNCHRONIZER.
*
* FUNCTION GCURVE=.0,.0,.025,.065,.05,.127,.075,.177,.1,.223,.125,.273,...
.15,.218,.175,.163,.2,.077,.225,.036,.25,.00
*
* FUNCTION SCURVE=.00,.032,.025,.032,.05,.031,.075,.029,.1,.027,...
.125,.025,.15,.027,.175,.029,.2,.031,.225,.030,.25,.030
*
* THE PHASE ERROR EQUALS THE TIMING ERROR MINUS THE FEEDBACK SIGNAL
PHASER=TIMERR-F
*
* E1=ABS(PHASER)
E2=AMOD(E1+.25,.5)-.25
E3=E2*SIGN(1.0,PHASER)
*
* G3=ABS(E3)
G2=AFGEN(GCURVE,G3)
G=SIGN(G2,E3)
*
* S=AFGEN(SCURVE,G3)
*
* RN=GAUSS(173,0.0,B)
*
* THE SIGNAL*NON-LINEARITY PLUS THE NOISE*NOISE SPECTRA NON-LINEAR-
* -ITY ARE INPUTS (CALLED FILTIN) TO THE LOOP FIRST ORDER BW FILTER
*
* FILTIN=G+S*RN
*
* THE FOLLOWING REPRESENTS THE FIRST ORDER BUTTERWORTH FILTER WITH
* CUTOFF FREQUENCY WC, WHICH IS SPECIFIED AS PARAMETER AND WILL
* VARY WITH EACH RUN.
*
* YIDDT=WC*(FILTIN - Y)
Y=INTGRL(0.0,YIDDT)
*
* THE FOLLOWING REPRESENTS THE VCO INTEGRATION IN THE FEEDBACK LOOP
F=INTGRL(0.0,Y)
*
* THE FOLLOWING CALCULATES THE MEAN AND THE MEAN-SQUARE OF THE
* PHASE ERROR WITHIN THE TRACKING LOOP.
*
* PP=STEP(10.0)*PHASER

```

```

PMEAN=INTGRL(0.0,PP)
PMSQ=INTGRL(0.0,PP*PP)
*
TIMER DELT=.01,FINTIM=15.0,PRDEL=.1,OUTDEL=.1
*
TERMINAL
*
*   THE FOLLOWING COMPUTES THE PHASE ERROR VARIANCE IN THE TRACKING LOOP.
*
PVAR=(PMSQ-(PMEAN*PMEAN))/(TIME-10.0)/(TIME-10.0)
WRITE(3,100) PVAR
100 FORMAT(10X,'PHASE ERROR VARIANCE = ',F10.7,/)
*
*   THE FOLLOWING COMPUTES THE RMS PHASE ERROR IN THE TRACKING LOOP
AMSQ=PMSQ/(TIME-10.0)
RMSERR=SQRT(AMSQ)
WRITE(3,200) RMSERR
200 FORMAT(10X,'RMS PHASE ERROR IN TRACKING LOOP = ',F10.7,/)
*
END
STOP
ENDJOB

```

APPENDIX C

DIGITAL COMPUTER ALGORITHM FOR BIT DETECTION
USING INTEGRATE/RESET METHOD

```

/WAT4 EF142136, TIME=03, PAGES=050 WEBB QUENTIN R 70.329 JOB 141
/
LIMITS=(T=3,P=50,C=1)
CLASS=W,PRIORITY=04,REGION=0132K,READER=READER1
/
C
C *****
C * BIT PROBABILITY OF ERROR ANALYSIS USING INTEGRATE/RESET METHODS. *
C * *****
C
1 INTEGER BIT(10)
2 REAL SNR(6),SIGNJ(240),SNRZ(240),SNJ(4),PENJ(4)
3 REAL X(3),Z(3),NOISEI(601),NOISEF(601),NOIND(561),CLK(240),
4 SIGJR(240),SIGJL(240),SIGI(240),SIGF(240),SJRNRZ(240),SJLNRZ(240),
5 SJR(20,4),SJL(20,4),PEJR(20,4),PEJL(20,4),PEFJR(20),PEFJL(20)
6 READ 101, (BIT(I),I=1,6)
7 101 FORMAT(6X,6I1)
8 PSNR=100.0
9 WRITE(3,29) PSNR
10 29 FORMAT(5X,'SIGNAL-TO-NOISE RATIO = ',F5.1,/)
C
C THE PHASE ERROR(JITTER) VARIANCE IS FOUND IN THE TRACKING LOOP
C ANALYSIS FOR A SPECIFIC TYPE OF INPUT TIME BASE JITTER.
C
11 BVAR=.1
12 SIGMA=SQRT(BVAR)
13
C
C THE FOLLOWING CALCULATES THE NOISE VARIANCE(POWER) AT THE OUTPUT
C OF THE RESET INTEGRATOR.
C
14 DO 30 I=1,601
15 NOISEI(I)=GAUSS(B)
16 CALL FILTI(X,Z,WC,T)
17 DO 31 K=1,601
18 CALL FILT(X,Z,NOISEI(K),FN)
19 31 NOISEF(K)=FN
20 A=0.0
21 DO 32 L=1,20
22 A=A+NOISEF(L)-NOISEF(L+20)
23 NOIND(1)=A/40.0
24 DO 33 M=2,561
25 33 NOIND(M)=NOIND(M-1)+(NOISEF(M+40)-2.*NOISEF(M+20)+NOISEF(M))/40.0
26 B=0.0
27 DO 34 N=1,561
28 34 B=B+NOIND(N)*NOIND(N)
29 VARIND=B/561.0
30 VARR=VARIND/PSNR
C
31 DO 4 J=1,6
32 INT1=J*40-39
33 INT2=INT1+19
34 AMPL=BIT(J)*2-1
35 DO 4 K=INT1,INT2
36 SIGI(K)=AMPL
37 4 SIGI(K+20)=-AMPL

```

```

C
38      DO 35 I=1,240
39      CALL FILT(X,Z,SIGI(I),FS)
40      35 SIGF(I)=FS
C
C      THE FOLLOWING IS THE REFERENCE CLOCK IN THE SYNCHRONIZER.
C
41      DO 36 J=1,201,40
42      JJ=J+19
43      DO 36 K=J,JJ
44      CLK(K)=+1.
45      36 CLK(K+20)=-1.
C
46      DO 37 J=1,20
47      DO 38 L=21,220
48      SIGJR(L)=SIGF(L-J)
49      SIGJL(L)=SIGF(L+J)
50      SIGNJ(L)=SIGF(L)
C
C      THE FOLLOWING CONVERTS THE SIGNAL + JITTER INTO NRZ.
C
51      SNRZ(L)=CLK(L)*SIGNJ(L)
52      SJRNRZ(L)=CLK(L)*SIGJR(L)
53      38 SJLNRZ(L)=CLK(L)*SIGJL(L)
C
C      THE FOLLOWING PERFORMS THE INTEGRATE/DUMP OPERATION ON THE JITTER-
C      ED SIGNAL.
C
54      IK=1
55      DO 40 N=41,161,40
56      NN=N+39
57      SUM=0.0
58      SUMR=0.0
59      SUML=0.0
60      DO 39 M=N,NN
61      SUM=SUM+SNRZ(M)
62      SUMR=SUMR+SJRNRZ(M)
63      39 SUML=SUML+SJLNRZ(M)
64      SUMNJ=SUM/40.0
65      SUM1=SUMR/40.0
66      SUM2=SUML/40.0
67      SNJ(IK)=SUMNJ
68      SJR(J,IK)=SUM1
69      SJL(J,IK)=SUM2
70      40 IK=IK+1
71      37 CONTINUE
C
C      THE FOLLOWING CALCULATES THE PROBABILITY OF ERROR FOR VARYING
C      VALUES OF INPUT SIGNAL JITTER AND THE FOUR POSSIBLE BIT SEQUENCES.
C
72      SNJ(4)=-SNJ(4)
73      DO 26 J=1,20
74      SJR(J,4)=-SJR(J,4)
75      26 SJL(J,4)=-SJL(J,4)
76      DO 49 IK=1,4
77      SAMPLE=SNJ(IK)
78      49 PENJ(IK)=ERRFN(SAMPLE,VARR)
79      DO 41 I=1,4

```



```

80      WRITE(3,44) I,SNJ(I)
81      DO 42 J=1,20
82      F=J
83      F=F/40.0
84      42 WRITE(3,43) F,SJR(J,I),SJL(J,I)
85      41 CONTINUE
86      44 FORMAT(/15X,'BIT SEQUENCE = ',I2,5X,'SNJ = ',F10.7,/)
87      43 FORMAT(5X,'JITTER = ',F10.7,5X,'SJR = ',F10.7,5X,'SJL = ',F10.7,/)
88      DO 50 JR=1,20
89      DO 50 IK=1,4
90      SAMPLE=SJR(JR,IK)
91      PEJR(JR,IK)=ERRFN(SAMPLE,VARR)
C
92      DO 51 JL=1,20
93      DO 51 IL=1,4
94      SAMPLE=SJL(JL,IL)
95      51 PEJL(JL,IL)=ERRFN(SAMPLE,VARR)
C
C
96      DO 48 IK=1,4
97      48 WRITE(3,47) IK,PENJ(IK)
98      47 FORMAT(5X,'BIT SEQUENCE = ',I2,5X,'PE NO JITTER = ',F10.7,/)
99      WRITE(3,779)
100     779 FORMAT(/75X,'THE FOLLOWING ARE THE PROBABILITIES OF BIT ERROR FOR
101           1 VARYING JITTER VALUES AND EACH SPECIFIC BIT SEQUENCE.',/)
102     DO 52 J=1,20
103     E=J
104     E=E/40.0
105     DO 52 IK=1,4
106     52 WRITE(3,91) E,IK,PEJR(J,IK),PEJL(J,IK)
107     91 FORMAT(5X,'JITTER = ',F10.7,5X,'BIT SEQ = ',I2,5X,'PEJR = ',F10.7,
108           15X,'PEJL = ',F10.7,/)
C
C
C     THE FOLLOWING COMPUTES THE PROBABILITY OF ERROR FOR A FIXED JITTER
C     VALUE TO THE RIGHT OR LEFT.
C
107     WRITE(3,777)
108     777 FORMAT(/75X,'THE FOLLOWING ARE THE PROB OF ERROR FOR FIXED VALUES
109           1 OF JITTER TO THE RIGHT',/)
110     DO 60 JR=1,20
111     TOTAL=0.0
112     E=JR
113     E=E/40.0
114     DO 61 IK=1,4
115     61 TOTAL=TOTAL+PEJR(JR,IK)
116     PERR1=TOTAL/4.0
117     PEFJR(JR)=PERR1
118     60 WRITE(3,311) E,PERR1
119     311 FORMAT(5X,'JITTER RIGHT = ',F10.7,5X,'PROB OF ERROR = ',F10.7,/)
C
119     WRITE(3,778)
120     778 FORMAT(/75X,'THE FOLLOWING ARE THE PROB OF ERROR FOR FIXED VALUES
121           1 OF JITTER TO THE LEFT',/)
122     DO 70 JL=1,20
123     TOTAL=0.0
124     E=JL
125     E=E/40.0
126     DO 71 IL=1,4
127     71 TOTAL=TOTAL+PEJL(JL,IL)
128     PERR2=TOTAL/4.0

```

```

128      PEFJL(JL)=PERR2
129      70 WRITE(3,377) E,PERR2
130      377 FORMAT(5X,'JITTER LEFT = ',F10.7,5X,'PROB OF ERROR = ',F10.7,/)
C
131      SUM=0.0
132      DO 277 I=1,4
133      277 SUM=SUM+PENJ(I)
134      PENJT=SUM/4.0
135      PEZJ=PENJT*(1.0/SQRT(2.*3.14159*SIGMA))
136      PESUM=0.0
137      DO 86 J=1,20
138      86 PESUM=PESUM+PEFJR(J)*PJ(J,SIGMA)
139      PETOTR=PESUM
140      PESUM1=0.0
141      DO 88 J=1,20
142      88 PESUM1=PESUM1+PEFJL(J)*PJ(J,SIGMA)
143      PETOTL=PESUM1
144      PETOT=PETOTR+PETOTL+PEZJ
145      WRITE(3,87) PETOT
146      87 FORMAT(10X,'TOTAL PROBABILITY OF ERROR = ', F10.7,/)
147      STOP
148      END

149      FUNCTION ERRFN(S,X)
150      AA=S/SQRT(2.0*X)
151      ERRFN=.5*ERFC(ABS(AA))
152      IF(AA.GT.0.0) ERRFN=1.0-ERRFN
153      RETURN
154      END

155      FUNCTION PJ(J,SIGMA)
156      PC=(1.0)/(SIGMA*SQRT(6.28318))
157      PX=(J*J)/(2.0*SIGMA*SIGMA)
158      PJ=0.0
159      IF(PX.GT.20.0) GO TO 9
160      PJ=PC
161      IF(PX.LE.0.0) GO TO 9
162      PJ=PC*EXP(-PX)
163      9 RETURN
164      END

165      SUBROUTINE FILTI(X,Z,WC,T)
166      REAL X(3),Z(3)
167      DO 50 I=1,3
168      50 X(I)=0.0
169      FACT=2.0/(WC*T)
170      Z(1)=1.+(FACT*SQRT(2.0))+(FACT*FACT)
171      Z(2)=2.0-(2.0*FACT*FACT)
172      Z(3)=1.0-(FACT*SQRT(2.0))+(FACT*FACT)
173      RETURN
174      END

175      SUBROUTINE FILT(X,Z,U,Y)
176      REAL X(3),Z(3)
177      X(1)=(U-Z(2)*X(2)-Z(3)*X(3))/Z(1)
178      Y=X(1)+2.*X(2)+X(3)
179      X(3)=X(2)
180      X(2)=X(1)
181      RETURN
182      END

```

```
183      FUNCTION GAUSS(S)
184      INTEGER IX/213711/
185      A=-6.
186      DO 1 I=1,12
187      A=A+RANDU(IX,IY)
188      1 IX=IY
189      GAUSS=A*S
190      RETURN
191      END

192      FUNCTION RANDU(IX,IY)
193      IY=IX*65539
194      IF(IY) 5,5,6
195      5 IY=IY+2147483647+1
196      6 X=IY
197      RANDU=X*.4656613E-9
198      RETURN
199      END

200      SUBROUTINE RAND(IX,IY,YFL)
201      IY = IX * 65539
202      IF (IY) 1,2,2
203      1 IY = IY + 2147483647+1
204      2 YFL = IY
205      YFL = YFL *.4656613E-9
206      IX = IY
207      RETURN
208      END
```

APPENDIX D

DIGITAL COMPUTER ALGORITHM FOR BIT DETECTION
USING FILTER/SAMPLE METHODS

```

/WAT4 EE142136,TIME=03,PAGES=050 WEBB QUENTIN R       70.329        JOB 132
/
LIMITS=(T=3,P=50,C=1)
CLASS=W,PRIORITY=04,REGION=0132K,READER=READER1
*****
C
C
C
C
C
C
C
C
1  INTEGER BIT(10)
2  DIMENSION AXISR(120),AXR(120),Y(120),YY(120)
3  REAL SNJF(240),SJRF(240),SJLF(240)
4  REAL SNR(6),SIGNJ(240),SNRZ(240),SNJ(4),PENJ(4)
5  REAL X(3),Z(3),SIGI(240),SIGF(240),NOISEI(601),NOISEF(601),
INOUT(601),CLK(240),PEJR(20,4),PEJL(20,4),PEFJR(20),PEFJL(20),
ISIGJR(240),SIGJL(240),SJRNRZ(240),SJLNRZ(240),SJR(20,4),SJL(20,4)
6  READ 101, (BIT(I),I=1,6)
7  101 FORMAT(6X,6I1)
8  PSNR=100.0
9  WRITE(3,29) PSNR
10  29 FORMAT(5X,'SIGNAL-TO-NOISE RATIO = ',F5.1,///)
C
C
C
C
C
11 THE PHASE ERROR(JITTER) VARIANCE IS FOUND IN THE TRACKING LOOP
12 ANALYSIS FOR A SPECIFIC TYPE OF INPUT TIME BASE JITTER.
C
13 BVAR=.1
C SIGMA=SQRT(BVAR)
C
14 B=SQRT(40.0)
C
C
C
C
14 THE RECEIVED NOISE IS PASSED THRU A 2.5 BIT RATE FILTER.
15 WC=15.7
16 T=.1
17 DO 11 I=1,601
11 NOISEI(I)=GAUSS(B)
18 CALL FILTI(X,Z,WC,T)
19 DO 22 J=1,601
20 CALL FILT(X,Z,NOISEI(J),FN)
21 22 NOISEF(J)=FN
C
C
C
C
22 THE FOLLOWING CALCULATES THE NOISE VARIANCE AT THE OUTPUT OF THE
23 BIT RATE/2 FILTER.
24 WN=3.14159
25 TT=.1
26 CALL FILTI(X,Z,WN,TT)
27 DO 14 I=1,601
14 CALL FILT(X,Z,NOISEI(I),BRN)
28 NOUT(I)=BRN
29 FNOISE=0.0
30 DO 3 K=1,601
3  FNOISE=FNOISE+NOUT(K)*NOUT(K)
31 FNVAR=FNOISE/600.0
32 FNSTDV=SQRT(FNVAR)
33 R=FNVAR/PSNR
34 WRITE(3,202) FNVAR
35 202 FORMAT(10X,'FILTERED NOISE VARIANCE = ',F12.7,///)
36 DO 4 J=1,6
37 INT1=J*40-39

```

```

38      INT2=INT1+19
39      AMPL=BIT(J)*2-1
40      DO 4 K=INT1,INT2
41      SIGI(K)=AMPL
42      4 SIGI(K+20)=-AMPL
      C
      C THE FOLLOWING IS THE REFERENCE CLOCK IN THE SYNCHRONIZER.
43      DO 36 J=1,201,40
44      JJ=J+19
45      DO 36 K=J,JJ
46      CLK(K)=+1.
47      36 CLK(K+20)=-1.
      C
      C THE INPUT SIGNAL IS PROCESSED BY A 2.5 BIT RATE FILTER PRIOR TO
      C ENTERING THE SIGNAL CONDITIONER/BIT SYNCHRONIZER.
48      WC=15.7
49      T=.1
50      CALL FILTI(X,Z,WC,T)
51      DO 41 I=1,240
52      CALL FILT(X,Z,SIGI(I),FS)
53      41 SIGF(I)=FS
      C
      C THE JITTERED SIGNAL IS CONVERTED FROM SPLIT-PHASE TO NON-RETURN-TO
      C -ZERO AND THEN IT IS PROCESSED BY A BIT RATE/2 FILTER.
54      WN=3.14159
55      TT=.1
56      CALL FILTI(X,Z,WN,TT)
57      DO 31 I=1,240
58      SIGNJ(I)=SIGF(I)
59      31 SNRZ(I)=CLK(I)*SIGNJ(I)
60      DO 33 I4=1,240
61      CALL FILT(X,Z,SNRZ(I4),FNJ)
62      33 SNJF(I4)=FNJ
63      WRITE(3,333) (SNJF(I),I=1,240)
64      333 FORMAT(//5X,'SIGNAL OUTPUT OF THE BIT RATE/2 FILTER',//,
        1(10X(10F10.7)))
65      DO 37 J=1,20
66      DO 38 I=1,240
67      IJ=I-J
68      JI=I+J
69      IF(IJ.LE.0) IJ=1
70      IF(JI.GT.240) JI=240
71      SIGJR(I)=SIGF(IJ)
72      SIGJL(I)=SIGF(JI)
73      SJRNZR(I)=CLK(I)*SIGJR(I)
74      38 SJLNRZ(I)=CLK(I)*SIGJL(I)
      C THE FOLLOWING FILTERS THE SIGNAL THRU THE BIT RATE/2 FILTER.
75      DO 34 I2=1,240
76      CALL FILT(X,Z,SJRNZR(I2),FSJR)
77      34 SJRF(I2)=FSJR
78      DO 35 I3=1,240
79      CALL FILT(X,Z,SJLNRZ(I3),FSJL)
80      35 SJLF(I3)=FSJL
      C
      C THE FOLLOWING SAMPLES THE SIGNAL OUTPUT OF THE BR/2 FILTER AT THE
      C END OF THE MID-BIT IN THE SPECIFIC BIT SEQUENCE.

```

```

81      IK=1
82      DO 39 K=80,200,40
83      SNJ(IK)=SNJF(K)
84      SJR(J,IK)=SJR(F(K)
85      SJL(J,IK)=SJLF(K)
86      39 IK=IK+1
87      37 CONTINUE
88      SNJ(4)=-SNJ(4)
89      DO 26 J=1,20
90      SJR(J,4)=-SJR(J,4)
91      26 SJL(J,4)=-SJL(J,4)
92      DO 141 I=1,4
93      WRITE(3,44) I,SNJ(I)
94      DO 42 J=1,20
95      F=J
96      F=F/40.0
97      42 WRITE(3,43) F,SJR(J,I),SJL(J,I)
98      141 CONTINUE
99      44 FORMAT(/15X,'BIT SEQUENCE = ',I2,5X,'SNJ = ',F10.7,/)
100     43 FORMAT(5X,'JITTER = ',F10.7,5X,'SJR = ',F10.7,5X,'SJL = ',F10.7,/)
      C
      C      THIS COMPUTES THE PROB OF ERROR FOR EACH BIT SEQUENCE AND VARYING
      C      VALUES OF TIME BASE JITTER J IN THE INCOMING BIT STREAM.
101     WRITE(3,108)
102     108 FORMAT(10X,'PROBABILITIES OF ERROR FOR VARYING JITTER VALUES AND
      C      1 EACH OF THE FOUR POSSIBLE BIT SEQUENCES',///)
103     DO 49 IK=1,4
104     SAMPLE=SNJ(IK)
105     49 PENJ(IK)=ERRFN(SAMPLE,R)
106     DO 48 IK=1,4
107     48 WRITE(3,47) IK,PENJ(IK)
108     47 FORMAT(5X,'BIT SEQUENCE = ',I2,5X,'PE NO JITTER = ',F10.7,/)
109     DO 51 J=1,20
110     E=J
111     E=E/40.0
112     DO 51 I=1,4
113     SR=SJR(J,I)
114     SL=SJL(J,I)
115     PEJR(J,I)=ERRFN(SR,R)
116     PEJL(J,I)=ERRFN(SL,R)
117     51 WRITE(3,57) E,I,PEJR(J,I),PEJL(J,I)
118     57 FORMAT(5X,'JITTER = ',F10.7,5X,'BIT SEQUENCE = ',I2,5X,
      C      1'PEJR = ',F10.7,5X,'PEJL = ',F10.7,/)
      C
      C      THIS COMPUTES THE AVERAGE PROB OF ERROR FOR A FIXED VALUE OF
      C      JITTER J OVER THE FOUR POSSIBLE INPUT BIT SEQUENCES.
119     DO 52 J=1,20
120     TOTR=0.0
121     TOTL=0.0
122     DO 53 I=1,4
123     TOTR=TOTR+PEJR(J,I)
124     53 TOTL=TOTL+PEJL(J,I)
125     TR=TOTR/4.0
126     TL=TOTL/4.0
127     PEFJR(J)=TR
128     52 PEFJL(J)=TL
      C

```

```

129      DO 56 J=1,20
130      F=J
131      F=F/40.0
132      56 WRITE(3,201) F,PEFJR(J),PEFJL(J)
133      201 FORMAT(5X,'JITTER = ',F10.7,5X,'PEFJR = ',F10.7,5X,'PEFJL = ',
1      F10.7,/)
C
C      THIS COMPUTES THE GROSS PROBABILITY OF BIT ERROR FOR THE SIGNAL
C      CONDITIONER/BIT SYNCHRONIZER FOR A GIVEN PSNR AND JITTER VARIANCE
C
134      SUM=0.0
135      DO 277 I=1,4
136      277 SUM=SUM+PENJ(I)
137      PENJT=SUM/4.0
138      PEZJ=PENJT*(1.0/SQRT(2.*3.14159*SIGMA))
139      PESUM=0.0
140      DO 86 J=1,20
141      86 PESUM=PESUM+PEFJR(J)*PJ(J,SIGMA)
142      PETOTR=PESUM
143      PESUM1=0.0
144      DO 88 J=1,20
145      88 PESUM1=PESUM1+PEFJL(J)*PJ(J,SIGMA)
146      PETOTL=PESUM1
147      PETOT=PETOTR+PETOTL+PEZJ
148      WRITE(3,97) PETOT
149      87 FORMAT(10X,'TOTAL PROBABILITY OF ERROR = ', F10.7,/)
150      STOP
151      END
152      FUNCTION ERRFN(S,X)
153      AA=S/SQRT(2.0*X)
154      ERRFN=.5*ERFC(ABS(AA))
155      IF(AA.GT.0.0) ERRFN=1.0-ERRFN
156      RETURN
157      END
158      FUNCTION PJ(J,SIGMA)
159      PC=(1.0)/(SIGMA*SQRT(6.28318))
160      PX=(J*J)/(2.0*SIGMA*SIGMA)
161      PJ=0.0
162      IF(PX.GT.20.0) GO TO 9
163      PJ=PC
164      IF(PX.LE.0.0) GO TO 9
165      PJ=PC*EXP(-PX)
166      9 RETURN
167      END
168      SUBROUTINE FILTI(X,Z,WC,T)
169      REAL X(3),Z(3)
170      DO 50 I=1,3
171      50 X(I)=0.0
172      FACT=2.0/(WC*T)
173      Z(1)=1.0+(FACT*SQRT(2.0))+(FACT*FACT)
174      Z(2)=2.0-(2.0*FACT*FACT)
175      Z(3)=1.0-(FACT*SQRT(2.0))+(FACT*FACT)
176      RETURN
177      END
178      SUBROUTINE FILT(X,Z,U,Y)
179      REAL X(3),Z(3)

```



```

180      X(1)=(U-Z(2)*X(2)-Z(3)*X(3))/Z(1)
181      Y=X(1)+2.*X(2)+X(3)
182      X(3)=X(2)
183      X(2)=X(1)
184      RETURN
185      END
.
186      FUNCTION GAUSS(S)
187      INTEGER IX/213711/
188      A=-6.
189      DO 1 I=1,12
190      A=A+RANDU(IX,IY)
191      1 IX=IY
192      GAUSS=A*S
193      RETURN
194      END
195      FUNCTION RANDU(IX,IY)
196      IY=IX*65539
197      IF(IY) 5,5,6
198      5 IY=IY+2147483647+1
199      6 X=IY
200      RANDU=X*.4656613E-9
201      RETURN
202      END
203      SUBROUTINE RAND(IX,IY,YFL)
204      IY = IX * 65539
205      IF (IY) 1,2,2
206      1 IY = IY + 2147483647+1
207      2 YFL = IY
208      YFL = YFL *.4656613E-9
209      IX=IY
210      RETURN
211      END

```