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Control aspects of a double-input buckboost power electronic converter

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CONTROL ASPECTS OF A DOUBLE-INPUT BUCKBOOST POWER ELECTRONIC CONVERTER

by

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ABSTRACT

Systems in which two or more energy sources combine to supply power to a common load are called hybrid energy systems. Applications of these systems have grown due to their flexibility and reliability. Hybrid energy systems have been successfully implemented in hybrid electric vehicles and wind-solar systems where two or more energy sources share the same load. Double-input (DI) dc-dc power electronic converters (DIPECs) have been gaining popularity in hybrid energy systems due to their reduced component count and control simplicity. In addition, employing DIPECs increases the reliability, stability, and flexibility of the system. In this thesis, a small-signal model for one of the DIPEC topologies, the DI buckboost converter, is developed and compensator design is carried out based on the small-signal model. The compensators are designed to accommodate optimal power sharing between the sources. Theoretically, it is also proven in this thesis that the two inputs of the DI buckboost topology can be independently controlled which gives great flexibility in terms of the compensator design. Time domain analysis of the system is carried out with the compensators included and the results agree with the theoretical analysis. In addition to the small-signal modeling, a new control method called offset time control is also introduced and successfully applied to a DIPEC topology in this thesis. The control scheme is based on adjusting the offset time between the switching commands; which is proven to have a direct impact on the amount of current drawn from each input. Small-signal modeling of the offset time control scheme has been carried out to prove the improvement in the speed of response of the system when the offset time control scheme is applied.

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1. INTRODUCTION

1.1. THE IMPORTANCE OF MULTI-INPUT CONVERTERS

Wind and solar energy generation is on the rise along with other green energy sources. The intermittent nature of these energy sources is the main drawback which has prevented their complete integration into mainstream energy generation. To address this issue, combining various energy sources with each other to form a hybrid energy system is proposed in the literature [1]. Batteries, ultra-capacitors, and flywheels are the most common energy storage mechanisms used to hybridize energy systems. Hybrid electric power-trains are other examples for energy systems with multiple sources. Hybridization can also happen at the energy storage level to combine ultra-capacitor and batteries together in order to make high power and high energy density storage systems.

In general, a dc-dc converter is required to integrate each energy related component into the system. Integrating each energy source with a dc-dc converter is expensive, bulky, less efficient, and hard to control. To overcome these shortfalls, using a single dc-dc isolated or non-isolated multi-input converter is proposed [1-16]. Utilizing a single dc-dc multi-input converter to integrate all the energy sources provides several advantages [7], including reduced component count, potential reduction in weight, control simplicity, and flexibility in the integration of the sources. Multi-input converters are much like their single-input counterparts in terms of the types of the components being used and the way they are connected. However, they are generally powered by at least two energy sources. In this thesis, the analysis and the discussion are based on DI dc-dc power converters (DIPECs), however, the same can be extended to other systems with more than two inputs.

1.2. ADVANTAGES AND CHALLENGES OF MULTI-INPUT CONVERTERS

Among several advantages [7], reduced component count, flexibility and control simplicity make DIPECs as attractive options to be utilized in hybrid energy systems where the input supplied power and the output load demand are variable. Several isolated and non-isolated DIPECs have been introduced, analyzed, and compared in the literature [9-16] including DI buck, buckboost, and buck-buckboost converters [9]. As suggested in [17] various topologies of these converters can be explored just by varying the number of common components. The authors of [17] also explore and compare various other topologies based on their reliability, flexibility, modularity potential, and cost.

DIPECs are also proven to be more flexible because various combinations of input voltages can be used to provide various combinations of output voltages. Compared to two single-input dc-dc converters which integrate two inputs to supply a common load, using a DIPEC is considered more advantageous in this case. This is because the inputs in a DIPEC topology would collaborate together to provide the required output voltage; whereas regulating the dc-bus voltage in the case with two single input converters would be much harder since the individual inputs compete to meet the load demand. The flexibility aspect of the DIPEC topologies when compared to two single-input dc-dc converters is explored in the next section.

The main challenge in the DIPEC topologies is the choice of the topology and the choice and implementation of the control strategy. Due to the availability of large number of these topologies the exact choice of the topology for a given application should be based on the type of the application and cost [17]. Also, the control strategy which decides on the amount of power supplied by each source plays an important role in DIPEC

topologies. And this control strategy varies from application to application thereby changing the control procedure.

1.2.1. Flexibility of the DIPEC Topologies in Power Sharing. In this section, a brief comparative study between two systems is carried out to show the amount of flexibility that is available in DIPEC topologies in terms of power sharing. In the first system, the sources are integrated to the load through two separate dc-dc converters (see Figs. 1.1 and 1.2). In the second system, the sources are integrated through a DIPEC topology (see Figs. 1.3 and 1.4). In both the cases, two different sources of V_1=40 V and V_2=70 V are being used to regulate the output voltage of the converter (V_0) at 90 V. In Fig. 1.1, a general block diagram of the first system is presented. In this case, source 1 is a fuel cell (FC) or an ultra-capacitor (UC) and source 2 can be a battery energy storage system (BESS). In Fig. 1.2, a specific case of Fig. 1.1 is presented where two single-input dc-dc buckboost converters are connected in parallel at the output to provide a constant output voltage of 90 V. It can be clearly seen from Fig. 1.2 that two capacitors and two inductors are needed in this case which adds to the cost, weight, and losses of the system.

The output voltage equation for the system (see Fig. 1.2) is given by [28, 29]:

$$V_0 = \frac{D_1 V_1}{(1-D_1)} \quad and \quad V_0 = \frac{D_2 V_2}{(1-D_2)} \tag{1.1}$$

where D_1 and D_2 and are the duty ratios of switches S_1 and S_2, respectively. Therefore, in order to regulate the output voltage at 90 V there is only one solution for (1.1) which is given by D_1=0.69 and D_2=0.5625. The main advantages of connecting two dc-dc

converters in parallel are 1) to increase the current rating of the system at low voltages, 2) to increase the fault-tolerance and modularity of the system [30].

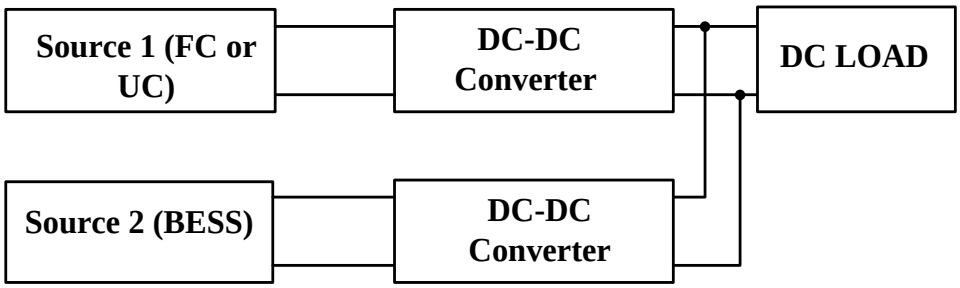

Fig. 1.1. General block diagram of a system with two single-input dc-dc converters

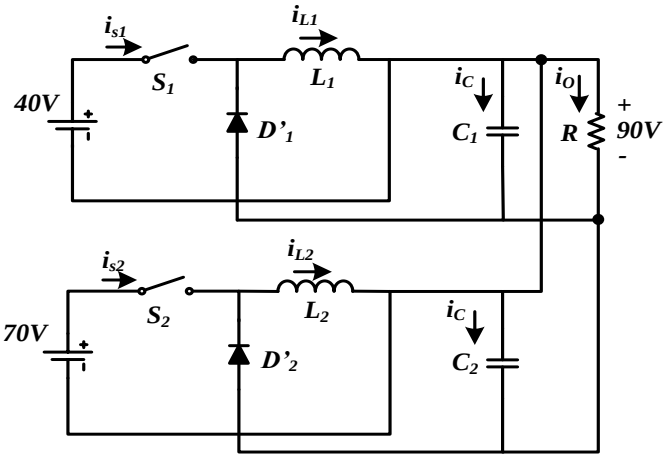

Fig. 1.2. Two independent single-input buckboost converters regulating the output voltage to 90 V

However, it must also be observed that this type of parallel connection is not ideal for systems which have different inputs with different voltages, i.e., V_1 and V_2. This is because both the loops in this case have to be regulated using the output voltage as a

reference signal and in the absence of any current sharing compensator the two converters interact with each other which causes oscillations in the output voltage and the duty ratio of the converter with the lower voltage loop gain gets saturated as mentioned in [30]. Therefore, the converters in this case compete with each other to meet the load demand.

The voltage loop gain of the converters is dependent on the converter parameters like V_1, L_1, C_1 and V_2, L_2, C_2 and therefore, it is hard to exactly match the voltage loop gains of converters with non-identical parameters. Therefore, a current sharing compensator must be used in this case which provides control over the amount of power supplied by each source. The design of the current sharing compensator is hard and has only been carried out for systems with equal input voltages and for equal current sharing among the sources [30-32]. In other words, it is hard to control the amount of power supplied by the FC or UC and the BESS and the system is not exactly suited for energy or power diversification between the two sources which is a major drawback of this system.

In the second system, a DIPEC topology is used to integrate both the sources to the load as shown in Fig. 1.3. In Fig. 1.4, a specific case of a DIPEC topology (DI buckboost converter) is used to integrate the sources to the load which has a single inductor and capacitor thereby reducing the number of components in the system. The steady-state output voltage V_0 of the DI buckboost converter can be described as [9, 14]:

$$V_0 = \frac{D_1 V_1}{(1 - D_1 - D_2)} + \frac{D_2 V_2}{(1 - D_1 - D_2)} \tag{1.2}$$

where D_1 and D_2 are again duty ratios of switches S_1 and S_2, respectively.

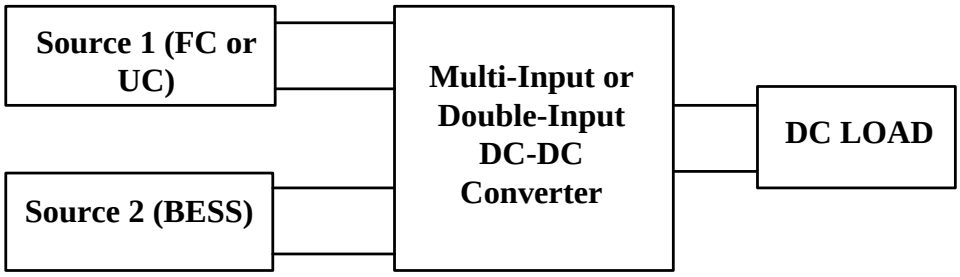

Fig. 1.3. General block diagram of a DIPEC topology

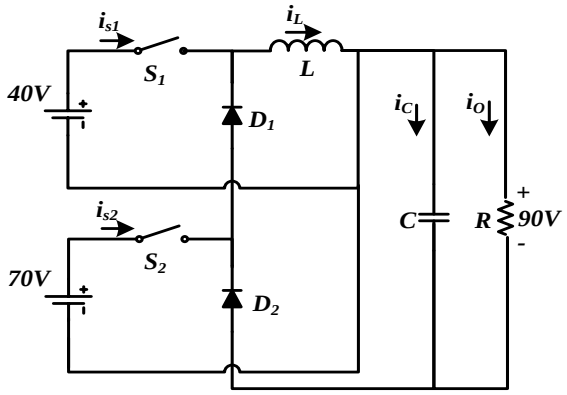

Fig. 1.4. DI buckboost converter regulating the output voltage at 90 V

In this case, (1.2) has more than one solution and a few of the solutions of (1.2) along with the average input powers supplied (P_1 and P_2) are presented in Fig. 1.5. It can be clearly observed from Fig. 1.5 that while keeping the output voltage and load constant, the amount of power supplied by each source P_1 and P_2 can be varied by varying duty ratios D_1 and D_2 without changing the inductor size, i.e., without interfering with the power stage. Thus, it can be concluded that the DI buckboost converter provides a lot of flexibility in terms of power sharing between the two sources. This flexibility in terms of power sharing is the main advantage DIPEC topologies provide in renewable energy

applications where the sources can be intermittent. However, the flexibility in power sharing also calls for a well-defined control strategy or control objective which decides on the amount of power supplied from each source based on factors like battery state-of-charge (SOC), solar irradiance, etc. Apart from power sharing, the control strategy should also focus on load regulation through a constant output voltage. These control challenges are presented in the next section.

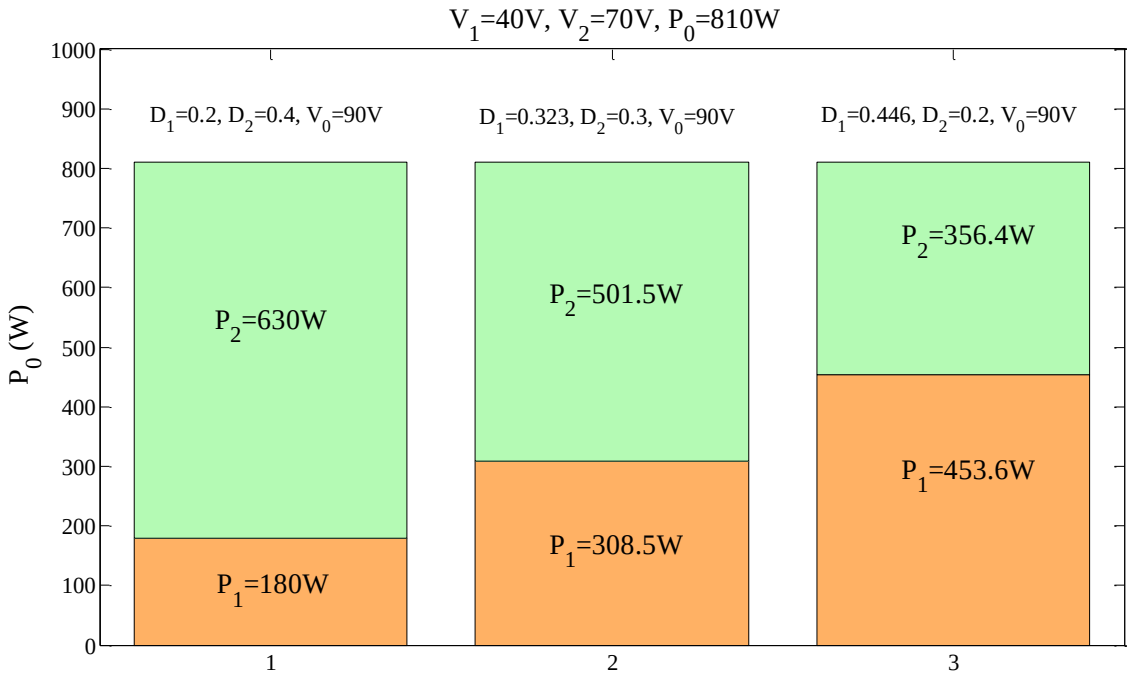

Fig. 1.5. Flexibility in power sharing of a DI buckboost converter when output voltage and load are constant

1.2.2. Control Challenges. As mentioned earlier, the control strategy plays a very prominent role in DIPEC topologies. Most of the work reported in this field only covers topology exploration and steady state operation of such converters. Different approaches to synthesize DI converters have also been reported earlier [13-19]. The control aspects for specific multi-input topologies are discussed in few papers [20-26]. Control of the amount of power drawn from each of the sources in a hybrid energy system is important. When the power supplied by one of the sources decreases, the power supplied by other sources must be managed effectively to meet the load demand.

Power sharing is necessary in hybrid energy systems such as a wind and solar combination or a battery and ultra-capacitor combination. For instance, on a cloudy day when the amount of solar power being supplied is less, the amount of power from other energy sources needs to increase. Also, in a battery and ultra-capacitor combination when the ultra-capacitor is discharged, the power drawn from the battery should be increased to meet the load demand. Thus, the controller must be able to control the amount of power flowing out from each individual source.

In [9], the importance of battery and ultra-capacitor combination for hybrid electric vehicles is emphasized and the various DIPEC topologies that can be used to realize the battery and ultra-capacitor integration are explored. One of the DIPEC topologies explored in [9] is the DI buckboost (see Fig. 1.4) topology which is introduced in [16]. In [16], a multiple-input buckboost converter is introduced and its steady state operation is discussed; the analysis and the equations can be simplified to a DI buckboost converter by assuming only two inputs. The DI buckboost converter is used for photovoltaic (PV)-grid integration in [21] and it is proven that input powers of the system

can be flexibly controlled while maintaining a constant output voltage. In [22], the same system is controlled such that maximum power is supplied by the PV array using ripple correlation control and the additional load demand is met by the grid for a constant load. In [27], the multi-input buckboost topology is slightly modified for bidirectional power flow and for operating the converter in all the three modes i.e. buck, boost and buckboost modes.

In this thesis, the same DI buckboost converter is controlled; however, the control objective in this case is different and the controller design is based on small-signal modeling of the DIPEC topologies which has not been reported earlier. In this thesis, the control objective is power sharing between the sources (e. g. battery and ultra-capacitor) for a variable load, where one of the sources is expected to supply a constant power and the other source is expected to meet the excess load demand during load variations while the output voltage is regulated. The authors of [23] propose a similar control objective for another DIPEC topology, the DI buck-buckboost converter.

1.3. SMALL-SIGNAL MODELING

DIPEC topologies are nonlinear systems just like their single-input counterparts and they have to be linearized. Linear time invariant (LTI) models of the converters are necessary for a systematic controller design. Development of such models is also crucial for analyzing system stability and for designing optimal compensators. In this thesis, the LTI small-signal model of the DI buckboost converter is developed. Various transfer functions necessary for realizing the control objective mentioned in the previous section are also developed. In this thesis, it is analytically proven in that the two control loops

controlling the two switches S_1 and S_2 are nearly independent of each other for the DI buckboost converter. This feature of the loops being independently controllable makes the compensator design much simpler as the two compensators can now be independently designed. Compensator design based on the transfer functions is carried out.

1.4. OFFSET TIME CONTROL

In this thesis, it is proven that the offset time between the switch commands has a direct impact on the power sharing of the two sources. Therefore, the proposed control method is called offset time control. Apart from the two control variables which happen to be the switch commands, controlling the offset time as an additional control variable gives an extra degree of freedom in meeting the control objectives. It is also shown that using the offset time as an additional control variable helps in regulating the output voltage faster when compared to a system with no offset time control.

1.5. THESIS ORGANIZATION

This thesis is organized into five sections; in Section 2 the small-signal modeling of the DI buckboost converter is carried out. Compensator design based on models developed in Section 2 is carried out in Section 3. It is also analytically proven in this section that the two control loops which control the two control inputs are nearly independent of each other and the compensators for the loops can be independently

designed. Offset time control scheme and its relevant equations are developed in Section 4 in which the advantages of having offset time control are discussed. Conclusions and future work are presented in Section 5.

2. SMALL-SIGNAL ANALYSIS OF A DI BUCKBOOST CONVERTER

Power electronic converters are nonlinear systems and to test the transient stability they have to be linearized by carrying out small-signal analysis. Compensators can then be designed based on the developed Linear Time Invariant (LTI) models in order to meet various control objectives. Small-signal analysis for single input dc-dc converters is very well established in the literature [28, 29]. However, small-signal modeling for DIPEC topologies has not been reported yet. Although, the control of DIPEC topologies has been reported in the literature [21, 23], a systematic design procedure of compensators based on LTI models has not been reported yet.

Small-signal models for the DIPEC topologies are necessary in order to optimize the compensator design and to provide a stable system which meets all the control objectives. This being the intention, the small-signal analysis of a DI buckboost converter is carried out in this section. A small-signal circuit model for the topology is also developed and various transfer functions that are responsible for the control of the converter are derived and analyzed. Similar analysis can be carried for other DIPEC topologies which are listed in [17] and the required transfer functions can then be derived from the obtained small-signal models.

2.1. DI BUCKBOOST CONVERTER

The circuit diagram of a DI buckboost converter is shown again in Fig. 2.1 [9, 12, 16, and 21]. In this topology, switch S_1 can be any kind of switch as long as V_1 is greater than V_2. However, if V_1 is not guaranteed to be greater than V_2 then S_1 needs to be a

reverse-blocking switch, such as an IGBT [13]. The DI buckboost converter has mode restriction and it cannot be powered by both the sources at the same time. In other words, both switches S_1 and S_2 cannot be ON at the same time [9]. The procedure to obtain the small-signal model for the DI buckboost converter is described in the next section. Modes of operation of the converter and the voltage across the inductor (V_L) are shown in Table 2.1.

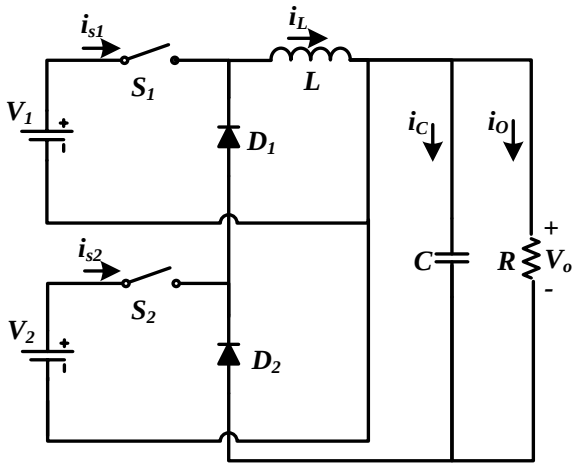

Fig. 2.1. Block diagram of a DI buckboost converter

Table. 2.1. Modes of operation of a DI buckboost converter

Mode	S_1	S_2	V_L
I	ON	OFF	V_1
II	OFF	ON	V_2
III	OFF	OFF	$-V_O$
IV	ON	ON	Not Allowed

2.2. DEVELOPMENT OF THE SMALL-SIGNAL MODEL

In a DI buckboost converter, the time varying circuit averaged equations (see Figs.2.2 and 2.3) which describe the low frequency behavior of the system are:

$$\langle v_L(t)\rangle_{T_s} = L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = d_1(t)v_1(t) + d_2(t)v_2(t) - \{1 - d_1(t) - d_2(t)\}\langle v_o(t)\rangle_{T_S} \tag{2.1}$$

$$\langle i_C(t)\rangle_{T_S} = C\frac{d\langle v_o(t)\rangle_{T_S}}{dt} = -\frac{\langle v_o(t)\rangle_{T_S}}{R} + \{1 - d_1(t) - d_2(t)\}\langle i_L(t)\rangle_{T_S} \tag{2.2}$$

where d_1(t) and d_2(t) are the time dependent duty ratios of switches S_1 and S_2, respectively. Equation (2.1) is obtained by finding the average of the voltage across the inductor v_L(t) during the ON time of the switches which is indicated by the dashed line in Fig. 2.2. Then average v_L(t) during the OFF time is found which is indicated by the other dashed line. The actual average inductor voltage during the whole switching cycle is shown in (2.1) is found by averaging the inductor voltage v_L(t) during the ON time and OFF time of the swithches and is indicated by the dotted line in the Fig. 2.2. In steady state this dotted line is very close to zero assuming there are no inductor current losses. Similar procedure is used to obtain (2.2) by averaging the capacitor current waveform shown in Fig. 2.3 when the switches are ON and OFF, respectively. The dotted lines shown in Figs. 2.2 and 2.3 represent the circuit averaged equations of (2.1) and (2.2) and the system would follow these dotted lines in a time-domain simulation when the circuit averaged model is used.

However, (2.1) and (2.2) both have terms which are products of time varying quantities and therefore the model is still a non-linear model and it cannot be used to

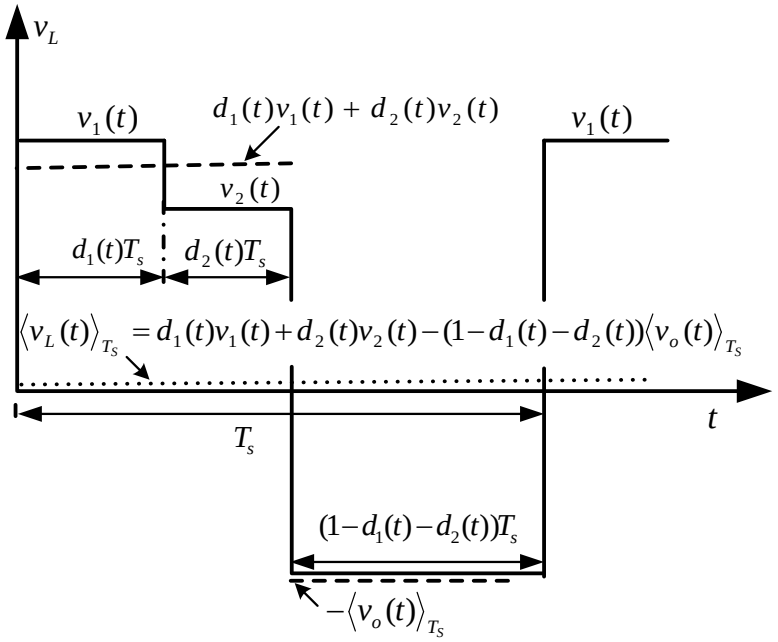

Fig. 2.2. Inductor voltage waveform and averaged inductor voltage waveform (indicated by dotted line)

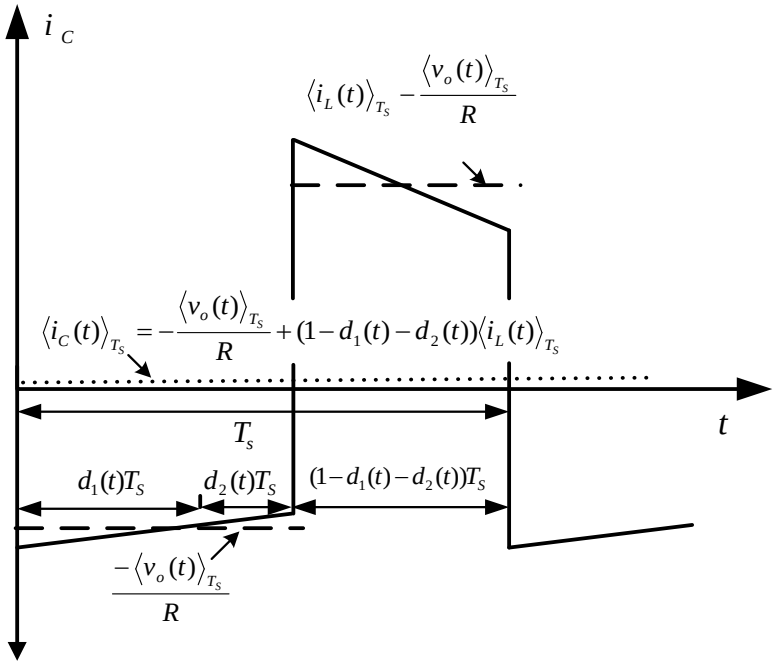

Fig. 2.3. Capacitor current waveform and averaged capacitor current waveform (indicated by dotted line)

predict the system behavior during load or input voltage transients. The model given by (2.1) and (2.2) can be linearized around a steady state operating point by including small-signal ac perturbations around the operating point. Then the time varying quantities in (2.1) and (2.2) change to:

$$\begin{aligned} d_1(t) &= D_1 + \hat{d}_1(t) \\ d_2(t) &= D_2 + \hat{d}_2(t) \\ v_1(t) &= V_1 + \hat{v}_1(t) \\ v_2(t) &= V_2 + \hat{v}_2(t) \\ \langle v_o(t) \rangle_{T_S} &= V_0 + \hat{v}_o(t) \\ \langle i_L(t) \rangle_{T_S} &= I_L + \hat{i}_L(t) \end{aligned} \tag{2.3}$$

In (2.3) all the values in capital case are steady state values and all the values with a hat are small-signal ac perturbations. Replacing the time varying parameters in (2.1) and (2.2) with the values in (2.3) would give:

$$\begin{aligned} L\frac{d(I_L + \hat{i}_L(t))}{dt} &= (D_1 + \hat{d}_1(t))(V_1 + \hat{v}_1(t)) + (D_2 + \hat{d}_2(t))(V_2 + \hat{v}_2(t)) \\ &\quad - (1 - D_1 - \hat{d}_1(t) - D_2 - \hat{d}_2(t))(V_0 + \hat{v}_o(t)) \end{aligned} \tag{2.4}$$

$$C\frac{d(V_0 + \hat{v}_o(t))}{dt} + \frac{(V_0 + \hat{v}_o(t))}{R} = (1 - D_1 - \hat{d}_1(t) - D_2 - \hat{d}_2(t))(I_L + \hat{i}_L(t)) \tag{2.5}$$

Neglecting the product of small-signal perturbed ac terms and equating the derivatives of the steady state terms to zero on both sides in (2.4) and (2.5) yeilds:

$$L\frac{d\hat{i}_L(t)}{dt} = D_1\hat{v}_1(t) + D_2\hat{v}_2(t) + (V_1 + V_0)\hat{d}_1(t) + (V_2 + V_0)\hat{d}_2(t) - (1 - D_1 - D_2)\hat{v}_o(t) \tag{2.6}$$

$$C\frac{d\hat{v}_o(t)}{dt} + \frac{\hat{v}_o(t)}{R} = -(\hat{d}_1(t) + \hat{d}_2(t))I_L + (1 - D_1 - D_2)\hat{i}_L(t) \tag{2.7}$$

Converting (2.6) and (2.7) into frequency domain using the Laplace Transformation would give[28, 29]:

$$\begin{aligned} sL\hat{i}_L(s) = {} & D_1\hat{v}_1(s) + D_2\hat{v}_2(s) + (V_1 + V_0)\hat{d}_1(s) + (V_2 + V_0)\hat{d}_2(s) \\ & -(1 - D_1 - D_2)\hat{v}_o(s) \end{aligned} \tag{2.8}$$

$$sC\hat{v}_o(s) + \frac{\hat{v}_o(s)}{R} = -(\hat{d}_1(s) + \hat{d}_2(s))I_L + (1 - D_1 - D_2)\hat{i}_L(s) \tag{2.9}$$

The process of obtaining small-signal model for the DIPEC topologies is very similar to the process ascertained for single-input dc-dc converters [28, 29]. The only difference for DIPEC topologies is that in this case there are two control inputs $\hat{d}_1, \hat{d}_2$ and also two disturbance inputs $\hat{v}_1, \hat{v}_2$. Multi-phase converters and converters connected in parallel also have more than one control input as discussed in [31]; however, in such systems the control inputs are generally made equal (i.e. $\hat{d}_1 = \hat{d}_2 = \hat{d}$) for equal current sharing in the inductors. The input side of the small-signal model which has the switch current perturbations can be obtained by perturbing the steady state switch current equations. The equations for steady state average switch currents I_{s1} and I_{s2} are given by

$$I_{s1} = D_1 I_L \tag{2.10}$$

$$I_{s2} = D_2 I_L \tag{2.11}$$

Equations (2.10) and (2.11) in perturbed form give

$$\begin{aligned} & I_{s1} + \hat{i}_{s1}(s) = (D_1 + \hat{d}_1(s))(I_L + \hat{i}_L(s)) \\ \Rightarrow\ & \hat{i}_{s1}(s) = I_L\hat{d}_1(s) + D_1\hat{i}_L(s) \end{aligned} \tag{2.12}$$

$$I_{s2} + \hat{i}_{s2}(s) = (D_2 + \hat{d}_2(s))(I_L + \hat{i}_L(s))$$
$$\Rightarrow \hat{i}_{s2}(s) = I_L \hat{d}_2(s) + D_2 \hat{i}_L(s) \quad . \tag{2.13}$$

The small-signal model shown in Fig. 2.4 is obtained by combining (2.8), (2.9), (2.12) and (2.13) into current sources, voltage sources, current dependent sources, and voltage dependent sources. In Fig. 2.4, the voltage and current sources which have either of the control inputs $\hat{d}_1$ or $\hat{d}_2$ in the product are independent sources and all the other sources which have the disturbance inputs $\hat{v}_1$ or $\hat{v}_2$, inductor current $\hat{i}_L$, and output voltage $\hat{v}_o$ states are dependent sources.

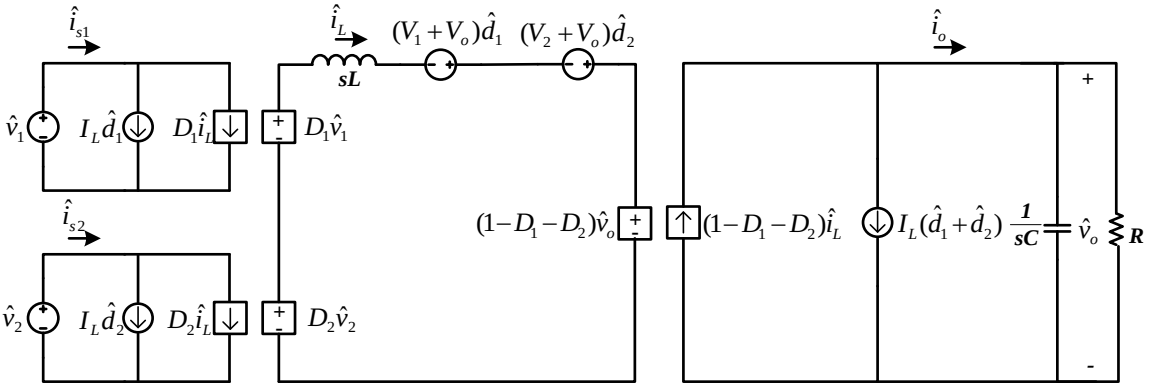

Fig. 2.4. Small-signal model of a DI buckboost converter

2.3. TRANSFER FUNCTIONS DERIVATION BASED ON THE SMALL-SIGNAL MODEL

It can be observed from Fig. 2.4 that the model has two control inputs $\hat{d}_1$, $\hat{d}_2$ and two disturbance inputs $\hat{v}_1, \hat{v}_2$ and all the other perturbations are dependent on these four

inputs. Without loss of generality, the control inputs $\hat{d}_1$, $\hat{d}_2$ are called as Control-1 and Control-2, respectively throughout the thesis. The two control inputs $\hat{d}_1$, $\hat{d}_2$ can be controlled based on various control objectives like maximum power point tracking or optimal power sharing between the inputs etc.

The transfer functions required to meet the various control objectives can be derived from the small-signal model shown Fig. 2.4. For instance, to study the effects of the perturbations in D_1 on output voltage V_0, one should find the transfer function $G_{vd1}(s)$. This is called as the control-1 $\hat{d}_1$ to output $\hat{v}_0$ transfer function therefore it is named as G_{vd1}(s); the naming is similar to the control to output transfer function of single-input dc-dc converters which is G_{vd}(s). This transfer function can be obtained from Fig 2.4 by assuming the disturbance inputs $\hat{v}_1 = \hat{v}_2 = 0$ and also the control-2 $\hat{d}_2 = 0$ resulting in Fig. 2.5. In order to obtain the transfer function Kirchoff's voltage law (KVL) and Kirchoff's current law (KCL) must be applied in circuit as shown in Fig. 2.5 this will simplify (2.8) and (2.9) to (2.14) and (2.15).

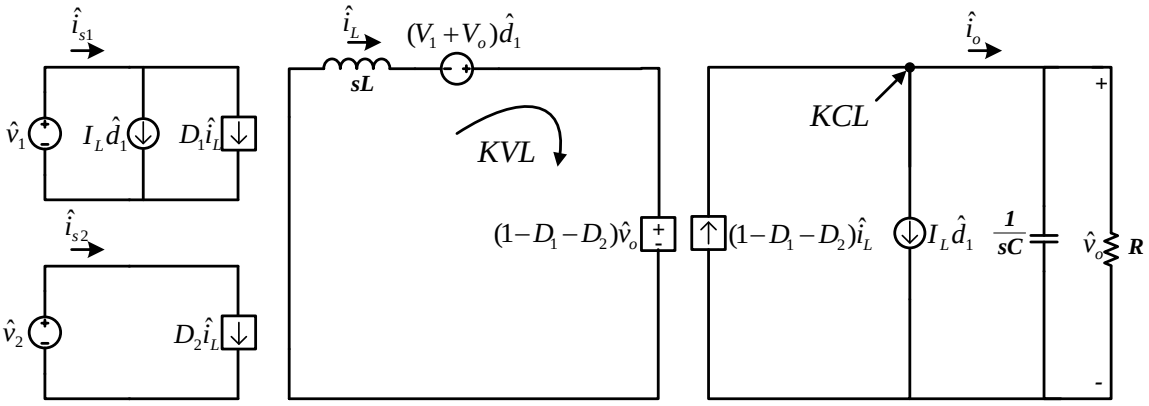

Fig. 2.5. Small-signal model of a DI buckboost converter when $\hat{d}_2 = \hat{v}_1 = \hat{v}_2 = 0$

$$\hat{i}_L(s) = \frac{(V_1 + V_0)\hat{d}_1(s) - (1 - D_1 - D_2)\hat{v}_o(s)}{sL} \tag{2.14}$$

$$\left(sC + \frac{1}{R}\right)\hat{v}_o(s) = -\hat{d}_1(s)I_L + (1 - D_1 - D_2)\hat{i}_L(s) \tag{2.15}$$

Eliminating $\hat{i}_L(s)$ from (2.14) and (2.15) results in

$$\left(sC + \frac{1}{R}\right)\hat{v}_o(s) = -\hat{d}_1(s)I_L + (1 - D_1 - D_2)\frac{(V_1 + V_0)\hat{d}_1(s) - (1 - D_1 - D_2)\hat{v}_o(s)}{sL} \tag{2.16}$$

Equation (2.16) can be further simplified to

$$\left(sC + \frac{1}{R} + \frac{(1 - D_1 - D_2)^2}{sL}\right)\hat{v}_o(s) = (-I_L + \frac{(1 - D_1 - D_2)(V_1 + V_0)}{sL})\hat{d}_1(s) \tag{2.17}$$

Equation (2.17) can be further simplified to

$$G_{vd1}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2 = \hat{v}_1 = \hat{v}_2 = 0} = \frac{(V_1 + V_0)(1 - D_1 - D_2) - sLI_L}{s^2LC + s\frac{L}{R} + (1 - D_1 - D_2)^2} \tag{2.18}$$

This transfer function is a second order system with a resonant pole pair and a right-half plane (RHP) zero. The RHP zero is a characteristic of the buckboost converters and it limits the bandwidth of the system. If D_2 is zero, then the transfer function will be reduced to that of a single input buckboost converter [28]. Similarly, the effect of the perturbations in D_2 on the output voltage V_o can be found by assuming $\hat{v}_1 = \hat{v}_2 = 0$ and also control-1 $\hat{d}_1 = 0$ and following the same procedure as

$$G_{vd2}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=\hat{v}_1=\hat{v}_2=0}=\frac{(V_2+V_0)(1-D_1-D_2)-sLI_L}{s^2LC+s\frac{L}{R}+(1-D_1-D_2)^2} \tag{2.19}$$

This transfer function is the control-2 to output transfer function and hence its name is G_{vd2}(s). Transfer function G_{vd2}(s) and its response are very similar to G_{vd1}(s) except for term V_2 in the numerator. This similarity is due to the fact that both the inputs of the system are connected to the output in a buckboost configuration. Transfer functions G_{vd1}(s) and G_{vd2}(s) would be different in case of other DIPEC topologies like DI buck-buckboost where one input is connected to the output in the buck configuration and the other input is connected to the output in the buckboost configuration. In such a case, it would be easier to regulate the output voltage by controlling the switch of the input connected in buck configuration; since, there will be a RHP zero in the control to output transfer function of input connected in buckboost configuration which will limit the bandwidth of the system. These are some of the design choices that will be available to the designer which are non-existent in the single-input topologies.

One can also study how perturbations in D_1 effect the inductor current and this is obtained by eliminating $\hat{v}_o(s)$ from (2.14) and (2.15) which leads to

$$G_{id1}(s)=\left.\frac{\hat{i}_L(s)}{\hat{d}_1(s)}\right|_{\hat{d}_2=\hat{v}_1=\hat{v}_2=0}=\frac{(V_1+V_0)(\frac{1}{R}+sC)+(1-D_1-D_2)I_L}{s^2LC+s\frac{L}{R}+(1-D_1-D_2)^2} \tag{2.20}$$

The control-1 to inductor current transfer function G_{id1}(s) is important when implementing a current-mode control scheme for controlling D_1 [32]. Similarly, the effect of perturbations in D_2 on the inductor current is given by

$$G_{id2}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=\hat{v}_1=\hat{v}_2=0} = \frac{(V_2+V_0)(\frac{1}{R}+sC)+(1-D_1-D_2)I_L}{s^2LC+s\frac{L}{R}+(1-D_1-D_2)^2} \tag{2.21}$$

If the objective is to maintain one of the average switch currents constant the following transfer functions shown in (2.24) and (2.25) are important in this context. Control-to-switch current gain for the buck converter has been derived in [33] in which average switch current in each cycle is controlled using charge control. Similar analysis can be carried out for the DI buckboost converter to obtain the control-2 to switch current 2 transfer function G_{is2d2}(s). From Fig. 2.4 the switch current 2 perturbations $\hat{i}_{s2}(s)$ are given by (2.22) and it is also known that the inductor current perturbations are functions of both the control inputs $\hat{d}_1$ and $\hat{d}_2$ as shown in (2.23)

$$\hat{i}_{s2}(s) = I_L\hat{d}_2(s) + D_2\hat{i}_L(s) \tag{2.22}$$

$$\hat{i}_L(s) = G_{id1}(s)\hat{d}_1(s) + G_{id2}(s)\hat{d}_2(s) \tag{2.23}$$

Substittuting (2.23) in (2.22) and commanding the control-1 $\hat{d}_1$=0 leads to the required transfer function

$$\Rightarrow \hat{i}_{s2}(s) = I_L \hat{d}_2(s) + D_2 G_{id1}(s)\hat{d}_1(s) + D_2 G_{id2}(s)\hat{d}_2(s)$$

$$\Rightarrow G_{is2d2}(s) = \left.\frac{\hat{i}_{s2}(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=0} = I_L + D_2 G_{id2}(s)$$

$$G_{is2d2}(s) = \left.\frac{\hat{i}_{s2}(s)}{\hat{d}_2(s)}\right|_{\hat{d}_1=\hat{v}_1=\hat{v}_2=0} = I_L + D_2 \frac{(V_2+V_0)(\frac{1}{R}+sC)+(1-D_1-D_2)I_L}{s^2LC + s\frac{L}{R} + (1-D_1-D_2)^2} \tag{2.24}$$

Similar analysis leads to the control-1 to switch current 1 transfer function G_{is1d1}(s):

$$G_{is1d1}(s) = \left.\frac{\hat{i}_{s1}(s)}{\hat{d}_1(s)}\right|_{\hat{d}_1=\hat{v}_1=\hat{v}_2=0} = I_L + D_1 \frac{(V_1+V_0)(\frac{1}{R}+sC)+(1-D_1-D_2)I_L}{s^2LC + s\frac{L}{R} + (1-D_1-D_2)^2} \tag{2.25}$$

From (2.24) and (2.25) it can be seen that the transfer functions G_{is1d1}(s) and G_{is2d2}(s) are important when one of the switch currents needs to be maintained constant and thereby supplying constant power from one of the sources irrespective of the load demand.

2.4. VERIFICATION OF THE TRANSFER FUNCTIONS BASED ON TIME DOMAIN ANALYSIS

Few of the developed transfer functions are verified in this section. As mentioned earlier, the control objective in this thesis is to supply constant power from one of the sources and meet the additional load demand from the other source even during load and input variations. The control objective can be realized by regulating output voltage V_0 through the control of the control variable D_1 and by maintaining the average switch current I_{s2} as constant through the control of the other control variable D_2 as shown in Fig.

2.6. In Fig. 2.6, the two loops are being independently controlled and this feature of the loops being independently controllable will be analytically proved in Section 3.

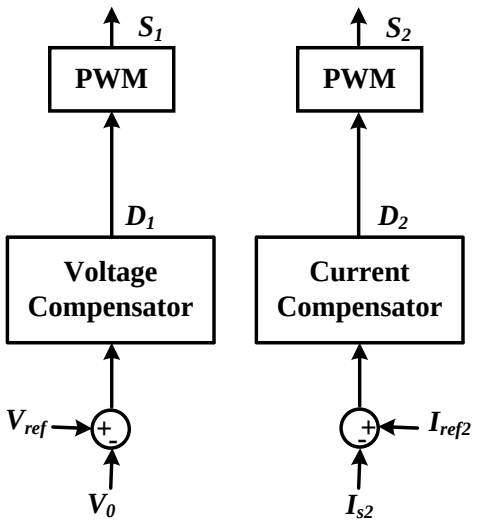

Fig. 2.6. Proposed control procedure with independent control of the loops to realize the control objective

In order to regulate the output voltage by controlling D_1, one needs to analyze transfer function $G_{vd1}(s) = \frac{\hat{v}_o(s)}{\hat{d}_1(s)}$ developed in (2.18). This transfer function is obtained at the following operating point:

V_1=40 V, V_2=70 V, V_0=90 V, L=50 µH, C=120 µF, R=10 Ω, D_1=0.2, and D_2=0.4

Initially, a time domain simulation is carried out at the same operating point by inducing small-signal time domain ac sinusoidal perturbations $\hat{d}_1(t)$ =0.05*sin(2π*f*t) at a given frequency 'f'. These ac small-signal perturbations impact output voltage V_0 and will

cause small-signal perturbations of $\hat{v}_o(t)$ as shown in the block diagram of Fig. 2.7. The simulation setup for measuring the effect of small-signal variations $\hat{d}_1(t)$ on $\hat{v}_o(t)$ is shown in Fig. 2.8 and the simulation is carried out in Matlab/Simulink. The model is designed considering all the diodes and switches are ideal. Also, the new model is designed to based on the equations of the components rather than using the components directly as this would reduce the simulation time. Apart from that the model is similar to a switched model of a converter that can be built in PSPICE or Simpower. This impact can be converted into frequency domain using

$$G_{vd1}(s) = \frac{\hat{v}_o(s)}{\hat{d}_1(s)} = 20 * \log\left(\frac{\hat{v}_o(t)}{\hat{d}_1(t)}\right) dB \tag{2.26}$$

Similarly, perturbations are induced at various other frequencies and a comparison is carried out between the measured G_{vd1}(s) and predicted G_{vd1}(s) as shown in the Fig. 2.9. The predicted function is obtained by calculating G_{vd1}(s) at the operating point and it is plotted in MATHCAD as shown in Fig. 2.9. As mentioned previously the system is a classic two pole system with a RHP zero which further introduces a phase delay of 90˚ in addition to the 180˚ caused by the resonant pole pair thereby making the system to settle at a phase angle of -270˚. It can be seen that there is a good match between the measurements made in time domain and those predicted through the bode plot. This indicates that the obtained transfer function G_{vd1}(s) is accurate. It must be noted here that in real time applications, the time domain measurements are obtained through a network analyzer [28] or through a digital modulator when the measured signal is discrete in which case analog modulation results are not accurate [34]. The transfer function G_{vd1}(s) can

therefore be used for designing a compensator for output voltage regulation through control of D_1. Similar analysis can be performed on transfer function G_{vd2}(s) and its time domain and frequency domain response would be very similar to G_{vd1}(s) as discussed earlier since both the inputs are connected in buckboost configuration to the output. Therefore, G_{vd2}(s) can also be used to regulate output voltage V_0 using control variable D_2.

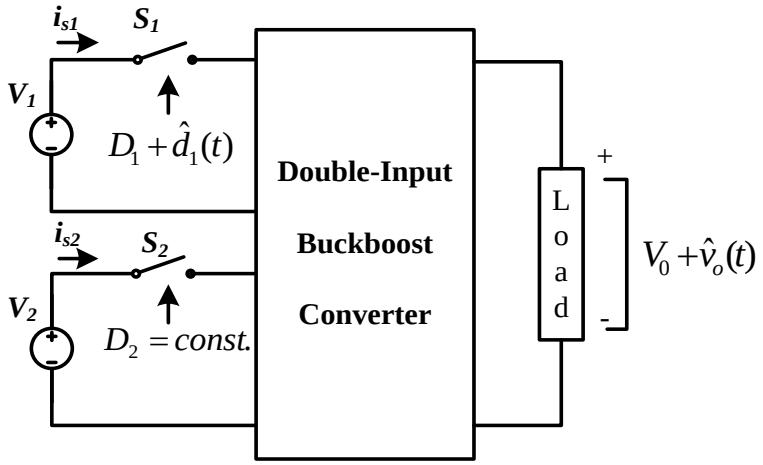

Fig. 2.7. Block diagram showing the effect of small-signal variations in $\hat{d}_1(t)$ on $\hat{v}_o(t)$

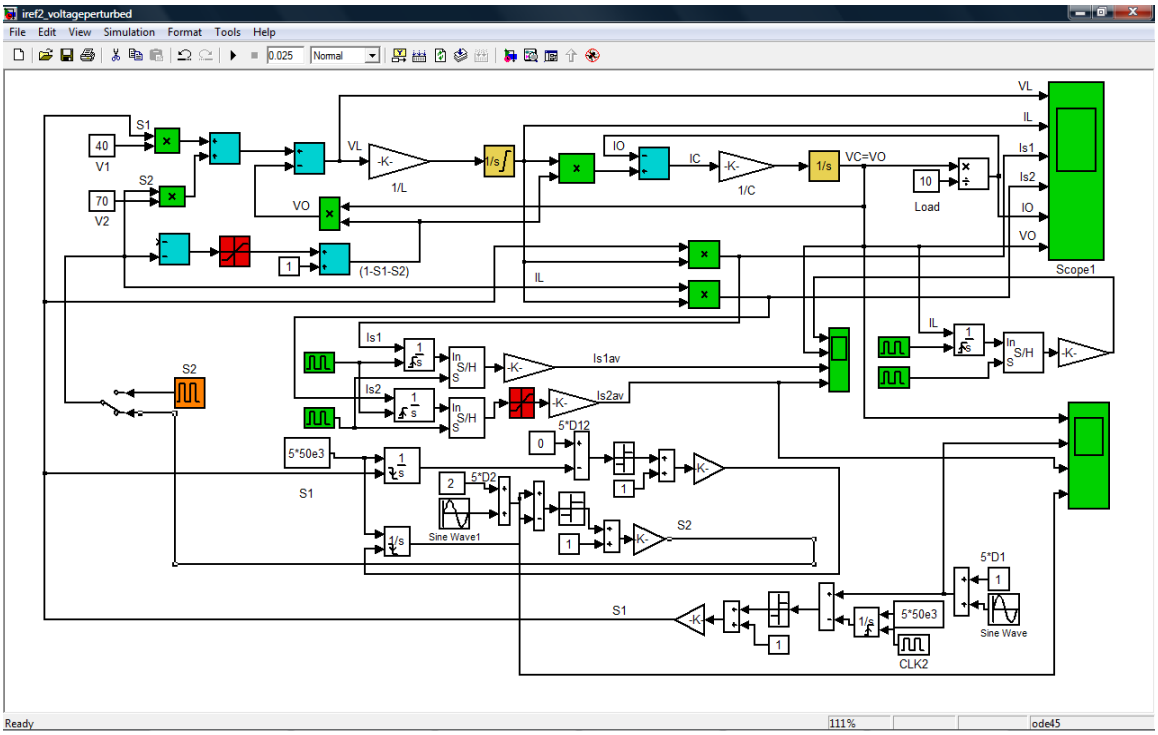

Fig. 2.8. Simulation setup for measuring the effect of small-signal variations in $\hat{d}_1(t)$ on $\hat{v}_o(t)$

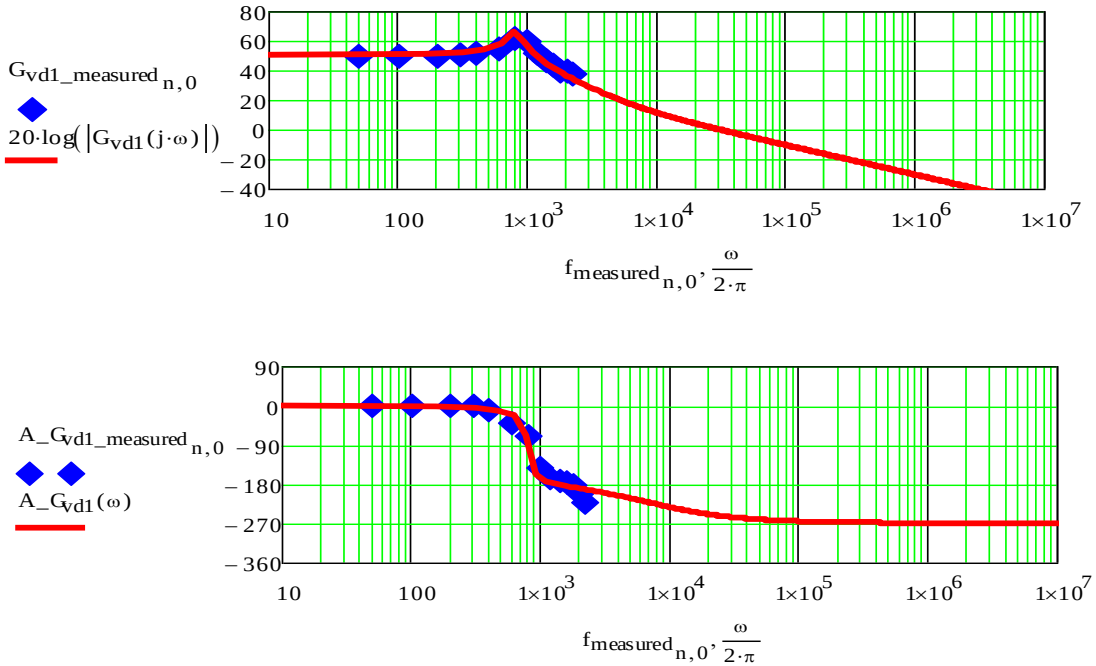

Fig. 2.9. Bode plot for the transfer function G_{vd1}(s)

In order to maintain average switch current I_{s2} constant by controlling duty ratio D_2, a current compensator must be designed (see Fig. 2.6) for transfer function G_{is2d2}(s) = $\frac{\hat{i}_{s2}(s)}{\hat{d}_2(s)}$ developed in (2.24). The transfer function G_{is2d2}(s) developed in (2.24) is therefore analyzed here to test its accuracy by comparing it to a time-domain simulation. Initially, a time domain simulation is carried out to study the effect of time domain ac sinusoidal perturbations in $\hat{d}_2(t)$=0.05*sin (2π*f*t) at a given frequency 'f'. These ac small-signal perturbations will impact the average switch current I_{s2} of source 2 and it will have small-signal variations of $\hat{i}_{s2}(t)$ as shown in the block diagram of Fig. 2.10 and the simulation setup is similar to the one shown in Fig. 2.8 except that now D_2 is perturbed with $\hat{d}_2(t)$ and $\hat{i}_{s2}(t)$ is measured. This impact can be converted into frequency domain using

$$G_{is2d2}(s) = \frac{\hat{i}_{s2}(s)}{\hat{d}_2(s)} = 20 * \log\left(\frac{\hat{i}_{s2}(t)}{\hat{d}_2(t)}\right) dB \qquad (2.27)$$

The same procedure is applied at various other frequncies and the measured G_{is2d2}(s) is compared with the predicted G_{is2d2}(s) as shown in Fig. 2.11. The predicted function is obtained by calculating G_{is2d2}(s) at the operating point and it is plotted in MATHCAD as shown in Fig. 2.11. The transfer function follows a single-pole response at low frequencies dominated by the transfer function G_{id2}(s) in (2.24) but at high-frequencies the response is dominated by the inductor current I_L and therefore the phase angle settles at 0˚ at high-frequencies. The good match between the values indicates that

the model obtained for the G_{is2d2}(s) is also accurate and it can be used to design the current compensator.

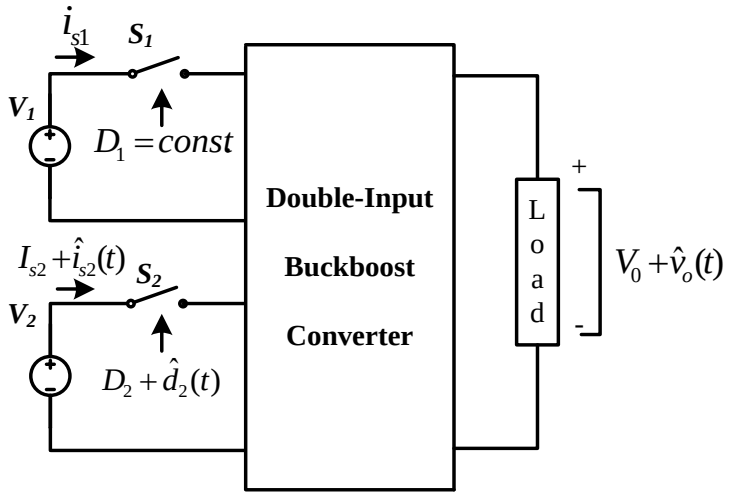

Fig. 2.10. Block diagram showing the effect of small-signal variations in $\hat{d}_2(t)$ on $\hat{i}_{s2}(t)$

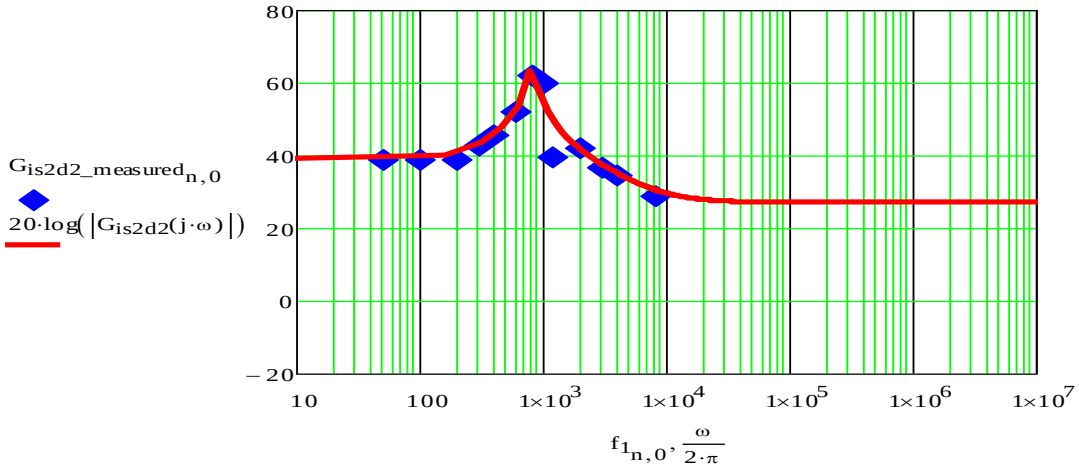

Fig. 2.11. Bode plot for the transfer function G_{is2d2}(s)

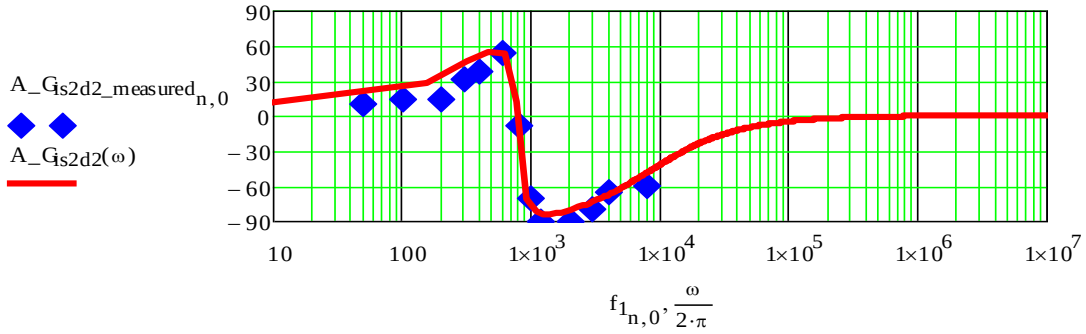

Fig. 2.11. Bode plot for the transfer function G_{is2d2}(s) (cont.)

Since developed transfer functions G_{vd1}(s) and G_{is2d2}(s) are accurate, it is important to discuss the procedure for the compensator design based on the control objective and to analytically prove the independency of the two control loops. These results are discussed and presented in Section 3. These results would aid in the formation of a stable closed-loop control system which meets all the control objectives and helps in optimizing the compensator design.

3. COMPENSATOR DESIGN AND INDEPENDENT CONTROL OF THE LOOPS

Compensator design for the DI buck boost converter is presented in this section. Chen et al. propose the following control strategies for DI buck-buckboost converter topology in [23], for various types of applications as shown in Table 3.1.

Table. 3.1. Different control strategies for DI converters

Case	Source 1	Source 2	Load
1	P_1=constant	P_2=variable	P_{out}=variable
2	P_1=variable	P_2=constant	P_{out}=variable
3	P_1=constant	P_2=constant	P_{out}=constant

It can be seen from the Table 3.1 that cases 1 and 2 are similar and in both of the cases one of the sources is supplying constant power and the other source is supplying variable power to meet the load demand during load variations. In case 3 both of the sources are controlled to supply constant powers and the load must be capable of taking the amount of supplied power. In cases 1 and 2, constant power is supplied from one of the sources by commanding the average switch currents, either I_{s1} or I_{s2}, as constant through the control of either D_1 or D_2 alongwith maintaining output voltage regulation by having V_0 constant through the control of the other control variable D_2 or D_1. The block diagram showing the control procedure for case 2 is shown in Fig. 3.1 which has been

developed by Chen et al. in [23] for another DIPEC topology, the DI buck-buckboost topology. Similar control procedure and control objective are applied in this section for a DI buckboost converter. From Fig. 3.1 it is also evident that the control signals from the voltage and current compensators are being added to generate control signal S_2 in order to include the effect of output voltage variations on duty ratio D_2 and switching signal S_2. It will be proved in the next section that this addition of the control signals is unnecessary if the current compensator is designed well.

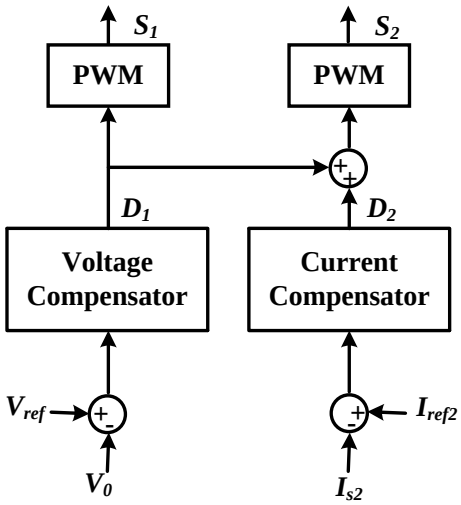

Fig. 3.1. Block diagram of the control system for case 2 where I_{s2} and V_0 are constant

3.1. INDEPENDENT CONTROL OF THE LOOPS

The system shown in Fig. 3.1 is a multiloop control system with a current control loop and voltage control loop. Current mode control of the single-input converters also forms a multi-loop system [34-35]. Modeling as well as analysis of the loop gains to

predict the stability are complex in the multi-loop systems [35] when compared to single-loop systems because of interaction between loop gains. Therefore, an effort is made in this section to simplify the multi-loop system of the DI buckboost converter into several individual and independent loops. In this section, it is analytically proven that control inputs $\hat{d}_1(s)$ and $\hat{d}_2(s)$ can be independently controlled with each loop having a different control objective, i.e., one of the loops is able to regulate output voltage V_0 and the other loop is regulating average switch current I_{s2} of source 2. The inner current control loop is shown in the Fig. 3.2 and average current mode control (ACMC) scheme is used to keep switch current I_{s2} constant. Transfer function G_{is2d2}(s) (the control-2 to switch current-2 gain) which is responsible for this has been developed and analyzed in Section 2. However, perturbations in $\hat{i}_{s2}(s)$ are also dependent on the control-1 $\hat{d}_1(s)$ and this dependency is given by transfer function G_{is2d1}(s) as shown in Fig. 3.2 and in (3.1).

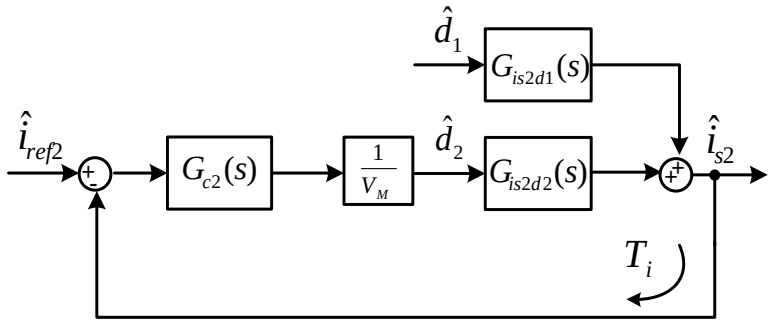

Fig. 3.2. Block diagram of the converter system with the inner current loop closed

$$\hat{i}_{s2}(s) = G_{is2d1}(s)\hat{d}_1(s) + G_{is2d2}(s)\hat{d}_2(s) \tag{3.1}$$

In order reduce this dependency, the perturbations $\hat{d}_1(s)$ are considered as disturbance signals for the inner current control loop once the loop is closed and this leads to

$$\hat{i}_{s2}(s) = \frac{G_{is2d1}(s)}{1+T_i(s)}\hat{d}_1(s) + \frac{T_i(s)}{1+T_i(s)}\hat{i}_{ref2}(s) \tag{3.2}$$

It is also known that the output voltage is a function of both the control input perturbations and this relation is given as:

$$\hat{v}_o(s) = G_{vd1}(s)\hat{d}_1(s) + G_{vd2}(s)\hat{d}_2(s) \tag{3.3}$$

Replacing $\hat{d}_2(s)$ with corresponding perturbations in $\hat{i}_{s2}(s)$ by using Fig. 3.2 results in

$$\hat{v}_o(s) = G_{vd1}(s)\hat{d}_1(s) + G_{vd2}(s)\frac{G_{c2}(s)}{V_M}\hat{i}_{s2}(s) \tag{3.4}$$

Equation (3.4) can be further simplified using (3.2) to

$$\hat{v}_o(s) = G_{vd1}(s)\hat{d}_1(s) + G_{vd2}(s)\frac{G_{c2}(s)}{V_M}\left(\frac{G_{is2d1}(s)}{1+T_i(s)}\hat{d}_1(s) + \frac{T_i(s)}{1+T_i(s)}\hat{i}_{ref2}(s)\right) \tag{3.5}$$

If the current control loop is faster than the voltage loop then $\hat{i}_{ref2}(s) \approx 0$ and therefore (3.5) becomes

$$\hat{v}_o(s) = G_{vd1}(s)\hat{d}_1(s) + G_{vd2}(s)\frac{G_{c2}(s)}{V_M}\left(\frac{G_{is2d1}(s)}{1+T_i(s)}\right)\hat{d}_1(s) \tag{3.6}$$

The new transfer function control-1 to output transfer function G_{new}(s) shown in (3.7) is dependent on G_{vd2}(s), G_{is2d1}(s) and the current compensator G_{c2}(s). G_{vd2}(s) and G_{is2d1}(s) functions can be derived following the procedure listed in Section 2 however, the current compensator G_{c2}(s) must be designed in order to compare the functions G_{vd1}(s) and G_{new}(s).

$$G_{new}(s) = \frac{\hat{v}_o(s)}{\hat{d}_1(s)} = G_{vd1}(s) + G_{vd2}(s)\frac{G_{c2}(s)}{V_M}\left(\frac{G_{is2d1}(s)}{1+T_i(s)}\right) \tag{3.7}$$

3.2. CURRENT COMPENSATOR G_{C2}(S) DESIGN

In this section, the current compensator design is discussed for the control of average switch current. Average current mode control has been extensively reported and implemented in the literature [31, 32, 36-39] for single-input topologies in which the average inductor current is generally controlled. Controlling the average inductor current for equal current sharing between inputs of a parallel connected dc-dc converter is discussed in [40]. In few papers like [33] and [41], the control of average input switch current for single-input topologies is proposed. Similar analysis is needed here to maintain the average switch current of one of the sources in the DI converter constant (in order to supply constant power from that source). This is the proposed control objective for case 1 and case 2 of Table 3.1.

Here, the analysis would be for case 2 to maintain I_{s2} constant and for this G_{is2d2}(s) is the transfer function for which a current compensator G_{c2}(s) must be designed in order to complete the current control loop T_i(s) as shown in Fig. 3.2. Bode plots of the transfer

function G_{is2d2}(s), the compensator G_{c2}(s) and the loop gain T_i(s) are shown in Fig. 3.3. It can be observed from Fig. 3.3 that transfer function G_{is2d2}(s) has enough phase margin. Therfore, it can be compensated just by using an integrator. However, in doing so the phase tends to -180˚ in the 1-10 kHz region and so the phase margin would not be enough in this case. Therefore, a Type-II (proposed in [42-44]) phase lead compensator which consists of two poles and a zero is used. This compensator gives a phase boost in the 1-10 kHz region and the gain of the compensator is adjusted to get the desired crossover frequency of around 2.5 kHz. The compensator G_{c2}(s) has a zero at frequency f_z=1.526 kHz and two poles at frequencies f_{p1} and f_{p2} one at origin f_{p1}=0 and the other at f_{p2}=22.07 kHz. The compensator transfer function is

$$G_{c2}(s) = \frac{400}{s}\left(\frac{1+\frac{s}{2\pi*1.526*10^3}}{1+\frac{s}{2\pi*22.07*10^3}}\right) \tag{3.8}$$

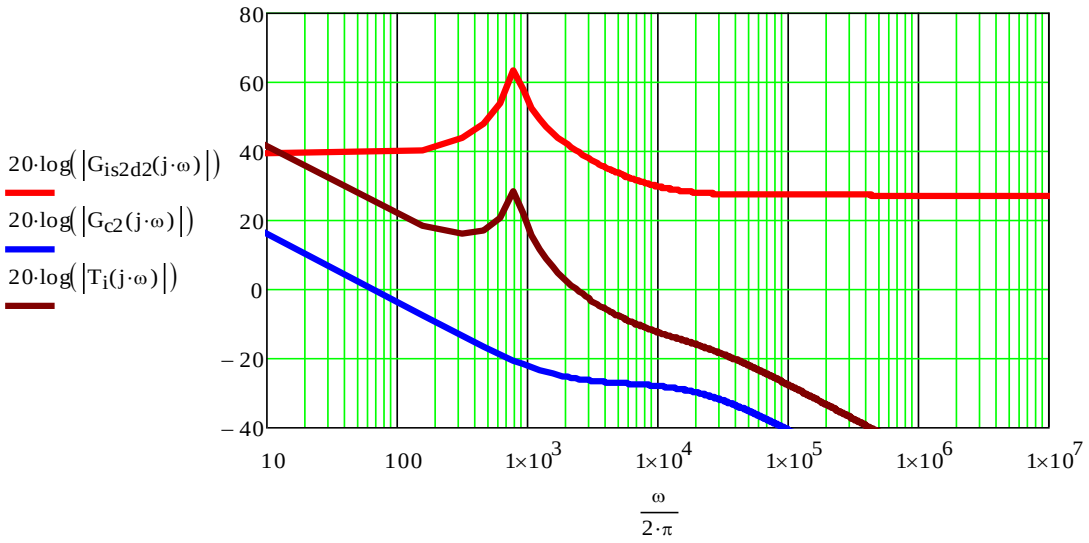

Fig. 3.3. Bode plots of the functions G_{is2d2}(s), G_{c2}(s) and T_i(s) of the system

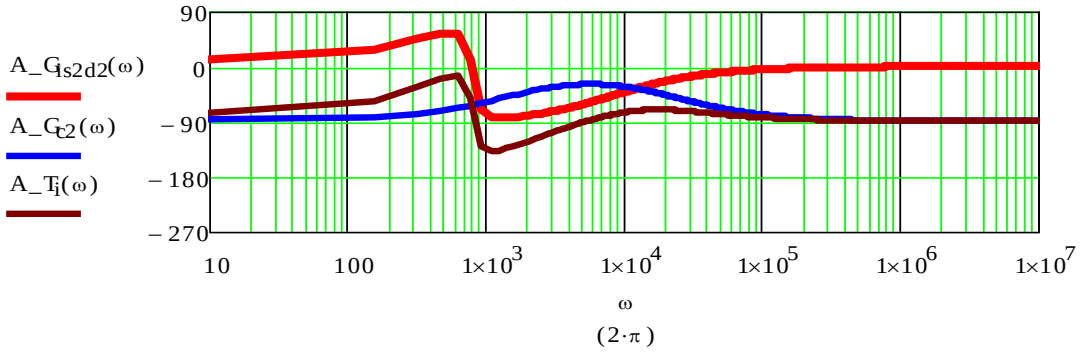

Fig. 3.3. Bode plots of the functions G_{is2d2}(s), G_{c2}(s) and T_i(s) of the system (cont.)

It can be observed from loop gain $T_i(s)$ in Fig. 3.3 that the system has a phase margin of 63˚ at the crossover frequency which is 2.365 kHz. Thus, the inner control T_i(s) is a stable control loop since its phase margin is positive and the phase margin and cross over frequency are enough to meet load and line transients with a fast settling time and a low overshoot. Now that the current compensator G_{c2}(s) is designed and the inner current control loop T_i(s) is a stable; the new control-1 to output transfer function G_{new}(s) can be calculated using (3.7). G_{new}(s) can be compared to the actual control-1 to output transfer function G_{vd1}(s). The bode plots of the transfer functions G_{vd1}(s) and G_{new}(s) are plotted in Fig. 3.4 and it can be seen that the two functions are close to each other over a wide frequency range both in terms of the magnitude and phase.

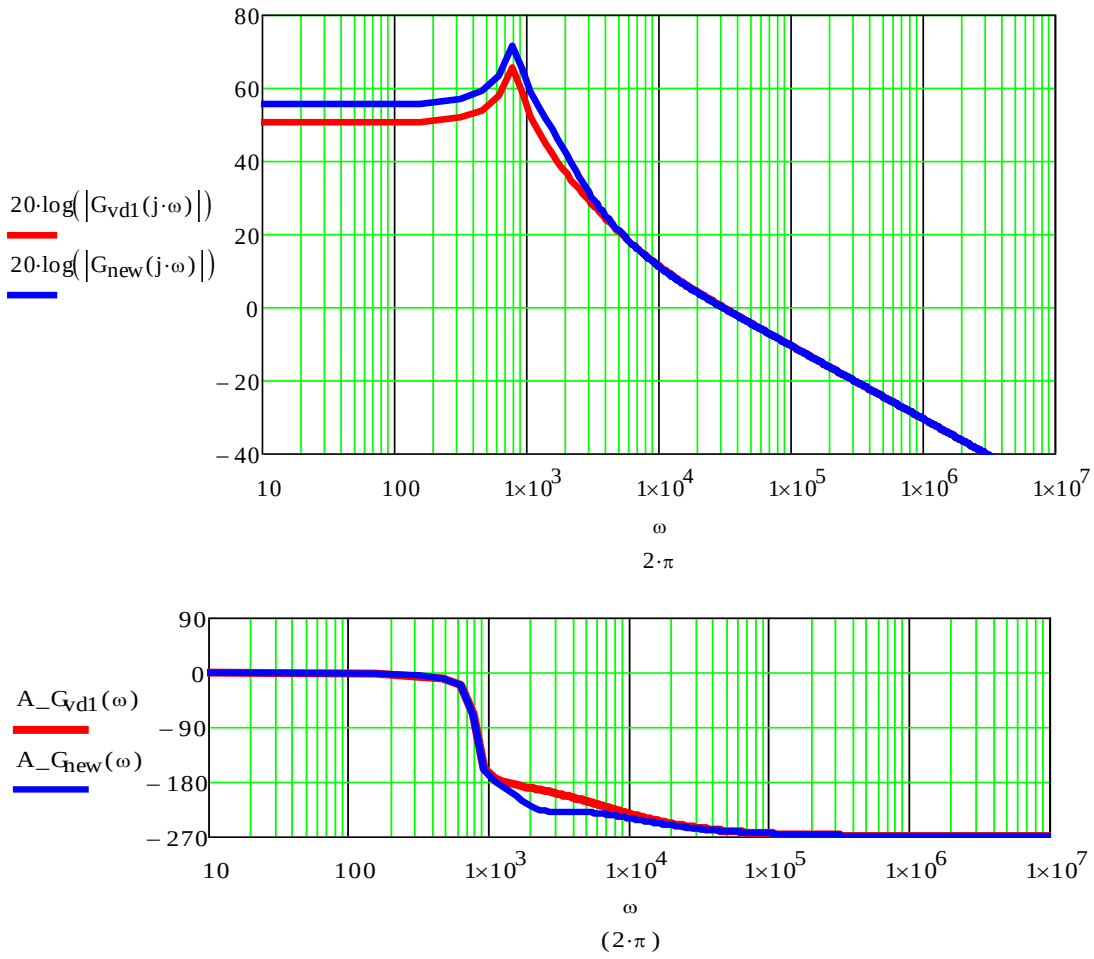

Fig. 3.4. Comparison between G_{vd1}(s) and G_{new}(s) to verify the independency of the loops

Therefore, it can be concluded that voltage compensator G_{c1}(s) can be designed independently neglecting the loop dynamics of current control loop T_i(s). However, it must be noted that this independent control of the two loops and the negligible effect of the inner current loop T_i(s) on the outer loop dynamics is true only if current compensator G_{c2}(s) is well designed and inner current loop T_i(s) is stable. It has already been proven that T_i(s) is a stable loop with a positive phase margin and therefore, both T_i(s) and T_v(s) can be independently controlled as shown in Fig. 3.5.

3.3. VOLTAGE COMPENSATOR G_{C1}(S) DESIGN

In this section, voltage compensator which is used to regulate output voltage (V_0) and its design is discussed and inner loop T_i(s) dynamics are neglected as shown in Fig. 3.5. The design procedure is similar to that of voltage mode controller design of single-input buckboost topology. In [42], the voltage mode controller design for converters with RHP zeros, i.e., the boost and the buckboost converters operating in CCM and DCM is elaborately presented. The DI buckboost converter is also operating in CCM and it also has a RHP zero and therefore, the same design methodology can be extended for this case.

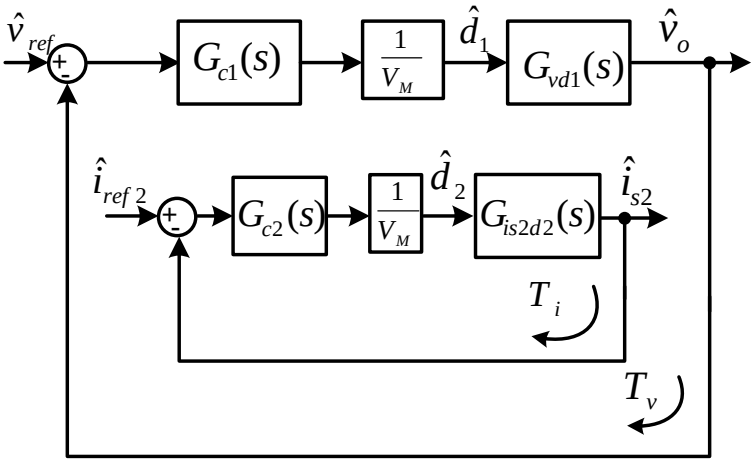

Fig. 3.5. Small-signal control loop of the DI buckboost converter where I_{s2} and V_0 are constant and the loops are independently controlled

The voltage compensator must be designed for control-1 to output gain (G_{vd1}(s)) as shown in Fig. 3.5. Bode plots of transfer function G_{vd1}(s), voltage compensator G_{c1}(s), and loop gain T_v(s) are shown in Fig. 3.6. It can be observed from Fig. 3.6 that the phase

angle of G_{vd1}(s) goes from 0˚ to -180˚ once the system reaches the resonant pole pair frequency f_{LC}=821.8 Hz and it gradually reaches a phase angle of -270˚ due to the RHP zero which is present at frequency f_{RHP}=7356 Hz. Therefore, the system requires a phase boost in the 1-25 kHz region. To provide this phase lead, a Type III compensator with two zeros and three poles is used. The zeros are placed at frequencies f_{z1}=f_{z2}=575.311 Hz which is 0.7*f_{LC} based on the design procedure. One of the poles is fixed at the origin f_{p1}=0 Hz and the other two poles are placed at frequencies f_{p2}=f_{p3}=36.78 kHz which is above half the switching frequency of 25 kHz. Placing these two poles at higher frequencies helps in increasing the phase margin of the system and provides good load regulation. Finally, the gain of the compensator is adjusted to have a crossover frequency of 1.285 kHz which makes the voltage loop slower than current loop T_i(s). Voltage loop T_v(s) has to be slower than current loop T_i(s) since in the dc-dc converter the output voltage states are slower than the inductor current states [29]. The final compensator transfer function is

$$G_{c1}(s) = \frac{30}{s}\left(\frac{1+\frac{s}{2\pi*575.311}}{1+\frac{s}{2\pi*36780}}\right)^2 \tag{3.9}$$

It can be observed from Fig. 3.6 that the system has a phase margin of 42˚ at the required crossover frequency of 1.285 kHz which makes the voltage loop T_v(s) a stable loop. Now that compensators G_{c1}(s) and G_{c2}(s) are designed, a time domain simulation is carried out to test the stability of the system during load changes, i.e., for load regulation. And the

system has to achieve the control objective as well. These results are presented in the next section.

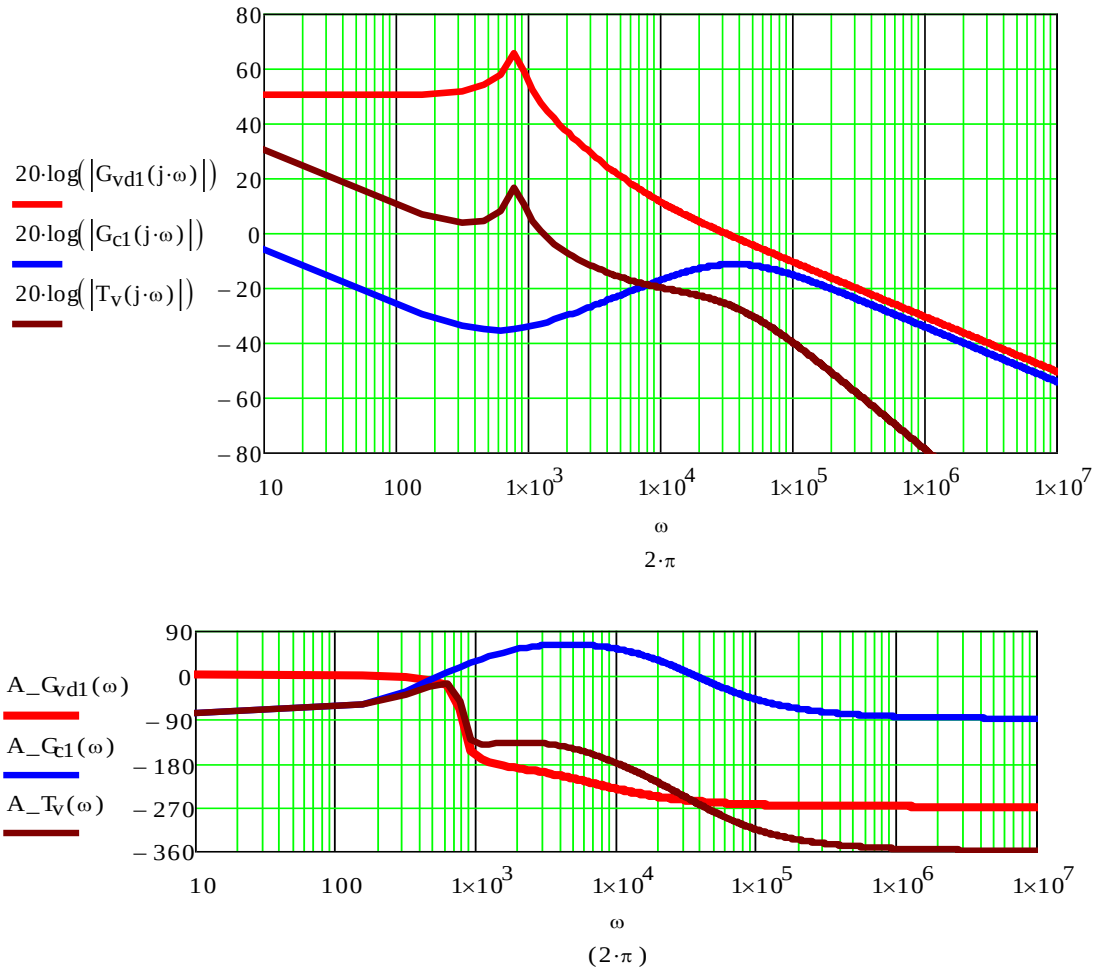

Fig. 3.6. Bode plots of the functions G_{vd1}(s), G_{c1}(s) and T_v(s) of the system

3.4. TIME-DOMAIN SIMULATION OF THE CLOSED LOOP SYSTEM

Closed-loop response of the system can be obtained when both the inner current control loop T_i(s) and outer voltage control loop T_v(s) are closed. The operating point around which the system is linearized is V_1=40 V, V_2=70 V, D_1=0.2, D_2=0.4, V_0=90 V and I_{s2}=9 A and R=10 Ω. The compensators G_{c1}(s) and G_{c2}(s) are also designed around the

same operating point of the system. Using the compensators, a time domain simulation of the system is carried out around the same operating point and the load is varied from 10 Ω to 5 Ω at t=0.015 s in order to test the stability and effectiveness of the system in meeting its control objectives. The results of the time domain simulation are shown in Figs. 3.7 3.8, and 3.9, respectively. It can be seen that output voltage V_0 remains constant at 90 V even during load variations and average switch current I_{s2} also remains constant at 9 A during load variations. The additional power requirements are met by the source 1 through changes in I_{s1}. Thus, the required control objective is effectively met through the independent control of the two loops and proper design of G_{c1}(s) and G_{c2}(s) compensators.

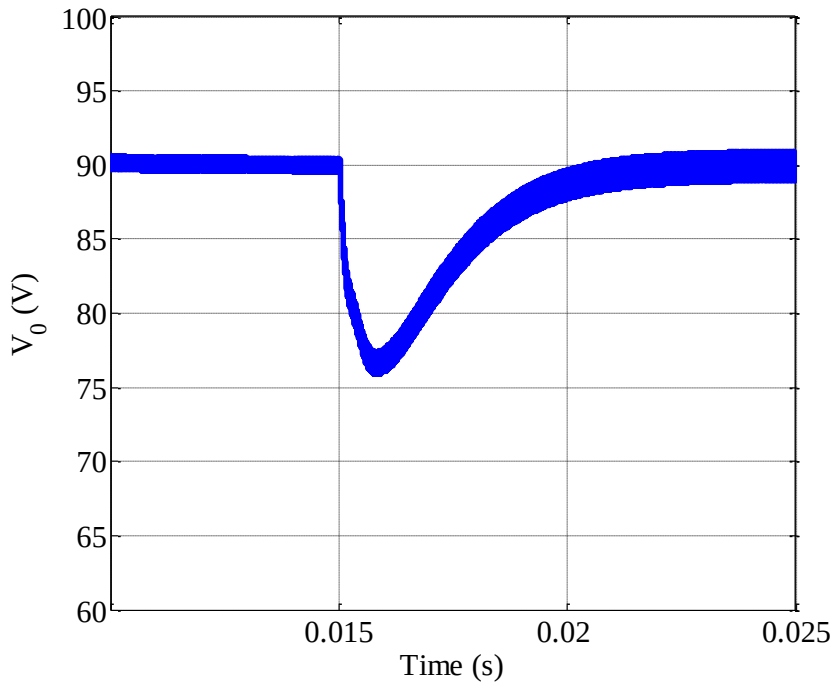

Fig. 3.7. Output voltage waveform for a step change in load from 10 to 5Ω at t=0.015s with the current and voltage loop closed with compensators $G_{c1}(s)$ and $G_{c2}(s)$

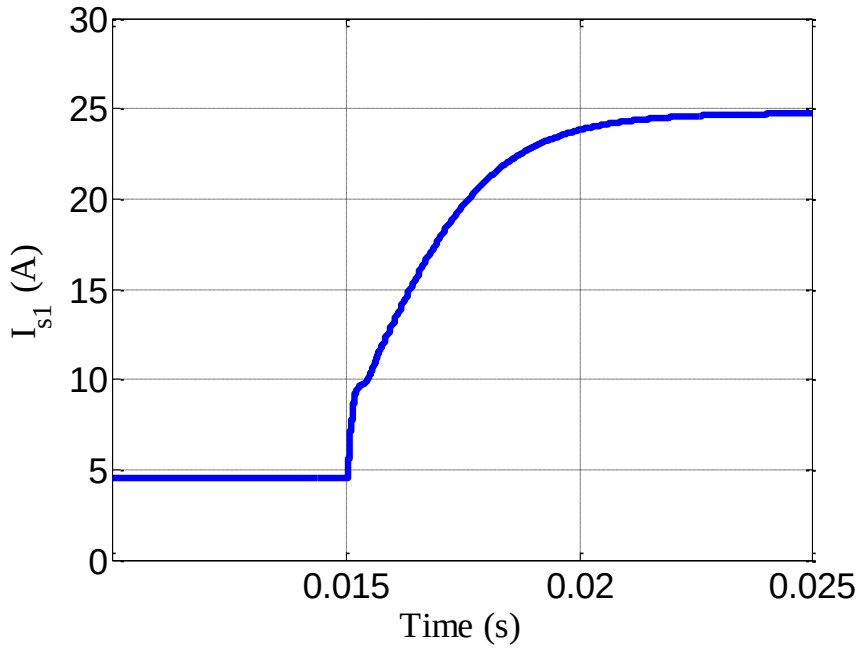

Fig. 3.8. Average current I_{S1} waveforms for a step change in load from 10 to 5Ω at t=0.015s with both loops closed

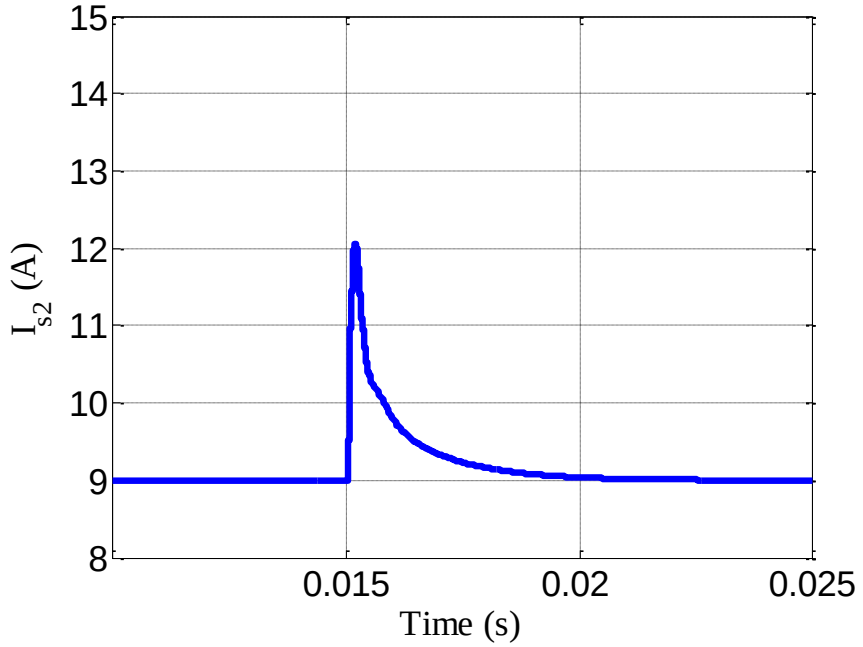

Fig. 3.9. Average current I_{s2} waveforms for a step change in load from 10 to 5Ω at t=0.015s with both loops closed

So far in this thesis, the DI buckboost converter has been controlled using only switch commands D_1 and D_2. In the next section, it will be proved that controlling the delay or offset time between switch commands D_1 and D_2 also helps in achieving the control objectives and improving the speed of response of the system.

4. OFFSET TIME CONTROL IN A DI BUCKBOOST CONVERTER

In Section 3, the closed loop control of the DI buckboost converter for the given control objectives was achieved through the independent control of control variables D_1 and D_2. In this section, it is analytically proven that the offset time $D_{12}T$ (see Fig. 4.1) or the delay between the switch commands can also be utilized as an additional control variable in the closed-loop control of the converter; the actual control variables being D_1 and D_2. In [45], a control strategy is proposed to minimize the inductor current ripple in a DI buck converter using D_{12}. Offset time control has been discussed and applied to a DI buckboost converter in [46].

In Fig. 4.1, the typical inductor current waveform for the converter is shown where D_1, D_2 are the ON time duty ratios of switches S_1 and S_2, respectively. D_{12}, D_{21} are the offset time duty ratios or the delay between the switch commands.

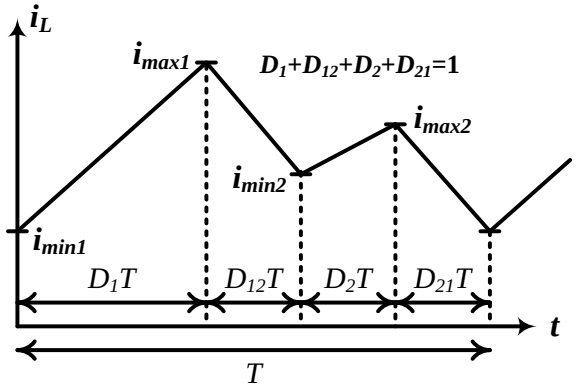

Fig. 4.1. Inductor current waveform in the steady state operation

Steady-state output voltage V_0 of the converter can be described as [9, 14]

$$V_0 = \frac{D_1 V_1}{(1 - D_1 - D_2)} + \frac{D_2 V_2}{(1 - D_1 - D_2)}. \tag{4.1}$$

Average inductor current I_L of the converter for a resistive load R is equal to [12]

$$I_L = \langle i_L \rangle = \frac{V_0}{R(1 - D_1 - D_2)}. \tag{4.2}$$

The ratio of average switch currents i_{s1} to i_{s2} is defined as α

$$\alpha = \frac{\langle i_{s1} \rangle}{\langle i_{s2} \rangle} \tag{4.3}$$

4.1. OFFSET TIME CONTROL SCHEME

In this section, the offset time control scheme is discussed. Alpha is proportional to the ratio of the currents drawn from sources V_1 and V_2 as shown in (4.3). The amount of power drawn from each source can thus be varied by varying α if V_1 and V_2 are constant. As it will be described, α itself can be controlled by adjusting the offset time or the delay between the switching commands ($D_{12}T$ or $D_{21}T$ in Fig. 4.1). Using the slopes of the inductor current, the minimum inductor current i_{min1} can be related to i_{max1} by (see Fig. 4.1)

$$i_{\min 1} = i_{\max 1} - \frac{V_1}{L} D_1 T. \tag{4.4}$$

Similarly, i_{min2} can be obtained from i_{max1} as

$$i_{\min 2} = i_{\max 1} - \frac{V_0}{L} D_{12} T. \tag{4.5}$$

And i_{max2} is related to i_{min2} by the following equation

$$i_{\max 2} = i_{\min 2} + \frac{V_2}{L} D_2 T \,. \tag{4.6}$$

Average switch currents $<i_{s1}>$ and $<i_{s2}>$ are given by the following equations:

$$\langle i_{s1} \rangle = (i_{\max 1} + i_{\min 1}) \frac{D_1}{2} \tag{4.7}$$

$$\langle i_{s2} \rangle = (i_{\max 2} + i_{\min 2}) \frac{D_2}{2} \tag{4.8}$$

From (4.5) and (4.6), it can be seen that inductor current values i_{max1} and i_{max2} are related to each other. From (4.5), it can also be observed that i_{min2} is dependent on offset time $D_{12}T$. From (4.8), it can be observed that the average value of the current supplied by V_2, i.e., $<i_{s2}>$ is dependent on i_{max2} and i_{min2} which are both in turn dependent on $D_{12}T$. Therefore, it can be concluded that by varying offset time $D_{12}T$ the average value of switch currents ($<i_{s1}>$ and $<i_{s2}>$) can be varied. Thus, the value of α can be varied by varying $D_{12}T$. By substituting (4.7) and (4.8) into (4.3) and by eliminating i_{min1}, i_{max2}, and i_{min2} using (4.4), (4.5), and (4.6), eq. (4.9) can be obtained.

$$i_{\max 1} = \frac{1}{2Lf} \frac{[2V_0 D_2 D_{12} - V_2 D_2^{\,2} - \frac{V_1 D_1^{\,2}}{\alpha}]}{[D_2 - \frac{D_1}{\alpha}]} \tag{4.9}$$

Average inductor current $\langle i_L \rangle$ can also be related to i_{max1} by calculating the area of the four trapezoids in Fig. 4.1. Using (4.4), (4.5), and (4.6) this procedure leads to

$$\langle i_L \rangle = i_{\max 1} - \frac{1}{2Lf}[D_1V_1 - D_2V_2 + D_1D_2(V_2 - V_1) + 2D_2(V_2 + V_0)D_{12}] \tag{4.10}$$

In (4.9), a relation for i_{max1} in terms of α and D_{12} is obtained; however, i_{max1} needs to be eliminated to find a relationship between D_{12} and α. This relationship can be obtained by combining (4.2), (4.9), and (4.10) to eliminate i_{max1}. The typical plot between α and D_{12} is shown in Fig. 4.2 where α_{min} and α_{max} give the range in which α can be varied for the given operating point of the converter which is determined by the value of D_1 (D_2 depends on D_1 in order to have a constant output voltage). As shown in Fig. 4.2, the relationship between α and D_{12} is almost linear and it can be observed that the ratio of power drawn from each of the sources can be varied by varying offset time duty ratio D_{12} of the converter.

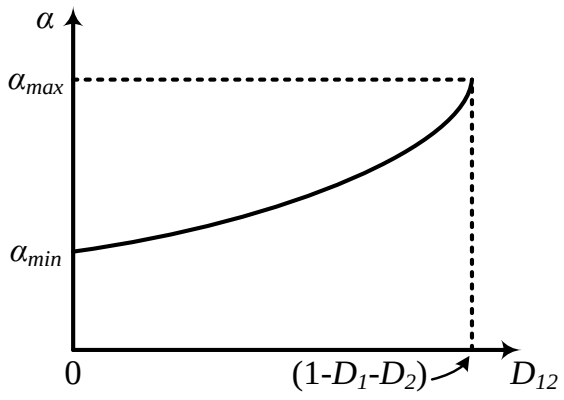

Fig. 4.2. Typical plot of α vs. D_{12}

4.2. CONTROL SCHEME REALIZATION

The offset time control scheme is implemented in two stages to control D_{12} as shown in Figs. 4.3 and 4.4. In the first stage (see Fig. 4.3) the outer loop is regulated for load regulation by maintaining output voltage V_0 constant through the control of D_1 through a voltage compensator. The average current of source 2 is held constant at I_{ref2} through the control of D_2 through a current compensator. The value of I_{ref2} is based on the energy management strategy and the control objective and is decided by an outer loop system-level controller. In this case, the control objective is to adjust the amount of power supplied by source 1 when the power from source 2 increases/decreases to meet the load demand while having output voltage regulation. In other words, when reference current I_{ref2} increases/decreases the average current of the other source (I_{s1}) has to decrease/increase accordingly to meet the load demand. For instance, in a battery/ultra-capacitor hybrid energy system the system-level controller has to decide upon an energy management strategy (i.e., choose a value for I_{ref2}) based on various factors like the battery SOC, ultra-capacitor SOC, and load demand. In this thesis, the value for I_{ref2} is being externally commanded without the use of any system-level controller.

The voltage and current compensators necessary (see Fig. 4.3) for the control of D_1 and D_2 have been designed in Section 3. Therefore, the offset time controller has all the required inputs of D_1, D_2, and I_{ref2} and it should be able to vary the offset time D_{12} between the switch commands. In Fig. 4.4, the offset time controller block diagram is shown. It can be realized by comparing the real value of α which is obtained at the end of each switching cycle to α_{ref} and integrating the error to obtain the offset time duty ratio (D_{12}). α_{ref} can be calculated as $<i_{s1}>/I_{ref2}$ as shown in Fig. 4.4 therefore, it must be noted

that the average switch current $<i_{s2}>$ is being controlled through control of D_2 and D_{12}, respectively. Finally, the PWM block (see Fig. 4.5) which has the offset time duty ratio (D_{12}) as an input generates the control pulses for switches S_1 and S_2 with a delay proportional to the offset time D_{12} between them.

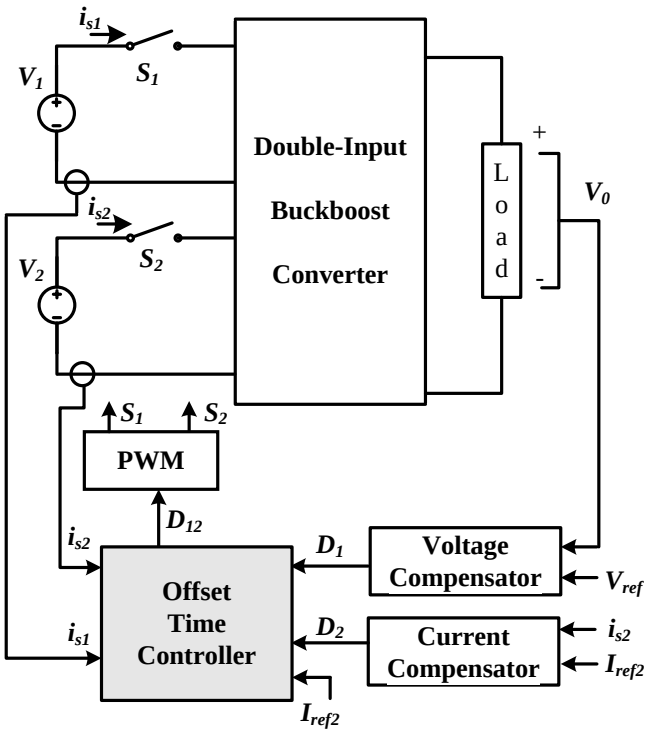

Fig. 4.3. Block diagram of the overall system

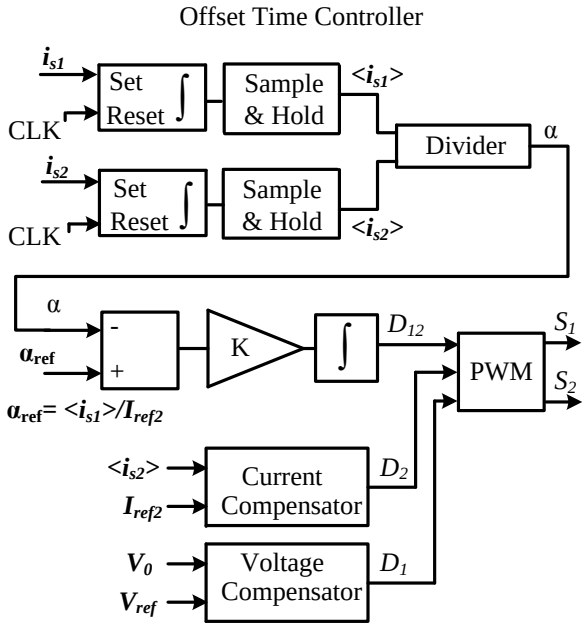

Fig. 4.4. Block diagram of the power sharing controller

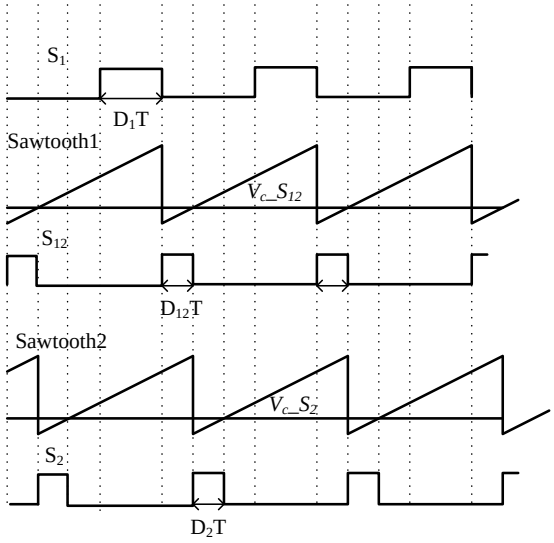

Fig. 4.5. Pulse width modulation block and delay D_{12} between S_1 and S_2

4.3. SIMULATION RESULTS FOR OPEN-LOOP RESPONSE

The DI buckboost converter with offset time controller was modeled in MATLAB Simulink. The overall system was simulated for the following input parameters V_1=40 V, V_2=70 V, V_0=90 V, f_s=50 kHz, L=50 µH for continuous conduction mode, and C=120 µF. Initially the steady-state relationship between α and D_{12} is plotted in Fig. 4.6 for 3 different values of D_1 (0.446, 0.323, 0.2). D_2 values are dependent on D_1 if it is assumed that the output voltage remains constant at 90 V. D_2 values can be found by substituting all other parameters in the steady state voltage transfer ratio given in (4.1).

From Fig. 4.6, it can be observed that the value of α increases almost linearly with an increase in D_{12} when D_1 and D_2 are kept constant. Therefore, it can be concluded that the ratio of the switch currents α can be controlled by controlling D_{12}. The range in which α can be varied depends on D_1 and D_2 as shown in Fig. 4.6. The average switch currents ($\langle i_{s1} \rangle$ and $\langle i_{s2} \rangle$)also change due to a change in D_{12}, D_1 and D_2 as shown in Fig. 4.7 in which the same set of D_1, and D_2 values used in Fig. 4.6 are used again. It can be observed from Fig. 4.7 that $\langle i_{s1} \rangle$ increases with an increase in D_{12} and $\langle i_{s2} \rangle$ decreases with an increase in D_{12}. Therefore, by increasing D_{12}, it is easier to increase average switch current 1 $\langle i_{s1} \rangle$ when average switch current 2 $\langle i_{s2} \rangle$ is decreasing since an increase in D_{12} also aids in decreasing $\langle i_{s2} \rangle$.

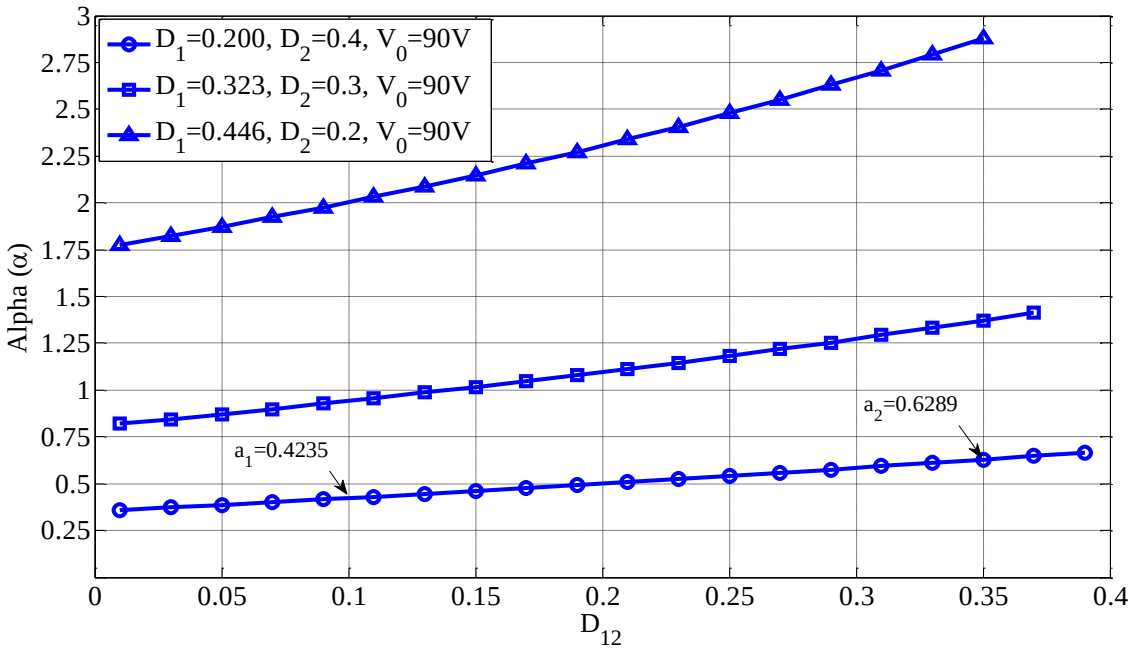

Fig. 4.6. Variations of α vs. D_{12}

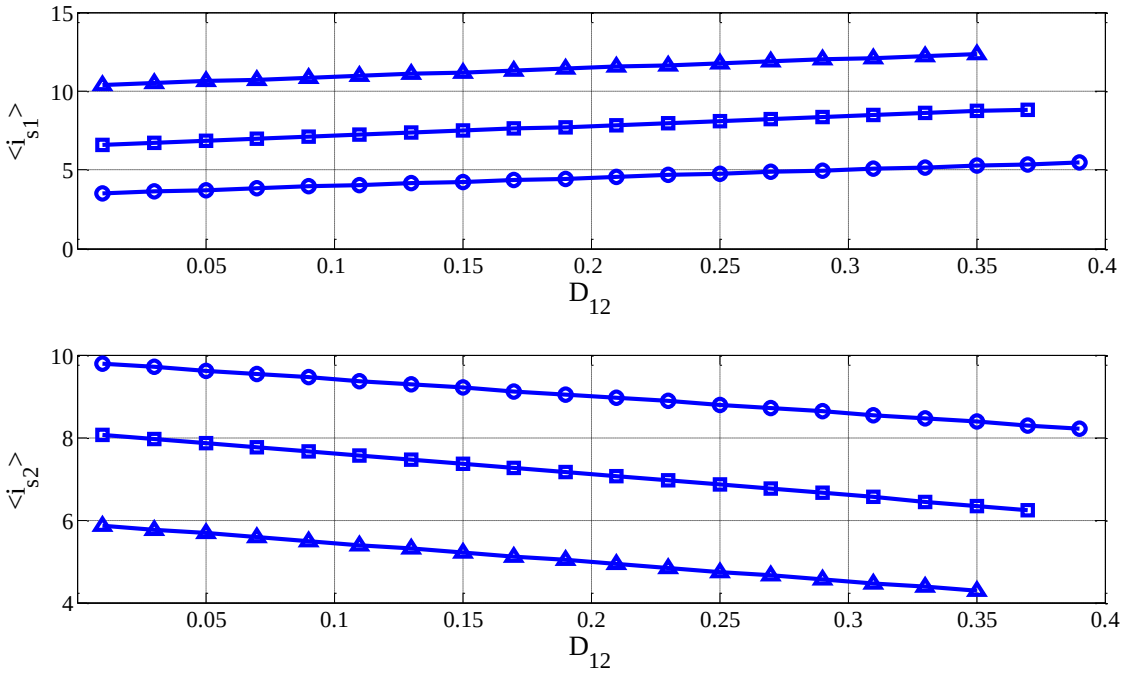

Fig. 4.7. Variations of $<i_{s1}>$ and $<i_{s2}>$ vs. D_{12} (refer to Fig. 4.6 for markers)

The system is then simulated to obtain an open-loop step response for α ,i.e., a step change in D_{12} from 0.10 to 0.35 occurs at t=0.015 s when D_1 and D_2 are kept constant at 0.2 and 0.4, respectively. The compensators for the current and the voltage loops are not included in the system. The value of α is expected to change from 0.4235 to 0.6289 (points a_1 and a_2, respectively) as predicted from the plot in Fig. 4.6. The step response of α for a step change in D_{12} is shown in Fig. 4.8 which indicates a very fast dynamics. The value of α changes almost instantaneously which indicates that the inner loop dynamics are very fast. Therefore, controlling the input currents through the control of the offset time would help in increasing the speed of response of the system.

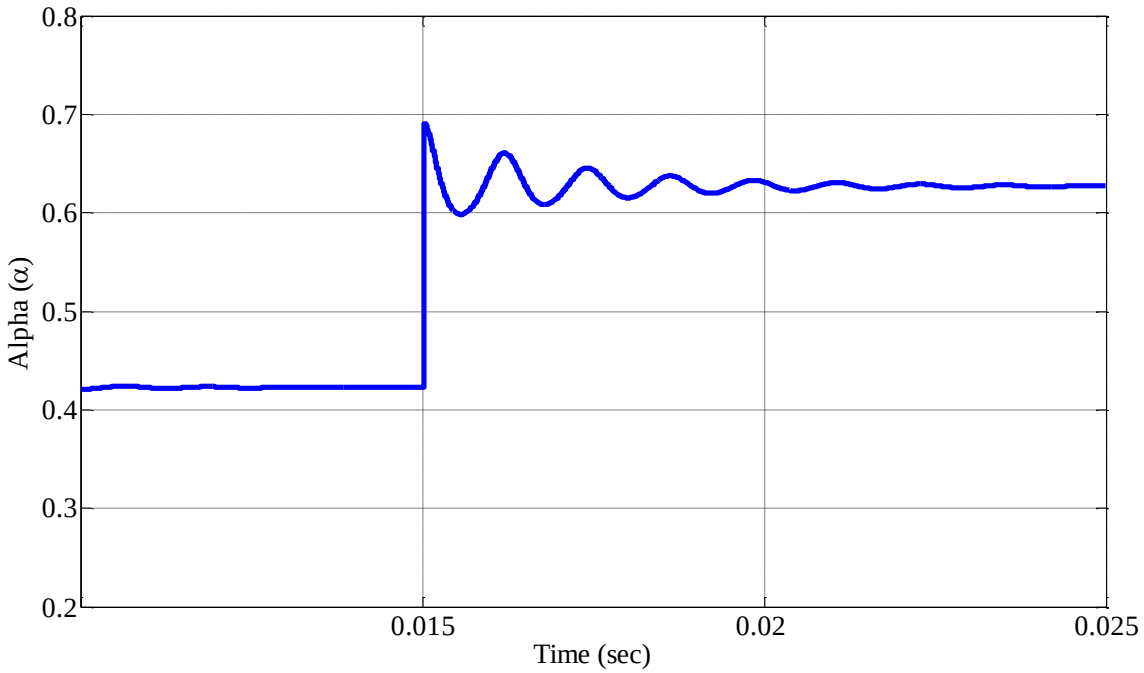

Fig. 4.8. Step response of α for a step change in D_{12} from 0.1 to 0.35

4.4. SMALL-SIGNAL ANALYSIS WITH OFFSET TIME CONTROL

In this section, the transfer functions are developed with the offset time control scheme included in the model. The average switch currents I_{s1} and I_{s2} can no longer be described by (2.10) and (2.11). The new more accurate average current equations which are obtained from the inductor current waveform shown in Fig. 4.1 are given by

$$I_{s1} = \frac{D_1}{2}(i_{\max 1} + i_{\min 1}) = \frac{D_1}{2}(2i_{\max 1} - \frac{V_1 D_1}{Lf}) \tag{4.11}$$

$$I_{s2} = \frac{D_2}{2}(i_{\max 2} + i_{\min 2}) = \frac{D_2}{2}(2i_{\max 1} - \frac{2V_0 D_{12}}{Lf} + \frac{V_2 D_2}{Lf}) \tag{4.12}$$

Perturbing average switch current I_{s1}, and the control variables D_1, D_2, and D_{12} in (4.11) gives

$$I_{s1} + \hat{i}_{s1}(s) = (D_1 + \hat{d}_1(s))(i_{\max 1} + \hat{i}_{\max 1}(s)) - \frac{V_1(D_1 + \hat{d}_1(s))^2}{2Lf} \tag{4.13}$$

It must be observed here that (4.11) seems to be a function of control variable D_1 only. However, i_{max1} is a function of D_1, D_2, and D_{12} as evident from (4.10). Therefore, it was perturbed in (4.13). Neglecting the product of perturbations and equating the steady state quantities on both sides (4.13) can be simplified to

$$\hat{i}_{s1}(s) = D_1 \hat{i}_{\max 1}(s) + [i_{\max 1} - \frac{2D_1 V_1}{2Lf}]\hat{d}_1(s) \tag{4.14}$$

where $\hat{i}_{\max 1}(s)$ is obtained by perturbing (4.10)

$$i_{\max 1} + \hat{i}_{\max 1}(s) = \langle i_L \rangle + \hat{i}_L(s) + \frac{1}{2Lf}[(D_1 + \hat{d}_1(s))V_1 - (D_2 + \hat{d}_2(s))V_2 + (D_1 + \hat{d}_1(s))(D_2 + \hat{d}_2(s))(V_2 - V_1) + 2(D_2 + \hat{d}_2(s))(V_2 + V_0)(D_{12} + \hat{d}_{12}(s))] \quad (4.15)$$

$$\hat{i}_{\max 1}(s) = \hat{i}_L(s) + \frac{[V_1 + D_2(V_2 - V_1)]}{2Lf}\hat{d}_1(s) + \frac{[2D_2(V_2 + V_0)]}{2Lf}\hat{d}_{12}(s) + \frac{[-V_2 + D_1(V_2 - V_1) + 2(V_2 + V_0)D_{12}]}{2Lf}\hat{d}_2(s) + \frac{2D_2D_{12}}{2Lf}\hat{v}_0(s) \quad (4.16)$$

substituting (4.16) in (4.14) leads to

$$\hat{i}_{s1}(s) = D_1\hat{i}_L(s) + F_{s1d1}\hat{d}_1(s) + F_{s1d2}\hat{d}_2(s) + F_{s1d12}\hat{d}_{12}(s) + \frac{D_1D_2D_{12}}{Lf}\hat{v}_o(s) \quad (4.17)$$

where

$$F_{s1d1} = D_1\frac{[V_1 + D_2(V_2 - V_1)]}{2Lf} + i_{\max 1} - \frac{2D_1V_1}{2Lf} \quad (4.18)$$

$$F_{s1d2} = D_1\frac{[-V_2 + D_1(V_2 - V_1) + 2D_{12}(V_2 + V_0)]}{2Lf} \quad (4.19)$$

$$F_{s1d12} = D_1\frac{[2D_2(V_2 + V_0)]}{2Lf} \quad (4.20)$$

Using similar analysis, average switch current I_{s2} in perturbed form is given by

$$\hat{i}_{s2}(s) = D_2\hat{i}_{\max 1}(s) + (i_{\max 1} + \frac{V_2D_2}{Lf} - \frac{V_0D_{12}}{Lf})\hat{d}_2(s) - \frac{V_0D_2}{Lf}\hat{d}_{12}(s) - \frac{D_2D_{12}}{Lf}\hat{v}_o(s) \quad (4.21)$$

Substituting (4.16) in (4.21) leads to

$$\hat{i}_{s2}(s) = D_2\hat{i}_L(s) + F_{s2\,d1}\hat{d}_1(s) + F_{s2d2}\hat{d}_2(s) + F_{s2d12}\hat{d}_{12}(s) + \frac{(D_2 - 1)D_2D_{12}}{Lf}\hat{v}_o(s) \tag{4.22}$$

where

$$F_{s2\,d1} = D_2\frac{[V_1 + D_2(V_2 - V_1)]}{2Lf} \tag{4.23}$$

$$F_{s2d2} = D_2\frac{[-V_2 + D_1(V_2 - V_1) + 2D_{12}(V_2 + V_0)]}{2Lf} + i_{\max 1} + \frac{V_2D_2}{Lf} - \frac{V_0D_{12}}{Lf} \tag{4.24}$$

$$F_{s2d12} = D_2\frac{[2D_2(V_2 + V_0)]}{2Lf} - \frac{V_0D_2}{Lf} \tag{4.25}$$

The new set of equations (4.17) and (4.22) for $\hat{i}_{s1}(s)$ and $\hat{i}_{s2}(s)$ lead to a new small-signal model which is shown in Fig. 4.9. It can be clearly observed from Fig. 4.9 that the switch current perturbations are functions of all the three control variables $\hat{d}_1(s)$, $\hat{d}_2(s)$, and $\hat{d}_{12}(s)$. It can also be observed that only the input side of the new small-signal model has changed when compared to the model without offset time control shown in Fig. 2.4 and the output side has remained the same. The $\hat{v}_o(s)$ terms shown in (4.17) and (4.22) are neglected in the model as the coefficients are negligible. Transfer functions G_{is1d1}(s) and G_{is2d2}(s) derived in Section 2 as (2.24) and (2.25) will change for the model with offset time control due to the changes in the input current dynamics in Fig. 4.9. The new transfer functions with offset time control included can be developed from the model shown in Fig. 4.9 and the procedure is described in the next section.

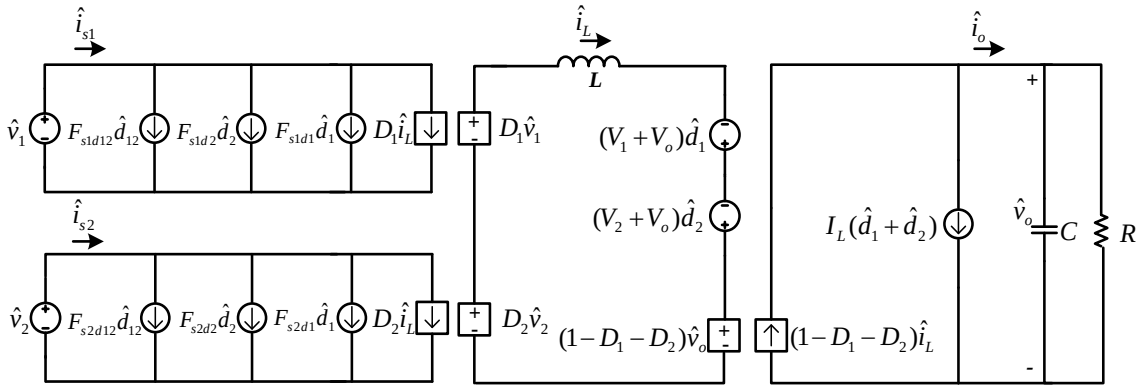

Fig. 4.9 Small-signal model of a DI buckboost converter with offset time control

4.5. TRANSFER FUNCTION DERIVATION WITH OFFSET TIME CONTROL INCLUDED

In this section, the derivation of transfer function G_{is1d1_offset}(s) is carried out which is the control-1 to switch current-1 transfer function when the offset time control is included. From Fig. 4.9 and (4.17)

$$\hat{i}_{s1}(s) = D_1\hat{i}_L(s) + F_{s1d1}\hat{d}_1(s) + F_{s1d2}\hat{d}_2(s) + F_{s1d12}\hat{d}_{12}(s) \tag{4.26}$$

In order to find transfer function G_{is1d1_offset}(s) one can assume $\hat{d}_2(s) = 0$ in (4.26) and the inductor current perturbations $\hat{i}_L(s)$ are converted into $\hat{d}_1(s)$ by using the control-1 to inductor current gain G_{id1}(s) derived earlier in Section 2 as (2.20). Furthermore, it is assumed that the offset time control loop is closed. Therefore, $\hat{d}_{12}(s)$ can be replaced with $\hat{\alpha}(s)$ by using Fig. 4.10 thereby simplifying (4.26) to

$$\hat{i}_{s1}(s) = D_1G_{id1}(s)\hat{d}_1(s) + F_{s1d1}\hat{d}_1(s) + \frac{F_{s1d12}G_{c3}(s)}{V_M}\hat{\alpha}(s) \tag{4.27}$$

From Fig. 4.10, it can be observed that $\hat{\alpha}(s)$ is also dependent on $\hat{d}_1(s)$ and this dependency is reduced by considering $\hat{d}_1(s)$ as the disturbance signal for the offset time control loop T_α(s), once the loop is closed. Then $\hat{\alpha}(s)$ can be written as shown in (4.28)

$$\hat{\alpha}(s) = \frac{T_\alpha(s)}{1+T_\alpha(s)}\hat{\alpha}_{ref}(s) + \frac{G_{\alpha d1}(s)}{1+T_\alpha(s)}\hat{d}_1(s) \tag{4.28}$$

It must be observed here that once the offset time control loop (T_α(s)) is closed then $\hat{\alpha}_{ref}(s) \approx 0$ and (4.27) changes to

$$\hat{i}_{s1}(s) = D_1 G_{id1}(s)\hat{d}_1(s) + F_{s1d1}\hat{d}_1(s) + F_{s1d12}\frac{G_{c3}(s)}{V_M}\frac{G_{\alpha d1}}{1+T_\alpha(s)}\hat{d}_1(s) \tag{4.29}$$

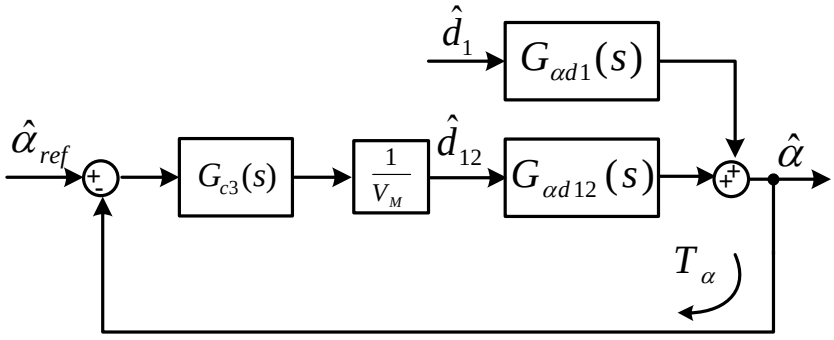

Fig. 4.10 Block diagram of the converter system with the inner offset time control loop closed

Now the transfer functions $G_{\alpha d12}$(s) and $G_{\alpha d1}$(s) need to be found in order to eliminate these terms from (4.29). These relationships can be found by considering that

the ratio $\alpha=I_{s1}/I_{s2}$ is controlled in offset time control. Therefore, the perturbations in $\hat{\alpha}(s)$ are given by

$$\begin{aligned} \alpha + \hat{\alpha}(s) &= \frac{I_{s1} + \hat{i}_{s1}(s)}{I_{s2} + \hat{i}_{s2}(s)} \\ \Rightarrow \hat{\alpha}(s) I_{s2} + \alpha \hat{i}_{s2}(s) &= \hat{i}_{s1}(s) \\ \Rightarrow \hat{\alpha}(s) &= \frac{\hat{i}_{s1}(s) - \alpha \hat{i}_{s2}(s)}{I_{s2}} \end{aligned} \tag{4.30}$$

In order to obtain transfer function $G_{\alpha d12}$(s), one can write $\hat{i}_{s1}(s)$ and $\hat{i}_{s2}(s)$ in terms of control variable $\hat{d}_{12}(s)$ using the relations F_{s1d12} and F_{s2d12} obtained earlier in (4.20) and (4.25) as

$$G_{\alpha d12}(s) = \frac{\hat{\alpha}(s)}{\hat{d}_{12}(s)} = \frac{F_{s1d12} - \alpha F_{s2d12}}{I_{s2}} \tag{4.31}$$

Using similar analysis one can also obtain the transfer function $G_{\alpha d1}$(s) as

$$G_{\alpha d1}(s) = \frac{\hat{\alpha}(s)}{\hat{d}_{1}(s)} = \frac{G_{is1d1}(s) - \alpha G_{is2d1}(s)}{I_{s2}} \tag{4.32}$$

Therefore, the new control-1 to switch current 1 function G_{is1d1_offset}(s) is obtained by substituting (4.31) and (4.32) in (4.29) leading to

$$G_{is1d1\_offset}(s) = \frac{\hat{i}_{s1}(s)}{\hat{d}_{1}(s)} = D_1 G_{id1}(s) + F_{s1d1} + F_{s1d12} \frac{G_{c3}(s)}{V_M} \frac{\dfrac{G_{is1d1}(s) - \alpha G_{is2d1}(s)}{I_{s2}}}{1 + T_{\alpha}(s)} \tag{4.33}$$

$$G_{c3}(s) = \frac{30000}{s} \tag{4.34}$$

The transfer function for $G_{is1d1\_offset}(s)$ obtained in (4.33) is compared with the original transfer function $G_{is1d1}(s)$ obtained in (2.20) using the compensator $G_{c3}(s)$ shown in (4.34) for offset time control loop and for the following operating point V_1=40 V, V_2=70 V, D_1=0.2, D_2=0.4, D_{12}=0.2, V_0=90 V, R=10 Ω, α=8/7, and I_{s2}=7 A. The bode plots for both the transfer functions $G_{is1d1}(s)$ and $G_{is1d1\_offset}(s)$ are shown in Fig. 4.11 in which the magnitude plots of both the transfer functions are nearly identical. However, the phase plots are slightly different and around the crossover region of $T_\alpha(s)$ loop, i.e., in the 1-5 kHz region, $G_{is1d1\_offset}(s)$ transfer function has better phase margin when compared to the $G_{is1d1}(s)$ function. This improvement in phase margin at the input side of the converter would help in improving the speed of response of the system with input current dynamics.

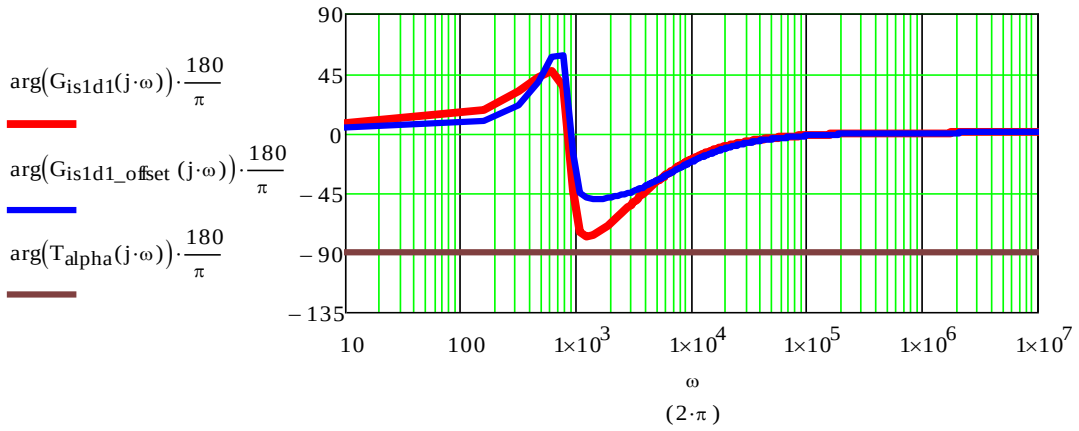

Fig. 4.11 Bode plots of the functions $G_{is1d1}(s)$, $G_{is1d1\_offset}(s)$ and $T_\alpha(s)$ of the system

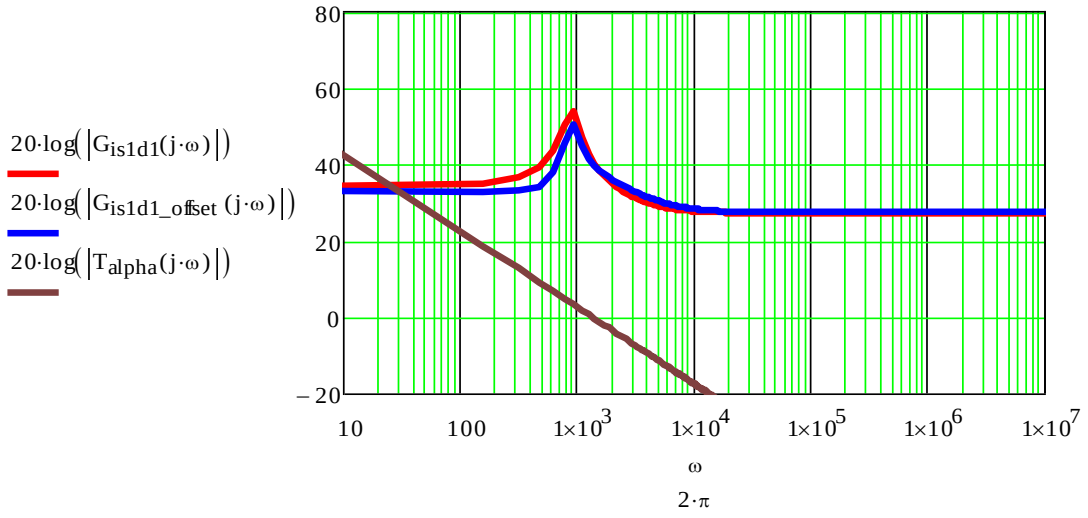

Fig. 4.11 Bode plots of the functions G_{is1d1}(s), $G_{is1d1\_offfset}$(s) and T_{α}(s) of the system (cont.)

4.6. SIMULATION RESULTS FOR CLOSED-LOOP RESPONSE

Closed-loop response of the system can be obtained when both the outer loops are closed. The same sets of compensators are used for controlling D_1, D_2, and D_{12}. For the sake of comparison, the results are obtained for two cases 1) without offset time control, i.e., only D_1 and D_2 are controlled and 2) with offset time control, i.e., D_1, D_2, and D_{12} are controlled. In both cases, a step change in the reference current of source 2, i.e., I_{ref2} takes place from 9 A to 7 A at t=0.015 s. The average current from source 1 ($<i_{s1}>$) is expected to increase in order to meet the constant load demand of R=10 Ω and the output voltage is expected to remain constant at 90 V. The voltage compensator G_{c1}(s) and current compensators G_{c2}(s) needed for controlling D_1 and D_2 have been designed in Section 3.

$$G_{c1}(s) = \frac{30}{s}\left(\frac{1+\frac{s}{2\pi*575.311}}{1+\frac{s}{2\pi*36780}}\right)^2$$
$$G_{c2}(s) = \frac{400}{s}\left(\frac{1+\frac{s}{2\pi*1.526*10^3}}{1+\frac{s}{2\pi*22.07*10^3}}\right) \quad (4.35)$$

The same compensators are used in this section to check the effectiveness of the offset time control scheme. Control variable D_{12} is controlled through the compensator G_{c3}(s) which is shown in (4.35). Output voltage V_0 and the average current waveforms of both the switches ($<i_{s1}>$ and $<i_{s2}>$) with and without offset time (D_{12}) control are shown in Figs. 4.12, 4.13 and 4.14, respectively. It can be clearly observed from Fig. 4.12 that the output voltage reaches the steady state value of 90 V much faster and has less overshoot when the offset time control is applied. It can also be observed from Figs. 4.13 and 4.14 that the average switch currents ($<i_{s1}>$ and $<i_{s2}>$) also settle to their new steady state values much faster when the offset time control scheme is applied. Therefore, offset time control scheme increases the speed of response of the system when the input currents of the DI buckboost converter are varying. This is very common in hybrid energy systems.

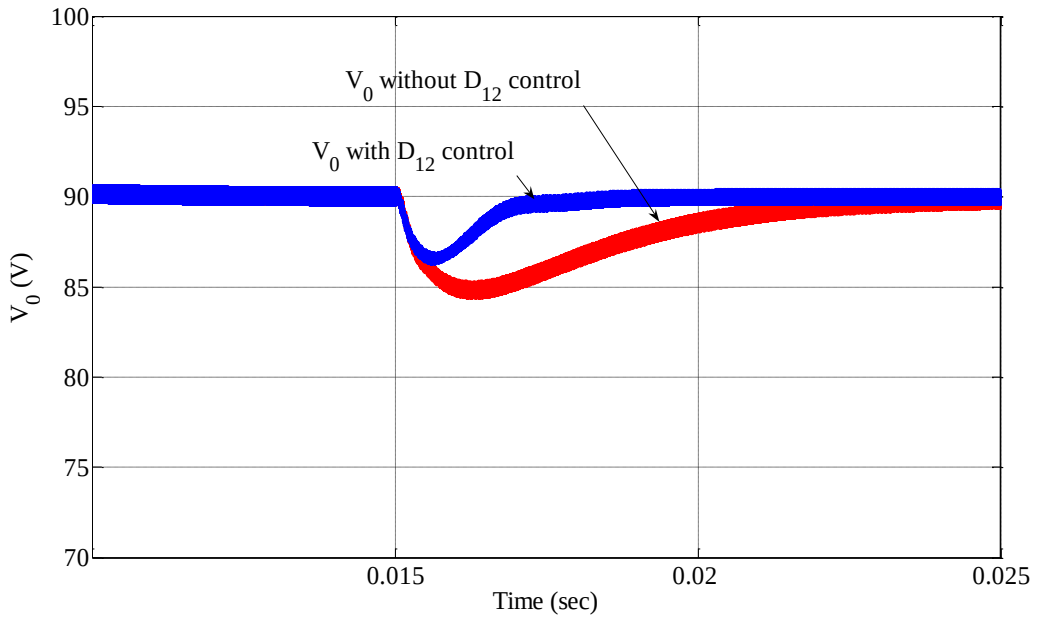

Fig. 4.12. Output voltage V_0 waveforms with and without D_{12} control for a step change in I_{ref2} from 9 to 7 A

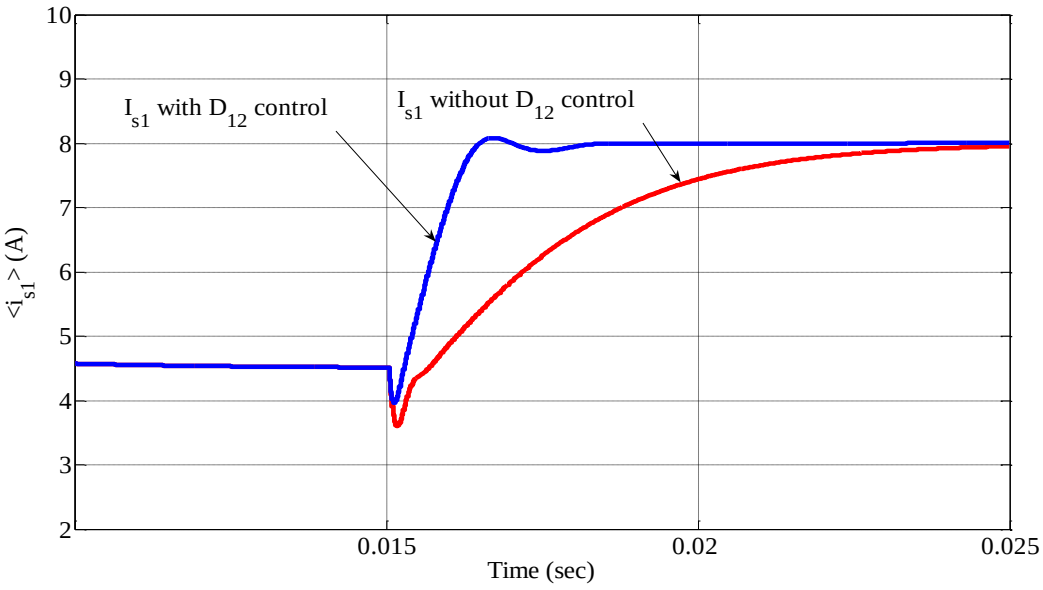

Fig. 4.13. Average current of source 1 $<i_{s1}>$ waveforms with and without D_{12} control for a step change in I_{ref2} from 9 to 7 A

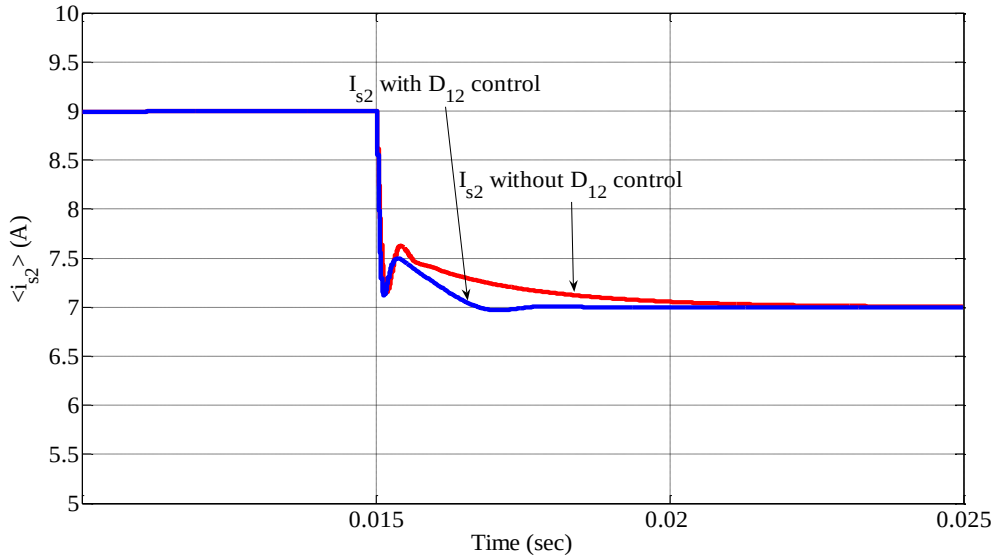

Fig. 4.14. Average current of source 2 $<i_{s2}>$ waveforms with and without D_{12} control for a step change in I_{ref2} from 9 to 7 A

4.7. CONCLUSION

Offset time control scheme is introduced and applied to a DI buckboost converter. It is theoretically proven that adjusting the offset time between the switch commands has a direct impact on the current drawn from each source. Offset time can be used as an additional control variable in systems with input current dynamics. Offset time control is very useful in situations like partial shading for a grid/solar combination or low ultra-capacitor SOC for a battery/ultra-capacitor combination where the average current supplied by the PV array or the ultra-capacitor is decreasing and the average current supplied by the other source has to increase to meet the load demand. In such situations, the ratio between the source currents is rapidly changing and controlling this ratio through a proportional control variable (offset time) would help in improving the dynamic performance of the system while the control objectives are achieved.

5. CONCLUSION

In this thesis, the control of DI buckboost converter is discussed. A small-signal model for the DI buckboost converter is developed and the compensator design is carried out for the system. Two compensators are designed to meet the control objective of supplying constant power from one source (PV) and meeting the additional load demand through the other source (battery) during load variations. It is analytically proven that the control objective can be achieved by independent control of the two loops controlling the two switches. This independent control of the two loops simplifies the compensator design procedure. Therefore, the compensators for the two loops are designed independently; one to maintain output voltage regulation and another to maintain switch current from source 2 constant. The closed-loop system is tested for load regulation using the designed compensators. The system is stable and has a good dynamic response. Apart from the small-signal modeling a new control method called the offset time control is also introduced and successfully applied to a DI buckboost converter in this thesis. The control scheme is based on adjusting the offset time between the switching commands which is proven to have a direct impact on the amount of current drawn from each input. This devised control method is fixed frequency and provides an extra degree of freedom in power sharing. The proposed control method has a very fast dynamic response, improves the stability of traditional controllers, and meets the control objectives better. The analysis can be extended to other DIPEC topologies which are used for the integration of various renewable energy sources.

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