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The design of a drum memory system

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DRUM MEMORY SYSTEM

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A

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ABSTRACT

Three methods for obtaining an auxiliary memory for an SCC-650 (Scientific Control Corporation) digital computer are presented. A logic design is then developed on the basis of using the drum and write circuits from an available IBM-650 digital computer and constructing the remaining logic functions. The results of the logic design are the transfer equations necessary to implement the memory system.

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I. INTRODUCTION

The University of Missouri at Rolla computer laboratory presently has a small general purpose digital computer, an SCC-650. This computer has a 4,096 word, 12 bit per word memory and a paper-tape input-output unit. The speed of the paper-tape unit is 10 characters per second.

The small size of the computer memory places a limitation on the size of program which can be executed quickly at any one time. Although additional random access memory banks can be purchased for the present computer, they are quite expensive, approaching $10,000 for each additional 4,096 words of storage. An additional memory, even though not of the random access type, would enhance the capabilities of the present machine. An additional feature of such an auxiliary memory would be to reduce the problem incurred by the use of a slow paper-tape reader. Blocks of frequently used information, programs or data, could be quickly loaded into the computer's main memory requiring only tenths of seconds as opposed to several minutes when the paper-tape reader is used.

Since the SCC-650 has a direct memory access (DMA) capability, it would be possible to load the computer memory directly and bypass the paper-tape reader. If some auxiliary memory were available to the computer through the DMA channel, large blocks of information could be quickly loaded into the SCC-650 memory. The DMA channel operates at a maximum rate of 5×10^5 read or write operations per second. Assuming the auxiliary memory could operate at a speed of 5×10^4 read or write operations per second, the entire SCC-650

memory could be loaded or emptied in less than 0.1 second, thus speeding up the loading process considerably.

An IBM-650 digital calculator, which utilizes a magnetic drum memory and vacuum tubes for active elements, is presently available for use as the above mentioned auxiliary memory. It is possible that all or part of the IBM-650 could be used as an auxiliary memory for the SCC-650 operating through the SCC-650's DMA channel.

Of course, the use of a magnetic drum as secondary or primary computer memory is not a new concept.[1,2] The purpose of this paper is to evaluate, specifically, the various methods available to mate the IBM-650 drum with the SCC-650 digital computer, and to produce a logic design of the approach which seems most desirable.

One possible solution would be to use as much of the present IBM-650 system as possible. This would require operation of the entire IBM-650 system, including the power supply. Access to the IBM-650 memory could be obtained through the present switch (manual input) register. This would require some interfacing between the IBM-650 and the SCC-650, including a conversion in number system since the IBM-650 represents numbers internally in the biquinary number system, while the SCC-650 utilizes the 2's complement binary number system.

A second approach would utilize only the drum and associated read-write heads from the present IBM-650 system. All required electronics, including head drivers and read circuits, would be built. Here, conversion of the drum from a two-out-of-five system

to straight binary would be required, this being primarily re-wiring.

The third and final approach to be considered would be to use the drum, read-write heads and write circuitry from the present IBM-650 system, while constructing the remaining required electronics. Other than the write circuitry, the second and third approaches are primarily the same.

II. APPROACH EVALUATION

The principal reason for considering the use of the entire IBM-650 system is the time and cost involved. Adapting this system to the SCC-650 would take the least amount of time and would involve the least expense of the three approaches to be examined. The primary task required here would be to build level and number system conversion units between the SCC-650 and the IBM-650 and to provide synchronization between the two computers.

There are, however, several major drawbacks to this approach. There is the fact that the IBM-650 system is a vacuum tube system which results in high maintenance requirements, primarily the replacement of vacuum tubes. Second, the IBM-650 system occupies two large cabinets of approximately 75 cubic feet each. It should be noted that both entire cabinets would have to be used. The circuitry necessary to the operation of the IBM-650 memory is scattered throughout both cabinets and therefore it would not be practical to condense the two cabinets into a smaller volume.

Probably, the biggest problem involved with the installation of this system would be removing the 12 kw of heat produced by the IBM-650, most of which is dissipated as filament power (approximately seven kw). In addition to the heat problem, the system produces a distracting noise level which results from the drum itself and the blowers within the computer required for cooling. However, the primary obstacle to this approach is the present non-functional condition of the computer. Several weeks were spent by the author in an attempt to place the IBM-650 in enough of an operational status to be able to use the memory alone. As a result of this work, it is

believed by the author that this task would have to be performed by someone with a technical knowledge of the IBM-650 system. Attempts by other University personnel in the past to place the IBM-650 in operating condition have also been unsuccessful.

The second approach suggested would be to use only the drum and the read-write heads from the IBM-650 system and to completely build the required electronics. An auxiliary memory system constructed in this manner would require very little space (approximately four cubic feet in addition to the drum itself) compared to the IBM-650 system. Also a considerable reduction in the amount of heat generated (approximately one kw in addition to a one-half horsepower motor required to drive the drum) would be realized. The reduced generated heat would also require less forced air cooling resulting in a reduction of the system noise level. It would be possible to insulate the drum acoustically from its surroundings, resulting in a further noise reduction.

On the negative side, the time and expense required in order to implement this system would be greater than if using the entire IBM-650 system. A major portion of the electronic parts cost would result from the solid-state design of the write circuits. The write heads presently used with the IBM-650 drum require a peak current of 300 ma for 1 μsec., which result in a 150 volt pulse[3] being applied to the transistor switch, if used in the configuration shown in Figure 1. Transistors which would withstand this voltage would cost on the order

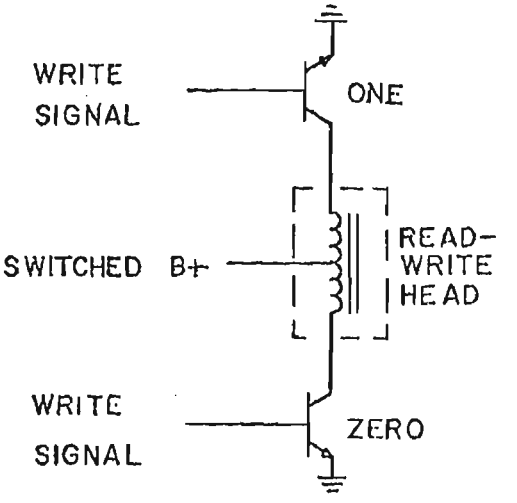

Figure 1. Example of a Transistor Write Circuit

of $7.00 each. Since the drum requires 400 write circuits, $2800 would be required for a single component type. This alone may be cause for taking yet a different approach.

The third possibility to be considered would be to use the present write circuits and drum from the IBM-650 and to construct the remaining required circuitry. This would alleviate the problem of using high voltage transistors in the write circuits. However, it would be necessary to provide a buffer between the solid state circuitry and the vacuum tube write circuits. A write power supply capable of providing 5 amperes at 250 volts would be required to provide power to the vacuum tube write circuits based on the assumptions on page 8. In addition, two other power supplies providing 2 amperes each at 70 volts and -63 volts would be required for biasing in order to eliminate major write circuit redesign.

Except for an increase in the power required and consequently the heat produced, the remaining comments which apply to the second

approach also apply to this approach.

At this point it should be mentioned that auxiliary memories, which will perform essentially the required tasks, are commercially available. One such source, Bryant Computer Products[4], has provided an estimate of $6500 on a drum and read-write circuits for 150,000 bits of storage. This would require the design and construction of control and interfacing networks. This system is also completely serial and would result in a reduction of write frequency from 5×10^4 operations per second to less than 2.5×10^3 operations per second. Additional verbal quotations from Control Data Corporation and from Scientific Control Corporation for $60,000 and $22,000 respectively have also been received. Although the last two estimates were for the smallest units these companies manufacture, the storage capacity of each was 16×10^5 bits and 2.64×10^4 bits respectively.

It is felt that a system constructed on the basis of the available IBM-650 drum would cost under $1,000 (Appendix C).

Because of the apparent inability to repair the present IBM-650 system, the first approach will no longer be considered, and a comparison will be made between the second and third approaches. Between the remaining choices, the primary factors to be considered are cost and maintenance. The maintenance required by the third approach is inherently greater because of some 200 vacuum tubes employed in the write circuits. However, the initial cost of the second approach is felt to be prohibitive at this time. Therefore, the third approach has been selected for the logic design.

It should be noted that if the parts cost of solid-state write circuits could be significantly reduced, the second approach would become practical. The logic design of the second and third approach would be quite similar.

III. LOGIC DESIGN

The assumptions for the logic design are as follows: 1) A DMA controller for the SCC-650 is available. This device is partially controllable by the SCC-650. The SCC-650 is able to specify the beginning address in the SCC-650 memory where information is to be placed or taken from by the DMA controller and the number of pieces of information to be transferred. A read or write cycle will also be specified by the SCC-650 through the DMA controller. Finally, certain timing information will be supplied by the DMA controller to the auxiliary memory. 2) The drum, read-write heads, and write circuits from the present IBM-650 system will be used with the least amount of modification possible. 3) The basic read-write concepts of the IBM-650 will be retained. Other methods[1] have been developed which allow tighter packing of information on the drum and yet retain high reliability in the readout from the drum. However, these methods require considerably more circuitry and more sophistication in their implementation. The present system, on the other hand, is quite simple and straight forward both in concept and in the circuitry required. 4) Data will be transferred from the SCC-650 to the auxiliary memory and from the auxiliary memory to the SCC-650 in 300 word blocks. Individual words within each block will not be addressable. It is felt that since access to the drum is inherently sequential, overall access time would be reduced by transferring blocks of programs, subroutines, or data. In addition, the amount of address decoding is drastically reduced by utilizing only 30 addressable locations as opposed to 9000 (30 addressable locations X 300 words per location = 9000 word capacity).

Certain information about the drum and its associated components must be ascertained before proceeding further.[5] The read-write head arrangement on the drum is as shown in Figure 2. Although corresponding heads of each row appear to be aligned, they are, in fact, slightly skewed so there is associated with each head a unique 600-bit track on the drum. Each of the five rows of heads correspond to a single bit position of the two-out-of-five code used in writing on the drum by the IBM-650. (The IBM-650 converts from biquinary in the machine proper to a two-out-of-five code for storage on the drum). In the present IBM-650 system, all of the zero-write circuits or all of the one-write circuits of each row are energized, depending on the particular decimal number to be written. However, only those circuits which are activated by a column selection circuit actually write. A column consists of one head from each row. Thus, five bits are written simultaneously. In the proposed memory system, 13-bit words (12 information bits plus a parity bit) will be processed. In order to write all 13 bits simultaneously, certain modifications to the write circuits will be necessary.

With reference to Figure 2, each row contains 40 heads, making a total of 200 available heads. This allows 15 groups of heads to write 13-bit words with five heads to be used as spares. Of the many configurations possible, the one shown in Figure 3 appears to require the least amount of write circuit modification. It should be noted that the selected grouping pattern repeats itself three times across the range of write heads, each group containing five 13-bit word patterns. Hereafter, a pattern refers to an arrangement of 13 write heads, five of which constitute a group.

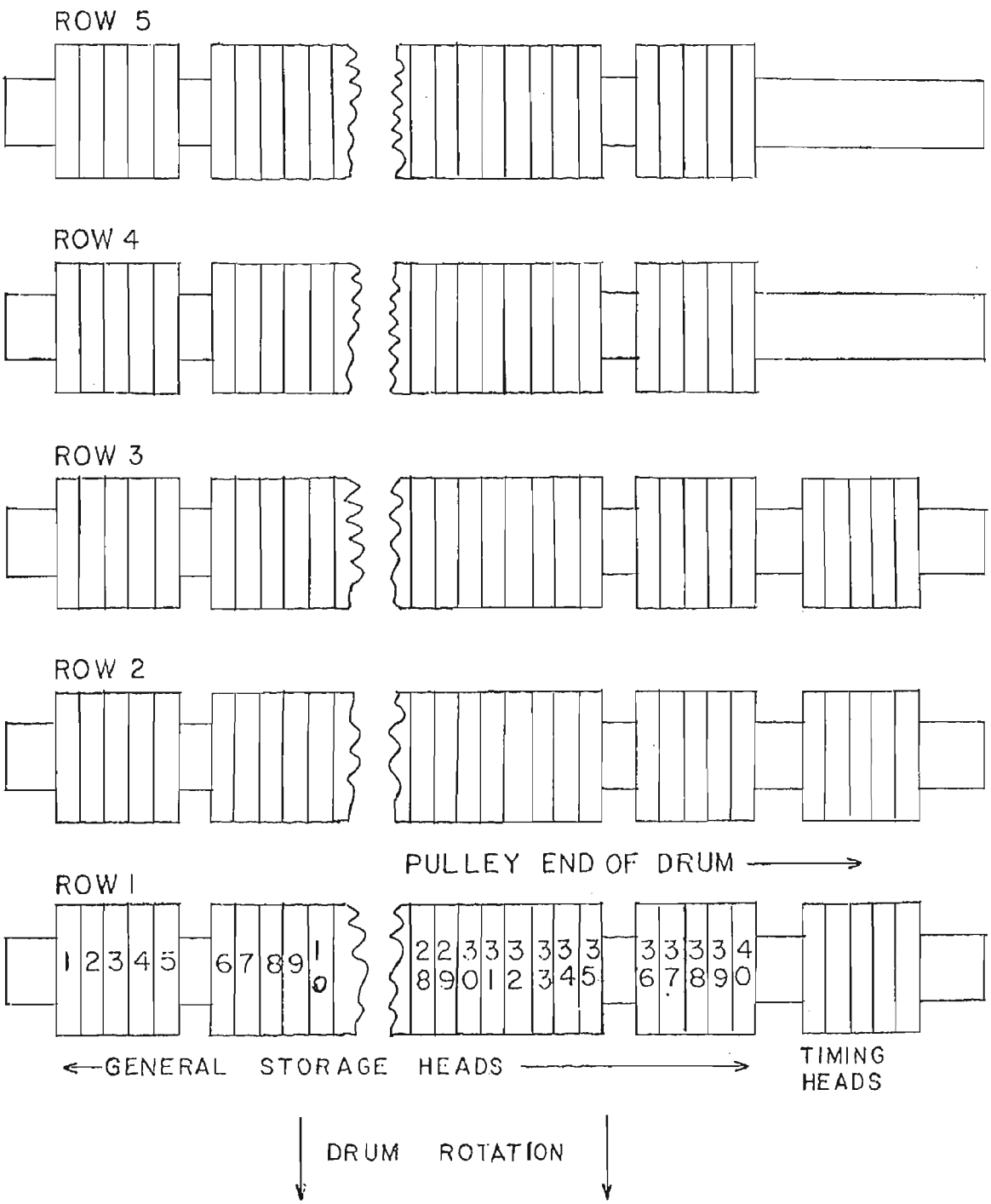

Figure 2. Drum Read-Write Head Arrangement

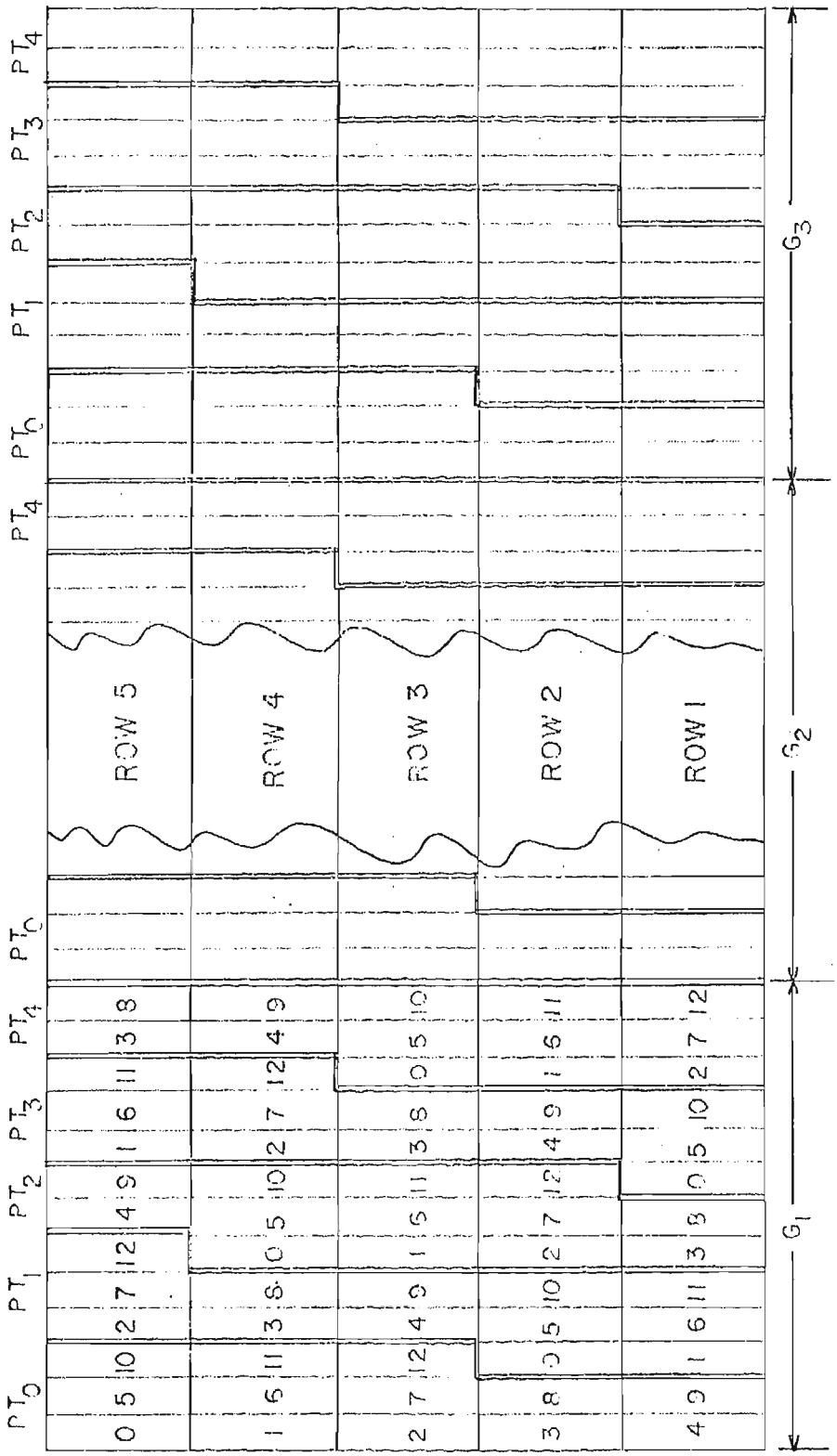

Figure 3. Group and Pattern Configuration

In order to place a 13-bit word on the drum, it must be known by which group and pattern the word is to be written.

Each write head is capable of writing in 600 separate bit positions around the periphery of the drum. Therefore, each block of 300 words, which will be written by the same set of heads, will take up one-half the circumference of the drum. Consequently, each set of 13 write heads will write on two sectors (one-half of the drum circumference). In order to completely specify a block location, it will be necessary to determine the sector, the group, and the pattern. To simplify the address decoding, each area (pattern, group, and sector) address will be decoded separately. Thus, a six-bit address register is required. The least significant bit will specify the sector, the two next least significant bits the group and the three most significant bits the pattern.

Since the SCC-650 has no way of directly addressing the auxiliary memory, the first word sent to the auxiliary memory will be used as the address of the location where information is to be stored. When the SCC-650 calls for information, it will also be necessary for the SCC-650 to first specify the auxiliary memory location of the stored information in the same manner as was used in storing the information.

In order to eliminate any decoding of the data to be written, each bit of every pattern is wired in parallel with the corresponding bit of all other patterns. Thus, all five-bits have the same value, one or zero, but only the five-bit of the chosen pattern and group actually write on the drum.

The auxiliary memory write sequence is described in the following paragraphs. Table I (in the notation of Bartee)[6] lists the registers and their definitions.

When it is desired to transfer information from the SCC-650 to the auxiliary memory, an instruction is executed by the SCC-650 to turn control of the SCC-650 memory over to the DMA controller. The first operation of the DMA controller is to call, from fixed locations in the SCC-650 memory in the order indicated, three words: a control word, a word indicating the number of words to be transferred in the block, and a word indicating the beginning location in the SCC-650 memory of the block of data to be transferred. A direct result of the transmission of the control word to the DMA controller is that the flip-flop Q, in the auxiliary memory is set which then initiates the series of transfers on page 18. The control word also specifies the mode of operation of the DMA controller. A single bit position indicates whether the transfer of that particular block will be chained to a subsequent block or will be a single block transfer. In the single block transfer mode, the DMA controller relinquishes control to the CPU at the end of the block. However, if a chained operation is indicated, the three SCC-650 memory locations immediately following the block of information to be transferred are interpreted as the three words to initiate yet another block transfer without turning control over to the CPU. The last block of a series of chained transfers is indicated by the control word associated with the last block.

TABLE I.

Register Definitions

$B = B_0, B_1, \ldots, B_{12}$*-

B_0 through B_{11} are data bits, B_{12} is a parity bit

$f_1(B) = B_{12} \oplus P(B)$**

$f_2(B) = B_9, B_{10}$

$f_3(B) = B_6, B_7, B_8$

$f_4(B)$ - is one when the parity check on register B fails

$L(B) = B_0, B_1, \ldots, B_{11}$

$P(B)$ - is one when there is an even number of ones in $L(B)$ and is zero otherwise

$DMO = DMO_0, DMO_1, \ldots, DMO_{11}$ - output data lines from the SCC-650

$DMI = DMI_0, DMI_1, \ldots, DMI_{11}$ - input data lines to the SCC-650

$DR = DR_0, DR_1, \ldots, DR_{12}$ - drum memory

$PT = PT_0, PT_1, PT_2$

$G = G_0, G_1$

$S = B_{11}$

$F = B_{11} \oplus SC$

$P = P_0, P_1$

Y, R, H, F, N, Q, Z, and SC are one-cell registers

*This notation defines B as a 13-cell register with cells numbered from left to right, zero through twelve.

**This notation indicates a dependent register as defined on page 19.

As a result of the control word in the DMA controller setting flip-flop Q to one, the first word, which is interpreted by the interface unit of the auxiliary memory as an address, is received by the auxiliary memory. Then the auxiliary memory prepares to receive the data by selecting the proper group, pattern, and sector. After a short delay, a ready signal (AK=1) is sent to the DMA controller indicating that the auxiliary memory is ready to receive the first data word on the next available SCC-650 memory cycle. Upon receiving the data word, the parity bit (B_{12}) is formed by combinational logic, the ready signal is raised (AK=0), and the auxiliary memory writes the previously received data word on the drum. The ready signal is again lowered (AK=1) and the request and write process is repeated until 299 data words have been transferred. Should the block contain less than 299 words, the process will be continued but no data will be received by the auxiliary memory. After completion of the data transfer, the auxiliary memory is reset and is again ready to execute another read or write cycle.

In order to implement the preceding sequence, certain timing information must be made available. This will be obtained both from the drum and from the SCC-650. Timing pulses available from the drum (Appendix A) are: 1) Home pulse (HP), one per revolution. This is the starting point on the drum to which all other timing is referenced. 2) Sector pulse (SP), two per revolution. This pulse indicates the start of each sector. One of these pulses is coincident with the HP. 3) Word pulses (AP and CP), 600 per revolution. These pulses mark the word position on the drum circumference. 4) Start and end of operation pulses (JP). These pulses are

used to indicate the start and end of a block-read and block-write operation. From the above pulses, the actual position of the drum with respect to the HP can be determined. Timing information can be placed on the drum, through the use of the present IBM-650, by the method outlined in Appendix B.

Two additional timing pulses from the SCC-650, t_0 and t_2 are also required. The t_0 pulse is used to initiate the actual transfers to and from the SCC-650. In order to insure that the address word is settled in the buffer register, B, a pulse t_2, which occurs 0.5 usec. after a t_0 pulse, is used to gate data from B to the other registers.

Figure 4 indicates the register interconnection necessary to select a particular group, pattern, and sector. After receiving the first word, the contents of the address register are decoded to perform this selection. The buffer register, B, holds each word as it is received from the SCC-650 until it is required either by the write circuits or the address register. The mod-four counter, P, which is incremented by JP_i and zeroed by SP, is used to locate the beginning and end of a block on the drum (Appendix A). The following are the transfer equations governing the operation of the counter, P. P is initially zero.

$$JP_1 \mid P + 1 \longrightarrow P$$

$$JP_2 \mid P + 1 \longrightarrow P$$

$$JP_3 \mid P + 1 \longrightarrow P$$

$$SP \mid 0 \longrightarrow P$$

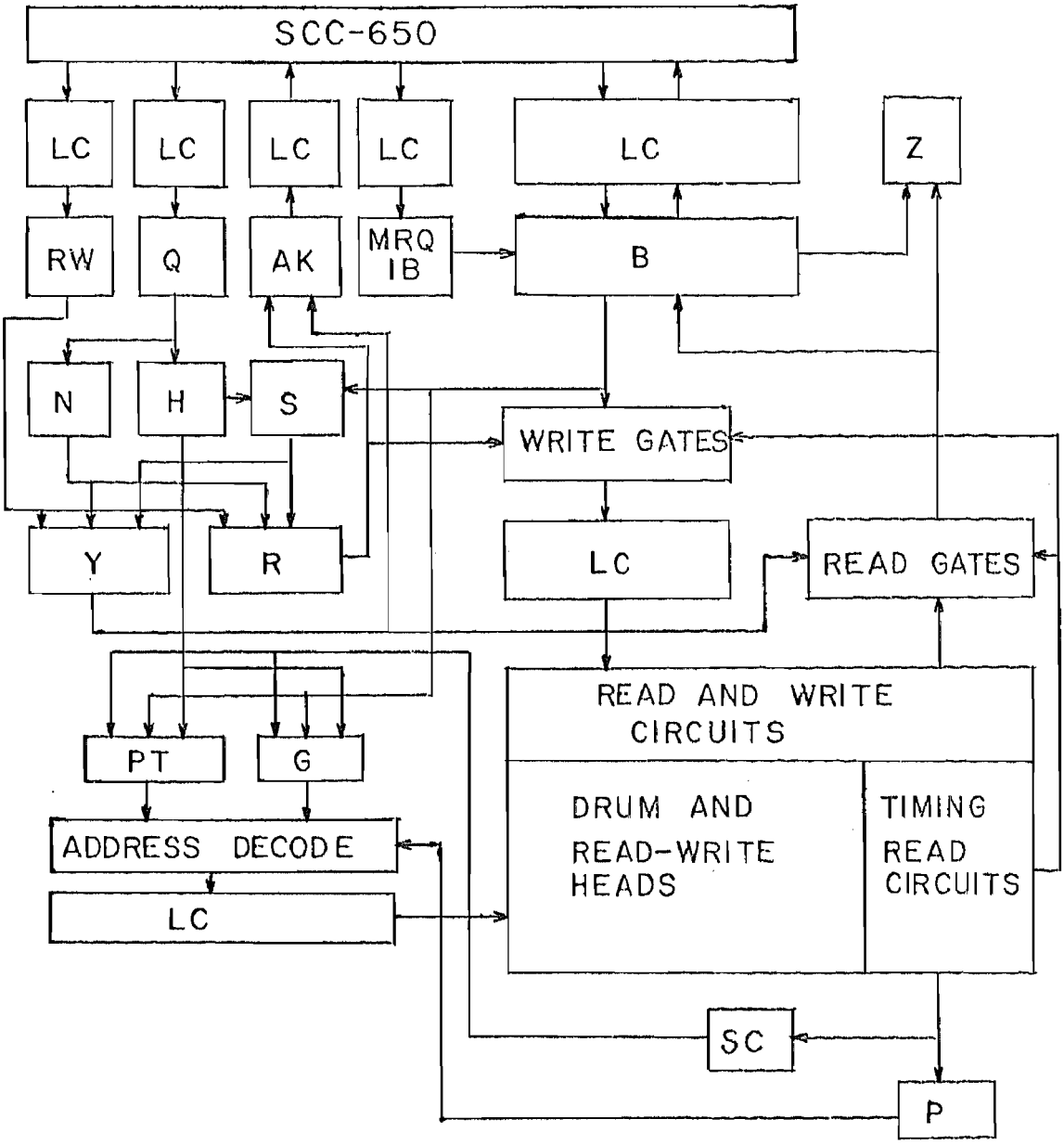

Figure 4. Register Structure for the Auxiliary Memory

The sector control flip-flop, SC, is set by the SP following the HP and reset by the HP.

To write information on the drum, the following control is needed: 1) A flip-flop, Q, which is set by the SCC-650 to enable the initial transfer of the address word into the auxiliary memory 2) A flip-flop, H, to indicate that the address word has been received and that a read or write cycle is about to begin 3) A flip-flop, N, to separate the transfer of the address word from the data words 4) A dependent register,[6] F, to insure that preparations for writing or reading are made just prior to the actual operation. A dependent register is a Boolean function of a register or registers and is generally realized with combinational networks. 5) A characteristic function,[6] p_i, of the counter P. A characteristic function, $\lambda_i(A)$ of a register, A, is one when the value of register A is i. 6) A flip-flop, R, to indicate that the transfer of data is about to begin 7) A ready flip-flop, AK, to indicate to the SCC-650 that the auxiliary memory is ready to accept a data word 8) A control line from the DMA controller, MRQ1B, to indicate when the DMA controller has acknowledged the auxiliary memory request for data[7] 9) A control line from the DMA controller, RW, (specified in the SCC literature as EXMRDWR) to indicate to the auxiliary memory whether a read or write operation is to take place.[7] Prior to a transfer sequence, registers, Q,N,H,R,S,PT,AK, and G are zero.

The auxiliary memory write transfer equations are as follows:

$$H \cdot t_0 \cdot Q \,|\, DMO \longrightarrow L(B)\ \ 1 \longrightarrow N,\ 1 \longrightarrow H$$

$$F \cdot N \cdot p_2 \cdot t_2 \,|\, 0 \longrightarrow N,\ B_{11} \longrightarrow S,\ f_2(B) \longrightarrow G,\ f_3(B) \longrightarrow PT$$

$RW \cdot F \cdot H \cdot SP \mid 1 \longrightarrow R$

$R \cdot AP \mid 0 \longrightarrow AK,\ 0 \longrightarrow B$

$R \cdot MRQ1B \cdot t_0 \mid DMO \longrightarrow L(B)\ 1 \longrightarrow AK$

$R \cdot CP \mid L(B) \longrightarrow L(DR),\ P(B) \longrightarrow DR_{12}$

$R \cdot AP \mid 0 \longrightarrow AK,\ 0 \longrightarrow B$

$\vdots$

$R \cdot AP \mid 0 \longrightarrow AK,\ 0 \longrightarrow B$

$MRQ1B \cdot t_0 \mid DMO \longrightarrow L(B)\ 1 \longrightarrow AK$

$R \cdot CP \mid L(B) \longrightarrow L(DR),\ P(B) \longrightarrow DR_{12}$

$R \cdot JP_3 \mid 0 \longrightarrow Q,\ 0 \longrightarrow H,\ 0 \longrightarrow R$
$\qquad\qquad\quad\ \ 0 \longrightarrow G,\ 0 \longrightarrow PT,\ 0 \longrightarrow S.$

The auxiliary memory read cycle is quite similar to the write cycle previously described. Down to the point where the reading is to take place, the operation of the DMA controller and the address selection circuits is identical with that of a write cycle.

The only additional timing required is a BP (B pulse) from the drum (Appendix A), which is required to clock the data from the drum into a temporary storage register.

The buffer register, B, holds the data as it is read from the drum until it can be accepted by the SCC-650. One additional flip-flop, Z, is used to indicate a parity check failure on the drum output data. Should this flip-flop become set, it must be manually reset.

The control required for a read sequence is the same as for a write sequence except that a control flip-flop, Y, is substituted for control flip-flop, R. The purpose of Y is to indicate that a

transfer of information from the auxiliary memory to the SCC-650 is about to begin.

In a read sequence, the setting of flip-flop Q, and the selection of the proper group, pattern, and sector is accomplished in the same manner as for a write sequence. Differences, however, become apparent at this point. As the appropriate sector comes under the read heads, the first data word is made available and is clocked into register B, where the word is temporarily stored. A memory cycle from the SCC-650 is then requested (AK=1). When the request is honored, the data is transferred from B into the SCC-650, and the request line is raised (AK=0). At this time, B is cleared and the next data word is made available. The sequence is repeated until 299 data words have been transferred. The auxiliary memory is then reset and is again ready to execute another read or write cycle.

The auxiliary memory read transfer equations are as follows:

$$H \cdot t_0 \cdot Q \,|\, DMO \longrightarrow B,\ 1 \longrightarrow N,\ 1 \longrightarrow H$$

$$F \cdot N \cdot p_2 \cdot t_2 \,\Big|\, \begin{array}{l} 0 \longrightarrow N,\ B_{11} \longrightarrow S, f_2(B) \longrightarrow G \\ f_3(B) \longrightarrow PT,\ 0 \longrightarrow B \end{array}$$

$$RW' \cdot F \cdot H \cdot Jp_1 \,|\, 1 \longrightarrow Y$$

$$Y \cdot BP \,|\, DR \longrightarrow M$$

$$Y \cdot CP \,|\, 0 \longrightarrow AK$$

$$Y \cdot MRQ1B \cdot t_0 \,\Big|\, \begin{array}{l} L(B) \longrightarrow DMI,\ 1 \longrightarrow B, 0 \longrightarrow B \\ Z' \cdot P_1(B) + Z \longrightarrow Z \end{array}$$

$$\vdots$$

$$Y \cdot BP \,|\, DR \longrightarrow B$$

$$Y \cdot CP \,|\, 0 \longrightarrow AK$$

$$Y \cdot MRQ1B \cdot t_0 \,|\, L(B) \longrightarrow DMI,\ 1 \longrightarrow AK,\ 0 \longrightarrow B,\ Z' \cdot P_1(B) + Z \longrightarrow Z$$

$$Y \cdot JP_1 \,|\, 0 \longrightarrow H,\ 0 \longrightarrow Y,\ 0 \longrightarrow G,\ 0 \longrightarrow PT,\ 0 \longrightarrow S,\ 0 \longrightarrow Q.$$

IV. ELECTRONIC AND MECHANICAL DESIGN

There are certain functions which must be electronically designed in order to physically implement the preceding logic design. One of these is the conversion from the solid-state levels of the address decoding circuits and the data lines to the levels required by the present vacuum tube write circuits. This function could probably be best implemented by vacuum tube circuits again in order to eliminate the requirement for expensive high voltage transistors.

Another level conversion required will be from the external SCC-650 levels (0 volts represents a logic 1 while +8 volts represents a logic 0)[7] to the levels of the auxiliary memory. This could be easily done with transistors.

The present read circuits should be replaced with transistor circuits, although the present read concept can be easily retained. A block diagram of the present circuit is shown in Figure 5.

Each block of Figures 6 and 7 represents a particular circuit function, each consisting of a single vacuum triode plus any necessary capacitors of a single vacuum triode plus any necessary capacitors and biasing resistors. The functions depicted are inverters, INXXX; cathode followers, CFXXX; and power drive circuit, PWXXX. There are presently five of the write circuits shown in Figure 6.[5] With the modifications shown in Figure 7, the addition of a second IN503 and an CF503,[5] this circuit can be made to write two of the 13 bits of a data word. Thus, three more circuits like that below line AA of Figure 7, would be required. The data line input to the circuit of Figure 7 would be the output of a level converter, which was mentioned previously.

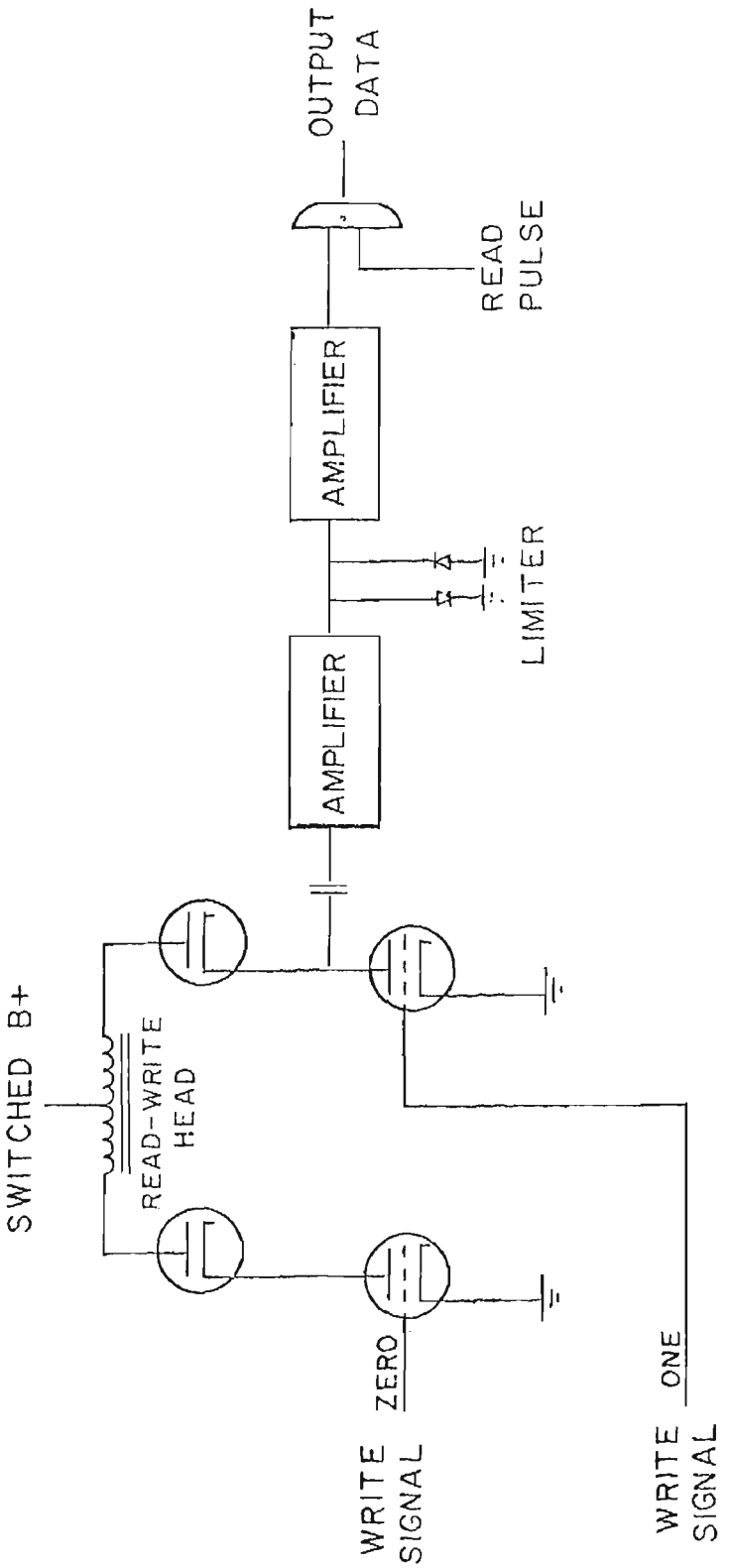

Figure 5. IBM-650 Read Circuit Diagram

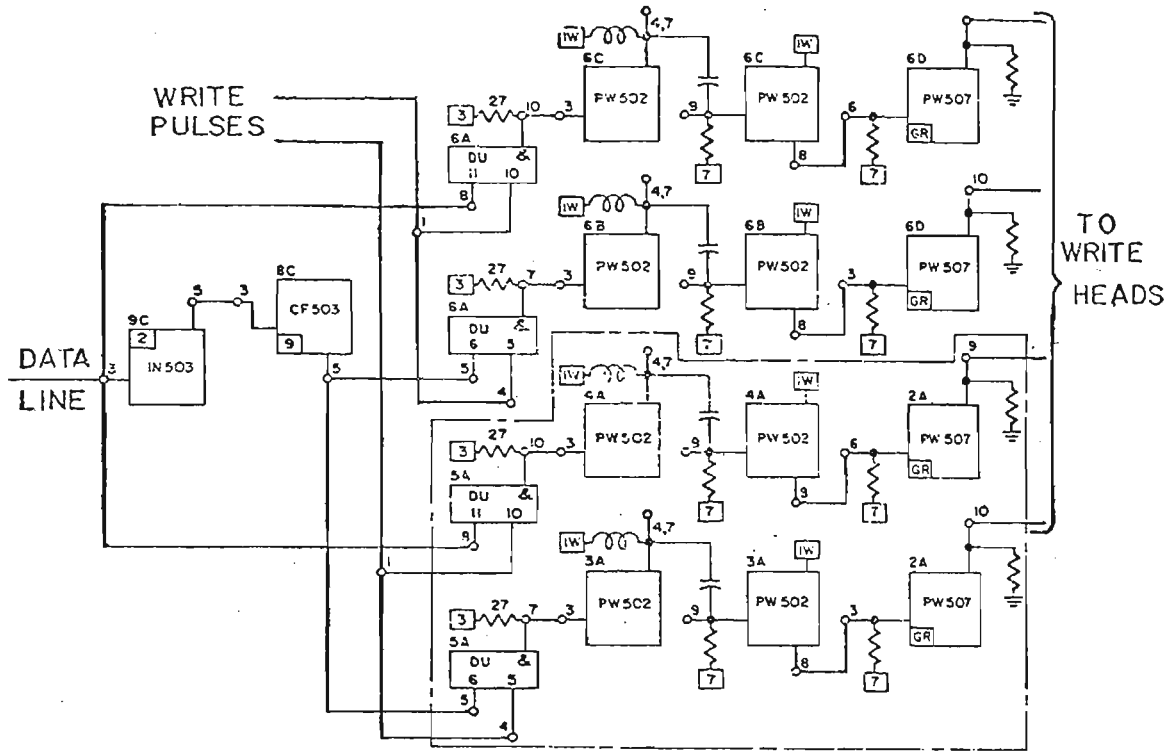

Figure 6. IBM-650 Write Circuit Diagram

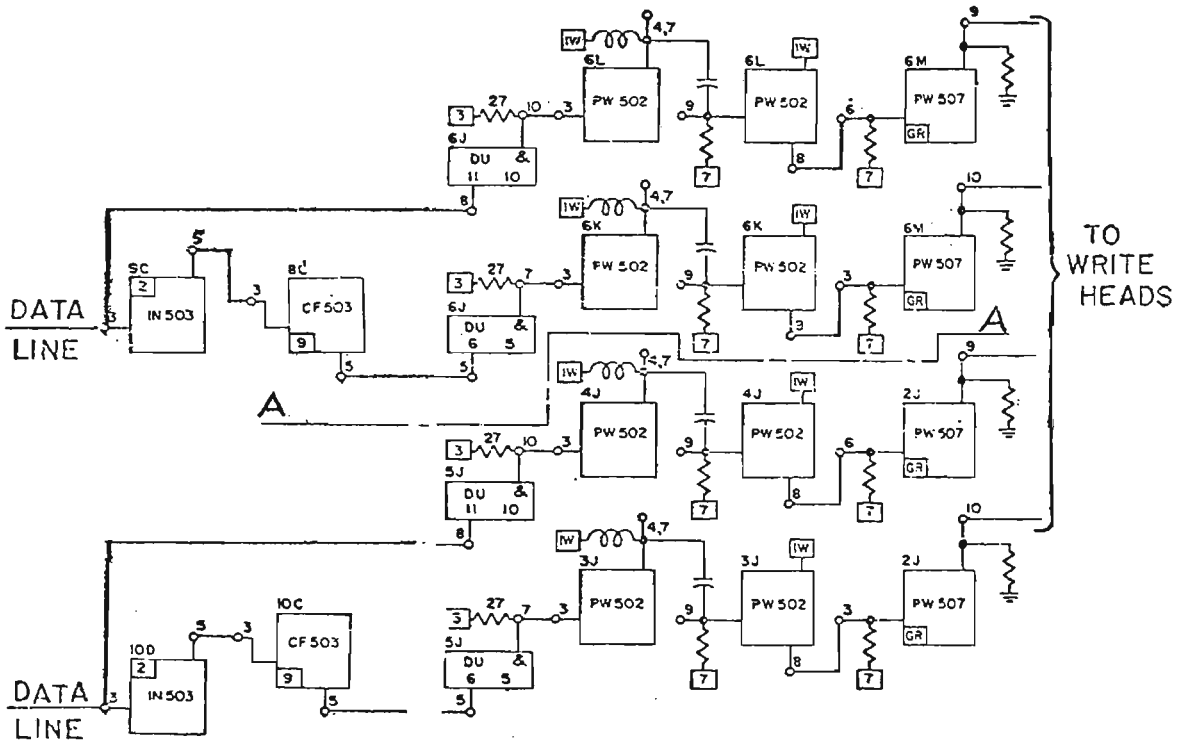

Figure 7. Suggested Write Circuit Diagram

In all cases, available parts, such as filament transformers, power supply transformers, filter capacitors, etc., should be used from the present IBM-650 system where possible.

Some mechanical features of the present IBM-650 system should be retained. The automatic oiler, which periodically provides an oil fog to the drum bearings should definitely be retained. Also a blower for forced air cooling of the write circuitry will be necessary.

The next effort in the realization of the described auxiliary memory should be to verify the operation of the drum in the simultaneous writing of 13 bits of information. It may be possible that adjacent heads cannot be used to write simultaneously without interaction. This matter could be easily remedied by separating the columns of a pattern. Before further time is spent on the actual design of the auxiliary memory, the detailed operation of the DMA controller should be verified. It is hoped that Scientific Control Corporation will be able to provide this presently unavailable information.

V. SUMMARY

Three methods for providing additional bulk storage for the SCC-650 digital computer through the use of the available IBM-650 system have been presented and evaluated. The primary basis for the chosen approach was cost.

The ensuing logic design was developed on the basis of an available DMA controller for the SCC-650 and resulted in the transfer equations necessary to implement the memory interface unit. Again, it should be noted that if the cost of solid-state write circuits could be lowered significantly, they should be incorporated.

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APPENDIX A

Timing Pulses Required from the IBM-650 Drum

Timing pulses are necessary to locate the different addressable areas of the drum and to place individual words on the drum. Those which must be available from the drum are the HP (home pulse), the SP (sector pulse), the AP (A pulse), the CP (C pulse), and the JP (J pulse).

The time relationship of these pulses is shown in Figure 8 and Figure 9, assuming the drum makes one revolution every 4.8 msec.

All of the pulses in Figure 8 and 9 are two μsec. wide except the BP which is one usec. wide. In addition, the BP need not specifically be generated from the drum, but can be derived from the trailing edge of an AP. The block diagram of a circuit which might be used to generate and shape the pulses is shown in Figure 10.

Timing presently available from the drum is located as follows.

HP	First head from pulley end - Row 2
AP	First head from pulley end - Row 1

An inverted signal from the AP track gives information for a CP. SP and JP are not presently on the drum in the manner specified.

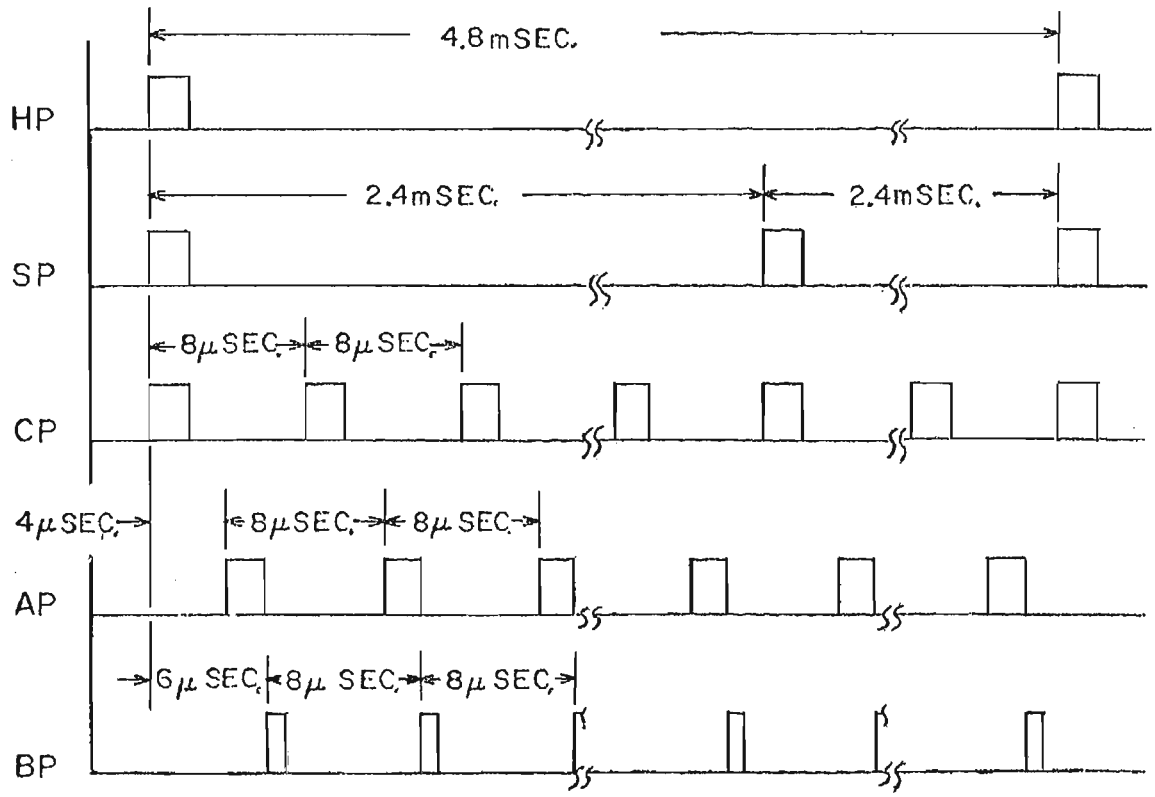


Figure 8. Time Relationship of AP, CP, SP, and HP

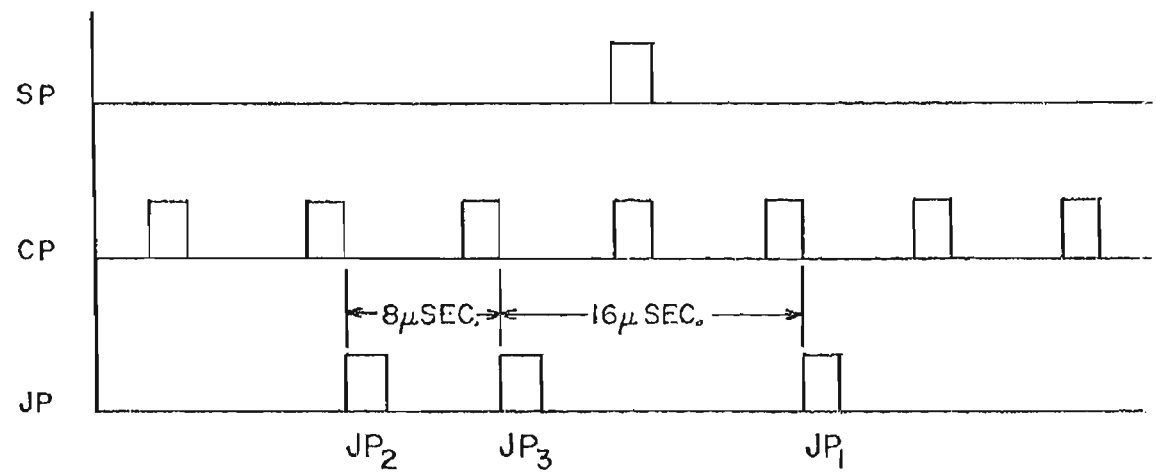


Figure 9. Time Relationship of CP, SP, and JP

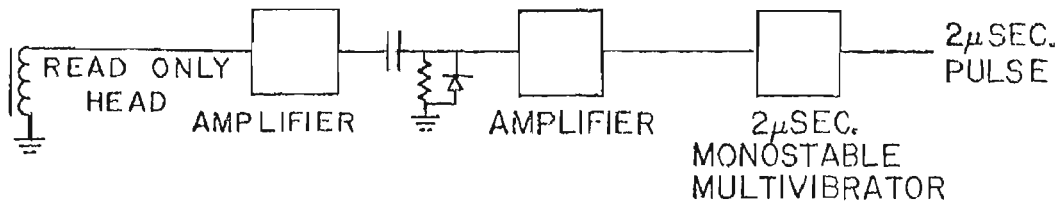


Figure 10. Suggested Timing Pulse Generation and Shaping Circuit

APPENDIX B

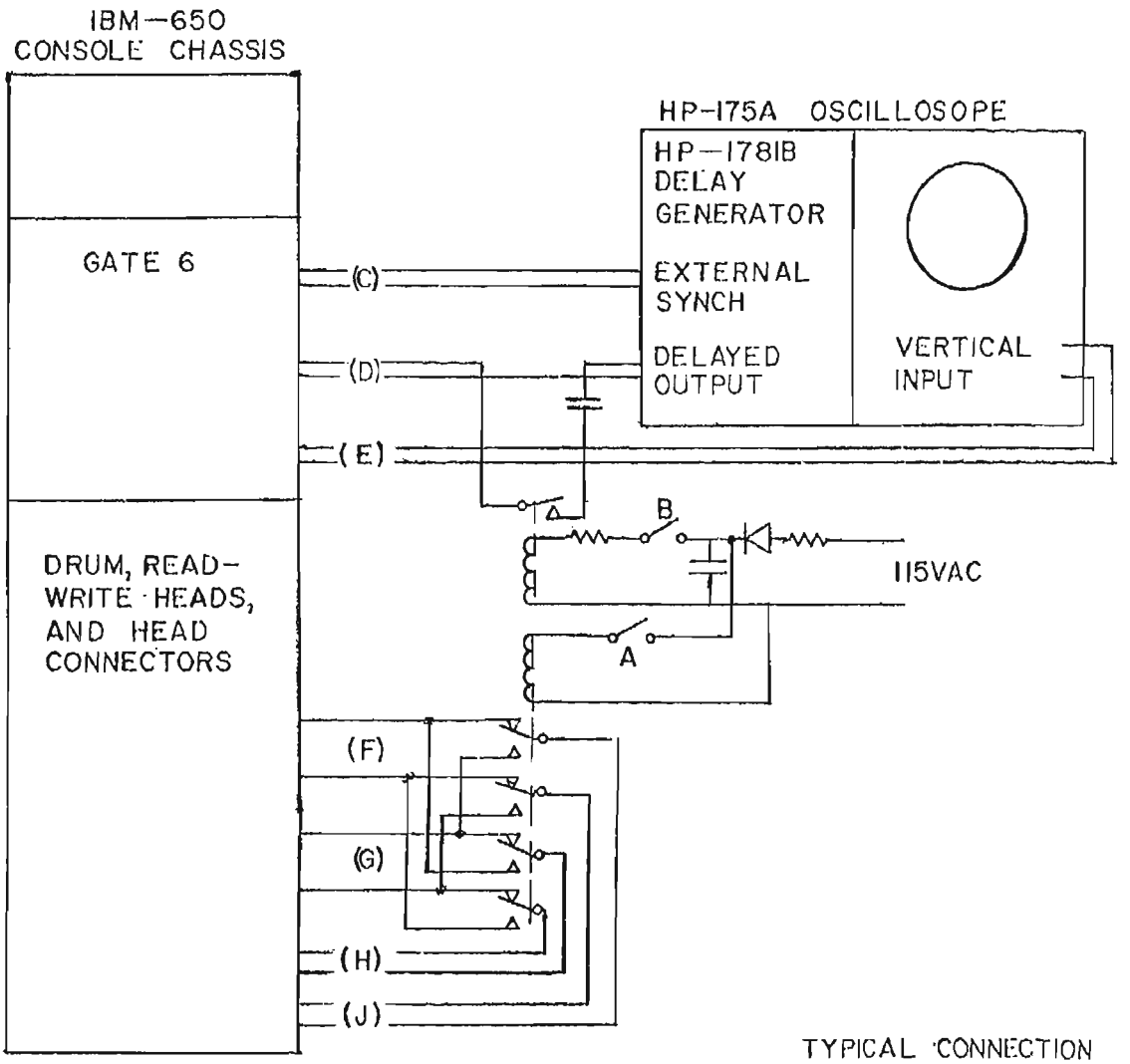
Method used in Placing Timing Information on the IBM-650 Drum

The connection of Figure 11 allows the observance of either the reference track or the track being generated. Pulses are placed on the track not being observed when switch B is closed. A counter is a valuable aid in accounting for the number of pulses already on the track.

In using the circuit shown in Figure 11, a position on the drum can be found with respect to either the reference track or the HP. The reference track can be observed by depressing switch A. Various positions on the drum are found by varying the amount of delay generated by the delayed sweep generator of the oscilloscope. The delayed sweep output pulse from the delayed sweep generator is used as the writing pulse. The actual writing on the generated track is performed by depressing switch A and then switch B. Switch B must then be released before switch A or writing will be performed on the reference track.

It should be noted that the writing circuits used in this appendix are not the same as described in the body of this paper. A block diagram of these circuits can be found in Reference 5, page II-63.

Before any of the present timing tracks are modified, it is strongly advised that some experimentation be performed in order to become familiar with the above described process.



		TYPICAL CONNECTION POINTS
SCOPE SYNCH PULSE	(C)	7Q-8 AND GROUND
INPUT TO BUFFER STORAGE WRITE CIRCUIT	(D)	5B-9 AND GROUND
OUTPUT FROM READ ONLY CIRCUIT	(E)	4U-8 AND GROUND
HEAD OF TRACK TO BE GENERATED	(F)	PINS 1 AND 2
HEAD OF REFERENCE TRACK	(G)	PINS 1 AND 2
OUTPUT FROM BUFFER STORAGE WRITE CIRCUIT	(H)	JACKS 4 AND 5
INPUT TO READ ONLY CIRCUIT	(J)	11V-3 AND GROUND

Figure 11. Circuits Used to Place Timing Information on the IBM-650 Drum

APPENDIX C

Estimated Parts Cost to Implement the Logic Design for the Auxiliary Memory

The following list is an estimate of the parts cost to implement the logic design presented in the body of this paper. The cost of the logic functions is placed at $1.00 per card based on logic cards presently available in the Electrical Engineering Department of the University of Missouri at Rolla. Power supply and level converter costs are based on using such parts as transformers, vacuum tubes, etc., from the present IBM-650 system. Those parts marked with an (*) are available from the Computer Control Corporation, Inc., Framingham, Massachusetts.

ITEM	COST
*Mounting rack, CCC P/N BL-33, 2 each	$480.00
Logic cards, 35 each	35.00
Logic power supply, 1 each	50.00
Write circuit power supply, 1 each	100.00
Remounting of drum, write circuits, blowers, and automatic oiler	80.00
Level converters	100.00
Cabinet	35.00
*Jumper lead set, CCC P/N JL-10, 1 each	40.00
Connectors	20.00
GRAND TOTAL	$940.00

VITA

The author was born on August 4, 1938, in Cainsville, Missouri. He received his primary education in Republic, Missouri and his secondary education in Baltimore, Maryland. He subsequently received a Bachelor of Science degree in May 1960, from the University of Missouri at Rolla, in Rolla, Missouri.

Since receiving his undergraduate education, he has been employed by the Sperry Phoenix Company, as a full-time engineer and by the U.S. Army as a 2nd Lieutenant. Since September of 1964, he has been employed by the University of Missouri at Rolla as a full-time instructor in Electrical Engineering while concurrently enrolled in the Graduate School of the same institution.