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Microcontroller-based multiple-input multiple-output transmitter systems

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MICROCONTROLLER – BASED MULTIPLE-INPUT MULTIPLE-OUTPUT TRANSMITTER SYSTEMS

by

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ABSTRACT

Multiple-Input Multiple-Output (MIMO) Systems use multiple antennas at both the transmitter and receiver to increase data throughput and/or system reliability. An MIMO transmitter can be implemented using a variety of approaches. This work describes some of the approaches that can be used to generate the transmitted waveforms, and discusses the features and limitations of each. In particular, it shows how a microcontroller-based system can be used for applications which require low power consumption. This thesis also describes the high-level design of a microcontroller-based MIMO transmitter. The computational speed of the microcontroller, as compared to Field-programmable Gate Array (FPGA) and Digital Signal Processors (DSP), coupled with other additional tasks which it may need to handle limit the transmitted data-rate. However, this low power and low cost design may make it attractive for some applications.

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1. INTRODUCTION

Wireless communication is a process of transferring information over a short distance or over long distances based on the kind of application. Recent technological advances in the field have allowed a wide variety of services such as 2G, 3G and LTE (Long Term Evolution) [1].

Two of the challenges wireless technologies frequently face include interference and fading [2]. These issues introduce errors into transmitted signals which reduce the throughput of the system.

Multiple-Input Multiple-Output (MIMO) technology has an ability to improve the throughput and bit-error rate of the system. A MIMO transmitter can be designed using various approaches based on the technical specification of the application. This work discusses the features and limitations of these approaches, lists some of the technical specifications of the application which are: low power dissipation and low cost, selects one of the approaches based on the above requirements, and gives a brief description of the high-level design of the implementation. The FPGA, DSP and the microcontroller are the different approaches taken into consideration and discussed in detail.

Recent developments in field-programmable devices have improved the process of hardware designing. Their ability to provide high data rates and high throughput has made them attractive for many DSP applications. However, the large power consumption of the FPGAs makes them ineffective for the selected application. DSP processors have been known for fulfilling fast operational needs of many signal processing applications, but their higher-power consumption as compared to a microcontroller make them unsuitable for this application. The advancements in the field of DSP have made manufacturers equip a general-purpose microcontroller with additional DSP-based features. The low power dissipation, low-cost and the ability to perform additional tasks using interrupts make the microcontroller one of the apt choices for this application. This work places further emphasis on the microcontroller-based approach and discusses its high-level designing in Section 6.

With reference to the data rates, it is found that the typical data rates offered by FPGAs can be as high as 480 Mbits/sec (i.e., 8bits x 60MHz), while some of the programmable logic designs are capable enough to support even higher data rates [3][4]. The data rates are very high compared to the ones produced by typical microcontrollers and DSP processors. But the total power consumption for an FPGA is found to be too high. The dynamic power consumption for certain FPGA designs like Virtex-4 and Stratix-II can be found to be about 6 Watts and 8 Watts, respectively. Thus, the FPGAs can be used in an application involving high data rates and conceding the total power consumption. Section 5 describes in detail the dynamic power consumption of FPGAs mentioned above.

Section 1 gives an overview of the research. Section 2 provides details on many concepts used in this work. Section 3 discusses the system architecture for a typical communication channel in detail. Section 4 illustrates an in-depth analysis of different approaches that can be used to design a MIMO transmitter system and section 5 discusses the dynamic power consumption of FPGAs. Section 6 provides the technical specification for the selected application and selects one of the earlier discussed approaches based on their features and limitations. Section 7 discusses the high-level block diagram for the selected approach and the last section summarizes the work.

2. BACKGROUND

This section provides a brief description of the background required for an effective understanding of this research work.

2.1 TYPICAL COMMUNICATION CHANNEL

A typical communication channel can be illustrated by Figure 2.1.

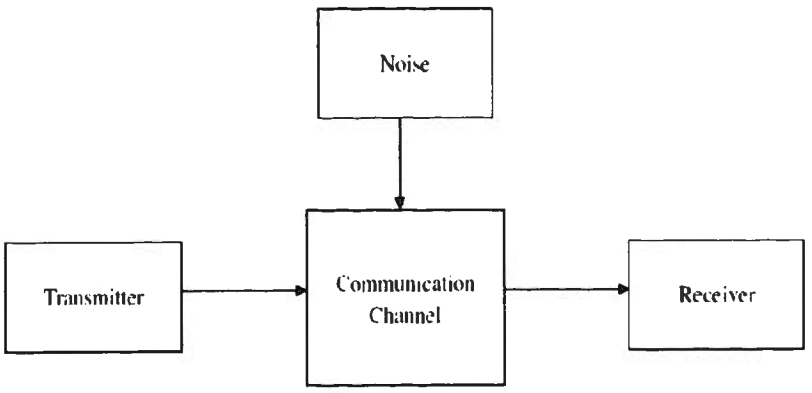


Figure 2.1 A Typical Communication System

It is clear that a typical communication system is made up of the following functional blocks:

i. Transmitter: It is an electronic device that is used to produce message signals which are transmitted using antennas

ii. Communication Channel: The channel through which the produced data is transmitted

iii. Noise: An unwanted effect that gets added to a message signal

iv. Receiver: The electronic device which is used to receive and process signals which have been captured by the receiving antenna

Noise is one of the important parameters that is always taken into consideration while designing any communication system. It often introduces error in the transmitted message signal. But certain error detection and error correction mechanisms can be used to improve the reliability of the demodulated data.

Error detection schemes like checksum algorithms, parity bits, cyclic redundancy checks (CRC's) etc. can be used. Methods such as automatic repeat request (ARQ), forward-error correction (FEC) and hybrid schemes (combination of ARQ and forward error correction) have been used for error correction [5].

2.2 ANTENNA CONFIGURATIONS

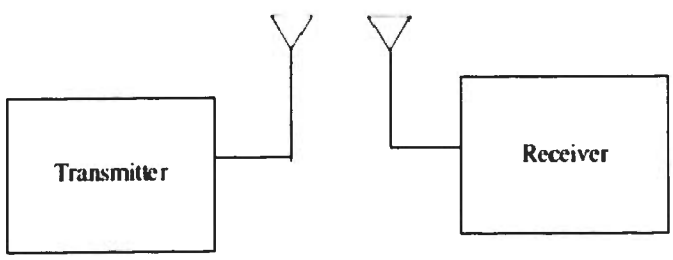
Communication systems can be implemented using a variety of antenna configurations at both the transmitter and the receiver. Some of the different configurations that can be used in a communication system are shown in Figure 2.2.

These set-ups can be explained as follows:

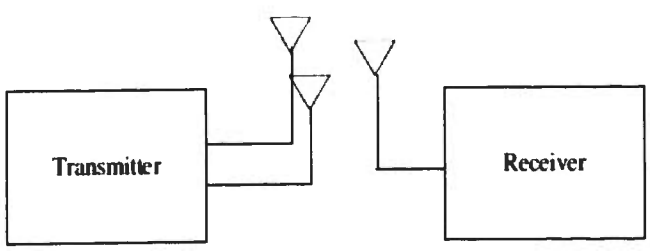
a) SISO is an acronym for Single-Input Single-Output system which simply stands for single transmitters at the transmitter and receiver ends.

b) MISO stands for the set-up that uses multiple antennas at the transmitter and only a single receiving antenna.

c) SIMO stands for the set-up that uses single antenna at the transmitting and multiple antennas at the receiving end.

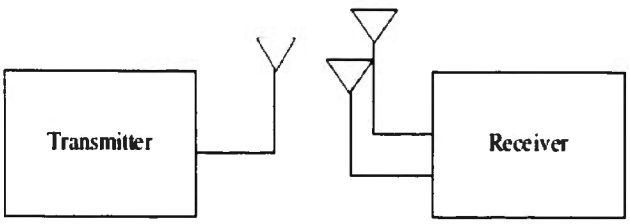


a) SISO System



b) MISO System

Figure 2.2 Different Types of Transmitter-receiver Set-ups



c) SIMO System

Figure 2.2 Different Types of Transmitter-receiver Set-ups (cont.)

Earlier designs of communication systems often focused on eliminating fading and interference, but the recent technology is more inclined towards better spectral efficiency and a low power budget [6]. This feature is exclusively provided by use of MIMO systems

2.3 MIMO SYSTEMS

This section introduces some important definitions associated with the work discussed later in the thesis. It defines some key concepts used in this work, outlines a background on how MIMO systems were introduced, and also describes its application on some of the complex communication engineering ventures. It also gives a brief description of the other approaches to communication systems, describes the challenges faced in those set-ups and finally introduces the MIMO technology.

2.3.1.Introduction. Significant improvements in capacity and bit error rates (BERs) have been a strong incentive for researchers to show more interest in multiple antenna systems, also termed multiple-input multiple-output (MIMO) systems [7]. MIMO wireless systems are those that have multiple antenna elements at both the transmitter and the receiver end [8]. MIMO systems have been known for their promising improvement in terms of performance and bandwidth efficiency [9].

The advantages of MIMO systems have been explored in many cellular technologies. Layered space-time (ST) receiver structure [7]-[9] and ST codes [13] make it possible to approach the channel capacity as revealed in [14] [15]. Commercial products working on same line are currently under development [15] [16].

A high-level block diagram for a MIMO-based communication system is illustrated in Figure 2.3.

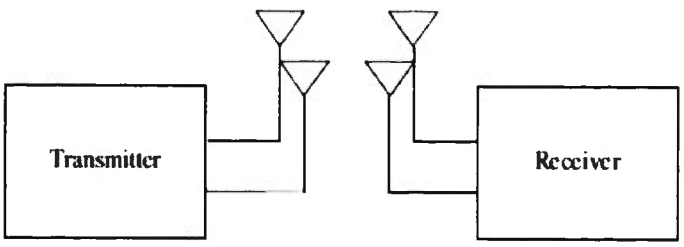


Figure 2.3 High-level Block Diagram for a Typical MIMO Communication System

It can be seen from the block diagram that the transmitter and the receiver ends are made up of multiple antennas which help MIMO systems dramatically increase the channel capacity in a fading environment [17]. These features have ensured that MIMO technology gets implemented in upcoming cellular technologies.

2.3.2.Background. The first set of ideas in the field of MIMO goes back to the work provided by A.R. Kaye and D.A George and W. van Etteh [18]. Jack Winters and Jack Salz who worked for Bell Laboratories have investigated beam forming [19]. These are considered some of the earlier works that laid foundation towards designing MIMO systems.

The concept of spatial multiplexing using MIMO systems was proposed by Arogyaswami Paulraj and Thomas Kailath [18]. Their research showed that the broadcast information capacity can be increased several-fold by this method [20]. Greg Raleigh and Gerard J. Foschini had found new approaches to the MIMO technology [10]-[14] which report that they conducted research on a Rayleigh fading environment under certain laboratory conditions[10]. These small steps in the MIMO technology ultimately helped Bell labs to demonstrate the first prototype of spatial multiplexing used to improve performance of MIMO systems [21].

2.3.3.Comparison with Related Technologies. MIMO systems have often been compared to SISO systems. It has been shown [17] that MIMO systems can support higher data rates at the same transmit power budget as SISO systems [22]. This signifies

that the transmission energy required to send a signal in MIMO systems is less as compared to energy required for SISO assuming same throughput requirements.

MIMO systems have also proved better than SISO systems in the field of cellular communication. It is shown that deployment of MIMO capable base stations can lower the site density required for achieving a certain necessary service compared to SISO deployment [23].

2.3.4.Applications of MIMO Systems. The performance of MIMO technology has made it an important part of modern communication systems. It is now an integral part of IEEE 802.11n (Wi-Fi) [24], 3GPP Long term-evolution (LTE) [1], Worldwide Interoperability for Microwave Access (WiMAX) [25] etc. These technologies can be described as follows:

1) Wi-Fi: This is an amendment to IEEE 802.11 standards that is capable of high throughputs and with a significant increase in the maximum data rate (≈ 600Mbits/sec) [26].

One of the major factors that ensures this high data rate is the use of spatial multiplexing, provided there are sufficient numbers of multiple-path reflections [27].

2) LTE: This is a project designed by 3rd Generation Partnership Project (3GPP). It is one of the approaches in cellular services to move forward as compared to the 3G services [1]. It is expected to improve the speed of data transfer and also improve the user experience with cellular technology [28].

Its performance requires physical layer technologies like Orthogonal Frequency Division Multiplexing (OFDM) and MIMO technology, which will help in increasing the data transfer rate by a significant value.

3) WiMAX: This is one of the technologies that enable wireless transmission of data packets at broadband data rate. It has been quoted as one of the 'future of data transmission' by many industrial analysts [25].

The significance of MIMO technology in WiMAX is the use of multiple antennas at the transmitter end and use of a multiple antenna in the cell phones too which will improve the reception of the signals.

2.3.5.Challenges in Using MIMO Systems. MIMO systems offer many benefits but at a cost. The challenges in using MIMO include:

1) Increased circuit complexity: As this technology needs multiple antennas at both the transmitter and the receiver ends, it requires added circuitry to produce the signals that are to be transmitted and also to decode or demodulate the signal (if the transmitted signal is modulated) at the receivers end.

2) Higher energy consumption: Circuit energy consumption involves energy consumed by all the circuit blocks along the signal path: Analog to Digital Converter (A/D Converter), Digital to Analog Converter (D/A Converter), Frequency Synthesizer, Mixer, Lower Noise Amplifier (LNA), Power Amplifier and baseband DSP [22]. This problem can dominate MIMO systems as compared to SISO systems. It has been shown in [22] that in short range application when data rate and the modulation schemes are fixed, SISO may show higher energy efficiency compared to MIMO systems.

3) Other challenges: The other major hurdles faced by MIMO systems can be given as follows:

i. Inter-modulation from other signals: The front ends of a communication system often have a large band-width so that it can capture the signal effectively. But if the receiver is somewhere near a cell-phone tower or some other signal sources, it's possible that the signals from the cell-phone towers can interfere with the message signal. This problem is pretty dominant in MIMO systems because the error induced gets multiplied due to the use of multiple antennas at the receivers end.

ii. Multipath fading: In wireless communication system, signals are often transmitted in all direction and in MIMO systems 'multipath propagation' is often used to increase the capacity of the channel [29]. At times this also leads to changes in the relative path lengths [29]. This happens basically because of some changes in the position of the reflective surface considering that the transmitter and the receiver positions are fixed. This leads to phase changes or even reduction in the power of the transmitted signal, thus resulting in fading.

iii. Receiver overload: This problem is associated with inter-modulation from other signals. If the undesired signal received at the receiver has a strong RF, it may result in the saturation of the transistors hence reducing the sensitivity of the receivers [30].

iv. Maintaining sync between the produced signals: Use of multiple antennas at the transmitter end requires use of different hardware models to produce the signals. It is highly important to maintain a perfect sync between these signals which requires additional hardware, thus leading to a further increase in the complexity of the system.

v. Non-linearity of power amplifiers and finite bit-precision of A/D and D/A converters: This leads to presence of additional interference both in frequency bands of the transmitter and receiver [31].

vi. General RF Noise: These can be produced by any radio equipment in the vicinity of the communication system. Some of the sources for these RF noises can be electric welders, brush-type motors, relays and switches of all kinds, fluorescent lights, TV etc.

vii. Cost: MIMO systems require additional hardware to produce desired signals which leads to a drastic increase in the cost of the built system.

3. SYSTEM ARCHITECTURE

This section introduces some important definitions and illustrations to define and explain typical system architecture for communication systems.

3.1. DEFINITION

It can be defined as a conceptual model which provides high-level information that defines the basic functionalities of various blocks of the system and also gives an overview of their performance.

3.2. DIGITAL COMMUNICATION SYSTEM

Figure 3.1 gives the system architecture for a typical digital communication system and illustrates the signal flow and signal processing steps on the signal path. The communication system can be divided into three different parts:

3.2.1.Transmitter. The functionality of the different blocks of the transmitter can be defined as the following:

1) Data: This is the source of information that is to be transmitted through the wireless channel. It can be a voice signal, a video signal, an image, a data file or command or control data [32].

2) Source Encoder: This block involves digitization of the analog data. The term source coding has taken a connotation of data compression in addition to data digitization [5]. It processes the input data and converts them into a sequence of information bits. The main functionality of the encoder is to remove the unstructured redundancy from the data to reduce the transmitted data rate, resulting in a reduced complexity [32]. Source encoding can be done by predictive coding, block coding, variable length coding etc.

3) Channel Encoder: This block is used for channel coding also termed as error correction coding. This block is used to convert the information bits produced by the source encoder into channel symbols, which can be a single bit or a sequence of bit. This is done to protect the data from distortion and noise from the channel. Sequences of such symbols are also termed bit-streams.

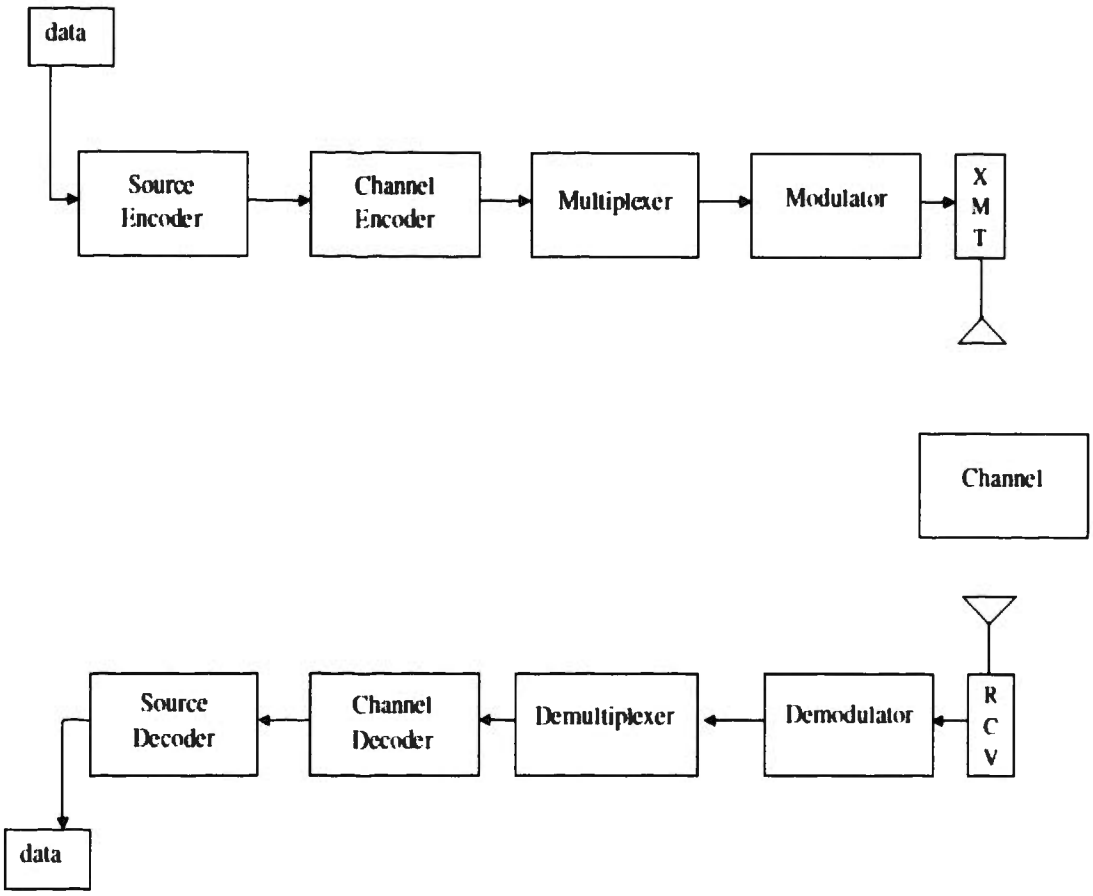


Figure 3.1 Block Diagram of a Typical Digital Communication System

4) Multiplexer: This block is used to transmit multiple data produced by same/different sources into a single line. The basic use of this is to make the system cost effective by transmitting large number of data through the same communication channel.

5) Modulator: This block is used for modulation of the channel symbol. Modulation can be defined as converting a sequence of data into suitable formats to make them compatible with specifications of a system [5]. Different types of modulation like Amplitude Modulation (AM), Frequency Modulation (FM) and Phase Modulation (PM) can be used as per the requirement of the application for the communication system.

3.2.2.Communication Channel. The channel is the medium used to transmit signals from the transmitter to the receiver. It can be a pair of wires, a coaxial cable, a band of radio frequencies, etc [33]. In wireless communication systems, band of radio frequencies are used for communication.

3.2.3.Receiver. The functionality of the different blocks of the receiver can be defined as follows:

1) Demodulator: This is the process of extracting the original signal i.e. separating the carrier signal from the original signal [14][34].

2) De-multiplexer: The multiplexer and de-multiplexer units are used to reduce the complexity and simultaneously the cost of the built system by providing an ability to send multiple signals from different sources through the channel.

3) Channel Decoder: This is used to extract the channel symbols out of the demodulated signal.

4) Source Decoder: This block is used to decode the channel symbols to extract the information signal or the message signal from it.

This summarizes the system architecture for a typical digital communication system.

4. VARIOUS APPROACHES

The message signals to be transmitted can be generated using different approaches. Each of these approaches has features which best suit specific applications. The approach is selected based on the application and technical specifications. This section provides a brief summary of three approaches that can be used.

4.1 FIELD-PROGRAMMABLE GATE ARRAYS (FPGAs)

Recent development in the field-programmable devices has changed the process of hardware designing. Board designs of today are made up of these high-density devices as compared to the large number of basic gates used in the older designs [35].

4.1.1.Definition. FPGAs are integrated circuits that are designed and configured based on the application requirements. They are often used to design prototypes for Application-specific Integrated Circuit (ASIC) designs or to implement hardware designs based on new algorithms [36]. Today FPGAs come with millions of basic gates integrated into them, thus making them efficient enough for many applications including communication devices, software-defined radios, radar, image and also other DSP operations [36].

They are made up of logic cells which can be configured using a set of on-board connections which can be programmed when the chip is powered up [37]. These cells are used for a variety of low-level functions, which can also be programmed. Typically FPGAs have an ability to generate high data rates hence are used for many DSP applications.

4.1.2.System Blocks. FPGAs as stated earlier have the ability to generate high-data speeds and hence are used in communication systems. Figure 4.1 gives the functional block diagram for an FPGA based MIMO system.

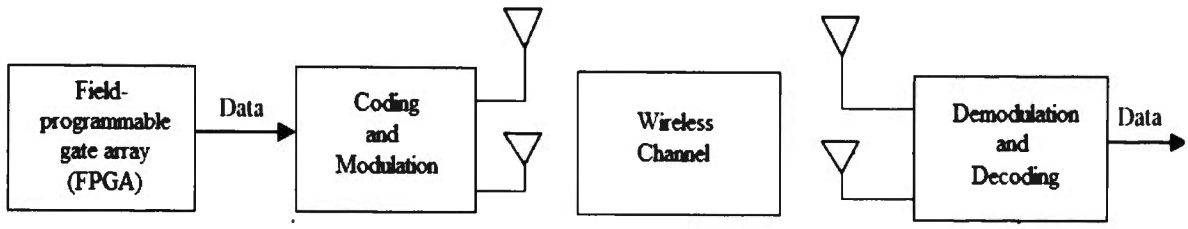


Figure 4.1 FPGA Based 2x2 MIMO System [37]
(© 2009 by ITC. Used by permission)

The FPGA-based MIMO system is basically made up of three parts:

1) Transmitter End: The transmitter end is made up of the FPGA processor which is used to produce the signal which is then forwarded to the coding and modulation unit. The FPGA is used because it provides a theoretical processing capability far excess of a DSP [38].

2) Communication Channel: The wireless communication channel is used for the transmission of the signal. The various problems encountered by the signal while being transmitted through the wireless channel were explained in section 3.

3) Receiver: The receiver has a series of demodulating and decoding units. The demodulating unit is required to separate the carrier signal off from the original signal and the decoding unit is needed to extract back the original signal from the demodulated signal.

4.1.3.Features of this Approach. The various advantages in using the FPGA as a signal producing unit can be cited as follows:

1) Higher Data-rates: The use of an FPGA creates an opportunity to speed up a DSP application [37]. The capability of the FPGA to produce high data-rates can be explored and used in the field of communications.

2) Higher throughput: They have a high throughput advantage over a number of high-performance microcontroller and DSP processors for certain types of applications.

3) High flexibility and reusability: The reprogramming ability provided FPGAs has made them flexible and reusable depending on the kind of application [39]. Due to this, the FPGA hardware can be modified throughout the design cycle [40].

4) Allows integration of soft-core processors: Current high-end FPGAs provide integration to soft-core processors which signifies that the FPGA now employ typical processor capabilities [39].

5) Other advantages: Research and development in the field of FPGAs has grown in the last few years and many advantages of DSP and ASIC have been added to it. This includes rapid development cycles, moderate cost and easy upgrading. The easy upgrading is based on the fact of using the abstract hardware description language (HDL). The other advantage is the visibility of the FPGA, which means that the internal state for many FPGA's are directly accessible. This capability helps to verify designs and to track and fix bugs in any system [40].

4.1.4.Challenges in Using this Approach. The above advantages make the FPGA seem attractive for a number of DSP processes, but using an FPGA has its own hurdles:

1) Large amount of time for redesigning as compared to the other approaches: The FPGA needs a large amount of time and efforts to configure and redesign computer architecture for a new or a different algorithm [41]. The construction of a computational structure suiting the demands of the application is the first step. The next step is to create the design which is done using hardware-description language at register-transfer level (RTL)[42]. This shows that implementation of a certain algorithm takes lots more effort and time using an FPGA

2) Constraint on the number of logic operations on an FPGA: This is one of the primary challenges of using FPGAs. It only allows implementation of a limited number of logic operations on a particular device [43].

3) Limited signal routing options: FPGAs normally offer limited number of signal routing options for connecting logical operators to the arrays [43].

4) Low energy efficiency and high cost: Having an energy efficient processor is one of the most important criteria for any DSP application. As discussed in the advantages, FPGAs are very flexible, but this flexibility comes with a disadvantage. More flexibility stands for more number of gates, more silicon area, more routing resources and thus higher energy consumption and higher cost [37].

4.2 DSP PROCESSORS

A digital signal processor (DSP) is a device with an optimized architecture that helps it to perform many DSP operations effectively [44] [45]. The use of DSP chips has shown a significant increase in applications where their speed and numerical processing ability proved to be a blessing [46].

4.2.1.System Blocks. Digital signal processors as stated above have an incredible speed and have a very high numerical processing speed; hence they are used in some DSP application. Figure 4.2 gives the functional block diagram for a DSP based MIMO system.

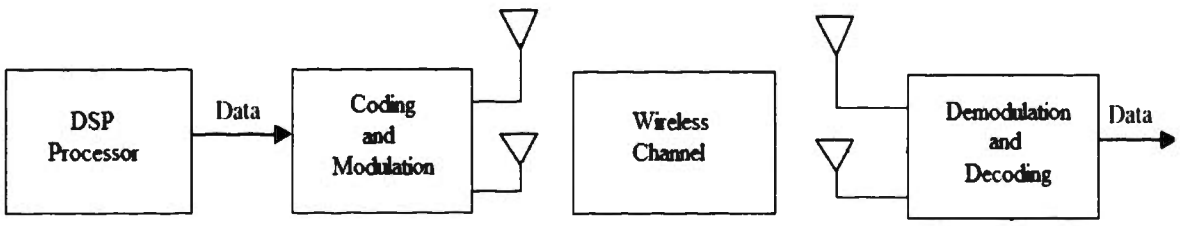


Figure 4.2 DSP Based 2x2 MIMO System

Figure 4.2 illustrated that a DSP processor is being used for producing the signal to be transmitted. The coding and the modulation block is used to provides means of mapping information into the message signal such that the receiver, using appropriate decoder and demodulator can retrieve back the sent message in a reliable manner.

The DSP-based MIMO system works on the same principle as a FPGA-based system but with some differences. The differences being the various advantages and hurdles the user faces while using either of the approaches.

4.2.2.Features of this Approach. DSP processors have been traditionally considered very effective for some DSP processes due to the following advantages:

1) Fast multiply-accumulate operation: The most important advantage cited for DSP processor is their ability to perform multiple-accumulate operation in a single instruction cycle. To help the DSP processors in performing this, it has a multiplier and an accumulator built in the arithmetic processing unit [47]. This feature has found a lot of importance in those applications which require fast processing or many multiplication operations like digital filter operations etc.

2) Multiple–access to the memory: DSP processors have an ability to make several accesses in a single instruction cycle. This helps them to speed up the process and also execute multiple instructions in a single cycle making them attractive for many DSP applications needing high execution speed.

3) Specialized addressing modes and program control: To reduce the execution time, DSP processors have dedicated address generation units. Once the appropriate address registers are configured, the address generation unit operates in the background. It produces the operands required parallel to the arithmetic operations [48]. This speeds up the overall processing ability of a DSP processor.

4) Peripherals and I/O interfaces: In order to provide high-performance input/outputs, most DSP processors provide a strong I/O interface. This allows it to be perfectly aligned with external devices like the A/D converter and D/A converter.

4.2.3.Challenges in Using this Approach. The use of the DSP approach has its own hurdles:

1) Higher power consumption: DSP processors have an ability to execute multiple instructions in a single clock cycle. This feature may reduce the execution time of the DSP processor, but this also means that the operation often consumes more power than a microcontroller.

2) Technical challenges: Software has been one of the clear weak spots in DSP processor technology. This includes developmental tools as well as software support required for optimum performance of the DSP processors [49]. The most important disadvantage is the unavailability of some sophisticated tools that can help in software optimization and debugging. Certain simple requirements such as displaying graphical data, analyzing them etc cannot be performed due to the lack of these tools.

3) Other challenges: DSP processors are used for implementing a mixture of normal algorithms as well as some other repetitive types of algorithms like vector dot products (can be used for FIR filter implementation). Some of the DSP processors try doing the vector product one clock cycle per element. Due to this, the DSP processors have most of their focus on the highly repetitive actions and some important interrupts are not attended. This is one of the important challenges faced by some of the DSP systems which are more inclined towards performing continuous arithmetic processes.

4.3 MICROCONTROLLERS

The advancements in the field of DSP world have made manufacturers add additional features into the general purpose microcontrollers which make them very attractive for many DSP applications.

A typical microcontroller cannot be used as a standalone-processor which means that it is connected to many external processes. A microcontroller analyzes the input and reacts based on the software code it is programmed with [50].

4.3.1.System Blocks. The block diagram for the Microcontroller based MIMO system is given in Figure 4.3:

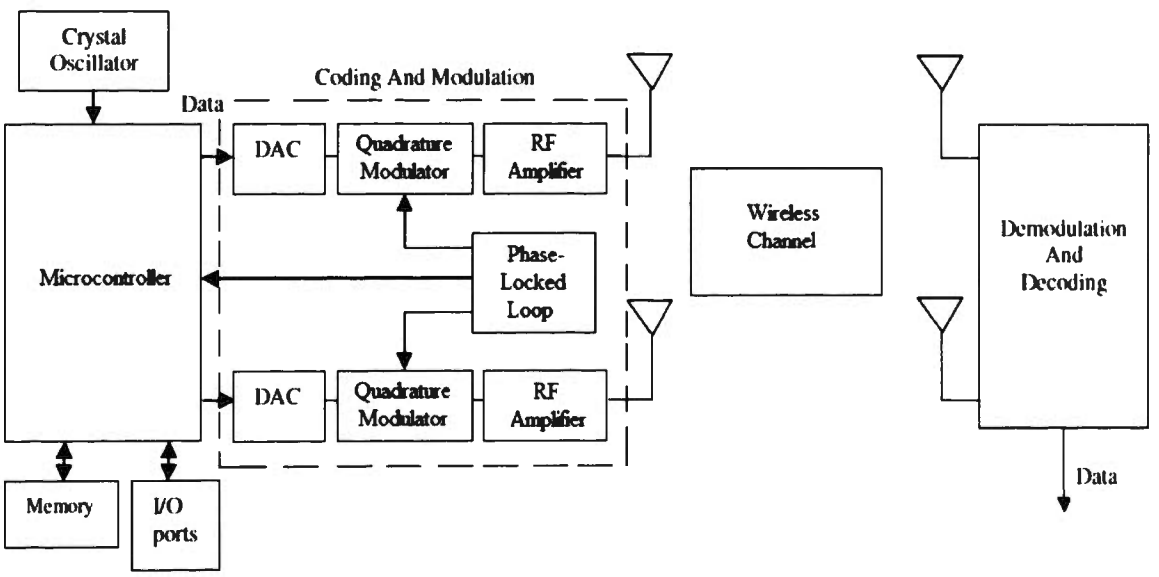


Figure 4.3 Microcontroller Based MIMO system [37]
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The functionality of the above figure can be explained on the same lines as FPGA and DSP, but it can be seen that the microcontroller itself is connected to a lot of external chips. This helps it to undertake multiple functions at the same time, which is one of the features that has helped it succeed in the field of communications.

4.3.2.Features of this Approach. The various advantages of a typical microcontroller can be given as follows:

1) Lower power consumption and low cost: It is found that DSP processors execute multiple instructions within a single cock cycle and hence they consume more power. The FPGA has flexibility, but this comes at the cost of higher power

consumption. Microcontrollers, however, offer most features of a DSP processor and still consume lower power. The reusability of the microcontroller is motivated by its programming ability; hence it works at a better power budget than an FPGA for most application [51].

2) General-purpose device: One of the most important features of the microcontroller is that it can be used for a variety of applications like computing, image processing, etc. [52]. Microcontrollers, as defined earlier, are always connected to external devices. This gives them an ability to perform a number of applications at the same time which is termed as *Multiplexing.*

3) Reusability: Microcontrollers are programmable device, which means that they can be used to execute functions as defined by the user and the application.

4) Input/ Output ports: These are the buffers and latches that are used to interface peripheral devices. The availability of the input/output ports makes it easier for the controller to communicate to the externally connected devices.

4.3.3.Challenges in Using this Approach. The primary disadvantage of the microcontroller-based approach is the inability of the microcontroller to produce higher date rates at the output, thus making them unsuitable for applications which require transmission of data at higher rates.

Recent developments in the field of microcontrollers are slowly and steadily bridging the gap between microcontrollers and other high-speed processors and the future looks bright for their use in the applications requiring higher data rates.

5. DYNAMIC POWER CONSUMPTION OF FPGAs

The power consumption in FPGAs is of two basic types: static and dynamic. The static power consumption occurs as a result of leakage current, which may be due to two major sources: reverse-biased PN junction and sub-threshold channel conduction [53]. This section basically gives a brief idea of how the dynamic power of the FPGA is calculated and also takes into consideration some FPGAs for analysis.

5.1 DEFINITION

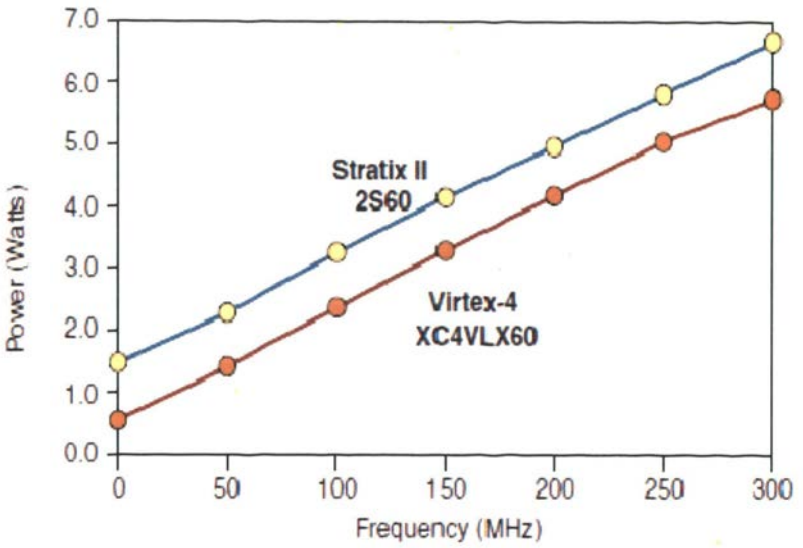
Dynamic power can be defined as the power required to charge and discharge the capacitive loads within a device [54]. Thus, at high frequencies the rate of signal transitions are more frequent and hence is the total dynamic power consumption. This can be illustrated by:

$$P = \sum_i C_i V_i^2 f_i \quad (55)$$

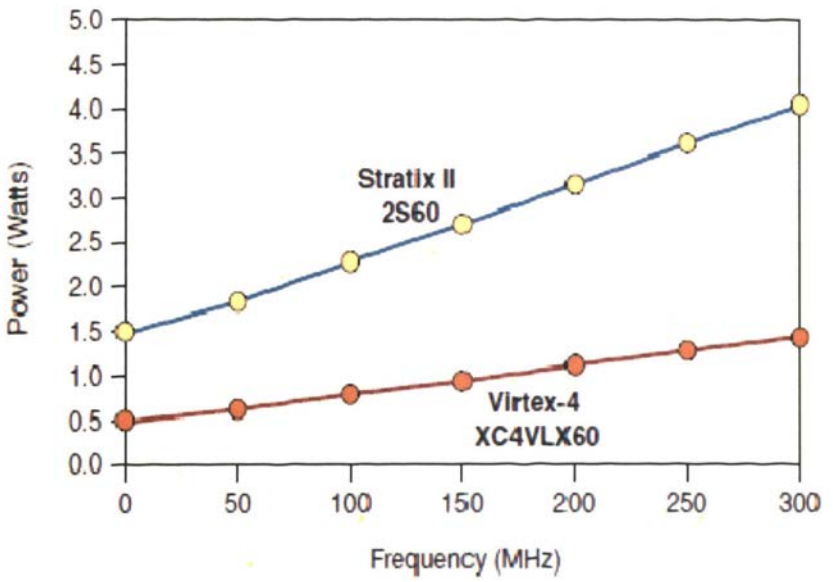
Where C_i,V_i and f_i are the capacitances, voltage swing, and operating frequency of resource i, respectively [56]. It is often seen that the dynamic power consumption is a larger contributor to the total power consumption [54]. The next section considers some FPGAs for analysis.

5.2 ANALYSIS OF FPGAs

The graphs in Figure 5.1 illustrate the dynamic power dissipation for Virtex-4 and Stratix-II for different tests.

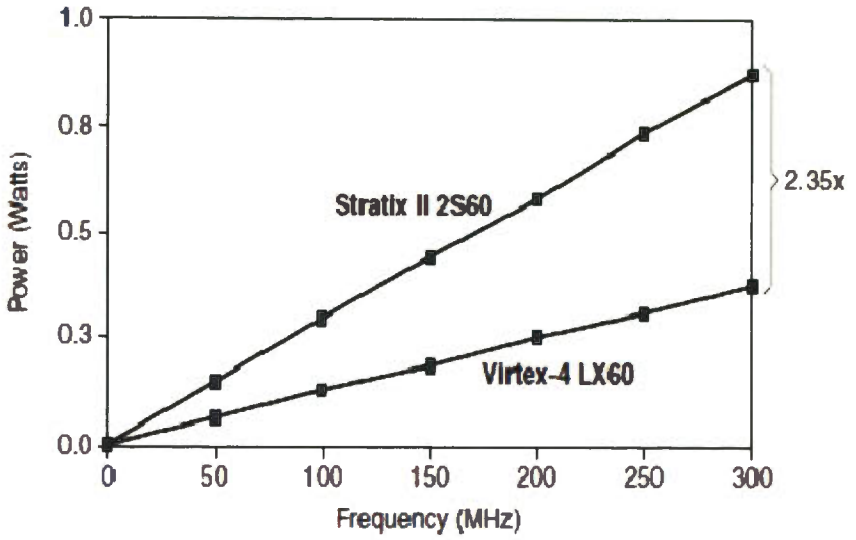


a) Dynamic Power: Fabric Test with 25,000 LUT/ALUTs and 21,000 FFs (High Toggle Rate). All measurements were taken at Tj = 85°C.

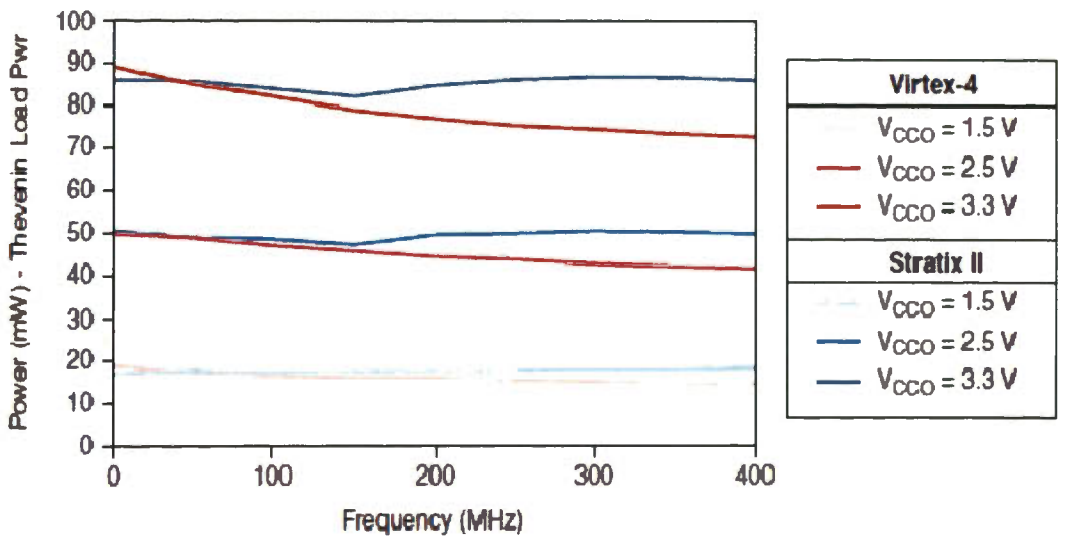


b) Dynamic Power :Memory using FIFO/Block RAM test with 252 M4K in Stratix II and 63 Block RAM in Virtex-4FPGAs (same total storage).
All measurements were taken at Tj = 85° C.

Figure 5.1 Dynamic Power Consumption of Virtex-4 and Stratix-II for Different Tests[57]



c) Dynamic Power: DSP test: 64-tap FIR filter



d) Dynamic Power at all three VCCIO voltages

Figure 5.1 Dynamic Power Consumption of Virtex-4 and Stratix-II for Different Tests[57] (cont.)

It can be inferred from Figure 5.1 that the considered FPGAs consume large dynamic power for most of the above tests. Specifically for the fabric test, it can be seen that the both the FPGAs consume 6-7 Watts of power, which is considered pretty high for most DSP applications. Figure 5.2 gives a brief summary about the total power dissipation of Stratix-II and Virtex-4.

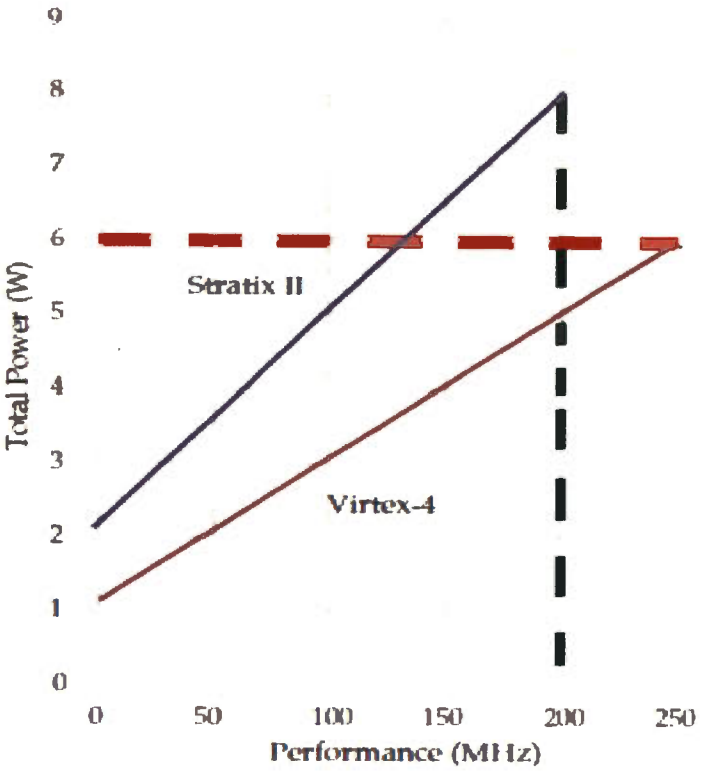


Figure 5.2 Total Power Consumption for Virtex-4 and Stratix-II [57]

In Figure 5.2 total power consumption for Stratix-II is found to be ≈8W and that for Virtex-4 is found to be approximately 5W. Thus from these values it is clear that dynamic power consumption plays an important role in deciding the total power consumption of the system.

Recent developments in the field of chip design have come-up with ideas that can reduce the total dynamic power consumption. But at the present time, it remains one of the major parameters that are to be considered before opting for an FPGA design.

6. SELECTION OF THE APPROACH

The MIMO system this paper discusses is specifically designed for those applications requiring the following specifications:

1) Low power consumption

2) Low cost

Based on the features of all the approaches discussed in Section 4, the microcontroller is selected over FPGA and DSP processors due to the requirements of the project.

7. HIGH-LEVEL BLOCK DIAGRAM DESCRIPTION

The high-level block diagram of the considered approach can be illustrated by Figure 7.1:

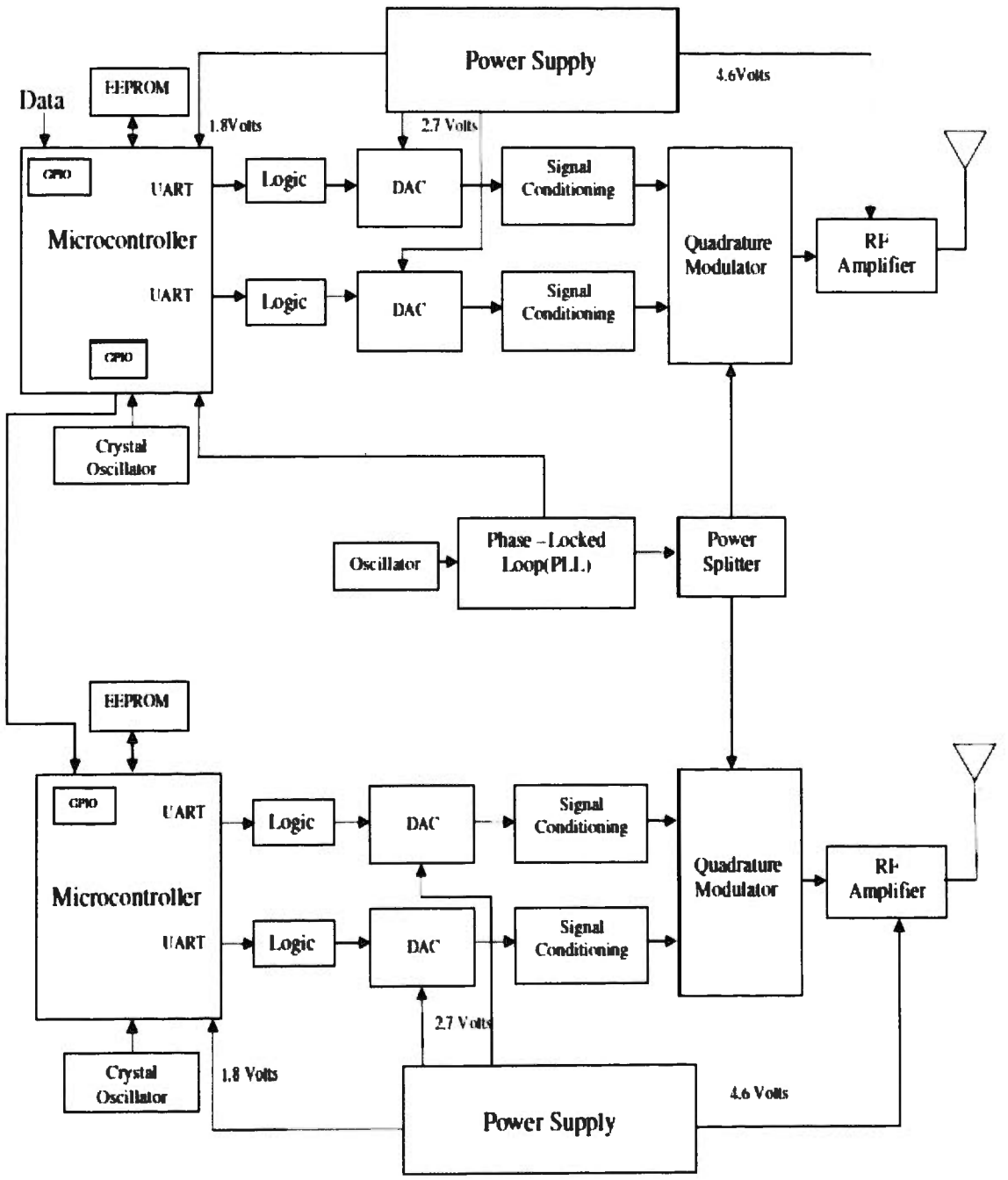


Figure 7.1 High-level Block Diagram for a Microcontroller Based MIMO Transmitter [37]

The various parts of the above diagram as be explained as below:

7.1. MICROCONTROLLER

Microcontrollers can be considered as a small computer designed on a single integrated circuit along with support devices like processor, memory and peripherals [58]. It may also include other support devices like A/D converters and serial I/O ports. In practical systems, the microcontroller is found to be a part of the system used to undertake specific functions related to the application.

Figure 7.2 illustrates the internal block diagram of a typical microcontroller and the blocks are explained in the corresponding sub-topics.

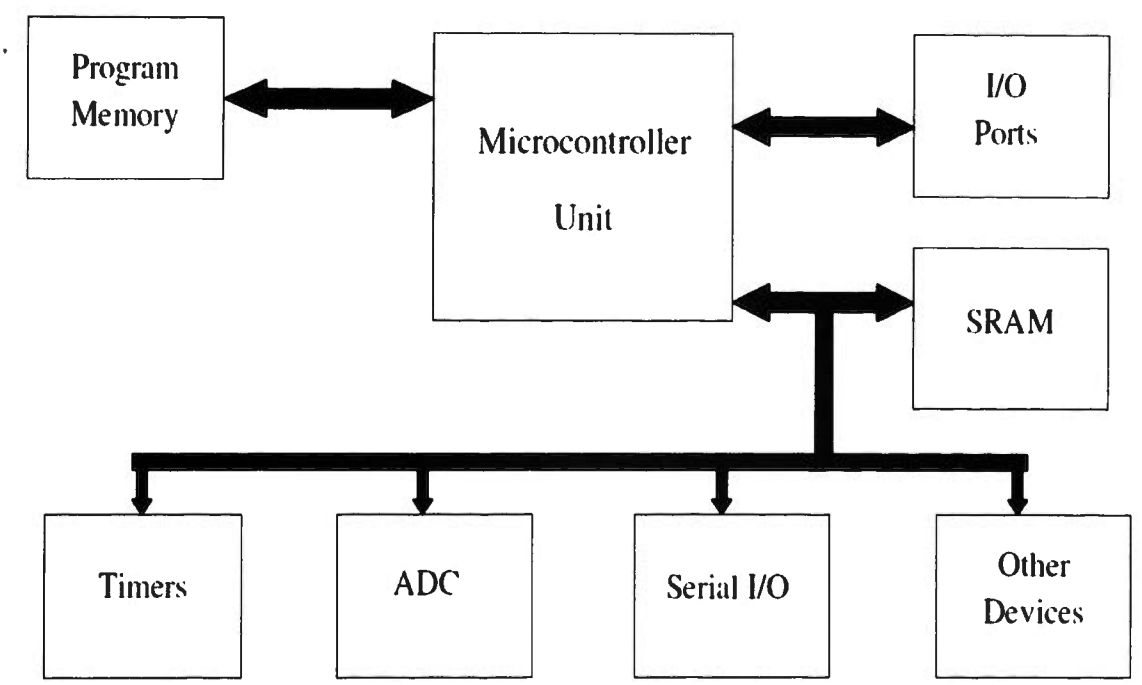


Figure 7.2 Block-diagram –microcontroller

7.1.1.Microprocessor. The Microprocessor Unit (MPU) unit is considered to be its brain of the microcontroller. Every MPU has three units as illustrated by Figure 7.3 and described as follows:

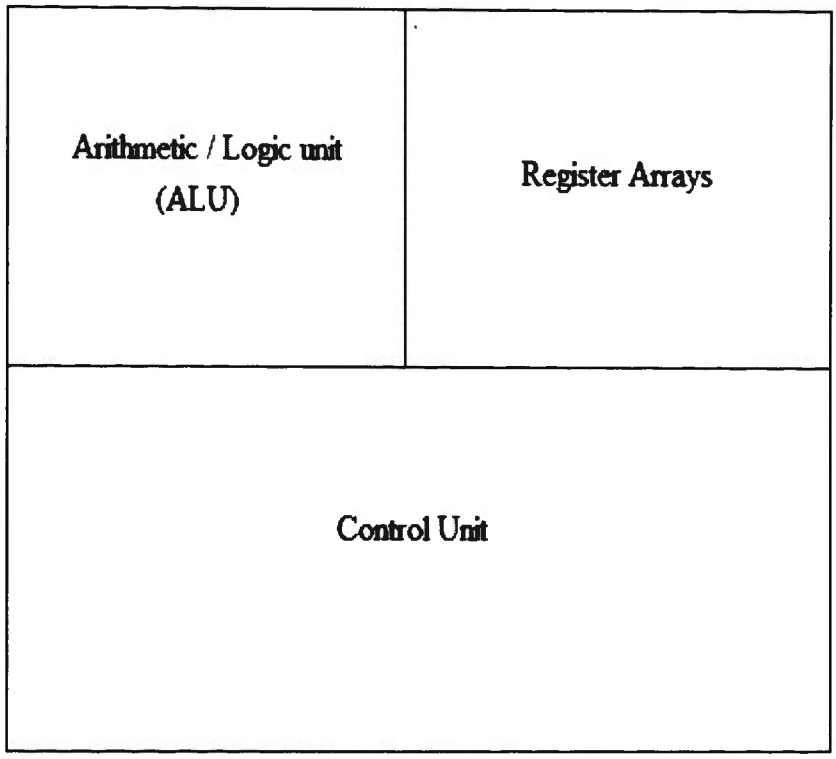


Figure 7.3 Block-diagram –microprocessor (MPU) Unit

Control Unit: This the main part of the MPU unit which is used for processing the instructions provided to it and enabling the connected devices to work according to the application [59].

Arithmetic / Logic Unit (ALU): This unit of the microcontroller is used to perform arithmetic and logic operation like addition, multiplication, performing AND / OR/ XOR operations etc

Register Arrays: The various registers are either used for storing data temporarily or permanently.

7.1.2.Memory. This is one of the integral parts of the microcontroller. It is basically used to store both instructions and data [52]. Modern day microcontroller comes with very large internal integrated memories which help it to perform faster and hold more data. An external memory can also be interfaced with a microcontroller to improve its performance and also ability to process long instructions and also long-stream of data.

7.1.3.Input/output (I/O) Devices. External input/ output peripheral devices can be connected to a microcontroller. Input devices include switches and keyboards. Output devices could be LCD devices, light-emitting diodes (LED's) etc.

7.1.4.Bus. The bus is used for transmission of data between various units of a microcontroller. Typically, buses are of three different types data bus, address bus and control bus.

7.1.5.Crystal Oscillator. A typical microcontroller works based on a primary clock input. A precise clock frequency is used and a proper gating is done and then supplied to the rest of the system [37].

7.1.6.Direct Memory Access (DMA) Controller. This is one feature which helps the microcontroller to use the system memory to read/write independent of the main memory [37]. It can thus, transfer streams of data from the buffer storage directly to the main memory without interference from the CPU [60].

The DMA controller is connected to the outside world via pins like UART (Universal Asynchronous Receiver/Transmitter), USB interfaces, etc., which are serial input/output pins. The microcontroller is programmed in such a way that the DMA is provided control over the buses for a limited period of time, during which it processes the data and transfers them to its external pins like UART which further is transferred to the D/A converter [37].

7.1.7.Supporting Devices. Advanced microcontrollers also have many supporting devices like timers, in-built A/D and D/A converter, direct memory access (DMA) controllers etc. These extra features have made microcontroller one of the best choices for many applications.

7.1.8.Technical Specifications Required for the Selected Microcontroller. The microcontroller selected requires a power supply of 1.8 Volts, a crystal oscillator and has an ability to generate data rates up to 200 MHz

7.2. D/A CONVERTER

The data that is to be transmitted is generated by the microcontroller and sent to the UART pins. This data is digital in nature and needs to be converted into an analog signal before transmission. The selection of the D/A converter is done not only based on its performance but also its power consumption. The low power consumption of the selected D/A is one of the additional features which makes it ideal for the application. Figure 7.4 illustrates the pin diagram for the selected D/A converter.

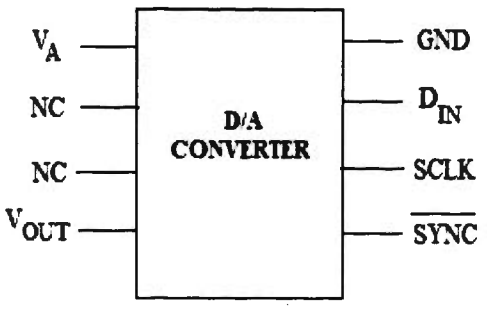


Figure 7.4 Pin Diagram of D/A Converter

The digital data from the microcontroller (UART) comes toD_{IN}. The digital signal is then converted into an analog signal and sent to V_{OUT} pin. V_A(2.7 Volts) is the voltage required by the D/A converter to function. The other pins of the D/A can be defined as follows:

1) SCLK: This is a serial clock input. Data is clocked to an internal shift register on the falling edge of this pin.

2) $\overline{SYNC}$: This is a frame synchronization input for the data input. When this pin goes low it enables the input shift register and the data is transferred at every falling edge of SCLK.

7.3. LOGIC BLOCK

The D/A requires SCLK, $\overline{SYNC}$ along with the digital data. The data from the DAC is at a very high frequency (≈ 10MHz), so a perfect precision is required while extraction of SCLK and $\overline{SYNC}$ signals.

These two signals need to be extracted by a logic block and the high-level block diagram for the logic block used to generate the desired signals using the microcontroller generated data bits is shown in Figure 7.5.

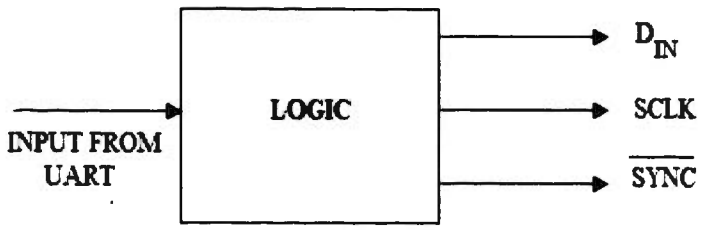


Figure 7.5 Logic Block Diagram

7.4. QUADRATURE MODULATOR

The quadrature modulator is used to modulate message signals (analog or digital) with carrier signals used for radio communications [29]. A typical quadrature modulator is basically made of a mixer, a summation block and a phase shifter [61]. In its application with MIMO system it is used on analog signals. It basically transmits two analog signals by modulating the amplitude of two carrier signals which are out of phase by Amplitude Modulation (AM) [37]. Figure 7.6 illustrates the block diagram of the quadrature modulator.

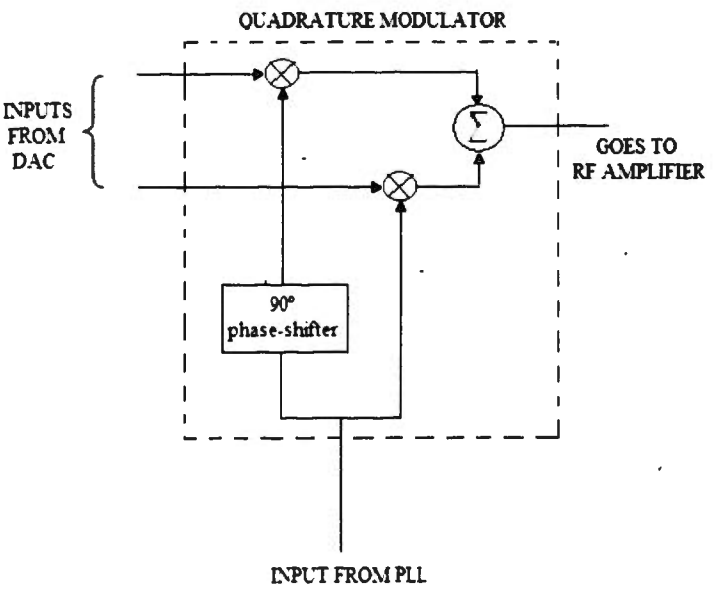


Figure 7.6 Block Diagram of Quadrature Modulator [37]
(© 2009 by ITC. Used by permission)

The analog signals from the DAC are used as the message signal which is then modulated by the phase-shifted carrier signals provided by the Phase-locked Loop (PLL). One of the signals is used directly and the other is phase shifted by 90°.

7.5. SIGNAL CONDITIONING

Signal conditioning is a technique used to manipulate signals in order to make them more compatible with the next stage [62]. This can include filtering, pulse shaping, amplification, pulse clipping, etc. This stage is used to make changes in the analog signal in order to meet the requirements of the system.

7.6. PHASE-LOCKED LOOP

The phase-locked loop is used to generate signals whose phase is proportional to the input signal, also referred to as the reference signal. Thus the designer has some control over variation of the output signal with reference to the inputs signal and this ability is sometimes beneficial in reducing the effect of noise on the reference signal [63].

In Figure 7.1, the PLL is used to generate the carrier signals which are used by the quadrature modulator to modulate the message signals. It is also connected to the microcontroller to ensure perfect synchronization between the two [37].

7.7. POWER SPLITTER

The power-splitter at the rear end of the PLL is used to split the output of the PLL into two equal parts which are further provided to the quadrature modulator.

7.8. RF AMPLIFIER

This block is used to amplify any low-power signal to a comparatively higher signal for driving the antenna at the MIMO transmitter end. This helps the signal to get transmitted across long distances. The added features of the RF amplifier are the high efficiency, high output power, high gain and decent power dissipation [37].

7.9. POWER SUPPLY

The power supply block is used to supply the required power to all the circuit. It is used to power the microcontroller (1.8Volts), D/A Converter (2.7 Volts) and the RF amplifier (4.6 Volts).

8. DISCUSSION AND CONCLUSIONS

The power of MIMO-based system has been in the limelight since its inception. It provides a scope to enhance certain features of the other set-ups like SISO, SIMO and MISO by introducing the ability to increase data-rate and throughput. MIMO systems have been used in the field of cellular technologies to utilize the above mentioned strengths to improve user experience with telecommunications. Additionally, designing a MIMO system demands different modeling approaches that can be selected based on the type of application and user requirements. This paper discusses different approaches that can be used to build a MIMO transmitter model and describes one of the approaches in detail which is selected based on the application requirement.

As an approach, use of FPGA or DSP processor has gained attention for both their feature as well as their limitations. FPGAs have the ability to offer high data rates, high throughput and high flexibility and reusability. In addition to this, current high-end FPGAs also provide integration to soft-core processors which signifies that they now have all the typical features of a processor [39]. However, these features come with some challenges like low energy efficiency, large time requirements for redesigning and also constraints on the number of logic operations that can be performed on a single FPGA. On similar grounds DSP processors offer fast multiple-accumulate operations, specialized addressing modes and also peripheral devices. But it consumes much more power than general-purpose microcontrollers and the support provided for DSP processors in terms of software and also other tools is not up to mark. These inabilities of FPGA and DSP processors do not make them attractive for the application selected. The application taken into consideration is specifically designed for a system requiring the following specifications:

- Low power consumption
- Low cost

These features are not provided by either of the above described approaches, hence we opt to use the microcontroller-based approach. In addition to these features, microcontrollers also provide other features like reusability, multitasking and also ability

to interface peripheral devices and perform complimentary functions along with signal generation. The only disadvantage found in this approach is the inability of the microcontroller to generate high-speed data. However, this work does not place any constraint on the data rate because the application pertains to work with low data rates; hence this disadvantage can be ignored.

The objectives accomplished in this research demonstrate our efforts towards understanding different approaches, their features and limitations, and work towards a high-level understanding of the microcontroller based MIMO transmitter system. The model discussed illustrates an insight into the different parts of the design and also their functionality towards making this approach ideal for the selected application.

The next step in this research will be to develop a hardware-based model and monitor its performance in a normal environment. An integration of this kind will provide a better picture of the intensity of certain problems faced by MIMO systems like multipath reflections, fading, non-linearity of power amplifiers,etc. Sorting out these problems while working in a closed environment may be the next step. Once these problems are sorted out, integrating compact designs of the microcontroller-based system onto certain applications like missile systems can help in testing the performance of the system in an open environment, which would further help us analyze the effects of changing environments on the built system.

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